



(51) **International Patent Classification:**
G06F 11/08 (2006.01) **G06F 12/00** (2006.01)
G06F 13/14 (2006.01)

(21) **International Application Number:**
PCT/US2009/056467

(22) **International Filing Date:**
10 September 2009 (10.09.2009)

(25) **Filing Language:** English

(26) **Publication Language:** English

(71) **Applicant** (for all designated States except US):
HEWLETT-PACKARD DEVELOPMENT COMPANY, L.P. [US/US]; 11445 Compaq Center Drive W., Houston, Texas 77070 (US).

(72) **Inventors; and**

(75) **Inventors/Applicants** (for US only): **EMERSON, Theodore, F.** [US/US]; 11445 Compaq Center Drive W., Houston, Texas 77070 (US). **HEINRICH, David, F.** [US/US]; 11445 Compaq Center Drive W., Houston, Texas 77070 (US). **LE, Hung, Q.** [US/US]; 11445 Compaq Center Drive W., Houston, Texas 77070 (US).

(74) **Agents:** **WEBB, Steven, L.** et al.; Hewlett-Packard Development Company, L.P., Intellectual Property Administration, Mail Stop 35, P.O. Box 272400, Fort Collins, Colorado 80527-2400 (US).

(81) **Designated States** (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PE, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) **Designated States** (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Declarations under Rule 4.17:

- as to the identity of the inventor (Rule 4.17(i))
- as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))

[Continued on next page]

(54) **Title:** MEMORY SUBSYSTEM HAVING A FIRST PORTION TO STORE DATA WITH ERROR CORRECTION CODE INFORMATION AND A SECOND PORTION TO STORE DATA WITHOUT ERROR CORRECTION CODE INFORMATION

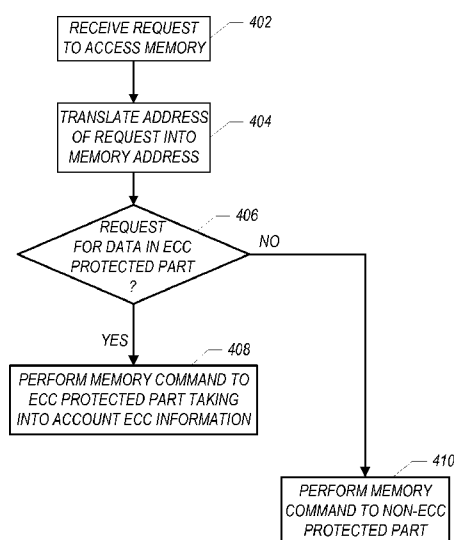


FIG. 4

(57) **Abstract:** A system comprising a memory subsystem having at least one memory device, and a memory controller to control access of the memory subsystem, wherein the memory controller is configured to store data with error correction code (ECC) information in a first portion of the memory subsystem, and to store data without ECC information in a second portion of the memory subsystem.

WO 2011/031260 A1



Published:

— *with international search report (Art. 21(3))*

- 1 -

Memory Subsystem Having A First Portion To Store
Data With Error Correction Code Information And A Second
Portion To Store Data Without Error Correction Code Information

Background

[0001] An electronic device such as a computer employs a memory subsystem having one or more memory devices. In some cases, the memory subsystem can be configured to store data with error correction code (ECC) information such that certain types of errors in the data can be detected and corrected. The ECC information be used to provide protection against errors in the data of up to a predefined number of bits.

[0002] An issue associated with using ECC protection for data stored in a memory subsystem is that ECC information can take up a substantial portion of storage capacity. For every collection of data bits of a certain length (*e.g.*, a byte), corresponding ECC information is stored. For example, for every byte of data, the accompanying ECC information can take up 5 or 6 bits. As a result, when ECC protection is used, the available storage capacity of a memory subsystem is reduced.

Brief Description Of The Drawings

[0003] Some embodiments of the invention are described with respect to the following figures:

Figs. 1 and 3 are block diagrams of exemplary systems incorporating some embodiments of the invention;

Fig. 2 is a diagram of address spaces according to an embodiment; and

Fig. 4 is a flow diagram of a process performed by a memory controller according to an embodiment.

Detailed Description

[0004] In accordance with some embodiments, a memory subsystem that has one or more memory devices can be configured to have multiple portions, where a first portion contains data with error correction code (ECC) information and a second portion contains data without ECC information. One example type of ECC is the Hamming code, which is

- 2 -

able to correct single-bit errors and detect two-bit errors. Other types of ECC can be used in other implementations. More generally, ECC information refers to any information that allows detection and correction of data errors. The ECC information is used for detecting an error in associated data, and if the error involves up to a certain number (*e.g.*, one or more) of data bits, the ECC information can be used to correct the data.

[0005] As used here, the term “data” refers generally to user data, software application data, software code, or any other information that is stored on behalf of components in a system or on behalf of devices or users outside the system. Data stored in a memory subsystem is contrasted with control information (such as ECC information) that is associated with the data and that is used to enable the performance of one or more tasks with respect to the data, such as error detection and/or correction, status indication, and so forth.

[0006] A memory controller that controls access of the memory subsystem is configured to store data with ECC information in the first portion of the memory subsystem, and to store data without ECC information in the second portion of the memory subsystem. As a result, no ECC protection is provided in the second portion of the memory subsystem.

[0007] By being able to divide the memory subsystem into multiple portions for which ECC protection is configurably enabled and disabled, more efficient usage of the storage capacity of the memory subsystem can be administered. Conventionally, ECC protection is either enabled or disabled for the entire memory subsystem. If enabled, that means that all data stored in the memory subsystem would have to be provided with ECC information. However, if ECC protection is disabled, then no ECC information is stored with data, which can result in system operation errors when errors occur in certain data.

[0008] One example of data that can be stored in the portion of the memory subsystem without ECC protection is video data. A characteristic of a video application is that there is a relatively large amount of video data, and high memory bandwidth is desirable for storing such video data. An error occurring in video data normally would not result in a system error. In fact, an error in video data may merely cause a visual artifact.

- 3 -

[0009] On the other hand, errors in data associated with software program code, for example, may cause a system to crash. Therefore, such data should be stored in the portion of the memory subsystem that is ECC protected.

[0010] By enabling ECC protection for one portion of the memory subsystem but disabling ECC protection for another portion of the memory subsystem, a balance can be achieved between the goals of increased memory subsystem performance and enhanced data integrity. Information considered to be important can be stored in the portion of the memory subsystem with ECC protection. However, non-critical data can be stored in the portion of the memory subsystem without ECC protection.

[0011] The foregoing refers to a memory subsystem that can include one or multiple memory devices. In an alternative embodiment, the memory subsystem includes just a single memory device. As used here, the term “single memory device” refers to a device having memory storage circuitry that is provided on a single support substrate. In some embodiments, the support substrate is a semiconductor substrate on which memory cells and associated peripheral control circuitry are formed to provide a memory chip. A “chip” refers to an integrated circuit device that has circuitry encapsulated in packaging.

[0012] In an embodiment in which a single memory device is provided, a first part of the memory device is configured to store data with redundancy information, while a second part of the memory device is configured to store data without redundancy information. One example of redundancy information is ECC information. Alternatively, redundancy information can refer to other types of control information used for detecting or detecting and correcting data errors. Examples of such other types of redundancy information include parity information, cyclic redundancy check (CRC) information, and so forth.

[0013] Fig. 1 illustrates an exemplary system 100 that includes a memory device 102 that is coupled to a memory controller 104, where the memory controller 104 controls access of the memory device 102. Although a direct link 106 is shown between the memory controller 104 and the memory device 102, it is noted that the memory controller 104 in some implementations may be indirectly connected to the memory device 102, such as through an intermediate controller.

- 4 -

[0014] The memory controller 104 includes a control circuit 108 that receives requests for accessing (reading or writing) the memory device 102, and issues commands over the link 106 to the memory device 102 to perform the requested accesses. The memory controller 104 also includes at least one configuration register 110 that stores configuration information in accordance with an embodiment. The configuration information in the configuration register 110 can indicate which part of the memory device 102 is to store data with redundancy information (*e.g.*, ECC information), and which other part of the memory device 102 is to store data without redundancy information (*e.g.*, ECC information).

[0015] The part of the memory device 102 that is not ECC protected has a larger bandwidth, since all data pins of the memory device 102 are available for inputting and outputting data. On the other hand, the part of the memory device that is ECC protected has a lower bandwidth, since a portion of the data pins of the memory device 102 is used for inputting and outputting ECC information. Note that reference to “data pins” of the memory device 102 assumes a parallel data input/output (I/O) implementation in which there are multiple data pins to input and output multiple data bits. Examples of memory devices with parallel I/O implementations include DDR2 (double-data-rate-2) and DDR3 DRAMs (dynamic random access memories). However, in some other implementations, the memory device 102 can have a serial data I/O implementation, such as RAMBUS memory device or an FBD (fully buffered dual inline memory module) memory device. With a memory device having a serial I/O implementation, accessing the part of the memory device that is ECC protected will cause a portion of the data I/O bandwidth to be consumed by the input or output of ECC information.

[0016] The memory controller 104 also includes various interface ports 112, 114. The interface port 112 can be used to connect to a video controller 116, and the interface port 114 can be used to connect to a processor 118. The video controller 116 and processor 118 are separate from the memory controller 104. Other interface ports can also be provided in the memory controller 104 for connection to other types of devices in the system 100. The devices connected through the interface ports of the memory controller 104 are considered “requestors” that are able to submit requests to access the memory device 102.

- 5 -

[0017] In an alternative embodiment, instead of providing multiple interface ports in the memory controller 104 to corresponding different devices, one interface port can be provided in the memory controller 104 for connection to another controller, where this other controller can then be used to connect to other devices (*e.g.*, the video controller 116 and processor 118) that are able to submit requests to the memory controller 104 for accessing the memory device 102. As yet another alternative, a bus structure can be implemented in which multiple requesters (devices requesting access of the memory controller 104) can arbitrate for a shared communication bus.

[0018] In some embodiments, the system 100 is an embedded system, which refers to a system on a chip. In an embedded system, the memory controller 104, video controller 116, processor 118, and other devices (not shown) may be formed on a common substrate. A characteristic of an embedded system is that it is desirable that such embedded system be relatively low cost and consumes a relatively low amount of power. In some implementations, an embedded system can connect to an external memory device. Alternatively, the memory device can be provided on the same substrate as the other components of the embedded system.

[0019] Fig. 2 is a diagram of three address spaces that may be present in the system 100, according to an example. A memory address space 202 is the address space of the memory device 102 of Fig. 1. The memory address space 202 represents the entire space available in the memory device 102 for storing information (including data and control information such as ECC information).

[0020] In accordance with some embodiments, the memory address space 202 of the memory device 102 is divided into a first part 204 that is ECC protected, and a second part 206 that is not ECC protected. Although Fig. 2 shows a specific embodiment, it is noted that other embodiments can be implemented. In Fig. 2, the lower part 204 of the memory address space 202 is ECC protected, while the upper part 206 is not ECC protected. Alternatively, the lower part 204 is not ECC protected, while the upper part 206 is ECC protected. As yet another alternative, a more complex arrangement of ECC and non-ECC protected parts can be defined, where the ECC and non-ECC parts may be interleaved or have some other complex arrangement with respect to each other. The definitions of such a complex

- 6 -

arrangement can be accomplished by use of multiple configuration registers in the memory controller.

[0021] In the example of Fig. 2, video data 214 is stored in the non-ECC protected part 206 of the memory-address space 202 starting at offset V from the end of the ECC-protected part 204. The parameter L in Fig. 2 is a configurable parameter whose value can be set using the configuration register 110 of Fig. 1, for example. The parameter L defines the amount of address space allocated to ECC protected memory. In the example implementation of Fig. 2, it is assumed that ECC protection is performed on a byte-wise basis and will consume half of the ECC protected memory part 204 due to practical constraints of a 16-bit wide memory device. In other implementations, different amounts of the ECC protected memory part 204 would be consumed by ECC control information.

[0022] As a result of ECC protection in the first part 204 of the memory address space 202, the available address space in this first part 204 that can be used for actually storing data associated with a requestor (*e.g.*, processor 118 in Fig. 1) is reduced. This reduced address space is represented as a processor address space 208 in Fig. 2, which represents the available portion of the memory device 102 that can actually be used to store data of the processor 118.

[0023] As shown in Fig. 2, the capacity of the part 204 of the memory address space 202 is $2*L$, where $2*L$ represents the length (in bits or bytes) of the part 204 of the memory address space 202. The processor address space 208 also has an ECC-protected part 210 and part 212. However, the ECC-protected part 210 of the processor address space 208 has a reduced length compared to the part 204 of the original memory address space 202. In the example of Fig. 2, the ECC-protected part 210 of the processor address space 208 has a length of L, which is half the length ($2*L$) of the part 204 of the memory address space 202. This is based on the assumption that the ECC information stored in the part 204 will render half of the part 204 unavailable for storing data. In one example, to protect 8 bits of data, the ECC code can either be 5 bits or 6 bits in length. A typical memory device arrangement has 16 data pins. Thus, in such an arrangement, 8 of the data bits can be used for inputting and outputting data into the ECC-protected part 204 of the memory device, while the remaining 8 data pins are used to input and output ECC information (note that 2 or 3 of the data pins will be unused depending upon whether the ECC information is 5 bits or 6 bits in length). In

- 7 -

other implementations, other arrangements are possible. For example, the 2 or 3 data pins can be used for inputting or outputting data, assuming that the memory controller 104 is configured to support such addressing.

[0024] Referring again to Fig. 2, the non-ECC protected part 212 of the processor address space 208 has the same length as the non-ECC protected part 206 of the memory address space 202. In the example of Fig. 2, video data 214 from video memory in a video controller address space 216 is stored in the non-ECC protected part 212 of the processor address space 208. The video controller address space 216 refers to the address space associated with the video controller 116 of Fig. 1.

[0025] Fig. 3 illustrates an alternative embodiment of a system 100A that has a memory controller 104A for controlling access of a memory subsystem 300 that includes multiple memory devices 302 (unlike the embodiment of Fig. 1 that includes just a single memory device). Control circuitry 108A in the memory controller 104A is able to control access of the multiple memory devices 302 in the memory subsystem 300, and at least one configuration register 110A is used to store configuration information that indicates which portions of the memory subsystem 300 are protected with ECC information and which portions of the memory subsystem 300 are not protected with ECC information.

[0026] As shown in Fig. 4, during operation, the memory controller 104 or 104A in Fig. 1 or 3, respectively, receives (at 402) a request to access memory (the memory device 102 or the memory subsystem 300 of Fig. 1 or 3, respectively). The request can be received from any one of various requestors, including as examples the video controller 116 or processor 118 in Fig. 1.

[0027] The address of the request is translated (at 404) into a memory address using mapping information (111 or 111A) stored in the memory controller 104 or 104A. The translation is performed since provision of ECC protection in the ECC protected part of the memory has reduced the available space for storing data of a requester. As shown in Fig. 2, an address of a received request would be in the processor address space 208. This address is translated into a memory address in the memory address space 202. For example, an address K in the ECC protected part 210 of the processor address space 208 would be translated to 2*K in the ECC protected part 204 of the memory address space 202. An address M in the

- 8 -

non-ECC protected part 212 of the processor address space 208 has two components: $L + N$, where L is the length of the ECC protected part 212 of the processor address space, and N is the offset from L into the non-ECC protected part 212 of the processor address space 208. In this case, the address M is translated to $2*L+N$. In other implementations, other translations are performed.

[0028] The mapping information 111 or 111A stored in the memory controller 104 or 104A provides the correlation between the processor address space 208 and the memory address space 202. The mapping information 111 or 111A, which can be stored in storage media of the memory controller 104 or 104A, accounts for the reduction in available space for data due to storage of ECC information in the ECC-protected part of memory.

[0029] Next, after translation of the address in the received request, it is determined (at 406) whether the received request is for data in the ECC protected part of the memory device. If so, a memory command (corresponding to the received request) performed (at 408) by the memory controller takes into account ECC information. If the memory command is a read command, then (assuming the example implementation described in Fig. 2) additional read operations may be performed to account for bandwidth consumed by ECC information. However, if the memory command is a write command, then the memory controller generates the corresponding ECC information for writing to the memory device.

[0030] On the other hand, if it is determined (at 406) that the request is for data in a non-ECC protected part, then a memory command (corresponding to the received request) is performed (at 410) without taking into account ECC information.

[0031] As noted above, a memory subsystem can be more efficiently utilized by being able to divide the memory subsystem into a portion that is ECC protected and another portion that is non-ECC protected. This benefit is particularly useful in a system having just a single memory device (such as a single memory chip) since the single memory device can be configured such that ECC is not applied to all data stored in the single memory device. For applications that involve a large amount of data and for which absolute data integrity is not critical, such as a video application, the data of such applications can be stored in the non-ECC protected portion of the memory.

- 9 -

[0032] In the foregoing description, numerous details are set forth to provide an understanding of the present invention. However, it will be understood by those skilled in the art that the present invention may be practiced without these details. While the invention has been disclosed with respect to a limited number of embodiments, those skilled in the art will appreciate numerous modifications and variations therefrom. It is intended that the appended claims cover such modifications and variations as fall within the true spirit and scope of the invention.

- 10 -

What is claimed is:

- 1 1. A system comprising:
2 a memory subsystem having at least one memory device; and
3 a memory controller to control access of the memory subsystem, wherein the memory
4 controller is configured to store data with error correction code (ECC) information in a first
5 portion of the memory subsystem, and to store data without ECC information in a second
6 portion of the memory subsystem.
- 1 2. The system of claim 1 or 2, wherein the memory subsystem includes a single memory
2 device, wherein a first part of the memory device is to store data with ECC information, and a
3 second part of the memory device is to store data without ECC information.
- 1 3. The system of claim 1, wherein the memory controller is configured with
2 configuration information to indicate that the first portion of the memory subsystem is to be
3 protected by ECC information, and that the second portion of the memory subsystem is not to
4 be protected by ECC information.
- 1 4. The system of claim 3, wherein the memory controller includes at least one
2 configuration register to store the configuration information.
- 1 5. The system of any of the preceding claims, wherein the memory controller is
2 configured to further:
3 receive a request to access the memory subsystem from a requestor; and
4 convert the request into at least one memory command that is sent to the memory
5 subsystem.
- 1 6. The system of claim 5, wherein the memory controller is configured to further:
2 translate an address of the request into an address of the memory subsystem to include
3 in the at least one memory command.

- 11 -

- 1 7. The system of claim 6, wherein translation of the address of the request into the
2 address of the memory subsystem is based on mapping information that accounts for the
3 reduction in available space for data due to storage of ECC information in the first portion.
- 1 8. A method comprising:
2 providing a memory device; and
3 providing a memory controller configured to store data with redundancy information
4 in a first part of the memory device, and to store data without redundancy information in a
5 second part of the memory device.
- 1 9. The method of claim 8, wherein storing data with the redundancy information
2 comprises storing data with error correction code (ECC) information.
- 1 10. The method of claim 8 or 9, further comprising storing mapping information in the
2 memory controller to map an address space of a requestor that uses the memory device to an
3 address space of the memory device.
- 1 11. The method of claim 10, wherein the address space of the requestor is smaller than the
2 address space of the memory device.
- 1 12. The method of claim 10 or 11, further comprising:
2 receiving, by the memory controller, a request from the requestor to access the
3 memory device; and
4 translate an address of the request into an address on the address space of the memory
5 device using the mapping information.
- 1 13. The method of claim 12, further comprising converting the request into one or more
2 memory commands submitted to the memory device.
- 1 14. A memory controller for use with a memory subsystem having at least one memory
2 device, comprising:
3 a control circuit to send commands to the memory subsystem; and

- 12 -

4 a storage to store configuration information that indicates that a first portion of the
5 memory subsystem is to store data with error correction code (ECC) information and a
6 second portion of the memory subsystem is to store data without ECC information.

1 15. The memory controller of claim 14, wherein the memory subsystem includes a single
2 memory device.

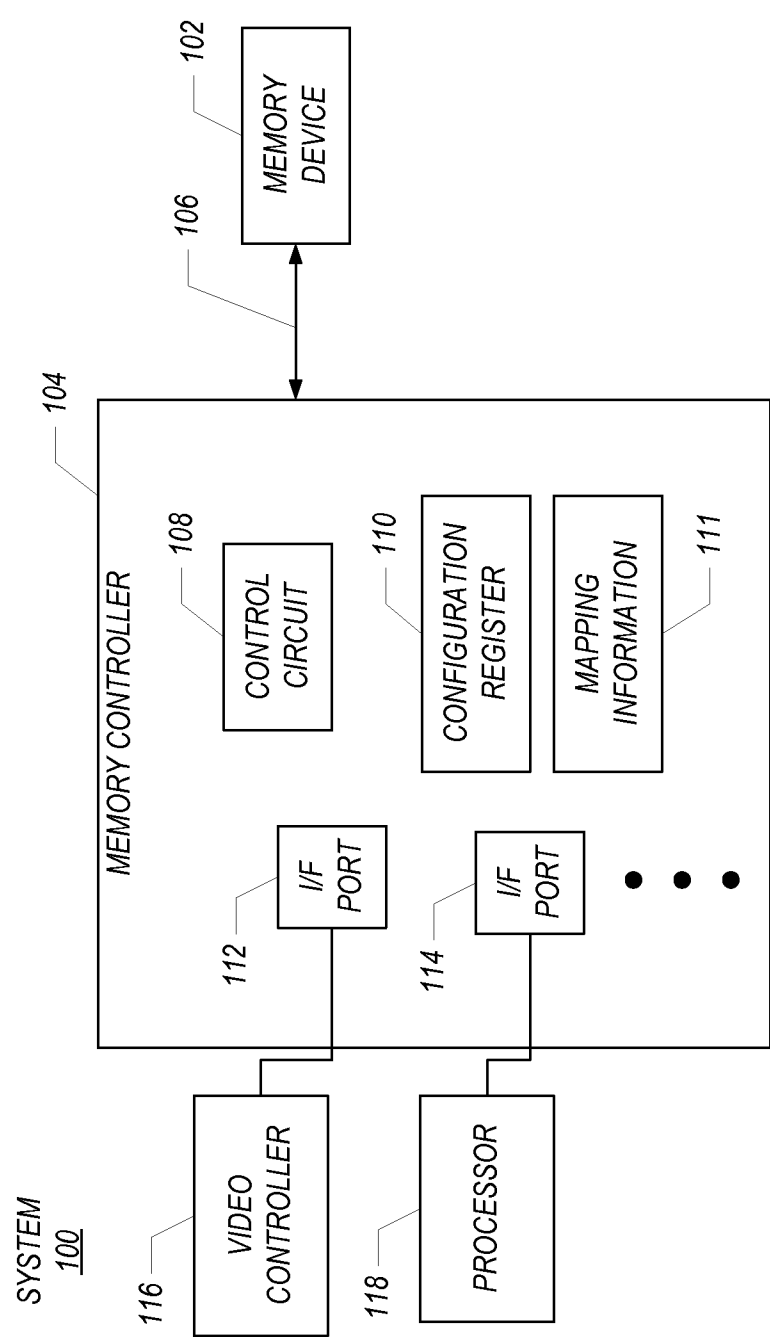


FIG. 1

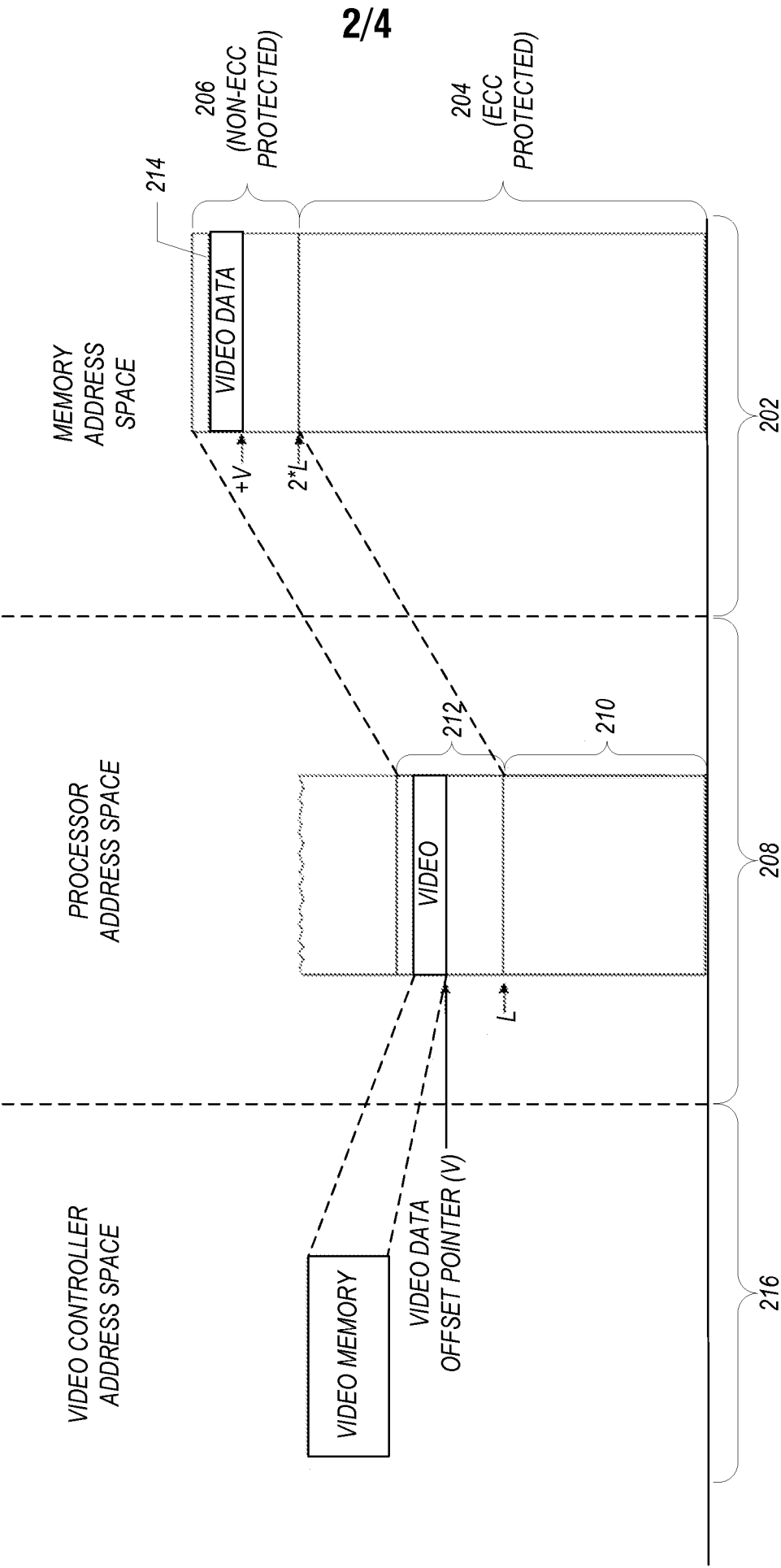


FIG. 2

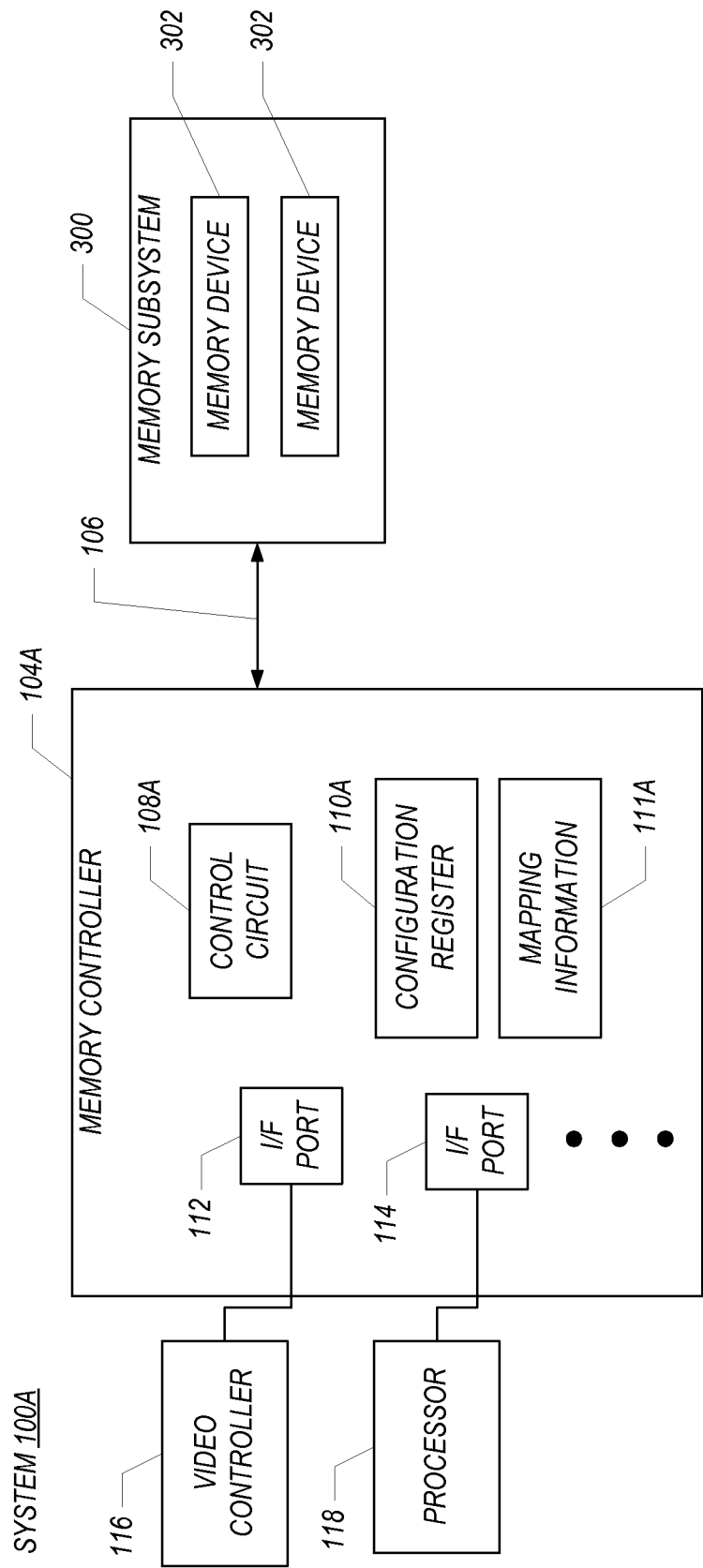


FIG. 3

4/4

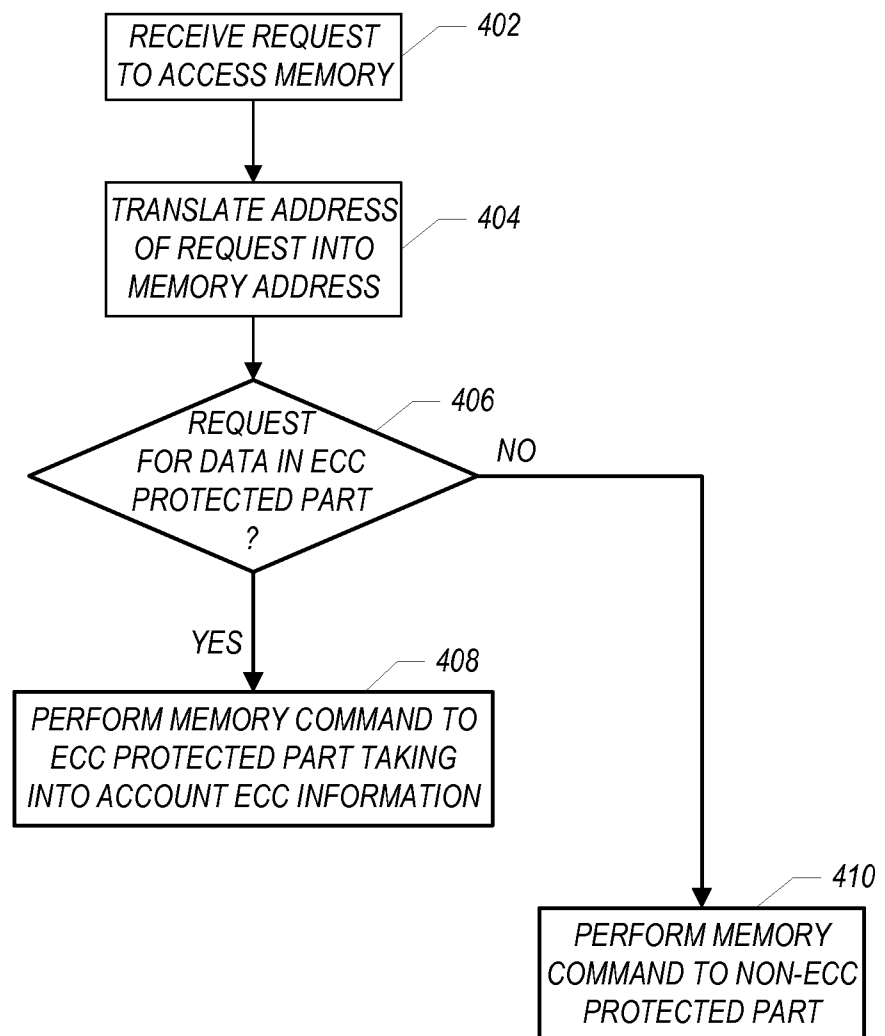


FIG. 4

A. CLASSIFICATION OF SUBJECT MATTER**G06F 11/08(2006.01)i, G06F 13/14(2006.01)i, G06F 12/00(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC: G06F; H03M

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords:(memory*)+((ECC*,error correct*)<near/2>(without*,non*,protec*))

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2003-0070054 A1 (WILLIAMS et al.) 10 April 2003	1-3, 8-9, 14-15
Y	See abstract; paragraphs 9-12, 18-26; and figures 1-2.	4-7, 10-11
Y	US 2008-0005646 A1 (BAINS) 03 January 2008 See abstract; paragraphs 16-24; and figure 1.	4-7, 10-11
A	US 2007-0220354 A1 (MOYER) 20 September 2007 See abstract; paragraphs 17-26; figure 1; and claim 11.	1-11, 14-15
A	US 2006-0123320 A1 (VOGT) 08 June 2006 See abstract; paragraphs 15-16; and figure 3.	1-11, 14-15



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

31 MAY 2010 (31.05.2010)

Date of mailing of the international search report

31 MAY 2010 (31.05.2010)

Name and mailing address of the ISA/KR

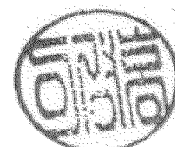
Korean Intellectual Property Office
Government Complex-Daejeon, 139 Seonsa-ro, Seo-
gu, Daejeon 302-701, Republic of Korea

Facsimile No. 82-42-472-7140

Authorized officer

LEE, Kyung Hong

Telephone No. 82-42-481-8212



INTERNATIONAL SEARCH REPORT

International application No.

PCT/US2009/056467**Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)**

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:
2. ☒ Claims Nos.: 13
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

Claim 13 refer to claim 12 which does not comply with PCT Rule 6.4(a). Therefore claim does not meet the requirements of PCT Article 6
3. ☒ Claims Nos.: 12
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.
2. ☐ As all searchable claims could be searched without effort justifying an additional fee, this Authority did not invite payment of any additional fee.
3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:
4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

- ☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.
- ☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.
- ☐ No protest accompanied the payment of additional search fees.

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2009/056467

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2003-0070054 A1	10.04.2003	AU 2000-62285 A1	13.02.2001
		US 2002-0029315 A1	07.03.2002
		US 2002-0029316 A1	07.03.2002
		US 6279072 B1	21.08.2001
		US 6397290 B1	28.05.2002
		US 6584543 B2	24.06.2003
		WO 01-08010 A1	01.02.2001
US 2008-0005646 A1	03.01.2008	CN 101097784 A	02.01.2008
		CN 101097784 C0	02.01.2008
		EP 2035938 A2	18.03.2009
		JP 2009-540477 A	19.11.2009
		KR 10-2009-0016604 A	16.02.2009
		TW 200809867 A	16.02.2008
		WO 2008-005781 A2	10.01.2008
US 2007-0220354 A1	20.09.2007	WO 2008-005781 A3	10.01.2008
		JP 2009-527820 A	30.07.2009
		JP 2009-527820 T	30.07.2009
		KR 10-2008-0098613 A	11.11.2008
		TW 200801932 A	01.01.2008
		US 7617437 B2	10.11.2009
		WO 2007-103590 A2	13.09.2007
US 2006-0123320 A1	08.06.2006	WO 2007-103590 A3	13.09.2007
		CN 101036131 A0	12.09.2007
		DE 112005002390 T5	11.10.2007
		GB 0706172 D0	09.05.2007
		GB 2433624 A	27.06.2007
		GB 2433624 B	15.10.2008
		JP 2008-521160 A	19.06.2008
		JP 2008-521160 T	19.06.2008
		KR 10-0884096 B1	19.02.2009
		KR 10-2007-0051930A	18.05.2007
		TW 1304591A	21.12.2008
		US 7464241 B2	09.12.2008
		WO 2006-057963 A2	01.06.2006
		WO 2006-057963 A3	01.06.2006