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(54) Title: PAD SURFACE ROUGHNESS CHANGE METRICS FOR CHEMICAL MECHANICAL POLISHING CONDITIONING DISKS

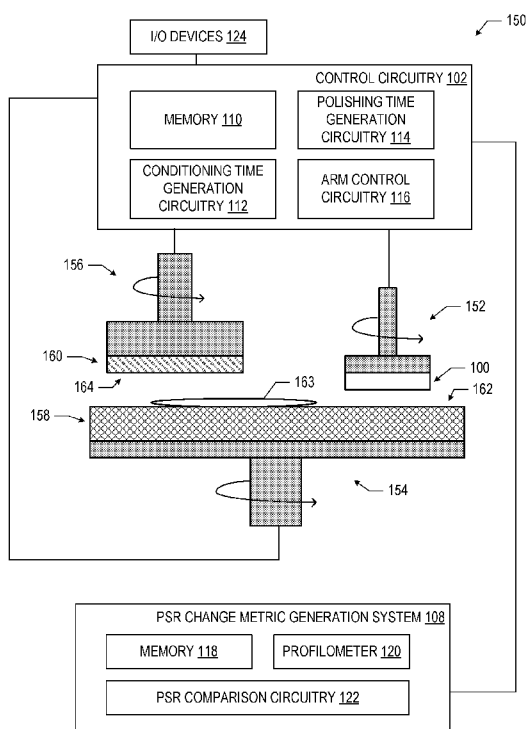


FIG. 1

(57) Abstract: Disclosed herein are pad surface roughness (PSR) change metrics for chemical mechanical polishing (CMP) conditioning disks. In some embodiments, a CMP system may include control circuitry to: access a stored PSR change metric for a CMP polishing pad and a CMP conditioning disk; generate, based on the PSR change metric, a conditioning time for conditioning the CMP polishing pad with the CMP conditioning disk to achieve a target PSR for the CMP polishing pad; and generate, based on the conditioning time, a control instruction for a first arm or a second arm of the CMP system, wherein the CMP conditioning disk is coupled to the first arm, the CMP polishing pad is coupled to the second arm, and the control instruction is to cause the CMP conditioning disk to condition the CMP polishing pad for the conditioning time.

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**PAD SURFACE ROUGHNESS CHANGE METRICS FOR CHEMICAL MECHANICAL POLISHING
CONDITIONING DISKS**

Technical Field

[0001] The present disclosure relates generally to chemical mechanical polishing (CMP), and more particularly, to CMP conditioning disks.

Background

[0002] Chemical mechanical polishing (CMP) typically includes rotating and translating a polishing pad on a wafer to remove material from the wafer and achieve a flat wafer surface. For example, a wafer may be polished to remove an oxide layer prior to a lithography step. The polishing process may degrade the polishing surface of CMP polishing pads; to "refurbish" a CMP polishing pad and mitigate a degradation in polishing performance, the polishing surface may be abraded using a CMP conditioning disk.

Brief Description of the Drawings

[0003] Embodiments will be readily understood by the following detailed description in conjunction with the accompanying drawings. To facilitate this description, like reference numerals designate like structural elements. Embodiments are illustrated by way of example, and not by way of limitation, in the figures of the accompanying drawings.

[0004] FIG. 1 is a diagram of a chemical mechanical polishing (CMP) system, in accordance with various embodiments.

[0005] FIGS. 2 and 3 are side views of conditioning different zones of a surface of a CMP polishing pad, in accordance with various embodiments.

[0006] FIG. 4 is a top view of a surface of a CMP polishing pad subsequent to the conditioning illustrated in FIGS. 2 and 3.

[0007] FIG. 5 illustrates surface profiles of different zones of a surface of a CMP polishing pad subsequent to the conditioning illustrated in FIGS. 2 and 3.

[0008] FIGS. 6 and 7 are plots depicting different pad surface roughness (PSR) change metrics, in accordance with various embodiments.

[0009] FIGS. 8 and 9 are plots depicting different functional relationships between wafer removal rate (WRR) and PSR in the CMP system of FIG. 1, in accordance with various embodiments.

[0010] FIG. 10 is a flow diagram of a method of characterizing one or more CMP conditioning disks, in accordance with various embodiments.

[0011] FIG. 11 is a flow diagram of a method of conditioning a CMP polishing pad with a CMP conditioning disk characterized by a PSR change metric, in accordance with various embodiments.

[0012] FIG. 12 is a flow diagram of a method of generating a functional relationship between WRR and PSR in a CMP system, in accordance with various embodiments.

[0013] FIG. 13 is a flow diagram of a method of controlling a CMP system to polish a wafer using a CMP polishing pad having a particular PSR, in accordance with various embodiments.

[0014] FIGS. 14A and 14B are top views of a wafer and dies that may be processed using CMP systems and techniques in accordance with any of the embodiments disclosed herein.

[0015] FIG. 15 is a cross-sectional side view of an IC device that may be processed using CMP systems and techniques in accordance with any of the embodiments disclosed herein.

[0016] FIG. 16 is a cross-sectional side view of an IC device assembly that may have components that may be processed using CMP systems and techniques in accordance with any of the embodiments disclosed herein.

[0017] FIG. 17 is a block diagram of an example computing device that may have components that may be processed using CMP systems and techniques in accordance with any of the embodiments disclosed herein.

Detailed Description

[0018] Disclosed herein are pad surface roughness (PSR) change metrics for chemical mechanical polishing (CMP) conditioning disks. In some embodiments, a CMP system may include control circuitry to: access a stored PSR change metric for a CMP polishing pad and a CMP conditioning disk; generate, based on the PSR change metric, a conditioning time for conditioning the CMP polishing pad with the CMP conditioning disk to achieve a target PSR for the CMP polishing pad; and generate, based on the conditioning time, a control instruction for a first arm or a second arm of the CMP system, wherein the CMP conditioning disk is coupled to the first arm, the CMP polishing pad is coupled to the second arm, and the control instruction is to cause the CMP conditioning disk to condition the CMP polishing pad for the conditioning time. In some embodiments, a CMP system may determine an unconditioned PSR on an unconditioned CMP polishing pad surface; condition a first CMP polishing pad surface with the CMP conditioning disk for a first conditioning time; after conditioning of the first CMP polishing pad surface, determine a first PSR of the first CMP polishing pad surface; condition a second CMP polishing pad surface with the CMP conditioning disk for a second conditioning time, wherein the second conditioning time is longer or shorter than the first conditioning time; after conditioning of the second CMP polishing pad surface, determine a second PSR of the second CMP polishing pad surface; and generate a PSR change metric for the CMP conditioning disk based on the unconditioned PSR, the first PSR, and the second PSR.

[0019] As used herein, the "PSR" of a CMP polishing pad may refer to any suitable surface roughness metric or combination of such metrics (e.g., a profile surface roughness metric, an area

surface roughness metric, any combination of such metrics, etc.). For example, the PSR may be the roughness average (known as "R_a"), calculated in accordance with:

$$\frac{1}{n} \sum_{i=1}^n |y_i|$$

[0020] where y_i is the vertical distance between the mean line and the i th data point in the surface profile, as known in the art. In some embodiments, the PSR may be the root mean square roughness (known as "R_q"), calculated in accordance with:

$$\sqrt{\frac{1}{n} \sum_{i=1}^n (y_i)^2}$$

[0021] In other embodiments, the PSR may be the maximum valley depth, the maximum peak height, the maximum total height and the surface profile, or any other surface roughness parameter. In some embodiments, multiple surface roughness parameters may be combined (e.g., in a linear or nonlinear combination) to generate a PSR. Various examples of particular PSRs are used to illustrate the systems and techniques disclosed herein, but these are simply for illustrative purposes, and any suitable PSR may be used.

[0022] Conventionally, the performance of CMP conditioning disks has been evaluated based on the pad cut rate (PCR), the amount of material removed from the CMP polishing pad during conditioning (normalized by the conditioning time). In particular, PCR has served as a measure of the aggressiveness of a CMP conditioning disk. Such conventional approaches have failed to recognize that the PSR of a CMP polishing pad may have an important impact on wafer polishing, separate from PCR. Moreover, the use of the PCR metric does not reveal how the PSR of a CMP polishing pad may change during conditioning. In particular, the PSR of a CMP polishing pad may change across the depth/thickness of the CMP polishing pad during conditioning, and thus a particular PCR may fail to characterize the changing PSR across the pad depth. The thickness of a CMP polishing pad may, in turn, depend on the conditioning time and PCR (as well as other process variables, such as polishing head downforce, head and platen rotation rate, slurry and other consumables, etc.). Further, conventional approaches have not provided any suggestion of how a CMP conditioning disk might be accurately quantified in terms of PSR to enable comparisons between CMP conditioning disks of different designs (e.g., CMP conditioning disks with different PCRs).

[0023] Various ones of the systems and techniques disclosed herein may enable the prediction of CMP conditioning disk performance, allowing the selection and optimization of CMP conditioning disks for particular performance objectives, and thus improving the CMP process. In some embodiments, metrics for quantifying the dynamics of change of the PSR of a CMP polishing pad

during conditioning by a CMP conditioning disk are provided. Some of these metrics may include normalization by the conditioning time required to remove a predetermined amount of material from the CMP polishing pad, allowing a comparison of PSR change dynamics between CMP conditioning disks having different PCRs.

[0024] In the following detailed description, reference is made to the accompanying drawings that form a part hereof wherein like numerals designate like parts throughout, and in which is shown, by way of illustration, embodiments that may be practiced. It is to be understood that other embodiments may be utilized and structural or logical changes may be made without departing from the scope of the present disclosure. Therefore, the following detailed description is not to be taken in a limiting sense.

[0025] Various operations may be described as multiple discrete actions or operations in turn, in a manner that is most helpful in understanding the claimed subject matter. However, the order of description should not be construed as to imply that these operations are necessarily order dependent. In particular, these operations may not be performed in the order of presentation. Operations described may be performed in a different order from the described embodiment. Various additional operations may be performed, and/or described operations may be omitted in additional embodiments.

[0026] For the purposes of the present disclosure, the phrase "A and/or B" means (A), (B), or (A and B). For the purposes of the present disclosure, the phrase "A, B, and/or C" means (A), (B), (C), (A and B), (A and C), (B and C), or (A, B, and C). The term "between," when used with reference to measurement ranges, is inclusive of the ends of the measurement ranges.

[0027] The description uses the phrases "in an embodiment" or "in embodiments," which may each refer to one or more of the same or different embodiments. Furthermore, the terms "comprising," "including," "having," and the like, as used with respect to embodiments of the present disclosure, are synonymous. The disclosure may use perspective-based descriptions such as "above," "below," "top," "bottom," and "side"; such descriptions are used to facilitate the discussion and are not intended to restrict the application of disclosed embodiments. The accompanying drawings are not necessarily drawn to scale. As used herein, the term "circuitry" may refer to an application-specific integrated circuit (ASIC), an electronic circuit, a processor (shared, dedicated, or group) and/or memory (shared, dedicated, or group) that execute one or more software or firmware programs, a combinational logic circuit, and/or other suitable hardware that provide the described functionality.

[0028] FIG. 1 is a diagram of a CMP system 150, in accordance with various embodiments. The CMP system 150 may include a CMP conditioning disk 100 disposed on a first arm 152. The CMP conditioning disk 100 may be formed of a substrate coated with an abrasive material, such as a

diamond film deposited using chemical vapor deposition (CVD). Any CMP conditioning disk 100 may be characterized by various ones of the techniques disclosed herein, and included in the CMP system 150. The CMP conditioning disk 100 may be secured to the first arm 152 using any suitable mechanism, such as vacuum, a clamp, a frame, or mechanical fasteners, for example. The first arm 152 may include mechanical linkages to allow the CMP conditioning disk 100 to translate "up and down" to bring the CMP conditioning disk 100 into contact with the CMP polishing pad 158 (discussed below). In some embodiments, the first arm 152 may include mechanical linkages to allow the CMP conditioning disk 100 to translate "side to side" while in contact with the CMP polishing pad 158. In some embodiments, the first arm 152 may include a rotor to allow the CMP conditioning disk 100 to rotate while in contact with the CMP polishing pad 158. The first arm 152 may include, for example, a head, as known in the art.

[0029] The CMP system 150 may include a CMP polishing pad 158 disposed on a second arm 154. The CMP polishing pad 158 may be formed from a porous material, such as a hard elastomer or a polyurethane-based material. The CMP polishing pad 158 may include other additives to achieve a desired porosity, as known in the art. Different CMP polishing pads 158 may have different mechanical properties, such as hardness (e.g., with "soft" pads having a hardness between 10 and 20 MPa and "hard" pads having a hardness between 200 and 1500 MPa). The CMP polishing pad 158 may be secured to the second arm 154 using any suitable mechanism, such as vacuum, a clamp, a frame, or mechanical fasteners, for example. The second arm 154 may include mechanical linkages to allow the CMP polishing pad 158 to translate "up and down" to bring the CMP polishing pad 158 into contact with the CMP conditioning disk 100 and/or the wafer 160 (discussed below). In some embodiments, the second arm 154 may include mechanical linkages to allow the CMP polishing pad 158 to translate "side to side" while in contact with the CMP conditioning disk 100 and/or the wafer 160. In some embodiments, the second arm 154 may include a rotor to allow the CMP polishing pad 158 to rotate while in contact with the CMP conditioning disk 100 and/or the wafer 160. The second arm 154 may be, for example, a platen, as known in the art.

[0030] The CMP system 150 may include a wafer 160 disposed on a third arm 156. The wafer 160 may have any suitable dimensions (e.g., 200, 300, or 450 mm in diameter). The wafer 160 may be secured to the third arm 156 using any suitable mechanism, such as vacuum, a clamp, a frame, or mechanical fasteners, for example. In some embodiments, the wafer 160 may be disposed in a retainer ring to control the "side to side" movement of the wafer 160, and vacuum force may be used to hold the wafer 160 against the third arm 156 to control the "up and down" movement of the wafer 160. The third arm 156 may include mechanical linkages to allow the wafer 160 to translate "up and down" to bring the wafer 160 into contact with the CMP polishing pad 158. In some

embodiments, the third arm 156 may include mechanical linkages to allow the wafer 160 to translate "side to side" while in contact with the CMP polishing pad 158. In some embodiments, the third arm 156 may include a rotor to allow the wafer 160 to rotate while in contact with the CMP polishing pad 158.

[0031] When the CMP conditioning disk 100 is brought into contact with the surface 162 of the CMP polishing pad 158, and the two are rotated (and/or translated) relative to one another, the abrasive material of the CMP conditioning disk 100 may "dig" into the surface of the CMP polishing pad 158 and create "microgrooves" in the CMP polishing pad 158. When the surface 164 of wafer 160 is brought into contact with the surface 162 of the CMP polishing pad 158, and the two are rotated (and/or translated) relative to one another, the CMP polishing pad 158 may remove material from the wafer 160 and thereby polish the wafer 160. A slurry 163 may be disposed on the CMP polishing pad 158. When the wafer 160 is brought into contact with the CMP polishing pad 158, and the two are rotated (and/or translated) relative to one another, the slurry 163 may flow between the CMP polishing pad 158 and the wafer 160 to facilitate the polishing of the wafer 160. In some embodiments, a retainer ring holding the wafer 160 on the third arm 156 may include grooves to allow the slurry 163 to flow to the wafer 160 and away from the wafer 160 during polishing. The slurry 163 may also flow through grooves in the CMP polishing pad 158 formed by the CMP conditioning disk 100. The slurry 163 may take any suitable form known in the art (e.g., an oxide slurry).

[0032] In some embodiments, the CMP conditioning disk 100 may be used to condition the CMP polishing pad 158 simultaneously with the CMP polishing pad 158 polishing the wafer 160. That is, the CMP conditioning disk 100 may be in contact with (and rotated relative to) the CMP polishing pad 158 at the same time that the wafer 160 may be in contact with (and rotated relative to) the CMP polishing pad 158. In other embodiments, the CMP polishing pad 158 may be conditioned by the CMP conditioning disk 100 before and/or after (but not simultaneously with) polishing the wafer 160 using the CMP polishing pad 158.

[0033] The CMP system 150 may include control circuitry 102, which may perform processing, communication, and control operations for the CMP system 150. The control circuitry 102 may include arm control circuitry 116. The arm control circuitry 116 may provide control over the first arm 152, the second arm 154, and the third arm 156 of the CMP system 150. In some embodiments, the arm control circuitry 116 may allow a user (or an automated set of computer-readable instructions) to set or adjust the rotation rate of the CMP conditioning disk 100 (via control of the first arm 152), the downward force exerted by the CMP conditioning disk 100 on the CMP polishing pad 158 (via control of the first arm 152), and/or the "side to side" translation of the CMP

conditioning disk 100 (via control the first arm 152), for example. In some embodiments, the arm control circuitry 116 may allow a user (or an automated set of computer-readable instructions) to set or adjust the rotation rate of the CMP polishing pad 158 (via control of the second arm 154) and/or the "side to side" translation of the CMP polishing pad 158 (via control of the second arm 154), for example. In some embodiments, the second arm 154 may not include "side to side" translation capability. In some embodiments, the arm control circuitry 116 may allow a user (or an automated set of computer-readable instructions) to set or adjust the rotation rate of the wafer 160 (via control of the third arm 156), the "side to side" translation of the wafer 160 (via control of the third arm 156), and/or the downward force exerted by the wafer 160 on the CMP polishing pad 158 (via control of the third arm 156), for example. In some embodiments, the control circuitry 102 (e.g., the arm control circuitry 116) may control the rate of flow of the slurry 163 from a slurry source (not shown).

[0034] The control circuitry 102 may include a memory 110. The memory 110 may store computer-readable instructions for performing suitable ones of the methods disclosed herein (i.e., the memory 110 may include computer-readable media). The memory 110 may store measurements and other determinations made by the control circuitry 102 (e.g., conditioning times, polishing times, functional relationships between PSR and wafer removal rate (WRR), etc., as discussed below), operational parameters, and any other suitable values used during the operation of the CMP system 150. The memory 110 may take any of the forms of the memory 1704 discussed below with reference to FIG. 17. The control circuitry 102 may be coupled to one or more input/output (I/O) devices 124 (discussed below).

[0035] The CMP system 150 may include a PSR change metric generation system 108. In some embodiments, the PSR change metric generation system 108 may be communicatively coupled to the control circuitry 102 (e.g., via a wired or wireless communication connection). The PSR change metric generation system 108 may be configured to characterize the CMP conditioning disk 100 in accordance with any of the techniques disclosed herein. For example, in some embodiments, the PSR change metric generation system 108 may determine an unconditioned PSR of an unconditioned CMP polishing pad surface; condition a first CMP polishing pad surface with the CMP conditioning disk 100 for a first conditioning time; after conditioning the first CMP polishing pad surface, determine a first PSR of the first CMP polishing pad surface; condition a second CMP polishing pad surface with the CMP conditioning disk 100 for a second conditioning time, wherein the second conditioning time is longer than the first conditioning time; after conditioning the second CMP polishing pad surface, determine a second PSR of the second CMP polishing pad surface; and generate a PSR change metric for the CMP conditioning disk 100 based on the unconditioned PSR,

the first PSR, and the second PSR. This and other embodiments are described in further detail below. The PSR change metric generation system 108 may share the I/O devices 124 with the control circuitry 102, or may have its own input device and/or output device (not shown) in accordance with any of the embodiments discussed below with reference to the I/O devices 124.

[0036] The PSR change metric generation system 108 may include a memory 118. The memory 118 may store computer-readable instructions for performing suitable ones of the methods disclosed herein (i.e., the memory 118 may include computer-readable media). The memory 118 may store measurements and other determinations made by the PSR change metric generation system 108 (e.g., PSR values, PSR ratio (PSRR) values (as discussed below), slopes and correlation coefficients of PSR versus normalized conditioning time data, etc.), operational parameters, and any other suitable values used during the operation of the PSR change metric generation system 108. The memory 118 may take any of the forms of the memory 1704 discussed below with reference to FIG. 17.

[0037] The PSR change metric generation system 108 may include a profilometer 120. The profilometer 120 may generate a surface profile of an object. In some embodiments, the profilometer 120 may be an optical profiler, such as a white light spectrometer, but any suitable profilometer may be used. The surface profile generated by the profilometer 120 may be further analyzed by the profilometer 120 to generate a surface roughness of the object, or the surface profile data generated by the profilometer 120 may be provided to another component of the PSR change metric generation system 108 (e.g., the PSR comparison circuitry 122), and that other component may generate the surface roughness of the object. When the object is the CMP polishing pad 158, the surface roughness generated from the surface profile is referred to herein as the "PSR," as discussed above. The PCR of a CMP conditioning disk 100 on a CMP polishing pad 158 may be measured using any of a number of techniques, such as making a hole within the CMP polishing pad 158 and measuring the hole depth before and after conditioning; for a grooved CMP polishing pad 158, measuring the heights of the groove before and after conditioning; or measuring the thickness of the CMP polishing pad 158 before conditioning, removing the CMP polishing pad 158 from the arm 154 (e.g., from a platen), and measuring its thickness after conditioning.

[0038] For example, FIGS. 2 and 3 are side views of conditioning different zones 166 and 168 of a surface 162 of a CMP polishing pad 158 with a CMP conditioning disk 100 as part of a method of characterizing the CMP conditioning disk 100, in accordance with various embodiments. In FIG. 2, the first arm 152 and the second arm 154 (under control of the arm control circuitry 116) may be used to bring the CMP conditioning disk 100 into contact with the surface 162 of the CMP polishing pad 158 to condition a first zone 166 of the CMP polishing pad 158. The first arm 152 may cause the CMP conditioning disk 100 to rotate, and the second arm 154 may cause the CMP polishing pad 158

to rotate. The first arm 152 may not swing. The first zone 166 of the CMP polishing pad 158 may be conditioned for a first amount of time (e.g., a time required to achieve a particular depth of removal of the CMP polishing pad 158, as discussed below). FIG. 3 depicts an arrangement in which the first arm 152 has translated the CMP conditioning disk 100 relative to its position in the arrangement of FIG. 2 (under control of the arm control circuitry 116) to condition a second zone 168 of the CMP polishing pad 158. The first arm 152 may cause the CMP conditioning disk 100 to rotate, and the second arm 154 may cause the CMP polishing pad 158 to rotate, and the second zone 168 of the CMP polishing pad 158 may be conditioned for a second amount of time (e.g., a multiple of the first amount of time, as discussed below). The first arm 152 may not swing. As suggested by FIGS. 2 and 3, the number of different zones of a single CMP polishing pad 158 that may be differently conditioned will depend on the relative dimensions of the CMP polishing pad 158 and the CMP conditioning disk 100.

[0039] FIG. 4 is a top view of the surface 162 of the CMP polishing pad 158 subsequent to the conditioning illustrated in FIGS. 2 and 3, showing the annular first and second zones 166 and 168, respectively. The surface 162 also includes unconditioned zones 170. FIG. 5 illustrates surface profiles of different zones of the surface 162 of the CMP polishing pad 158 of FIG. 4; in particular, the surface profile 172 may be a surface profile of an unconditioned zone 170, the surface profile 174 may be a surface profile of the first zone 166, and the surface profile 176 may be a surface profile of the second zone 168. Mean lines of each surface profile are also indicated. To generate the surface profiles of FIG. 5, the CMP polishing pad 158 of FIG. 4 may be removed from the second arm 154, cut across the different conditioned zones, and measured by the profilometer 120.

[0040] As suggested in FIG. 5, in some embodiments, the PSR of the first zone 166 of the CMP polishing pad 158 (calculated based on the surface profile 174) may be less than the PSR of the unconditioned zone 170 of the CMP polishing pad 158 (calculated based on the surface profile 172). In some embodiments, further conditioning may further reduce the PSR of the CMP polishing pad 158. For example, when the second amount of conditioning time (used to condition the second zone 168 of the CMP polishing pad 158) is greater than the first amount of conditioning time (used to condition the first zone 166 of the CMP polishing pad 158), the PSR of the second zone 168 (calculated based on the surface profile 176) may be less than the PSR of the first zone 166 (calculated based on the surface profile 174), as suggested by FIG. 5.

[0041] Returning to FIG. 1, the PSR change metric generation system 108 may include PSR comparison circuitry 122. The PSR comparison circuitry 122 may be configured to compare the PSRs for two or more different CMP polishing pad surfaces to identify changes in the PSRs and generate one or more PSR change metrics. In particular, the PSRs compared by the PSR comparison circuitry

122 may be different PSRs that represent different amounts of conditioning time by a particular CMP conditioning disk 100 on a particular CMP polishing pad 158. In some embodiments, the different PSRs may be measured on different zones of a single CMP polishing pad 158 that were conditioned by the CMP conditioning disk 100 for different times. In other embodiments, the different PSRs may be measured on different CMP polishing pads 158 (all having nominally the same design, including material and geometry) that were conditioned by the CMP conditioning disk 100 for different times. Although "the" CMP polishing pad 158 may be discussed herein, different CMP polishing pads 158 having the same design may be used as suitable. Moreover, in some embodiments, a single CMP conditioning disk 100 may be used to perform all of the different conditioning trials, while in other embodiments, different CMP conditioning disks 100 (all having nominally the same design, including material and geometry) may be used to perform different ones of the different conditioning trials. Although "the" CMP conditioning disk 100 may be discussed herein, different CMP conditioning disks 100 having the same design may be used as suitable. In some embodiments, the PSR comparison circuitry 122 may calculate the PSR for a CMP polishing pad 158 based on the surface profile provided by the profilometer 120, while in other embodiments, the profilometer 120 may itself calculate the PSR, as noted above.

[0042] The PSR comparison circuitry 122 may generate one or more PSR change metrics. Generally, a PSR change metric may represent the change in PSR of a CMP polishing pad 158 after different amounts of conditioning by a particular CMP conditioning disk 100. Thus, a PSR change metric may be associated with both a particular CMP polishing pad 158 and a particular CMP conditioning disk 100 (or, more precisely, a particular design of a CMP polishing pad 158 and a particular design of a CMP conditioning disk 100). When PSR change metrics are generated for two different CMP conditioning disks 100 and a common CMP polishing pad 158, the PSR change metrics for each CMP conditioning disk 100 may be used to characterize the two CMP conditioning disks 100 to compare their conditioning performance, as discussed further herein.

[0043] Any suitable PSR change metric may be used with the systems and techniques disclosed herein. For example, in some embodiments, the PSR change metric may be a PSR ratio (PSRR) between a PSR of an unconditioned surface of the CMP polishing pad 158 and a PSR of the surface of the CMP polishing pad 158 after conditioning for a predetermined period of time with the CMP conditioning disk 100. In some embodiments, the PSR comparison circuitry 122 may generate multiple PSRRs for a given combination of CMP conditioning disk 100 and CMP polishing pad 158, reflecting PSR changes after different conditioning times. For example, a first PSRR may represent a ratio between an "unconditioned PSR" and a PSR after conditioning for a period of time T, while the

second PSR may represent a ratio between the unconditioned PSR and a PSR after conditioning for a period of time $2T$.

[0044] When a PSRR is used to compare two different designs of CMP conditioning disks 100, the amount of conditioning time used when generating the PSRR may be selected to enable an appropriate comparison between the two CMP conditioning disks 100. In some embodiments, the amount of conditioning time may be the amount of time required to achieve removal of material of the CMP polishing pad 158 to a predetermined depth. Since the properties of the CMP polishing pad 158 may vary as a function of depth, comparing the PSRs achieved by two different CMP conditioning disks 100 may be most appropriate when the surfaces measured are at the same "depth" in the CMP polishing pad 158. For example, if the desired depth is d , and a first conditioning disk 100 takes 5 minutes to remove material from the CMP polishing pad 158 to a depth d , the PSRR of the first conditioning disk 100 may be a ratio between the PSR of the unconditioned CMP polishing pad 158 and the PSR after 5 minutes of polishing with the first conditioning disk 100. If a second conditioning disk 100 takes 10 minutes to remove material from the CMP polishing pad 158 to a depth d , the PSR of the second conditioning disk 100 may be a ratio between the PSR of the unconditioned CMP polishing pad 158 and the PSR after 10 minutes of polishing with the second conditioning disk 100. In this manner, the PSRRs of the first and second conditioning disks 100 may be based on a "normalized" conditioning time (i.e., the time required to achieve a depth of removal d), which may facilitate a particularly useful comparison. In some applications (e.g., when comparing CMP conditioning disks 100 of the same design), non-normalized times may be used to generate the PSRR and slope/correlation coefficient metrics.

[0045] Table 1 lists a number of example PSRRs for different sample CMP conditioning disks 100 when tested on the same design of the CMP polishing pad 158 under the same operating conditions (e.g., platen rotation rate, disk arm rotation rate, conditioning disk downforce, etc.). In particular, PSRRs based on two different PSRs (R_a and R_q) are shown, as are PSRRs taken at two different normalized conditioning times. These PSRRs represent the PSR of an unconditioned surface divided by the PSR of the corresponding conditioned surface. Table 1 also lists the corresponding pad cut rates (PCRs) for the same CMP conditioning disks 100, and the ratios between the PCRs of the different CMP conditioning disks 100 and Disk C. These ratios may be used to determine the appropriate conditioning times to generate PSRR; for example, if a conditioning time TC is required to achieve a depth d in the CMP polishing pad 158 for Disk C, then a conditioning time of $TC/4$ may be used to achieve a depth d for Disk A, and a conditioning time of $TC/0.28$ may be used to achieve a depth d for Disk B. As evident from Table 1, PCR is not determinative of PSRR; for example, note that Disk B has a lower PCR than Disk C, but has higher PSRRs.

Disk	PSRR (R_a , time to achieve depth d)	PSRR (R_a , time to achieve depth 2d)	PSRR (R_q , time to achieve depth d)	PSRR (R_q , time to achieve depth 2d)	PCR	PCR/PCR of Disk C
A	1.4	1.8	1.3	1.6	1.42	4
B	1.5	2.2	1.4	1.9	0.1	0.28
C	1.4	1.5	1.3	1.3	0.36	1

Table 1.

[0046] In some embodiments, the PSR change metric generated by the PSR comparison circuitry 122 may be representative of the slope of a linear fit of PSR of a CMP polishing pad 158 versus normalized conditioning time when conditioned by a CMP conditioning disk 100. As discussed above with reference to the PSRR, the normalized conditioning time may be the conditioning time normalized by the time required to achieve a predetermined depth of removal (to facilitate comparison between the PSR change metrics of different CMP polishing pads 100). Use of the normalized time may allow an accurate comparison of the aggressiveness of CMP conditioning disks 100 of different designs by using these CMP conditioning disks to condition a CMP polishing pad 158 for different times specific for each disk design. For example, FIG. 6 is a plot 600 of data 604 of PSR (characterized by R_a) versus normalized conditioning time (where "0" represents no conditioning, "1" represents the time required to achieve a particular depth d of removal of the CMP polishing pad 158, and "2" represents twice the time of "1") for a CMP conditioning disk 100 (in particular, Disk A discussed above with reference to Table 1). All the data 604 may be gathered under the same operating conditions (e.g., platen rotation rate, disk arm rotation rate, conditioning disk downforce, etc.). The plot 600 includes the least mean squares linear fit 602, having an associated slope S and correlation coefficient R^2 . In the example of FIG. 6, the slope S may be approximately -1.1, and the correlation coefficient R^2 may be approximately 0.78. The slope S (optionally along with the correlation coefficient R^2) may provide a PSR change metric.

[0047] FIG. 7 is a plot 700 of data 704 of PSR (characterized by R_q) versus normalized conditioning time (as discussed with reference to FIG. 6) for a CMP conditioning disk 100 (in particular, Disk A discussed above with reference to Table 1). All the data 704 may be gathered under the same operating conditions (e.g., platen rotation rate, disk arm rotation rate, conditioning disk downforce, etc.). The plot 700 includes the least mean squares linear fit 702, having an associated slope S and correlation coefficient R^2 . In the example of FIG. 7, the slope S may be approximately -1.2 and the correlation coefficient may be approximately 0.75. The slope S (optionally along with the correlation coefficient R^2) may provide a PSR change metric. Table 2 lists a number of example PSRRs for the different sample CMP conditioning disks 100 of Table 1 when tested on the same design of the CMP polishing pad 158 under the same operating conditions (e.g., platen rotation rate, disk arm rotation

rate, conditioning disk downforce, etc.). In particular, slopes S and correlation coefficients R^2 based on two different PSRs (R_a and R_q) are shown. Table 2 also lists the corresponding pad cut rates (PCRs) for the same CMP conditioning disks 100. As evident from Table 2, PCR is not determinative of slope S ; for example, note that Disk B has a lower PCR than Disk C but has steeper values of the slope S .

Disk	$S (R_a)$	$R^2 (R_a)$	$S (R_q)$	$R^2 (R_q)$	PCR
A	-0.71	0.92	-0.75	0.89	1.42
B	-1.1	0.78	-1.2	0.75	0.4
C	-0.51	0.9	-0.51	0.5	0.36

Table 2.

[0048] Embodiments of various techniques for generating PSR change metrics for different CMP conditioning disks 100 are discussed below with reference to FIG. 10. As noted above, a PSR change metric may be associated with a particular set of operating conditions (e.g., platen rotation rate, disk arm rotation rate, conditioning disk downforce, etc.). Different PSR change metrics may be generated under different operating conditions (e.g., a slope S and correlation coefficient R^2 under a downforce of 5 lbs., and a different slope S and correlation coefficient R^2 under a downforce of 10 lbs.).

[0049] In some embodiments, a PSR change metric generated by the PSR change metric generation system 108 may be provided to the control circuitry 102, stored in the memory 110, and used by the control circuitry 102 to control the conditioning time of the CMP polishing pad 158 by the CMP conditioning disk 100. In particular, the control circuitry 102 may include conditioning time generation circuitry 112. The conditioning time generation circuitry 112 may be configured to access a stored PSR change metric for the CMP polishing pad 158 and the CMP conditioning disk 100 (e.g., from the memory 110), and generate (based on the accessed PSR change metric) a conditioning time for conditioning the CMP polishing pad 158 with the CMP conditioning disk 100 to achieve a target PSR for the CMP polishing pad 158. For example, with reference to Table 1, if the CMP conditioning disk 100 is Disk A, the value of R_q for the unconditioned CMP polishing pad 158 is R_{q0} , and the target value of R_q for the CMP polishing pad is $(5/8) \cdot R_{q0}$, the CMP polishing pad 158 may be conditioned by the CMP conditioning disk 100 for approximately two normalized time units. In another example, with reference to Table 2, if the CMP conditioning disk 100 is Disk A, the value of R_a for the unconditioned CMP polishing pad 158 is 4, and the target value of R_a for the CMP polishing pad 158 is 2.9, the CMP polishing pad 158 may be conditioned by the CMP conditioning disk 100 for approximately $4 - (1.5)(0.71) = 2.9$ normalized time units.

[0050] The conditioning time generation circuitry 112 may access the normalization factor (used to convert between normalized time units and "actual" time units, and based on the depth d) from the

memory 110 to generate an "actual" conditioning time. In particular, the normalization factor may represent the amount of time required to achieve a depth of removal d in the CMP polishing pad 158. In some embodiments, the conditioning time generation circuitry 112 may provide the generated conditioning time to the arm control circuitry 116 (e.g., as part of a control instruction). In response, the arm control circuitry 116 may cause the CMP conditioning disk 100 to condition the CMP polishing pad 158 for the generated conditioning time (e.g., via a control instruction for the first arm 152 and/or the second arm 154). Embodiments of various techniques for controlling the conditioning time of the CMP system 150 are discussed below with reference to FIG. 11.

[0051] The PSR of the CMP polishing pad 158 may have a functional relationship with the rate at which material from the wafer 160 is removed when the wafer 160 is polished with the CMP polishing pad 158 (referred to herein as the wafer removal rate (WRR)). For example, FIGS. 8 and 9 are plots depicting different functional relationships between WRR and PSR in the CMP system 150, in accordance with various embodiments. FIG. 8 is a plot 800 including data 804 representative of different WRRs as a function of the PSR of the CMP polishing pad 158 (represented by R_a). The plot 800 also includes a second order polynomial fit 802 to the data 804. As an example, the second order polynomial fit 802 of FIG. 8 may take the approximate form:

$$399 + 80PSR - 63(PSR - 3.86)^2$$

[0052] The second order polynomial fit 802, or another suitable fit, may be stored in the memory 110 and used to represent the functional relationship between WRR and PSR.

[0053] FIG. 9 is a plot 900 including data 904 representative of different WRRs as a function of the PSR of the CMP polishing pad 158 (represented by R_q). The plot 900 also includes a second order polynomial fit 902 to the data 904. As an example, the second order polynomial fit 802 of FIG. 8 may take the approximate form:

$$456 + 49PSR - 25(PSR - 5.09)^2$$

[0054] The second order polynomial fit 902, or another suitable fit, may be stored in the memory 110 and used to represent the functional relationship between WRR and PSR.

[0055] In some embodiments, the control circuitry 102 may be configured to control the polishing time of the wafer 160 based on the PSR of the CMP polishing pad 158. In particular, the control circuitry 102 may include polishing time generation circuitry 114. The polishing time generation circuitry 114 may be configured to use a functional relationship (stored, e.g., in the memory 110) between the PSR of the CMP polishing pad 158 and the WRR of the CMP polishing pad 158 to generate a polishing time to achieve a target amount of wafer removal from the wafer 160. For example, in the embodiment represented by FIG. 8, to achieve a WRR of approximately 700 Angstroms/minute, the target value of R_a may be approximately 4. In some embodiments, the

polishing time generation circuitry 114 may provide the generated polishing time to the arm control circuitry 116 (e.g., as part of a control instruction). In response, the arm control circuitry 116 may cause the CMP polishing pad 158 to polish the wafer 160 for the generated polishing time (e.g., via a control instruction for the second arm 154 and/or the third arm 156). Embodiments of various techniques for generating the functional relationship between the PSR and the WRR, and for controlling the polishing time of the CMP system 150 are discussed below with reference to FIGS. 12 and 13.

[0056] Communication within the CMP system 150 may occur over wired communication pathways and/or wireless communication pathways, over direct couplings, and/or over personal, local, and/or wide area networks. The components of the CMP system 150 (e.g., the control circuitry 102 and the PSR change metric generation system 108) may include suitable hardware for supporting the communication pathways, such as network interface cards, modems, Wi-Fi devices, Bluetooth devices, and so forth. The control circuitry 102 and the PSR change metric generation system 108 may each include a processing device (not shown) and accompanying storage (e.g., the memory 110 and the memory 118, respectively). The processing device may include one or more processing devices, such as one or more processing cores, ASICs, electronic circuits, processors (shared, dedicated, or group), combinational logic circuits, and/or other suitable components that may be configured to process electronic data. The storage may include any suitable memory or mass storage devices (such as solid-state drive, diskette, hard drive, compact disc read-only memory (CD-ROM), and so forth). Different ones of the components of the CMP system 150 may include one or more buses (and bus bridges, if suitable) to communicatively couple the processing device, the storage, and any other devices included in the respective components. The storage (e.g., the memory 110 and/or the memory 118) may include a set of computational logic, which may include one or more copies of computer readable media having instructions stored therein, which, when executed by the processing device of the component, may cause the component to implement any suitable ones of the techniques and methods disclosed herein, or any portion thereof.

[0057] In some embodiments, the I/O devices 124 may include one or more communication devices. The communication devices may enable wired and/or wireless communications for the transfer of data to, from, and/or between components of the CMP system 150. The communication devices may support one or more wired communication protocols, such as inter-integrated circuit (I2C), universal serial bus (USB), serial peripheral interface (SPI), or any other communication protocol. Multiple communication devices included in the I/O devices 124 may enable communication in accordance with different communication protocols.

[0058] In some embodiments, the I/O devices 124 may include a display device. The display device may provide a visual representation of any of the data discussed herein with reference to the operation of the CMP system 150 (e.g., PCR values, PSRR values, PSR change metric values, functional relationships between WRR and PSR, operating conditions, etc.). The display device may include one or more heads-up displays (i.e., displays including a projector arranged in an optical collimator configuration and a combiner to provide data without requiring a user to look away from his or her typical viewpoint), computer monitors, projectors, touchscreen displays, liquid crystal displays (LCDs), light-emitting diode displays, or flat panel displays, for example. Examples of other devices that may be included in the I/O devices 124 may include a keyboard, a cursor control device such as a mouse, a stylus, a touchpad, a bar code reader, a Quick Response (QR) code reader, a radio frequency identification (RFID) reader, a GPS receiver, an audio capture device (which may include one or more microphones arranged in various configurations), one or more speakers or other audio transducers (which may be, e.g., mounted in one or more earphones or earbuds), printers, projectors, or any suitable I/O device. Input devices included in the I/O devices 124 (e.g., a keyboard or touchscreen) may be used to receive user selections of operating conditions for the CMP system 150 (e.g., platen rotation rate, disk arm swing, disk rotation rate, downforce, conditioning time, polishing time, etc.) or any other selections or indications relevant to the operation of the CMP system 150.

[0059] FIG. 10 is a flow diagram of a method 1000 of characterizing one or more CMP conditioning disks, in accordance with various embodiments. Although various operations of the method 1000 (and the other methods disclosed herein) may be illustrated with reference to the CMP system 150, the method 1000 may be performed using any suitable devices. Any of the methods disclosed herein may be performed by suitable ones of the components of the CMP system 150, in accordance with the present disclosure.

[0060] At 1002, a number D may be set, representative of a number of CMP conditioning disks to be tested. In some embodiments, the number D may be input to the control circuitry 102 via an input device (e.g., as indicators from a keyboard or touchscreen) included in the I/O devices 124. In some embodiments, the number D may be input to the control circuitry 102 via a programmed set of instructions.

[0061] At 1004, a number Z may be set, representative of a number of zones of a CMP polishing pad that will be tested. As discussed above with reference to FIGS. 2-4, the maximum possible value of Z may depend on the relative dimensions of the CMP conditioning disk 100 and the CMP polishing pad 158 that will be used during testing. In some embodiments, the number Z may be input to the control circuitry 102 via an input device (e.g., as indicators from a keyboard or touchscreen) included

in the I/O devices 124. In some embodiments, the number Z may be input to the control circuitry 102 via a programmed set of instructions.

[0062] At 1006, a conditioning time multiple $M(j)$ may be set for each of the number of zones $j=1,...,Z$. The conditioning time multiple M may represent the total conditioning time for the particular zone j as a multiple of the normalized conditioning time. As discussed above, the normalized conditioning time may be a conditioning time required to achieve a particular depth of removal of material from the CMP polishing pad 158. The conditioning time multiples $M(j)$ may take any value greater than 0. In some embodiments, the numbers $M(j)$ may be input to the control circuitry 102 via an input device (e.g., as indicators from a keyboard or touchscreen) included in the I/O devices 124. In some embodiments, the numbers $M(j)$ may be input to the control circuitry 102 via a programmed set of instructions.

[0063] At 1008, a counter variable i may be set equal to 1. This may be done automatically by the control circuitry 102.

[0064] At 1010, a PCR of CMP conditioning disk i ($PCR(i)$) may be determined. This determination may be performed in accordance with any of the embodiments discussed herein. In some embodiments, the PCR of CMP conditioning disk i may be already known (e.g., from previous testing or manufacturer materials); in such embodiments, the operations discussed with reference to 1010 may not be performed, and instead, the PCR may be accessed from a memory (e.g., the memory 110 or the memory 118) or the PCR may be input to the control circuitry 102 via the I/O devices 124.

[0065] At 1012, a time T may be determined for CMP conditioning disk i to achieve a predetermined CMP polishing pad removal depth d , based on $PCR(i)$. This time may be referred to as $T(i)$, and may be the normalization factor for CMP conditioning disk i . The time $T(i)$ may be calculated in accordance with

$$T(i) = \frac{d}{PCR(i)}$$

[0066] In some embodiments, the value of d may be input to the control circuitry 102 via an input device (e.g., as indicators from a keyboard or touchscreen) included in the I/O devices 124. In some embodiments, the value of d may be input to the control circuitry 102 via a programmed set of instructions.

[0067] At 1014, a counter variable j may be set equal to 1. This may be done automatically by the control circuitry 102.

[0068] At 1016, a CMP polishing pad may be conditioned, by the CMP conditioning disk i , in zone j , for a conditioning time equal to $M(j)T(i)$. This conditioning may occur under the control of the arm control circuitry 116.

[0069] At 1018, the counter variable j may be compared to the zone number Z to determine if $j=Z$ (i.e., if all zones have been conditioned). If j does not equal Z , the value of the counter variable j may be incremented at 1026 (e.g., automatically by the control circuitry 102), and the method may return to 1016, at which the CMP polishing pad may be conditioned, by the CMP conditioning disk i , in zone j , for a conditioning time equal to $M(j)T(i)$.

[0070] If it is determined at 1018 that the counter variable j is equal to Z , the method may proceed to 1020 and a PSR may be determined for each of the zones $j=1,...,Z$. The PSR for zone j may be referred to as $PSR(j)$. At 1018, a PSR for an unconditioned zone of the CMP polishing pad may also be determined; the PSR for this zone may be referred to as $PSR(0)$. The PSRs of the different zones may be determined at 1018 in accordance with any of the embodiments discussed above (e.g., using the profilometer 120).

[0071] At 1022, a PSRR may be generated for each of the zones $j=1,...,Z$ based on the PSRs determined at 1020. In particular, the PSRR for zone j , $PSRR(j)$, may be calculated in accordance with:

$$PSRR(j) = \frac{PSR(0)}{PSR(j)}$$

[0072] In some embodiments, the PSRRs may be generated at 1022 by the PSR comparison circuitry 122. Although the PSRR in the expression above has $PSR(0)$ in the numerator and $PSR(j)$ in the denominator, the PSRR may instead take the form of $PSR(j)/PSR(0)$, or any other suitable ratio. The PSRRs calculated at 1022 may be stored in a memory (e.g., the memory 110 and/or the memory 118). In some embodiments, the operations discussed above with reference to 1022 may not be performed, and no PSRR may be calculated.

[0073] At 1024, a slope S and a correlation coefficient R^2 may be generated as a linear fit of $PSR(j)$ as a function of $M(j)$ for all of $j=1,...,Z$ (e.g., a minimum mean square fit or another suitable fit). The generation of the slope S and the correlation coefficient R^2 may be performed as discussed above with reference to FIGS. 6 and 7. In some embodiments, the slope S and the correlation coefficient R^2 may be stored in a memory (e.g., the memory 110 and/or the memory 118). In some embodiments, the operations discussed above with reference to 1024 may not be performed, and no slope S or correlation coefficient R^2 may be calculated.

[0074] At 1028, the counter variable i may be compared with the disk number D to determine if $i=D$ (i.e., if all CMP conditioning disks have been tested). If i does not equal D , the value of the counter variable i may be incremented at 1030 (e.g., automatically by the control circuitry 102), and the method may return to 1010, at which the PCR for the CMP conditioning disk i may be determined. If it is determined at 1028 that the counter variable i is equal to D , the method may end.

[0075] FIG. 11 is a flow diagram of a method 1100 of conditioning a CMP polishing pad with a CMP conditioning disk characterized by a PSR change metric, in accordance with various embodiments.

[0076] At 1102, an initial PSR of a CMP polishing pad may be set. This initial PSR may represent, for example, a PSR of an unconditioned CMP polishing pad 158. In some embodiments, the initial PSR may be input to the control circuitry 102 via an input device (e.g., as indicators from a keyboard or touchscreen) included in the I/O devices 124. In some embodiments, the initial PSR may be input to the control circuitry 102 via a programmed set of instructions. In some embodiments, the initial PSR may be generated by the profilometer 120 and/or provided to the control circuitry 102 by the profilometer 120.

[0077] At 1104, a target PSR of the CMP polishing pad of 1102 may be set. This target PSR may represent a desired PSR for at least a portion of the CMP polishing pad. In some embodiments, the target PSR may be input to the control circuitry 102 via an input device (e.g., as indicators from a keyboard or touchscreen) included in the I/O devices 124. In some embodiments, the target PSR may be input to the control circuitry 102 via a programmed set of instructions. In some embodiments, the target PSR may be selected based on a target WRR and a known functional relationship between WRR and PSR for the CMP polishing pad 158, as discussed above with reference to FIGS. 6 and 7. In some such embodiments, the target WRR may be set at 1104, and the control circuitry 102 may identify the corresponding target PSR based on the known functional relationship (e.g., stored in the memory 110).

[0078] At 1106, a conditioning time may be generated, using a PSR change metric for a CMP conditioning disk in the CMP system, to achieve the target PSR from the initial PSR. In some embodiments the conditioning time generation circuitry 112 may generate the conditioning time at 1106. The generation of the conditioning time at 1106 may be performed in accordance with any of the techniques disclosed herein. For example, if the PSR change metric is the PSRR of Table 1, the CMP conditioning disk 100 is Disk A, the value of R_q for the unconditioned CMP polishing pad 158 is R_{q0} , and the target value of R_q for the CMP polishing pad is $(5/8) \cdot R_{q0}$, the CMP polishing pad 158 may be conditioned by the CMP conditioning disk 100 for approximately two normalized time units. In another example, if the PSR change metric is the slope S of Table 2, the CMP conditioning disk 100 is Disk A, the value of R_a for the unconditioned CMP polishing pad 158 is 4, and the target value of R_a for the CMP polishing pad 158 is 2.9, the CMP polishing pad 158 may be conditioned by the CMP conditioning disk 100 for approximately $4 - (1.5)(0.71) = 2.9$ normalized time units. The conditioning time generation circuitry 112 may convert the normalized time units into "actual" time units by multiplying the number of normalized time units by the corresponding normalization factor (stored, e.g., in the memory 110).

[0079] At 1108, the CMP system may be controlled to condition the CMP polishing pad with the CMP conditioning disk for the conditioning time generated at 1106. For example, in some embodiments, the conditioning time generation circuitry 112 may provide the conditioning time generated at 1106 to the arm control circuitry 116, and the arm control circuitry 116 may cause the conditioning of the CMP polishing pad 158 with the CMP conditioning disk 100 for the generated conditioning time. Upon conditioning, the CMP polishing pad 158 may have approximately the target PSR. The method 1100 may then end.

[0080] FIG. 12 is a flow diagram of a method 1200 of generating a functional relationship between WRR and PSR in a CMP system, in accordance with various embodiments.

[0081] At 1202, a number P may be set, representative of a number of CMP polishing pads to be tested. In some embodiments, the number P may be input to the control circuitry 102 via an input device (e.g., as indicators from a keyboard or touchscreen) included in the I/O devices 124. In some embodiments, the number P may be input to the control circuitry 102 via a programmed set of instructions.

[0082] At 1204, a counter variable i may be set equal to 1. This may be done automatically by the control circuitry 102.

[0083] At 1206, a PSR may be determined for the CMP polishing pad i. This PSR may be referred to as PSR(i) and may be determined at 1206 in accordance with any of the embodiments discussed above (e.g., using the profilometer 120).

[0084] At 1208, a WRR may be determined for the CMP polishing pad i. This WRR may be referred to as WRR(i) and may be determined using any suitable technique (e.g., polishing a wafer with the CMP polishing pad i for a period of time, then measuring the amount of wafer removed and normalizing that amount by the period).

[0085] At 1210, the counter variable i may be compared with the pad number P to determine if $i=P$ (i.e., if all CMP polishing pads have been tested). If i does not equal P, the value of the counter variable i may be incremented at 1214 (e.g., automatically by the control circuitry 102), and the method may return to 1206, at which the PSR for the CMP polishing pad may be determined.

[0086] If it is determined at 1210 that the counter variable i is equal to P, the method 1200 may proceed to 1212 and a functional relationship may be generated between WRR(i) as a function of PSR(i) for all $i=1, \dots, P$. In some embodiments, the polishing time generation circuitry 114 may access the WRR and PSR data from the memory 110 and fit a curve (e.g., a polynomial) to the data to parameterize this functional relationship. Examples of such parameterizations were discussed above with reference to FIGS. 8 and 9, and any suitable parameterization may occur at 1212. The

functional relationship generated at 1212 may be stored in a memory (e.g., the memory 110). The method 1200 may then end.

[0087] FIG. 13 is a flow diagram of a method 1300 of controlling a CMP system to polish a wafer using a CMP polishing pad having a particular PSR, in accordance with various embodiments.

[0088] At 1302, a target wafer removal amount may be set. This target wafer removal amount may represent, for example, an amount of the wafer 160 to be removed by polishing with the CMP polishing pad 158. In some embodiments, the target wafer removal amount may be input to the control circuitry 102 via an input device (e.g., as indicators from a keyboard or touchscreen) included in the I/O devices 124. In some embodiments, the target wafer removal amount may be input to the control circuitry 102 via a programmed set of instructions.

[0089] At 1304, a polishing time may be generated, using a functional relationship between PSR and WRR of the CMP polishing pad (stored, e.g., in the memory 110), to achieve the target wafer removal amount. In some embodiments, the polishing time generation circuitry 114 may generate the polishing time at 1304. The generation of the polishing time at 1304 may be performed in accordance with any of the techniques disclosed herein. For example, if the PSR of the CMP polishing pad that will be used to polish the wafer is approximately 4, in the embodiment represented by FIG. 8, the CMP polishing pad will have a WRR of approximately 700 Angstroms/minute. If the target wafer removal amount of 1302 is 350 Angstroms, the polishing time generated at 1304 may be 30 seconds.

[0090] At 1306, the CMP system may be controlled to polish the wafer with the CMP polishing pad for the polishing time generated at 1304. For example, in some embodiments, the polishing time generation circuitry 114 may provide the polishing time generated at 1304 to the arm control circuitry 116, and the arm control circuitry 116 may cause the polishing of the wafer 160 by the CMP polishing pad 158 for the generated polishing time. Upon polishing, the target wafer removal amount may be removed from the wafer 160. The method 1300 may then end.

[0091] Devices processed using the CMP systems and techniques disclosed herein (e.g., polished for a polishing time determined by the PSR of the CMP polishing pad, polished by CMP polishing pads conditioned to have a particular PSR, and/or conditioned by a CMP conditioning disk characterized using the techniques disclosed herein) may be included in any suitable electronic device. FIGS. 14-17 illustrate various examples of apparatuses that may include devices processed using the CMP systems and techniques disclosed herein.

[0092] FIGS. 14A-B are top views of a wafer 1400 and dies 1402 that may be processed using CMP systems and techniques in accordance with any of the embodiments disclosed herein. In particular, the wafer 1400 may be the wafer 160 polished in the CMP system 150 of FIG. 1. The wafer 1400

may be composed of semiconductor material and may include one or more dies 1402 having integrated circuit (IC) structures formed on a surface of the wafer 1400. Each of the dies 1402 may be a repeating unit of a semiconductor product that includes any suitable IC. After the fabrication of the semiconductor product is complete (e.g., after the semiconductor product is polished in accordance with any of the techniques disclosed herein), the wafer 1400 may undergo a singulation process in which each of the dies 1402 is separated from one another to provide discrete "chips" of the semiconductor product. In particular, devices processed using the CMP systems and techniques disclosed herein may take the form of the wafer 1400 (e.g., not singulated) or the form of the die 1402 (e.g., singulated). The die 1402 may include one or more transistors (e.g., some of the transistor(s) 1540 of FIG. 15, discussed below) and/or supporting circuitry to route electrical signals to the transistors, as well as any other IC components. In some embodiments, the wafer 1400 or the die 1402 may include a memory device (e.g., a static random access memory (SRAM) device), a logic device (e.g., an AND, OR, NAND, or NOR gate), or any other suitable circuit element. Multiple ones of these devices may be combined on a single die 1402. For example, a memory array formed by multiple memory devices may be formed on a same die 1402 as a processing device (e.g., the processing device 1702 of FIG. 17) or other logic that is configured to store information in the memory devices or execute instructions stored in the memory array.

[0093] FIG. 15 is a cross-sectional side view of an IC device 1500 that may be processed using CMP systems and techniques in accordance with any of the embodiments disclosed herein. The IC device 1500 may be formed on a substrate 1502 (e.g., the wafer 1400 of FIG. 14A) and may be included in a die (e.g., the die 1402 of FIG. 14B). The substrate 1502 may be a semiconductor substrate composed of semiconductor material systems including, for example, N-type or P-type materials systems. The substrate 1502 may include, for example, a crystalline substrate formed using a bulk silicon or a silicon-on-insulator substructure. In some embodiments, the semiconductor substrate 1502 may be formed using alternative materials, which may or may not be combined with silicon, that include but are not limited to germanium, indium antimonide, lead telluride, indium arsenide, indium phosphide, gallium arsenide, or gallium antimonide. Further materials classified as group II-VI, III-V, or IV may also be used to form the substrate 1502. Although a few examples of materials from which the substrate 1502 may be formed are described here, any material that may serve as a foundation for an IC device 1500 may be used. The substrate 1502 may be part of a singulated die (e.g., the dies 1402 of FIG. 14B) or a wafer (e.g., the wafer 1400 of FIG. 14A).

[0094] The IC device 1500 may include one or more device layers 1504 disposed on the substrate 1502. The device layer 1504 may include features of one or more transistors 1540 (e.g., metal oxide semiconductor field-effect transistors (MOSFETs)) formed on the substrate 1502. The device layer

1504 may include, for example, one or more source and/or drain (S/D) regions 1520, a gate 1522 to control current flow in the transistors 1540 between the S/D regions 1520, and one or more S/D contacts 1524 to route electrical signals to/from the S/D regions 1520. The transistors 1540 may include additional features not depicted for the sake of clarity, such as device isolation regions, gate contacts, and the like. The transistors 1540 are not limited to the type and configuration depicted in FIG. 15 and may include a wide variety of other types and configurations such as, for example, planar transistors, non-planar transistors, or a combination of both. Non-planar transistors may include FinFET transistors, such as double-gate transistors or tri-gate transistors, and wrap-around or all-around gate transistors, such as nanoribbon and nanowire transistors.

[0095] Each transistor 1540 may include a gate 1522 formed of at least two layers, a gate dielectric layer and a gate electrode layer. The gate dielectric layer may include one layer or a stack of layers. The one or more layers may include silicon oxide, silicon dioxide, and/or a high-k dielectric material. The high-k dielectric material may include elements such as hafnium, silicon, oxygen, titanium, tantalum, lanthanum, aluminum, zirconium, barium, strontium, yttrium, lead, scandium, niobium, and zinc. Examples of high-k materials that may be used in the gate dielectric layer include, but are not limited to, hafnium oxide, hafnium silicon oxide, lanthanum oxide, lanthanum aluminum oxide, zirconium oxide, zirconium silicon oxide, tantalum oxide, titanium oxide, barium strontium titanium oxide, barium titanium oxide, strontium titanium oxide, yttrium oxide, aluminum oxide, lead scandium tantalum oxide, and lead zinc niobate. In some embodiments, an annealing process may be carried out on the gate dielectric layer to improve its quality when a high-k material is used.

[0096] The gate electrode layer may be formed on the gate dielectric layer and may include at least one P-type work function metal or N-type work function metal, depending on whether the transistor 1540 is to be a PMOS or an NMOS transistor. In some implementations, the gate electrode layer may consist of a stack of two or more metal layers, where one or more metal layers are work function metal layers and at least one metal layer is a fill metal layer. Further metal layers may be included for other purposes, such as a barrier layer. For a PMOS transistor, metals that may be used for the gate electrode include, but are not limited to, ruthenium, palladium, platinum, cobalt, nickel, and conductive metal oxides (e.g., ruthenium oxide). For an NMOS transistor, metals that may be used for the gate electrode include, but are not limited to, hafnium, zirconium, titanium, tantalum, aluminum, alloys of these metals, and carbides of these metals (e.g., hafnium carbide, zirconium carbide, titanium carbide, tantalum carbide, and aluminum carbide).

[0097] In some embodiments, when viewed as a cross-section of the transistor 1540 along the source-channel-drain direction, the gate electrode may consist of a U-shaped structure that includes a bottom portion substantially parallel to the surface of the substrate and two sidewall portions that

are substantially perpendicular to the top surface of the substrate. In other embodiments, at least one of the metal layers that form the gate electrode may simply be a planar layer that is substantially parallel to the top surface of the substrate and does not include sidewall portions substantially perpendicular to the top surface of the substrate. In other embodiments, the gate electrode may consist of a combination of U-shaped structures and planar, non-U-shaped structures. For example, the gate electrode may consist of one or more U-shaped metal layers formed atop one or more planar, non-U-shaped layers.

[0098] In some embodiments, a pair of sidewall spacers may be formed on opposing sides of the gate stack to bracket the gate stack. The sidewall spacers may be formed from a material such as silicon nitride, silicon oxide, silicon carbide, silicon nitride doped with carbon, and silicon oxynitride. Processes for forming sidewall spacers are well known in the art and generally include deposition and etching process steps. In some embodiments, a plurality of spacer pairs may be used; for instance, two pairs, three pairs, or four pairs of sidewall spacers may be formed on opposing sides of the gate stack.

[0099] The S/D regions 1520 may be formed within the substrate 1502 adjacent to the gate 1522 of each transistor 1540. The S/D regions 1520 may be formed using either an implantation/diffusion process or an etching/deposition process, for example. In the former process, dopants such as boron, aluminum, antimony, phosphorous, or arsenic may be ion-implanted into the substrate 1502 to form the S/D regions 1520. An annealing process that activates the dopants and causes them to diffuse farther into the substrate 1502 may follow the ion implantation process. In the latter process, the substrate 1502 may first be etched to form recesses at the locations of the S/D regions 1520. An epitaxial deposition process may then be carried out to fill the recesses with material that is used to fabricate the S/D regions 1520. In some implementations, the S/D regions 1520 may be fabricated using a silicon alloy such as silicon germanium or silicon carbide. In some embodiments, the epitaxially deposited silicon alloy may be doped in situ with dopants such as boron, arsenic, or phosphorous. In some embodiments, the S/D regions 1520 may be formed using one or more alternate semiconductor materials such as germanium or a group III-V material or alloy. In further embodiments, one or more layers of metal and/or metal alloys may be used to form the S/D regions 1520.

[0100] Electrical signals, such as power and/or input/output (I/O) signals, may be routed to and/or from the transistors 1540 of the device layer 1504 through one or more interconnect layers disposed on the device layer 1504 (illustrated in FIG. 15 as interconnect layers 1506-1510). For example, electrically conductive features of the device layer 1504 (e.g., the gate 1522 and the S/D contacts 1524) may be electrically coupled with the interconnect structures 1528 of the interconnect layers

1506-1510. The one or more interconnect layers 1506-1510 may form an interlayer dielectric (ILD) stack 1519 of the IC device 1500.

[0101] The interconnect structures 1528 may be arranged within the interconnect layers 1506-1510 to route electrical signals according to a wide variety of designs (in particular, the arrangement is not limited to the particular configuration of interconnect structures 1528 depicted in FIG. 15). Although a particular number of interconnect layers 1506-1510 is depicted in FIG. 15, embodiments of the present disclosure include IC devices having more or fewer interconnect layers than depicted.

[0102] In some embodiments, the interconnect structures 1528 may include trench structures 1528a (sometimes referred to as "lines") and/or via structures 1528b (sometimes referred to as "holes") filled with an electrically conductive material such as a metal. The trench structures 1528a may be arranged to route electrical signals in a direction of a plane that is substantially parallel with a surface of the substrate 1502 upon which the device layer 1504 is formed. For example, the trench structures 1528a may route electrical signals in a direction in and out of the page from the perspective of FIG. 15. The via structures 1528b may be arranged to route electrical signals in a direction of a plane that is substantially perpendicular to the surface of the substrate 1502 upon which the device layer 1504 is formed. In some embodiments, the via structures 1528b may electrically couple trench structures 1528a of different interconnect layers 1506-1510 together.

[0103] The interconnect layers 1506-1510 may include a dielectric material 1526 disposed between the interconnect structures 1528, as shown in FIG. 15. In some embodiments, the dielectric material 1526 disposed between the interconnect structures 1528 in different ones of the interconnect layers 1506-1510 may have different compositions; in other embodiments, the composition of the dielectric material 1526 between different interconnect layers 1506-1510 may be the same.

[0104] A first interconnect layer 1506 (referred to as Metal 1 or "M1") may be formed directly on the device layer 1504. In some embodiments, the first interconnect layer 1506 may include trench structures 1528a and/or via structures 1528b, as shown. The trench structures 1528a of the first interconnect layer 1506 may be coupled with contacts (e.g., the S/D contacts 1524) of the device layer 1504.

[0105] A second interconnect layer 1508 (referred to as Metal 2 or "M2") may be formed directly on the first interconnect layer 1506. In some embodiments, the second interconnect layer 1508 may include via structures 1528b to couple the trench structures 1528a of the second interconnect layer 1508 with the trench structures 1528a of the first interconnect layer 1506. Although the trench structures 1528a and the via structures 1528b are structurally delineated with a line within each interconnect layer (e.g., within the second interconnect layer 1508) for the sake of clarity, the trench

structures 1528a and the via structures 1528b may be structurally and/or materially contiguous (e.g., simultaneously filled during a dual-damascene process) in some embodiments.

[0106] A third interconnect layer 1510 (referred to as Metal 3 or "M3") (and additional interconnect layers, as desired) may be formed in succession on the second interconnect layer 1508 according to similar techniques and configurations described in connection with the second interconnect layer 1508 or the first interconnect layer 1506.

[0107] The IC device 1500 may include a solder resist material 1534 (e.g., polyimide or similar material) and one or more bond pads 1536 formed on the interconnect layers 1506-1510. The bond pads 1536 may be electrically coupled with the interconnect structures 1528 and configured to route the electrical signals of the transistor(s) 1540 to other external devices. For example, solder bonds may be formed on the one or more bond pads 1536 to mechanically and/or electrically couple a chip including the IC device 1500 with another component (e.g., a circuit board). The IC device 1500 may have other alternative configurations to route the electrical signals from the interconnect layers 1506-1510 than depicted in other embodiments. For example, the bond pads 1536 may be replaced by or may further include other analogous features (e.g., posts) that route the electrical signals to external components.

[0108] FIG. 16 is a cross-sectional side view of an IC device assembly 1600 that may include components processed using any of the CMP systems and techniques disclosed herein. The IC device assembly 1600 includes a number of components disposed on a circuit board 1602 (which may be, e.g., a motherboard). The IC device assembly 1600 includes components disposed on a first face 1640 of the circuit board 1602 and an opposing second face 1642 of the circuit board 1602; generally, components may be disposed on one or both faces 1640 and 1642.

[0109] In some embodiments, the circuit board 1602 may be a printed circuit board (PCB) including multiple metal layers separated from one another by layers of dielectric material and interconnected by electrically conductive vias. Any one or more of the metal layers may be formed in a desired circuit pattern to route electrical signals (optionally in conjunction with other metal layers) between the components coupled to the circuit board 1602. In other embodiments, the circuit board 1602 may be a non-PCB substrate.

[0110] The IC device assembly 1600 illustrated in FIG. 16 includes a package-on-interposer structure 1636 coupled to the first face 1640 of the circuit board 1602 by coupling components 1616. The coupling components 1616 may electrically and mechanically couple the package-on-interposer structure 1636 to the circuit board 1602, and may include solder balls (as shown in FIG. 16), male and female portions of a socket, an adhesive, an underfill material, and/or any other suitable electrical and/or mechanical coupling structure.

[0111] The package-on-interposer structure 1636 may include an IC package 1620 coupled to an interposer 1604 by coupling components 1618. The coupling components 1618 may take any suitable form for the application, such as the forms discussed above with reference to the coupling components 1616. Although a single IC package 1620 is shown in FIG. 16, multiple IC packages may be coupled to the interposer 1604; indeed, additional interposers may be coupled to the interposer 1604. The interposer 1604 may provide an intervening substrate used to bridge the circuit board 1602 and the IC package 1620. The IC package 1620 may be or include, for example, a die (the die 1402 of FIG. 14B), an IC device (e.g., the IC device 1500 of FIG. 15), or any other suitable component. Generally, the interposer 1604 may spread a connection to a wider pitch or reroute a connection to a different connection. For example, the interposer 1604 may couple the IC package 1620 (e.g., a die) to a ball grid array (BGA) of the coupling components 1616 for coupling to the circuit board 1602. In the embodiment illustrated in FIG. 16, the IC package 1620 and the circuit board 1602 are attached to opposing sides of the interposer 1604; in other embodiments, the IC package 1620 and the circuit board 1602 may be attached to a same side of the interposer 1604. In some embodiments, three or more components may be interconnected by way of the interposer 1604.

[0112] The interposer 1604 may be formed of an epoxy resin, a fiberglass-reinforced epoxy resin, a ceramic material, or a polymer material such as polyimide. In some implementations, the interposer 1604 may be formed of alternate rigid or flexible materials that may include the same materials described above for use in a semiconductor substrate, such as silicon, germanium, and other group III-V and group IV materials. The interposer 1604 may include metal interconnects 1608 and vias 1610, including but not limited to through-silicon vias (TSVs) 1606. The interposer 1604 may further include embedded devices 1614, including both passive and active devices. Such devices may include, but are not limited to, capacitors, decoupling capacitors, resistors, inductors, fuses, diodes, transformers, sensors, electrostatic discharge (ESD) devices, and memory devices. More complex devices such as radio-frequency (RF) devices, power amplifiers, power management devices, antennas, arrays, sensors, and microelectromechanical systems (MEMS) devices may also be formed on the interposer 1604. The package-on-interposer structure 1636 may take the form of any of the package-on-interposer structures known in the art.

[0113] The IC device assembly 1600 may include an IC package 1624 coupled to the first face 1640 of the circuit board 1602 by coupling components 1622. The coupling components 1622 may take the form of any of the embodiments discussed above with reference to the coupling components 1616, and the IC package 1624 may take the form of any of the embodiments discussed above with reference to the IC package 1620.

[0114] The IC device assembly 1600 illustrated in FIG. 16 includes a package-on-package structure 1634 coupled to the second face 1642 of the circuit board 1602 by coupling components 1628. The package-on-package structure 1634 may include an IC package 1626 and an IC package 1632 coupled together by coupling components 1630 such that the IC package 1626 is disposed between the circuit board 1602 and the IC package 1632. The coupling components 1628 and 1630 may take the form of any of the embodiments of the coupling components 1616 discussed above, and the IC packages 1626 and 1632 may take the form of any of the embodiments of the IC package 1620 discussed above. The package-on-package structure 1634 may be configured in accordance with any of the package-on-package structures known in the art.

[0115] FIG. 17 is a block diagram of an example computing device 1700 that may include one or more components processed using the CMP systems and techniques disclosed herein. For example, any suitable ones of the components of the computing device 1700 may include a die (e.g., the die 1402 (FIG. 14B)) processed using the CMP systems and techniques disclosed herein. Additionally or alternatively, one or more of the computing devices 1700 may be included in the CMP system 150 (e.g., as part of the control circuitry 102 and/or the PSR change metric generation system 108). A number of components are illustrated in FIG. 17 as included in the computing device 1700, but any one or more of these components may be omitted or duplicated, as suitable for the application. In some embodiments, some or all of the components included in the computing device 1700 may be attached to one or more motherboards. In some embodiments, some or all of these components are fabricated onto a single system-on-a-chip (SoC) die.

[0116] Additionally, in various embodiments, the computing device 1700 may not include one or more of the components illustrated in FIG. 17, but the computing device 1700 may include interface circuitry for coupling to the one or more components. For example, the computing device 1700 may not include a display device 1706, but may include display device interface circuitry (e.g., a connector and driver circuitry) to which a display device 1706 may be coupled. In another set of examples, the computing device 1700 may not include an audio input device 1724 or an audio output device 1708, but may include audio input or output device interface circuitry (e.g., connectors and supporting circuitry) to which an audio input device 1724 or audio output device 1708 may be coupled.

[0117] The computing device 1700 may include a processing device 1702 (e.g., one or more processing devices). As used herein, the term "processing device" or "processor" may refer to any device or portion of a device that processes electronic data from registers and/or memory to transform that electronic data into other electronic data that may be stored in registers and/or memory. The processing device 1702 may include one or more digital signal processors (DSPs),

application-specific integrated circuits (ASICs), central processing units (CPUs), graphics processing units (GPUs), cryptoprocessors (specialized processors that execute cryptographic algorithms within hardware), server processors, or any other suitable processing devices. The computing device 1700 may include a memory 1704, which may itself include one or more memory devices such as volatile memory (e.g., dynamic random access memory (DRAM)), nonvolatile memory (e.g., read-only memory (ROM)), flash memory, solid state memory, and/or a hard drive. In some embodiments, the memory 1704 may include memory that shares a die with the processing device 1702. This memory may be used as cache memory and may include embedded dynamic random access memory (eDRAM) or spin transfer torque magnetic random-access memory (STT-MRAM).

[0118] In some embodiments, the computing device 1700 may include a communication chip 1712 (e.g., one or more communication chips). For example, the communication chip 1712 may be configured for managing wireless communications for the transfer of data to and from the computing device 1700. The term "wireless" and its derivatives may be used to describe circuits, devices, systems, methods, techniques, communications channels, etc., that may communicate data through the use of modulated electromagnetic radiation through a nonsolid medium. The term does not imply that the associated devices do not contain any wires, although in some embodiments they might not.

[0119] The communication chip 1712 may implement any of a number of wireless standards or protocols, including but not limited to Institute for Electrical and Electronic Engineers (IEEE) standards including Wi-Fi (IEEE 802.11 family), IEEE 802.16 standards (e.g., IEEE 802.16-2005 Amendment), Long-Term Evolution (LTE) project along with any amendments, updates, and/or revisions (e.g., advanced LTE project, ultra mobile broadband (UMB) project (also referred to as "3GPP2"), etc.). IEEE 802.16 compatible Broadband Wireless Access (BWA) networks are generally referred to as WiMAX networks, an acronym that stands for Worldwide Interoperability for Microwave Access, which is a certification mark for products that pass conformity and interoperability tests for the IEEE 802.16 standards. The communication chip 1712 may operate in accordance with a Global System for Mobile Communication (GSM), General Packet Radio Service (GPRS), Universal Mobile Telecommunications System (UMTS), High Speed Packet Access (HSPA), Evolved HSPA (E-HSPA), or LTE network. The communication chip 1712 may operate in accordance with Enhanced Data for GSM Evolution (EDGE), GSM EDGE Radio Access Network (GERAN), Universal Terrestrial Radio Access Network (UTRAN), or Evolved UTRAN (E-UTRAN). The communication chip 1712 may operate in accordance with Code Division Multiple Access (CDMA), Time Division Multiple Access (TDMA), Digital Enhanced Cordless Telecommunications (DECT), Evolution-Data Optimized (EV-DO), and derivatives thereof, as well as any other wireless protocols that are designated

as 3G, 4G, 5G, and beyond. The communication chip 1712 may operate in accordance with other wireless protocols in other embodiments. The computing device 1700 may include an antenna 1722 to facilitate wireless communications and/or to receive other wireless communications (such as AM or FM radio transmissions).

[0120] In some embodiments, the communication chip 1712 may manage wired communications, such as electrical, optical, or any other suitable communication protocols (e.g., the Ethernet). As noted above, the communication chip 1712 may include multiple communication chips. For instance, a first communication chip 1712 may be dedicated to shorter-range wireless communications such as Wi-Fi or Bluetooth, and a second communication chip 1712 may be dedicated to longer-range wireless communications such as GPS, EDGE, GPRS, CDMA, WiMAX, LTE, EV-DO, or others. In some embodiments, a first communication chip 1712 may be dedicated to wireless communications, and a second communication chip 1712 may be dedicated to wired communications.

[0121] The computing device 1700 may include battery/power circuitry 1714. The battery/power circuitry 1714 may include one or more energy storage devices (e.g., batteries or capacitors) and/or circuitry for coupling components of the computing device 1700 to an energy source separate from the computing device 1700 (e.g., AC line power).

[0122] The computing device 1700 may include a display device 1706 (or corresponding interface circuitry, as discussed above). The display device 1706 may include any visual indicators, such as a heads-up display, a computer monitor, a projector, a touchscreen display, a liquid crystal display (LCD), a light-emitting diode display, or a flat panel display, for example.

[0123] The computing device 1700 may include an audio output device 1708 (or corresponding interface circuitry, as discussed above). The audio output device 1708 may include any device that generates an audible indicator, such as speakers, headsets, or earbuds, for example.

[0124] The computing device 1700 may include an audio input device 1724 (or corresponding interface circuitry, as discussed above). The audio input device 1724 may include any device that generates a signal representative of a sound, such as microphones, microphone arrays, or digital instruments (e.g., instruments having a musical instrument digital interface (MIDI) output).

[0125] The computing device 1700 may include a global positioning system (GPS) device 1718 (or corresponding interface circuitry, as discussed above). The GPS device 1718 may be in communication with a satellite-based system and may receive a location of the computing device 1700, as known in the art.

[0126] The computing device 1700 may include an other output device 1710 (or corresponding interface circuitry, as discussed above). Examples of the other output device 1710 may include an

audio codec, a video codec, a printer, a wired or wireless transmitter for providing information to other devices, or an additional storage device.

[0127] The computing device 1700 may include an other input device 1720 (or corresponding interface circuitry, as discussed above). Examples of the other input device 1720 may include an accelerometer, a gyroscope, a compass, an image capture device, a keyboard, a cursor control device such as a mouse, a stylus, a touchpad, a bar code reader, a Quick Response (QR) code reader, any sensor, or a radio frequency identification (RFID) reader.

[0128] The computing device 1700 may have any desired form factor, such as a hand-held or mobile computing device (e.g., a cell phone, a smart phone, a mobile internet device, a music player, a tablet computer, a laptop computer, a netbook computer, an ultrabook computer, a personal digital assistant (PDA), an ultra-mobile personal computer, etc.), a desktop computing device, a server or other networked computing component, a printer, a scanner, a monitor, a set-top box, an entertainment control unit, a vehicle control unit, a digital camera, a digital video recorder, or a wearable computing device. In some embodiments, the computing device 1700 may be any other electronic device that processes data.

[0129] The following paragraphs provide various examples of the embodiments disclosed herein.

[0130] Example 1 is a chemical mechanical polishing (CMP) system, including: control circuitry to: access a stored pad surface roughness (PSR) change metric for a CMP polishing pad and a CMP conditioning disk, generate, based on the PSR change metric, a conditioning time for conditioning the CMP polishing pad with the CMP conditioning disk to achieve a target PSR for the CMP polishing pad, and cause the CMP conditioning disk to condition the CMP polishing pad for the conditioning time.

[0131] Example 2 may include the subject matter of Example 1, and may further specify that the control circuitry is further to: receive an indicator of an initial PSR of the CMP polishing pad, and an indicator of the target PSR for the CMP polishing pad; and wherein generation of the conditioning time is based on the PSR change metric, the initial PSR, and the target PSR.

[0132] Example 3 may include the subject matter of any of Examples 1-2, and may further specify that cause the CMP conditioning disk to condition the CMP polishing pad for the conditioning time includes generate, based on the conditioning time, a control instruction for a first arm or a second arm of the CMP system, wherein the CMP conditioning disk is coupled to the first arm, and the CMP polishing pad is coupled to the second arm.

[0133] Example 4 may include the subject matter of Example 3, and may further specify that the second arm includes a platen.

[0134] Example 5 may include the subject matter of any of Examples 3-4, and may further specify that the first arm allows the CMP conditioning disk to rotate and translate relative to the CMP polishing pad.

[0135] Example 6 may include the subject matter of any of Examples 1-5, and may further specify that the PSR change metric is a PSR ratio (PSRR) between an unconditioned PSR and a PSR after conditioning for a predetermined period of time.

[0136] Example 7 may include the subject matter of Example 6, and may further specify that the predetermined period of time is a time required to achieve removal of material of the CMP polishing pad to a predetermined depth.

[0137] Example 8 may include the subject matter of Example 6, and may further specify that the PSR is a roughness average.

[0138] Example 9 may include the subject matter of Example 6, and may further specify that the PSR is a root mean square roughness.

[0139] Example 10 may include the subject matter of any of Examples 1-5, and may further specify that the PSR change metric is representative of a slope of a linear fit of PSR versus normalized conditioning time.

[0140] Example 11 may include the subject matter of Example 10, and may further specify that the normalized conditioning time is normalized by a time required to achieve removal of material of the CMP polishing pad to a predetermined depth.

[0141] Example 12 is a method of conditioning a chemical mechanical polishing (CMP) polishing pad, including: receiving, by control circuitry of a CMP system, an initial pad surface roughness (PSR) of the CMP polishing pad; receiving, by the control circuitry of the CMP system, a target PSR of the CMP polishing pad; determining, by the control circuitry of the CMP system, using a PSR change metric for a CMP conditioning disk in the CMP system, a conditioning time to achieve the target PSR; and causing, by the control circuitry of the CMP system, the CMP system to condition the CMP polishing pad with the CMP conditioning disk for the conditioning time.

[0142] Example 13 may include the subject matter of Example 12, and may further specify that the PSR change metric is a PSR ratio (PSRR) between an unconditioned PSR and a PSR after conditioning for a predetermined period of time.

[0143] Example 14 may include the subject matter of Example 13, and may further specify that the predetermined period of time is a time required to achieve removal of material of the CMP polishing pad to a predetermined depth.

[0144] Example 15 may include the subject matter of any of Examples 12-14, and may further specify that the PSR is a roughness average.

[0145] Example 16 may include the subject matter of any of Examples 12-14, and may further specify that the PSR is a root mean square roughness.

[0146] Example 17 may include the subject matter of any of Examples 12-14, and may further specify that the PSR change metric is representative of a slope of a linear fit of PSR versus normalized conditioning time.

[0147] Example 18 may include the subject matter of Example 17, and may further specify that the normalized conditioning time is normalized by a time required to achieve removal of material of the CMP polishing pad to a predetermined depth.

[0148] Example 19 may include the subject matter of any of Examples 12-18, and may further specify that the PSR change metric is associated with a CMP operating condition, cause the CMP system to condition the CMP polishing pad includes cause the CMP system to operate under the CMP operating condition, and the CMP operating condition includes a platen rotation rate, a disk arm rotation rate, or a downforce on the CMP conditioning disk.

[0149] Example 20 is one or more computer-readable media having instructions thereon that, in response to execution by one or more processing devices of a chemical mechanical polishing (CMP) system, cause the CMP system to: receive a target pad surface roughness (PSR) of a CMP polishing pad of the CMP system; generate, using a PSR change metric for a CMP conditioning disk in the CMP system, a conditioning time to achieve the target PSR; and generate a control instruction for the CMP system to condition the CMP polishing pad with the CMP conditioning disk for the conditioning time.

[0150] Example 21 may include the subject matter of Example 20, and may further specify that the PSR change metric is a PSR ratio (PSRR) between an unconditioned PSR and a PSR after conditioning for a predetermined period of time.

[0151] Example 22 may include the subject matter of Example 21, and may further specify that the predetermined period of time is a time required to achieve removal of material of the CMP polishing pad to a predetermined depth.

[0152] Example 23 may include the subject matter of any of Examples 21-22, and may further specify that the PSR is a roughness average.

[0153] Example 24 may include the subject matter of any of Examples 21-22, and may further specify that the PSR is a root mean square roughness.

[0154] Example 25 may include the subject matter of any of Examples 21-24, and may further specify that the PSR change metric is representative of a slope of a linear fit of PSR versus normalized conditioning time.

[0155] Example 26 may include the subject matter of Example 25, and may further specify that the normalized conditioning time is normalized by a time required to achieve removal of material of the CMP polishing pad to a predetermined depth.

[0156] Example 27 may include the subject matter of any of Examples 21-26, and may further specify that the PSR change metric is associated with a CMP operating condition, the control instruction is to cause the CMP system to operate under the CMP operating condition, and the CMP operating condition includes a platen rotation rate, a disk arm rotation rate, or a downforce on the CMP conditioning disk.

[0157] Example 28 may include the subject matter of any of Examples 21-27, and may further specify that receive the target PSR of the CMP polishing pad includes: access a target wafer removal rate (WRR) for a wafer of the CMP system; and generate, using a stored relationship between PSR and WRR for the CMP polishing pad, the target PSR.

[0158] Example 29 may include the subject matter of Example 28, and may further specify that the stored relationship between PSR and WRR for the CMP polishing pad includes a second order polynomial relationship between PSR and WRR.

[0159] Example 30 is a method of characterizing a chemical mechanical polishing (CMP) conditioning disk, including: determining an unconditioned pad surface roughness (PSR) on an unconditioned CMP polishing pad surface; conditioning a first CMP polishing pad surface with the CMP conditioning disk for a first conditioning time; after conditioning the first CMP polishing pad surface, determining a first PSR of the first CMP polishing pad surface; conditioning a second CMP polishing pad surface with the CMP conditioning disk for a second conditioning time, wherein the second conditioning time is longer than the first conditioning time; after conditioning the second CMP polishing pad surface, determining a second PSR of the second CMP polishing pad surface; and generating a PSR change metric for the CMP conditioning disk based on the unconditioned PSR, the first PSR, and the second PSR.

[0160] Example 31 may include the subject matter of Example 30, and may further specify that the unconditioned CMP polishing pad surface, the first CMP polishing pad surface, and the second CMP polishing pad surface are all surfaces of a single CMP polishing pad.

[0161] Example 32 may include the subject matter of any of Examples 30-31, and may further specify that the PSR change metric includes a first PSR ratio (PSRR) between the unconditioned PSR and the first PSR, and a second PSRR between the unconditioned PSR and the second PSR.

[0162] Example 33 may include the subject matter of any of Examples 30-32, and may further specify that the first conditioning time is a time required to achieve removal of material of the CMP polishing pad to a predetermined depth.

[0163] Example 34 may include the subject matter of any of Examples 30-33, and may further specify that the unconditioned, first, and second PSRs are roughness averages.

[0164] Example 35 may include the subject matter of any of Examples 30-33, and may further specify that the unconditioned, first, and second PSRs are root mean square roughnesses.

[0165] Example 36 may include the subject matter of any of Examples 30-35, and may further specify that the PSR change metric is representative of a slope of a linear fit of PSR versus conditioning time.

[0166] Example 37 may include the subject matter of any of Examples 30-36, and may further specify that the CMP conditioning disk is a first CMP conditioning disk, and wherein the method further includes: determining a second unconditioned pad surface roughness (PSR) on a second unconditioned CMP polishing pad surface; conditioning a third CMP polishing pad surface with a second CMP conditioning disk, different from the first CMP conditioning disk, for a third conditioning time; after conditioning the third CMP polishing pad surface, determining a third PSR of the third CMP polishing pad surface; conditioning a fourth CMP polishing pad surface with the second CMP conditioning disk for a fourth conditioning time, wherein the fourth conditioning time is longer than the third conditioning time; after conditioning the fourth CMP polishing pad surface, determining a fourth PSR of the fourth CMP polishing pad surface; and generating a PSR change metric for the second CMP conditioning disk based on the second unconditioned PSR, the third PSR, and the fourth PSR; wherein the first conditioning time is a time required to achieve removal of the first CMP polishing pad to a predetermined depth, the third conditioning time is a time required to achieve removal of the second CMP polishing pad to the predetermined depth, the second conditioning time is a multiple of the first conditioning time, and the fourth conditioning time is the multiple of the third conditioning time.

[0167] Example 38 may include the subject matter of Example 37, and may further specify that conditioning the first CMP polishing pad surface, conditioning the second CMP polishing pad surface, conditioning the third CMP polishing pad surface, and conditioning the fourth CMP polishing pad surface are performed with a same platen rotation rate, disk arm rotation rate, and downforce of the CMP conditioning disk.

[0168] Example 39 is an apparatus including means for performing any of the methods disclosed herein, including any of the foregoing Example methods.

[0169] Example 40 is one or more computer readable media (e.g., non-transitory computer readable media) having instructions thereon that, in response to execution by one or more processing devices of a system, cause the system to perform any of the methods disclosed herein, including any of the foregoing Example methods.

Claims:

1. A chemical mechanical polishing (CMP) system, comprising:
control circuitry to:
 - access a stored pad surface roughness (PSR) change metric for a CMP polishing pad and a CMP conditioning disk,
 - generate, based on the PSR change metric, a conditioning time for conditioning the CMP polishing pad with the CMP conditioning disk to achieve a target PSR for the CMP polishing pad, and
 - cause the CMP conditioning disk to condition the CMP polishing pad for the conditioning time.
2. The CMP system of claim 1, wherein the control circuitry is further to:
receive an indicator of an initial PSR of the CMP polishing pad, and an indicator of the target PSR for the CMP polishing pad; and
wherein generation of the conditioning time is based on the PSR change metric, the initial PSR, and the target PSR.
3. The CMP system of claim 1, wherein cause the CMP conditioning disk to condition the CMP polishing pad for the conditioning time includes generate, based on the conditioning time, a control instruction for a first arm or a second arm of the CMP system, wherein the CMP conditioning disk is coupled to the first arm, and the CMP polishing pad is coupled to the second arm.
4. The CMP system of claim 3, wherein the second arm comprises a platen.
5. The CMP system of claim 3, wherein the first arm allows the CMP conditioning disk to rotate and translate relative to the CMP polishing pad.
6. The CMP system of any of claims 1-5, wherein the PSR change metric is a PSR ratio (PSRR) between an unconditioned PSR and a PSR after conditioning for a predetermined period of time.
7. The CMP system of claim 6, wherein the predetermined period of time is a time required to achieve removal of material of the CMP polishing pad to a predetermined depth.
8. The CMP system of claim 6, wherein the PSR is a roughness average.
9. The CMP system of claim 6, wherein the PSR is a root mean square roughness.
10. The CMP system of any of claims 1-5, wherein the PSR change metric is representative of a slope of a linear fit of PSR versus normalized conditioning time.
11. The CMP system of claim 10, wherein the normalized conditioning time is normalized by a time required to achieve removal of material of the CMP polishing pad to a predetermined depth.

12. One or more computer-readable media having instructions thereon that, in response to execution by one or more processing devices of a chemical mechanical polishing (CMP) system, cause the CMP system to:

receive a target pad surface roughness (PSR) of a CMP polishing pad of the CMP system;

generate, using a PSR change metric for a CMP conditioning disk in the CMP system, a conditioning time to achieve the target PSR; and

generate a control instruction for the CMP system to condition the CMP polishing pad with the CMP conditioning disk for the conditioning time.

13. The one or more computer-readable media of claim 12, wherein the PSR change metric is a PSR ratio (PSRR) between an unconditioned PSR and a PSR after conditioning for a predetermined period of time.

14. The one or more computer-readable media of claim 13, wherein the predetermined period of time is a time required to achieve removal of material of the CMP polishing pad to a predetermined depth.

15. The one or more computer-readable media of claim 12, wherein the PSR is a roughness average.

16. The one or more computer-readable media of claim 12, wherein the PSR is a root mean square roughness.

17. The one or more computer-readable media of claim 12, wherein the PSR change metric is representative of a slope of a linear fit of PSR versus normalized conditioning time.

18. The one or more computer-readable media of claim 17, wherein the normalized conditioning time is normalized by a time required to achieve removal of material of the CMP polishing pad to a predetermined depth.

19. The one or more computer-readable media of any of claims 12-18, wherein the PSR change metric is associated with a CMP operating condition, the control instruction is to cause the CMP system to operate under the CMP operating condition, and the CMP operating condition includes a platen rotation rate, a disk arm rotation rate, or a downforce on the CMP conditioning disk.

20. The one or more computer-readable media of any of claims 12-18, wherein receive the target PSR of the CMP polishing pad includes:

access a target wafer removal rate (WRR) for a wafer of the CMP system; and

generate, using a stored relationship between PSR and WRR for the CMP polishing pad, the target PSR.

21. The one or more computer-readable media of claim 20, wherein the stored relationship between PSR and WRR for the CMP polishing pad includes a second order polynomial relationship between PSR and WRR.

22. A method of characterizing a chemical mechanical polishing (CMP) conditioning disk, comprising:

determining an unconditioned pad surface roughness (PSR) on an unconditioned CMP polishing pad surface;

conditioning a first CMP polishing pad surface with the CMP conditioning disk for a first conditioning time;

after conditioning the first CMP polishing pad surface, determining a first PSR of the first CMP polishing pad surface;

conditioning a second CMP polishing pad surface with the CMP conditioning disk for a second conditioning time, wherein the second conditioning time is longer than the first conditioning time;

after conditioning the second CMP polishing pad surface, determining a second PSR of the second CMP polishing pad surface; and

generating a PSR change metric for the CMP conditioning disk based on the unconditioned PSR, the first PSR, and the second PSR.

23. The method of claim 22, wherein the unconditioned CMP polishing pad surface, the first CMP polishing pad surface, and the second CMP polishing pad surface are all surfaces of a single CMP polishing pad.

24. The method of any of claims 22-23, wherein the CMP conditioning disk is a first CMP conditioning disk, and wherein the method further comprises:

determining a second unconditioned pad surface roughness (PSR) on a second unconditioned CMP polishing pad surface;

conditioning a third CMP polishing pad surface with a second CMP conditioning disk, different from the first CMP conditioning disk, for a third conditioning time;

after conditioning the third CMP polishing pad surface, determining a third PSR of the third CMP polishing pad surface;

conditioning a fourth CMP polishing pad surface with the second CMP conditioning disk for a fourth conditioning time, wherein the fourth conditioning time is longer than the third conditioning time;

after conditioning the fourth CMP polishing pad surface, determining a fourth PSR of the fourth CMP polishing pad surface; and

generating a PSR change metric for the second CMP conditioning disk based on the second unconditioned PSR, the third PSR, and the fourth PSR;
wherein the first conditioning time is a time required to achieve removal of the first CMP polishing pad to a predetermined depth, the third conditioning time is a time required to achieve removal of the second CMP polishing pad to the predetermined depth, the second conditioning time is a multiple of the first conditioning time, and the fourth conditioning time is the multiple of the third conditioning time.

25. The method of claim 24, wherein conditioning the first CMP polishing pad surface, conditioning the second CMP polishing pad surface, conditioning the third CMP polishing pad surface, and conditioning the fourth CMP polishing pad surface are performed with a same platen rotation rate, disk arm rotation rate, and downforce of the CMP conditioning disk.

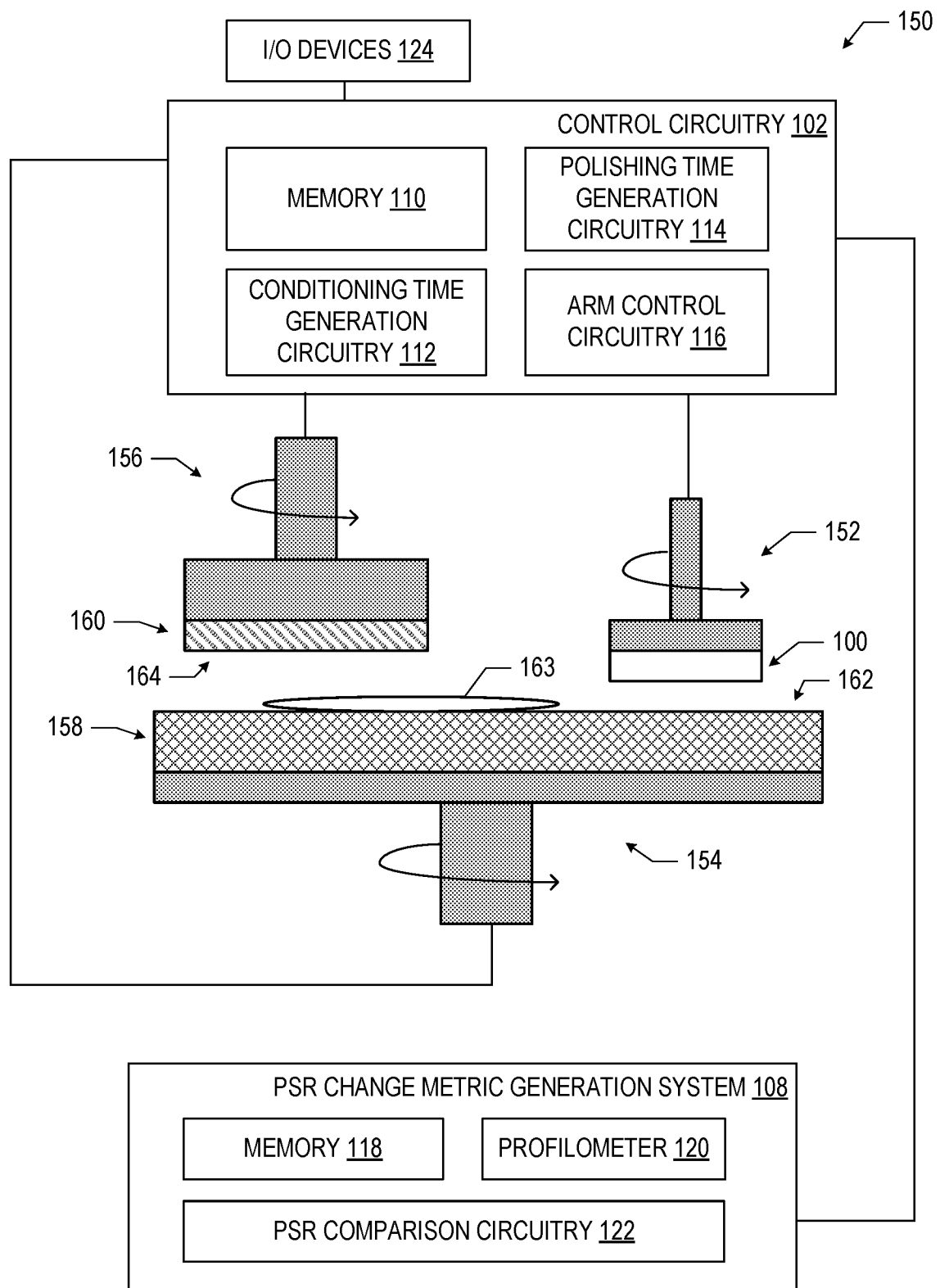


FIG. 1

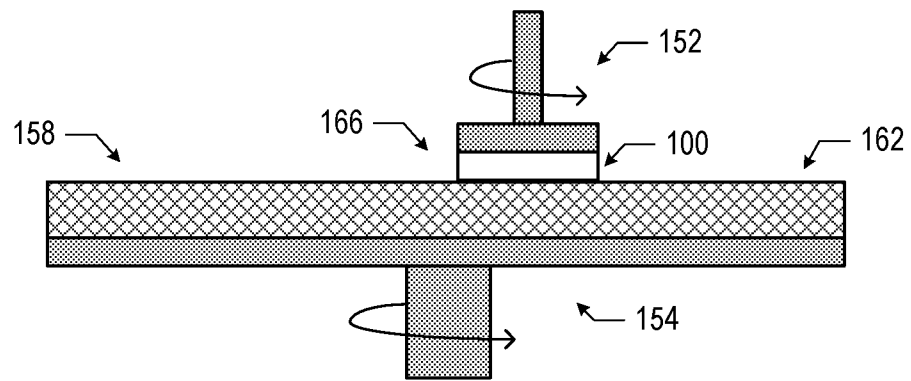


FIG. 2

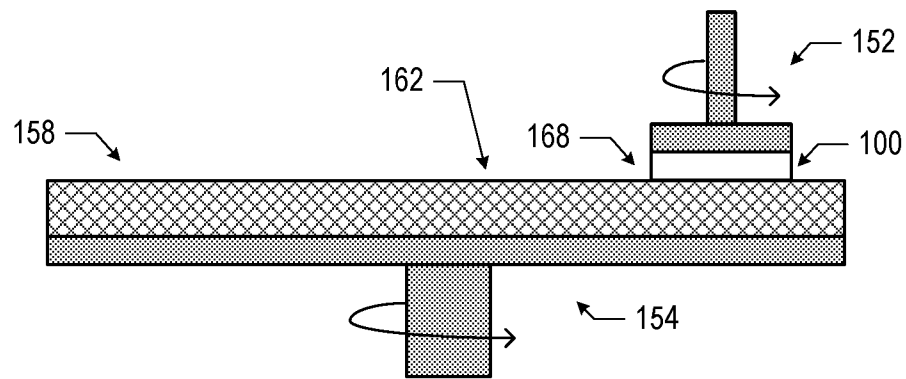


FIG. 3

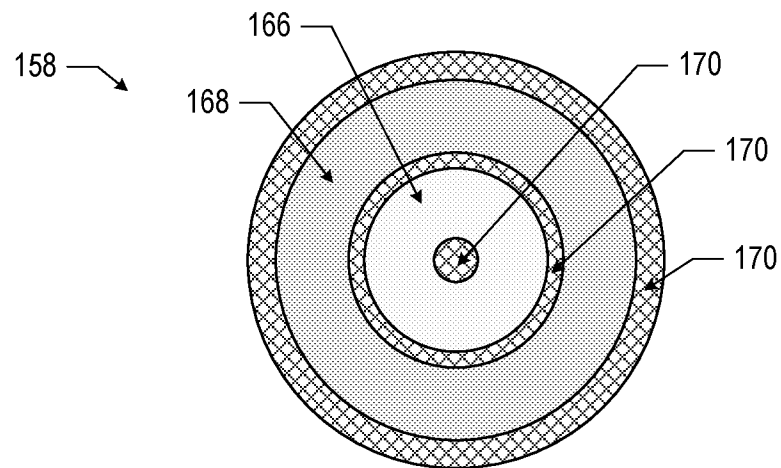


FIG. 4

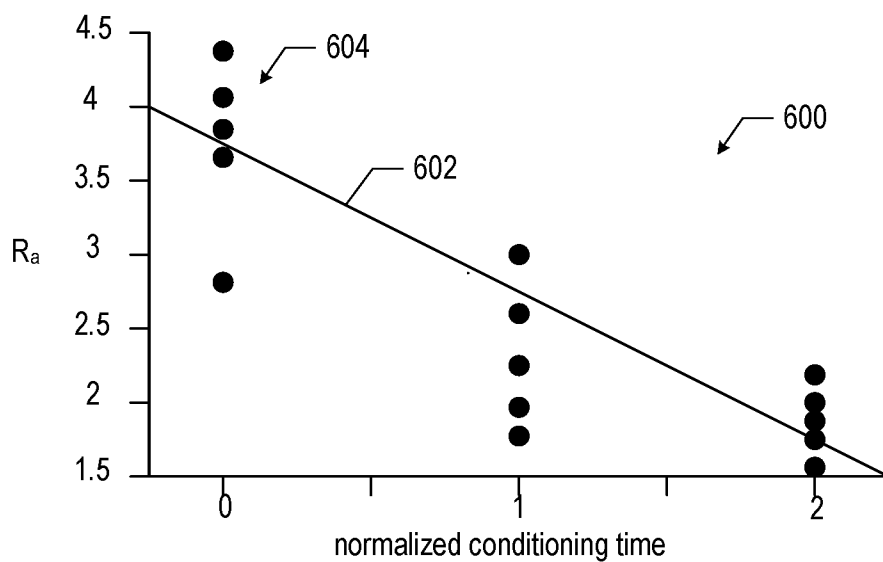
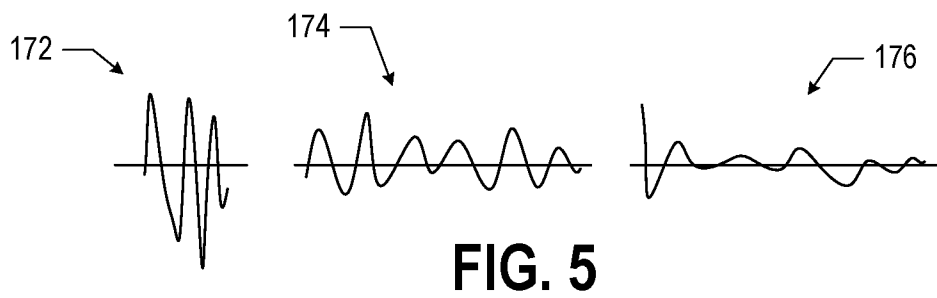


FIG. 6

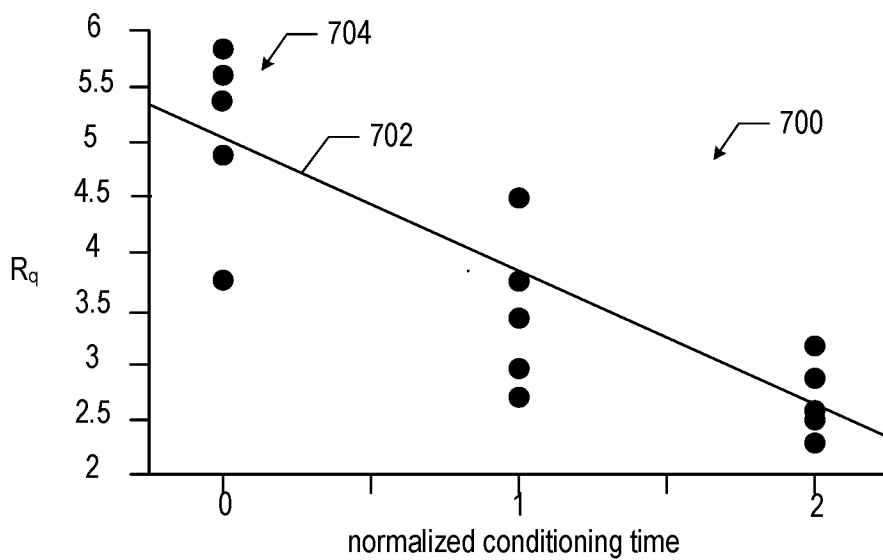
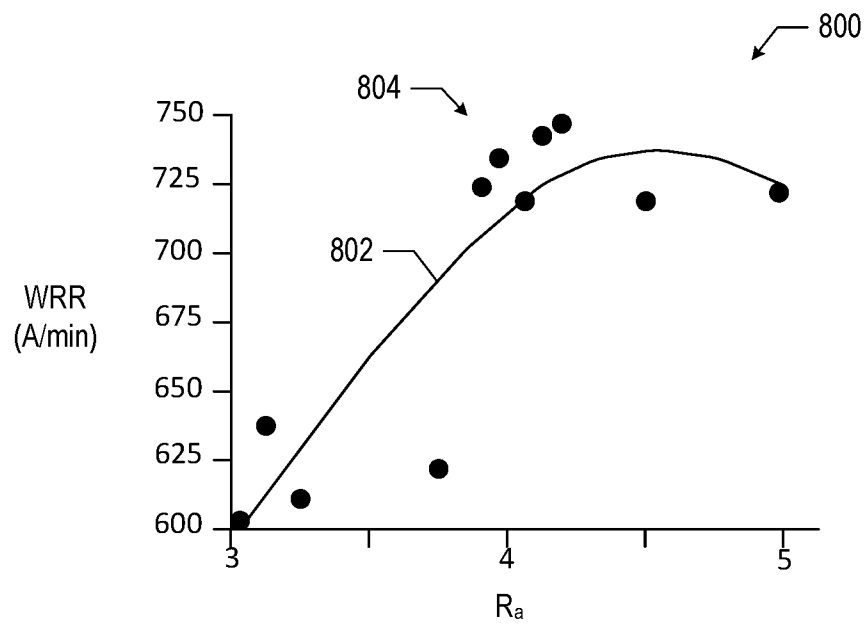
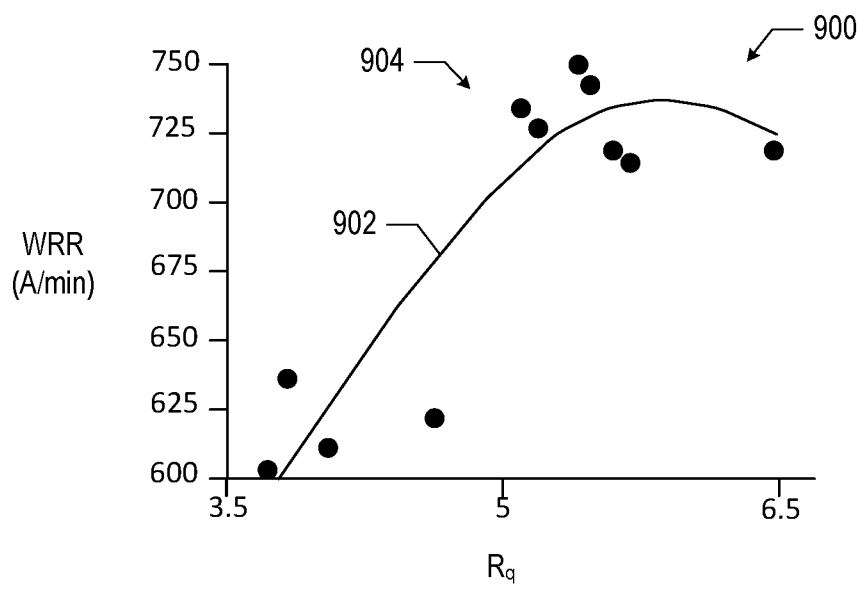


FIG. 7

**FIG. 8****FIG. 9**

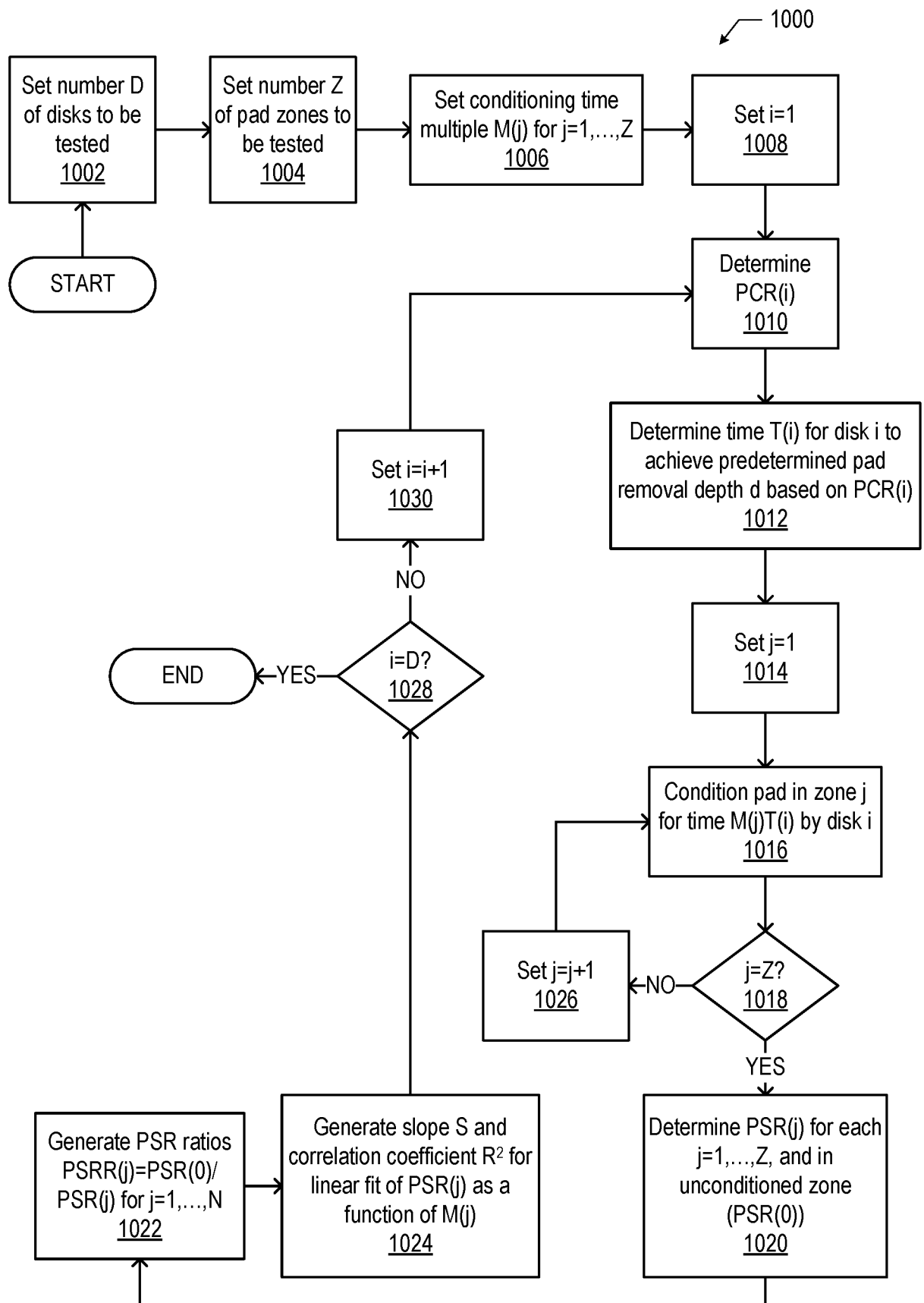


FIG. 10

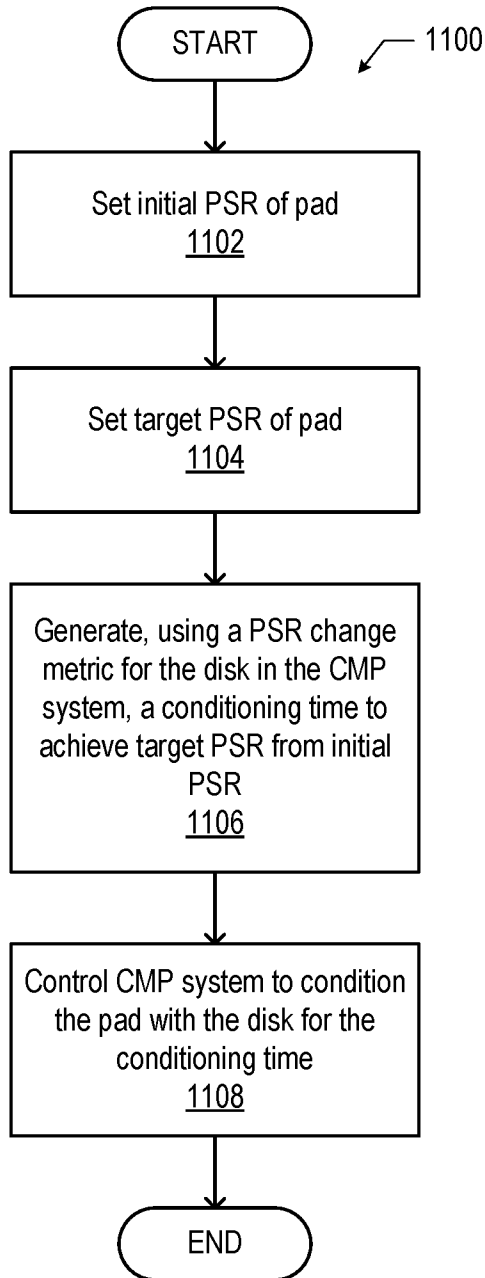


FIG. 11

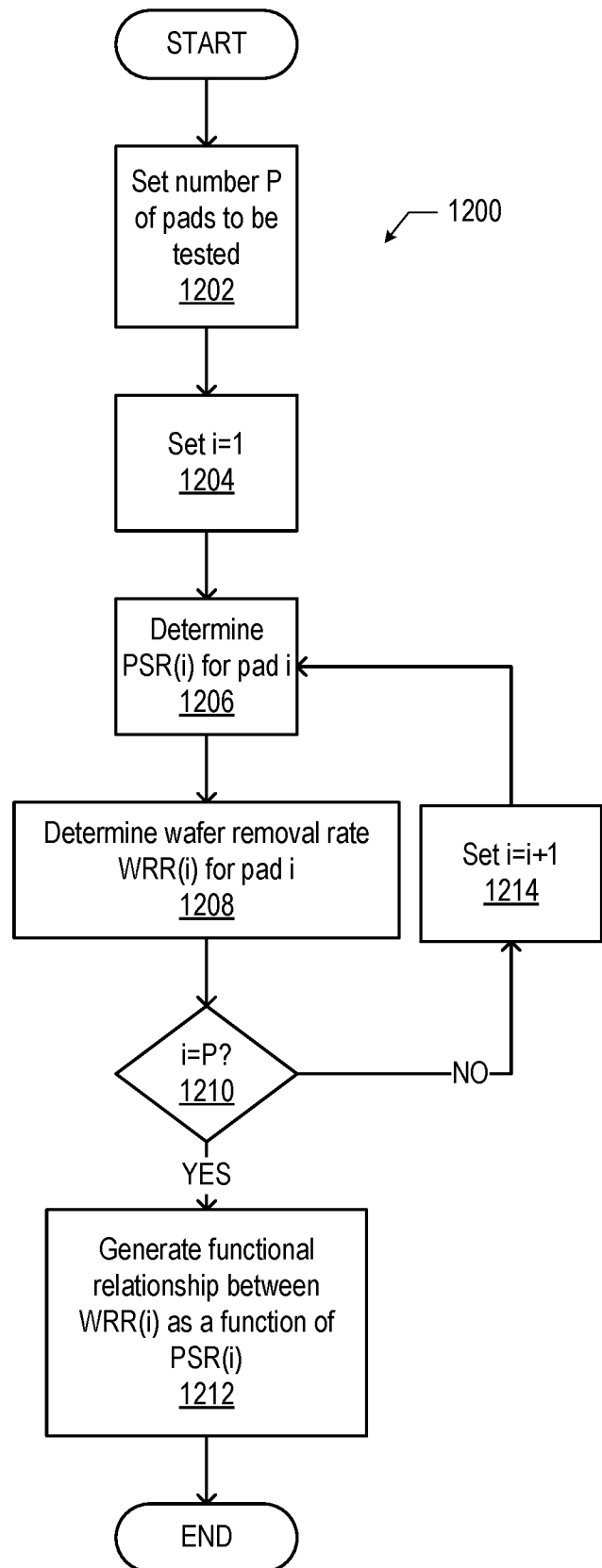
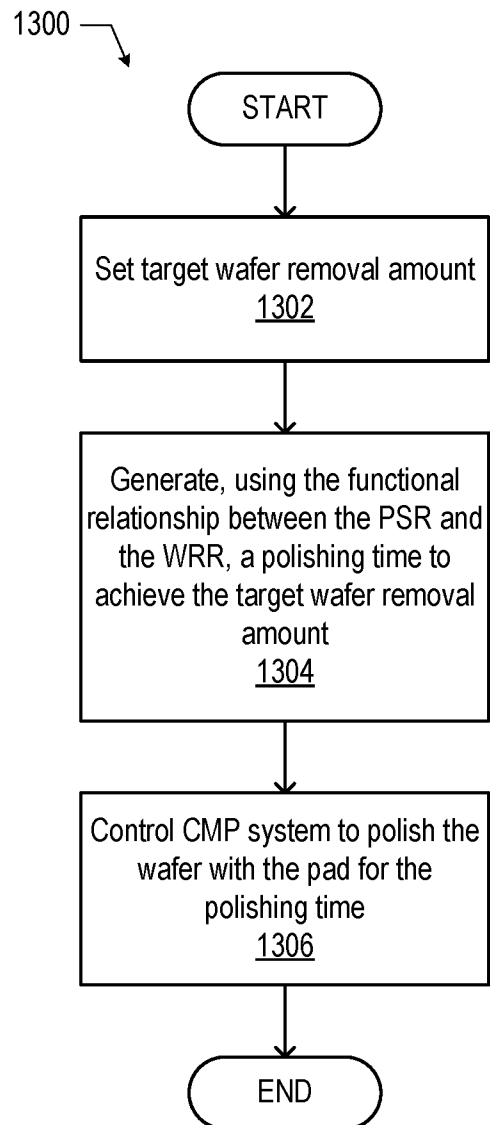


FIG. 12

**FIG. 13**

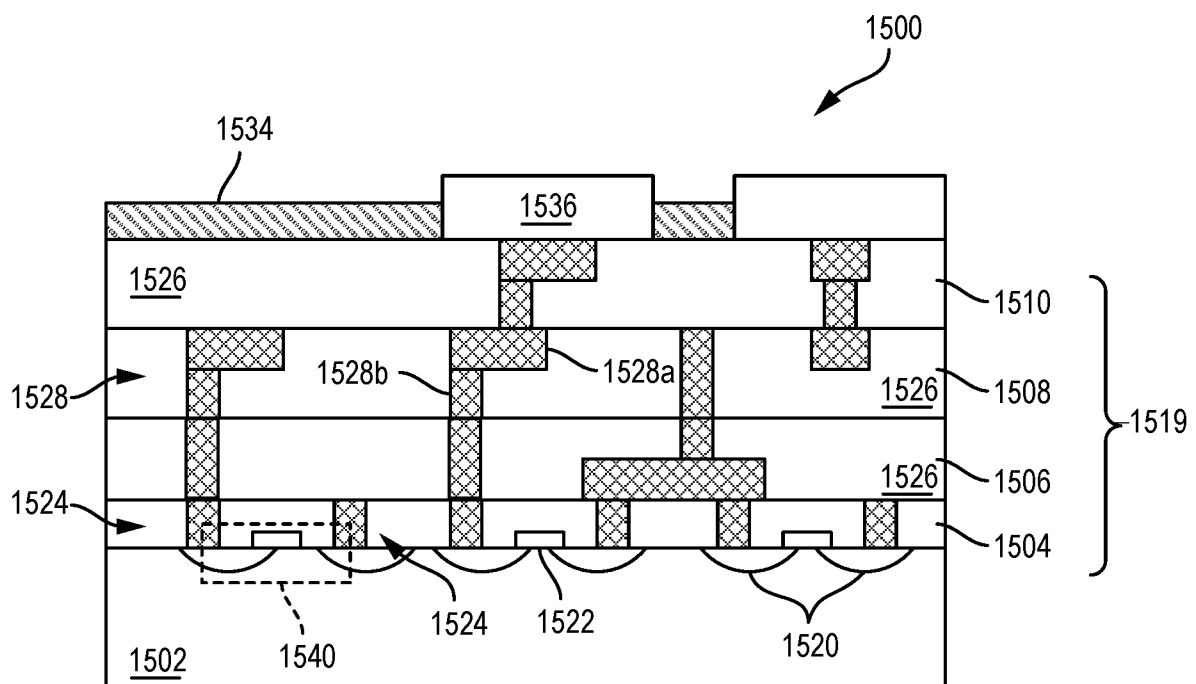
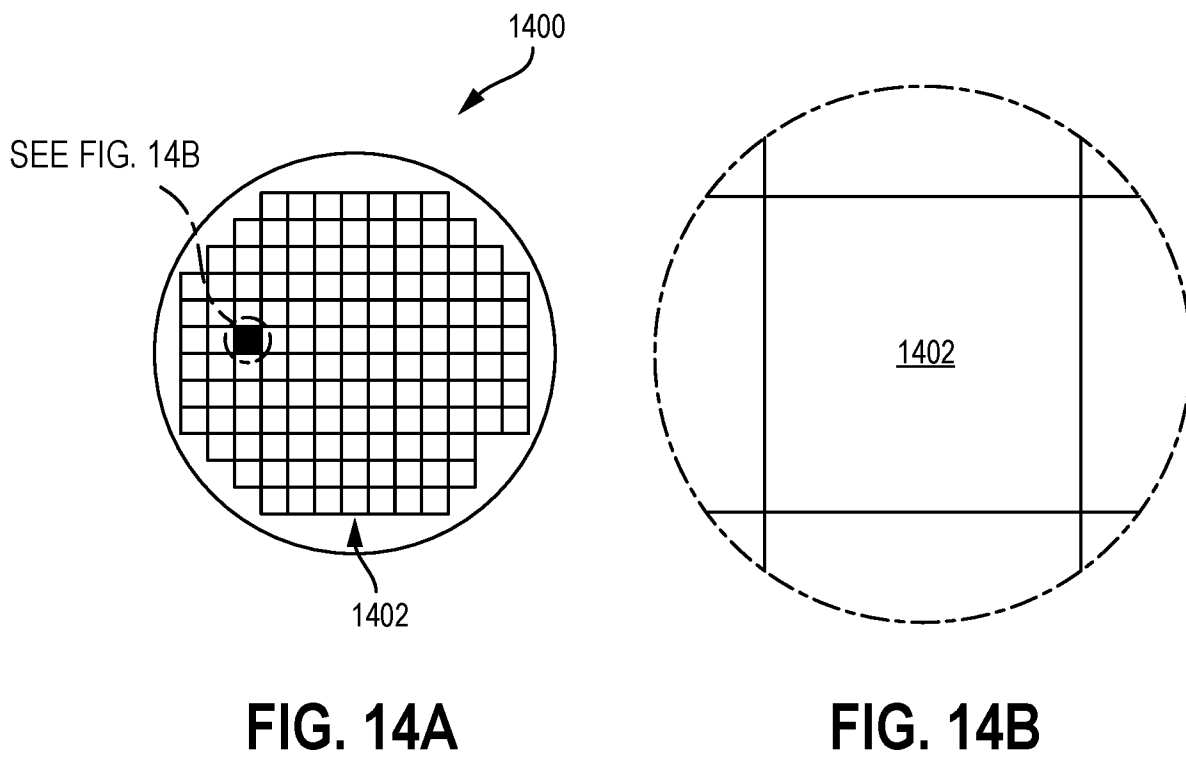


FIG. 15

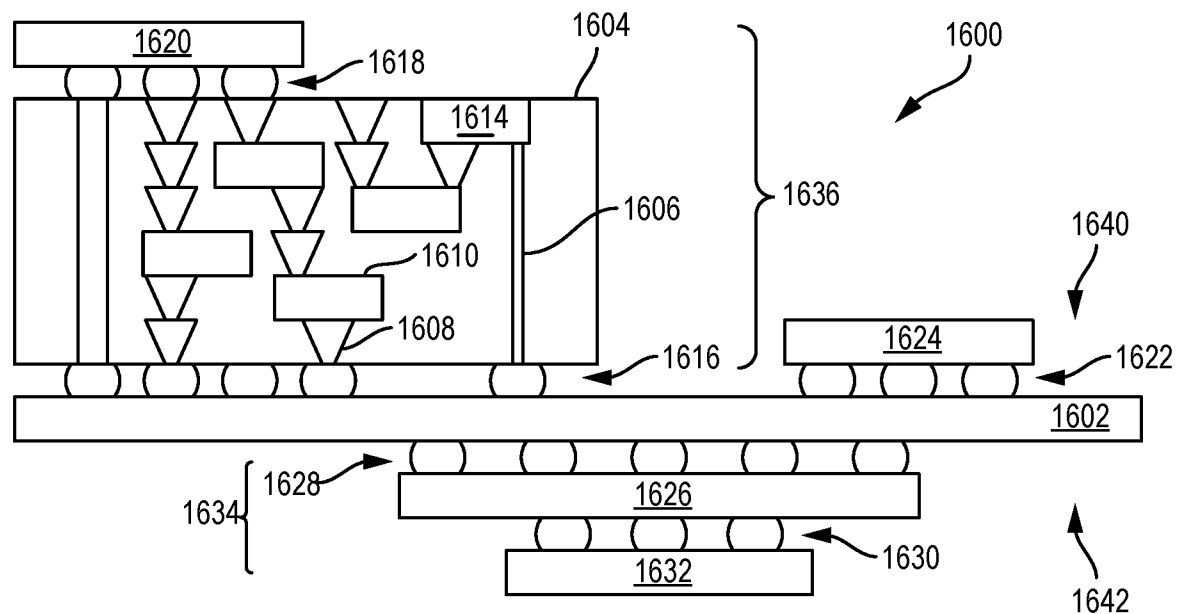


FIG. 16

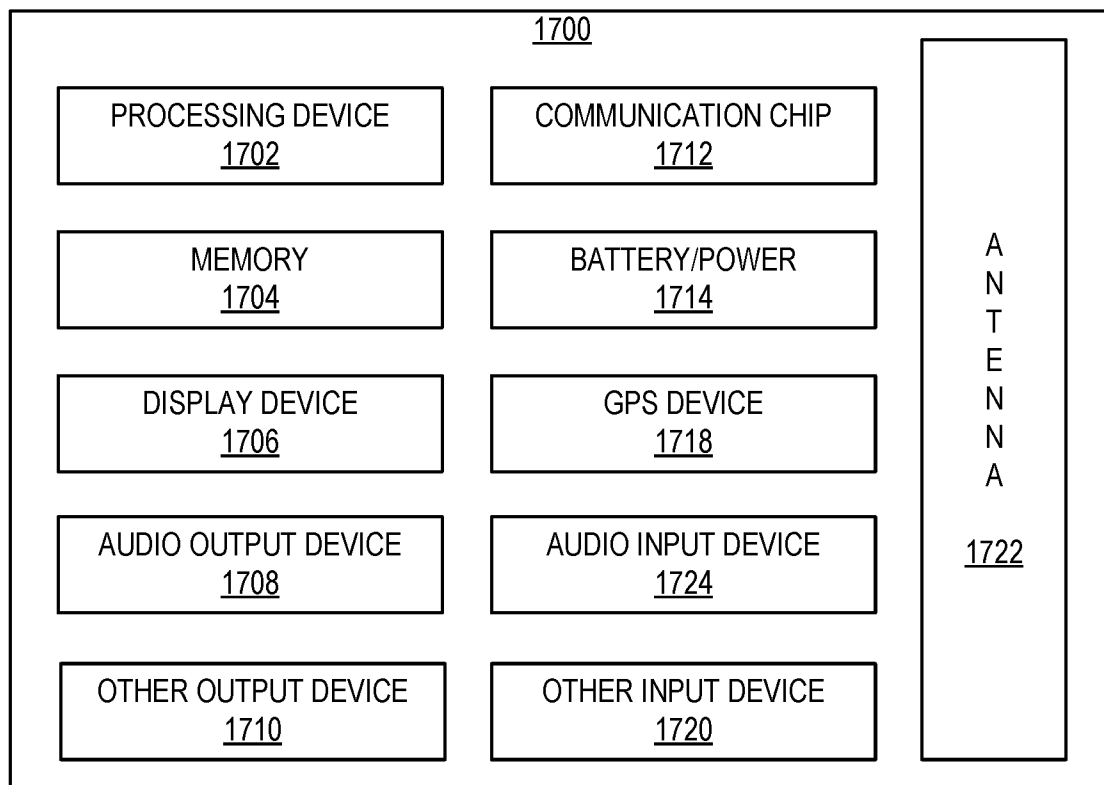


FIG. 17

A. CLASSIFICATION OF SUBJECT MATTER**H01L 21/304(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 21/304; G05B 13/04; B24B 53/00; B24B 37/00; B24B 49/00

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: CMP, pad, surface roughness, metric profile, conditioning time

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2012-0053721 A1 (ARULKUMAR P. SHANMUGASUNDRAM et al.) 01 March 2012 See paragraphs [0051]-[0091], claims 1, 15 and figures 1-7.	1-25
A	US 6045434 A (THOMAS R. FISHER, JR. et al.) 04 April 2000 See column 6, line 52 - column 9, line 2, claims 1-6 and figures 1, 2.	1-25
A	US 2004-0259477 A1 (THOMAS W. ANDERSON) 23 December 2004 See paragraphs [0014]-[0028], claims 1-5, 16-22 and figures 1-3.	1-25
A	JP 2005-088128 A (SANYO ELECTRIC CO., LTD. et al.) 07 April 2005 See paragraphs [0020]-[0046], claims 1, 5 and figures 1-6.	1-25
A	JP 2007-067110 A (TOKYO SEIMITSU CO., LTD.) 15 March 2007 See paragraphs [0032]-[0054], claims 1, 2 and figures 1, 2.	1-25



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

24 November 2016 (24.11.2016)

Date of mailing of the international search report

24 November 2016 (24.11.2016)

Name and mailing address of the ISA/KR

International Application Division

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2016/019985

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