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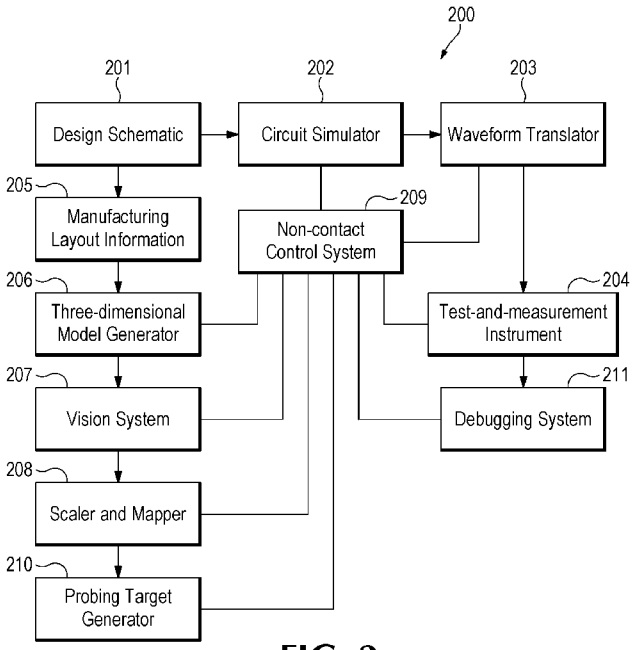


FIG. 2

(57) Abstract: A system for verifying signals in electronic circuits that includes a waveform translator and a test-and-measurement instrument. The waveform translator is configured to receive a simulated waveform for a node of a simulated prototype circuit and to translate the simulated waveform into a translated waveform. The test-and-measurement instrument is configured to obtain a measured waveform and to determine a deviation of the measured waveform from the simulated waveform using the translated waveform.

[Continued on next page]

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ELECTRONIC SIGNAL VERIFICATION USING A TRANSLATED SIMULATED WAVEFORM

CROSS-REFERENCES TO RELATED APPLICATIONS

[0001] This patent application claims the benefit of provisional Application No. 63/050,053 filed July 9, 2020. That application is incorporated into the present disclosure by this reference.

TECHNICAL FIELD

[0002] The subject matter is related to a system and methods for validating an electronic circuit by using a simulated waveform in a test-and-measurement instrument.

BACKGROUND

[0003] The current process for validation of an electronic circuit requires that a designer design the circuit, simulate it, and then build the circuit. Once the circuit is built, the designer probes the circuit with an oscilloscope or other test-and-measurement instrument and then visually compares the signal at the probed point with what is expected (either by design knowledge or rerunning the simulation while monitoring the node being checked).

[0004] Configurations of the disclosed technology address shortcomings in the prior art.

BRIEF DESCRIPTION OF THE DRAWINGS

[0005] FIG. 1 shows representations of physical prototype circuit, a simulated prototype circuit, and fabricated circuit.

[0006] FIG. 2 is a functional block diagram showing an example arrangement of components of a system configured to perform the signal verification method illustrated in FIG. 1.

[0007] FIG. 3 illustrates a signal verification method using a translated simulated waveform, according to an example configuration.

DETAILED DESCRIPTION

[0008] As described in this disclosure, aspects are directed to a signal verification method for electronic circuits. Configurations of the disclosed technology support the ability to integrate circuit simulation with validation of a designed circuit. Specifically, configurations of the disclosed technology use the circuit simulator's ability to export the expected simulated waveform and also incorporate the expected simulated waveform as a reference waveform on a test-and-measurement instrument, such as an oscilloscope. This allows for automated comparison by using the existing mathematical and mask functions of the test-and-measurement instrument. Configurations of the disclosed technology automate the process of translating the simulated waveform into a format that can be used for validation, performance, and tolerance testing on the test-and-measurement instrument.

[0009] As used in this disclosure, the term "physical circuit" means a tangible electronic circuit, while the term "simulated circuit" means an intangible electronic circuit that exists only as mathematical modeling in computer software. As used in this disclosure, the term "physical prototype circuit" means a physical circuit that is intended to be the design standard for a designed electronic circuit. The designed electronic circuit may be, for example, an integrated circuit designed to perform a certain function or functions. The term "fabricated circuit" means a physical circuit that was built to the design standard of the physical prototype circuit. The layout of the fabricated circuit functionally matches the layout of the physical prototype circuit. The term "simulated prototype circuit" means an intangible electronic circuit whose layout, which exists only as mathematical modeling in computer software, models the function of the physical prototype circuit or portions of the physical prototype circuit.

[0010] In the processes discussed here, the simulated prototype circuit, which is generated from the physical prototype circuit, is used to validate the fabricated circuit. In this context, "validate" means that the fabricated circuit is tested to confirm that the fabricated circuit conforms to the design standard of the physical prototype circuit. Accordingly, the information used in the design process of the electronic circuit is also applied it to the validation process. The result is a simpler and more expedient way to validate the fabricated circuit.

[0011] Accordingly, FIG. 1 shows representations of a physical prototype circuit, a simulated prototype circuit, and a fabricated circuit. FIG. 2 is a functional block diagram showing an example arrangement configuration of components of a system configured to perform a signal verification method, according to embodiments. FIG. 3 illustrates an example signal verification method **300** using a translated simulated waveform, according to embodiments.

[0012] With reference to FIGs. 1–3, at the processes labeled **301** and **302**, a design schematic **201** for a physical prototype circuit **101** is captured and modeled in a circuit simulator **202**, such as a circuit simulation software, to produce a simulated prototype circuit **103** (illustrated in FIG. 1 as appearing on an example display screen). The circuit simulator **202** may be, for example, a computer-aided-design (CAD) -based tool.

[0013] At the process labeled **303** in the configuration illustrated in FIG. 1, the circuit simulator **202** generates a simulated waveform for a particular node **105** in the simulated prototype circuit **103**. In configurations, the example node **105** in the simulated prototype circuit **103** corresponds to an example node **104** of interest in the physical prototype circuit **101**. A simulated waveform is a mathematical representation of what the waveform of the corresponding node **104** of the physical prototype circuit **101** is calculated to be based on the simulated prototype circuit **103**. The simulated waveform from the circuit simulator **202** may be exported from the circuit simulator **202** to a waveform translator **203**.

[0014] At the process labeled **304**, the waveform translator **203** translates the simulated waveform into a translated waveform of a type that can be used by the test-and-measurement instrument **204**. One such type, for example, is as a reference waveform. In configurations, the translation may include, for example, adding information to or removing information from the simulated waveform so that the resulting translated waveform is compatible with the test-and-measurement instrument **204**. In configurations, the translation may include resampling the simulated waveform so that the resulting translated waveform is compatible with the test-and-measurement instrument **204**.

[0015] In configurations, the translation process is automatic, meaning that the process starts and operates independently when the waveform translator **203** receives the simulated

waveforms from the circuit simulator **202**. For example, the translation process may be executed by a program or script.

[0016] In configurations, at the process labeled **305** an additional translated waveform may be generated by the waveform translator **203** by, for example, modifying the simulated waveform and then translating the modified simulated waveform. The additional translated waveform may be useful, for example, to provide a tolerance waveform for a test-and-measurement instrument **204** that does not have mathematical capabilities. Hence, for example, the tolerance waveform may be offset from the translated waveform by a predetermined amount that corresponds to a desired tolerance. The tolerance may be a fixed amount, a percentage difference from the simulated waveform, or another representation of a maximum desired variance. In configurations, two additional translated waveforms may be generated: the first additional translated waveform being offset from the translated waveform in a positive direction, and the second additional translated waveform being offset from the translated waveform in a negative direction. Together, the first additional translated waveform and the second additional translated waveform may define a tolerance band or tolerance area (sometimes known as a triggering mask) around the translated waveform. In configurations, this tolerance area may be used to determine if a measured waveform (discussed below for the process labeled **311**) passes for being within the tolerance area or fails for being outside of the tolerance area.

[0017] In configurations, the translated waveform may be imported into the test-and-measurement instrument **204** as a reference waveform. This may also include importing the additional translated waveform(s) from process labeled **305**, if any, as additional reference waveform(s).

[0018] At the process labeled **306**, manufacturing layout information **205** is generated for a fabricated circuit **102** based on the physical prototype circuit **101**. The manufacturing layout information **205** corresponds to the design schematic **201** for the physical prototype circuit **101**. In this context, "corresponding to" means that, functionally, the fabricated circuit **102** (and, thus, the manufacturing layout information **205**) substantially matches the physical prototype

circuit **101**. As used in this disclosure, "substantially matches" means largely or essentially equivalent, without requiring perfect identicalness.

[0019] At the process labeled **307**, an electronic, three-dimensional model of the physical circuit is generated from the manufacturing layout information **205**. The three-dimensional model may be generated by a three-dimensional model generator **206**.

[0020] At the process labeled **308**, the fabricated circuit **102** is built based on the manufacturing layout information **205**.

[0021] At the process labeled **311**, the fabricated circuit **102** is probed (using a probe from the test-and-measurement instrument **204**) to measure a signal (i.e. obtain a measured waveform) from an example node **106** on the fabricated circuit **102** that corresponds to the example node **105** of the simulated prototype circuit **103** discussed above. In this context, "corresponds to" means that, with regard to its relative placement in the circuit, the example node **106** on the fabricated circuit **102** substantially matches the example node **105** of the simulated prototype circuit **103**.

[0022] In configurations, at the process labeled **309**, a vision system **207** obtains visual environment information (information about the visual environment) for the fabricated circuit **102**. The vision system **207** may be part of an augmented reality system or a machine vision system. Using the visual environment information from the vision system **207**, at the process labeled **310** a scaler and mapper **208** may scale and orient the three-dimensional model to correlate the circuit nodes of the simulated prototype circuit **103** with the visual environment of the fabricated circuit **102** to allow an accurate location of the desired probing points on the fabricated circuit **102**.

[0023] Once correlated, a probing target generator **210** may use the three-dimensional model to identify probing targets in an augmented reality system to assist a human operator to make a measurement on the correct node. The three-dimensional model could also be used to generate positioning information for an automated probing system that is part of a machine vision system to make an automated measurement of the desired circuit node. Hence, probing the circuit at the process labeled **311** may further include using the three-dimensional model,

noted above for the process labeled **307**, in conjunction with visual environment information obtained by the vision system **207**.

[0024] At the process labeled **312**, the measured signal from the process labeled **311** is compared to the translated waveform from the process labeled **304** to determine the deviation of the translated waveform (and, thus, the simulated waveform from the process labeled **303**) from the actual measured waveform (from the process labeled **311**). The deviation may be determined by, as examples, subtracting the measured waveform from the translated waveform or by using a desired tolerance to define a mask limit. The tolerance may be a fixed amount, a percentage difference from the translated waveform, or another representation of a maximum desired variance.

[0025] In configurations, the comparison at the process labeled **312** may be used to provide information to an automated debugging system **211** that utilizes the design schematic **201** for the physical prototype circuit **101** and the simulated waveform for the selected node **105** in the simulated prototype circuit **103** to characterize and validate the fabricated circuit **102**. In configurations, the automated debugging system **211** may systematically probe new locations of the fabricated circuit **102** based on the results of the previously measured nodes **106** to determine if the fabricated circuit **102** is working properly or, if it is not operating properly, to isolate failed portions of the fabricated circuit **102**. In configurations, the new locations may be determined by, for example, complex circuit-analysis algorithms. Such algorithms may utilize, for example, artificial intelligence or machine learning based on significant exposure to training patterns, which may identify the highest probability item as the next place in the circuit to check for proper operation.

[0026] At the process labeled **313**, the mathematical functionality of the test-and-measurement instrument **204** is used on the translated waveform to establish pass/fail criteria. For example, a desired tolerance may be included in or input into the mathematical functionality of the test-and-measurement instrument **204**. The tolerance may be a fixed amount, a percentage difference from the translated waveform, or another representation of a maximum desired variance, for example, a signal or triggering mask. This tolerance may be used, at the process labeled **314**, to determine if a measured waveform (discussed above for

the process labeled **311**) passes for being within the desired tolerance from the translated waveform or fails for being outside of the desired tolerance from the translated waveform. In configurations, the building (the process labeled **308**), the probing (the process labeled **311**), and the determining (the process labeled **312**) processes are iterative. In such configurations, at the process labeled **314**, the deviations determined in prior iterations may be used to determine a next node of the fabricated circuit for the probing process of the next iteration.

[0027] In configurations, the system may include a non-contact system control interface **209** to simplify user interactions with the system. The contactless control may be or include voice- or gesture-based operations, as examples.

EXAMPLES

[0028] Illustrative examples of the disclosed technologies are provided below. A particular configuration of the technologies may include one or more, and any combination of, the examples described below.

[0029] Example 1 includes a signal verification method for an electronic circuit, the method comprising: receiving, from a circuit simulator, a simulated waveform for a node of a simulated prototype circuit; translating, by a waveform translator, the simulated waveform into a translated waveform, the translated waveform having a format different from a format of the simulated waveform; obtaining, with a test-and-measurement instrument, a measured waveform from a node of the fabricated circuit that corresponds to a node of the simulated prototype circuit; and determining, by the test-and-measurement instrument, a deviation of the measured waveform from the simulated waveform using the translated waveform.

[0030] Example 2 the method of Example 1, further comprising: capturing, by the circuit simulator, a design schematic for a physical prototype circuit before modeling the design schematic; modeling, by the circuit simulator, the design schematic for the physical prototype circuit to produce the simulated prototype circuit; and generating, by the circuit simulator, the simulated waveform for the node of the simulated prototype circuit.

[0031] Example 3 includes the method of any of Examples 1–2, in which the translated waveform is a reference waveform for the test-and-measurement instrument.

[0032] Example 4 includes the method of any of Examples 1–3, further comprising generating, by the waveform translator, an additional translated waveform from the simulated waveform.

[0033] Example 5 includes the method of Example 4, in which generating the additional translated waveform from the simulated waveform comprises replicating the simulated waveform to create a replicated waveform and then modifying the replicated waveform by a predetermined amount corresponding to a desired tolerance.

[0034] Example 6 includes the method of any of Examples 1–5, further comprising: determining, by the test-and-measurement instrument, a pass-fail criterion based on a maximum desired variance from the simulated waveform; identifying the measured waveform as passing when the determined deviation of the measured waveform is within the pass-fail criterion; and identifying the measured waveform as failing when the determined deviation of the measured waveform is outside of the pass-fail criterion.

[0035] Example 7 includes the method of any of Examples 1–6, further comprising: generating manufacturing layout information for the fabricated circuit, the manufacturing layout information corresponding to the design schematic for the physical prototype circuit; and building the fabricated circuit based on the manufacturing layout information.

[0036] Example 8 includes the method of any of Examples 1–7, further comprising generating an electronic, three-dimensional model of the physical circuit from the manufacturing layout information.

[0037] Example 9 includes the method of Example 8, further comprising correlating a location of the node of the simulated prototype circuit with a location of the node of the fabricated circuit by: obtaining, with a vision system, visual environment information for the fabricated circuit; and scaling and orienting the three-dimensional model by a scaler and mapper based on the visual environment information.

[0038] Example 10 includes the method of any of Examples 1–9, in which obtaining the measured waveform from the node of the fabricated circuit comprises probing the node of the fabricated circuit.

[0039] Example 11 includes the method of any of Examples 1–10, in which determining the deviation of the measured waveform from the simulated waveform using the translated waveform comprises at least one of subtracting the measured waveform from the translated waveform and using a desired tolerance to define a mask limit.

[0040] Example 12 includes the method of any of Examples 1–11, in which the receiving, the translating, the obtaining, and the determining processes are iterative, the method further comprising utilizing the deviations determined in prior iterations to determine a next node of the fabricated circuit for the obtaining process of the next iteration.

[0041] Example 13 includes a system for verifying signals in electronic circuits, the system comprising: a waveform translator configured to receive a simulated waveform for a node of a simulated prototype circuit and to translate the simulated waveform into a translated waveform, the translated waveform having a format different from a format of the simulated waveform; and a test-and-measurement instrument configured to obtain a measured waveform from a node on a fabricated circuit that corresponds to the node of the simulated prototype circuit, the test-and-measurement instrument further configured to determine a deviation of the measured waveform from the simulated waveform using the translated waveform.

[0042] Example 14 includes the system of Example 13, in which the waveform translator is further configured to replicate the simulated waveform to create a replicated waveform and to modify the replicated waveform by a predetermined amount corresponding to a desired tolerance.

[0043] Example 15 includes the system of any of Examples 13–14, in which the test-and-measurement instrument is further configured to determine a pass-fail criterion based on a maximum desired variance from the simulated waveform, the test-and-measurement instrument further being configured to identify the measured waveform as passing when the

determined deviation of the measured waveform is within the pass-fail criterion, and the test-and-measurement instrument further being configured to identify the measured waveform as failing when the determined deviation of the measured waveform is outside of the pass-fail criterion.

[0044] Example 16 includes the system of any of Examples 13–15, in which the fabricated circuit corresponds to a design schematic for a physical prototype circuit, the system further comprising a three-dimensional model generator configured to generate an electronic, three-dimensional model of the physical circuit from manufacturing layout information for the fabricated circuit, the manufacturing layout information corresponding to the design schematic for the physical prototype circuit.

[0045] Example 17 includes the system of Example 16, further comprising a vision system configured to obtain visual environment information for the fabricated circuit.

[0046] Example 18 includes the system of Example 17, further comprising a scaler and mapper configured to scale and orient the three-dimensional model based on the visual environment information.

[0047] Example 19 includes the system of any of Examples 13–18, further comprising a non-contact system control interface configured to allow contactless user interaction with at least one of the waveform translator and the test-and-measurement instrument.

[0048] Example 20 includes the system of any of Examples 10–19, further comprising a circuit simulator configured to receive a design schematic for a physical prototype circuit and to model the physical prototype circuit to produce the simulated prototype circuit, the circuit simulator further configured to generate the simulated waveform for the node of the simulated prototype circuit.

[0049] *****

[0050] Aspects may operate on a particularly created hardware, on firmware, digital signal processors, or on a specially programmed general-purpose computer including a processor operating according to programmed instructions. The terms “controller” or “processor” as used

herein are intended to include microprocessors, microcomputers, ASICs, and dedicated hardware controllers. One or more aspects may be embodied in computer-usable data and computer-executable instructions, such as in one or more program modules, executed by one or more computers (including monitoring modules), or other devices. Generally, program modules include routines, programs, objects, components, data structures, etc. that perform particular tasks or implement particular abstract data types when executed by a processor in a computer or other device. The computer executable instructions may be stored on a non-transitory computer readable medium such as a hard disk, optical disk, removable storage media, solid state memory, RAM, etc. As will be appreciated by one of skill in the art, the functionality of the program modules may be combined or distributed as desired in various configurations. In addition, the functionality may be embodied in whole or in part in firmware or hardware equivalents such as integrated circuits, field programmable gate arrays (FPGA), and the like. Particular data structures may be used to more effectively implement one or more aspects of the disclosed systems and methods, and such data structures are contemplated within the scope of computer executable instructions and computer-usable data described herein.

[0051] The previously described versions of the disclosed subject matter have many advantages that were either described or would be apparent to a person of ordinary skill. Even so, all of these advantages or features are not required in all versions of the disclosed apparatus, systems, or methods.

[0052] Additionally, this written description makes reference to particular features. It is to be understood that the disclosure in this specification includes all possible combinations of those particular features. For example, where a particular feature is disclosed in the context of a particular example configuration, that feature can also be used, to the extent possible, in the context of other example configurations.

[0053] Also, when reference is made in this application to a method having two or more defined steps or operations, the defined steps or operations can be carried out in any order or simultaneously, unless the context excludes those possibilities.

[0054] Furthermore, the term “comprises” and its grammatical equivalents are used in this application to mean that other components, features, steps, processes, operations, etc. are optionally present. For example, an article “comprising” or “which comprises” components A, B, and C can contain only components A, B, and C, or it can contain components A, B, and C along with one or more other components.

[0055] Although specific example configurations have been described for purposes of illustration, it will be understood that various modifications may be made without departing from the spirit and scope of the disclosure.

CLAIMS:

I (or we) claim:

1. A signal verification method for an electronic circuit, the method comprising:

receiving, from a circuit simulator, a simulated waveform for a node of a simulated prototype circuit;

translating, by a waveform translator, the simulated waveform into a translated waveform, the translated waveform having a format different from a format of the simulated waveform;

obtaining, with a test-and-measurement instrument, a measured waveform from a node of a fabricated circuit that corresponds to the node of the simulated prototype circuit; and

determining, by the test-and-measurement instrument, a deviation of the measured waveform from the simulated waveform using the translated waveform.

2. The method of claim 1, further comprising:

capturing, by the circuit simulator, a design schematic for a physical prototype circuit before modeling the design schematic;

modeling, by the circuit simulator, the design schematic for the physical prototype circuit to produce the simulated prototype circuit; and

generating, by the circuit simulator, the simulated waveform for the node of the simulated prototype circuit.

3. The method of claim 1, in which the translated waveform is a reference waveform for the test-and-measurement instrument.

4. The method of claim 1, further comprising generating, by the waveform translator, an additional translated waveform from the simulated waveform.

5. The method of claim 4, in which generating the additional translated waveform from the simulated waveform comprises replicating the simulated waveform to create a replicated

waveform and then modifying the replicated waveform by a predetermined amount corresponding to a desired tolerance.

6. The method of claim 1, further comprising:

determining, by the test-and-measurement instrument, a pass-fail criterion based on a maximum desired variance from the simulated waveform;

identifying the measured waveform as passing when the determined deviation of the measured waveform is within the pass-fail criterion; and

identifying the measured waveform as failing when the determined deviation of the measured waveform is outside of the pass-fail criterion.

7. The method of claim 1, further comprising:

generating manufacturing layout information for the fabricated circuit, the manufacturing layout information corresponding to the design schematic for the physical prototype circuit; and

building the fabricated circuit based on the manufacturing layout information.

8. The method of claim 7, further comprising generating an electronic, three-dimensional model of the physical circuit from the manufacturing layout information.

9. The method of claim 8, further comprising correlating a location of the node of the simulated prototype circuit with a location of the node of the fabricated circuit by:

obtaining, with a vision system, visual environment information for the fabricated circuit; and

scaling and orienting the three-dimensional model by a scaler and mapper based on the visual environment information.

10. The method of claim 1, in which obtaining the measured waveform from the node of the fabricated circuit comprises probing the node of the fabricated circuit.

11. The method of claim 1, in which determining the deviation of the measured waveform from the simulated waveform using the translated waveform comprises at least one of subtracting

the measured waveform from the translated waveform and using a desired tolerance to define a mask limit.

12. The method of claim 1, in which the receiving, the translating, the obtaining, and the determining processes are iterative, the method further comprising utilizing the deviations determined in prior iterations to determine a next node of the fabricated circuit for the obtaining process of the next iteration.

13. A system for verifying signals in electronic circuits, the system comprising:

a waveform translator configured to receive a simulated waveform for a node of a simulated prototype circuit and to translate the simulated waveform into a translated waveform, the translated waveform having a format different from a format of the simulated waveform; and

a test-and-measurement instrument configured to obtain a measured waveform from a node on a fabricated circuit that corresponds to the node of the simulated prototype circuit, the test-and-measurement instrument further configured to determine a deviation of the measured waveform from the simulated waveform using the translated waveform.

14. The system of claim 13, in which the waveform translator is further configured to replicate the simulated waveform to create a replicated waveform and to modify the replicated waveform by a predetermined amount corresponding to a desired tolerance.

15. The system of claim 13, in which the test-and-measurement instrument is further configured to determine a pass-fail criterion based on a maximum desired variance from the simulated waveform, the test-and-measurement instrument further being configured to identify the measured waveform as passing when the determined deviation of the measured waveform is within the pass-fail criterion, and the test-and-measurement instrument further being configured to identify the measured waveform as failing when the determined deviation of the measured waveform is outside of the pass-fail criterion.

16. The system of claim 13, in which the fabricated circuit corresponds to a design schematic for a physical prototype circuit, the system further comprising a three-dimensional model

generator configured to generate an electronic, three-dimensional model of the physical prototype circuit from manufacturing layout information for the fabricated circuit, the manufacturing layout information corresponding to the design schematic for the physical prototype circuit.

17. The system of claim 16, further comprising a vision system configured to obtain visual environment information for the fabricated circuit.

18. The system of claim 17, further comprising a scaler and mapper configured to scale and orient the three-dimensional model based on the visual environment information.

19. The system of claim 13, further comprising a non-contact system control interface configured to allow contactless user interaction with at least one of the waveform translator and the test-and-measurement instrument.

20. The system of claim 10, further comprising a circuit simulator configured to receive a design schematic for a physical prototype circuit and to model the physical prototype circuit to produce the simulated prototype circuit, the circuit simulator further configured to generate the simulated waveform for the node of the simulated prototype circuit.

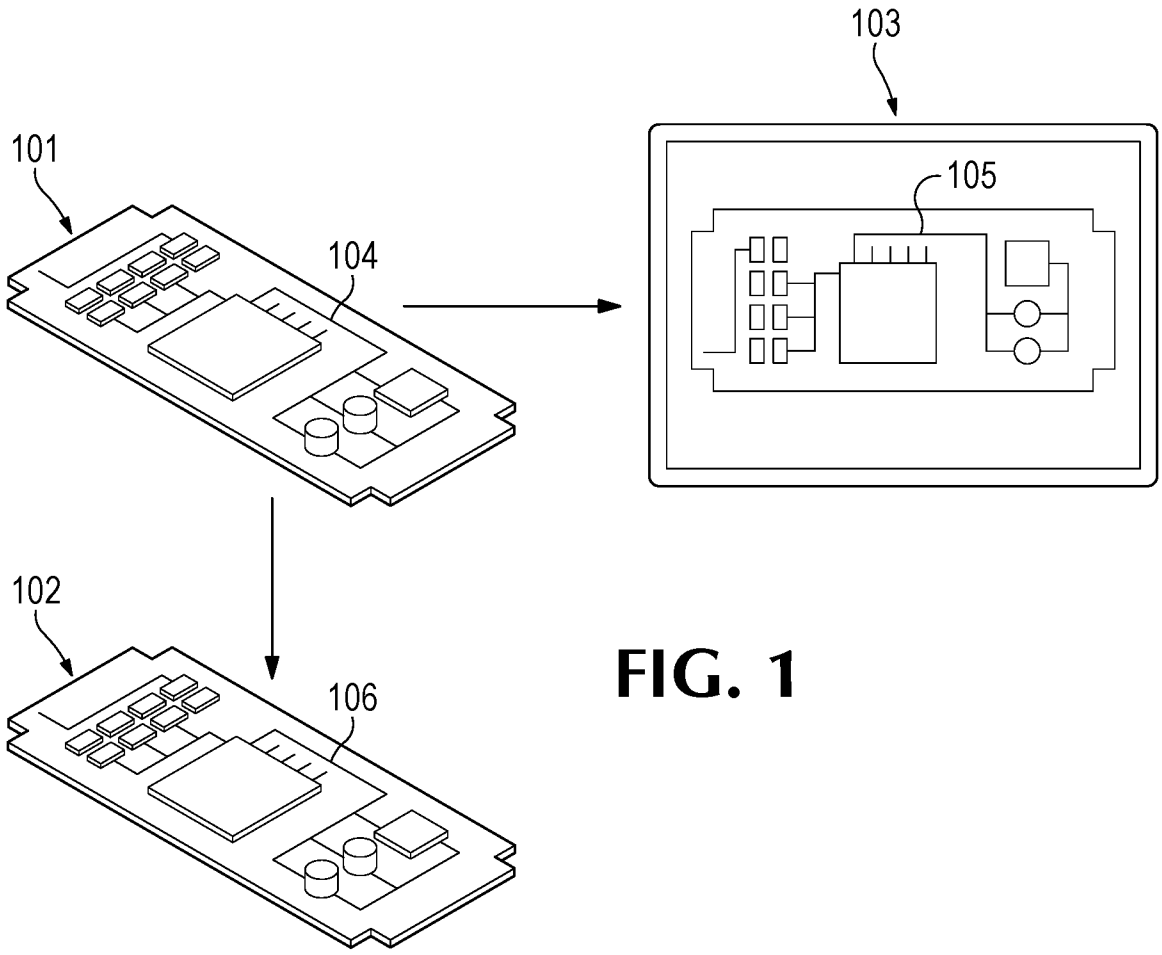


FIG. 1

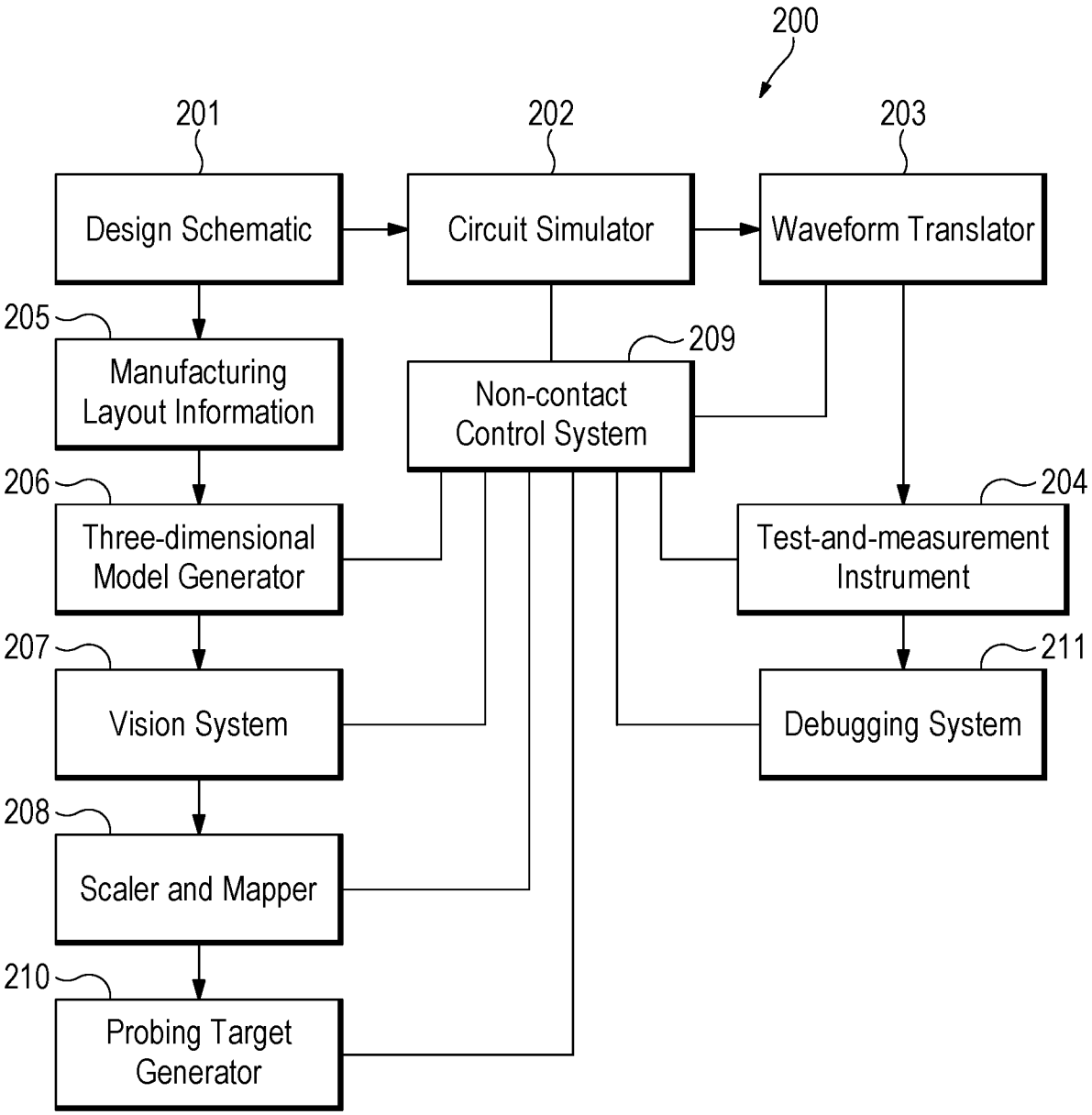

200
201
202
203
Design Schematic
Circuit Simulator
Waveform Translator
205
Manufacturing Layout Information
209
Non-contact Control System
206
Three-dimensional Model Generator
204
Test-and-measurement Instrument
207
Vision System
211
Debugging System
208
Scaler and Mapper
210
Probing Target Generator

FIG. 2

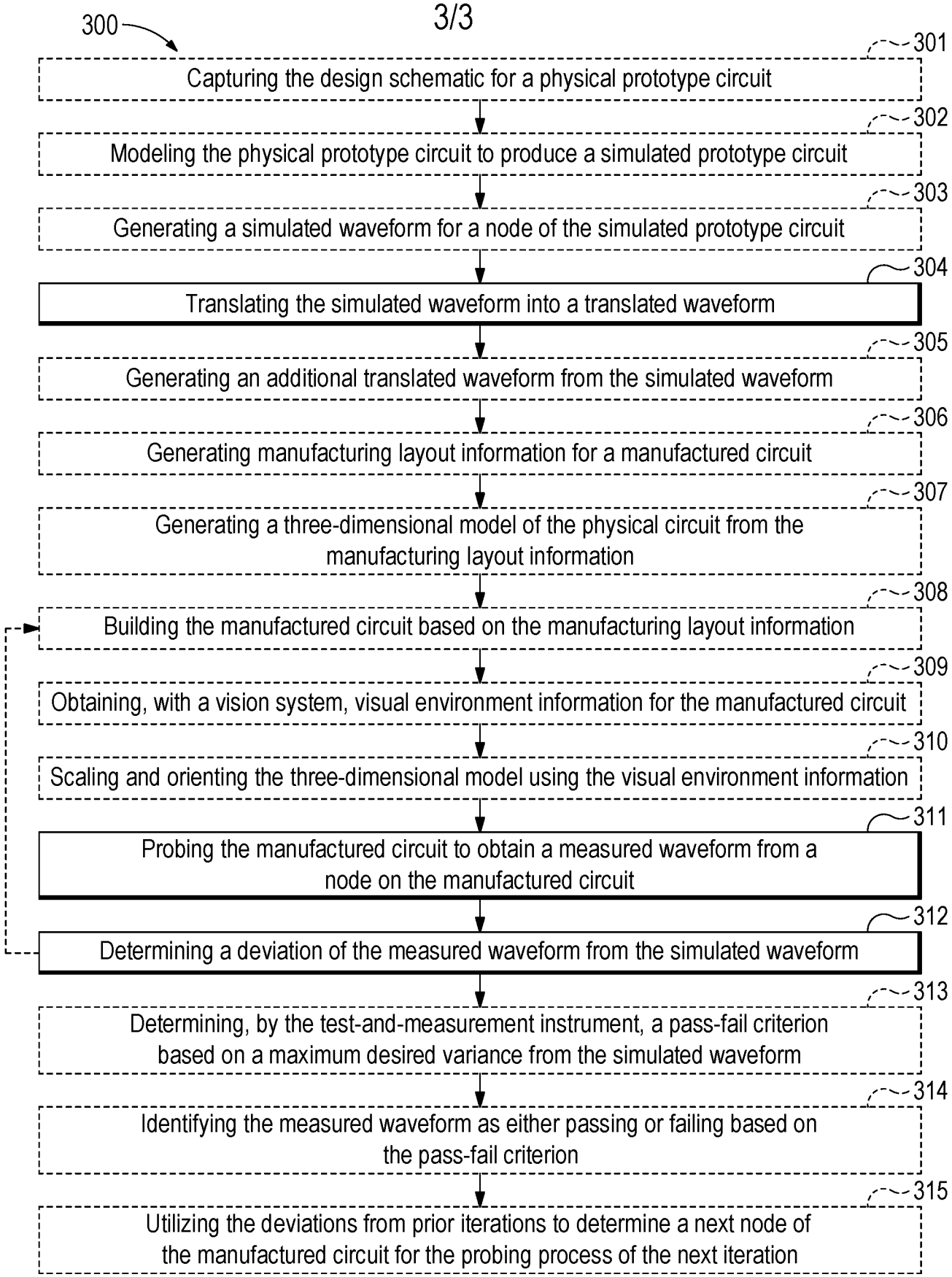

300
301
Capturing the design schematic for a physical prototype circuit
302
Modeling the physical prototype circuit to produce a simulated prototype circuit
303
Generating a simulated waveform for a node of the simulated prototype circuit
304
Translating the simulated waveform into a translated waveform
305
Generating an additional translated waveform from the simulated waveform
306
Generating manufacturing layout information for a manufactured circuit
307
Generating a three-dimensional model of the physical circuit from the manufacturing layout information
308
Building the manufactured circuit based on the manufacturing layout information
309
Obtaining, with a vision system, visual environment information for the manufactured circuit
310
Scaling and orienting the three-dimensional model using the visual environment information
311
Probing the manufactured circuit to obtain a measured waveform from a node on the manufactured circuit
312
Determining a deviation of the measured waveform from the simulated waveform
313
Determining, by the test-and-measurement instrument, a pass-fail criterion based on a maximum desired variance from the simulated waveform
314
Identifying the measured waveform as either passing or failing based on the pass-fail criterion
315
Utilizing the deviations from prior iterations to determine a next node of the manufactured circuit for the probing process of the next iteration

FIG. 3

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2021/040963

A. CLASSIFICATION OF SUBJECT MATTER

G01R 31/3183(2006.01)i; **G01R 23/16**(2006.01)i; **G01R 23/00**(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

G01R 31/3183(2006.01); G06F 17/50(2006.01); G06F 30/00(2020.01)

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords:test, waveform, simulation, verification, deviation

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 5325309 A (RAMIN HALAVIATI et al.) 28 June 1994 (1994-06-28) column 1, lines 64-67; column 3, lines 47-49; column 10, lines 20-22; column 13, lines 7-8; claims 1, 4; and figure 2	1-20
Y	US 2002-0040288 A1 (HIROAKI YAMOTO et al.) 04 April 2002 (2002-04-04) Paragraph [0063]; and figure 7	1-20
Y	KR 10-2019-0070876 A (TECTOTEK OY) 21 June 2019 (2019-06-21) Paragraphs [0074]-[0075]; claim 2; and figure 1	7-9,16-18
A	US 2007-0093999 A1 (PARAG BIRMIWAL et al.) 26 April 2007 (2007-04-26) Paragraphs [0022]-[0030]; claim 1; and figures 1-3	1-20
A	KR 10-2020-0005832 A (SK HYNIX INC. et al.) 17 January 2020 (2020-01-17) Paragraphs [0020]-[0055]; and figure 2	1-20

☐ Further documents are listed in the continuation of Box C. ☑ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"D" document cited by the applicant in the international application
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
28 October 2021	**29 October 2021**

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INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
PCT/US2021/040963

Patent document cited in search report	Publication date (day/month/year)	Patent family member(s)	Publication date (day/month/year)
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