(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
18 January 2007 (18.01.2007)

PCT

(10) International Publication Number
WO 2007/008701 A2

(51) International Patent Classification:
G11C 7/10 (2006.01)

(21) International Application Number:
PCT/US2006/026581

(22) International Filing Date: 10 July 2006 (10.07.2006)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
11/179,077 11 July 2005 (11.07.2005) US

(63) Related by continuation (CON) or continuation-in-part (CIP) to earlier application:
US 11/179,077 (CON)
Filed on 11 July 2005 (11.07.2005)

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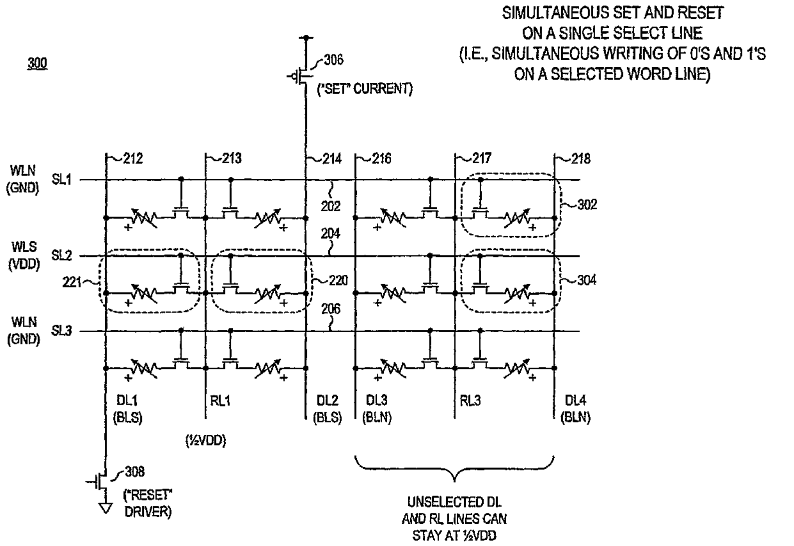
(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LV, LY, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IS, IT, LT, LU, LV, MC, NL, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:
— *without international search report and to be republished upon receipt of that report*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: APPARATUS AND METHOD FOR PROGRAMMING AN ARRAY OF NONVOLATILE MEMORY CELLS INCLUDING SWITCHABLE RESISTOR MEMORY ELEMENTS



(57) Abstract: A non-volatile memory cell includes a switchable resistor memory element in series with a switch device. An array of such cells may be programmed using only positive voltages. A method for programming such cells also supports a direct write of both 0 and 1 data states without requirement of a block erase operation, and is scalable for use with relatively low voltage power supplies. A method for reading such cells reduces read disturb of a selected memory cell by impressing a read bias voltage having a polarity opposite that of a set voltage employed to change the switchable resistor memory element to a low resistance state. Such programming and read methods are well suited for use in a three-dimensional memory array formed on multiple levels above a substrate, particularly those having extremely compact array line drivers on very tight layout pitch.

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APPARATUS AND METHOD FOR PROGRAMMING AN ARRAY OF NONVOLATILE MEMORY CELLS INCLUDING SWITCHABLE RESISTOR MEMORY ELEMENTS

TECHNICAL FIELD

The present invention relates to a nonvolatile memory array, and particularly to an array of nonvolatile memory cells having switchable resistor memory elements.

BACKGROUND ART

There are materials that have at least two distinct stable resistivity states. This class of materials can be switched from a high-resistivity state to a low-resistivity state by applying a voltage across the material having a given polarity. To switch the material from the low-resistivity state back to a high-resistivity state, a voltage having the opposite polarity can be applied.

Some of these materials can be switched between resistivity states at relatively low applied voltages, for example two volts or less. These properties would make these materials attractive for use in nonvolatile memory arrays, which retain their memory state even when power is removed from the device. Low-voltage switching is advantageous to reduce power consumption in devices, but many challenges must be overcome to provide the low voltages and reversible voltages required to operate cells incorporating such material, and to avoid accidental programming and/or erase during read.

DISCLOSURE OF INVENTION

In general, and without limiting the invention in any way, the invention is directed to a method for programming a memory array of nonvolatile memory cells having switchable resistor memory elements. Such a programming method may be implemented using only positive voltages, and is also well suited for use in a three-dimensional memory array formed on multiple levels above a substrate, particularly those having extremely compact array line drivers on very tight layout pitch. Such method also supports a direct write of both 0 and 1 data states without requirement of a block erase operation, and which is scalable for use with relatively low voltage power supplies.

In one aspect the invention provides a method for programming one or more memory cells of a memory array, each memory cell having a switchable resistor memory element in series with a switch device controlled by an associated select line, together coupled between an associated data line and a parallel associated reference line, said method comprising: (a) biasing a first data line and a parallel first reference line both associated with a first memory cell to respective voltages such that their relative polarity depends upon a data state to be programmed into the first memory cell; and (b) biasing a first select line to turn on the switch device in the first memory cell.

In another aspect the invention provide a method for programming one or more memory cells of a memory array, each memory cell having a switchable resistor memory element in series with a thin film transistor switch device controlled by an associated select line, together coupled between an associated data line and an associated reference line, said method comprising: (a) biasing a first data line and a first reference line both associated with a first memory cell to respective voltages such that their relative polarity depends upon a data state to be programmed into the first memory cell; and (b) biasing a first select line to turn on the switch device in the first memory cell.

In yet another aspect the invention provides a method for programming memory cells of a memory array, each memory cell having a switchable resistor memory element in series with a transistor switch device, said method comprising simultaneously programming a plurality of memory cells, programming at least one memory cell to a low-resistance state by impressing a set voltage thereacross having a first polarity, and programming at least one other memory cell to a high-resistance state by impressing a reset voltage thereacross having a second polarity opposite the first polarity.

In still another aspect the invention provides an integrated circuit comprising: (a) an array of memory cells, each memory cell having a switchable resistor memory element in series with a switch device controlled by an associated select line, together coupled between an associated data line and a parallel associated reference line; and (b) write circuitry for biasing a first data line and a parallel first reference line both associated with a first memory cell to respective voltages such that their relative polarity depends upon a data state to be programmed into the first memory cell.

In still another aspect the invention provides an integrated circuit comprising: (a) an array of memory cells, each memory cell having a switchable resistor memory element in series with a transistor switch device; and (b) write circuitry for simultaneously programming a plurality of memory cells, programming at least one memory cell to a low-resistance state by impressing a set voltage thereacross having a first polarity, and programming at least one other memory cell to a high-resistance state by impressing a reset voltage thereacross having a second polarity opposite the first polarity.

Each of the aspects and embodiments of the invention and the inventive features described herein can be used alone or in combination with one another. The invention in several aspects is suitable for integrated circuits having a memory array, for methods for operating such integrated circuits and memory arrays, and for computer readable media encodings of such integrated circuits or memory arrays.

The foregoing summary is illustrative only and is not intended to be in any way limiting of the invention, which is defined by the following claims. Other aspects, inventive features, and advantages of the invention may be apparent from the detailed description of the preferred embodiments set forth below.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a cross-sectional view of an exemplary memory cell structure useful for the present invention.

Fig. 2 is a schematic diagram representing an exemplary memory array structure as represented in Fig. 1.

Fig. 3 is a diagram of the current-voltage relationship of an exemplary switchable resistor memory element.

Fig. 4 is a schematic diagram depicting conceptual write conditions for certain embodiments of the present invention.

Fig. 5 is a diagram of the current-voltage relationship of an exemplary switchable resistor memory element to illustrate potential read disturb of the element.

Fig. 6 is a diagram of the current-voltage relationship of an exemplary switchable resistor memory element depicting preferred read conditions for some embodiments of the present invention.

Fig. 7 is a schematic diagram of an exemplary read circuit consistent with some embodiments of the invention.

Fig. 8 is a schematic diagram of another exemplary read circuit consistent with some embodiments of the invention.

Fig. 9 is a schematic diagram representing an exemplary memory array structure consistent with some embodiments of the invention.

Fig. 10 is a schematic diagram depicting conceptual write conditions for certain embodiments of the present invention using a memory array shown in Fig. 9.

Fig. 11 is a schematic diagram of an exemplary write circuit consistent with some embodiments of the invention.

Fig. 12 is a schematic diagram of another exemplary read circuit consistent with some embodiments of the invention.

Fig. 13 is a schematic diagram of yet another exemplary read circuit consistent with some embodiments of the invention.

Fig. 14 is a schematic diagram of still another exemplary read circuit consistent with some embodiments of the invention.

Fig. 15 is a cross-sectional diagram of a three-dimensional memory array consistent with some embodiments of the invention.

Fig. 16 is a diagram of the current-voltage relationship of an exemplary switchable resistor memory element depicting multiple set currents consistent with some embodiments of the present invention.

MODE(S) FOR CARRYING OUT THE INVENTION

It has been noted that some materials can be reversibly switched between more than one stable resistivity state, for example between a high-resistivity state and a low-resistivity state. For certain materials, the conversion from a high-resistivity state to low-resistivity state is affected by applying a voltage of a certain magnitude, called a *set* voltage magnitude, in one direction, while the reverse conversion, from a low-resistivity state to a high resistivity state, is affected by applying a voltage magnitude, called a *reset* voltage magnitude, in the opposite direction (i.e., opposite polarity).

A basic structure of a switchable resistor memory element for a non-volatile memory cell can be constructed by forming a variable resistance material between two electrodes. One such variable resistance material is amorphous silicon doped with V, Co, Ni, Pd, Fe or Mn, for example as described more fully in Rose et al., U.S. Patent No. 5,541,869. Another class of material is taught by Ignatiev et al. in U.S. Patent No. 6,473,332: these are perovskite materials such as $Pr_{1-X}Ca_XMnO_3$ (PCMO), $La_{1-X}Ca_XMnO_3$ (LCMO), $LaSrMnO_3$ (LSMO), or $GdBaCo_XO_Y$ (GBCO). Another option for this variable-resistance material is a carbon-polymer film comprising carbon black particulates or graphite, for example, mixed into a plastic polymer, as taught by Jacobson et al. in US Patent No. 6,072,716.

A preferred material is taught by Campbell et al. in U.S. Patent Application No. 09/943,190 (now U.S. Patent No. 6,881,623), and by Campbell in U.S. Patent Application No. 09/941,544 (now published as U.S. Patent Application Publication 2003/0047765). This material is doped chalcogenide glass of the formula A_XB_Y, where A includes at least one element from Group IIIA (B, Al, Ga, In, Tl), Group IVA (C, Si, Ge, Sn, Pb), Group VA (N, P, As, Sb, Bi), or Group VIIA (F, Cl, Br, I, At) of the periodic table, where B is selected from among S, Se and Te and mixtures thereof. The dopant is selected from among the noble metals and transition metals, including Ag, Au, Pt, Cu, Cd, Ir, Ru, Co, Cr, Mn or Ni. As will be described, in the present invention this chalcogenide glass (amorphous chalcogenide, not in a crystalline state) is formed in a memory cell adjacent to a reservoir of mobile metal ions. Some other solid electrolyte material could substitute for chalcogenide glass.

Exemplary variable resistance materials include many cases where the set threshold voltage is less than 1 volt, and some as low as 200 mV, which make them suitable for scaling.

The operation of chalcogenide glass in a memory cell is described more fully in U. S. Application No. 11/179,122 entitled "Nonvolatile Memory Cell Comprising Switchable Resistor and Transistor" by Roy E. Scheuerlein (hereinafter the "Scheuerlein I" application) and U. S. Application No. 11/179,095 entitled "Memory Cell Comprising a Thin Film Three-Terminal Switching Device Having a Metal Source and/or Drain Region" by Roy E. Scheuerlein and Christopher J. Petti (hereinafter the "Scheuerlein II" application), both applications hereby incorporated by reference in their entirety. Briefly, under voltage applied in one direction, mobile metal ions migrate from the adjacent ion reservoir, forming a conductive bridge through the chalcogenide layer. When the voltage is reversed, the metal ions migrate back into the ion reservoir, dissolving the conductive bridge and returning the chalcogenide material to its original high-resistivity state. In addition, additional descriptions of the formation of memory cell structures using such materials may also be found in these referenced applications.

Referring now to Fig. 1, a cross-sectional view is shown of a portion of an exemplary memory array 100 showing several memory cells. Each memory cell includes a field effect transistor and a switchable resistor memory element in series, together coupled between an associated data line and an associated reference line. In preferred embodiments, the FET may be a thin-film transistor adapted to be formed in a monolithic three dimensional memory array having more than one level of memory cells, thus forming a highly dense memory device. One such memory level is shown in the figure, which may represent one level of a three-dimensional array, or a two-dimensional array. Substantially parallel rails 102 (shown in cross section, extending out of the page) include a plurality of line sets 104, each line set 104 consisting of two data lines 106 (106a and 106b, for example) and one reference line 108 (108a, for example) immediately adjacent to and between the two data lines 106a and 106b. Above the rails 102 and preferably extending perpendicular to them are substantially parallel select lines 110. Select lines 110 are coextensive with gate dielectric layer 112 and channel layer 114. Transistors are formed between each adjacent data line and reference line pair. For example, transistor 120 includes channel region 122 between source region 124 and drain region 126. Each select line 110 controls the transistors it is associated with. Switchable resistance memory element 130 is disposed between channel region 122 and data line 106b. In this embodiment, adjacent transistors share a reference line; for example transistor 120 shares a reference line 108a with transistor 140. Transistor 140 also includes a switchable resistor memory element 150 between channel region 142 and data line 106a. No transistor exists in the region 152 between adjacent data lines 106b and 106c. A potential leakage path between data lines 106b and 106c may be prevented either by selectively doping channel layer 114 in this region 152 (as shown in the figure as a P doped region) or by removing this section of channel layer 114 using a channel trim masking step (not shown).

The switchable resistor memory element 130 includes a chalcogenide layer 132 located between two electrodes 134, 136. Chalcogenide layer 132 is amorphous, and is high-resistivity as formed, so switchable resistor memory element 130 is in a high-resistance state. Preferably the switchable resistor memory element 130 is a germanium containing chalcogenide. Electrode 136 is a source of mobile metal ions, preferably silver, and may be thought of as the anode electrode. Electrode 134 is any conductor which will not readily provide mobile metal ions, for example tungsten, aluminum, nickel, platinum, or heavily doped semiconductor material, and may be thought of as the cathode electrode. As can be seen, the cathode electrode is on the channel side of the resistor, while the anode electrode (i.e., the reservoir of mobile ions) is on the data line rail side of the resistor. The N+ doped polysilicon layer 138 may be used to up-diffuse dopants into the channel layer 114, to form the source region 126.

The transistor 120 is preferably a thin film transistor (TFT) formed of deposited Si, a Si-Ge alloy or Ge about 200 to 500 Angstroms thick with a HDP silicon dioxide gate layer and a word line. A TFT containing germanium or a silicon-germanium alloy can provide a lower threshold voltage and/or lower resistance switch device. It is preferable for memory cells with especially low threshold resistor material or for scaled technology where it is desirable to decrease voltages such as the select line voltage (due to the lower Vt of the device) and the drain-to-source voltage (due to the higher mobility of devices with SiGe alloys). The select line 110 may be any suitable conductor such as a doped polysilicon which is then salicided, or a tungsten-containing material. A corrugated channel reduces the short channel effect and allows very small spacing between data line rails without excessive short channel effects.

Additional fabrication details of such memory cells are described more fully in the aforementioned Scheuerlein I and Scheuerlein II applications previously incorporated. In addition, other cells suitable for use with this invention are described in these same applications.

Referring now to Fig. 2, a schematic diagram is shown of a memory array 200 such as that shown in Fig. 1. Three select lines 202, 204, 206 are shown, as well as two reference lines 213, 217 and four data lines 212, 214, 216, 218. Data lines 212, 214 and reference line 213 together form line set 208, and data lines 216, 218 and reference line 217 together form line set 210. The data lines are generally parallel to the reference lines (slight skews excepted), and both are generally perpendicular to the select lines. A total of twelve different memory cells are shown associated with various ones of these array lines. For example, memory cell

220 is associated with select line 204, data line 214, and reference line 213. The memory cell 220 includes a switchable resistor memory element 222 in series with a switch device 224, together coupled between the data line 214 and the reference line 213. Here, the switch device 224 is shown as a three-terminal transistor switch device, and more specifically, as a field effect transistor. The switchable resistor memory element 222 is indicated with a plus-sign ("+") at its end closest to the data line 214 to indicate the anode electrode. As will be described below, other memory cell configurations having the resistor connected to the reference line are also contemplated.

In the configuration shown, such select lines may be thought of by some as word lines, and the data lines may be thought of by some as bit lines. While such terminology is believed to be widely adopted by many in the art for many types of memory array structures, such terminology may imply, to some, a particular organization of the memory array, such as word width, page size, block size, etc., which may be limiting and is unintended herein. Consequently, the description that follows will generally use the more general terms of select lines, data lines, and reference lines.

Referring now to Fig. 3, an I-V curve (i.e., current-voltage curve) is shown which illustrates the basic operation of an exemplary switchable resistor memory element within the memory cell. When a positive voltage of a sufficient magnitude is applied to the anode electrode (e.g., electrode 136 in Fig. 1) relative to the voltage of the cathode electrode (e.g., electrode 134 in Fig. 1), electrons flow toward the anode electrode, while silver ions migrate from the anode electrode into the chalcogenide layer (e.g., the variable resistor material layer 132 in Fig. 1). The silver forms a conductive bridge across the chalcogenide layer, and the switchable resistor memory element is set to a low-resistance state. The critical voltage for causing this state change to occur may be called the write threshold voltage or the "set" voltage (labeled 253), and this causes the switchable resistor memory element to change from a high resistance state (shown as a linear I-V curve labeled 252) to a low-resistance state (shown as a linear I-V curve labeled 254). The actual resistance of the low-resistance state may continue to decrease as additional mobile ions (e.g., Ag ions) migrate into the variable resistor material layer, and so may be controlled by limiting the set current to a particular value of current (labeled as 256).

To change the switchable resistor memory element back to its high resistance state 252, the voltage across the switchable resistor memory element is reversed. A negative voltage is applied to the anode electrode relative to the voltage on the cathode electrode. Electrons flow toward the cathode electrode, the silver in the chalcogenide layer is oxidized, and silver ions migrate back into the anode electrode, thus breaking down the conductive bridge, and leaving the chalcogenide layer once again in its high-resistance state. The critical voltage for causing this state change to occur may be called the "reset" voltage (labeled 255), and this causes the switchable resistor memory element to change from the low resistance curve 254 to the high resistance curve 252.

For certain materials the SET voltage may be as low as 200 to 300 mV at a low current level. Also, the RESET voltage is likewise about –200 to –300 mV (about the same voltage, but much higher current).

The difference in resistance between the low-resistance and high-resistance states of the switchable resistor memory element may be readily and repeatably detectable, and in this way a memory state (data "0" or data "1", for example) can be stored into a memory cell and then later read. Of course, it is arbitrary which resistance state corresponds to a data 0 or a data 1. It may be customary to view certain non-volatile memory cells as being "programmed" to a data "0" state and "erased" to a data "1" state, but such association with specific data states is also arbitrary. It may also be customary to view non-volatile memory cells as being in an "erased" state as initially fabricated, and which cells are "programmed" to the other state, irrespective of which data states (i.e., data 1 and 0) correspond to such programmed and erased states. As used herein, memory cells may be programmed (i.e., written) to either data state. The "set" state refers to the low resistance state and the "reset" state refers to the high resistance state. A switchable resistor memory element is changed from a high-resistance state to a low-resistance state by applying a *set* voltage across the element having a certain magnitude and polarity (e.g., a "forward biased" resistor), while the reverse conversion is affected by applying a *reset* voltage having a certain magnitude and of the opposite polarity (e.g., a "reverse biased" resistor). The set and reset operation can be repeated many times. Any colloquial use herein of any of these various terms shall not be interpreted in conflict with this understanding or in a limiting manner. For convenience, "erasing" may be used to refer to an operation to change the switchable resistor memory element to its high resistance state. In such a context, "programming" may then be used to refer to an operation to change the switchable resistor memory element to a low resistance state. Thus, a programmed memory cell has been "set" to its low resistance state, and an erased memory cell has been "reset" to its high-resistance state.

it is important to carefully control the circuit conditions experienced by each cell during read, write, and erase. For example, when programming a cell to its low resistance state, if too little current is used to form the conductive bridge, the cell will not be highly conductive, the conductive state may be unreliable, and the difference between the programmed and unprogrammed state will be difficult to detect. If too much current is provided, the conductive bridge formed across the chalcogenide layer becomes so conductive that when an erase is attempted, the resistance of the conductive bridge is too low (the current is too high) to allow enough voltage to easily build up across the switchable resistor memory element sufficient to cause the silver in the bridge to oxidize and to migrate back to the anode electrode.

Referring still to Fig. 3, such relationships are illustrated. When programming a memory cell, preferably the current flowing through the switchable resistor memory element is limited to a certain value. This current limit for "set" (labeled 256) controls the magnitude of the low resistance state as the operating point of the switchable resistor memory element jumps upward from the critical set point (labeled 253) until it is limited by the set current limit 256.

When erasing a programmed memory cell, a sufficiently high amount of current must conduct through the memory cell to allow the switchable resistor memory element to reach the reset critical point 255. To ensure adequate margin, preferably a minimum amount of current 257 is provided through such device, which is by design more current than needed to reach the critical reset point 255 (i.e., the current magnitude crosses the I-V curve "below" the critical reset point, as shown).

Referring now to Fig. 4, the exemplary memory array 200 (here labeled 300) is shown with an exemplary write bias. The select lines 202, 206, the data lines 216, 218, and the reference line 217 are assumed to be unselected. The select line 204, the data lines 212, 214, and the reference line 213 are assumed to be selected, and thus memory cells 220, 221 are selected. In the figure shown, the selected memory cell 220 is shown as being programmed, while the selected memory cell 221 is shown as being erased.

In this embodiment, the unselected data lines 216, 218 and unselected reference line 217 are biased at a write standby voltage of approximately one-half VDD and unselected select lines 202, 206 are biased at ground. As used herein, VDD represents a power supply voltage operably coupled to such a memory array. VDD could be supplied by a connection to voltage sources outside the integrated circuit or produced by circuitry on the integrated circuit itself. While not necessarily required, VDD is preferably a positive voltage relative to a ground reference voltage (i.e., GND or "ground"). The unselected memory cells (e.g., unselected memory cell 302) and the half-selected memory cells (i.e., those cells, such as memory cell 304, associated with a selected word line (e.g., select line 204) contribute no power dissipation since the data line and reference line associated with each unselected and half-selected memory cell are both biased at the same voltage, and therefore no voltage is impressed across such memory cells.

In this embodiment the selected reference line(s) is also biased at ½VDD, which allows one of the associated selected data lines to be biased at a higher voltage to program memory cell 220, and also allows the other associated selected data line to be biased at a lower voltage to erase memory cell 221. In other words, with the selected reference line biased at ½VDD, the switchable resistor memory element within memory cell 220 may be forward biased and yet the switchable resistor memory element within memory cell 221 may be reversed biased. As long as the magnitude of the VDD voltage is large enough, both the set voltage and the reset voltage may be adequately developed across the respective resistor elements to simultaneously write a data 0 into one or more cells and write a data 1 into one or more other cells. Such a capability may be termed a direct write of both data 0 and data 1 states, and avoids any requirement for a block erase operation as is common in certain flash memory devices.

The data line 214 is biased to a VDD through a current limiting circuit 306, here shown as a PMOS device as might be employed in a current mirror circuit (with an appropriate bias on its gate terminal) or other suitable current limiting circuit. The magnitude of this current limiting circuit 306 is preferably set to provide a current equal to the set current limit 256 through the selected memory cell 220. For ease of understanding the bias conditions, this current limiting circuit 306 is shown conceptually as being directly connected to the selected data line 214. In many practical embodiments, there may actually be one or more intervening circuits, such as select devices, decoder circuits, etc. This current limiting circuit 306 may nevertheless be viewed as being coupled to the selected data line 214. Of course, any such intervening circuits should be carefully designed to not significantly interfere with the development of the necessary set voltage across the selected memory cell's resistor element at a current which is limited to the desired set current limit.

The data line 212 is biased to a ground through a current providing circuit 308, here shown as an NMOS device as might be employed in a driver circuit or other suitable current providing circuit. Such a driver circuit may as simple as a reasonable sized driver device coupled to a bias level, with a simple digital control used to control the device (to avoid providing another current value into the array). The magnitude of this current providing circuit 308 is preferably set to provide a current equal to the reset current 257 through the selected memory cell 221. As before, for ease of understanding the bias conditions, this current providing circuit 308 is shown conceptually as being directly connected to the selected data line 212. In many practical embodiments, there may actually be one or more intervening circuits, such as select devices, decoder circuits, etc. This current providing circuit 308 may nevertheless be viewed as being coupled to the selected data line 212. Again, any such intervening circuits should not significantly interfere with the development of the necessary reset voltage across the selected memory cell's resistor element at a current level at least that of the minimum reset current (and preferably with some margin higher than such reset current).

As mentioned above, it is important that the RESET current driver provides a current at least equal in magnitude (and opposite in polarity) to the SET current to ensure that the reset driver can force a voltage across the switchable resistor memory element that is greater than the RESET voltage. Accordingly, the SET current limit is substantially less than the minimum RESET current to ensure that memory cells do not get "stuck" in the SET state. In other words, $I_{SET} < I_{RESET}$ for proper operation.

While a single line set of array lines is shown in Fig. 4 as being selected (i.e., in this embodiment a single reference line and two associated data lines), additional line sets may also be selected to thus select additional data lines. Accordingly, a plurality of memory cells along a selected word line can be written to an arbitrary choice of the set or reset data states, respectively, in the same operation, thereby providing for a direct write of 0 or 1 data states, i.e. avoiding the use of a block mode erase operation as in many types of Flash memory.

In the embodiment shown, such a direct write capability is provided even though only positive voltages are used for the various array lines. Alternatively, in some other embodiments, both positive and negative voltages may be utilized. For example, the selected reference line could be biased at ground, and a positive voltage used to set a selected memory cell, and a negative voltage used to reset a selected memory cell. In this case the unselected data lines 216, 218 and unselected reference line 217 are preferably biased at a write standby voltage of ground.

The bias conditions shown in Fig. 4 also provide for a low latency write capability. Between write operations (i.e., write cycles), all data lines and reference lines can be biased at a write standby voltage of ½VDD, and all select lines can be biased at ground. Then, to write a memory cell, a selected word line is driven high, and the selected data lines are biased above or below the write standby voltage. The bulk of the memory array lines need not be re-biased to accomplish the write operation. In particular, there is no need for charge pump circuits to drive many unselected lines to voltages above VDD (i.e., above the highest power supply voltage operably coupled to the memory array), which can require considerable time before the write could proceed. If desired, the selected word line voltage can be capacitively coupled above VDD for higher drive on the TFT devices within the memory cells. Preferably the selected word line may be boosted to a voltage of VDD plus about 1.0 to 1.5 volts.

In some embodiments suitable for very low VDD operation, the reference line may be biased at VDD and the selected data line biased to either ground or a boosted level of about 2VDD (such as might be generated using charge pump circuits or other suitable circuits). Such an embodiment would be useful if the VDD power supply choice is less than the voltage required to set or reset the memory cell through the various drivers and the IR drops of the memory array lines. Such a boosted data line would likely increase write latency and/or increase power dissipation to operate such charge pump circuits.

It should be noted that because the reference lines and the data lines are parallel, and both are perpendicular to the word lines, any given reference line only must support current flow through at most two selected memory cells. As a result, voltage drops due to the resistance of the reference line (i.e., so-called "IR drops") are reduced. Such IR drops can negatively affect both the writing and particularly the reading of such memory cells, as described in more detail below. Moreover, in other embodiments described herein, each selected reference line supports current flow through only a single selected memory cell.

While the reset driver 308 and the set current limiting circuit 306 are shown, for clarity of illustrating exemplary voltage bias levels, as being coupled to respective data lines at opposite ends thereof, in many practical memory array embodiments both such circuits may be located in close physical proximity to each other, and may both be coupled to the respective data lines at the same end of such data lines.

Referring now to Fig. 5, the potential disturb of a reset state during a read operation can occur when the memory cell is biased with a forward biased voltage across the switchable resistor memory element. A linear TFT load line 320 is shown in the upper-right quadrant of the I-V curve, corresponding to a positive voltage being impressed across a selected memory cell (i.e., a voltage across the memory cell resulting in a forward biased resistor element), or in other words, a read voltage having the same polarity as the set voltage on the switchable resistor memory element.

This TFT load line 320 intersects the operating curves for the switchable resistor memory element well above the current corresponding to the set voltage (i.e., point 253), and results in a disturb of the memory cell to a lower resistance state. In the case depicted, the resistance would be disturbed to the point 321 which may be above the normal set current value (point 258) as is shown, or which may be below such point 258 (e.g., point 323, as shown for an exemplary diode load line 322), but in any case represents a total destruction of the memory cell data state from the high resistance state to a low resistance state.

Alternatively, a constant load current may be utilized, represented by a flat load line 324, to ensure that the voltage across the switchable resistor memory element does not reach the set voltage. Such a constant current would need to be less in magnitude than the current corresponding to the set voltage (i.e., the current at point 253). Such small values of current, particularly for large, heavily loaded array lines, would lead to very long time constants for array lines to stabilize, and thus would increase the time to sense the data state of the memory cell. Moreover, even small amounts of noise could still trigger a disturbance of one or more memory cells.

Using a forced voltage at a very low level (e.g., 100 mV) with current mode sensing avoids disturb because the voltage across the switchable resistor memory element can never reach the set voltage. But this requires a very low resistance switch device within the memory cell, and the voltage control problems of such low voltages still risk disturb. This is particularly difficult in 3D memory arrays where the arrays are potentially subject to more noise, and where the array lines could be of higher resistance materials. In addition, it is more difficult to fabricate a very low resistance switch device in such 3D memory arrays, and the load line slope of the switch device should be comparable to the low resistance state to not lose signal.

On one hand, the low set voltage of such switchable resistor memory elements makes them very suitable for scaling and use in high density memory arrays. Many such materials have a set threshold voltage that is less than 1 volt, and some as low as 200 mV. On the other hand, however, due to such very low set thresholds, it is difficult to read the data state of the memory cell with good performance and without disturbing the memory cell.

Referring now to Fig. 6, the switching behavior of the resistor element and the load line representing the resistance of the TFT switch device during a read with reverse bias is shown. A linear TFT load line 330 is shown in the lower-left quadrant of the I-V curve, corresponding to a negative voltage being impressed across a selected memory cell (i.e., a voltage across the memory cell resulting in a reverse-biased resistor element), or in other words, a read voltage having the opposite polarity as the set voltage of the switchable resistor memory element. The resistance and therefore the slope of the switch device load line 330 preferably is comparable to the low resistance state (load line 254) so as not to dilute the signal available from the cell. In this read method the read voltage magnitude can be significantly larger than the switching threshold of the low resistance state (i.e., the set voltage) while avoiding disturb concerns. The current sensed is indicated by the intersection points with the SET state line (labeled 332) and RESET state line (labeled 334). The read point 334, as can be seen, resides at a greater voltage magnitude than the set voltage (although opposite in polarity). The available signal may actually be a little larger than shown because the switchable resistor memory element is preferably on the data line side of the memory cell, which may act as the source side of the TFT switch device when reading the memory cell. The bias of the source decreases the current through the TFT for the high resistance state, and yet hardly changes the current through the TFT for the low resistance state. The resistance of the TFT device is preferably comparable to the low-resistance state

In various embodiments herein , the read voltage impressed across a selected memory cell may be larger in magnitude than the set voltage of the memory cell. The read voltage impressed on the array may for convenience in circuit design be as large as the programming voltages applied to the array. This may be accomplished by using a bias voltage on the select line (e.g., the word line) that is higher during programming than during read. This provides for a select device having as low a resistance as possible during the set operation (subject to device breakdown limitations), and particularly helps realize a switch device having a resistance low enough to allow the application of the desired current limit for set. As seen in Fig. 6, in reverse bias during read the load line of the TFT has a higher voltage drop i.e. flatter load line than the IV curve of the low resistance state accomplished by using a bias voltage on the select line that is lower during read than was used during write. This protects the low resistance state from disturb during reading as the load line intersects the low resistance I-V curve (at point 332) significantly below the critical point for disturb of the low resistance state (i.e., the reset voltage, point 255).

As shown in Fig 6, in reverse bias the TFT has a lower voltage drop i.e. steeper load line than the IV curve of the high resistance state. Hence the high resistance state sees a high bias voltage under read conditions. The high resistance state is inherently protected from disturb under these conditions because the bias voltage is in a direction to reinforce the change to the high resistance state. This protects the high resistance state from disturb.

Referring to Fig. 7, a read circuit arrangement 350 is shown which utilizes voltage-clamped data line sensing. As before in regards to the programming discussion, the select lines 202, 206, the data lines 216, 218, and the reference line 217 are assumed to be unselected. The select line 204, the data lines 212, 214, and the reference line 213 are assumed to be selected, and thus memory cells 220, 221 are selected.

In this embodiment, the unselected array lines (i.e., unselected data lines, reference lines, and select lines) are biased at a read standby voltage equal to ½VDD. The unselected memory cells and the half-selected memory cells (i.e., associated with a selected word line but an unselected data line) contribute no power dissipation since the data line and reference line associated with each such cell are both biased at ½VDD, and thus no voltage is impressed across such memory cells.

In this embodiment the selected reference line(s) is driven to a voltage above ½VDD (e.g., ½VDD + 0.5 volts), which reverse biases both selected memory cells 220, 221. The selected data line 212 is voltage clamped to ½VDD (and thus biased to ½VDD). Current flowing on the selected data line 212 through the selected memory cell 221 is sensed to determine whether the switchable resistor memory element within the selected memory cell 221 is in the set data state or the reset data state. The selected word line 204 is driven to VDD and unselected word lines WLN 202, 206 are maintained at ground potential. The standby biases are compatible with the biases of some of the write embodiments such as the write method described above and shown in Fig. 4 for low latency read and write operations.

A two device driver circuit (transistors 352, 354) is connected to each data line. If the data line is selected, a SELECT signal 356 enables device 352 to couple the selected data line 212 to a bus line 358. Conversely, if the particular data line is unselected, the SELECT signal 356 enables device 354 to couple the unselected data line to ½VDD, and device 352 is off to thereby decouple an unselected data line from the bus line 358.

A clamp device 360 is biased with a BIAS signal 362 having a magnitude appropriate for maintaining the selected data line at about ½VDD. Such a bias voltage 362 may be generated using a feedback-controlled circuit which comprehends the ½VDD voltage, the threshold voltage of the PMOS transistor 360, device temperature, etc. A resistor 366 coupled between node 364 and ground represents a load circuit that provides a reference current which preferably is set to a magnitude halfway between the respective expected cell currents for a low-resistance and a high-resistance data state in the memory cell. An amplifier or comparator circuit 368 compares the signal on node 364 to a reference voltage (not shown) to generate an output signal reflecting the data state of the selected memory cell.

The read circuit shown is somewhat of an idealized circuit, as additional selection or decoding devices may actually be present in the read path between the selected memory cell and the clamp device 360. Exemplary current sensing circuits are described in greater detail in "CURRENT SENSING METHOD AND APPARATUS PARTICULARLY USEFUL FOR A MEMORY ARRAY OF CELLS HAVING DIODE-LIKE CHARACTERISTICS" by Roy E. Scheuerlein, U. S. Application No. 09/896,468, filed June 29, 2001, which application is hereby incorporated by reference in its entirety.

Any such intervening circuits should be designed to not significantly interfere with the read signal. Preferably the resistance of the read path should be designed to be less than or comparable to the switchable resistor memory element in the memory cell to yield good signal margin.

Since the selected reference line 213 is shared with a second data line 214, the memory cell 220 may optionally be sensed at the same time. The read bias conditions depicted provide for a fast read capability, as all non-selected array lines can stay at ½VDD without consuming power in the array. When an address is received and decoded, the selected word line can be quickly driven to its selected level (even if boosted above VDD) and the selected reference line driven quickly to its selected level. The selected word line preferably is driven to VDD for high read performance, but in other embodiments could be boosted to an active level 1.0 to 1.5 volts above VDD. Other line sets, two data lines and one reference line, can simultaneously be biased to read at least two more memory cells. In an exemplary three-dimensional memory array having four memory levels, an exemplary read configuration may simultaneously read four memory cells from each of the four memory levels, for a total of 16 memory cells.

Referring to Fig. 8, a read circuit arrangement 370 is shown which also utilizes voltage-clamped data line sensing, and which arrangement shows a variation of the selection circuitry of the previous configuration. Using a bias advantageous for low VDD applications, the unselected array lines are biased at a VDD-level read standby voltage. The selected reference line(s) is driven to a voltage above VDD (e.g., VDD + 0.5 volts), and the selected data line 212 is voltage clamped to VDD (i.e., biased to VDD). A clamp device 360 is used, as before, to provide this bias, and sensing proceeds as in the previous configuration using a reference current resistor 366 and amplifier 368.

In this configuration, however, a hierarchical data line arrangement is presumed, in which the data lines within the array correspond to local data lines, one of which is selected and coupled to an associated global data line, which is then further selected and steered to the sensing circuit. For example, the data line 212 corresponds to a local bit line, which is coupled by a selection device 352 to a global bit line 376. One or more additional selection devices (e.g., selection device 372) may further be utilized to select one of several global bit lines and couple the selected one to sense and write driver circuitry. Further description of exemplary global bit line arrangements is set forth in U.S. Application No. 10/403,752 by Roy E. Scheuerlein, et al, entitled "Three-Dimensional Memory Device Incorporating Segmented Bit Line Memory Array", filed on March 31, 2003 (now published as U.S. Patent Application Publication 2004/0188714), which application is hereby incorporated by reference in its entirety. Such global bit line configurations may also be employed with many of the embodiments of the present invention described herein.

Since the selected reference line 213 is shared with a second "local" data line 214, the selected memory cell associated with data line 214 may optionally be sensed at the same time. In addition, additional line sets (e.g., in this embodiment, two data lines and their shared reference line) may also be simultaneously selected to allow reading of more than two memory cells at the same time. In another exemplary configuration, eight memory cells from a single memory level may be simultaneously accessed (i.e., read or written).

Referring now to Fig. 9, an alternate memory array structure 400 is shown in which each reference line is associated with only a single data line. Three select lines 402, 404, 406 are shown, as well as three reference lines 413, 417, 421 and three data lines 412, 416, 420. Data line 412 and reference line 413 together form a line set. Likewise, data line 416 and reference line 417 together form a line set, and data line 420 and reference line 421 together form a line set. The data lines are generally parallel to the reference lines (slight skews excepted), and both are generally perpendicular to the select lines. A total of nine different memory cells are shown associated with various ones of these array lines.

In the configuration shown, such select lines may also be referred to as word lines, and the data lines as bit lines. Consequently, the select line 402 (also labeled SL1) is in addition labeled parenthetically as word line 1. The remaining array lines are also labeled with alternate terminology, which is provide in the figure for convenience, and not in a limiting sense. For example, even though the data line 416 is also referred to as "e.g., bit line 2", such reference does not preclude such a data line in fact corresponding to a local bit line, or corresponding to some other array line in another configuration. Moreover, use of such convenient terminology should not be taken to necessarily imply any particular organization of the memory array, such as word width, page size, block size, etc.

The memory array structure 400 may be implemented with a similar structure to that shown in Fig. 1, with one of the data lines removed and an isolation region (e.g., region 152) provided between adjacent but not associated array lines (e.g., between reference line RL1 and data line DL2 in Fig. 9). In addition, a memory array structure 400 may be implemented using a vertical TFT device formed below a switchable resistor memory element. Details of exemplary vertical memory cell structures and their formation is set forth in the aforementioned Scheuerlein I application previously incorporated.

Referring now to Fig. 10, a conceptual method is shown for writing both data 0 and data 1 into a memory array such as that shown in Fig. 9 having non-shared reference lines. The select lines 402, 406 (also both labeled WLN for "word line not selected"), the data line 416, and the reference line 417 are assumed to be unselected. The select line 404 (also labeled WLS for "word line selected"), the data lines 412, 420, and the reference lines 413, 421 are assumed to be selected, and thus memory cells 422, 423 are selected. In the figure shown, the selected memory cell 423 is shown as being "programmed" (changed to the set state), while the selected memory cell 422 is shown as being "erased" (changed to the reset state).

In this embodiment 430, the unselected array lines (i.e., unselected data lines, reference lines, and select lines) are preferably biased at a write standby voltage of ground, although the unselected data lines and reference lines may be biased at any of several other voltages, such as VDD or ½VDD. The unselected memory cells and the half-selected memory cells contribute no power dissipation as there is no voltage impressed across such memory cells.

In this memory array embodiment a selected reference line is biased at a voltage depending upon the data state to be programmed, as is the associated selected data line. In other words, the bias conditions on both a selected data line and its associated reference line both depend upon the data state to be programmed. For example, to program memory cell 423 to the set state, the data line 420 is biased at VDD through a current limiting circuit 440 (configured to limit current flow into the data line to the magnitude of the desired set current), while the reference line 421 is driven to ground through a select device 442. In this manner, the switchable resistor memory element within the memory cell 423 may be impressed with a forward biased voltage greater than the set voltage.

Conversely, to program memory cell 422 to the reset state, the data line 412 is biased at ground by a reset driver 436 (and by way of an intervening select device 434), while the associated reference line 413 is driven to VDD through a select device 432. In this manner, the switchable resistor memory element within the memory cell 422 may be impressed with a reversed biased voltage and driven with sufficient current to exceed the reset voltage across the resistor element.

This arrangement allows the entire VDD voltage to be utilized in developing the requisite set or reset voltage within a selected memory cell. More specifically, it allows almost the entire VDD voltage to be impressed across a selected memory cell, to promote developing a voltage across the switchable resistor memory element within the selected memory cell that reaches the requisite set or reset voltage. Consequently, this array configuration and write arrangement is particularly well suited for use with a very low power supply voltage, i.e., about half the magnitude of a minimum power supply voltage used for a mid-value reference line biasing scheme as shown in Fig. 4.

Each of the various selection devices 432, 434, 438, 442 may represent one or more levels of decoding and/or selection devices, including use with a hierarchical array line structure (e.g., global bit lines/local bit lines). In many practical embodiments, there may actually be several intervening select devices, decoder circuits, etc. This current limiting circuit 440 may nevertheless be viewed as being coupled to the selected data line 420. Such intervening circuits should be carefully designed to not significantly degrade the voltage on the data line.

The data line 412 is biased to a ground through a current providing circuit, here shown as an NMOS reset driver 436 coupled to a bias level (e.g., ground), with a simple digital control used to control the device, or other suitable current providing circuit. This current providing circuit 436 may be viewed as being coupled to the selected data line 412, notwithstanding one or more intervening selection devices and circuits.

One or more line sets may be simultaneously selected. Accordingly, a plurality of memory cells along a selected word line can be written to an arbitrary choice of the set or reset data states, respectively, in the same operation, thereby providing for a direct write of 0 or 1 data states, i.e. avoiding the use of a block mode erase operation as in many types of Flash memory.

In the embodiment shown, such a direct write capability is provided even though only positive voltages are used for the various array lines. Alternatively, in some other embodiments, both positive and negative voltages may be utilized. For example, the selected reference line could be biased at ground, and a positive voltage used to set a selected memory cell, and a negative voltage used to reset a selected memory cell.

The bias conditions shown in Fig. 10 also provide for a low latency write capability. Between write operations (i.e., write cycles), all array lines can be biased at a particular write standby voltage. Then, to write a memory cell, a selected word line is driven high, and the selected data lines and reference lines are biased in accordance with the data states to be programmed. The bulk of the memory array lines need not be re-biased to accomplish the write operation. Preferably the selected word line may be boosted to a voltage of VDD plus about 1 to 1.5 volts.

It should be noted that because the reference lines and the data lines are parallel, and both are perpendicular to the word lines, any given reference line only must support current flow through a single selected memory cells. As a result, voltage drops due to the resistance of the reference line (i.e., so-called "IR drops") are reduced, and pattern sensitivities may be likewise greatly reduced.

While the reset driver 436 and the set current limiting circuit 440 are shown as being coupled to respective data lines at opposite ends thereof, in many practical memory array embodiments both such circuits may be located in close physical proximity to each other, and may both be coupled to the respective data lines at the same end of such data lines.

Referring now to Fig. 11, memory array 450 illustrates an embodiment for write circuitry for a memory array of the type shown in Fig. 9 having non-shared reference lines. This arrangement may be viewed as accomplishing the conceptual configuration described in the previous figure.

Two arrangements are actually depicted in this figure. On the left side of the figure, an arrangement is shown having a data line driver coupled to one end of the data line, and having a reference line driver coupled to the other end of the reference line. To program memory cell 422 to the set state, the data line 412 is biased at VDD through a current limiting circuit 452, while the reference line 413 is driven to ground through a driver device 464. Both the reset driver 454 and the reset driver 462 remain off. Conversely, to program memory cell 422 to the reset state, the data line 412 is biased at ground by a reset driver 454, while the associated reference line 413 is driven to VDD through a reset driver 462, and both set driver 452 and set driver 464 remain off.

The data line 412 is coupled through one or more selection device 458, 460 to a bus line 456, which is then driven high or low by one of the two drivers 452, 454. In addition, the reference line 413 is coupled through one or more selection devices 468 to a bus line 466, which is then driven high or low by one of the two drivers 462, 464. As noted, if the data line is driven high, the reference line is driven low, and vice versa.

On the right side of the figure, an arrangement is shown having a data line driver and a reference line driver coupled to the same ends of the data line and reference line, but otherwise the circuitry and its operation is similar. To program memory cell 423 to the set state, the data line 420 is biased at VDD through a current limiting circuit 452, while the reference line 421 is driven to ground through a driver device 464. Both the reset driver 454 and the reset driver 462 remain off. Conversely, to program memory cell 423 to the reset state, the data line 420 is biased at ground by a reset driver 454, while the associated reference line 421 is driven to VDD through a reset driver 462, and both set driver 452 and set driver 464 remain off.

The data line 420 is coupled through one or more selection device 458, 460 to a bus line 456, which is then driven high or low by one of the two drivers 452, 454. In addition, the reference line 421 is coupled through one or more selection devices 468, 461 to a bus line 466, which is then driven high or low by one of the two drivers 462, 464. Also shown are devices 459, 469, which couple the data line and reference line, respectively, to a write standby voltage of, for example, ½VDD conveyed on node 470.

In some preferred embodiments, the selection circuit closest to the data line and reference line (i.e., coupled directly to the data line and reference line) is a two-device decoder head circuit, such as that formed by devices 458, 459. As the exemplary circuit shows, both the pullup current and the pulldown current for the respective data states for both a data line and for a reference line are preferably conducted through the respective NMOS transistor of such a two-device driver. Such two-device driver heads are useful in multi-headed decoder arrangements. Exemplary multi-headed decoders, useful for both row and column decoder circuits, are set forth in: "Multi-Headed Decoder Structure Utilizing Memory Array Line Driver with Dual Purpose Driver Device" by Roy E. Scheuerlein and Matthew P. Crowley, U. S. Patent No. 6,856,572, the disclosure of which is hereby incorporated by reference in its entirety; in "Tree Decoder Structure Particularly Well-Suited to Interfacing Array Lines Having Extremely Small Layout Pitch" by Roy E. Scheuerlein and Matthew P. Crowley, U. S. Patent No. 6,859,410, the disclosure of which is hereby incorporated by reference in its entirety; in "Dual-Mode Decoder Circuit, Integrated Circuit Memory Array Incorporating Same, and Related Methods of Operation" by Kenneth K. So, Luca G. Fasoli and Roy E. Scheuerlein, U. S. Application No. 11/026,493 filed on December 30, 2004 (now published as U.S. Patent Application Publication 2006/0145193), which application is hereby incorporated by reference in its entirety; and in "Apparatus and Method for Hierarchical Decoding of Dense Memory Arrays Using Multiple Levels of Multiple-Headed Decoders" by Luca G. Fasoli, et al., U. S. Application No. 11/026,470, filed December 30, 2004 (now published as U.S. Patent Application Publication 2006/0146639), the disclosure of which is hereby incorporated by reference.

Unselected data lines in a multi-headed decoder arrangement are held at the read or write standby (i.e., inactive) voltage. This allows efficient array line driver layout in 2D and especially 3D array implementations with very tight array line pitches. Moreover, use of such driver circuits allows improved layout, as all such devices nearest the array in a simultaneously selected group of array lines can be the same type (e.g., NMOS). By use of only positive voltages, the layout of such driver circuits may be reduced in area since device wells need not contemplate bipolar voltages relative to ground. In some embodiments, various ones of the decoder outputs may be boosted above VDD, particularly such outputs as control selection devices 458 and 460.

Several embodiments for reading a memory array having non-shared reference lines will be next described. Referring now to Fig. 12, a memory array 480 is shown which utilizes voltage-clamped data line sensing much like that shown in Fig. 7. The unselected array lines (i.e., unselected data lines, reference lines, and select lines) are biased at a read standby voltage equal to VDD. The unselected and half-selected memory cells contribute no power dissipation.

The selected reference line(s) is driven to a voltage above VDD (e.g., VDD + 0.5 volts), which reverse biases the selected memory cell 422. The selected data line 412 is voltage clamped to VDD. Current flowing on the selected data line 412 through the selected memory cell 422 is sensed to determine whether the switchable resistor memory element within the selected memory cell 422 is in the set data state or the reset data state.

A select device 352 couples the selected data line 412 to a bus line 358. A clamp device 360 is biased with a BIAS signal 362 having a magnitude appropriate for maintaining the selected data line 412 at about VDD. Sensing node 364 proceeds as in the earlier embodiment. Likewise, the read bias conditions depicted provide for a fast read capability, as all non-selected array lines can stay at VDD without consuming power in the array.

There would be less signal if, within the memory cell, the resistor element is instead on the drain side of the switch because the source voltage would drop, decreasing the resistance of the switch, when sensing a high resistance state. But embodiments with resistor elements on the drain side are also envisioned, as long as the anode side of the resistor is still on the more negative side, i.e. still biased during read in the direction of a RESET operation.

In cell arrangements that do not share reference lines between columns of memory cells, sensing can be done on the reference line. Referring now to Fig. 13, a memory array 500 is shown in which the selected reference line is voltage clamped to a positive read voltage (relative to the read standby voltage) and current sensed. Clamp control device 502 is biased at a level appropriate for maintaining a read voltage of about 0.5 volts on the selected reference line 413, and resistor 504, node 506, and amplifier 508 (which are analogous to resistor 366 and amplifier 368) generate an output signal reflective of the data state.

This arrangement still impresses a read voltage across the selected memory cell that reverse biases the switchable resistor memory element, and specifically that is opposite in polarity to the set voltage for the switchable resistor memory element. In addition, sensing the reference line as shown allows the read standby voltage to be ground rather than VDD. Advantageously, we can use an NMOS select device (e.g., 502) as a clamp device, which has a lower resistance than a PMOS device, and which helps keep the resistance modest relative to the memory cell resistance element. Note that such an arrangement may also be viewed alternatively as sensing a data line while holding the reference line at ground, with the relative position of the switchable resistor memory element and transistor switch device within the memory cell reversed to that shown. Such an embodiment is particularly appropriate in a vertical memory cell structure in which the reference lines are not shared. Consequently, in the claims that follow, no relative position of the resistor element and the switch device within a memory cell is to be presumed unless explicitly recited in the claim.

Alternatively, we can sink current from the selected data line that is less than the critical point for disturbing the low resistance state, and detect voltage. Referring now to Fig. 14, an array 520 is shown which utilizes voltage sensing rather than current sensing. This eliminates the data line clamp circuit, but may be slower if there is significant capacitance on the data lines. Note that the V_{GS} of the switch device within the selected memory cell 422 is about the same for both reading a “1” and reading a “0” because the TFT source voltage of the device is just the V_{DS} of the TFT switch device (at a known magnitude of current, as determined by the "I_{SENSE}" current source circuit 526) below the reference line voltage. Thus, the voltage signal developed on the data line (which may range from approximately VDD to almost ground) is determined by the sense current passing through either the high-resistance or low-resistance value of the switchable resistor memory element. In other words, the difference in voltage for the two data states is determined by the sense current times the difference in the high-state and low-state values of resistance. However, there would be less signal if the resistor element is on the drain side of the switch (i.e., closest to the reference line rather than to the data line) because the source voltage of the TFT switch device would drop, decreasing the resistance of the switch, when we are sensing a high resistance state. Consequently, the resistance of the TFT would not remain essentially constant, and would offset some of the high resistance state, and generate less total signal. An exemplary data line select device 522 is shown coupling the selected data line to a bus line 524, which is shown as an input of amplifier 528, although any number of various selection configurations may alternatively be used, including those having additional levels of selection and/or decoding.

Referring now to Fig. 15, a cross-sectional view is shown representing array lines of a three-dimensional memory array 600. Four memory levels are depicted, with each level including multiple line sets of coplanar array lines (two line sets of which are shown perpendicular to the plane of the page). In this example, each line set includes a pair of data lines (in this embodiment also described as bit lines) and a shared reference line disposed between and adjacent to the data lines. Each memory level also includes a plurality of select lines (in this embodiment also described as word lines), one of which is shown traversing from left to right on the page. For clarity, four of the array lines are labeled consistent with the embodiment shown in Fig. 2.

In various embodiments, one or more memory cells may be written and/or read (i.e., accessed) at the same time. Obviously, if one memory cell is accessed, then only one select line, only one data line, and only one reference line is involved. However, if more than one memory cell is accessed, more than one data line is involved by necessity, and possibly more than one word line and more than one reference line.

For example, four memory cells may be accessed on a single memory level, all four associated with the same word line. In the embodiment shown, all four depicted data lines and both reference lines would be involved (assuming that the selected line sets are adjacent, although such is not required). Alternatively, four memory cells may be accessed with two cells disposed on each of two memory levels. Preferably this would be accomplished by selecting a respective line set on each level, but other configurations are contemplated. For example, a line set could be selected, and only one of the two data lines actually biased at a different level than the reference line, leaving the other data line essentially unselected. Thus, two different line sets on each of two memory levels could be selected to access four memory cells. If, alternatively, each line set included only a single data line (e.g., Fig. 9), then such a configuration would be a preferred configuration.

In some embodiments a group of adjacent data lines is simultaneously selected on each of a group of adjacent memory levels to simultaneously access a plurality of memory cells. For example, sixteen memory cells may be accessed by selecting all sixteen data lines shown in the figure, all eight reference lines shown, and all four word lines shown. Decoding and/or selection circuitry may be more easily accomplished when simultaneously selected data lines are adjacent, both horizontally and vertically. Nevertheless, numerous variations of simultaneous access of more than one memory cell are suggested by the above description, and are specifically contemplated.

In the above embodiments, each memory cell is assumed to have either a low-resistance state or a high-resistance state, thereby providing for a single data bit stored in each memory cell. However, since the value of the low-resistance state may be controlled by limiting the magnitude of the set current that is allowed to flow through a memory cell when programmed to the "set" state, in some embodiments a memory cell may be programmed to one of several "set" states.

Referring now to Fig. 16, an I-V curve illustrates such operation with more than one set state. The critical "set" voltage (labeled 253) remains as before, and when reached, causes the switchable resistor memory element to change from the high resistance state 252 to a lower-resistance state. If the set current is limited to that shown as STATE 1, then the actual resistance of the low-resistance state 1 will be set to the point labeled 652 (and the associated SET STATE 1 resistive line through the origin). Similarly, a set current for STATE 2 results in a resistance corresponding to point 654, and a set current for STATE 3 results in a resistance corresponding to point 258.

Such a cell is preferably read with reverse bias. A linear TFT load line 330 is shown in the lower-left quadrant of the I-V curve, corresponding to a negative voltage being impressed across a selected memory cell. The resistance and therefore the slope of the switch device load line 330 preferably is comparable to the lowest resistance state (load line 254) so as not to dilute the signal available from the cell. The current sensed is indicated by the intersection points with the three SET state lines (labeled 653, 655, 332) and RESET state line (labeled 334). Each of these bias points 334, 653, 655, 332 corresponds respectively to the amount of read current in Set State 1, Set State 2, Set State 3, and the Reset State.

The reset current should be at least as large as the highest set current limit. To set a memory cell to one of the intermediate values, the cell may be reset to the highest-resistance state, and then set to the appropriate one of the set states. Such a reset operation may be carried out on an entire block of memory cells (e.g., a page of data at a time) before any memory cells are programmed to one of the set states. Such a block reset may be implemented internally as sequential reset operations, each for resetting one or more memory cells, using as many of such internal reset operations as is required to "erase" the entire block, even if such a block erase is initiated by a single command and appears to execute as a single operation. Such operation would provide for compatibility with page oriented memory integrated circuits having erase operations embodied in on-chip control logic, similar to commercially available NAND flash memory devices.

Alternatively, a memory cell could be set from one set state to a "higher" set state without such an initial "erase" operation (e.g., by first reading the memory cell to determine its current state before programming), but this would be data dependent.

A memory cell in a large array may be disturbed when voltage is applied to neighboring cells, for example to a cell on a shared conductor. In arrays such as that taught in, for example, Herner et al., U.S. Patent Application No. 11/125,939, "Rewriteable Memory Cell Comprising a Diode and a Resistance-Switching Material," filed May 9, 2005, hereby incorporated by reference, a resistance-switching material is paired with a diode to provide electrical isolation. A diode is not the most advantageous choice of use with materials such as those described herein. The resistance-switching materials of the present invention utilize bi-directional voltage and current, while a diode is generally a one-way device. In addition, the relatively low switching voltages of many of the resistance-switching materials contemplated for use in the present invention are difficult to achieve given the relatively high turn-on voltages associated with most conventional diodes, assuming a reasonably low power supply voltage.

Another monolithic three dimensional memory array comprising transistors and resistance-switching memory elements is described in Petti, U.S. Patent Application No. 11/143,269, entitled "Rewriteable Memory Cell Comprising a Transistor and Resistance-Switching

Material in Series," filed June 2, 2005, owned by the assignee of the present invention, and hereby incorporated by reference. The resistance switching materials described therein are both set and reset with the same polarity of voltage. A risk of read disturb arises from the very low reset voltage that changes the low-resistance state to the high-resistance state. Such memory cells are likewise advantageously read with a read voltage that is opposite in polarity than the set voltage. In this case, the read voltage is opposite in polarity to *both* the set and reset voltages.

As used herein, a current source (i.e., also "constant current" source) may be viewed as a circuit providing generally a constant current irrespective of the voltage impressed across the device. Examples include a current mirror circuit. In many such practical constant current circuits, the magnitude of the "constant" current may diminish as the voltage across the circuit is reduced. A "current limiting circuit" may also be thought of as such a constant current source, although the "current limiting" terminology acknowledges that the constant current may decrease for some bias voltages thereacross, but the current therethrough is nonetheless limited to a maximum magnitude for all such biases.

As used herein, a node which is "biased to a voltage higher than X" may mean that the node is coupled to a voltage source through a constant current or current limiting circuit, such that the voltage developed on the biased node is indeed higher than X, but not necessarily of a predictable or fixed voltage value. As used herein, "coupling a node to a voltage" may include one or more intervening devices, such that the node may not necessarily reach the voltage. For example, a node may be coupled to a first voltage through a current limiting circuit, and possibly through one or more selection devices.

As used herein the SET state is assumed to be a low-resistance state, while the RESET state is assumed to be a high-resistance state. The SET action is for programming the memory cell resistor to the SET state; likewise for RESET action is for programming the memory cell resistor to the SET state. The SET threshold is in a forward direction, and RESET threshold in a reverse direction.

In some embodiments, the memory cells may be formed entirely in a semiconductor substrate. In other embodiments, including many of those described above, the memory cells are formed entirely in layers formed above such a substrate, including non-semiconductor substrates. Many specific forms of a switchable resistor memory element are contemplated, including those set forth in the aforementioned Scheuerlein I and Scheuerlein II applications previously incorporated.

In some embodiments, a non-shared reference line may be biased at an intermediate voltage, such as ½VDD, and the associated data line driven above or below the voltage of said reference line (similar to that shown in Fig. 4).

The phrases "programming a memory cell to a set state" and "programming the switchable resistor memory element within a memory cell to a set state" and "programming a memory cell to a low-resistance state" and "programming the switchable resistor memory element within a memory cell to a low-resistance state" may be used interchangeably herein, and no subtle distinctions should be inferred from such use.

In most preferred embodiments, memory array support is formed in the substrate beneath the memory, and electrical connections must be made from the ends of the data lines, reference lines, and select lines of the array to this circuitry. An advantageous scheme for making these connections while minimizing use of substrate area is described in Scheuerlein et al., U.S. Patent No. 6,879,505, "Word Line Arrangement Having Multi-Layer Word Line Segments for Three-Dimensional Memory Array," owned by the assignee of the present invention and hereby incorporated by reference. Moreover, in certain embodiments, such support circuitry may include select line decoders and data line decoders arranged in a checkerboard fashion beneath a three-dimensional memory array formed above a substrate. Additional information regarding exemplary checkerboard arrangements may be found in U.S. Patent No.: 6,735,104, issued May 11, 2004, which is hereby incorporated by reference in its entirety.

A monolithic three dimensional memory array is one in which multiple memory levels are formed above a single substrate, such as a wafer, with no intervening substrates. The layers forming one memory level are deposited or grown directly over the layers of an existing level or levels. In contrast, stacked memories have been constructed by forming memory levels on separate substrates and adhering the memory levels atop each other, as in Leedy, US Patent No. 5,915,167, "Three dimensional structure memory." The substrates may be thinned or removed from the memory levels before bonding, but as the memory levels are initially formed over separate substrates, such memories are not true monolithic three dimensional memory arrays.

A monolithic three dimensional memory array formed above a substrate comprises at least a first memory level formed at a first height above the substrate and a second memory level formed at a second height different from the first height. Three, four, eight, or indeed any number of memory levels can be formed above the substrate in such a multilevel array.

As used herein, a "global array line" (e.g., a global bit line) is an array line that connects to array line segments in more than one memory block, but no particular inference should be drawn suggesting such a global array line must traverse across an entire memory array or substantially across an entire integrated circuit.

Based upon the teachings of this disclosure, it is expected that one of ordinary skill in the art will be readily able to practice the present invention. The descriptions of the various embodiments provided herein are believed to provide ample insight and details of the present invention to enable one of ordinary skill to practice the invention. Nonetheless, in the interest of clarity, not all of the routine features of the implementations described herein are shown and described. It should, of course, be appreciated that in the development of any such actual implementation, numerous implementation-specific decisions must be made in order to achieve the developer's specific goals, such as compliance with application- and business-related constraints, and that these specific goals will vary from one implementation to another and from one developer to another. Moreover, it will be appreciated that such a development effort might be complex and time-consuming, but would nevertheless be a routine undertaking of engineering for those of ordinary skill in the art having the benefit of this disclosure.

For example, decisions as to the number of memory cells within each array or sub-array, the particular configuration chosen for word line and bit line pre-decoder and decoder circuits and bit line sensing circuits, as well as the word organization, are all believed to be typical of the engineering decisions faced by one skilled in the art in practicing this invention in the context of developing a commercially-viable product. As is well known in the art, various row and column decoder circuits are implemented for selecting a memory block, and a word line and bit line within the selected block, based upon address signals and possibly other control signals. Nonetheless, even though a mere routine exercise of engineering effort is believed to be required to practice this invention, such engineering efforts may result in additional inventive efforts, as frequently occurs in the development of demanding, competitive products.

While circuits and physical structures are generally presumed, it is well recognized that in modern semiconductor design and fabrication, physical structures and circuits may be embodied in computer readable descriptive form suitable for use in subsequent design, test or fabrication stages as well as in resultant fabricated semiconductor integrated circuits. Accordingly, claims directed to traditional circuits or structures may, consistent with particular language thereof, read upon computer readable encodings and representations of same, whether embodied in media or combined with suitable reader facilities to allow fabrication, test, or design refinement of the corresponding circuits and/or structures. The invention is contemplated to include circuits, related methods or operation, related methods for making such circuits, and computer-readable medium encodings of such circuits and methods, all as described herein, and as defined in the appended claims. As used herein, a computer-readable medium includes at least disk, tape, or other magnetic, optical, semiconductor (e.g., flash memory cards, ROM), or electronic medium and a network, wireline, wireless or other communications medium. An encoding of a circuit may include circuit schematic information, physical layout information, behavioral simulation information, and/or may include any other encoding from which the circuit may be represented or communicated.

The foregoing description has described only a few of the many possible implementations of the present invention. For this reason, this detailed description is intended by way of illustration, and not by way of limitation. Variations and modifications of the embodiments disclosed herein may be made based on the description set forth herein, without departing from the scope and spirit of the invention. It is only the following claims, including all equivalents, that are intended to define the scope of this invention. Moreover, the embodiments described above are specifically contemplated to be used alone as well as in various combinations. Accordingly, other embodiments, variations, and improvements not described herein are not necessarily excluded from the scope of the invention.

CLAIMS:

1. A method for programming one or more memory cells of a memory array, each memory cell having a switchable resistor memory element in series with a switch device controlled by an associated select line, together coupled between an associated data line and a parallel associated reference line, said method comprising:

biasing a first data line and a parallel first reference line both associated with a first memory cell to respective voltages such that their relative polarity depends upon a data state to be programmed into the first memory cell; and

biasing a first select line to turn on the switch device in the first memory cell.

2. The method as recited in claim 1 further comprising:

limiting current flow through the first memory cell to a first magnitude for one polarity of the first data line relative to the first reference line, to change the switchable resistor memory element within the first memory cell to a low resistance state, and

providing a current flow through the first memory cell of at least a second magnitude for the other polarity of the first data line relative to the first reference line, to change the switchable resistor memory element within the first memory cell to a high resistance state.

3. The method as recited in claim 2 wherein the second magnitude is higher than the first magnitude.

4. The method as recited in claim 2 further comprising:

limiting current flow through the first memory cell to a second magnitude for said one polarity of the first data line relative to the first reference line, to change the switchable resistor memory element within the first memory cell from the high resistance state to a second low resistance state.

5. The method as recited in claim 2 further comprising:

programming the first memory cell to one of the high-resistance and low-resistance states during a block operation for the memory array; then programming the first memory cell to the other of the high-resistance or low-resistance states if the data state to be programmed corresponds to the other such data state.

6. The method as recited in claim 2 further comprising:

programming the first memory cell to the high-resistance; then

programming the first memory cell to one of a plurality of low-resistance states, by limiting current flow through the first memory cell to one of a plurality of current magnitudes, for said one polarity of the first data line relative to the first reference line.

7. The method as recited in claim 1 wherein the biasing step comprises:

biasing the first reference line to a predetermined voltage; and

biasing the first data line to a voltage level above or below the predetermined voltage according to the data state to be programmed into the first memory cell.

8. The method as recited in claim 7 wherein the biasing the first data line step comprises:

coupling the first data line to a first voltage through a first circuit that provides at most a first current level to change the switchable resistor memory element within the first memory cell to a low resistance state, or to a second voltage through a second circuit that provides at least a second current level to change the switchable resistor memory element within the first memory cell to a high resistance state, according to the data state to be programmed into the first memory cell.

9. The method as recited in claim 8 wherein the second current level has a higher magnitude than the first current level.

10. The method as recited in claim 8 further comprising:

coupling the first data line through a given data line selection device to both the first circuit and the second circuit; and

enabling one of the first circuit and the second circuit in accordance with the data state to be programmed into the first memory cell.

11. The method as recited in claim 10 wherein:
the given data line selection device comprises an NMOS transistor.

12. The method as recited in claim 11 further comprising:
driving a gate terminal of the given data line selection device to a voltage above both the first and second voltages.

13. The method as recited in claim 7 wherein the predetermined voltage comprises an intermediate voltage between a first power supply voltage and a ground reference voltage.

14. The method as recited in claim 13 further comprising:
coupling the first data line to either the first power supply voltage through a pullup circuit or to the ground reference voltage through a pulldown circuit according to the data state to be programmed into the first memory cell.

15. The method as recited in claim 14 wherein:
one of the pullup or pulldown circuits is employed to reset the switchable resistor memory element within the first memory cell to a high resistance state, and the other one of the pullup or pulldown circuits is employed to set the switchable resistor memory element within the first memory cell to a low resistance state; and
the current through the pullup or pulldown circuit employed to reset the switchable resistor memory element has a higher magnitude than the one employed to set the switchable resistor memory element.

16. The method as recited in claim 13 wherein:
the intermediate voltage is approximately one-half of the first power supply voltage relative to the ground reference voltage.

17. The method as recited in claim 13 further comprising:
biasing unselected data lines and reference lines at the intermediate voltage;
biasing unselected switch device select lines at the ground reference voltage; and

programming selected one or more memory cells by transitioning only one or more selected data lines and switch device select lines to respective bias conditions for programming.

18. The method as recited in claim 1 wherein respective bias voltages on both the first data line and the first reference line are determined by the data state to be programmed into the first memory cell.

19. The method as recited in claim 18 wherein the first-mentioned biasing step comprises:

coupling the first reference line to one of a first voltage and a second voltage in accordance with the data state to be programmed into the first memory cell; and

coupling the first data line to the other of the second voltage and the first voltage.

20. The method as recited in claim 18 further comprising:

coupling one of the first data line and first reference line to a first voltage through a first circuit that provides at most a first current level, and coupling the other of the first data line and first reference line to a second voltage, to change the switchable resistor memory element within the first memory cell to a low-resistance state; or

coupling said one of the first data line and first reference line to the second voltage through a second circuit that provides at least a second current level, and coupling said other of the first data line and first reference line to the first voltage, to change the switchable resistor memory element within the first memory cell to a high-resistance state;

according to the data state to be programmed into the first memory cell.

21. The method as recited in claim 20 further comprising:

coupling said one of the first data line and first reference line through a given data line selection device to a common node which is coupled to both the first and second circuits.

22. The method as recited in claim 18 further comprising:

for a first data state to be programmed into the first memory cell, coupling one of the first data line and first reference line to a first power supply voltage and coupling the other one of the first data line and first reference line to a ground reference voltage; and

for a second data state to be programmed into the first memory cell, coupling said one of the first data line and first reference line to the ground reference voltage and coupling said other one of the first data line and first reference line to the first power supply voltage.

23. The method as recited in claim 22 wherein:

a reset current employed to change the switchable resistor memory element within the first memory cell to a high resistance state, has a higher magnitude than a set current employed to change the switchable resistor memory element within the first memory cell to a low resistance state.

24. The method as recited in claim 22 further comprising:

for the first data state to be programmed into the first memory cell, coupling the first data line to the first power supply voltage through a first current limiting circuit and coupling the first reference line to the ground reference voltage; and

for the second data state to be programmed into the first memory cell, coupling the first data line to the ground reference voltage and coupling the first reference line to the first power supply voltage.

25. The method as recited in claim 24 wherein the each memory cell switch device comprises a TFT switch device coupled between its switchable resistor memory element and its associated reference line.

26. The method as recited in claim 1 further comprising:

biasing a second data line and a parallel reference line both associated with a second memory cell to respective voltages such that their relative polarity depends upon a data state to be programmed into the second memory cell; and

turning on the switch device in the second memory cell;

wherein the respective data state for the first and second memory cells are different.

27. The method as recited in claim 26 wherein:

the memory array comprises a monolithic three-dimensional memory array having more than one memory level formed above a substrate;

the reference line associated with the second memory cell comprises a second reference line separate from the first reference line; and

the first and second memory cells reside on separate memory levels.

28. The method as recited in claim 26 wherein:

the first reference line and the reference line associated with the second memory cell comprise a single shared reference line; and

the first and second memory cells share a common select line coupled to the respective switch device therein.

29. The method as recited in claim 28 wherein:

the memory array comprises a monolithic three-dimensional memory array having more than one memory level formed above a substrate; and

each memory level comprises shared reference lines which are each disposed between a respective pair of data lines.

30. The method as recited in claim 28 further comprising:

biasing the first reference line to an intermediate voltage between a first power supply voltage and a ground reference voltage.

31. The method as recited in claim 30 further comprising:

coupling the first data line to either a first power supply voltage through a respective pullup circuit or to a ground reference voltage through a respective pulldown circuit according to the data state to be programmed into the first memory cell; and

coupling the second data line to either the first power supply voltage through a respective pullup circuit or to the ground reference voltage through a respective pulldown circuit according to the data state to be programmed into the second memory cell.

32. The method as recited in claim 26 further comprising:

simultaneously programming the first and second memory cells to different data states.

33. The method as recited in claim 32 further comprising:

simultaneously programming the first and second memory cells from respective first and second data states directly to respective second and first data states without utilizing a block erase operation.

34. A method for programming one or more memory cells of a memory array, each memory cell having a switchable resistor memory element in series with a thin film transistor switch device controlled by an associated select line, together coupled between an associated data line and an associated reference line, said method comprising:

biasing a first data line and a first reference line both associated with a first memory cell to respective voltages such that their relative polarity depends upon a data state to be programmed into the first memory cell; and

biasing a first select line to turn on the switch device in the first memory cell.

35. The method as recited in claim 34 wherein:

the memory array comprises a monolithic three-dimensional memory array having more than one memory level formed above a substrate.

36. The method as recited in claim 34 wherein:

the first data line and the first reference line are parallel.

37. The method as recited in claim 34 further comprising:

limiting current flow through the first memory cell to a first magnitude for one polarity of the first data line relative to the first reference line, to change the switchable resistor memory element within the first memory cell to a low resistance state, and

providing a current flow through the first memory cell of at least a second magnitude for the other polarity of the first data line relative to the first reference line, to change the switchable resistor memory element within the first memory cell to a high resistance state.

38. The method as recited in claim 37 wherein the second magnitude is higher than the first magnitude.

39. The method as recited in claim 37 further comprising:

limiting current flow through the first memory cell to a second magnitude for said one polarity of the first data line relative to the first reference line, to change the switchable resistor memory element within the first memory cell from the high resistance state to a second low resistance state.

40. The method as recited in claim 37 further comprising:

programming the first memory cell to one of the high-resistance and low-resistance states during a block operation for the memory array; then

programming the first memory cell to the other of the high-resistance or low-resistance states if the data state to be programmed corresponds to the other such data state.

41. The method as recited in claim 37 further comprising:

programming the first memory cell to the high-resistance; then

programming the first memory cell to one of a plurality of low-resistance states, by limiting current flow through the first memory cell to one of a plurality of current magnitudes, for said one polarity of the first data line relative to the first reference line.

42. The method as recited in claim 34 wherein the biasing step comprises:

biasing the first reference line to a predetermined voltage; and

biasing the first data line to a voltage level above or below the predetermined voltage according to the data state to be programmed into the first memory cell.

43. The method as recited in claim 42 wherein the biasing the first data line step comprises:

coupling the first data line to a first voltage through a first circuit that provides at most a first current level to change the switchable resistor memory element within the first memory cell to a low resistance state, or to a second voltage through a second circuit that provides at least a second current level to change the switchable resistor memory element within the first memory cell to a high resistance state, according to the data state to be programmed into the first memory cell.

44. The method as recited in claim 42 wherein the predetermined voltage comprises an intermediate voltage between a first power supply voltage and a ground reference voltage.

45. The method as recited in claim 44 wherein:

the intermediate voltage is approximately one-half of the first power supply voltage relative to the ground reference voltage.

46. The method as recited in claim 34 wherein respective bias voltages on both the first data line and the first reference line are determined by the data state to be programmed into the first memory cell.

47. The method as recited in claim 46 wherein the first-mentioned biasing step comprises:

coupling the first reference line to one of a first voltage and a second voltage in accordance with the data state to be programmed into the first memory cell; and

coupling the first data line to the other of the second voltage and the first voltage.

48. The method as recited in claim 46 further comprising:

coupling one of the first data line and first reference line to a first voltage through a first circuit that provides at most a first current level, and coupling the other of the first data line and first reference line to a second voltage, to change the switchable resistor memory element within the first memory cell to a low-resistance state; or

coupling said one of the first data line and first reference line to the second voltage through a second circuit that provides at least a second current level, and coupling said other of the first data line and first reference line to the first voltage, to change the switchable resistor memory element within the first memory cell to a high-resistance state;

according to the data state to be programmed into the first memory cell.

49. A method for programming memory cells of a memory array, each memory cell having a switchable resistor memory element in series with a transistor switch device, said method comprising:

simultaneously programming a plurality of memory cells, programming at least one memory cell to a low-resistance state by impressing a set voltage thereacross having a first polarity, and programming at least one other memory cell to a high-resistance state by impressing a reset voltage thereacross having a second polarity opposite the first polarity.

50. The method as recited in claim 49 further comprising:

simultaneously programming a first memory cell and a second memory cell from respective first and second data states directly to respective second and first data states, the first and second data states corresponding respectively to a reset state and a set state of the switchable resistor memory element within a memory cell;

wherein a set voltage impressed across the first memory cell to set its switchable resistor memory element is of opposite polarity as a reset voltage impressed across the second memory cell to reset its switchable resistor memory element.

51. The method as recited in claim 49 wherein:

each memory cell is coupled between as associated data line and an associated reference line;

the reference line associated with each simultaneously programmed memory cell is biased at a reference level; and

the associated data line for at least one of the simultaneously programmed memory cells is biased at a voltage higher than the reference level; and

the associated data line for at least one of the simultaneously programmed memory cells is biased at a voltage lower than the reference level.

52. The method as recited in claim 49 wherein:

the memory array comprises a monolithic three-dimensional memory array having more than one memory level formed above a substrate.

53. The method as recited in claim 49 wherein:

each memory cell is coupled between as associated data line and an associated reference line; and

the data lines and the reference lines are parallel.

54. The method as recited in claim 53 wherein:

each reference line is shared by two data lines.

55. An integrated circuit comprising:

an array of memory cells, each memory cell having a switchable resistor memory element in series with a switch device controlled by an associated select line, together coupled between an associated data line and a parallel associated reference line; and

write circuitry for biasing a first data line and a parallel first reference line both associated with a first memory cell to respective voltages such that their relative polarity depends upon a data state to be programmed into the first memory cell.

56. The integrated circuit as recited in claim 55 wherein:

the memory array comprises a monolithic three-dimensional memory array having more than one memory level formed above a substrate.

57. The integrated circuit as recited in claim 56 wherein:

the respective switch device within each memory cell comprises a thin film transistor.

58. An integrated circuit comprising:

an array of memory cells, each memory cell having a switchable resistor memory element in series with a transistor switch device; and

write circuitry for simultaneously programming a plurality of memory cells, programming at least one memory cell to a low-resistance state by impressing a set voltage thereacross having a first polarity, and programming at least one other memory cell to a high-resistance state by impressing a reset voltage thereacross having a second polarity opposite the first polarity.

59. The integrated circuit as recited in claim 58 wherein:

the memory array comprises a monolithic three-dimensional memory array having more than one memory level formed above a substrate.

60. The integrated circuit as recited in claim 59 wherein:

the respective switch device within each memory cell comprises a thin film transistor.

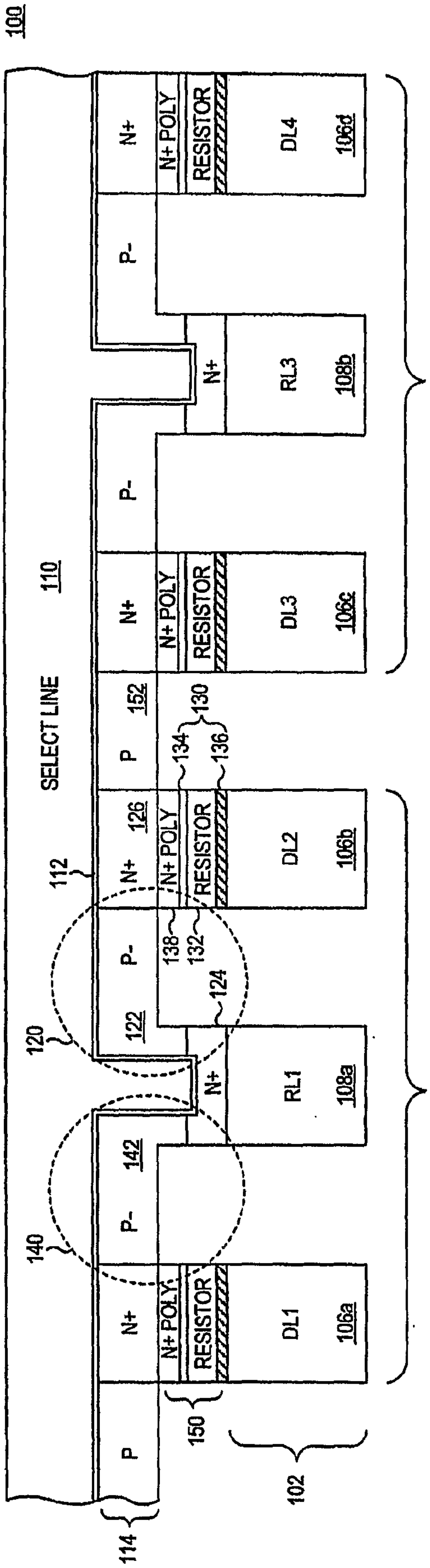
100
SELECT LINE
110
112
120
122
140
142
152
N+
P-
P
N+ POLY
RESISTOR
126
130
134
136
138
132
124
DL1
106a
DL2
106b
DL3
106c
DL4
106d
RL1
108a
RL3
108b
104
102
114
150

FIG. 1

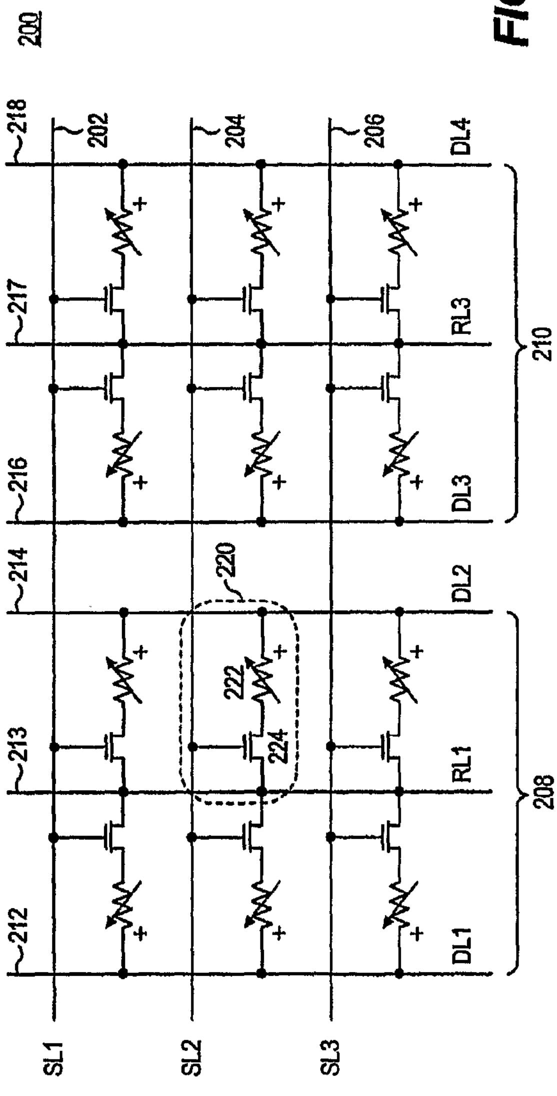
200
202
204
206
212
213
214
216
217
218
208
210
220
222
224
SL1
SL2
SL3
DL1
RL1
DL2
DL3
RL3
DL4

FIG. 2

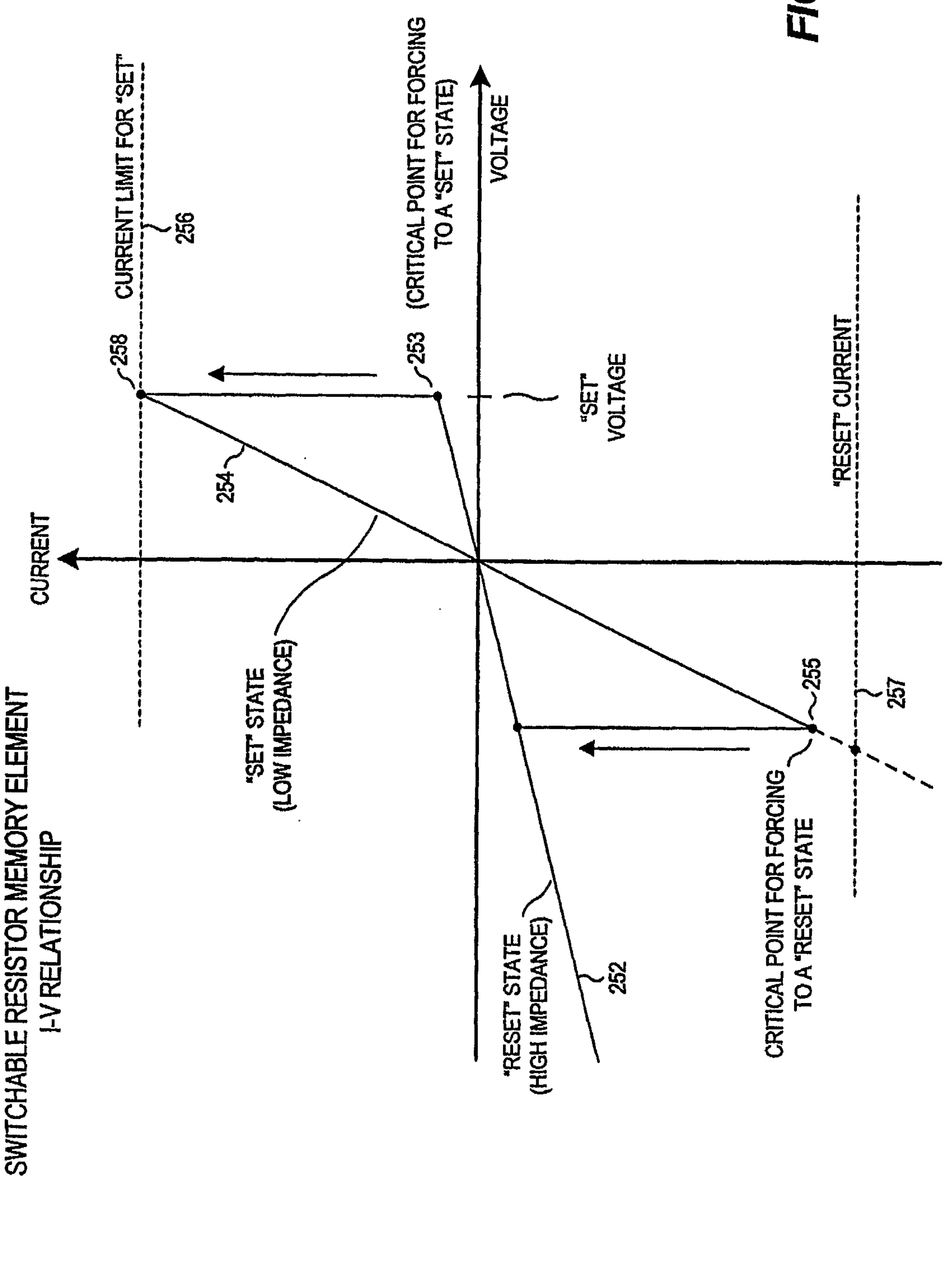
SWITCHABLE RESISTOR MEMORY ELEMENT
I-V RELATIONSHIP
CURRENT
VOLTAGE
CURRENT LIMIT FOR "SET"
256
258
253
(CRITICAL POINT FOR FORCING TO A "SET" STATE)
"SET" VOLTAGE
254
"SET" STATE (LOW IMPEDANCE)
"RESET" CURRENT
255
257
CRITICAL POINT FOR FORCING TO A "RESET" STATE
"RESET" STATE (HIGH IMPEDANCE)
252

FIG. 3

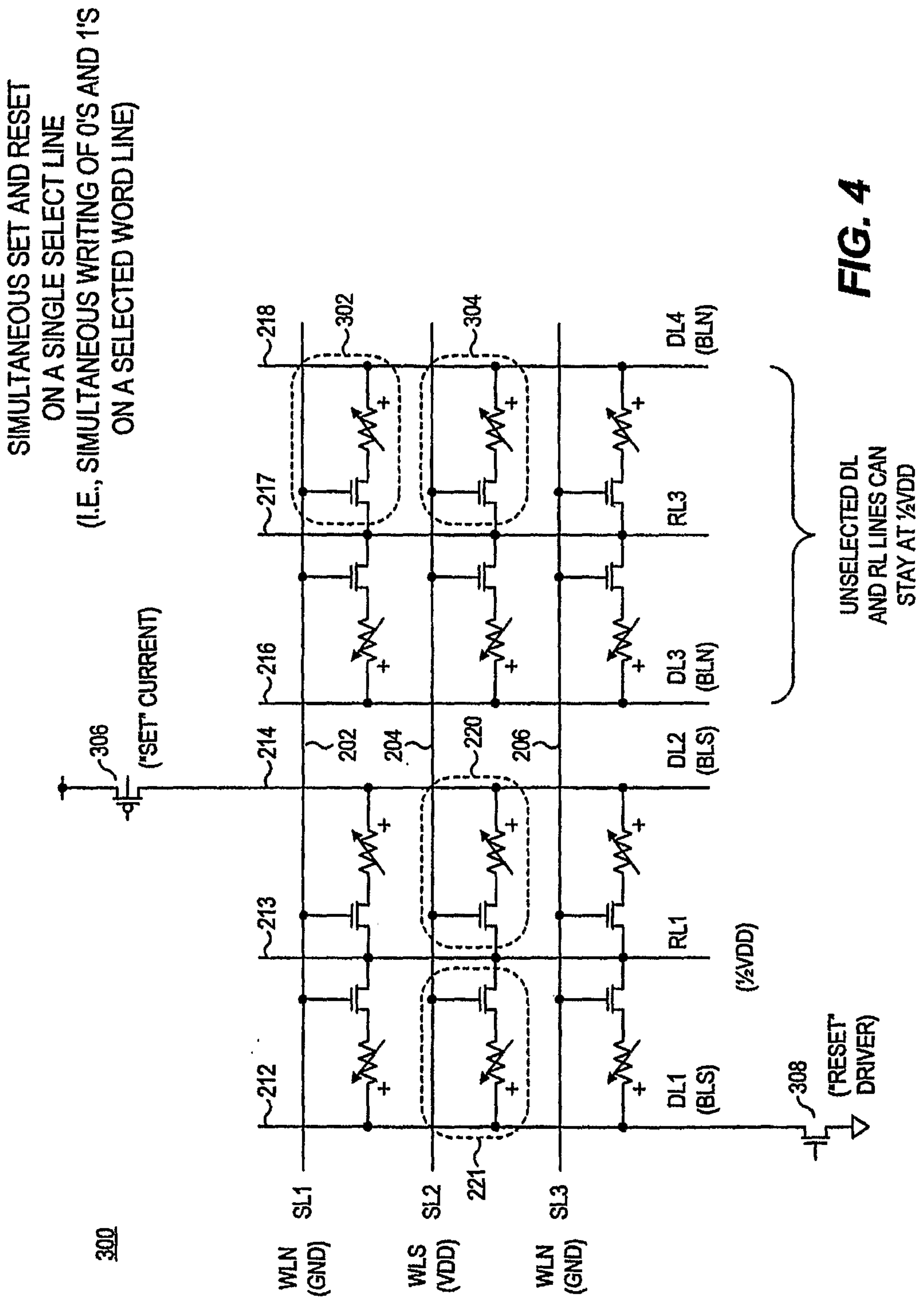
SIMULTANEOUS SET AND RESET
ON A SINGLE SELECT LINE
(I.E., SIMULTANEOUS WRITING OF 0'S AND 1'S
ON A SELECTED WORD LINE)
300
306
("SET" CURRENT)
212
213
214
216
217
218
202
204
206
220
221
302
304
WLN (GND) SL1
WLS (VDD) SL2
WLN (GND) SL3
DL1 (BLS)
RL1
(½VDD)
DL2 (BLS)
DL3 (BLN)
RL3
DL4 (BLN)
308
("RESET" DRIVER)
UNSELECTED DL
AND RL LINES CAN
STAY AT ½VDD

FIG. 4

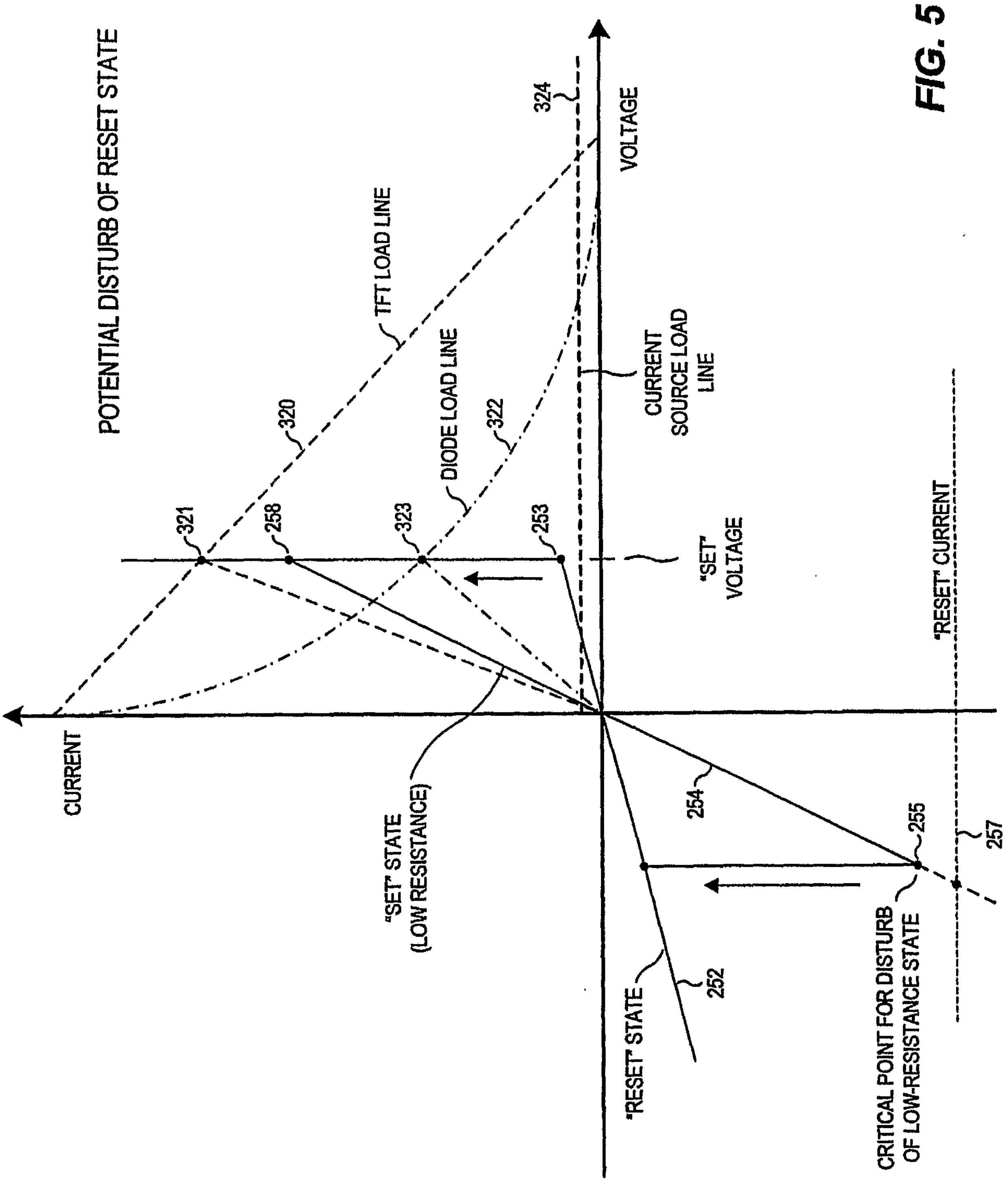
POTENTIAL DISTURB OF RESET STATE
TFT LOAD LINE
DIODE LOAD LINE
VOLTAGE
CURRENT SOURCE LOAD LINE
CURRENT
"SET" VOLTAGE
"RESET" CURRENT
"SET" STATE (LOW RESISTANCE)
"RESET" STATE
CRITICAL POINT FOR DISTURB OF LOW-RESISTANCE STATE
320
321
322
323
324
252
253
254
255
257
258

FIG. 5

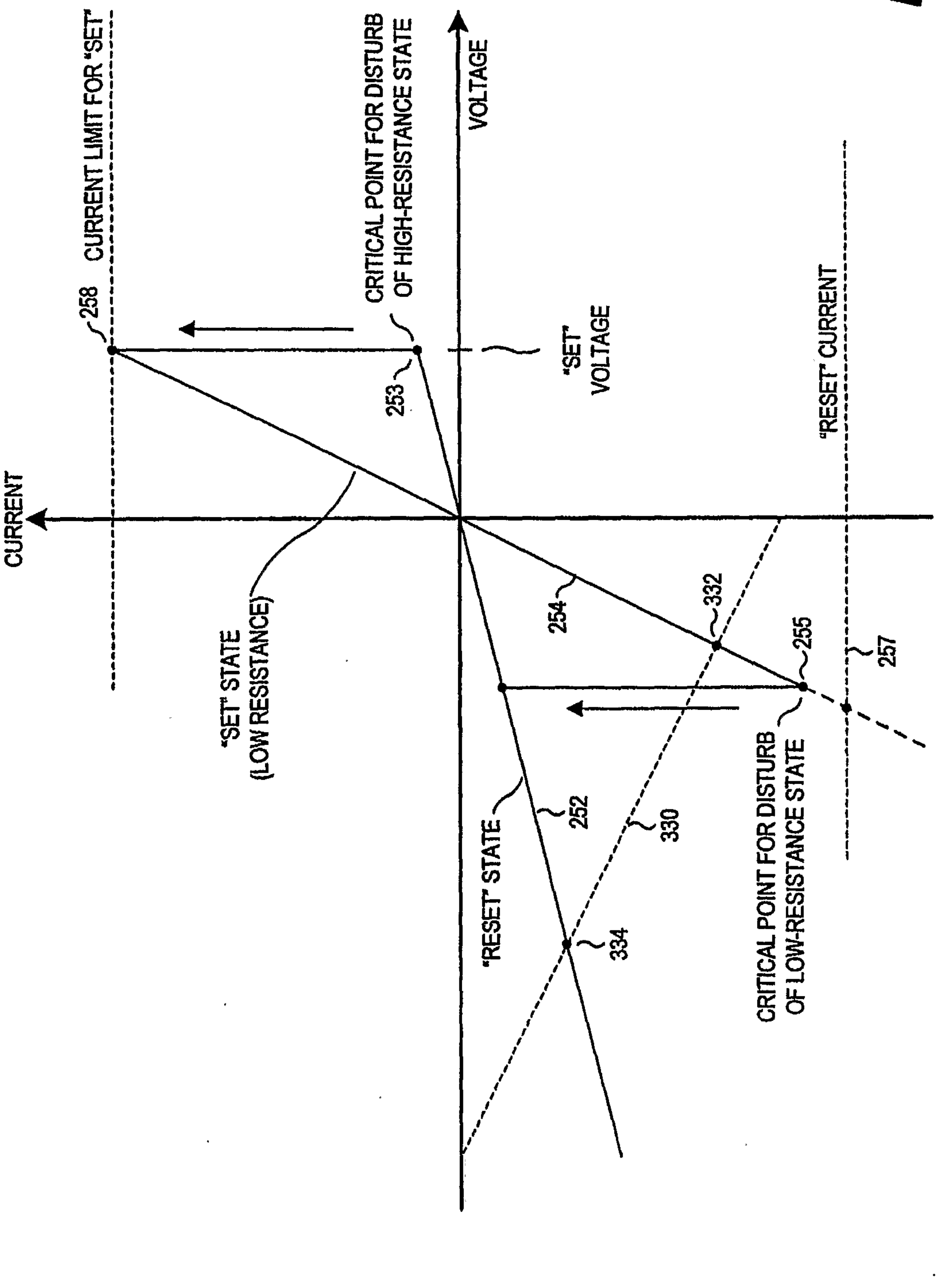
CURRENT LIMIT FOR "SET"
CRITICAL POINT FOR DISTURB OF HIGH-RESISTANCE STATE
VOLTAGE
258
253
"SET" VOLTAGE
CURRENT
"SET" STATE (LOW RESISTANCE)
"RESET" CURRENT
254
332
255
257
"RESET" STATE
252
330
334
CRITICAL POINT FOR DISTURB OF LOW-RESISTANCE STATE

FIG. 6

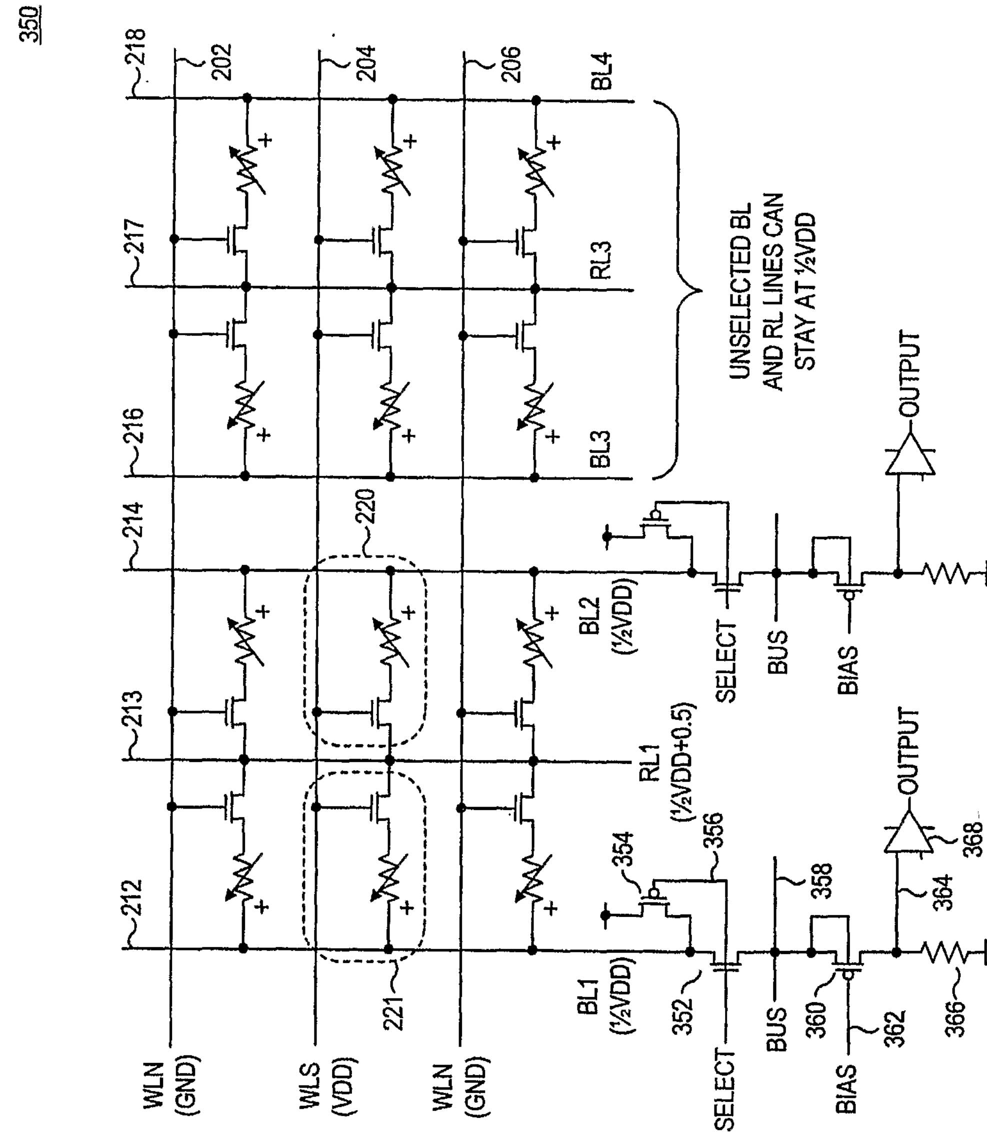
350
WLN (GND)
WLS (VDD)
WLN (GND)
202
204
206
212
213
214
216
217
218
220
221
BL1 (½VDD)
RL1 (½VDD+0.5)
BL2 (½VDD)
BL3
RL3
BL4
UNSELECTED BL AND RL LINES CAN STAY AT ½VDD
SELECT
BUS
BIAS
OUTPUT
SELECT
BUS
BIAS
OUTPUT
352
354
356
358
360
362
364
366
368

FIG. 7

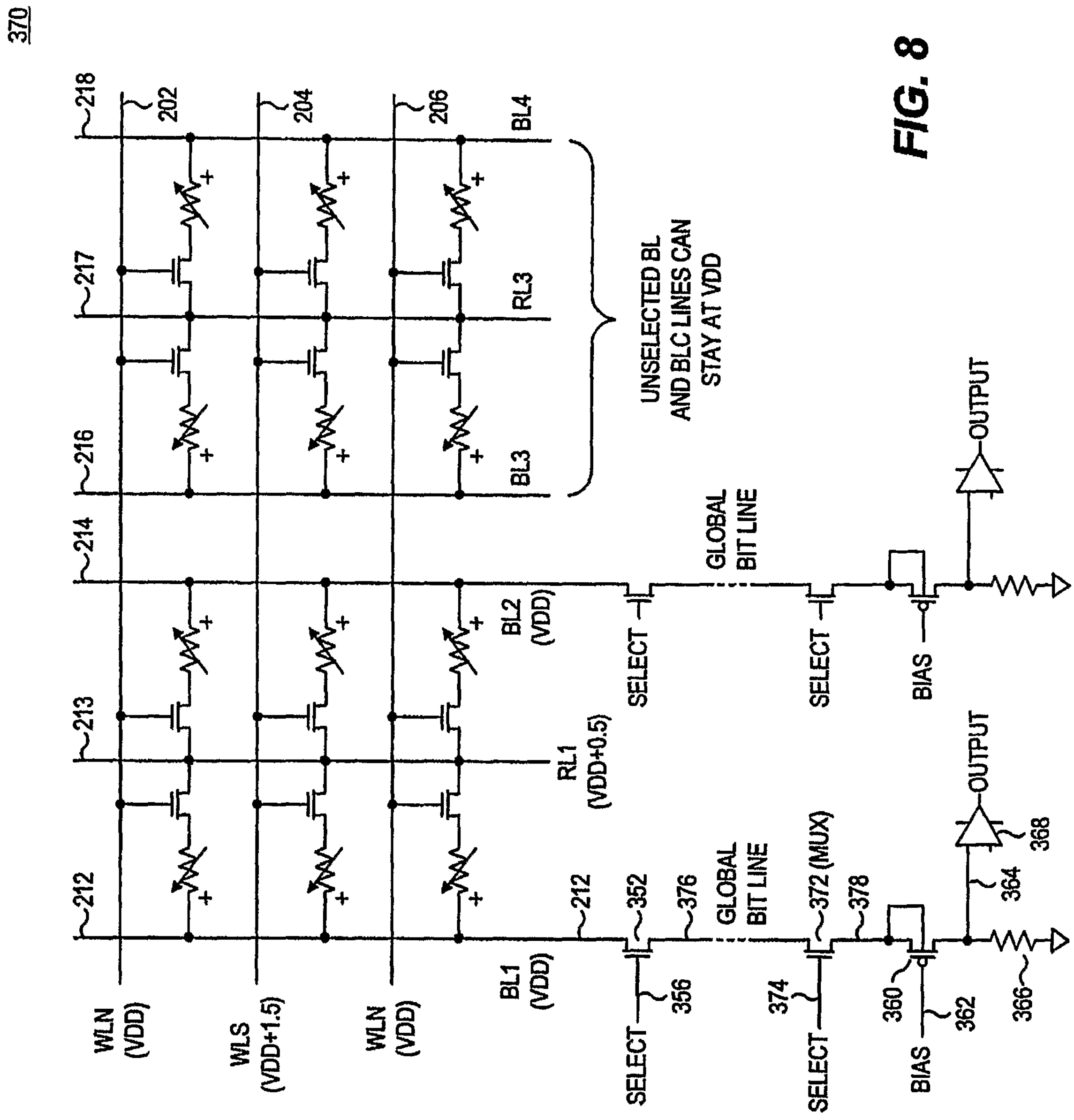
370
218
202
204
206
BL4
217
RL3
216
BL3
UNSELECTED BL
AND BLC LINES CAN
STAY AT VDD
214
GLOBAL
BIT LINE
OUTPUT
BL2
(VDD)
SELECT
SELECT
BIAS
213
RL1
(VDD+0.5)
212
WLN
(VDD)
WLS
(VDD+1.5)
WLN
(VDD)
BL1
(VDD)
212
352
376
GLOBAL
BIT LINE
372 (MUX)
378
364
368
OUTPUT
SELECT
356
374
SELECT
360
BIAS
362
366

FIG. 8

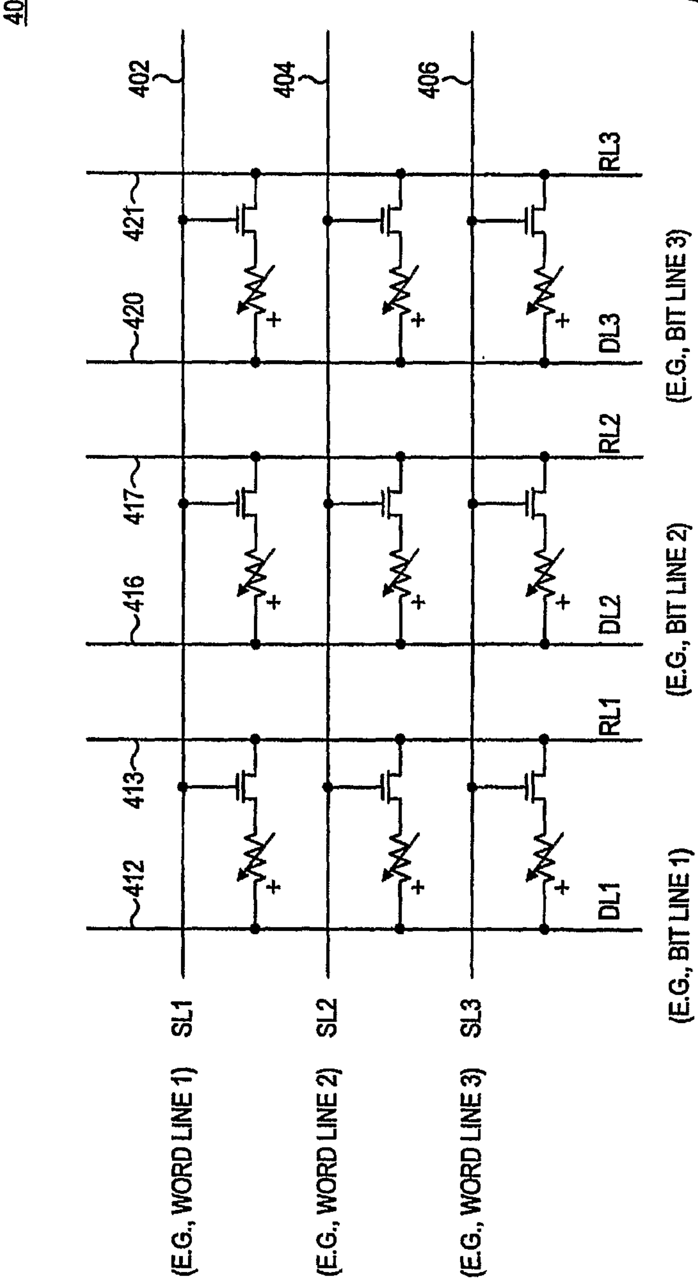
400
402
404
406
421
420
417
416
413
412
RL3
DL3
RL2
DL2
RL1
DL1
(E.G., BIT LINE 3)
(E.G., BIT LINE 2)
(E.G., BIT LINE 1)
SL1
SL2
SL3
(E.G., WORD LINE 1)
(E.G., WORD LINE 2)
(E.G., WORD LINE 3)

FIG. 9

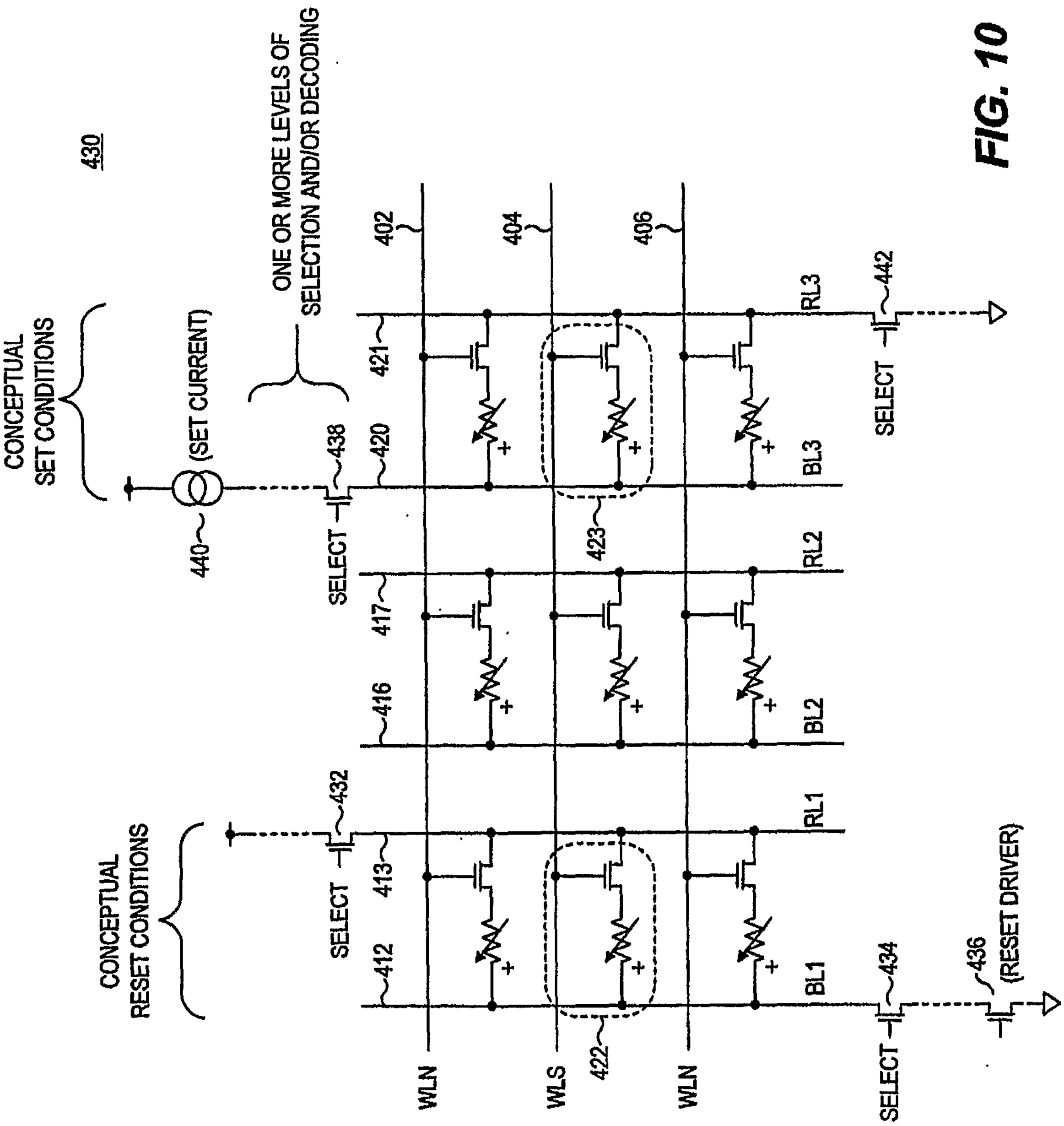
430
CONCEPTUAL SET CONDITIONS
(SET CURRENT)
440
ONE OR MORE LEVELS OF SELECTION AND/OR DECODING
CONCEPTUAL RESET CONDITIONS
SELECT
438
432
434
442
436
(RESET DRIVER)
402
404
406
412
413
416
417
420
421
422
423
WLN
WLS
WLN
BL1
RL1
BL2
RL2
BL3
RL3

FIG. 10

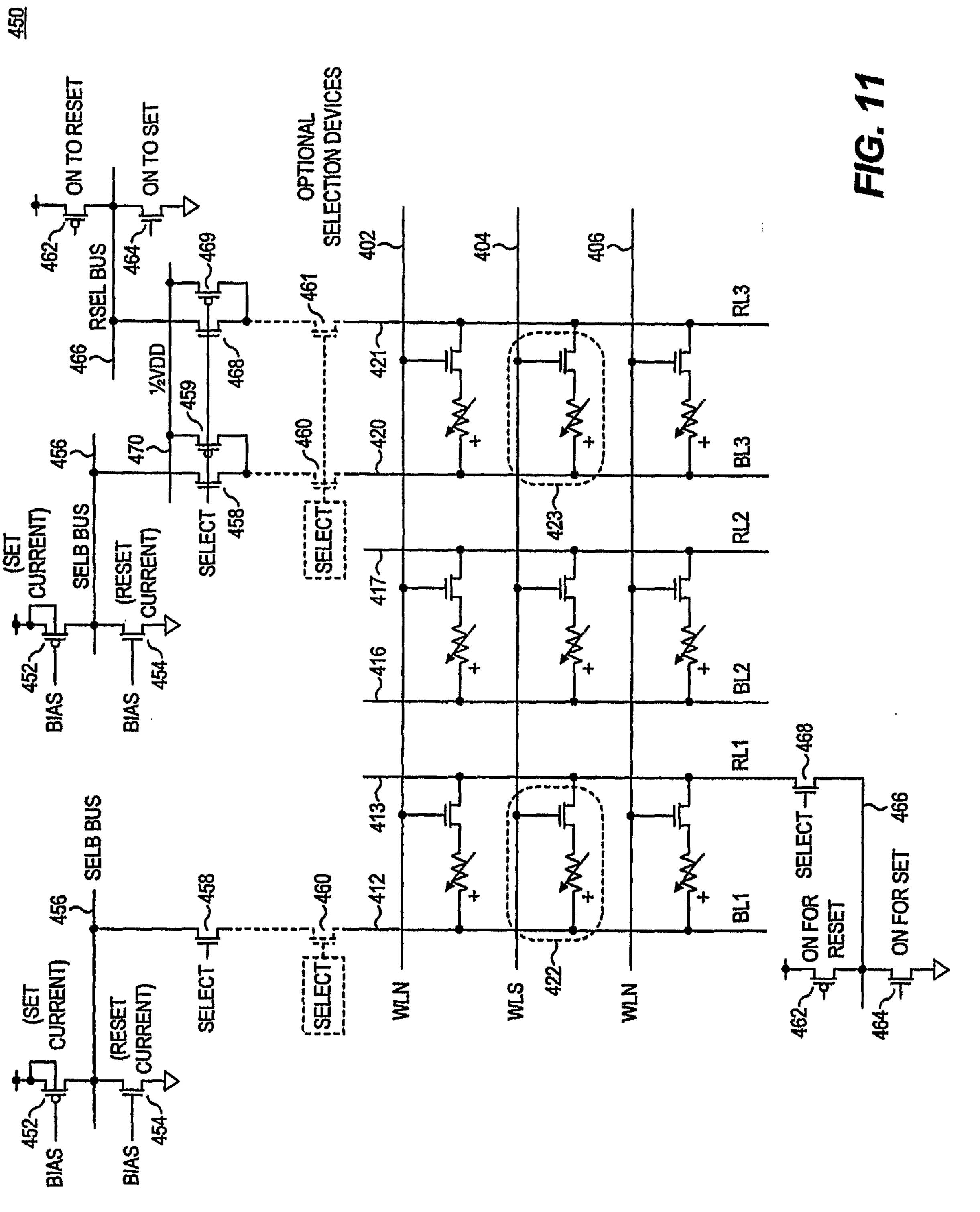
450
ON TO RESET
ON TO SET
462
464
RSEL BUS
466
OPTIONAL SELECTION DEVICES
469
461
468
½VDD
459
470
456
460
SELECT
458
(SET CURRENT)
SELB BUS
(RESET CURRENT)
BIAS
452
454
402
404
406
421
420
417
416
413
412
423
422
RL3
BL3
RL2
BL2
RL1
BL1
WLN
WLS
ON FOR RESET
ON FOR SET

FIG. 11

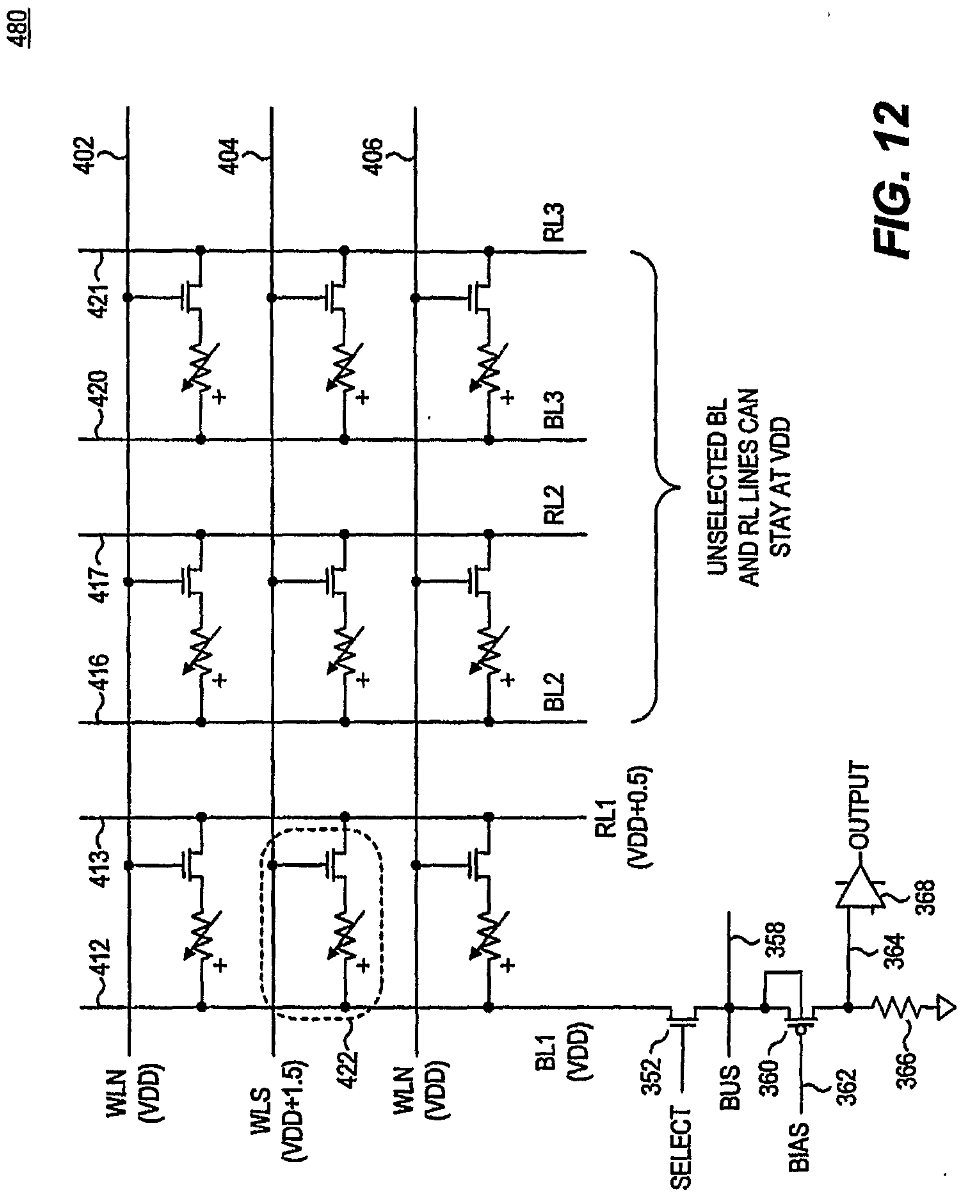
480
402
404
406
421
420
417
416
413
412
422
RL3
BL3
RL2
BL2
RL1
(VDD+0.5)
BL1
(VDD)
WLN
(VDD)
WLS
(VDD+1.5)
WLN
(VDD)
UNSELECTED BL
AND RL LINES CAN
STAY AT VDD
SELECT
352
BUS
358
360
BIAS
362
364
366
368
OUTPUT

FIG. 12

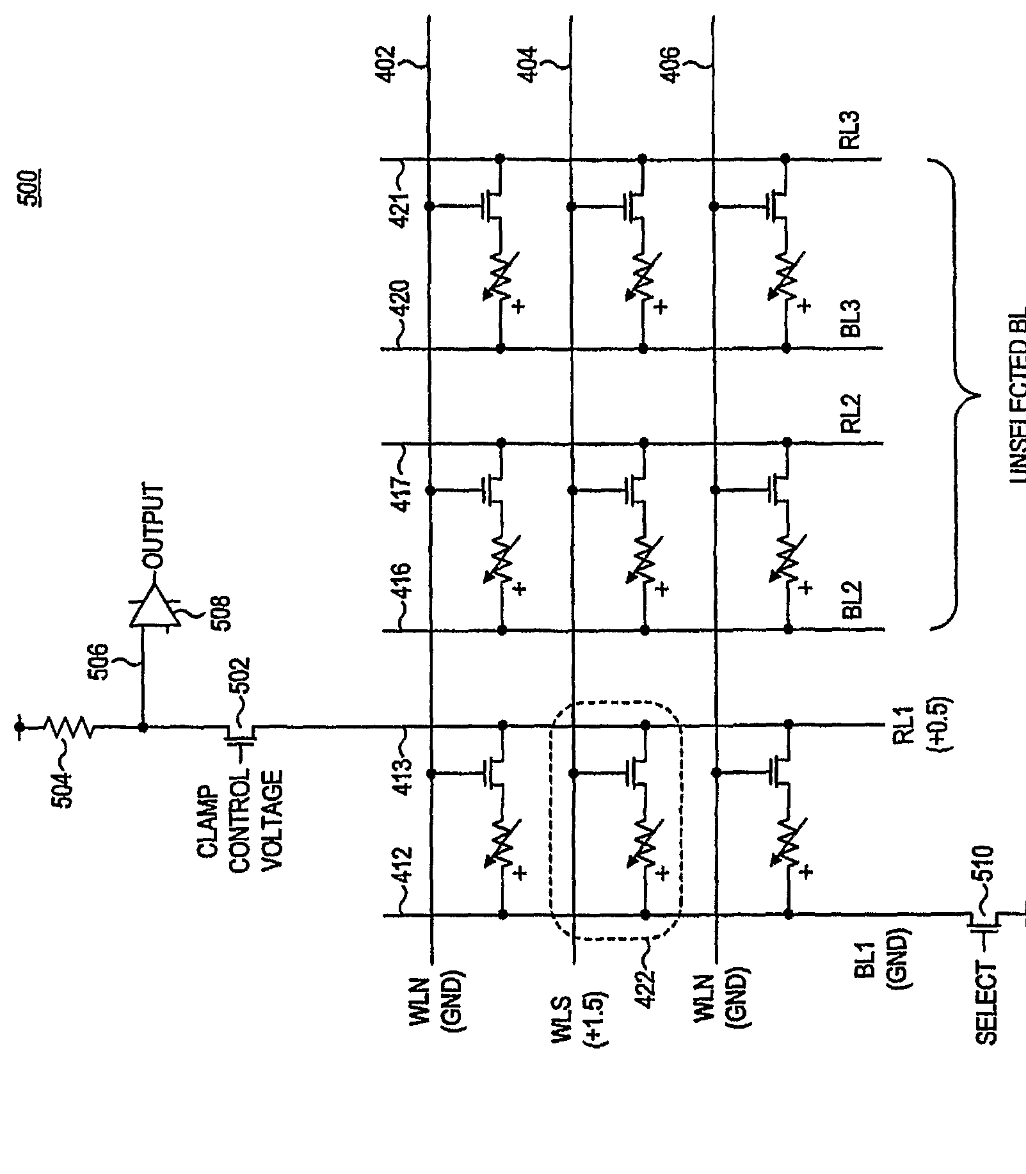
500
504
506
508
OUTPUT
502
CLAMP CONTROL VOLTAGE
402
404
406
412
413
416
417
420
421
422
WLN (GND)
WLS (+1.5)
WLN (GND)
BL1 (GND)
RL1 (+0.5)
BL2
RL2
BL3
RL3
SELECT
510
UNSELECTED BL AND RL LINES CAN STAY AT GND

FIG. 13

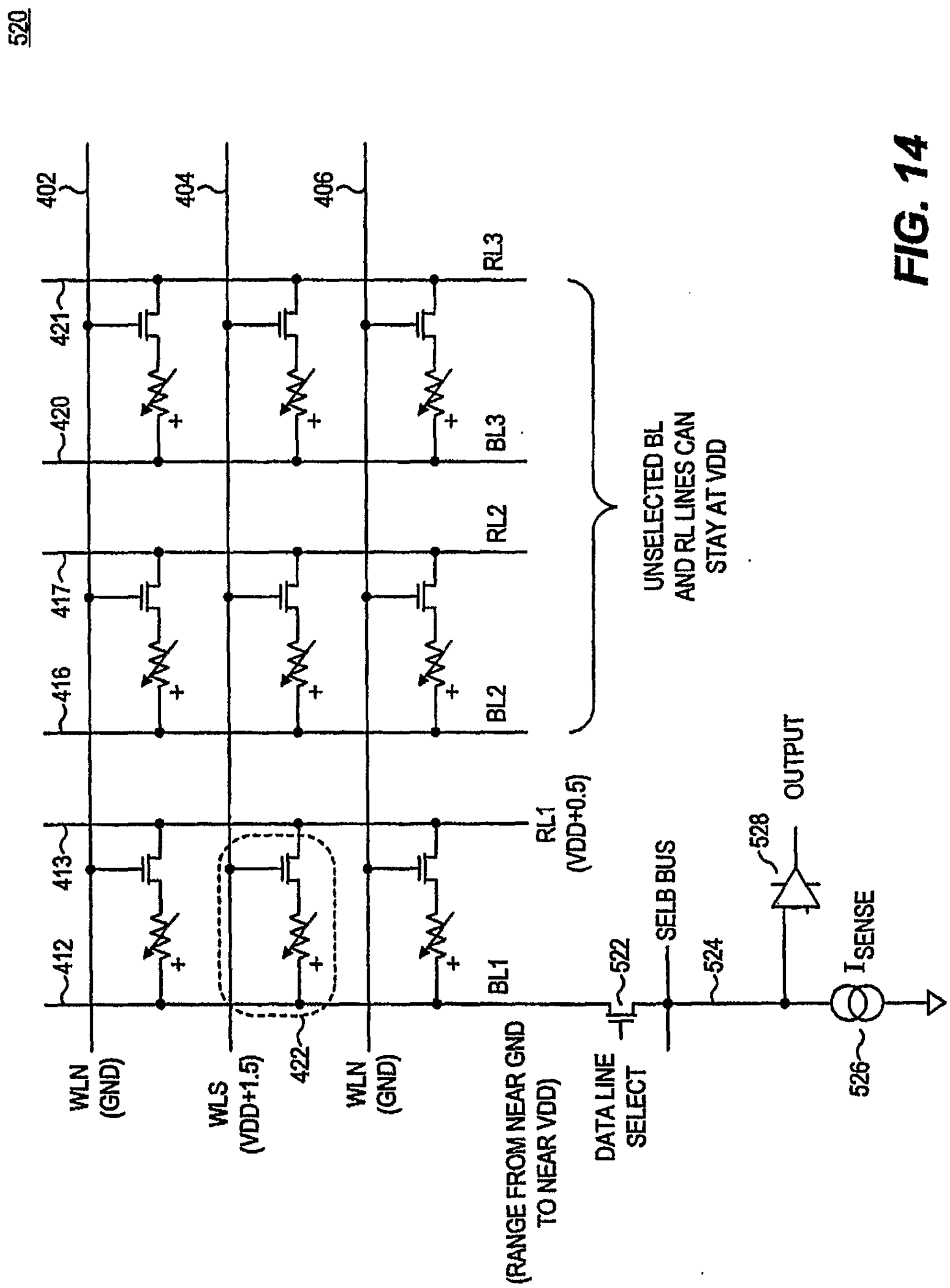
520
402
404
406
421
420
417
416
413
412
422
RL3
BL3
RL2
BL2
RL1
(VDD+0.5)
BL1
UNSELECTED BL
AND RL LINES CAN
STAY AT VDD
WLN
(GND)
WLS
(VDD+1.5)
WLN
(GND)
(RANGE FROM NEAR GND
TO NEAR VDD)
DATA LINE
SELECT
522
SELB BUS
524
528
OUTPUT
526
I_{SENSE}

FIG. 14

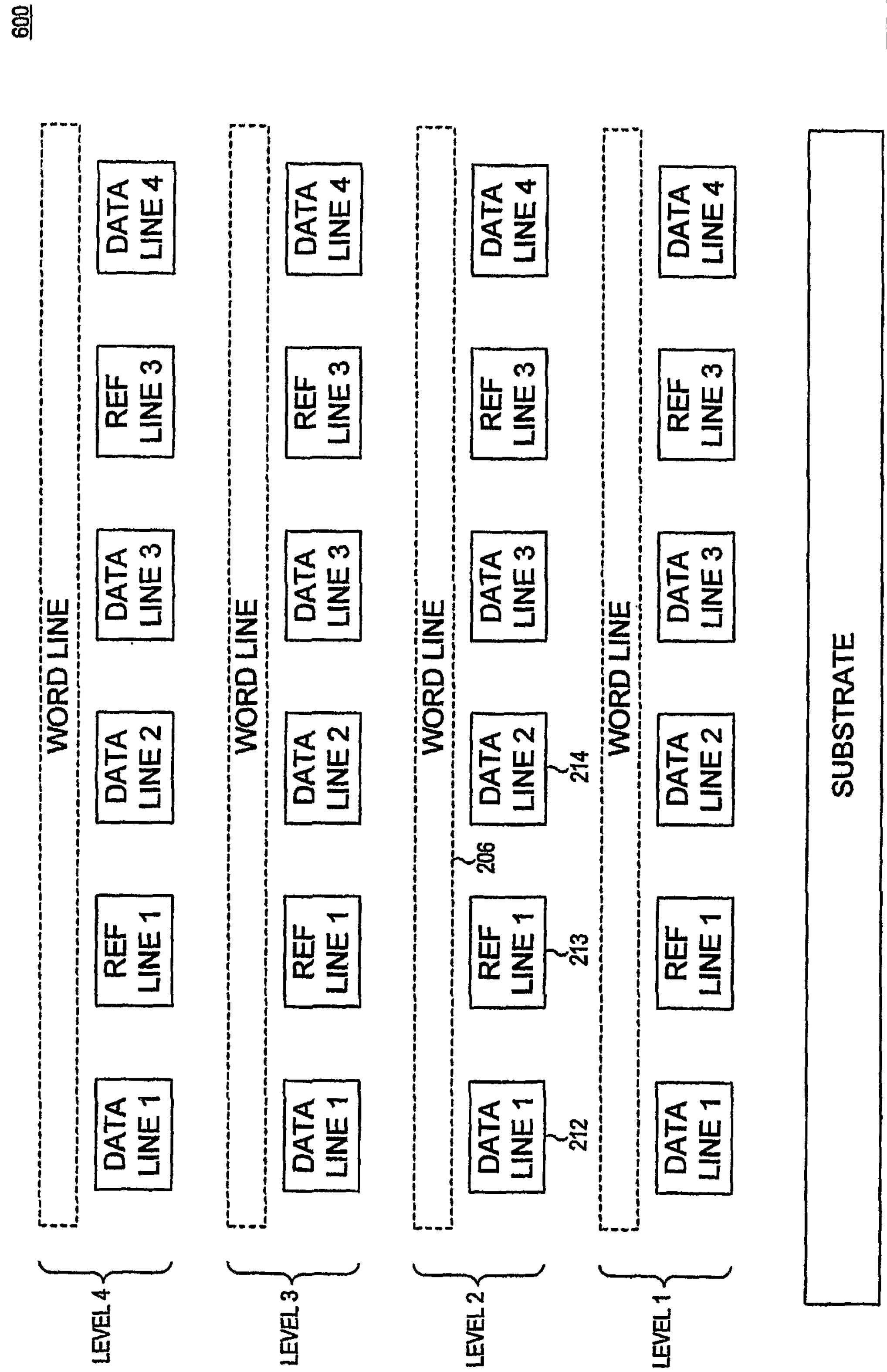
600
WORD LINE
DATA LINE 1
REF LINE 1
DATA LINE 2
DATA LINE 3
REF LINE 3
DATA LINE 4
LEVEL 4
LEVEL 3
LEVEL 2
LEVEL 1
212
213
206
214
SUBSTRATE

FIG. 15

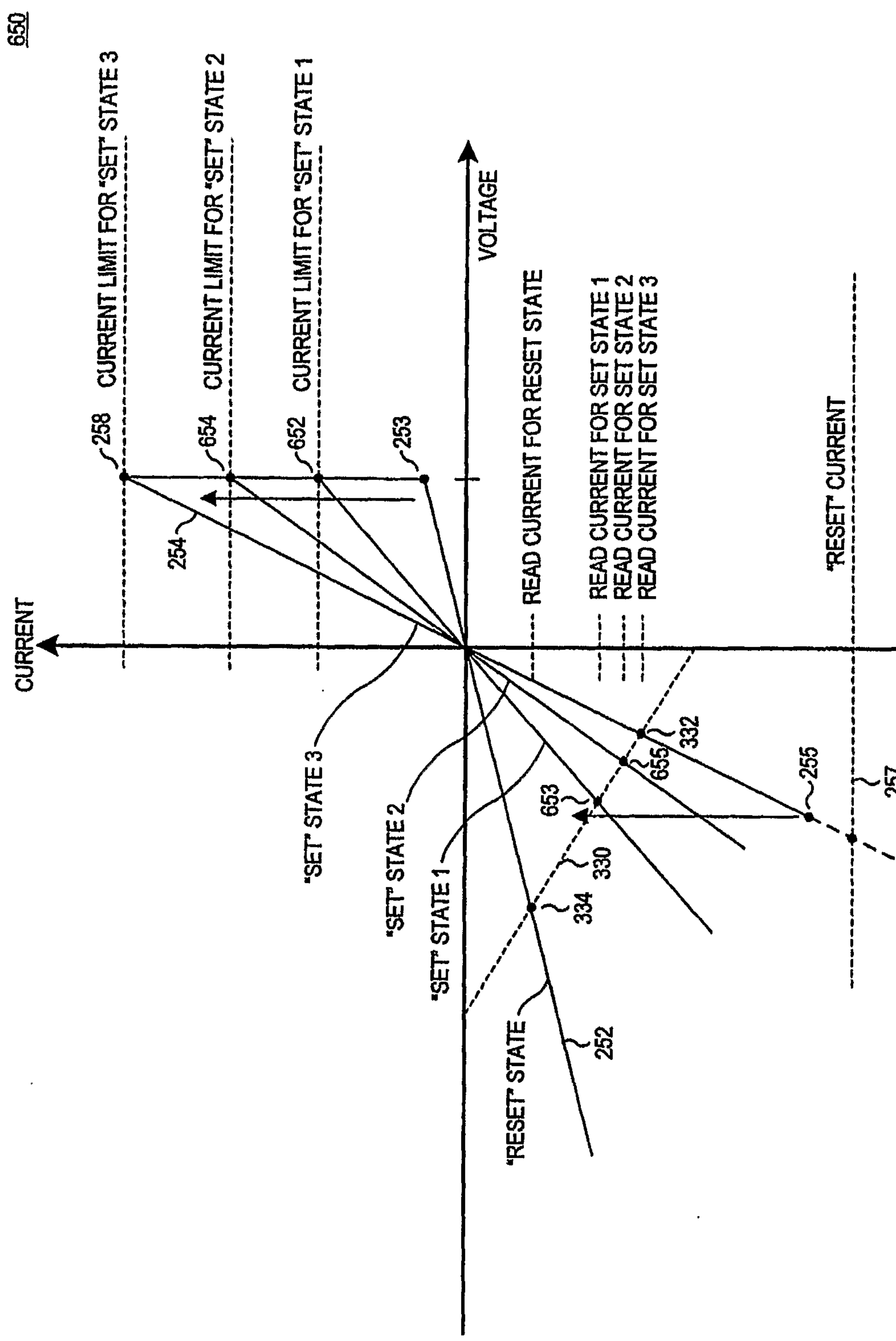
650
CURRENT
VOLTAGE
CURRENT LIMIT FOR "SET" STATE 3
CURRENT LIMIT FOR "SET" STATE 2
CURRENT LIMIT FOR "SET" STATE 1
READ CURRENT FOR RESET STATE
READ CURRENT FOR SET STATE 1
READ CURRENT FOR SET STATE 2
READ CURRENT FOR SET STATE 3
"RESET" CURRENT
258
654
652
253
254
"SET" STATE 3
"SET" STATE 2
"SET" STATE 1
"RESET" STATE
252
334
330
653
655
332
255
257

FIG. 16