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(56) Documents cited **GB 1480423**
(58) Field of search **G4N H4D**
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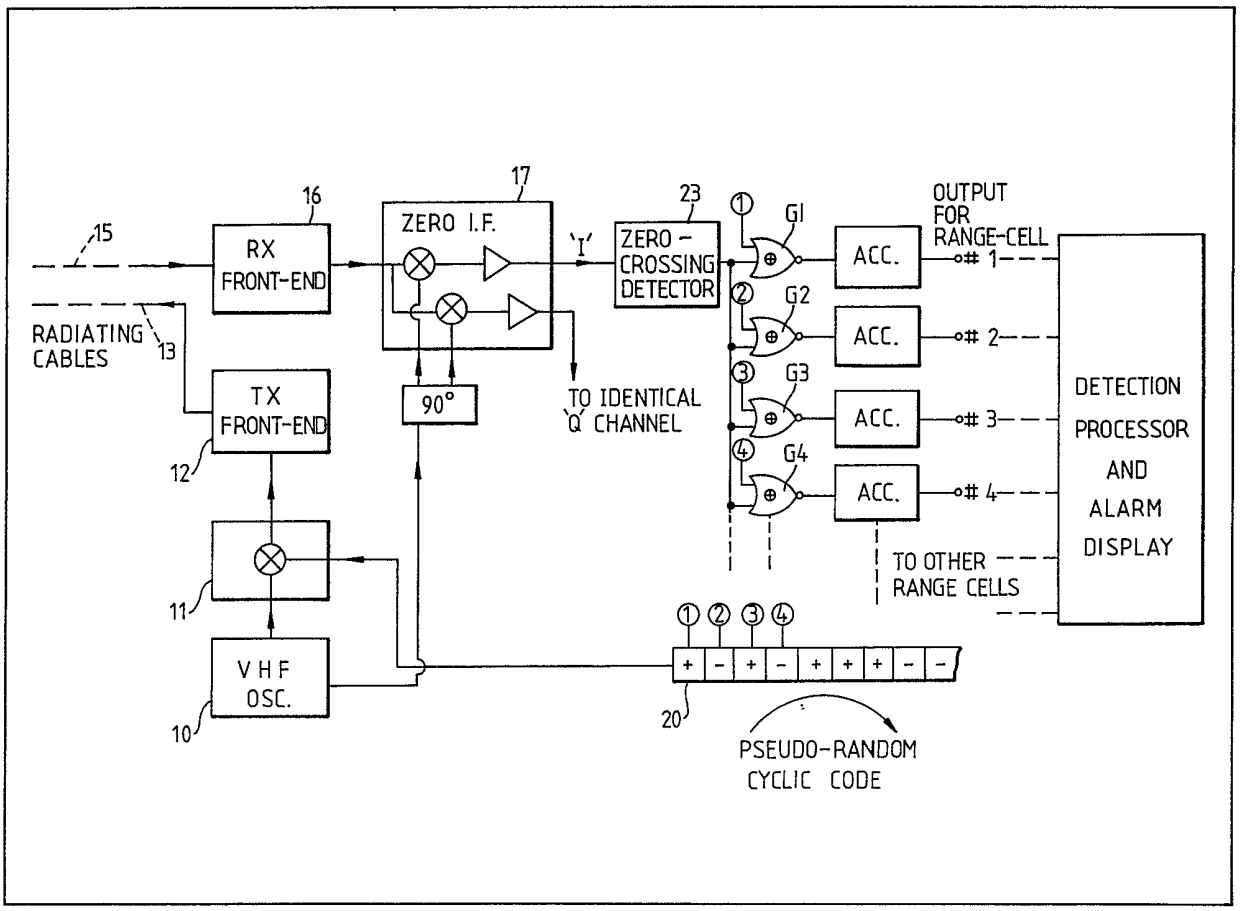
(54) **Radar or sonar system**

(57) An intruder detector system employing Doppler radar consists of an encoder (11) for modulating r.f. pulses with a cyclic pulse code, the code being cycled at a frequency equal to the r.f. pulse frequency and the pulses being modulated on a VHF carrier for transmission along one of a pair of parallel radiating cables. The received signal from the second cable is demodulated and digitised by a zero crossing detector (23) functioning as a one-bit analogue to digital converter. A bank of exclusive - OR gates (G1 etc.) functioning as one-bit correlators then simultaneously correlate each successive bit of the digitised signal with the values of the respective bits in each fixed position of the transmitted code sequence.



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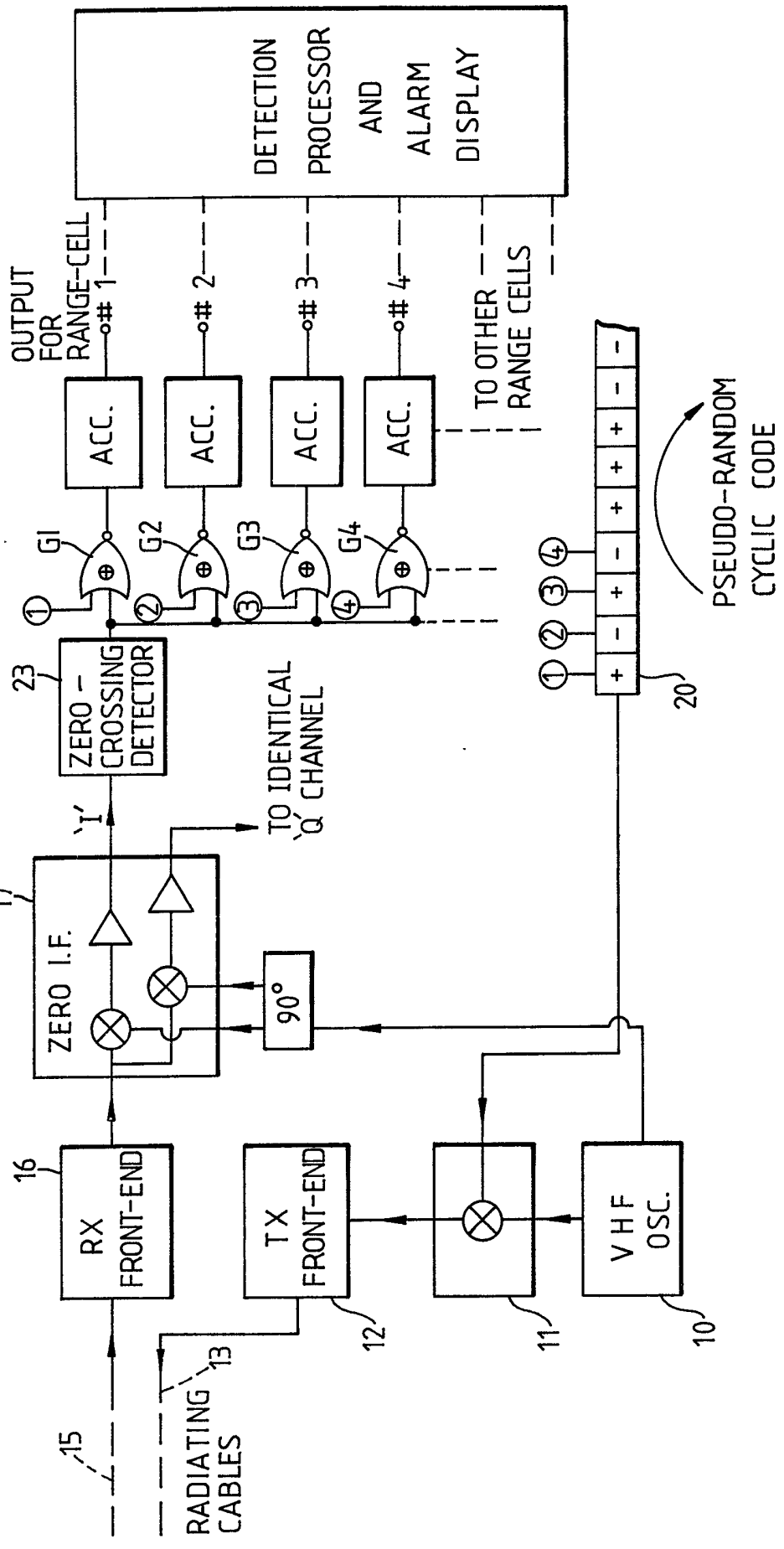
The drawing(s) originally filed was/were informal and the print here reproduced is taken from a later filed formal copy.


DETECTION PROCESSOR AND ALARM DISPLAY
OUTPUT FOR RANGE-CELL # 1
2
3
4
TO OTHER RANGE CELLS
ACC.
G1
G2
G3
G4
PSEUDO-RANDOM CYCLIC CODE
20
23
ZERO - CROSSING DETECTOR
TO IDENTICAL 'Q' CHANNEL
'I'
17
ZERO I.F.
90°
16
RX FRONT-END
TX FRONT-END
12
11
VHF OSC.
10
15
RADIATING CABLES
13

SPECIFICATION

Radar or sonar system

This invention relates to a radar or sonar system such as may be used in, inter alia, intruder detection systems for guarding the perimeter of an area.

In our copending application number 8013259 we describe an intruder detection system in which RF pulses are modulated on a VHF carrier, each RF pulse being modulated with a pseudo-random pulse code sequence and the carrier being transmitted along a length of radiating cable. Signals received from the cable, for example, along a second length of cable disposed substantially parallel to the first length of cable, are correlated with replicas of the code sequence, the replicas being generated under control of a range delay circuit so that the presence of a return signal within a given range cell is detected. The range delay circuit may be arranged so that either a sequence of range cells is cyclically monitored, or a set of parallel code mixers can be used for different range cells so that the signals from all range cells are processed simultaneously.

An object of the present invention is to reduce the complexity of the receiving and processing circuits in such a system, while still maintaining simultaneous correlation of all range cells.

According to the present invention there is provided a radar or sonar system comprising an encoder for modulating a carrier transmission with a cyclic pulse code, the code being cycled at a frequency equal to the pulse repetition frequency, a 1-bit analogue-to-digital converter for digitising the received pulses, and a plurality of 1-bit correlators for simultaneously correlating each successive bit of the digitised signal with the values of the respective bits in each expected position of the received code sequence.

In a preferred embodiment of the invention the 1-bit A to D converter comprises a zero crossing detector, and each 1-bit correlator comprises an exclusive-OR logic gate.

By way of example only, an intruder detection system embodying the invention will now be described with reference to the accompanying drawing in which the sole Figure is a block diagram of the detection system.

The basic operation of the system is described more fully in our aforesaid copending application 8013259. Briefly, a VHF signal source 10 is modulated by RF pulses containing a psuedo-random pulse code sequence in a spread spectrum modulator 11, and the resulting signal is fed to transmitter 12 for transmission along a first radiating cable 13. Return signals are transmitted back along a second length of cable 15 and received at the receiver front end 16. The received signals are mixed with quadrature components of the transmitted VHF signal in a zero intermediate frequency unit 17 to derive sequences of D.C. pulses for I and Q channel processing.

From this point, the circuit shown in the accompanying drawing differs from that described in application 8013259. The psuedo-random cyclic code is stored in a cyclic shift register 20 and is continuously rotated at a period equal to the desired pulse repetition frequency of the system. The output from the shift register 20 is applied to the spread spectrum modulator 11 so that the successive pulses are modulated with a different code for different range cells. The number of range cells covered by the system is therefore equal to the length of the code.

Each stage of the shift register containing one bit of the pseudo-random code is also applied to a first input of a respective gate in a bank of exclusive-OR logic gates G1, G2, G3 etc., these gates being used as 1-bit correlators.

D.C. pulses for each channel are processed separately but, for simplicity, only further processing of the I component is shown, the processing of the Q component being identical. The pulses are fed to a zero crossing detector 23 which functions as a 1-bit analogue-to-digital converter. The output of the detector 23 is fed to the second input of each OR gate so that if, say, the successive bits from the detector match the successive bits appearing at the first input of the gate G3, this will indicate the received pulses have been reflected from a target in the third range cell. The resulting outputs from the gates are applied to respective up-down counters functioning as accumulators. Code chips can thus be integrated not only for the length of the code but also for a number of the RF pulses. This accumulation of pulses prior to subsequent processing in a Fourier transform processor reduces the required size of the processor and leads to higher processing speeds, as more fully described and separately claimed in our copending application No. being filled concurrently herewith.

The outputs of the various accumulators are finally scanned by the detection processor to extract the information from the different range cells, and actuate an alarm display whenever a moving target is detected.

In this specification, a 1-bit signal digital system is defined as one in which a logical 1 represents a positive input and a logical 0 represents a negative input, or vice-versa.

It can be shown that the dynamic range of a digital system is not limited to that of the analogue-to-digital conversion process in the system. With Gaussian noise present, the digital system is able to discern signals and signal changes that are smaller than the quantisation step, as long as the standard deviation of the noise is significantly larger than the quantisation step, and that sufficient integration is performed on the signal samples to lift the signal above the thermal and quantisation noise. Such criteria can be applied to a 1-bit digital system.

CLAIMS

1. A radar or sonar system comprising an encoder for modulating a carrier transmission with a cyclic pulse code, the code being cycled at a frequency equal to the pulse repetition frequency, a 1-bit analogue-to-digital converter for digitising the received pulses, and a plurality of 1-bit correlators for simultaneously correlating each successive bit of the

digitised signal with the values of the respective bits in each expected position of the received code sequence.

2. A system according to Claim 1 in which the 1-bit A to D converter comprises a zero crossing detector.

3. A system according to Claim 1 or Claim 2 in which each 1-bit correlator comprises an exclusive-OR gate.

4. A system according to any one of the preceding claims further comprising means for accumulating the respective outputs of the 1-bit correlators for the length of the code sequence.

5. A system according to Claim 4 in which each accumulator further accumulates the outputs of the respective 1-bit correlators for a predetermined number of RF pulses.

6. A system according to Claim 4 or Claim 5 in which each accumulator comprises an up-down counter connected to receive the output of the respective 1-bit correlator.

7. A system according to any one of the preceding claims in which the pulse code sequence is modulated on a carrier for transmission and in which the received carrier is demodulated in a zero intermediate frequency unit to recover the pulse code sequence.

8. A radar or sonar system according to Claim 1 and substantially as herein described with reference to the accompanying drawing.

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