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PATENT REQUEST: STANDARD PATENT/PATENT OF ADDITION

We, being the person(s) identified below as the Applicant, request the grant of a patent to the person identified below as the Nominated Person, for an invention described in the accompanying standard complete specification.

Full application details follow.

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[54] Invention Title: METHOD AND APPARATUS FOR CONTROLLING  
AN INVERTER

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BASIC CONVENTION APPLICATION(S) DETAILS

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Drawing number recommended to accompany the abstract:

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KABUSHIKI KAISHA TOSHIBA

By: 

Registered Patent Attorney

# DECLARATION IN SUPPORT OF A CONVENTION APPLICATION FOR A PATENT OR PATENT OF ADDITION

(1) Here insert (in full) Name of Company. In support of the Convention Application made by<sup>(1)</sup>.....  
**Kabushiki Kaisha Toshiba**.....

(2) Here insert title of Invention. for a patent.....for an invention entitled<sup>(2)</sup>.....  
**"Method & Apparatus for Controlling an Inverter"**.....

(3) Here insert Name and Address of Company Official authorised to make declaration. I,<sup>(3)</sup> **Kensuke NORICHIKA**.....  
of **1-1-1, Shibaura, Minato-ku, Tokyo, Japan**.....

do solemnly and sincerely declare as follows:

1. I am authorised by<sup>(1)</sup>.....**Kabushiki Kaisha Toshiba**.....

.....the applicant for the patent.....to make this declaration on its behalf.

2. The basic application as defined by Section 141 of the Act was.....

made in<sup>(4)</sup>.....**Japan**.....

on the.....**24th**.....day of.....**January**.....**1989**, by.....

.....**Kabushiki Kaisha Toshiba**.....

on the.....**2nd**.....day of.....**June**.....**1989**, by.....

.....**Kabushiki Kaisha Toshiba**.....

on the.....**14th**.....day of.....**September**.....**1992**, by.....

.....**Kabushiki Kaisha Toshiba**.....

<sup>3,(5)</sup> **Satoshi Miyazaki, Ben-Brahim Lazhar, & Ryoichi Kurosawa**  
all at C/o Intellectual Property Division, Toshiba Corporation,  
**1-1-1 Shibaura, Minato-ku, Tokyo, Japan**.....

.....the actual inventor of the invention, and the facts upon which<sup>(1)</sup>.....

.....is entitled to make the application, are as follows:

The said<sup>(1)</sup>.....**Kabushiki Kaisha Toshiba**.....

is the assignee of the said<sup>(6)</sup>.....**Satoshi Miyazaki, Ben-Brahim and**.....

.....**Ryoichi Kurosawa**.....

4. The basic application referred to in paragraph 2 of this Declaration was.....the first application made in a Convention country in respect of the invention the subject of the application.

DECLARED at.....**Tokyo, Japan**.....

this.....**2nd**.....day of.....**April**.....**1993**.....

(7) Signature.

To:

(7) *Kensuke Norichika*  
**Kensuke NORICHIKA, General Manager,**  
**Intellectual Property Division**



(12) PATENT ABRIDGMENT (11) Document No. AU-B-31956/93  
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(54) Title  
METHOD AND APPARATUS FOR CONTROLLING AN INVERTER

International Patent Classification(s)

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(56) Prior Art Documents  
AU 589036 77750/87 H02M 7/537 G05F 1/455  
AU 529601 55674/80 H02M 7/537 5/458 1/12  
AU 521684 40027/78 H02M 7/515 1/06

(57) Claim

1. A method of controlling an inverter generating a plurality of phase voltages and a corresponding plurality of line voltages defined as the differences between said phase voltages, said method comprising the steps of:

generating voltage reference signals having <sup>corresponding</sup> ~~plural~~ phases;

determining one of (1) a normal mode, (2) a rectangle mode and (3) a zero correction mode of operation of said inverter in response to values and polarities of said voltage references;

using the voltage references during the normal mode as a reference value for controlling said inverter; and

in at least one of said determined rectangle and zero correction modes, converting the voltage reference signals to converted voltage reference signals in accordance with a preset algorithm such that each phase voltage based on said converted voltage reference signals

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has a controlled pulse width greater than or equal to a minimum ON-pulse width or a minimum OFF-pulse width ~~predetermined minimum width~~ and such that the resulting line voltages do not change when compared to said line voltages generated using said voltage reference signals.

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AUSTRALIAPatents Act 1990COMPLETE SPECIFICATION  
FOR A STANDARD PATENT

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RYOICHI KUROSAWAAddress for Service: CULLEN & CO.,  
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240 Queen Street,  
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Australia.Invention Title: METHOD AND APPARATUS FOR CONTROLLING  
AN INVERTERThe following statement is a full description of this invention,  
including the best method of performing it known to us:

METHOD AND APPARATUS FOR CONTROLLING  
AN INVERTER

Background of the Invention

Field of the Invention

5           The invention relates to a control apparatus applied to a pulse width modulation (PWM) control inverter for converting DC power into AC power, a PWM control converter for converting AC power into DC power, and the like.

10           Description of the Related Art

          For general background into the subject matter of the invention, reference is made to co-pending German application DE 42 06 263 entitled "Control Device of Neutral Point Clamped Power Inverter Apparatus,"  
15           incorporated herein by reference.

          A pulse width modulation control inverter uses self-quenching type switching elements such as gate turn-off (GTO) thyristors.

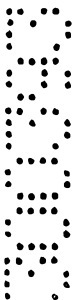
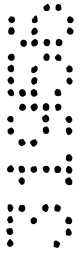
          As shown in Fig. 1, the inverter control apparatus  
20           comprises a controller 300, a comparator 301 and pulse correction circuit 302. The controller 300 outputs a voltage reference signal  $V^*$ . The comparator 301 compares the voltage reference signal  $V^*$  and carrier signals  $V_{CP}$  and  $V_{CN}$ , and outputs an output signal  $V_{CMP}$ . The pulse  
25           correction circuit 302 corrects the output signal  $V_{CMP}$  from the comparator 301, and outputs a gate signal  $V_G$ . These gate signals are used to control the switching elements, e.g., GTOs in the inverter as is well known in the prior art, e.g., Fig. 13.





signals having plural phases; (b) determining one of (1)  
a normal mode, (2) a rectangle mode and (3) a zero  
correction mode of operation of the inverter in response  
to values and polarities of the voltage references; (3)  
5 using the voltage references during the normal mode as a  
reference value for controlling the inverter; and (4) in  
at least one of the determined rectangle and zero  
correction modes, converting the voltage reference  
signals to converted voltage reference signals in  
10 accordance with a preset algorithm such that each phase  
voltage based on the converted voltage reference signals  
has a controlled pulse width greater than or equal to a  
~~minimum ON-pulse width or a minimum OFF-pulse width~~  
~~predetermined minimum width~~ and such that the resulting  
line voltages do not change when compared to the line  
15 voltages generated using the voltage reference signals.

In accordance with another aspect of the invention,  
there is provided a method of controlling an inverter  
generating a plurality of phase voltages and a  
corresponding plurality of line voltages defined as the  
20 differences between the phase voltages. The method  
comprising the steps of: a) generating voltage references  
signals having a plurality of phases; b) selecting the  
phase of the voltage reference signal which has the most  
positive value; c) converting the selected phase to a  
25 phase of a converted voltage reference signal which has  
one of (1) a preset minimum value which is negative and  
(2) a preset value which is zero; d) converting the other  
phases of the voltage reference signals to converted  
voltage reference signals of the inverter such that the  
30 resulting line voltages do not change when compared to  
the line voltages generated using the voltage reference  
signals; e) selecting the phase of the voltage reference  
signal which has the most negative value; f) converting  
the selected phase to a phase of a converted voltage  
35 reference signal which has one of (1) a preset minimum  
value which is positive and (2) a preset value which is  
zero; g) converting the other phases of the voltage  
reference signals to converted voltage reference signals



of the inverter such that the resulting line voltages do not change when compared to the line voltages generated using the voltage reference signals; and h) switching alternately between steps b)-d) and steps e)-g) to control the inverter.

According to yet another aspect of the invention, there is provided an inverter control apparatus for an inverter generating a plurality of phase voltages and a corresponding plurality of line voltages defined as the differences between the phase voltages. The control apparatus comprising:

a) mode decision means for determining one of (1) a normal mode, (2) a rectangle mode and (3) a zero correction mode in response to values and polarities of voltage reference signals having <sup>corresponding</sup> plural phases; and

b) voltage reference conversion means:

1) operative in the normal mode for outputting the voltage reference signals as converted voltage reference signals which are identical to the voltage reference signals; and

2) operative in the rectangle and zero correction modes for outputting corrected voltage reference signals in response to the voltage reference signals in accordance with an algorithm such that the resulting line voltages do not change when compared to the line voltages generated using the voltage reference signals.

The invention may be further defined with respect to another aspect of the invention as a control apparatus for controlling a neutral point clamped three-phase inverter. The inverter has switching elements and generates a plurality of phase voltages and a corresponding plurality of line voltages. The control apparatus comprising: means for generating voltage reference signals having <sup>corresponding</sup> plural phases; voltage reference conversion means for: (1) converting the voltage reference signals to converted voltage reference signals, the conversion means fixing the value of one of a



corrected voltage reference signal to one of a positive minimum value or a negative minimum value when the width of any of the plurality of phase voltages becomes equal to a minimum value corresponding to a minimum ON pulse width of the switching elements; and (2) converting the other of the voltage references signals such that the resulting line voltages do not change when compared to the line voltages generated using the voltage reference signals.

10 In yet another aspect of the invention, an inverter control apparatus is provided for controlling a neutral point clamped three-phase inverter. The inverter generates a plurality of phase voltages and a corresponding plurality of line voltages. The control apparatus comprising: means for generating voltage reference signals having ~~plural~~<sup>corresponding</sup> phases; first voltage reference conversion means for converting all phases of the voltage reference signals to converted voltage reference signals, all having a positive polarity, such that the resulting line voltages generated from the converted voltage reference signals do not change when compared to the line voltages generated using the voltage reference signals; second voltage reference conversion means for converting all phases of the voltage reference signals to converted voltage reference signals, all having a negative polarity, such that the resulting line voltages generated from the converted voltage reference signals do not change when compared to the line voltages generated using the voltage reference signals; and switching means for alternately controlling the inverter using the first and second voltage reference conversion means.

35 Still in a further aspect, the invention may be defined as an inverter control apparatus for controlling a neutral point clamped three-phase inverter, the inverter generating three phase voltages and a corresponding three line voltages, in which the control apparatus comprises: a) a generator which generates



voltage reference signals having a <sup>corresponding</sup> plurality of phases; b) means for selecting the phase of the voltage reference signal which has the most positive value; c) means for converting the selected phase to a phase of a converted voltage reference signal which has a preset positive maximum value; d) means for converting the other phases of the voltage reference signals to converted voltage reference signals of the inverter such that the resulting line voltages do not change when compared to the line voltages generated using the voltage reference signals; e) means for selecting the phase of the voltage reference signal which has the most negative value; f) means for converting the selected phase to a phase of a converted voltage reference signal which has a preset negative maximum value; g) means for converting the other phases of the voltage reference signals to converted voltage reference signals of the inverter such that the resulting line voltages do not change when compared to the line voltages generated using the voltage reference signals; and h) means for switching alternately between steps b)-d) and steps e)-g) to control the inverter.

Brief Description of the Drawings

The accompanying drawings, which are incorporated in and constitute a part of the specification, illustrate presently preferred embodiments of the invention, and together with the general description given above and the detailed description of the preferred embodiments given below, serve to explain the principles of the invention.

Fig. 1 is a schematic block diagram illustrating the structure of a prior art inverter control apparatus;

Fig. 2 illustrates prior art waveforms showing the relation among a voltage reference signal  $V^*$ , carrier signals  $V_{CP}$  and  $V_{CN}$ , minimum ON pulse width  $T_0$ , minimum voltage reference  $\pm V_{min}$ , output signal  $V_{out}$  and gate signal  $V_g$ ;



Fig. 3 is a schematic block diagram illustrating the structure of one embodiment of the invention;

5 Fig. 4 is a flow chart illustrating how to determine a normal mode, rectangle mode or zero correction mode in a mode decision circuit of a first embodiment of the invention;

10 Figs. 5 (a) through Fig. 5(c) are flowcharts illustrating operation of the normal mode, rectangle mode or zero correction mode of the first embodiment of the invention;

Fig. 6 is a waveform time chart illustrating operation during a rectangle mode of the first embodiment;

15 Fig. 7 is a waveform time chart illustrating operation during a zero correction mode of the first embodiment;

Fig. 8 is a timing chart illustrating operation of the first embodiment;

20 Fig. 9 is a flow chart illustrating how to select a switching timing of a switching timing selection circuit of the first embodiment;

Fig. 10 is a circuit diagram illustrating a switching timing circuit of the first embodiment;

25 Figs. 11(a) through Fig. 11(e) are charts illustrating a switching timing of a new voltage reference signal  $V''$  ( $V''$  corresponds to  $V_u''$ ,  $V_v''$  and  $V_w''$ ) of the first embodiment of the invention;

30 Fig. 12 is a waveform timing chart illustrating operation in which a voltage reference signal of a phase near positive or negative maximum value corrects to take on a zero value in a rectangle mode of the first embodiment of the invention;

Fig. 13 is a schematic view illustrating a main circuit of a neutral point clamped three-phase inverter;

35 Fig. 14 is a schematic block diagram illustrating a fourth embodiment of the invention;

Fig. 15 is a schematic block diagram illustrating a fifth embodiment of the invention;

Fig. 16 is a flow chart illustrating a sixth embodiment of the invention;

Fig. 17 is a waveform timing chart in a rectangle mode illustrating the sixth embodiment of the invention;

5 Fig. 18 is a flowchart illustrating a seventh embodiment of the invention;

Fig. 19 is a waveform timing chart in a rectangle mode illustrating the seventh embodiment of the invention;

10 Fig. 20 is a schematic view showing the eighth and ninth embodiments of the invention;

Fig. 21 is a flowchart illustrating operation of a mode decision circuit of the eight and ninth embodiments of the invention;

15 Fig. 22 is a waveform timing chart illustrating a voltage reference signal, line voltage and phase voltage of the eight embodiment; and

Fig. 23 is a waveform timing chart illustrating a voltage reference signal, line voltage and phase voltage of the ninth embodiment.

#### Detailed Description of the Preferred Embodiments

Fig. 3 shows the hardware structure in an inverter control apparatus using PWM control according to a first embodiment of the invention.

25 Referring to Fig. 3, a controller 1 outputs voltage reference signals  $V^*$  (representing  $V_u^*$ ,  $V_v^*$ , and  $V_w^*$ ) for three phases (U phase, V phase and W phase) and controls an inverter (used, for example, in a speed control for a motor). A mode decision circuit 2 decides which mode of a normal mode, rectangle mode or zero correction mode will be effective in accordance with the algorithm shown in Fig. 4 whenever the voltage reference signals are output. When all of the voltage reference signals are greater than a minimum voltage reference signal  $V_{min}$ , the normal mode is selected. When at least two voltage reference signals ( $V_u^*$  and  $V_v^*$ ,  $V_v^*$  and  $V_w^*$ ,  $V_u^*$  and  $V_w^*$ ) are

30

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equal to or less than the minimum voltage reference signal  $V_{min}$ , the rectangle mode is selected. Also when three voltage reference signals are twice as much as the minimum voltage reference signal  $V_{min}$  or less, or when two voltage reference signals are twice as much as the minimum voltage reference signal  $V_{min}$  or less and the two voltage reference signals are the opposite sign, the rectangle mode is selected. When one voltage reference signal is equal to or less than the minimum voltage reference signal  $V_{min}$  and the others are twice as much as the minimum voltage reference signal  $V_{min}$  or less and are the opposite sign as the minimum voltage reference signal  $V_{min}$ , the zero correction mode is selected.

Further the mode decision circuit 2 selects among the detailed modes (mode = 0 ~  $\pm$  6) shown in Figs. 5(a) - 5(c), after selecting one of the three modes (normal mode, rectangle mode, and zero correction mode). In the case of the normal mode, the mode which is "Mode = 0" is selected automatically shown in Fig. 5(a). In case of the rectangle mode, as shown in Fig. 5(b), all of voltage reference signals are multiplied together and a signal PNFLG is obtained. The signal PNFLG has a sign (i.e., a positive sign or negative sign) which changes about every 60° in phase with the voltage reference signals. When the signal PNFLG is positive, namely, when one voltage reference signal is positive and the others are negative, the voltage reference signal which has the positive maximum value of the three is selected. When the selected voltage reference signal is  $V_u^*$ , the mode is set "Mode = -1". Further when the selected voltage reference signal is  $V_v^*$  or  $V_w^*$ , the mode is set "Mode = -2" or "Mode = -3" respectively. When the signal PNFLG is negative, the voltage reference signal which has the greatest, negative value of the three is selected. Then when the selected voltage reference signal is  $V_u^*$ ,  $V_v^*$ , or  $V_w^*$ , the mode is set "Mode = 1", "Mode = 2", or "Mode = 3" respectively.

In case of the zero correction mode, since only one voltage reference signal is equal to or less than the minimum voltage reference signal  $V_{min}$ , the mode which is "Mode =  $\pm 4$ " through "Mode =  $\pm 6$ " is selected due to the voltage reference signal which is equal to the minimum voltage reference signal  $V_{min}$  and its polarity as shown in Fig. 5(c).

A voltage reference conversion circuit 3 corrects the voltage reference signals  $V_u'$ ,  $V_v'$ , and  $V_w'$  according to the mode (i.e. normal mode, rectangle mode, or zero correction mode), and outputs new voltage reference signals  $V_u''$ ,  $V_v''$ , and  $V_w''$ :

The correction will be described as follows.

(a) In case of the normal mode:

The mode decision circuit 2 selects "Mode = 0" and outputs the previous voltage reference signals  $V_u'$ ,  $V_v'$ , and  $V_w'$  as the new voltage reference signals  $V_u''$ ,  $V_v''$ , and  $V_w''$ .

$$V_u' = V_u'' \quad . . . (1)$$

$$V_v' = V_v'' \quad . . . (2)$$

$$V_w' = V_w'' \quad . . . (3)$$

(b) In case of the rectangle mode:

The mode decision circuit 2 selects "Mode =  $\pm 1$ " through "Mode =  $\pm 3$ " and fixes the voltage reference signal  $V'$  which has the greatest value of the three signals (i.e.,  $V_u'$ ,  $V_v'$ , and  $V_w'$ ) to the minimum voltage reference  $V_{min}$  which has the opposite polarity to that of the selected greatest value voltage reference signal (or to zero voltage in the embodiment of Fig. 12).

Additionally the circuit 2 shifts the other voltage reference signals without change of the line voltage of the other phase, and outputs the fixed and shifted voltage reference signals  $V_u''$ ,  $V_v''$  and  $V_w''$ .

For instance, when the voltage reference signal  $V_u'$  is the greatest of the three and positive, each voltage reference signal is corrected as follows.

$$V_u'' = - V_{min} \dots (4)$$

$$V_v'' = - V_{min} - (V_u' - V_v') \dots$$

$$V_w'' = - V_{min} - (V_u' - V_w') \dots (6)$$

5 Also, when the voltage reference signal  $V_v'$  is the greatest of the three and negative, each of the voltage reference signals is corrected as follows.

$$V_u'' = V_{min} \dots (7)$$

$$V_v'' = V_{min} - (V_u' - V_v') \dots (8)$$

$$V_w'' = V_{min} - (V_u' - V_w') \dots (9)$$

10 The operational waveforms during the rectangle mode are shown in Fig. 6.

In Fig. 6,  $V_u$ ,  $V_v$ , and  $V_w$  indicate phase voltages (e.g., see Fig. 13), and  $V_{uv}$ ,  $V_{vw}$ , and  $V_{wu}$  indicate line voltages respectively where:

15  $V_{uv} = V_u - V_v$

$$V_{vw} = V_v - V_w \text{ and}$$

$$V_{wu} = V_w - V_u.$$

As shown in Fig. 6, the mode is changed about every 60° in phase, and the voltage reference signal which has the greatest value of the three signals (i.e.  $V_u'$ ,  $V_v'$ , and  $V_w'$ ) in each mode is fixed to the minimum voltage reference signal  $V_{min}$  which has the opposite polarity as the greatest value voltage reference signal. Utilization of formulas (1)-(9) has the result that all three of the voltage reference signals are shifted so that the value of the line voltages do not change from that of the previous value, e.g., the value which would have resulted using  $V'$  instead of  $V''$  as the reference voltages. As is known in the art, no change in the line voltage is equivalent to requiring that the sum of the widths of the line voltage pulses during any cycle (e.g., mode) be the same when using either  $V'$  or  $V''$  as a reference. By controlling the line voltage of the inverter, one can control the inverter output voltage as is desired.

35 In the rectangle mode, all of three phases change positive or negative once about every 60°. Consequently this mode is called "60° conversion method".

(c) In case of the zero correction mode:

The mode decision circuit 2 selects "Mode =  $\pm 4$ " through "Mode =  $\pm 6$ " and changes the voltage reference signal from  $V^*$  to  $V^{**}$ , where  $V^{**}$  is set to the minimum voltage reference signal  $V_{\min}$ , when the voltage reference phase  $V^*$  would otherwise have crossed the zero voltage point. Further the circuit 2 shifts the other voltage reference signals so as not to change the line voltage corresponding to the other voltage reference signals from the previous value.

For instance, when the voltage reference signal  $V_u^*$  crosses the zero point from the positive side to the negative side, each voltage reference signal is corrected as follows.

15 
$$V_u^{**} = V_{\min} \quad . . . (10)$$

$$V_v^{**} = V_{\min} - (V_u^* - V_v^*) \quad . . . (11)$$

$$V_w^{**} = V_{\min} - (V_u^* - V_w^*) \quad . . . (12)$$

Also when the voltage reference signal  $V_u^*$  crosses the zero point from the negative side to the positive side, each voltage reference signal is corrected as follows.

20 
$$V_u^{**} = - V_{\min} \quad . . . (13)$$

$$V_v^{**} = - V_{\min} - (V_u^* - V_v^*) \quad . . . (14)$$

$$V_w^{**} = - V_{\min} - (V_u^* - V_w^*) \quad . . . (15)$$

25 The operational waveforms during the zero correction mode are shown in Fig. 7.

A first data latching circuit 7 stores the outputs  $V_u^{**}$ ,  $V_v^{**}$  and  $V_w^{**}$  from the voltage reference conversion circuit 3 via the normally closed switch SW1. A switching timing selection circuit 4 selects one of four conversion timings 0X, 1X, 2X and 3X shown in Fig. 8 according to the outputs  $V_u^{**}$ ,  $V_v^{**}$  and  $V_w^{**}$  from the voltage reference conversion circuit 3 and the previous outputs  $V_u^{**}$ ,  $V_v^{**}$  and  $V_w^{**}$  which are stored in the first data latching circuit 7 and are output from the circuit 7. Normally open switch SW2 connects the output of the first

data latching circuit 7 with its input and also to a second data latching circuit 8.

5 A timing and carrier comparison circuit 5 decides whether or not to update the content in the first data latching circuit 7.

10 A switching timing circuit 6 latches the output of the second data latching circuit 8 (which may, for example, be a flip-flop) according to the timing which is selected by the switching timing selection circuit 4. A comparator 9 compares the output from second data latching circuit 8 and the carrier, and outputs a gate signal.

15 The controller 1, the mode decision circuit 2, the voltage reference conversion circuit 3, the switching timing selection circuit 4, the timing and carrier comparison circuit 5, and the data latching circuit 7 may be implemented in a data processor such as a microprocessor programmed by software. These elements may thus be referred to as CPU 10.

20 The data loading in CPU 10, namely, the data input into controller 1 is done at the bottom (0X) and top (2X) of the positive side carrier. The voltage reference signals  $V_w'$ ,  $V_v'$  and  $V_w''$  are output from controller 1. The data input provides timing and phase information for the software generation of the sinusoidal reference voltage signals  $V'$ .

25 The switching timing signal TChgX is output as 2-bit data (i.e. 0X=00, 1X=01, 2X=10 and 3X=11) from the switching timing selection circuit 4. The voltage reference signal  $V''(k)$  indicates a signal which is output at this time, and the previous voltage reference signal  $V''(k-1)$  indicates a signal which is output immediately preceding time.

30 The switching timing selection circuit 4 selects a switching timing TChgX (i.e. 0X through 3X) corresponding to the voltage reference signal  $V''(k)$  and the previous voltage reference signal  $V''(k-1)$  according to the flowchart shown in Fig. 9. The flowchart of Fig. 9 is

appropriate whenever the reference voltage signal transitions from positive to negative or visa versa as will become apparent in view of Fig. 11(a) and the subsequent description. In Fig. 9, in step S1, the present or current value of  $V''$  is compared to zero and if it is greater than or equal to zero the program proceeds to step S2 where the previous value of  $V''$  is compared to zero. If this previous value is also greater than or equal to zero, the switching timing selection circuit 4 sets the value of TChgX to 0X=00 which corresponds to the 0a point in Fig. 8. If in step S2, the previous value of  $V''$  is negative, the program proceeds to step S4 where the switching timing selection circuit 4 sets the value of TChgX to 1X=01 which corresponds to the 1a point in Fig. 8. If in step S1, the current value of  $V''$  is negative, the program proceeds to step S5 where the previous value of  $V''$  is compared to zero. If this previous value is greater than or equal to zero, the program proceeds to step S6 where the switching timing selection circuit 4 sets the value of TChgX to 3X=11 which corresponds to the 3a point in Fig. 8. If in step S5, the previous value of  $V''$  is negative, the program proceeds to step S7 where switching timing selection circuit 4 sets the value of TChgX to 2X=10 which corresponds to the 2a point in Fig. 8. In the normal use of the algorithm of Fig. 9, the program proceeds according to steps S1, S2, S4 for a negative to positive transition (see Fig. 11(a)) or via steps S1, S5, S6 for a positive to negative transition (see Fig. 11(b)).

As shown in Fig. 10, the switching timing circuit 6 compares the switching timing signal TChgX 91 which consist of two bits and carrier phase signal 92 which consist of two bits. The carrier phase signal 92 may be obtained by means of dividing the carrier signal into four equal parts and distinguishing the phase range from "0X" to "3X" as shown in Fig. 8. The comparison is made using the XOR circuits 93 and 95, NOR circuits 94 and 96 and OR circuit 98. A discrimination signal 90 is also

utilized to condition the NOR circuit 94 depending upon whether or not it is desired to distinguish between the 0X and 2X timing condition. If there is no need to discriminate between 0X and 2X, the discrimination signal 90 is set to 0, and if it is desired to so discriminate, then the signal 90 is set to 1.

In Fig. 10, L indicates a lower digit and H indicates a higher digit. The XOR circuit 93 compares the lower order bits of the carrier signal and the TChgX signal and outputs a 0 logic signal whenever they are the same. The output of the XOR circuit 93 is fed to NOR circuit 94 which is also conditioned by the discrimination signal 90 and the lower order carrier bit. If it is not desired to distinguish the 0X and 2X timings, (discrimination signal = 0), the NOR circuit 94 outputs a logical 0 whenever the lower order bits of the TChgX signal and the carrier are the both logical 0, e.g., wherever the timing is either 0X or 2X. If the discrimination signal is set to 1, the output of NOR circuit 94 will never be logical 1, and the timing is controlled by the circuits 93, 95 and 96. The inputs to the NOR circuit 96 are both logical 0 only when both the upper and lower bits of the TChgX and carrier bits are equal to each other, and this the NOR circuit 96 outputs a logical 1 only when the timing of the TChgX and carrier are exactly equal. When these two signals are equal to each other, a clock signal is generated from the switching timing circuit 6 which enables the latching of the output data of the second data latching circuit 8.

The preferred operation is illustrated in Figs. 11(a) and 11(b). As seen in these figures, when the polarity of voltage reference signal does not change, the switching timing changes at a timing 0X or 2X. When the polarity of voltage reference signal changes, the switching timing changes at a timing 1X or 3X. In this case, a zero is set as the discrimination signal 90 in Fig. 10, and thus the timings 0X and 2X are not distinguished. Also the switching timing does not switch when the voltage

reference signals  $V_u^{**}$ ,  $V_v^{**}$  and  $V_w^{**}$  crosses the carriers  $V_{CP}$  and  $V_{CN}$ .

To effect no change in the voltage reference signal, the normally closed switch SW1 is open and the normally open switch SW2 is closed. In this manner, the previous value of the voltage reference signal, stored in the first data latching circuit 7 is output to the switching timing selection circuit 4 and via the switch SW2 to the input of the second data latching circuit 8. The newly calculated voltage reference signal is only sent to the switching timing selection circuit 4 but is not fed to the first data latching circuit 7 since the switch SW1 is open. Thus, the previous value of the voltage reference signal is again used at the timings 1X, 3X as long as the polarity of the voltage reference signal does not change. However, at timings 0X and 2X the new value of the voltage reference signal is used since in now switch SW1 will be closed and SW2 will be open. In this case, the new value of the voltage reference signal is fed to the first data latching circuit 7, the switching timing selection circuit 4 and the second data latching circuit 8. The output of the first data latching circuit 7 now is fed only to the switching timing selection circuit 4 and its input is fed with the new value of the voltage reference signal. Thus, in this case, the value of the voltage reference signal changes as seen in Figs. 11 (a) and 11(b).

If the switching timing is always fixed at the timings 0X and 2X, or the timings 1X and 3X, the voltage reference signals,  $V_u^{**}$ ,  $V_v^{**}$  and  $V_w^{**}$  would cross the carriers  $V_{CP}$  and  $V_{CN}$ , and pulses of widths which are less than a minimum ON-pulse widths would be generated at the time that the voltage reference signals  $V_u^{**}$ ,  $V_v^{**}$  and  $V_w^{**}$  are generated as shown in Figs. 11(c) and 11(d). The timing indicates an area which is close to zero voltage or a high voltage regime. Use of this switching timing is thus not done since it would result in the same

problem as exist in the prior art in generating gate pulses less than the minimum ON pulse width.

5 The timing and carrier comparison circuit 5 is similar to the switching timing circuit 6. It compares the switching timing signal TChgX, consisting of two bit and the carrier phase signal, consisting of two bit. When the two signals are equal, the circuit 5 controls the operation of the switches SW1 and SW2 to update the content of first data latching circuit 7 and thus assist in selecting the correct switching timing.

10 Normally, the calculation of the new values of the voltage reference signals are accomplished substantially instantaneously and the procedure set forth above produces the desired result as shown in Figs. 11(a) and 11(b).

15 Sometimes, however, the calculations may take considerably longer. For instance, as shown in Fig. 8, the data loading is done at the timing 0a and one may assume that the new data values for the voltage reference signal are not ready until time 2a. In this case, if the switching is done at the time 1a, the switching timing signal TChgX is output before the finish of the V<sup>''</sup> calculation at time 2a. Since the resulting data is thus incorrect, the output from second data latching circuit 8 is not latched between the timing 2a and timing 0b. In this situation, when the next switching timing is selected, the content of first data latching circuit 7 is not rewritten since the correct result cannot be obtained.

20  
25  
30 In the case of the pulse width modulation (PWM) control using gate turn-off (GTO) thyristors, when an imperfect OFF-gate pulse is fed to the GTO thyristor, current concentrates at one part inside the GTO thyristor and the GTO thyristor breaks down. Accordingly the width of the ON-gate pulse is controlled so as not to be less than the minimum ON-pulse width.

35 As shown in Fig. 11(e), since the width of pulse becomes less than the minimum OFF-pulse width in areas T<sub>MP</sub>

and  $T_{MN}$  where the voltage reference  $V''$  (i.e.,  $V''$  indicates the voltage reference signals  $V_u''$ ,  $V_v''$  and  $V_w''$ ) is over a maximum voltage references  $V_{max}$  and  $-V_{max}$ , the GTO thyristors are held ON in these areas. The maximum voltage references  $V_{max}$  and  $-V_{max}$  are near the maximum value of carrier signals A and B. The carrier signal A is a triangular wave which has a constant frequency and changes in level between 0 and  $V_{max}$ . The carrier signal B is a triangular wave which has a constant frequency, changes in level between 0 and  $-V_{max}$ , and is in phase with the carrier signal A. That is, when  $A = V_{max}$ ,  $B = 0$ , and when  $A = 0$ ,  $B = -V_{max}$ .

In the above case, the starting point and ending point in the area  $T_{MP}$  are changed at the timing  $0X$  and the starting point and ending point in the area  $T_{MN}$  are changed at the timing  $2X$ . In this case, the value 1 is set as the discrimination signal 90 of Fig. 10, and the timings  $0X$  and  $2X$  may thus be distinguished. Accordingly, a positive maximum voltage output area may be distinguished from a negative maximum voltage output area.

In the rectangle mode ( $60^\circ$  conversion method), a correction is achieved by converting  $V'$  to  $V''$  in which  $V''$  changes sign in relation to  $V'$  and takes on the value of the positive or negative minimum voltage reference  $V_{min}$ . Accordingly an alternative embodiment to that of fixing the voltage reference signal to such minimum values is to fix the voltage reference signal to 0 (zero). The voltage reference signal which is set to zero is the positive or negative maximum value of the three phases.

Fig. 12 shows an example of waveform of the voltage reference signals  $V_u'$  through  $V_w'$  corresponding to the above correction, and an example of waveform of the PWM controlled output voltage (phase voltage and line voltage).

As shown in Fig. 12, the corrected voltage reference signal  $V_u''$  is 0 (zero) during the times  $T_{UP}$  and  $T_{UN}$  in

which the voltage reference signal  $V_u'$  corresponds to the positive and negative maximum value.

5 A main circuit of a neutral point clamped three-phase inverter is shown in Fig. 13. Further details concerning the operation of the inverter may be obtained, for example, from the above referenced co-pending application.

10 A neutral point is provided by two capacitors 103. Those capacitors 103 are provided between positive side P and negative side N of a DC voltage source 104. Zero voltage can be output, since voltage outputs  $V_u$ ,  $V_v$  and  $V_w$  are clamped to the neutral point. Consequently electric potential between positive side P and negative side N of the DC voltage source 104 and a three-level voltage output are obtained. In relation to Fig.3, it may be appreciated that the output of the comparator 9 provides six separate gate pulses to turn on/off the GTOs along six separate gate lines. The GTOs are operated in pairs, on being turned on where the other is turned off. 15 The six pairs are: SU1,SU3; SU2,SU4; SV1,SV3; SV2,SV4; SW1,SW3; and SW2,SW4. 20

25 If the voltage reference is fixed to the zero voltage as described above, the number of times the GTO thyristors need to be switched decreased sharply. As the switching loss decreases, the efficient of operation can be improve. Further as the current flowing through the GTO thyristors flows equally in the positive direction and negative direction alternately, heat which is generated from the GTO thyristors is balanced and the rate of using the GTO thyristors is improved. Moreover it is possible to control the output voltage without outputting a pulse which is equal to or less than the minimum ON pulse width near the zero point of the voltage reference due to the zero correction mode. Additionally 30 it is possible to control high output voltage without outputting a pulse which is equal to or less than the minimum OFF pulse width near the maximum value of the voltage reference. Accordingly since it is possible to 35

control the line voltage linearly over the whole output voltage area from the low output voltage area to the high output voltage area, one may obtain an accurately controllable inverter.

5 Next a second embodiment of the invention will be described.

10 In this embodiment, when any one or more voltage reference signals,  $V_u^*$ ,  $V_v^*$  and  $V_w^*$ , are equal to or less than the minimum voltage reference signal  $V_{min}$ , the zero correction mode is selected. When not included, the normal mode is selected. This operation is achieved by the mode decision circuit 2. In this second embodiment, no rectangular mode is utilized.

15 In case of the zero correction mode, a phase (U phase, V phase or W phase) which is equal to or less than the minimum voltage reference signal  $V_{min}$  is distinguished, and then the type of mode, which is comprised of "Mode =  $\pm 4$ " through "Mode =  $\pm 6$ ", is selected as shown in Fig. 5(c).

20 The voltage reference conversion circuit 3 converts the voltage reference signals  $V_u^*$ ,  $V_v^*$  and  $V_w^*$  into new voltage reference signals  $V_u^{**}$ ,  $V_v^{**}$  and  $V_w^{**}$  due to the distinguished modes. An example for mode =  $\pm$  is illustrative.

25 (1) Mode = 4: Only  $V_u^*$  is equal to 0 or greater and is equal to  $V_{min}$  or less.

$$V_u^{**} = V_{min} \quad . . . (16)$$

$$V_v^{**} = V_{min} - (V_u^* - V_v^*) \quad . . . (17)$$

$$V_w^{**} = V_{min} - (V_u^* - V_w^*) \quad . . . (18)$$

30 (2) Mode = -4: Only  $V_u^*$  is equal to  $-V_{min}$  or greater and is less than 0.

$$V_u^{**} = -V_{min} \quad . . . (19)$$

$$V_v^{**} = -V_{min} - (V_u^* - V_v^*) \quad . . . (20)$$

$$V_w^{**} = -V_{min} - (V_u^* - V_w^*) \quad . . . (21)$$

As described above, the voltage reference signal is discontinuous in phase voltage, but the voltage reference signal can form a continuous sinewave in line voltage which is the differences between the phase voltages.

5           According to the second embodiment, it is possible to control the low output voltage without outputting a pulse which is equal to or less than the minimum ON pulse width near the zero point of the voltage reference. Further it is possible to control the high output voltage  
10 without outputting a pulse which is equal to or less than the minimum OFF pulse width near the maximum value of the voltage reference.

Consequently, when this operation is used in a neutral point clamped inverter, it is possible to control  
15 the line output voltage linearly over the whole output voltage area from the low output voltage area to the high output voltage area without increasing the number of switchings for the switching element, e.g., the GTO thyristors.

20           Next a third embodiment of the invention will be described. This embodiment utilizes only the rectangular correction mode.

In this embodiment, a first method of selecting the positive maximum value of the voltage reference signals  $V_u^*$ ,  $V_v^*$  and  $V_w^*$  and a second method of selecting the negative maximum value of the voltage reference signals  $V_u^*$ ,  $V_v^*$  and  $V_w^*$  are used about every  $60^\circ$  at the phase of U phase voltage reference signal  $V_u^*$  in the mode decision circuit 2 shown in Fig. 3. For example, in the first  
25 method when the positive maximum value is the U phase voltage reference signal  $V_u^*$ , "Mode = -1" is selected. Also when the negative maximum value is the U phase voltage reference signal  $V_u^*$ , "Mode = 1" is selected.

30           Further the voltage reference conversion circuit 3 converts the voltage reference signals  $V_u^*$ ,  $V_v^*$  and  $V_w^*$  into new voltage reference signals  $V_u^{**}$ ,  $V_v^{**}$  and  $V_w^{**}$  due to the selected mode in the mode decision circuit 2.  
35

For example, in the case of "Mode = 1", new voltage reference signals  $V_u''$ ,  $V_v''$  and  $V_w''$  are obtained following the expressions (16) through (18). Moreover in the case of "Mode = -1", new voltage reference signals  $V_u''$ ,  $V_v''$  and  $V_w''$  are obtained following the expressions (19) through (21).

Consequently the new voltage reference signals are discontinuous in phase voltage, but the new voltage reference signals can form a continuous sinewave in line voltage which is the differences between the phase voltages.

Next a fourth embodiment of the invention will be described with reference to Fig. 14.

As shown in Fig. 14, in the fourth embodiment of the invention, the switching timing selection circuit 4, the timing and carrier comparison circuit 5 and the first data latching circuit 7 are omitted. A timing circuit 6A is provided instead of the switching timing circuit 6.

The timing circuit 6A changes the voltage reference signal at the fixed timings 0X and 2X and may be implemented with a simple NOR circuitry.

In this case, the pulse widths of the minimum voltage reference signal  $V_{\min}$  and the maximum voltage reference signal  $V_{\max}$  are set to be twice as great as the minimum ON pulse width and the minimum OFF pulse width, since in the case of the 0X and 2X timings as seen in Figs. 11(c) and 11(d), when the voltage reference is changed, a pulse which has half the width as the minimum ON pulse width or the minimum OFF pulse width is generated.

According to the fourth embodiment, it is possible to control the line voltage linearly over the whole output voltage area.

Next a fifth embodiment of the invention will be described with reference to Fig. 15.

In this fifth embodiment, a level detection circuit 11 and a pulse correction circuit 12 are provided in addition to the elements of the fourth embodiment.

The level detection circuit 11 distinguishes whether the new voltage reference signals  $V_u''$ ,  $V_v''$  and  $V_w''$  are near the zero point or the signals  $V_u''$ ,  $V_v''$  and  $V_w''$  are near the maximum voltage value.

5 The pulse correction circuit 12 deletes a pulse or fixes the pulse width to the minimum ON pulse width or the minimum OFF pulse width.

The pulse is generated when the voltage reference is changed and has a half width ( $T_{1/2}$  in Fig. 11 (c)) as the  
10 minimum ON pulse width or the minimum OFF pulse width.

Next a method of deciding the mode during the rectangle mode will be described as a sixth embodiment of the invention with reference to Figs. 16 and 17.

In this embodiment, when the mode is changed to the  
15 rectangle mode, a periodic clock pulse is counted. Whenever the counted number reaches at a determined clock number, the counted number is initialized and the sign of the flag PNFLG is changed. As a result, the type of mode may be distinguished from the sign of PNFLG. The mode  
20 consists of six kinds which are "Mode =  $\pm 1$ " through "Mode =  $\pm 3$ ".

In this method the sign of PNFLG periodically changes. The change is not related to the frequency of voltage reference signals  $V_u'$ ,  $V_v'$  and  $V_w'$ . This method is  
25 named "time changing method of the rectangle mode."

An example of the waveform resulting when the sign of PNFLG is changed every 20ms using the above method is illustrated in Fig. 17.

Accordingly to the sixth embodiment, since the  
30 switching elements (GOT thyristors) which are provided at the positive side and negative side become ON without relation to the frequency of the voltage reference signals  $V_u'$ ,  $V_v'$  and  $V_w'$ , the range of temperature variations of the switching elements can be controlled to  
35 be quite small.

Consequently the efficient of operating an inverter is greatly improved.

Next a seventh embodiment of the invention will be described with reference to Fig. 18.

As shown in Fig. 18, when the mode is changed the rectangle mode, the system distinguishes whether or not the frequency of changes in the voltage reference signals  $V_u^*$ ,  $V_v^*$  and  $V_w^*$  are greater than a preset value. As the result, when the frequency is equal to or greater than the preset value, the mode decision is done as described in Fig. 5(b). When the frequency is less than the preset value, the mode decision is done as described in Fig. 16.

A waveform example is illustrated in Fig. 19. In this example, the waveform is generated when the frequency of the voltage reference changes from 5Hz to 10Hz and the time changing method is changed to the  $60^\circ$  changing method near 8.3Hz.

According to the seventh embodiment, in the low frequency regime or during outputting DC power, it is possible to control the increase of temperature of the switching elements due to the time changing method.

Accordingly the efficient of operating is improved.

In the normal frequency area, the number of switchings required for the switching elements such as the GTO thyristor decreases sharply.

Consequently it is possible to operate the inverter in an efficient manner.

Next an eighth embodiment of the invention will be described in reference to Fig. 20.

Fig. 20 shows a neutral point clamped inverter using PWM control. A controller 201 outputs voltage reference signals  $V_u^*$ ,  $V_v^*$  and  $V_w^*$  and controls an inverter (not shown). A mode decision circuit 202 sets a 1 or -1 into a positive/negative changing signal PNFLG every positive or negative period  $T$  of  $V^{**}$ . The period is timed by means of a timer or counter (not shown) which increments an index  $i$  as shown in Fig. 21 in a similar fashion as in Fig. 16.

When the signal PNFLG1 is 1, a voltage reference signal which has the positive maximum value of the three

signals  $V_u^*$ ,  $V_v^*$  and  $V_w^*$  is selected. If the selected signal is  $V_u^*$ , "Mode 1" is selected. Further if the selected signal is  $V_v^*$  or  $V_w^*$ , "Mode 2" or "Mode 3" is selected respectively. Additionally when the signal PNFLG is -1, the voltage reference signal which has the negative maximum value of the three signals  $V_u^*$ ,  $V_v^*$  and  $V_w^*$  is selected. If the selected signal is  $V_u^*$ ,  $V_v^*$  or  $V_w^*$ , "Mode -1", "Mode -2" or "Mode -3" is selected respectively.

10 According the mode decision circuit 202 outputs one of the possible six types of modes as described above.

A voltage reference conversion circuit 203 corrects the voltage reference signals  $V_u^*$ ,  $V_v^*$  and  $V_w^*$  and output new voltage reference signals  $V_u^{**}$ ,  $V_v^{**}$  and  $V_w^{**}$  due to the above modes. An example for the U-phase is as follows with the other phases related in a similar manner.

(1) Mode = 1: when  $V_u^*$  is the positive maximum value of the three signals.

$$V_u^{**} = V_{max} \quad . . . (22)$$

$$V_v^{**} = V_{max} - (V_u^* - V_v^*) \quad . . . (23)$$

$$V_w^{**} = V_{max} - (V_u^* - V_w^*) \quad . . . (24)$$

(2) Mode = -1: when  $V_u^*$  is the negative maximum value of the three signals.

$$V_u^{**} = - V_{max} \quad . . . (25)$$

$$V_v^{**} = - V_{max} - (V_u^* - V_v^*) \quad . . . (26)$$

$$V_w^{**} = - V_{min} - (V_u^* - V_w^*) \quad . . . (27)$$

$V_{max}$  means the maximum voltage reference.

Fig. 22 shows waveforms of the voltage reference signals, the phase voltages and the line voltages in accordance with the eighth embodiment of the invention.

The controller 201, the mode decision circuit 202 and the voltage reference conversion circuit 203 may be implemented in software via a programmed data processor such as a microprocessor. These elements may thus be referred to as CPU 205.

As described above, in this embodiment, the voltage reference is discontinuous in the phase voltage; however, the new voltage reference signals  $V_u''$ ,  $V_v''$  and  $V_w''$  can form a continuous sinewave in the line voltage which is the difference between the phase voltages.

A comparator 204 compares the new voltage reference signals  $V_u''$ ,  $V_v''$  and  $V_w''$  from the voltage reference conversion circuit 203 with the carrier signals, and produces a gate signal when the reference signals crosses the carrier signals.

Accordingly the voltage reference signals  $V_u'$ ,  $V_v'$  and  $V_w'$  are not output as a pulse which is equal to or less than the minimum ON pulse width from the voltage reference conversion circuit 203. Further the line voltage is converted to new voltage reference signals  $V_u''$ ,  $V_v''$ , and  $V_w''$  respectively. The line voltage signals corresponding to  $V_u''$ ,  $V_v''$  and  $V_w''$  form a continuous sinewave.

Consequently when the output frequency from the inverter is in the low voltage regime, the increase in temperature of switching elements, such as GTO thyristors, is fixed, and it is possible to control the output line voltage linearly.

Next a ninth embodiment of the invention will now be described.

In this embodiment, a positive/negative changing signal PNFLG is set to "+1" or "-1" in the mode decision circuit 202 (shown in Fig. 20) every positive/negative changing period T by a timer (not shown). Then, due to the positive/negative changing signal PNFLG, the voltage reference signals  $V_u'$ ,  $V_v'$  and  $V_w'$  are added to a fixed voltage reference using the following expressions, and new voltage reference signals  $V_u''$ ,  $V_v''$  and  $V_w''$  are obtained as shown in Fig. 23.

All of the new voltage reference signals  $V_u''$ ,  $V_v''$  and  $V_w''$  are changed positive or negative every positive/negative changing period T.

(1) When PNFLG is "1":

$$V_u'' = V_u' + 1/2 \cdot V_{max} \quad . . . (28)$$

$$V_v'' = V_v' + 1/2 \cdot V_{max} \quad . . . (29)$$

$$V_w'' = V_w' + 1/2 \cdot V_{max} \quad . . . (30)$$

5 (1) When PNFLG is "-1":

$$V_u'' = V_u' - 1/2 \cdot V_{max} \quad . . . (31)$$

$$V_v'' = V_v' - 1/2 \cdot V_{max} \quad . . . (32)$$

$$V_w'' = V_w' - 1/2 \cdot V_{max} \quad . . . (33)$$

10  $V_{max}$  means the maximum voltage reference, and  $V_u'$  is equal to  $1/2 \cdot V_{max}$  or less. Thus, in terms of absolute values,  $V''$  is less than or equal to  $V_{max}$ .

15 The ninth embodiment of the invention has the advantage of a particularly simple construction. Further when the output frequency from the inverter is in the low level regime, the increase of the temperature of the switching elements, such as GTO thyristors, is fixed, and it is possible to control the output line voltage linearly.

20 The present invention is represented by the control block diagram of hardware for the sake of descriptive convenience. However, it is apparent that the present invention can be realized by arithmetic operations by means of software using a microcomputer or the like.

25 Furthermore, in the above embodiments, the present invention is applied to the inverter apparatus for converting DC power into AC power. However, as is well understood by those skilled in the art, the present invention is equally applicable to a converter apparatus for converting AC power into DC power.

30 Additional advantages and modifications will readily occur to those skilled in the art. Therefore, the invention in its broader aspects is not limited to the specific details, and representative devices, shown and described herein. Accordingly, various modifications may  
35 be made without departing from the spirit or scope of the



THE CLAIMS DEFINING THE INVENTION ARE AS FOLLOWS:-

1. A method of controlling an inverter generating a plurality of phase voltages and a corresponding plurality of line voltages defined as the differences between said phase voltages, said method comprising the steps of:

5 generating voltage reference signals having <sup>corresponding</sup> plural phases;

10 determining one of (1) a normal mode, (2) a rectangle mode and (3) a zero correction mode of operation of said inverter in response to values and polarities of said voltage references;

using the voltage references during the normal mode as a reference value for controlling said inverter; and

15 in at least one of said determined rectangle and zero correction modes, converting the voltage reference signals to converted voltage reference signals in accordance with a preset algorithm such that each phase voltage based on said converted voltage reference signals has a controlled pulse width greater than or equal to a ~~predetermined minimum width~~ <sup>minimum ON-pulse width or a minimum OFF-pulse width</sup> and such that the resulting line voltages do not change when compared to said line voltages generated using said voltage reference signals.

20 2. The method recited in claim 1 wherein the step of generating voltage reference signals comprises generating voltage reference signals having three phases, and the method further comprising the steps of:

25 determining the normal mode when the all three phases of the voltage reference signals are over a preset value;

30 determining the rectangle mode when at least one of the following conditions exist: (1) at least two phases of the voltage reference signals are less than or equal to the preset value, and (2) at least two phases of the voltage reference signals are less than or equal to twice the preset value and the signs of said at least two

phases of the voltage reference signals are of different polarities with respect to each other; and

5 determining the zero correction mode when the voltage reference of one phase of the voltage reference signals is less than or equal to the set value, and the other two phases of the voltage reference signals are less than or equal to twice the preset value and have the same polarity.

10 3. The method as recited in claim 1 or 2, wherein said converted voltage reference signals have phases corresponding to the phases of said voltage reference signals and wherein said step of converting said voltage reference signals to said converted voltage reference signals in said rectangular mode comprises the steps of:

15 selecting the phase of said voltage reference signals which has the greatest absolute value, and

20 fixing the phase of the converted voltage reference signal corresponding to said selected phase to a predetermined value,  $V_{min}$ , where  $V_{min}$  has the opposite sign as said selected phase, and fixing the other phases of the converted voltage reference signals such that the resulting line voltages do not change when compared to said line voltages generated using said voltage reference signals.

25 4. The method as recited in claim 1 or 2, wherein said converted voltage reference signals have phases  $V_u''$ ,  $V_v''$ , and  $V_w''$ , corresponding respectively to the phases  $V_u'$ ,  $V_v'$ , and  $V_w'$  of said voltage reference signals and wherein said step of converting said voltage reference signals to said converted voltage reference signals in said rectangular mode comprises the steps of:

30 a) when the voltage reference signal  $V_u'$  is the greatest of the three phases and is positive, setting the values of the corrected voltage reference signals according to the following relations:

35

$$V_u^{**} = - V_{\min}$$

$$V_v^{**} = - V_{\min} - (V_u^* - V_v^*)$$

$$V_w^{**} = - V_{\min} - (V_u^* - V_w^*), \text{ and}$$

when the voltage reference signal  $V_u^*$  is the greatest of the three phases and is negative, setting the values of the corrected voltage reference signals according to the following relations:

$$V_u^{**} = V_{\min}$$

$$V_v^{**} = V_{\min} - (V_u^* - V_v^*)$$

$$V_w^{**} = V_{\min} - (V_u^* - V_w^*)$$

where  $V_{\min}$  is a predetermined value.

5. The method as recited in claim 1 or 2, wherein said converted voltage reference signals have phases  $V_u^{**}$ ,  $V_v^{**}$ , and  $V_w^{**}$ , corresponding respectively to the phases  $V_u^*$ ,  $V_v^*$ , and  $V_w^*$  of said voltage reference signals and wherein said step of converting said voltage reference signals to said converted voltage reference signals in said rectangular mode comprises the steps of:

a) when the voltage reference signal  $V_u^*$  is the greatest of the three phases and is positive, setting the values of the corrected voltage reference signals according to the following relations:

$$V_u^{**} = 0$$

$$V_v^{**} = - V_{\min} - (V_u^* - V_v^*)$$

$$V_w^{**} = - V_{\min} - (V_u^* - V_w^*), \text{ and}$$

when the voltage reference signal  $V_u^*$  is the greatest of the three phases and is negative, setting the values of the corrected voltage reference signals according to the following relations:

$$V_u^{**} = 0$$

$$V_v^{**} = V_{\min} - (V_u^* - V_v^*)$$

$$V_w^{**} = V_{\min} - (V_u^* - V_w^*)$$

where  $V_{\min}$  is a predetermined value.

6. The method as recited in claim 1 or 2, wherein the step of converting said voltage reference signals to

5 said converted voltage reference signals in said rectangular mode takes place at one of (1) a fixed time when the frequency of said voltage reference signals is less than a prefixed value, and (2) at a time which is determined by a predetermined phase of said voltage reference signals when the frequency of voltage reference signals is greater than or equal to said prefixed value.

10 7. The method as recited in claim 3, wherein the step of converting said voltage reference signals to said converted voltage reference signals in said rectangular mode takes place at one of (1) a fixed time when the frequency of said voltage reference signals is less than a prefixed value, and (2) at a time which is determined by a predetermined phase of said voltage reference signals when the frequency of voltage reference signals is greater than or equal to said prefixed value.

15 20 8. The method as recited in claim 4, wherein the step of converting said voltage reference signals to said converted voltage reference signals in said rectangular mode takes place at one of (1) a fixed time when the frequency of said voltage reference signals is less than a prefixed value, and (2) at a time which is determined by a predetermined phase of said voltage reference signals when the frequency of voltage reference signals is greater than or equal to said prefixed value.

25 30 9. A method of controlling an inverter generating a plurality of phase voltages and a corresponding plurality of line voltages defined as the differences between said phase voltages, comprising the steps of:

- 35
- a) generating voltage references signals having ~~a~~ <sup>corresponding</sup> plurality of phases;
  - b) selecting the phase of the voltage reference signal which has the most positive value;
  - c) converting said selected phase to a phase of a converted voltage reference signal which has one of (1)



a preset minimum value which is negative and (2) a preset value which is zero;

5 d) converting the other phases of said voltage reference signals to converted voltage reference signals of said inverter such that the resulting line voltages do not change when compared to said line voltages generated using said voltage reference signals;

10 e) selecting the phase of the voltage reference signal which has the most negative value;

f) converting said selected phase to a phase of a converted voltage reference signal which has one of (1) a preset minimum value which is positive and (2) a preset value which is zero;

15 g) converting the other phases of said voltage reference signals to converted voltage reference signals of said inverter such that the resulting line voltages do not change when compared to said line voltages generated using said voltage reference signals; and

20 h) switching alternately between steps b)-d) and steps e)-g) to control said inverter.

25 10. An inverter control apparatus for an inverter generating a plurality of phase voltages and a corresponding plurality of line voltages defined as the differences between said phase voltages, comprising:

a) mode decision means for determining one of (1) a normal mode, (2) a rectangle mode and (3) a zero correction mode in response to values and polarities of voltage reference signals having <sup>corresponding</sup> plural phases; and

30 b) voltage reference conversion means:

1) operative in said normal mode for outputting the voltage reference signals as converted voltage reference signals which are identical to said voltage reference signals; and

2) operative in said rectangle and zero correction modes for outputting corrected voltage reference signals in response to said voltage reference signals in accordance with an algorithm such that the



resulting line voltages do not change when compared to said line voltages generated using said voltage reference signals.

5 11. The inverter control apparatus as recited in claim 10, wherein said inverter is a neutral point clamped inverter which outputs three phase voltages and wherein, in said rectangle mode, said voltage reference conversion means is operative to fix one phase of said  
10 corrected voltage reference signals to a zero value.

12. An inverter control apparatus for controlling a neutral point clamped three-phase inverter having switching elements and generating a plurality of phase voltages and a corresponding plurality of line voltages comprising:

15 means for generating voltage reference signals having <sup>corresponding</sup> plural phases;

voltage reference conversion means for:

20 (1) converting said voltage reference signals to converted voltage reference signals, said conversion means fixing the value of one of a corrected voltage reference signal to one of a positive minimum value or a negative minimum value when the width of any of said  
25 plurality of phase voltages becomes equal to a minimum value corresponding to a minimum ON pulse width of the switching elements; and

(2) converting the other of said voltage references signals such that ~~the resulting line voltages~~ do not change when compared to said line voltages generated using said voltage reference signals.  
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13. An inverter control apparatus for controlling a neutral point clamped three-phase inverter, said inverter generating a plurality of phase voltages and a corresponding plurality of line voltages comprising:

35 means for generating voltage reference signals having <sup>corresponding</sup> plural phases;

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5 first voltage reference conversion means for converting all phases of said voltage reference signals to converted voltage reference signals, all having a positive polarity, such that the resulting line voltages generated from said converted voltage reference signals do not change when compared to said line voltages generated using said voltage reference signals;

10 second voltage reference conversion means for converting all phases of said voltage reference signals to converted voltage reference signals, all having a negative polarity, such that the resulting line voltages generated from said converted voltage reference signals do not change when compared to said line voltages generated using said voltage reference signals; and

15 switching means for alternately controlling said inverter using said first and second voltage reference conversion means.

20 14. An inverter control apparatus for controlling a neutral point clamped three-phase inverter, said inverter generating a three phase voltages and a corresponding three line voltages, comprising:

25 first voltage reference conversion means for converting two phases of said voltage reference signals to converted voltage reference signals, each having a positive polarity, and for converting the other phase of said voltage reference signal to a converted voltage reference signal of a zero value, said conversion such that the resulting line voltages generated from said converted voltage reference signals do not change when compared to said line voltages generated using said voltage reference signals;

30 second voltage reference conversion means for converting two phases of said voltage reference signals to converted voltage reference signals, each having a negative polarity, and for converting the other phase of said voltage reference signal to a converted voltage reference signal of a zero value, said conversion such

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that the resulting line voltages generated from said converted voltage reference signals do not change when compared to said line voltages generated using said voltage reference signals; and

5 switching means for alternately controlling said inverter using said first and second voltage reference conversion means.

10 15. An inverter control apparatus for controlling a neutral point clamped three-phase inverter, said inverter generating three phase voltages and a corresponding three line voltages, comprising:

a) a generator which generates voltage reference signals having a ~~plurality~~<sup>corresponding</sup> of phases;

15 b) means for selecting the phase of the voltage reference signal which has the most positive value;

c) means for converting said selected phase to a phase of a converted voltage reference signal which has a preset positive maximum value;

20 d) means for converting the other phases of said voltage reference signals to converted voltage reference signals of said inverter such that the resulting line voltages do not change when compared to said line voltages generated using said voltage reference signals;

25 e) means for selecting the phase of the voltage reference signal which has the most negative value;

f) means for converting said selected phase to a phase of a converted voltage reference signal which has a preset negative maximum value;

30 g) means for converting the other phases of said voltage reference signals to converted voltage reference signals of said inverter such that the resulting line voltages do not change when compared to said line voltages generated using said voltage reference signals; and

35 h) means for switching alternately between steps b) - d) and steps e) - g) to control said inverter.

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Abstract of the Disclosure

An inverter control apparatus comprises a controller, a mode decision circuit and a voltage reference conversion circuit. The mode decision circuit determines one of three kinds of modes which may be used to control the inverter, namely, a normal mode, a rectangle mode and zero correction mode selected according to values and polarities of multi-phase voltage reference signals. The voltage reference conversion circuit corrects the voltage reference signals according to the determined mode in the mode decision circuit. In the case of the normal mode, the mode decision circuit outputs the previous voltage reference signal  $V^*$  without change as the new or corrected voltage reference signals. In the case of the rectangle mode, the circuit fixes the voltage reference signal  $V^*$  having the greatest value of the three phase (U-phase, V-phase and W-phase) to a minimum voltage reference  $V_{min}$  which is of opposite polarity to the selected greatest value signal, or, in another embodiment, to a zero value. Further the circuit converts the others voltage reference signals to corrected voltage reference signals without change of line voltage.

The control circuit permits control of the inverter even in a regime of low reference voltage which would otherwise result in an uncontrolled region of the inverter.

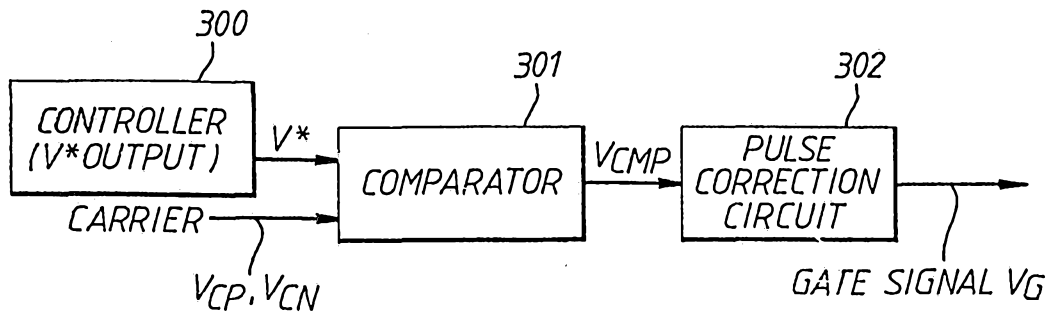


Fig. 1 (PRIOR ART)

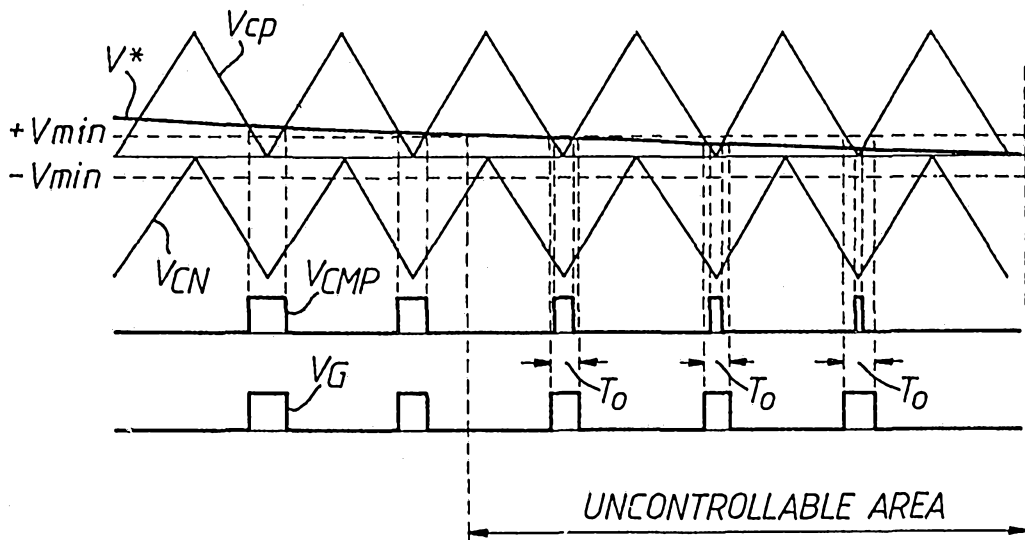
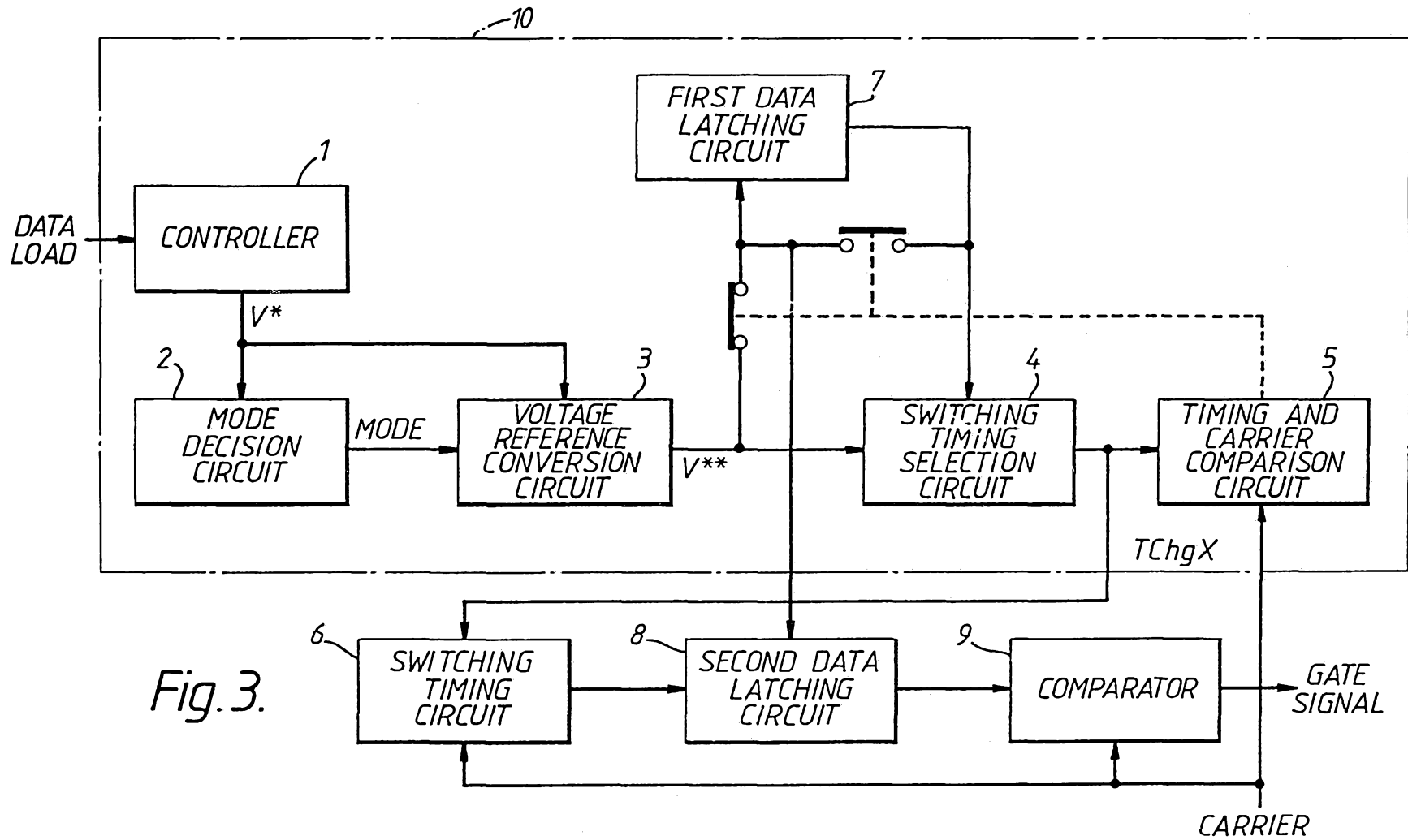
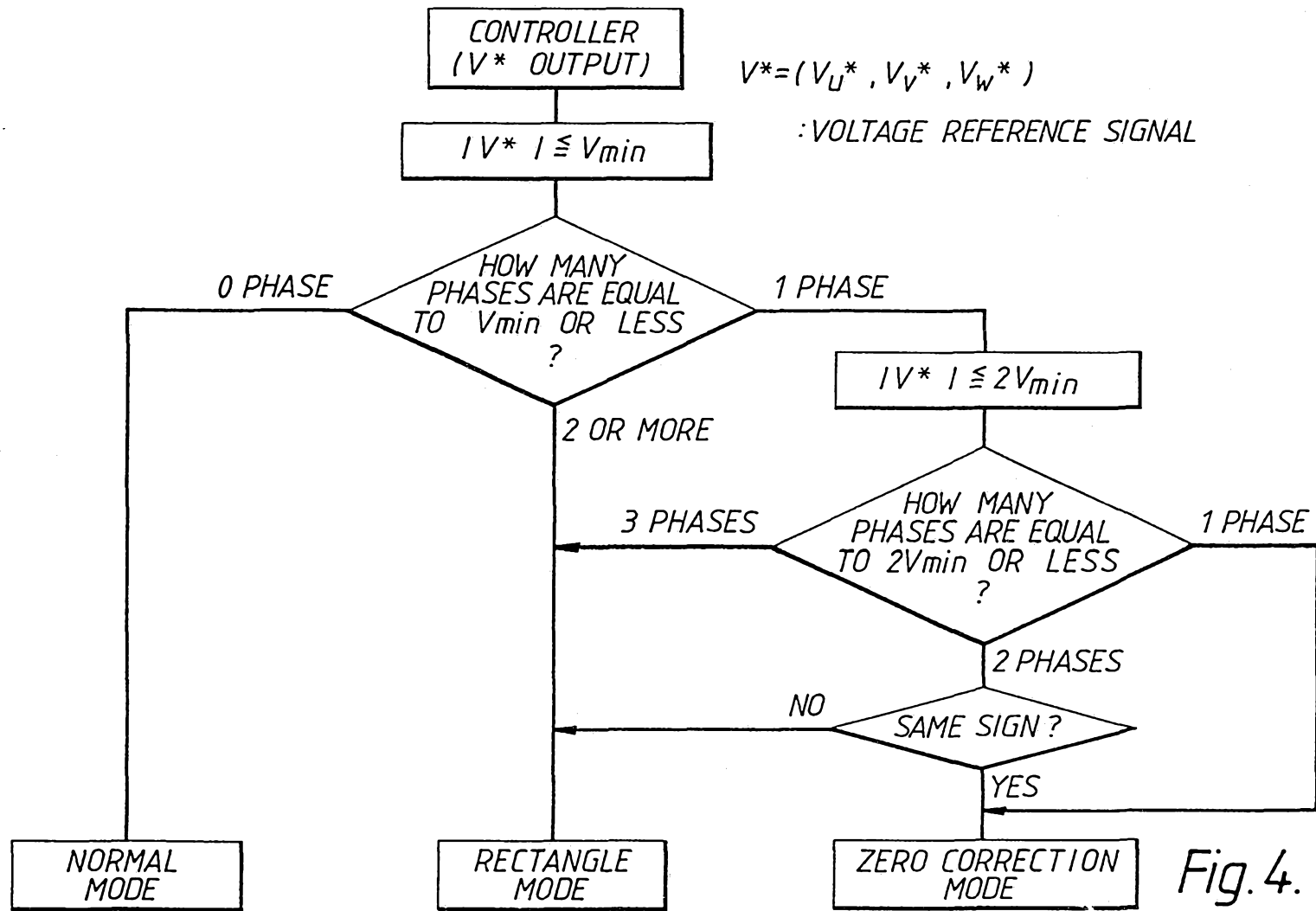


Fig. 2 (PRIOR ART)



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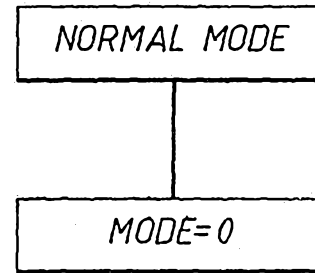


Fig. 5(a)

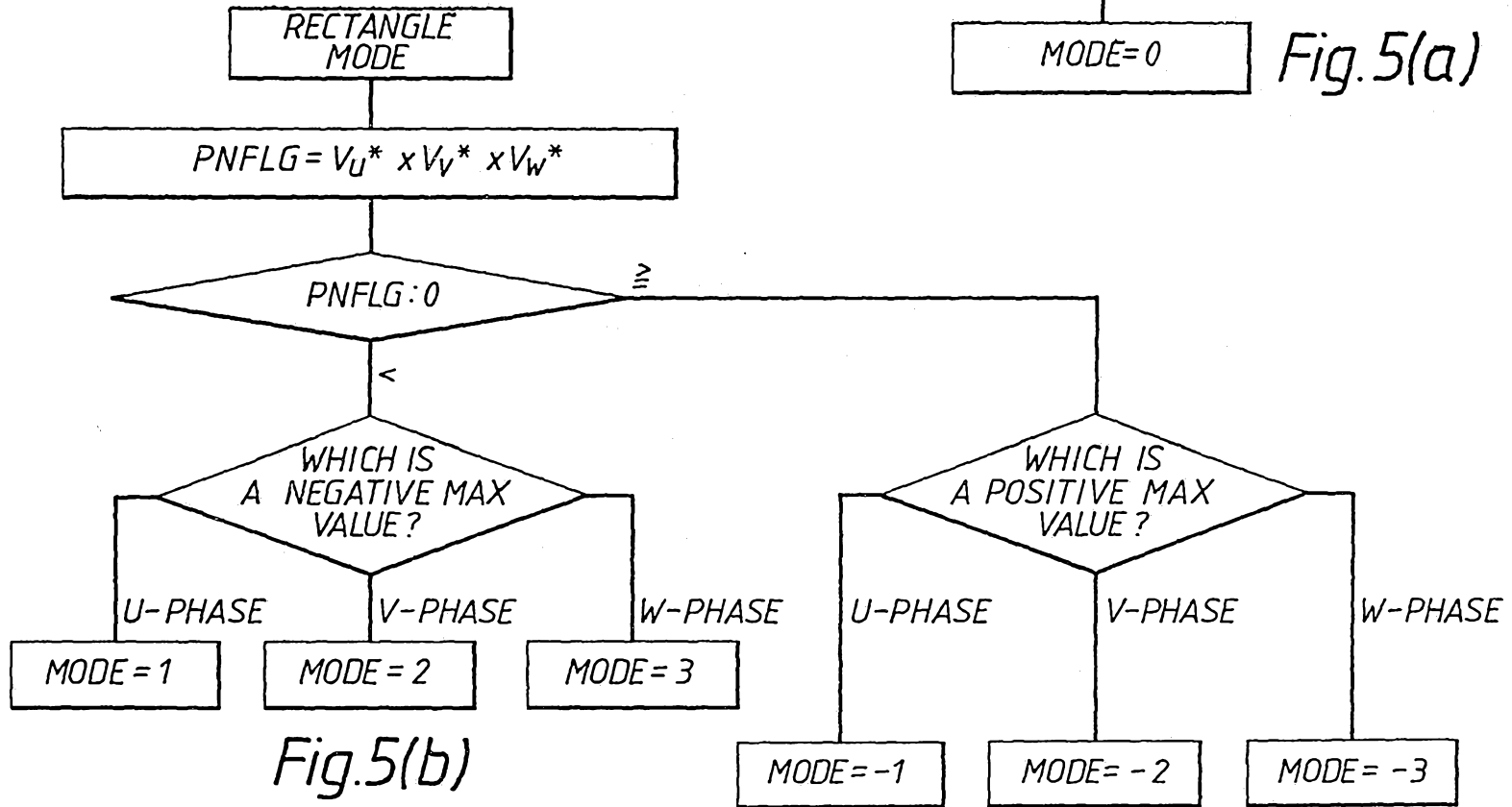


Fig. 5(b)

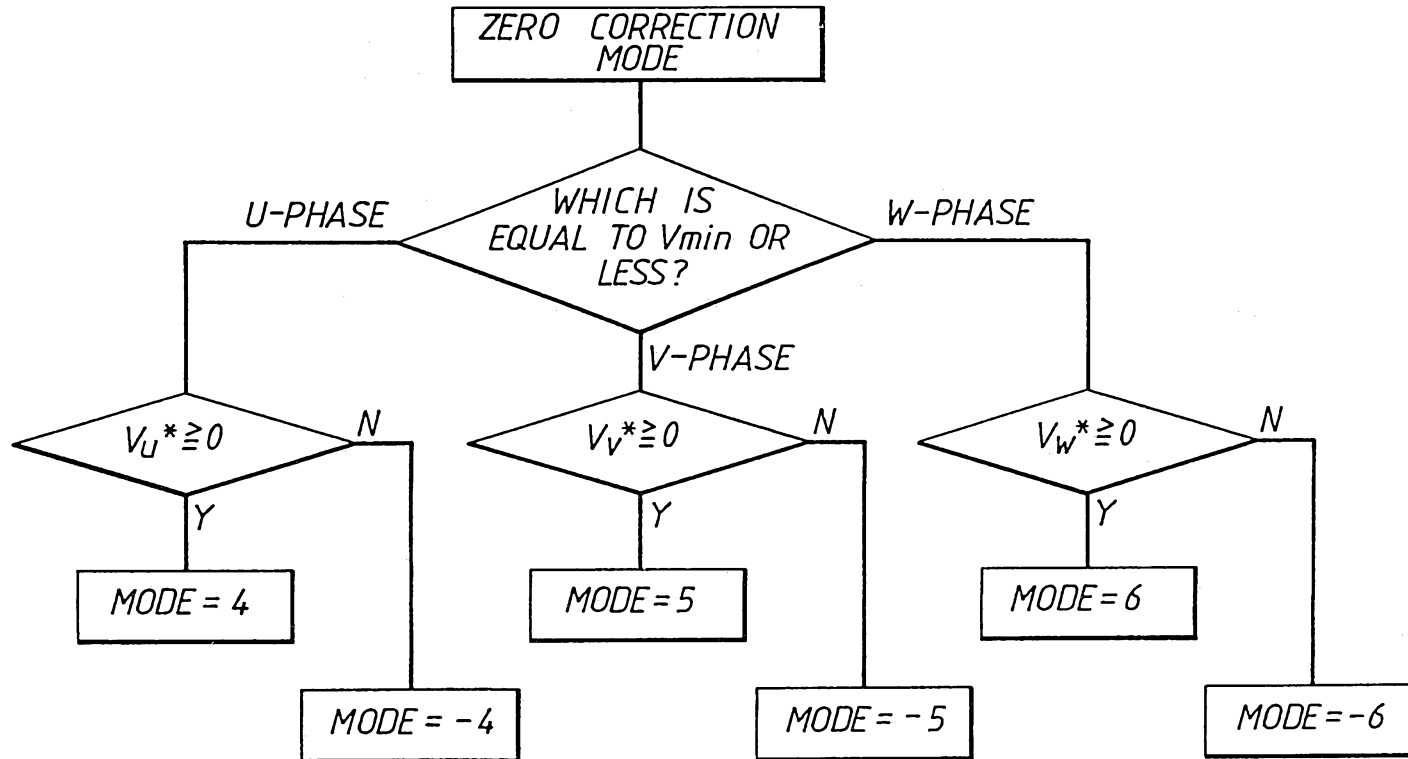


Fig.5(c)

3000 3195

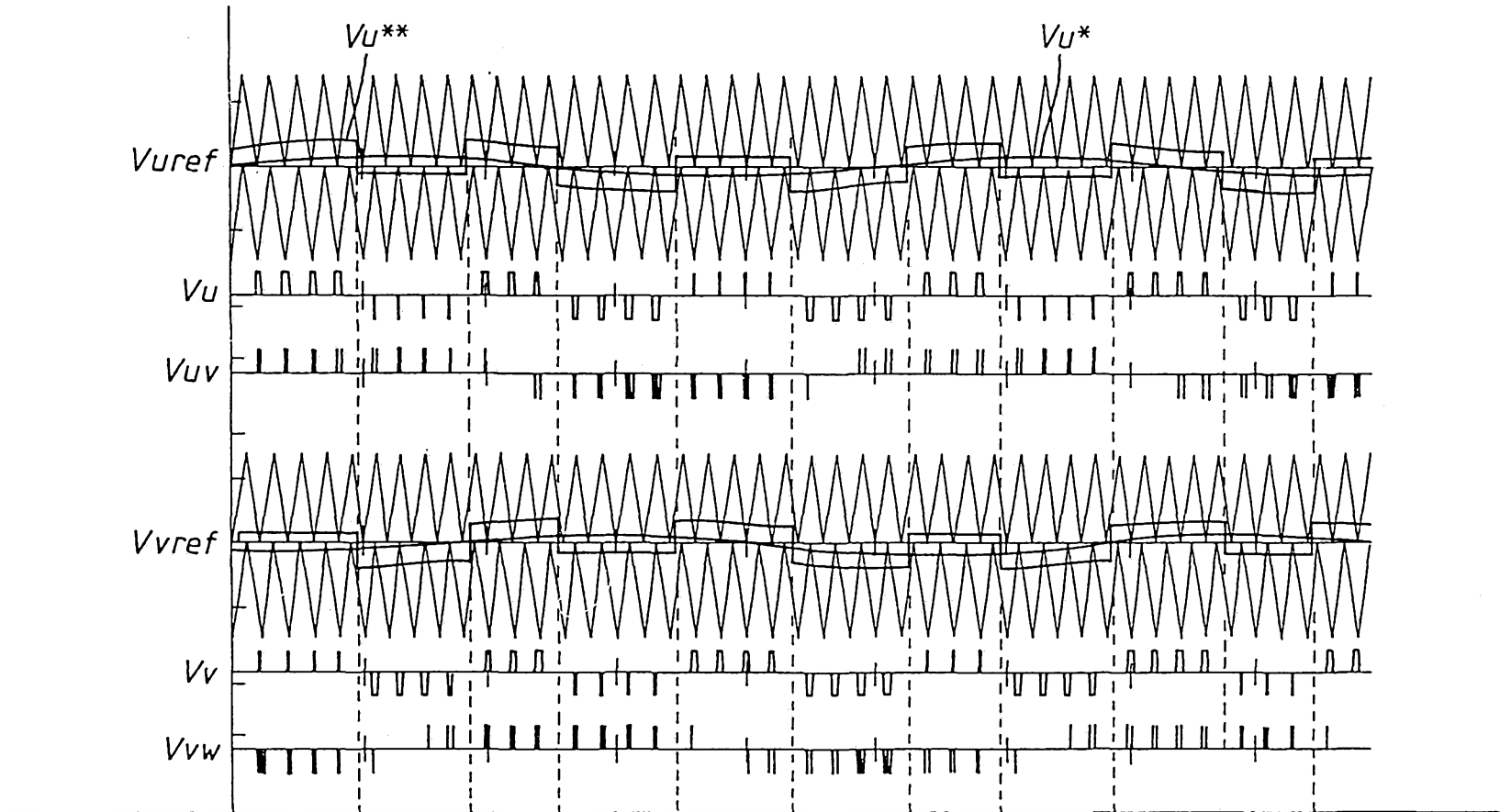


Fig.6.

3000 310

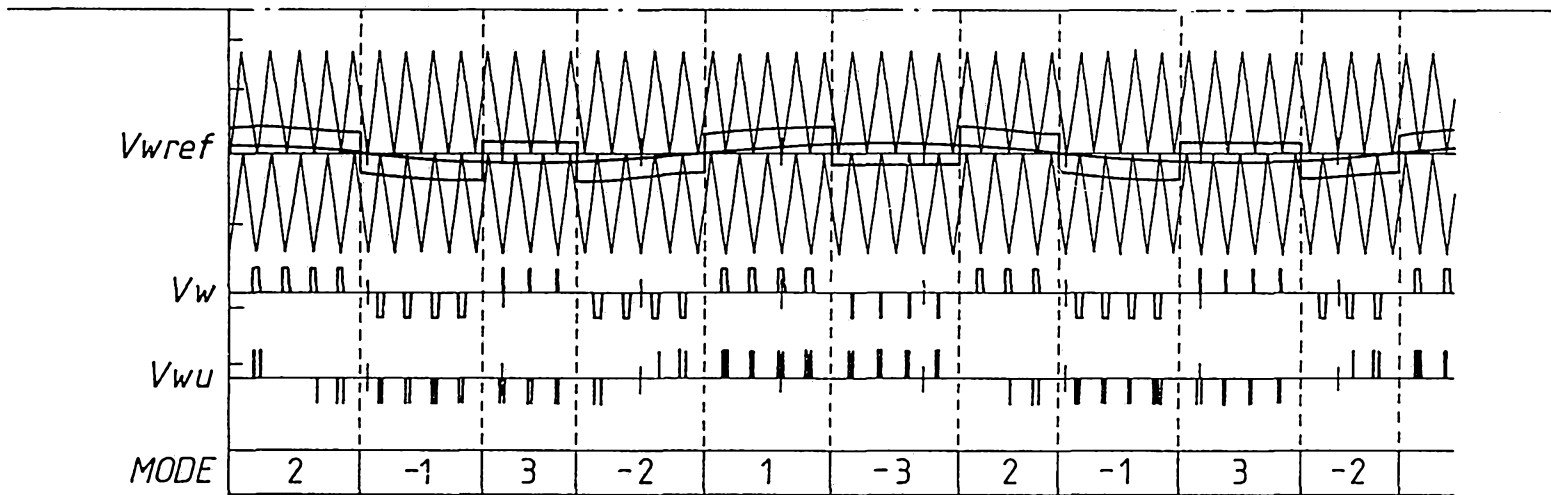


Fig. 6(cont.)

3000 319

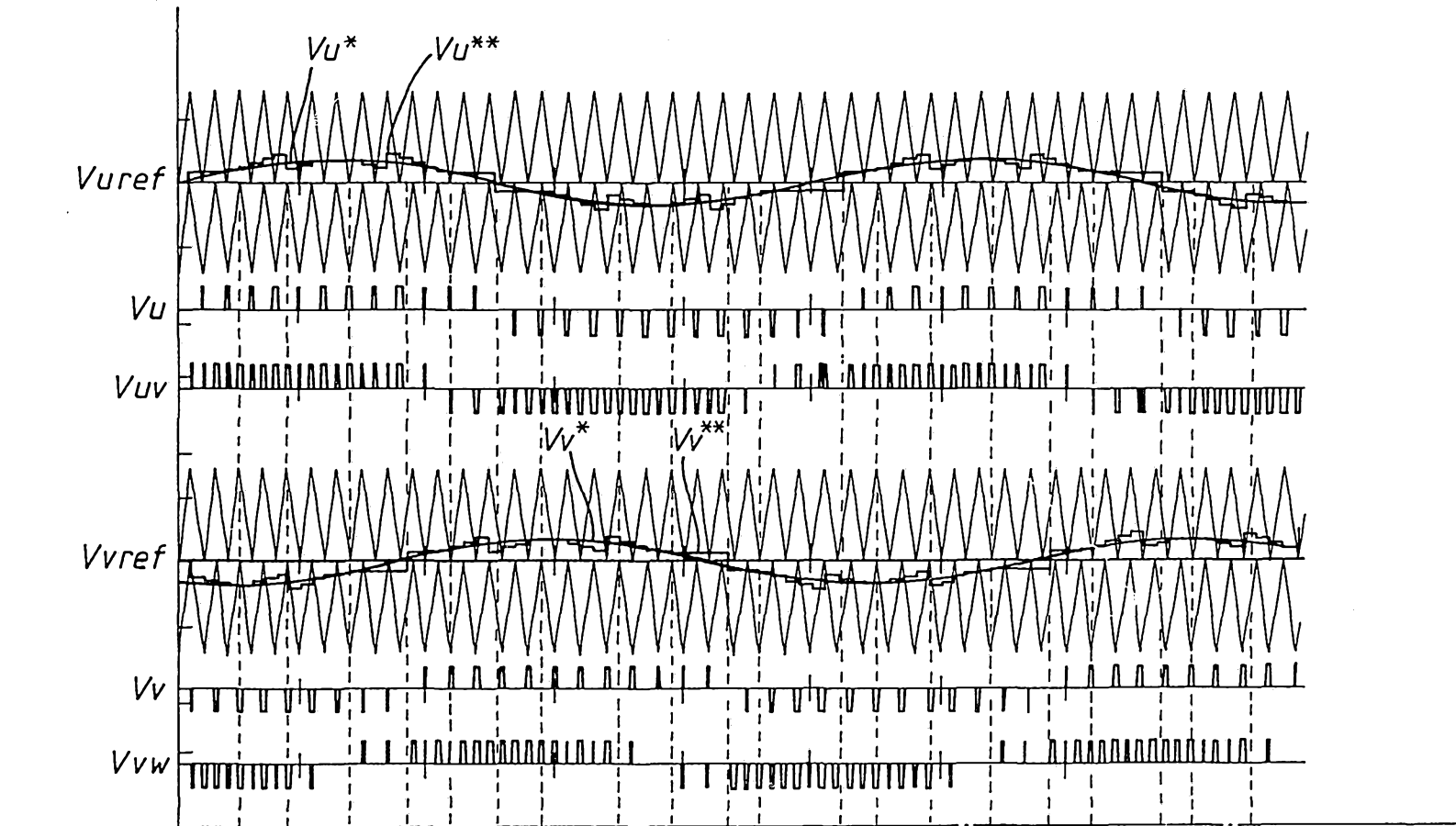


Fig. 7.

3000 315

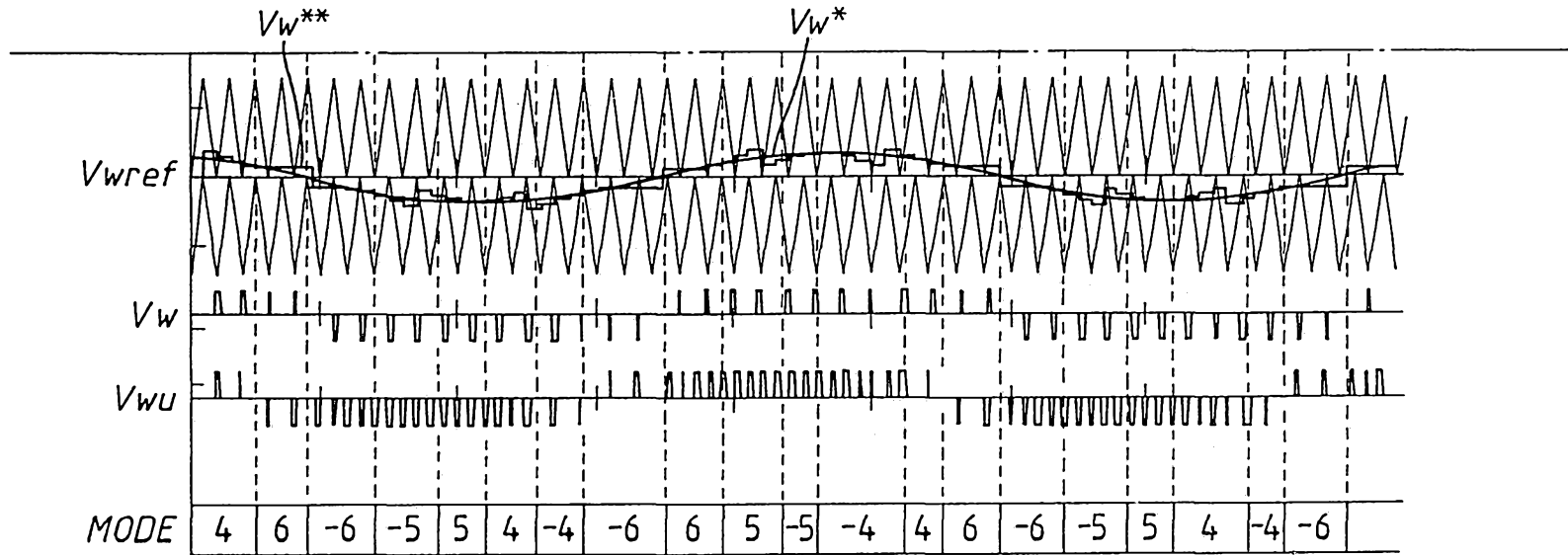


Fig. 7(cont.)

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30093 3199

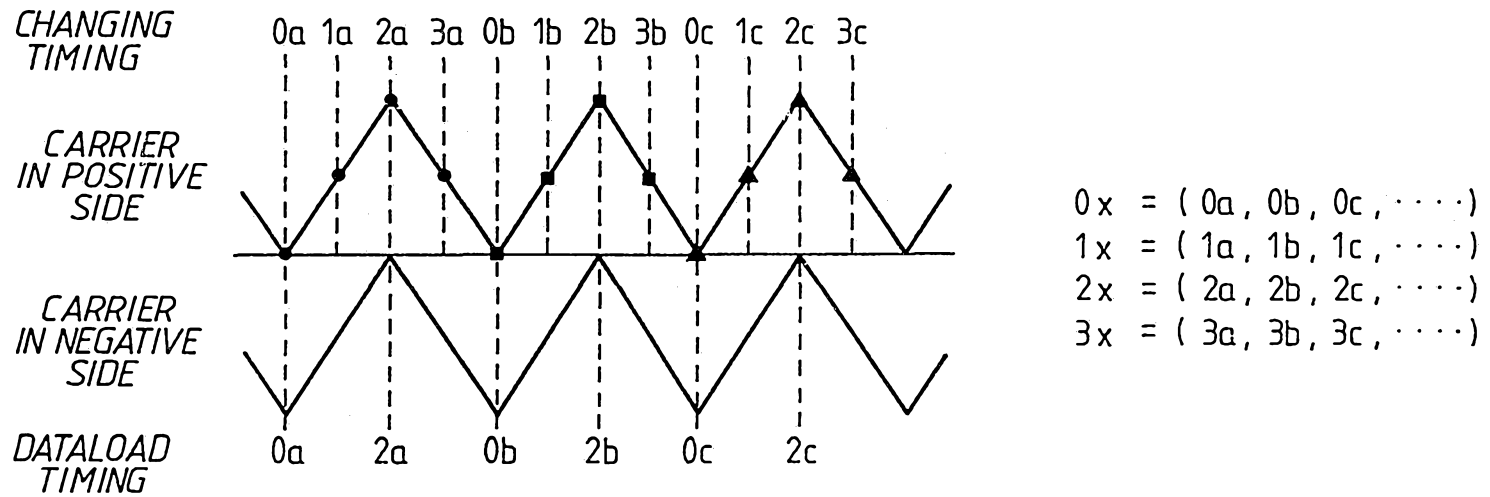


Fig.8.

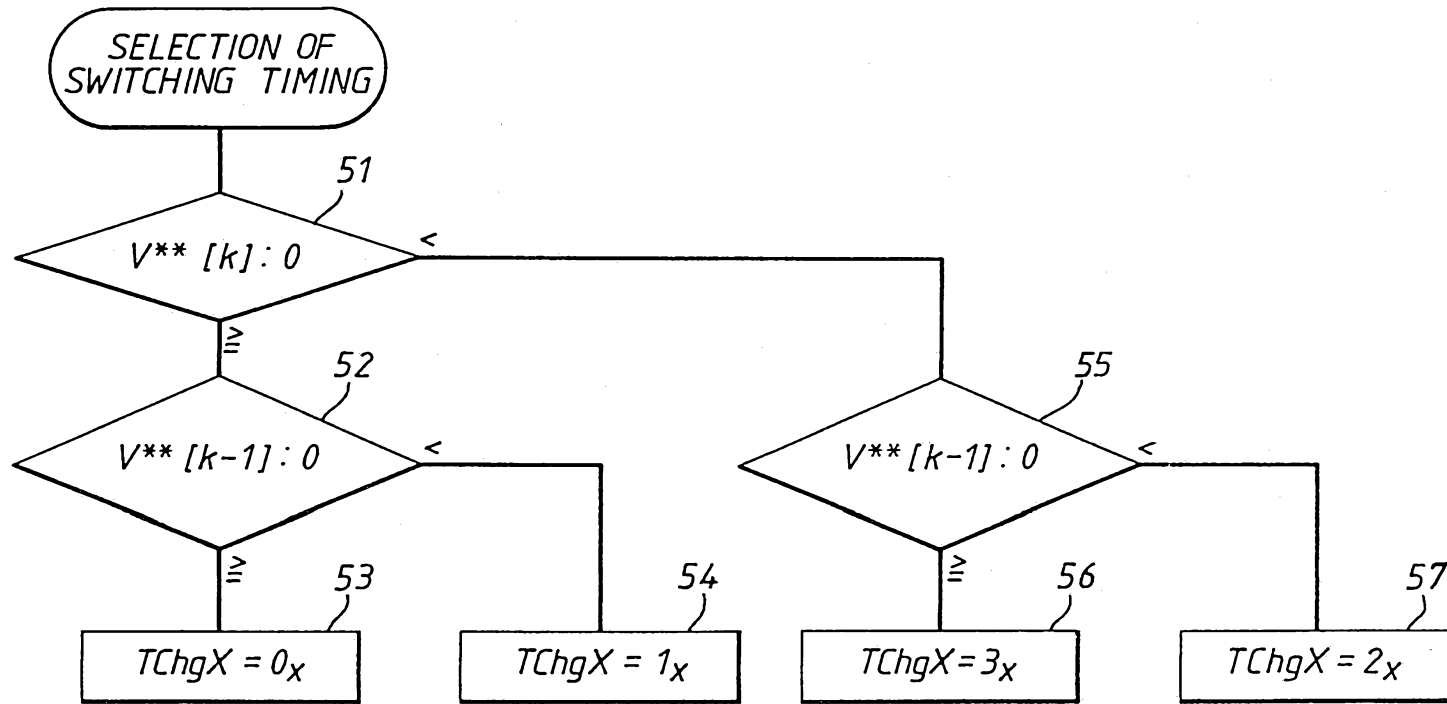


Fig. 9.

3000 3000

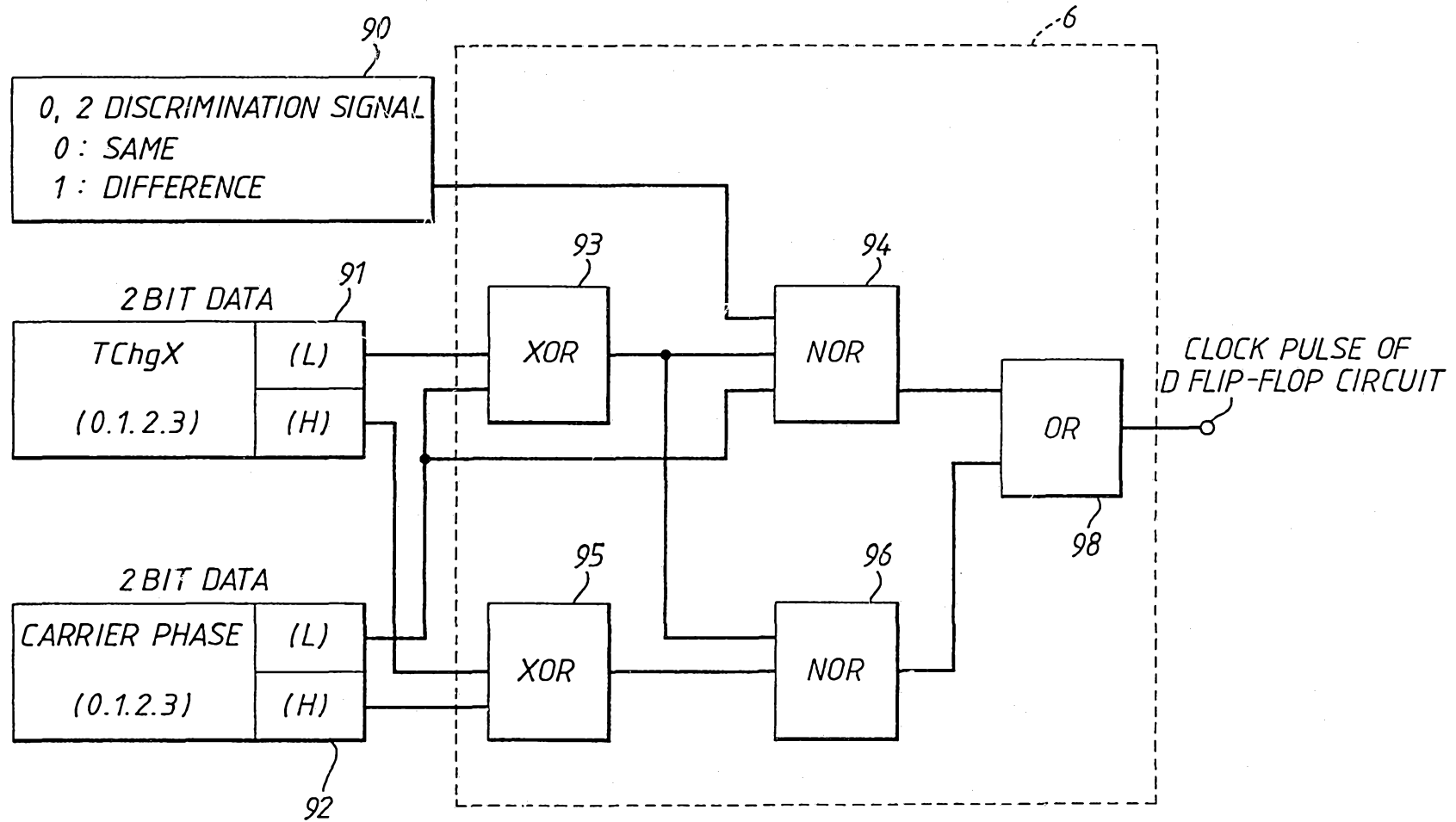


Fig.10.

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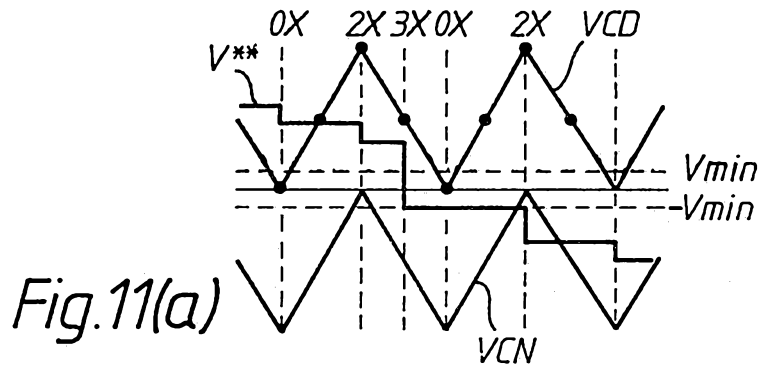


Fig. 11(a)

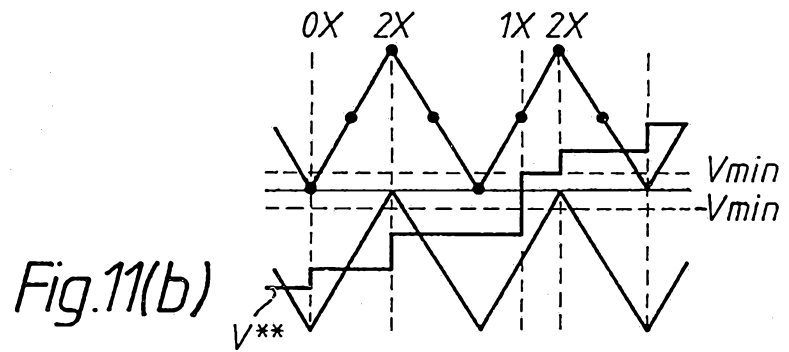


Fig. 11(b)

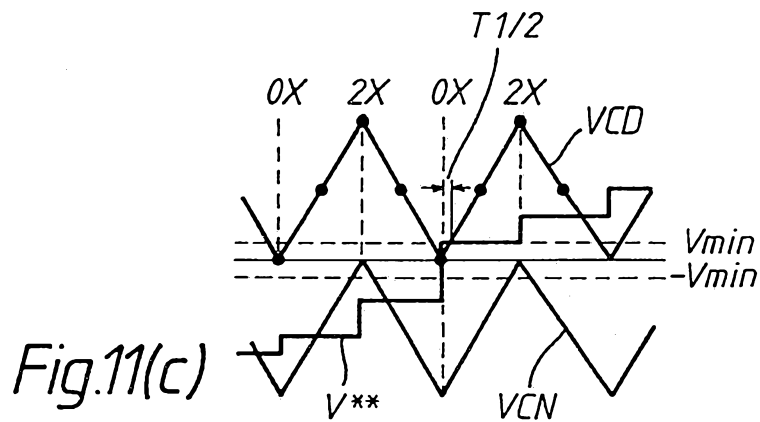


Fig. 11(c)

PULSE IS EQUAL TO A MINIMUM ON PULSE WIDTH OR LESS

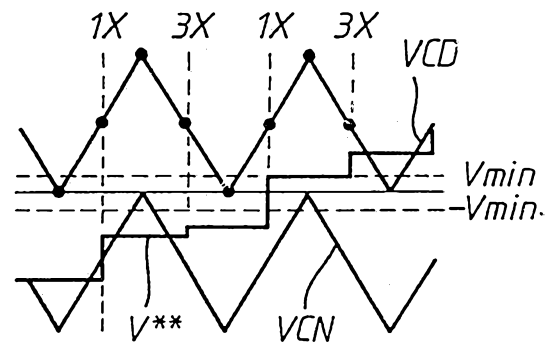


Fig. 11(d)

PULSE IS EQUAL TO A MINIMUM ON PULSE WIDTH OR LESS

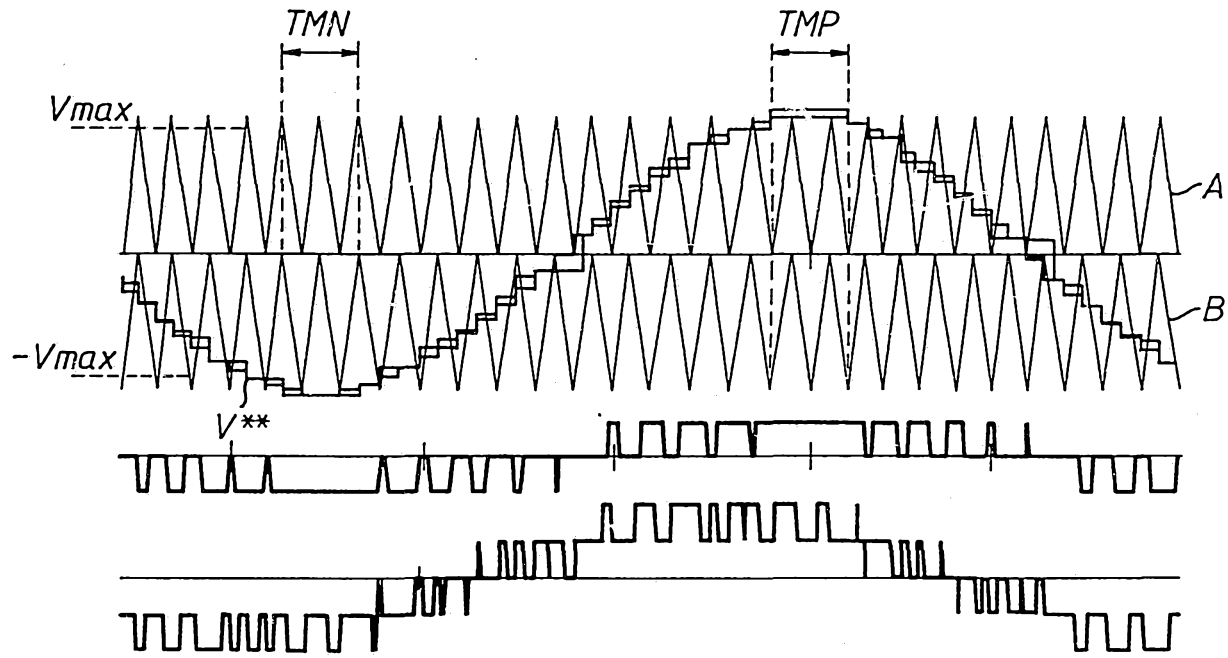


Fig.11(e)

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3003 3195

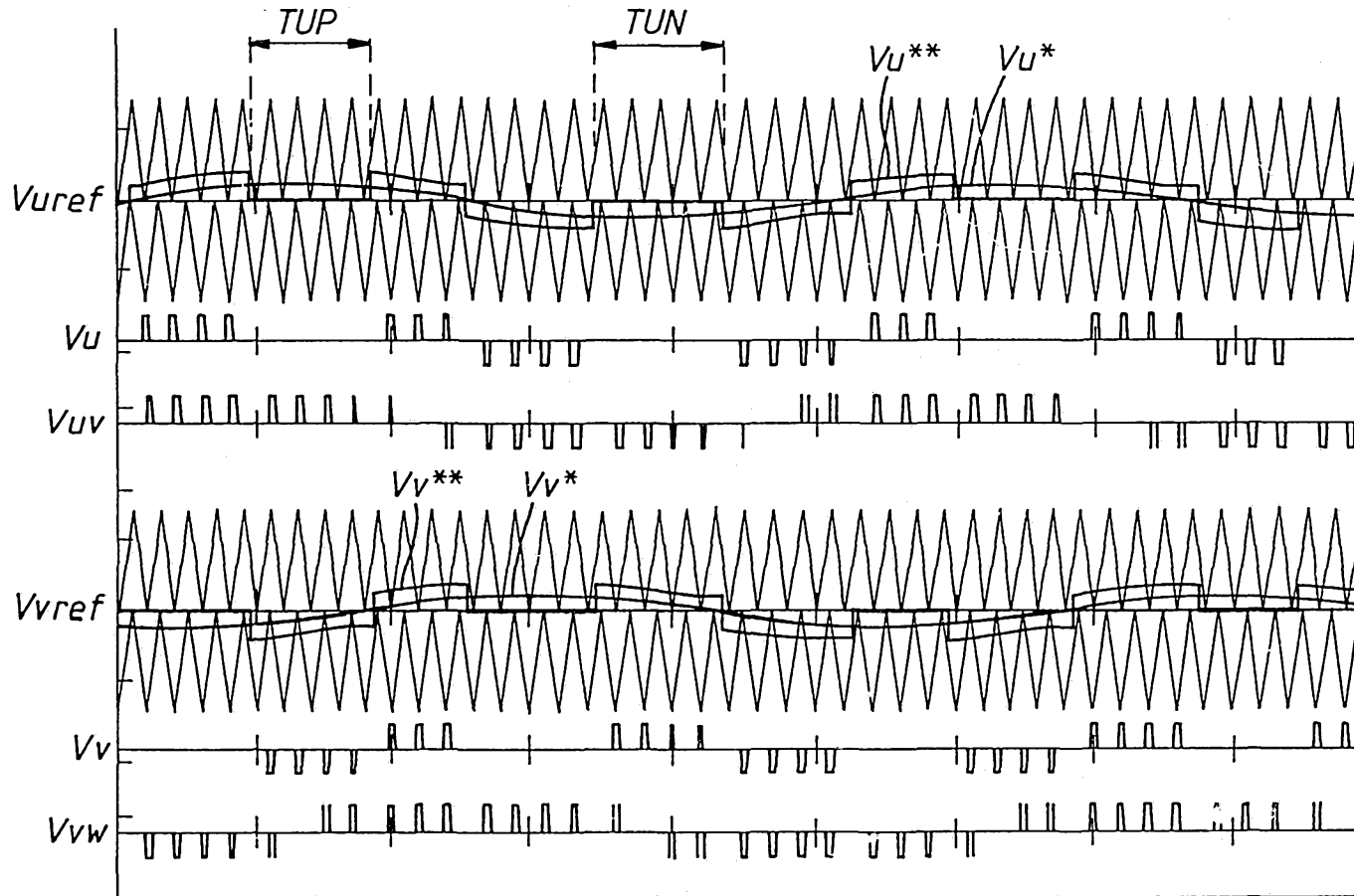


Fig.12.

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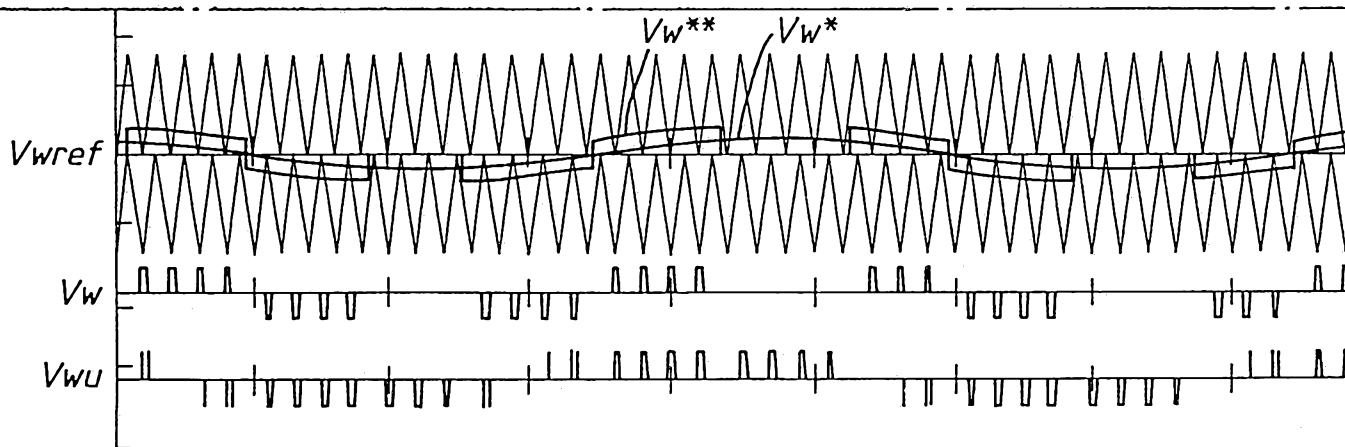


Fig.12(cont.)

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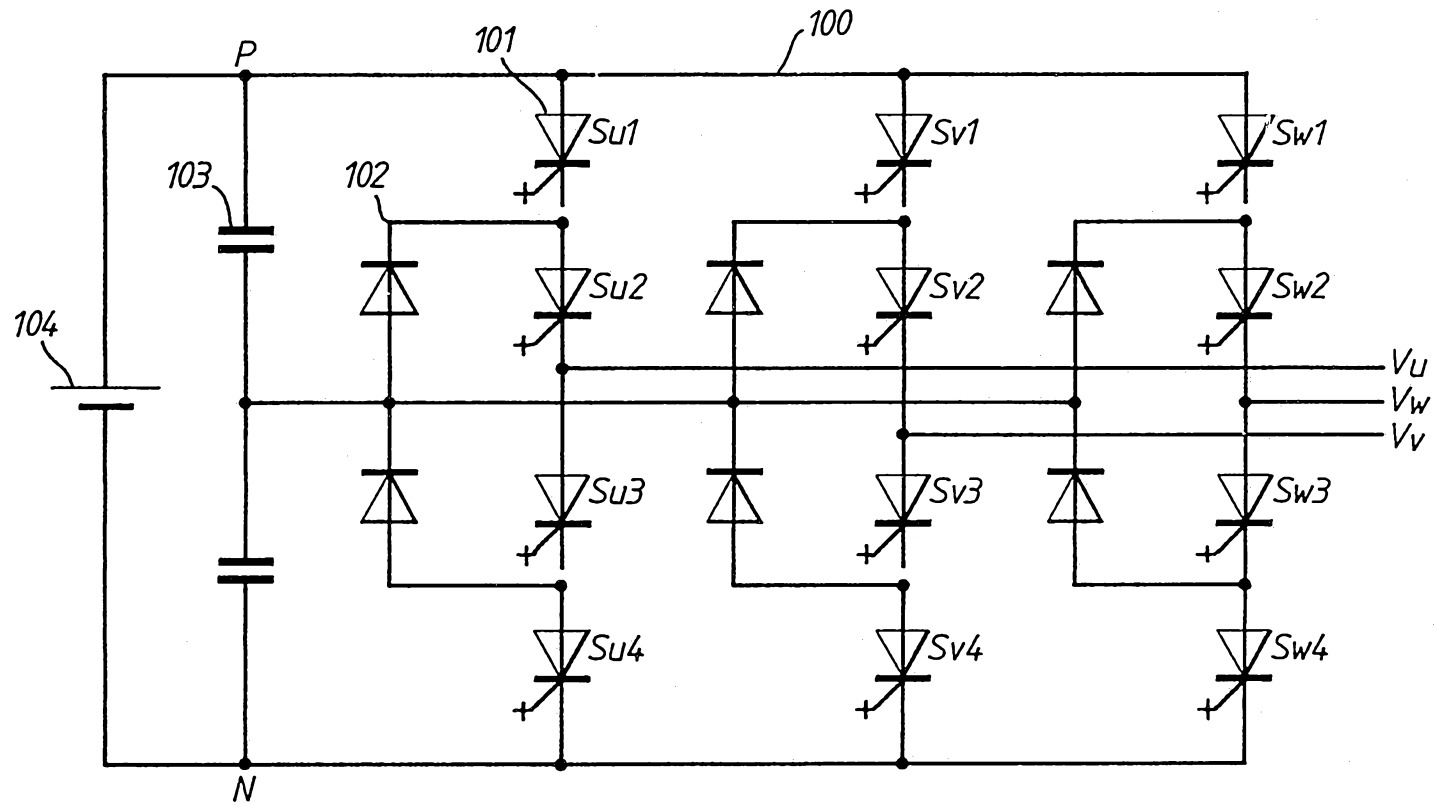
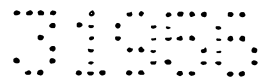


Fig.13.

3 1 5 3 1 5 5

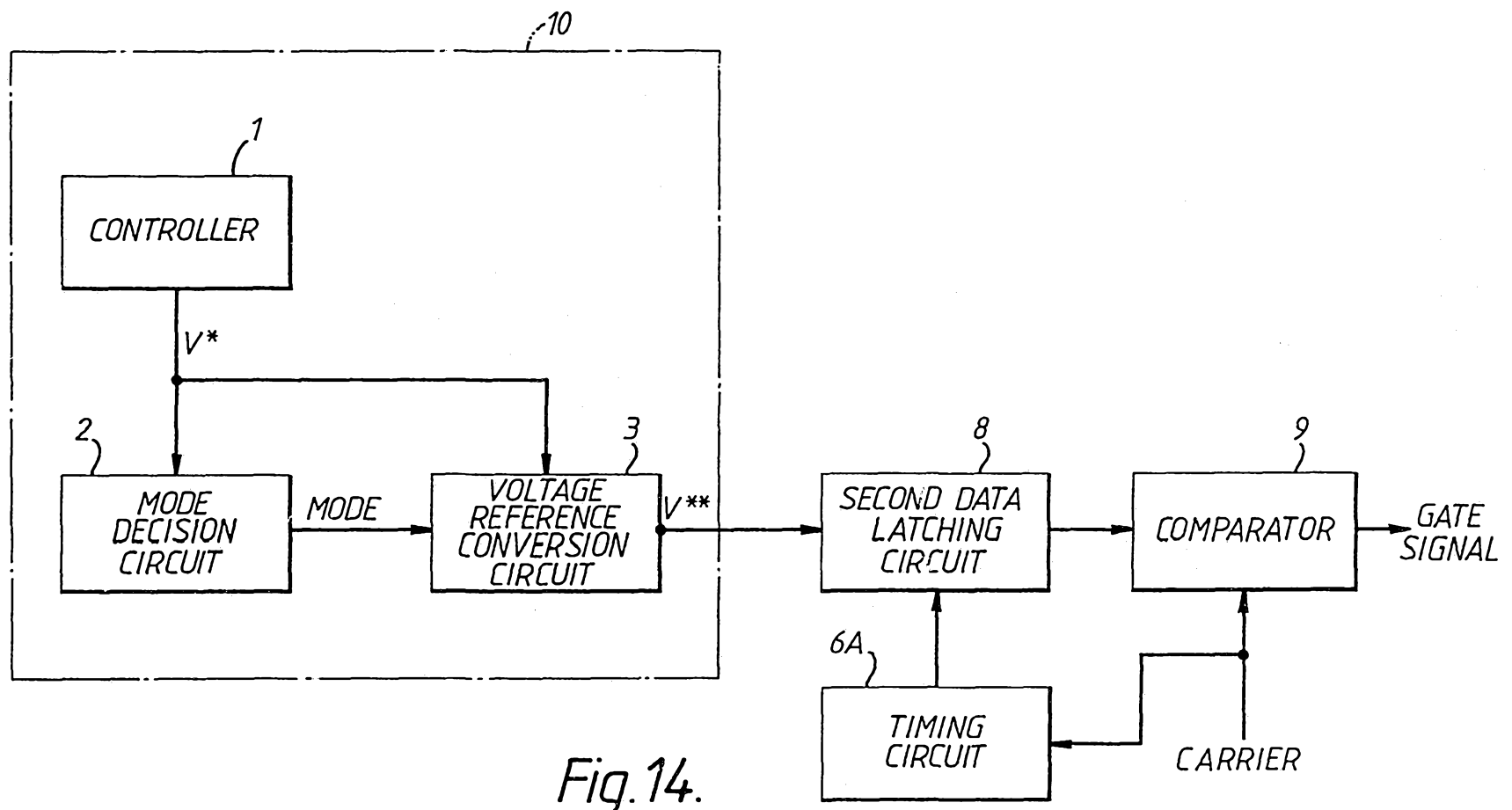


Fig. 14.

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3005 3195

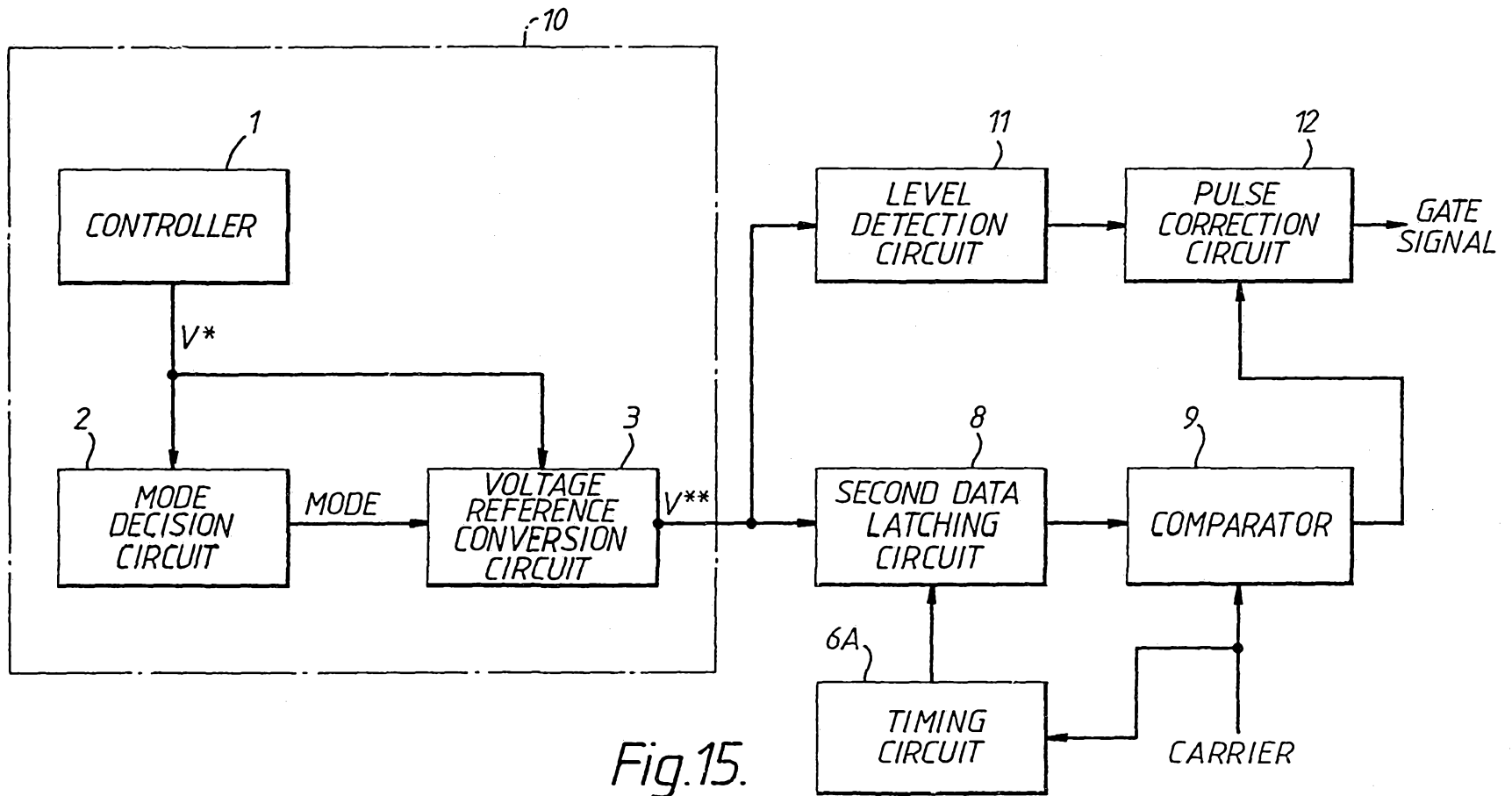


Fig.15.

3055 3055

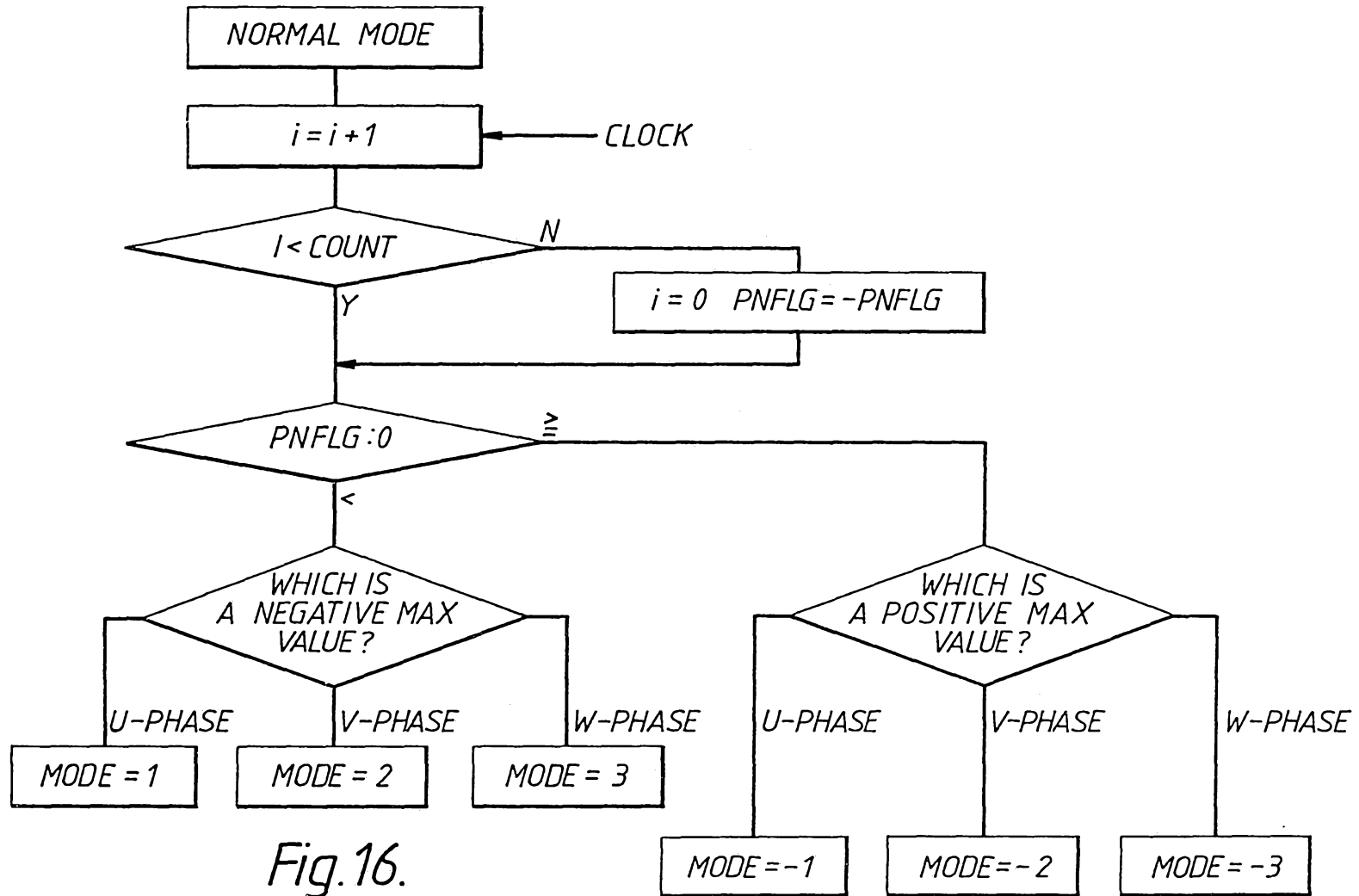
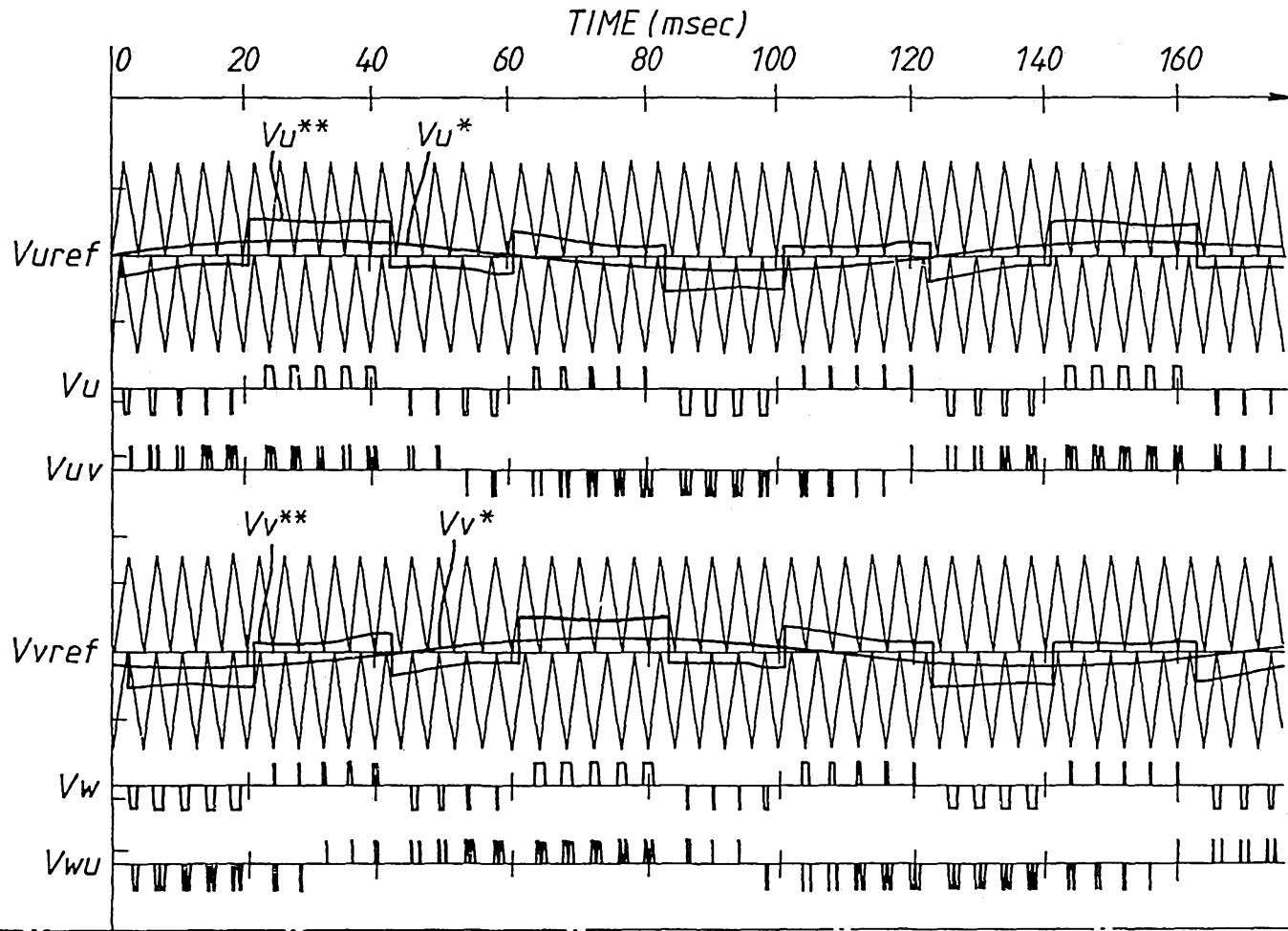


Fig. 16.

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3 1 3 5 5



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Fig.17.

2000 3100

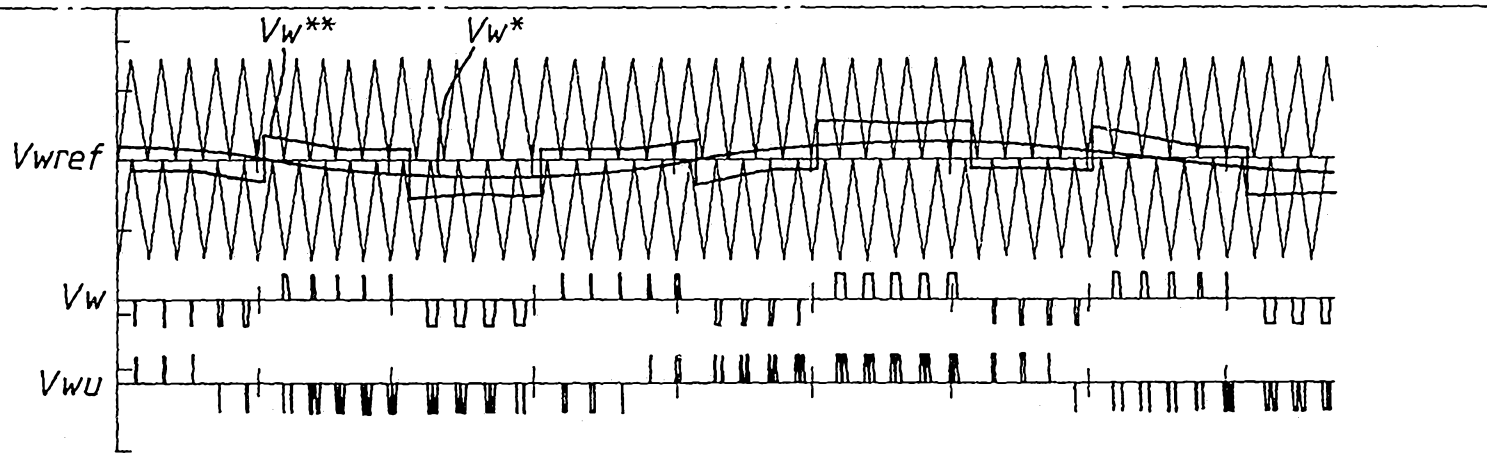
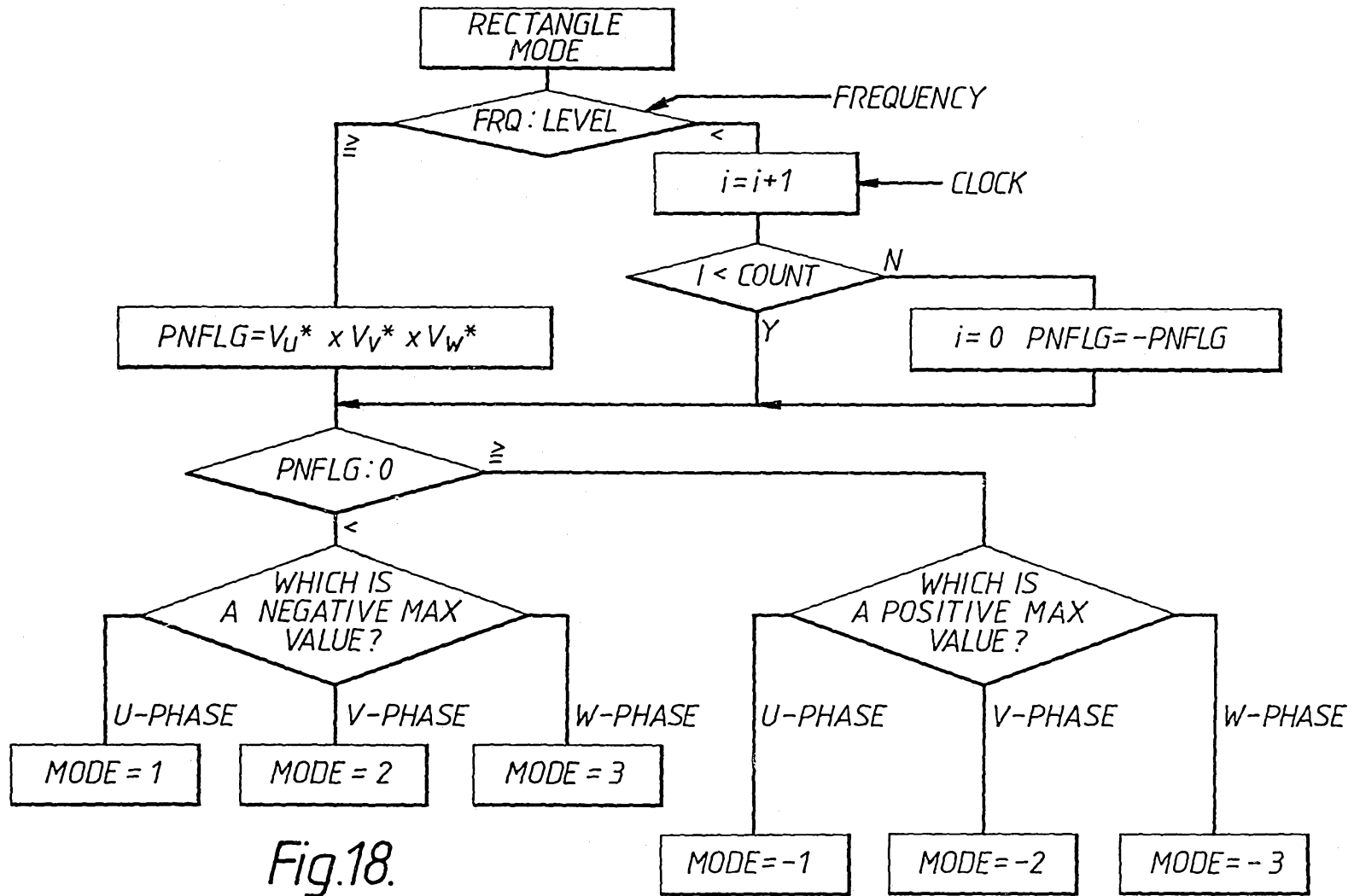


Fig.17(cont.)

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3000 3000



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Fig.18.

3000 0000

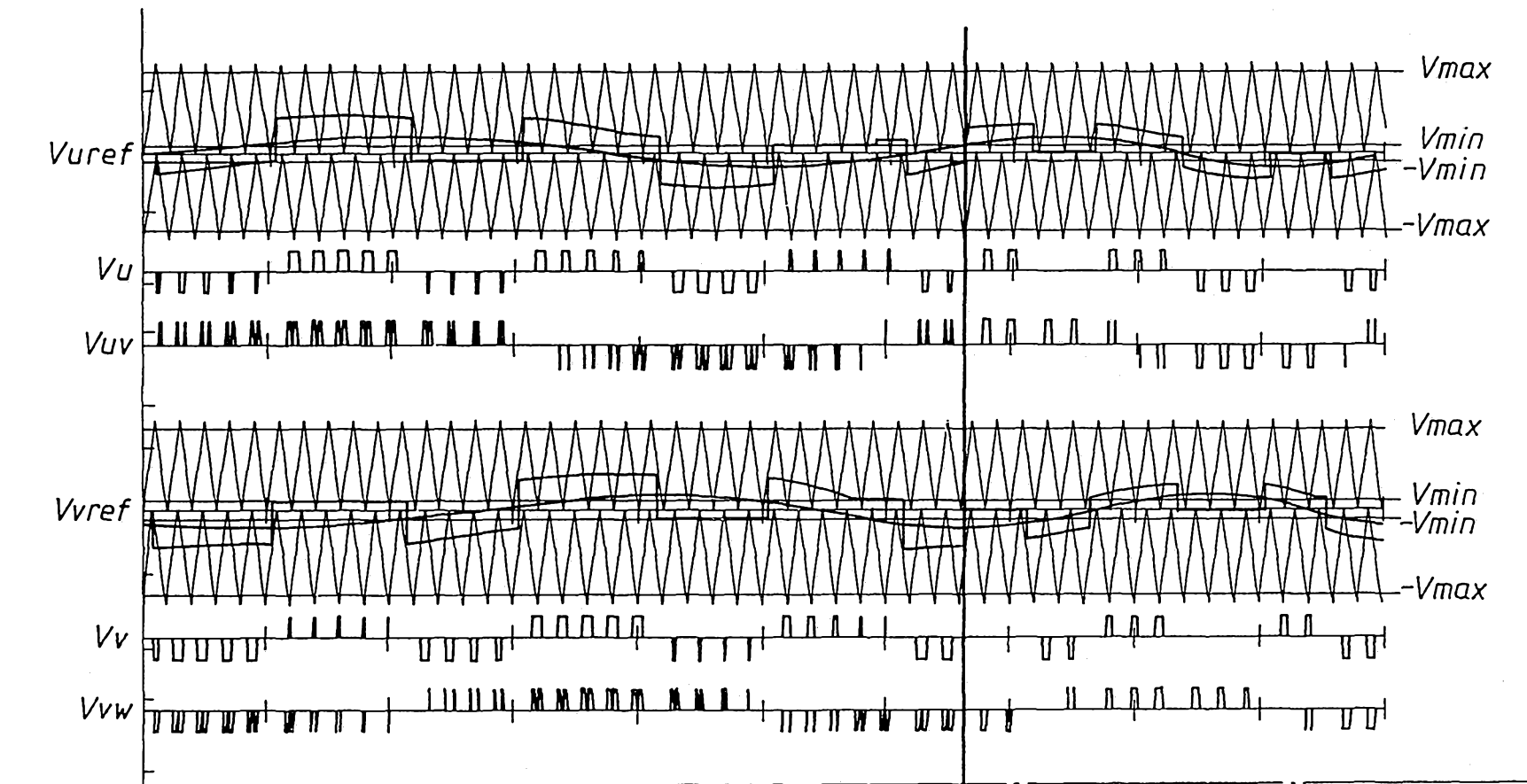


Fig.19.

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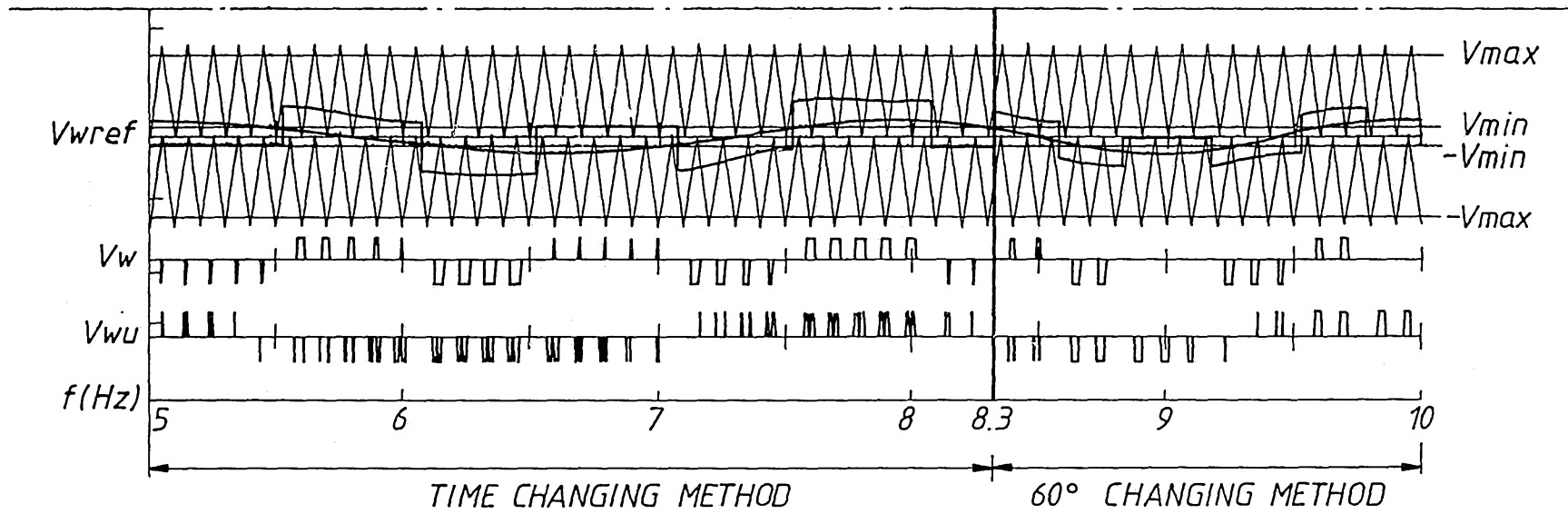


Fig.19(cont.)

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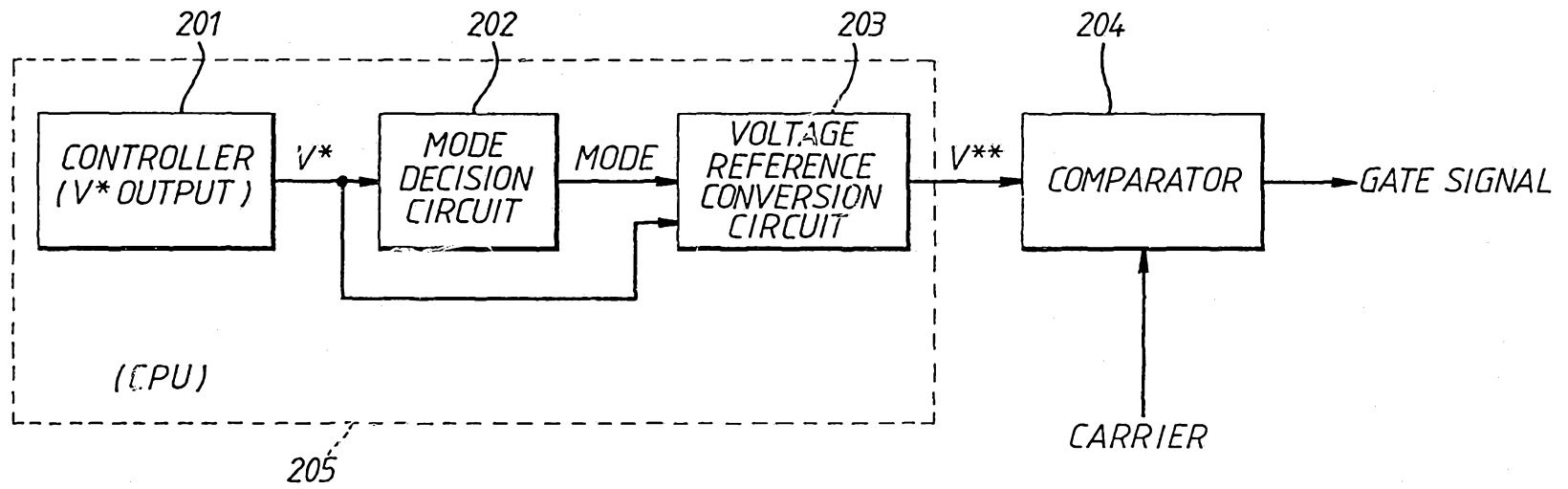


Fig. 20.

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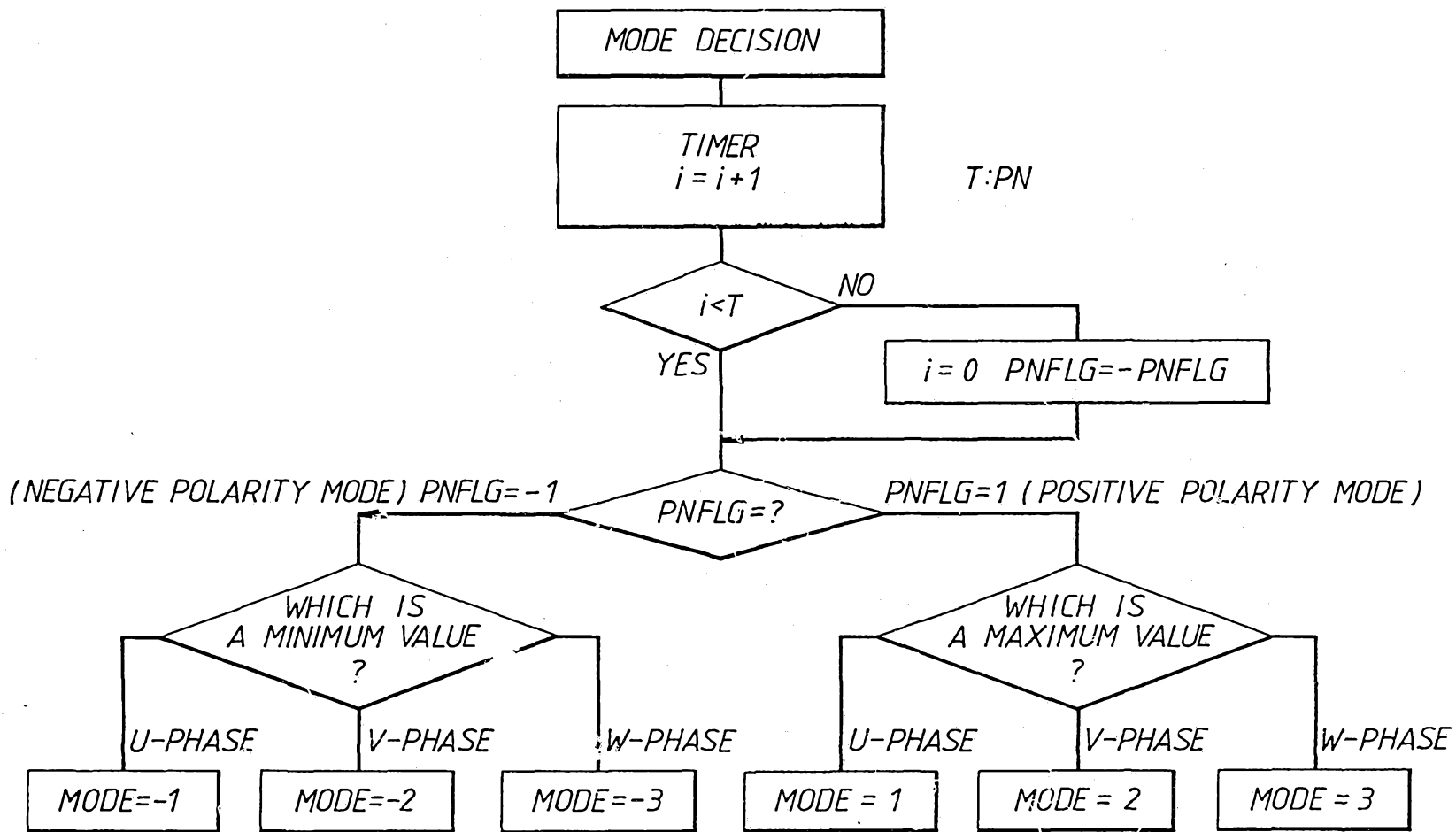
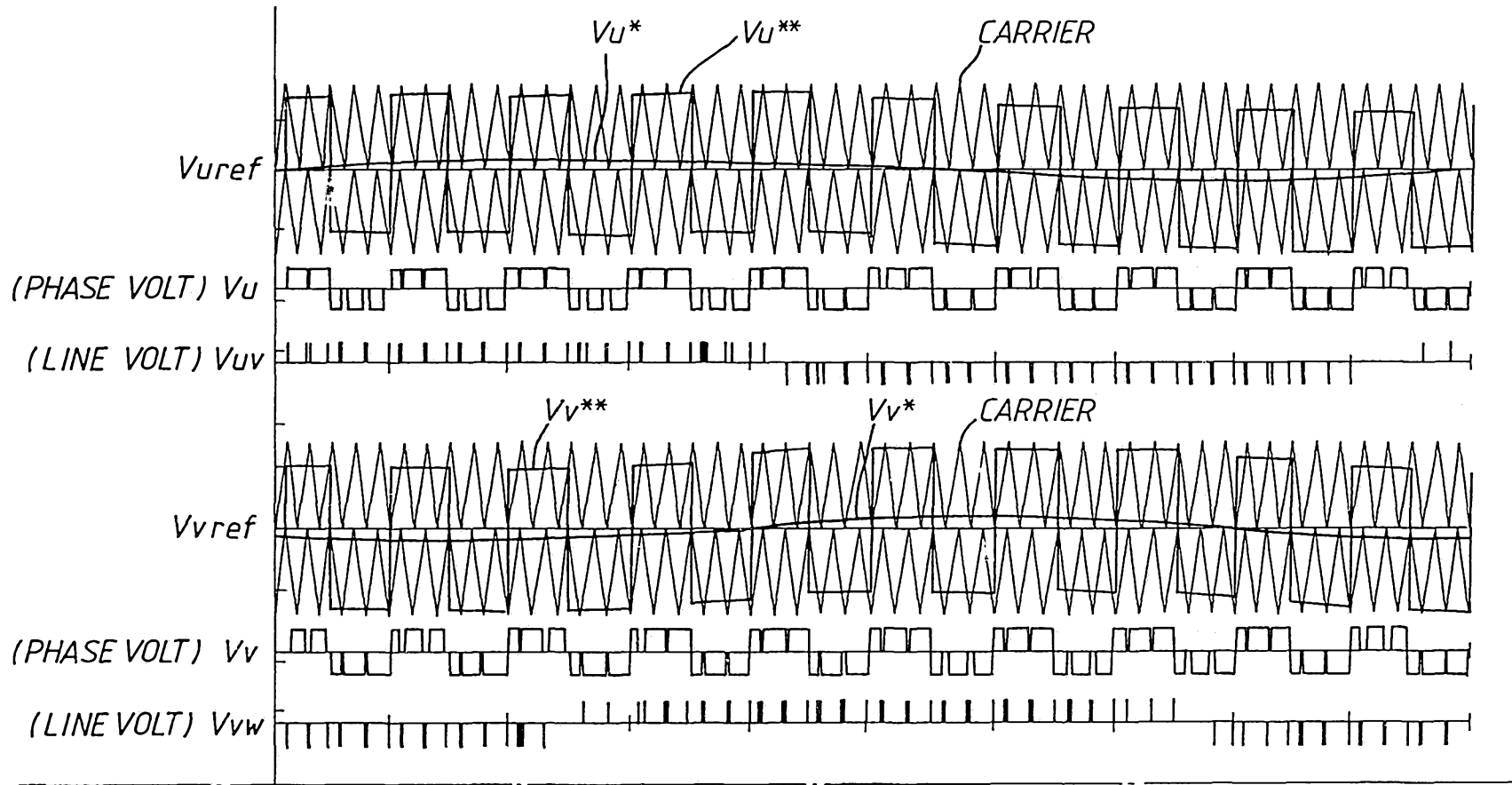


Fig. 21.

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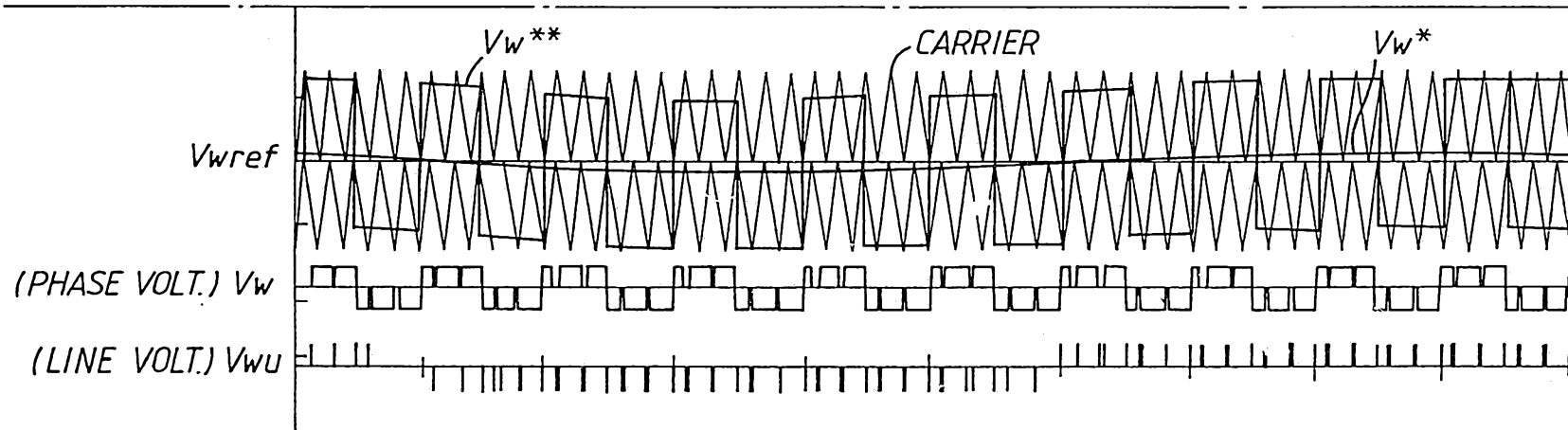
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Fig.22.

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Fig.22(cont.)

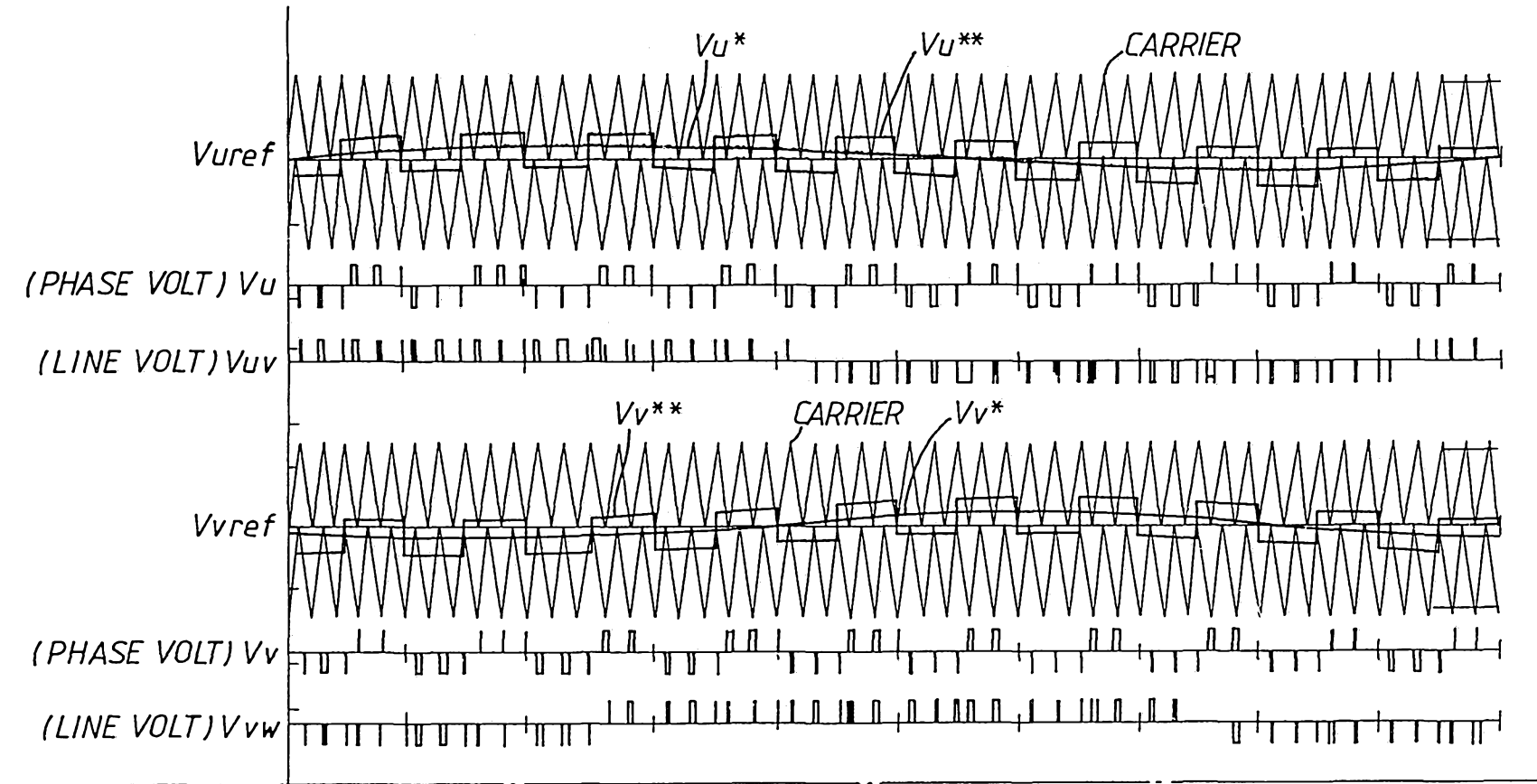


Fig.23.

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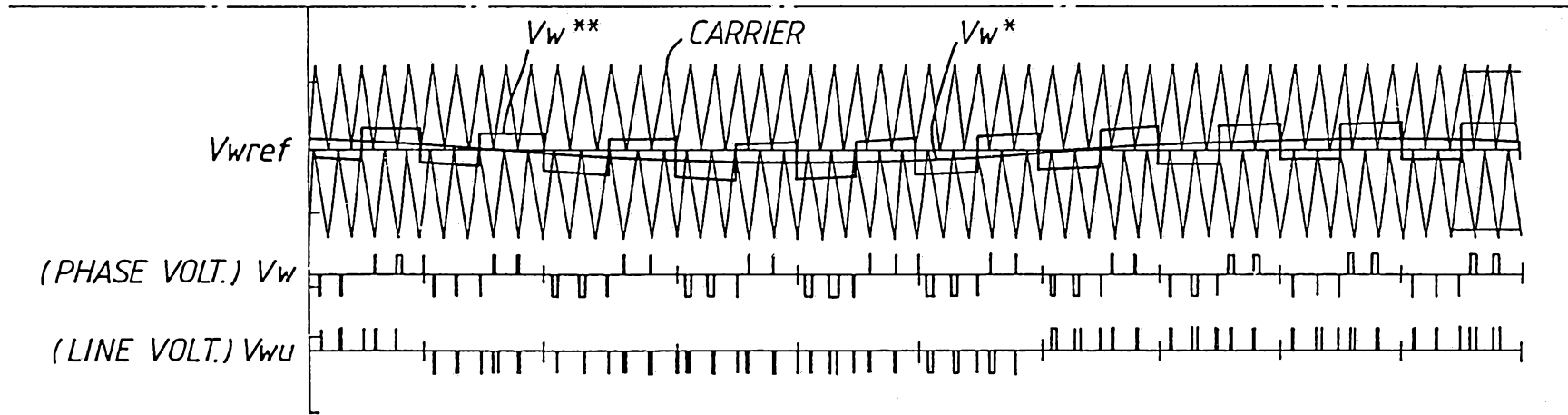


Fig.23(cont.)