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[54] SETUP SYSTEM IN ANALOG COMPUTER

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Dec. 27, 1968 Japan.....43/95342

[52] **U.S. Cl.**.....**235/183,** 235/180, 235/184, 235/193

[51] **Int. Cl.**.....**G06g 7/18,** G06g 7/36

[58] **Field of Search**.....235/180, 182, 183, 193, 197, 235/184

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Primary Examiner—Joseph F. Ruggiero

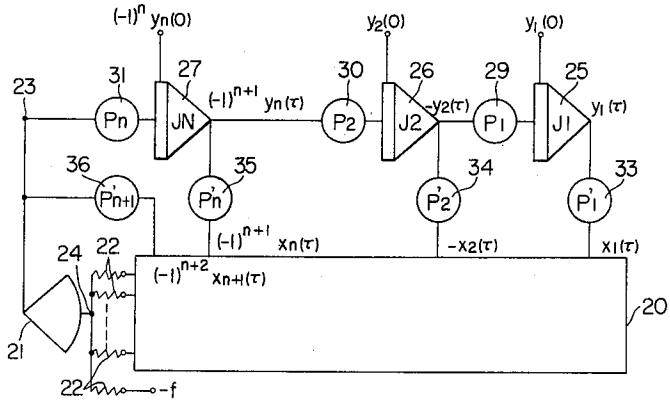
Attorney—Robert E. Burns and Emmanuel J. Lobato

[57] **ABSTRACT**

A setup system in an analog computer wherein a group of potentiometers are inserted in the input sides of an integrator provided in the computer corresponding to the variables in an equation to be solved, and another group of potentiometers are inserted in the output sides of the integrators so that the factors for the time and amplitude employed for the variables can be controlled separately and in a unitary manner.

In another aspect of the invention, a dummy variable is introduced by an additional provision of an integrator, whereby the solution of an equation having a coefficient which tends to be infinitive at a time instant within a range for which the equation is to be solved is much facilitated.

5 Claims, 5 Drawing Figures



PRIOR ART FIG. 1

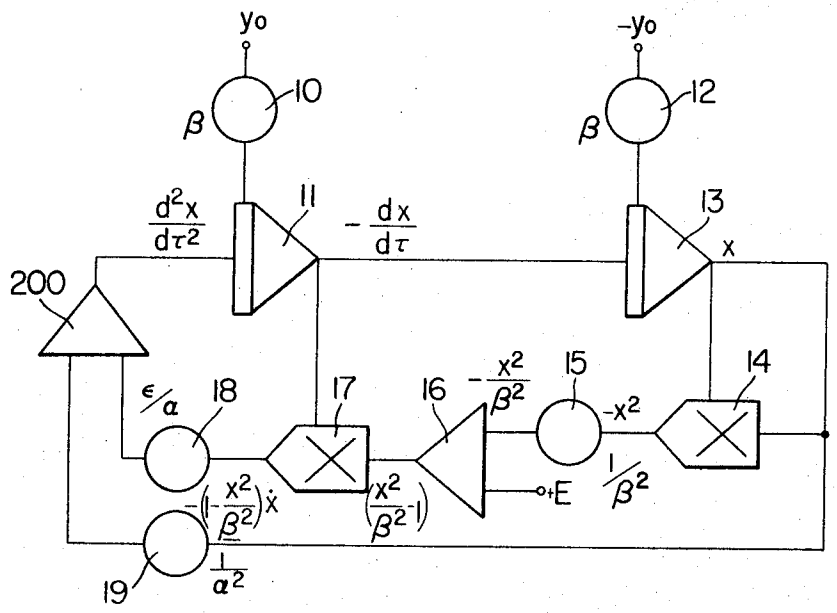


FIG. 2

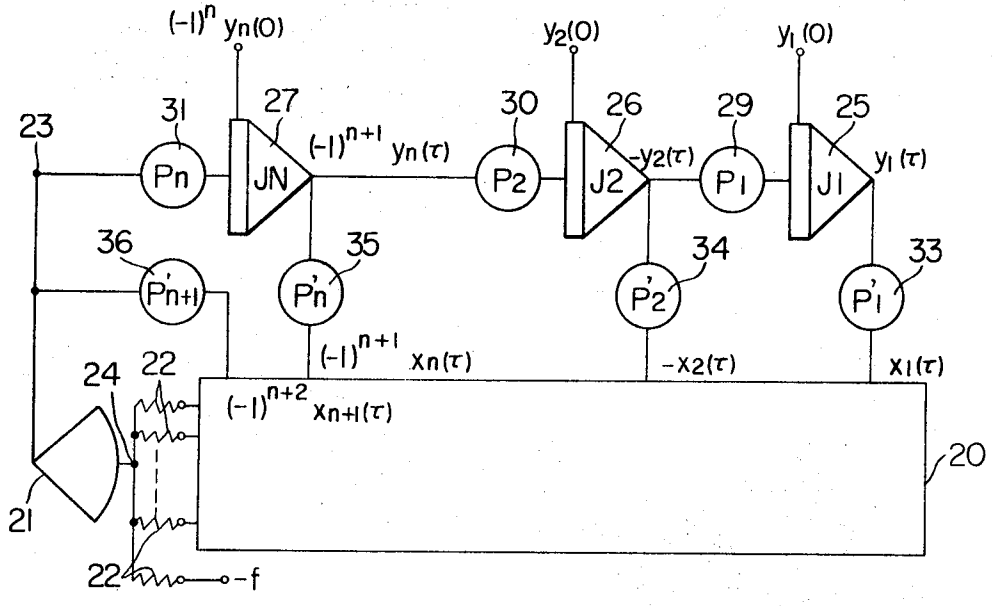
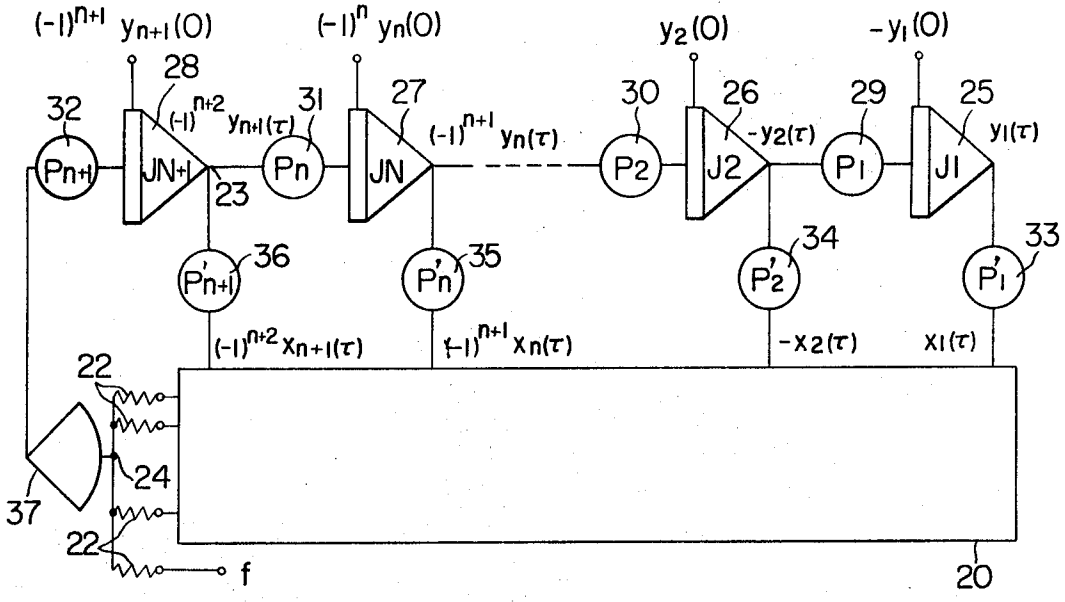


FIG. 3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$(-1)^{n}$ $y_n(0)$
$y_2(0)$
$-y_1(0)$
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30
26
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$(-1)^{n+2}$ $y_{n+1}(\tau)$
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$y_1(\tau)$
P_{n+1}
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P_n
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J_2
P_1
J_1
36
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P'_{n+1}
P'_n
P'_2
P'_1
$(-1)^{n+2} x_{n+1}(\tau)$
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$x_1(\tau)$
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f
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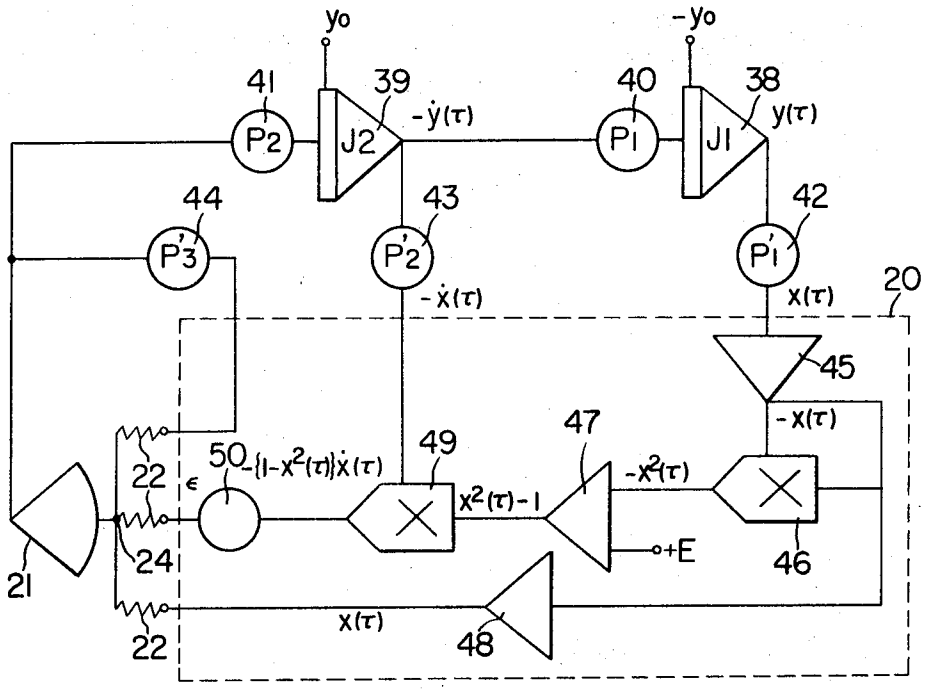
FIG. 4


y_o
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P'_2
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$-\dot{x}(\tau)$
$x(\tau)$
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$-x(\tau)$
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$\{1-x^2(\tau)\}\dot{x}(\tau)$
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$x(\tau)$
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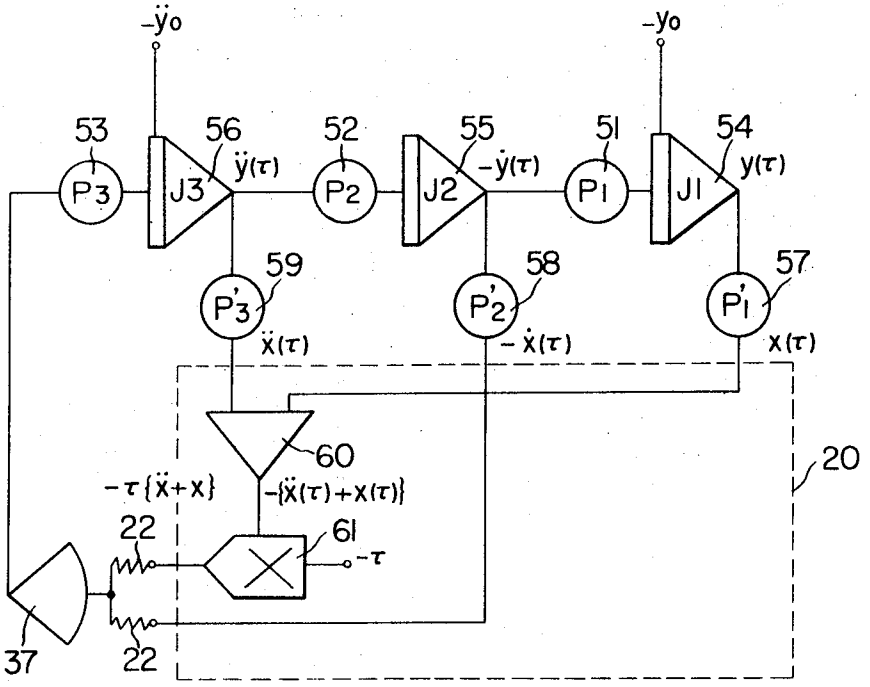
FIG. 5


-ÿo
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P'3
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-{ẍ(τ)+x(τ)}
22
61
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22

SETUP SYSTEM IN ANALOG COMPUTER

BACKGROUND OF THE INVENTION

This invention relates generally to analog computers and more particularly to a setup system in an analog computer wherein the time scale factor and the amplitude scale factor are introduced separately, so that a linear or nonlinear ordinary differential equation can be solved in a simple and systematic manner.

Heretofore, it has been the general practice in solving a given equation in an analog computer to solve the equation by employing and combining various computing elements in the computer in such a manner that the output voltages thereof correspond to respective variables in the equation.

However, the frequency responses of the variables in an equation to be solved vary in a wide range, and the magnitudes of the coefficients and the variables thereof are also distributed in a wide range. There are, of course, limitations to such magnitudes and frequency ranges realizable by the analog computing elements which are employed for solving the equation.

For this reason, a time scale factor α and an amplitude scale factor β are introduced into the equation to be solved, and the above described magnitudes and frequency ranges must be reduced to those values falling within limits which can be handled by the analog computing elements. In the conventional practice, the factors α and β have been determined by "trial and error" during the solution of the equation in an analog computer.

However, in the conventional setup systems in analog computers, the time scale factor α and the amplitude scale factor β are dealt with in various forms in each of the potentiometers, so that they must be adjusted individually, whereby it has not been convenient in determining the factors α and β in the "trial and error" procedure. For example, the time scale factor α and the amplitude scale factor are not included in each potentiometer in a $1\alpha\beta$, $1\beta^2$ 1α and $1\alpha^2$. Furthermore, when a term of the highest order derivative in the equation is expressed with the other terms including the coefficient of the highest order derivatives, and an outer forcing term, the equation thus setup in the analog computer is expressed in a form such that the right-hand side of the equation has a divisor consisting of the coefficient of the highest order derivative in the original equation. Accordingly, if the coefficient of the highest order derivative in the original equation tends to become zero at an instant $t = t_1$, the coefficients of other terms in the newly setup equation, defined in a region including t_1, approach infinity (∞) as the value of t approaches t_1.

For this reason, when such an equation is to be solved in a computer, special care must be exercised so that the coefficients of these terms are not caused to become infinity.

SUMMARY OF THE INVENTION

Therefore, the primary object of the present invention is to provide a novel setup in an analog computer whereby the above described inconveniences in the conventional setup can be completely eliminated.

Another object of the present invention is to provide a novel setup system in an analog computer wherein a time scale factor and an amplitude scale factor are introduced separately in such a manner that the required response frequencies and amplitudes thereof may fall within the range allowable in the analog computer and also in the associated apparatuses.

Still another object of the present invention is to provide a novel setup system which is so organized that the time scale factor α and the amplitude scale factor β are introduced separately therein and can be controlled independently of one another, and all of the linear and nonlinear ordinary differential equations which are expressed by employing these scale factors can be handled in a unitary manner.

These and other objects of the present invention can be achieved by a novel setup system in an analog computer, wherein a number of integrators corresponding, respectively, to the variables in an equation to be solved and means for separating the time and the amplitude scale factors thereof are provided, and an improvement wherein the means for dealing separately with the scale factors comprise a first group of potentiometers each disposed at the input side each of the integrators so that a time scale factor α may be introduced in all of the variables, and a second group of potentiometers each inserted in the respective loops in the output side of each integrator so that new variables incorporated with an amplitude conversion factor β are obtained; all of the terms, except the forcing term, of the equation to be solved are expressed with these variables; all of the terms thus expressed in new variables and also the forcing term are gathered at the input side of an operational amplifier; and a feedback loop is formed around the operational amplifier for producing a new coefficient related to the original coefficient of the highest order derivative in the equation to be solved, whereby the time scale factor and the amplitude scale factor thus introduced or converting the variables of the equation can be controlled in a unitary manner by controlling the first and second groups of the potentiometers.

In another aspect of the invention, the setup system may also be composed in such a manner that a dummy variable is provided so that it consists of a derivative of an order higher than that of the highest order derivative in the equation; a time conversion factor is introduced in all of the variables of the equation and also in the dummy variable by the provision of a group of potentiometers in the input circuits of integrators provided corresponding to the variables and the dummy variable; an amplitude scale factor is also introduced by disposing a second group of potentiometers in the loops formed at the output sides of the integrators in such a manner that new variables incorporating the amplitude scale factor are formed through the use of the outputs of the integrators; all of the terms in the equation except a forcing term are then expressed by utilizing the new variables; the terms thus expressed and the forcing term are collected on an input summing point of a high gain amplifier of adjustable gain; and a loop is formed around the amplifier so that the output of the amplifier or a signal obtained from the output by reversing a sign of the output is fed back to the input side of the amplifier for stabilizing the operation, whereby the time scale factor and the amplitude scale factor thus introduced in the equation can be controlled in a unitary manner by controlling the first and second groups of the potentiometers.

The nature, principle, and the utility of the invention will be more apparently understood from the following description when read in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

In the drawings:

FIG. 1 is a schematic diagram showing an example of the conventional setup in an analog computer which is employed in solving "van der Pol's differential equation";

FIG. 2 is a schematic diagram showing the principle of a basic setup in an analog computer in accordance with the present invention;

FIG. 3 is a schematic diagram showing the principle of another setup according to the present invention wherein the basic setup shown in FIG. 2 is somewhat expanded;

FIG. 4 is a schematic diagram showing another example of the setup according to the present invention which is applied for solving "van der Pol's differential equation"; and

FIG. 5 is a schematic diagram showing still another example of the setup according to the present invention which is applied for the solution of "Bessel Functions of zero order".

DETAILED DESCRIPTION

The organization of the present invention will be more apparent when the setup according to the invention is compared with the conventional setups some of which are indicated in the following Examples.

EXAMPLE 1.

Van der Pol's differential equation

$$\frac{d^2y}{dt^2}-\epsilon(1-y^2)\frac{dy}{dt}+y=0 \quad (1)$$

is to be solved under the initial conditions of $y(\mathbf{O}) = yo$ and $y'(0) = y'o$, the time scale factor α and the amplitude scale factor β being selected as

$$\tau=\alpha t \text{ and } x=\beta y \quad (2)$$

When these values are substituted in Equation (1) and Equation (1) is rearranged for $d^2x/d\tau^2$

$$\frac{dx}{d\tau^2}=\left(1-\frac{x^2}{\beta^2}\right)\frac{1}{\alpha}\frac{dx}{d\tau}-\frac{1}{\alpha^2}x \quad (1)'$$

is obtained. Equation (1)' can be solved by a setup in an analog computer as shown in FIG. 1, wherein reference numerals **11** and **13** designate integrators, the output signals thereof being $-dx/d\tau$ and x respectively, numerals **16** and **200** are summing amplifiers, the output signals thereof being

$$\left(\frac{x^2}{\beta^2}-1\right) \text{ and } \frac{d^2x}{d\tau^2}$$

respectively. The reference numerals **10**, **12**, **15**, **18**, and **19** designate potentiometers, the values thereof being β, β, $1/\beta^2$, ϵ/α, and $1/\alpha^2$ respectively. It will be apparent from FIG. **1** that the setup in the conventional practice has had a complicated organization. Example **2**.

A Bessel's differential equation of the 0-th order

$$t\frac{d^2y}{dt^2}+\frac{dy}{dt}+ty=0 \quad (3)$$

is to be solved under the initial conditions of

α and β are selected as shown in Equation (2), whereupon Equation (3) can be rearranged as follows.

$$\frac{dx}{d\tau^2}=-\frac{1}{\tau}\frac{dx}{d\tau}-\frac{1}{\alpha^2}x \quad (3)'$$

However, it is difficult to solve this Equation (3)' from the instant of $\tau = 0$ for the reason that the coefficient $-1/\tau$ for the first term in the right-hand side of the equation (3)' becomes infinity ∞) for the value of $\tau = 0$.

As is apparent from Example **1**, the conventional setup has been inconvenient for determining the time scale factor α and the amplitude scale factor β by the "trial and error" procedure.

Furthermore, as is the case of the Bessel's differential equation of Example 2, wherein there is included a point at which the coefficient of the highest order derivative term becomes zero, the equation could not be solved unless some special method adapted to the nature of the equation were employed.

According to the present invention, the above described drawbacks can be eliminated. FIG. **2** shows a basic setup according to the present invention which is applied in the solution of an ordinary differential equation of nth order:

$$a_{n+1}\,y_{n+1}(t)+a_n\,y_n(t)+\text{- - - - -}+a_1\,y_1(t)=f \quad (4)$$

wherein,

$$y(t)=\frac{d^{i-1}y(t)}{dt^{i-1}},\ i=1-(n+1)$$

under the initial conditions of $y_n(0), y_{n-1}(0), \ldots, y_1(0)$.

In order that the responses of the variables $y_{n+1}(t)$, $y_n(t)$, $\ldots, y_1(t)$ (5)

in equation (4) be delayed to $1/\alpha$, a new time axis, $\tau=\alpha t$, is adopted, whereby the variables (5) are converted to

$$y_{n+1}(\tau),\ y_n(\tau),\ \ldots,\ y_1(\tau) \quad (6)$$

The responses of these variables are delayed to $1/\alpha$ of the real responses with respect to the real time t. Accordingly, when it is desired to maintain the relations between all of the variables in (6) in an analog computer, the speed of the integrations must be decreased to $1/\alpha$.

For the realization of such relations, potentiometers P_1, P_2, ..., P_n, also designated by **29**, **30**, ... , **31**, respectively, are disposed on the input sides of integrators J_1, J_2, ..., J_n, also designated by **25**, **26**, **27**, ..., in FIG. **2**, so that the speed of the integrations therein is reduced to $1/\alpha$. In such an arrangement if a signal corresponding to $y_{n+1}(\tau)$ is applied to a circuit position **23** in FIG. **2**, $y_n(\tau)$, ..., $y_1(\tau)$ are obtained from the respective output terminals of the integrators, such as **27**, **26**, **25**. When the conversion ratio of potentiometers P'_{n+1} ....., P'_1, also designated by **36**, **35**, **34**, **33**, is selected to be α,

$$x_{n+1}(\tau),\ldots\ldots,x_1(\tau) \quad (7)$$

can be obtained from the output terminals of the potentiometers P'_{n+}, ..., P'_1.

When the left-hand side of Equation (4), namely, $a_{n+1}\,x_{n+1}(\tau)+a_n\,x_n(\tau)+\ldots..\,a_1\,x_1(\tau)$ is composed in a circuit **20** based on the variables (7) obtained from the output terminals of the potentiometers P'_n**n+1**, ..., P'_1, the left-hand side of the equation

$$\{a_{n+1}x_{n+1}(\tau)+a_nx_n(\tau)+\ \ldots\ +\ a_1x_1(\tau)-f\}=\frac{yn+1(\tau)}{\mu}\doteqdot 0$$

is formed at the input terminal **24** of an operational amplifier **21** having a sufficiently high amplification factor μ, whereby a solution of Equation (4) can be obtained.

Throughout the drawings, components designated by **22** are input resistors employed on the input side of the operational amplifier **21**. As is apparent from the above description, in the basic circuit in accordance with the present invention shown in FIG. **2**, the time scale factor α and the amplitude scale factor β are introduced separately, so that each of the factors can be controlled independently and in unison.

The basic setup constituting a basic form of the present invention can be somewhat expanded as in the case illustrated in FIG. **3**. In the circuit shown in FIG. **3**, a dummy variable consisting of a derivative $Y_{n+2}(t)$ which is one order higher than the highest order derivative $y_{n+1}(t)$ is employed. As a result, the input of a potentiometer $P_{n+1}(1/\alpha)$ designated by **32** will be $y_{n+2}(\tau)$, and the output obtained at the output position **23** of an integrator **28** will be $y_{n+1}(\tau)$. With this arrangement, the left-hand side of Equation (4) to be solved is organized in a circuit **20** based on the outputs $x_{n+1}(\tau)$, $x_n(\tau)$, ... , $x_1(\tau)$ obtained from the potentiometers P'_{n+1}, ..., P'_1 $(+\beta)$, also designated by **36**, **35**, **34**, and, **33**, respectively, and employing the high gain operational amplifier **37**, a loop is closed in the same manner as indicated in the basic setup in FIG. **2**.

As is described hereinbefore, a coefficient a_{n+1} for the highest derivative in the equation to be solved is included in the feedback through a loop connected between the potentiometer P'_{n+1} **1** and the input point **24** of the operational amplifier **21** in FIG. **2** For this reason, at a time when $a_{n+1} = 0$ at $t = t_1$, the fed-back amount around the operational amplifier **21** has been brought to zero at $t = t_1$, and the operation of the operational amplifier **21** at that time is unstable, causing difficulty in obtaining the solution of the equation.

However, in the arrangement shown in FIG. **3**, because the fed-back amount to the operational amplifier **37** has no relation to the coefficient of the highest order derivative in the equation to be solved, the solution thereof can be always obtained in a stable manner.

When van der Pol's differential equation shown in Example **1** is to be solved by employing the basic setup according to the present invention shown in FIG. **2**, the form of the circuit will be as shown in FIG. **4**, wherein the conversion ratio of the potentiometers **40** and **41** (p_1 and P_2) is $1/\alpha$, and that of the potentiometers **42**, **43**, and **44** (P'_1, P'_2, and P'_3) is β.

When the output of an integrator **39** (J_2) is $-y'(\tau)$, the output of the integrator **38** (J_1) is $y(\tau)$. Furthermore, the output of sign changers **45** and **48** are $-x(\tau)$ and $x(\tau)$, respectively, and the output of multiplier **46** is $-x^2(\tau)$. The output of the summing amplifier **47** is $x^2(\tau) - 1$, and the output of another multiplier **49** is $-\{1 - x^2(\tau)\}\,\dot{x}(\tau)$. Accordingly, when the

valve of a potentiometer **50** is caused to be , the input of the potentiometer **41** (P_2) becomes $\ddot{y}(\tau)$. In the same drawing, numeral **21** designates a high gain amplifier.

When the Bessel Function of zero order shown in Example 2 is to be solved by employing the embodiment thereof shown in FIG. **3**, the circuit shown in FIG. **5** is obtained. In this circuit, the conversion ratio of potentiometers **53**, **52** and **51** (P_3, P_2, and P_1) is selected to be $1/\alpha$, and the output signals from integrators **56**, **55**, and **54** (J_3, U_2, and J_1) are $\dddot{y}(\tau)$, $-\dot{y}(\tau)$ and $y(\tau)$, respectively. The conversion ratio of potentiometers **59**, **58**, and **57** (P'_3, P'_2, and P'_1) is selected to be β. The output of the summing amplifier **60** is $-\ddot{x}(\tau)+x(\tau)$, and the output of multiplier **61** is $-\tau\{\ddot{x}(\tau)+x(\tau)\}$. Numeral **37** designates a high gain amplifier, the gain of which is adjustable.

As is apparent from the above description, in the setup system according to he invention, the potentiometers for introducing the time scale factor α and the amplitude scale factor β are arranged in a much more simplified and orderly manner than in the conventional setup systems, and a linear or nonlinear ordinary differential equation can thereby be solved in a unitary manner by the employment of a basic setup as indicated in FIG. **3**. Since in the conventional setup system in an analog computer, the connection of the required elements has been manually carried out on a batch-board, there are disadvantages such as: (1) the accumulation of the information about the setup systems in an analog computer is not positive as in the case of subprograms in the digital computers; (2) because of the progress in the consolidation of the operation elements in the analog computer, the size of the computer is growing larger so that complicated problems can be handled in the computer, and it is becoming more difficult to set up these elements manually on the batch-board.

For the purpose of eliminating these disadvantages, a system of analog computers tends to be automatically set up by means of, for instance, a digital computer and the setup informations are positively stored in the digital computer as in the case of subprograms thereof.

Thus, the setup systems according to the present invention, wherein the linear or nonlinear ordinary differential equation is solved in a unitary manner as shown in FIGS. **2** and **3**, is important and advantageous in various applications in the art.

We claim:

1. In a setup system in an analog computer having a number of integrators corresponding respectively to variables in an equation to be solved and means for converting the variables with respect to time and amplitude, an improvement wherein: said means for converting the variables with respect to time comprises a first group of potentiometers individually connected to the input side of respective ones of said integrators; said means for converting the variables with respect to amplitude comprises a second group of potentiometers individually connected to the output side of respective ones of said integrators; all of the terms of the equation to be solved, except the forcing term, are expressed in terms of these variables; an operational amplifier having a summing point receptive of the terms thus newly expressed and the forcing term; and a feedback loop provided around said operational amplifier for producing a new coefficient of the highest order derivative in the equation to be solved, whereby the time scale factor and the amplitude scale factor thus introduced can be controlled separately and in a unitary manner by controlling said first and second groups of potentiometers.

2. In a setup system in an analog computer having a number of integrators corresponding respectively to the variables in an equation to be solved and means for converting the variables with respect to time and amplitude, an improvement comprising: an integrator corresponding to a variable which is of a higher order by one than the highest order derivative in the equation to be solved; said means for converting the variables with respect to time comprises a first group of potentiometers individually connected to the input side of respective ones of the integrators; said means for converting the variables with respect to amplitude comprises a second group of potentiometers individually connected to the output side of respective ones of the integrators; all of the terms of the equation to be solved, except the forcing term, are expressed in terms of these variables; an operational amplifier having means for adjusting the gain thereof and having a summing point receptive of the terms thus newly expressed and the forcing term; and a feedback loop around said operational amplifier for stabilizing the operation of said operational amplifier, whereby the time scale factor and the amplitude scale factor thus introduced can be controlled separately and in a unitary manner by controlling said first and second groups of potentiometers.

3. In a setup system in an analog computer for solving an equation expressable as a series of variable terms plus a forcing term: a plurality of serially connected together integrators each receptive of a signal representative of a variable term in an equation to be solved and each having an input side and an output side; first converting means comprising a first group of potentiometers each connected to the input side of one of said integrators for introducing a time conversion factor in each of the signals; second converting means comprising a second group of potentiometers each connected to the output side of one of said integrators for introducing an amplitude conversion factor in each of said integrated and time-converted signals, means including an operational amplifier connected to receive all the amplitude-converted signals and a forcing signal representative of the forcing term in the equation to be solved for summing the signals and providing a corresponding output signal; and a feedback loop around said operational amplifier receptive of said output signal for producing a coefficient signal representative of the coefficient of the highest order derivative in the equation to be solved.

4. A setup system according to claim **3**; wherein said last-mentioned means includes a potentiometer connected in said feedback loop.

5. A setup system according to claim **3**; wherein said last-mentioned means includes an integrator corresponding to a variable term which is of a one higher order than the highest order derivative in the equation to be solved.

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