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[21] Appl. No. **733,515**
[22] Filed **May 31, 1968**
[45] Patented **July 20, 1971**
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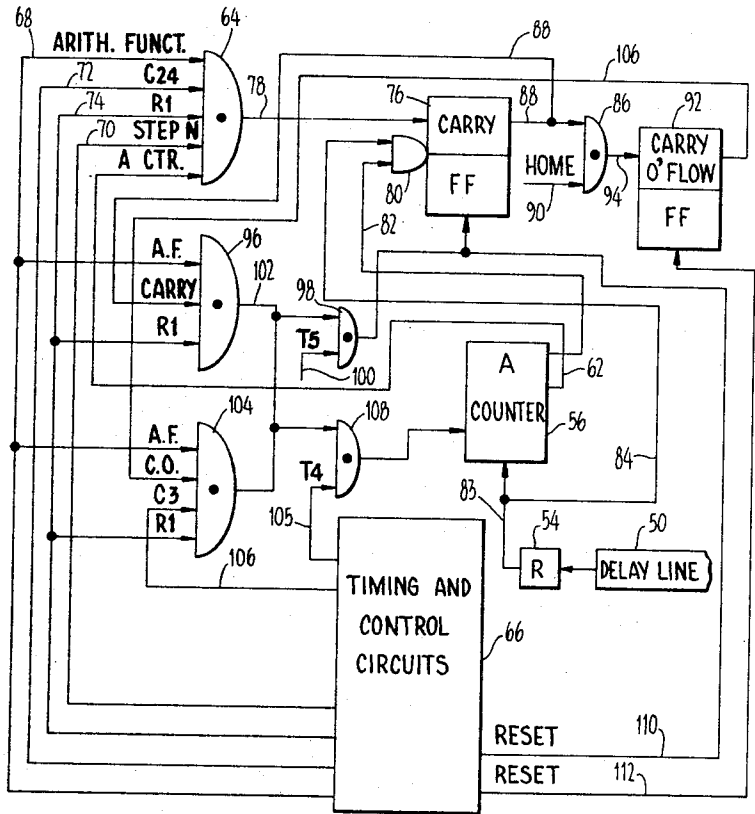
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[54] **ROUND OFF APPARATUS FOR ELECTRONIC CALCULATORS**
10 Claims, 9 Drawing Figs.

[52] U.S. Cl. **235/160,**
235/156
[51] Int. Cl. **G06f 7/38**
[50] Field of Search **235/156,**
160, 168, 176, 152

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ABSTRACT: Rounding off numbers in a desk top electronic calculator having a data train that recirculates in accordance with a predetermined sequence is accomplished by sensing whether the numeral in the next least significant digit position following the least significant digit position of interest is five or greater when it occurs in a predetermined location of the data train. When the numeral is five or greater, this condition is temporarily stored. Gating means coupled to the storage and to control signals indicative of the occurrence of the least significant digit position of interest in a predetermined location of the data train enables the numeral in the least significant digit position of interest to be increased by one. Much of the circuitry utilized to perform round off is also used to perform a carry function as arithmetically required.



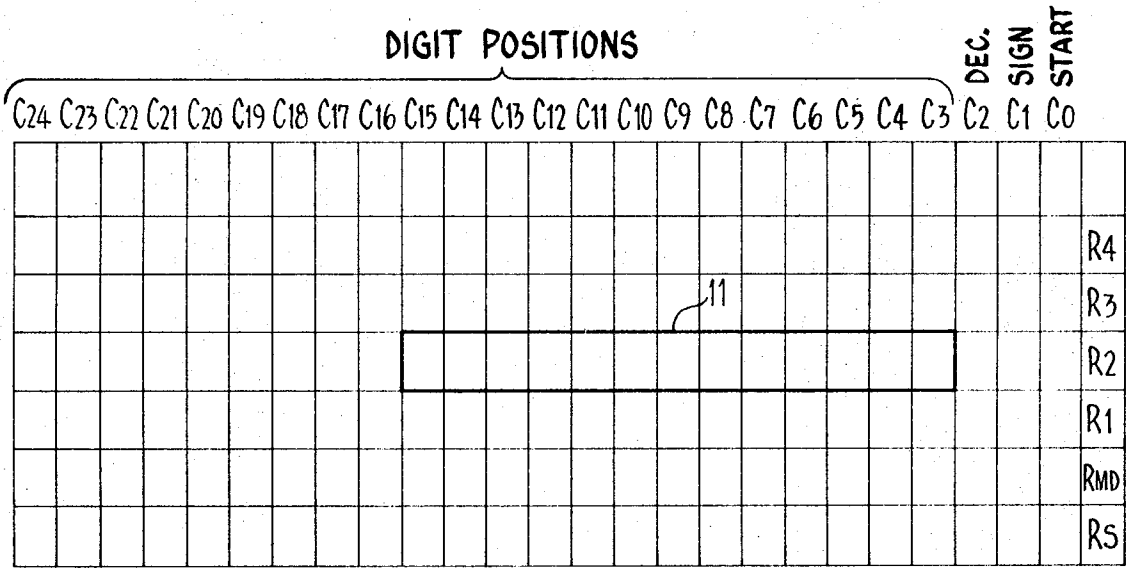


FIG. 1

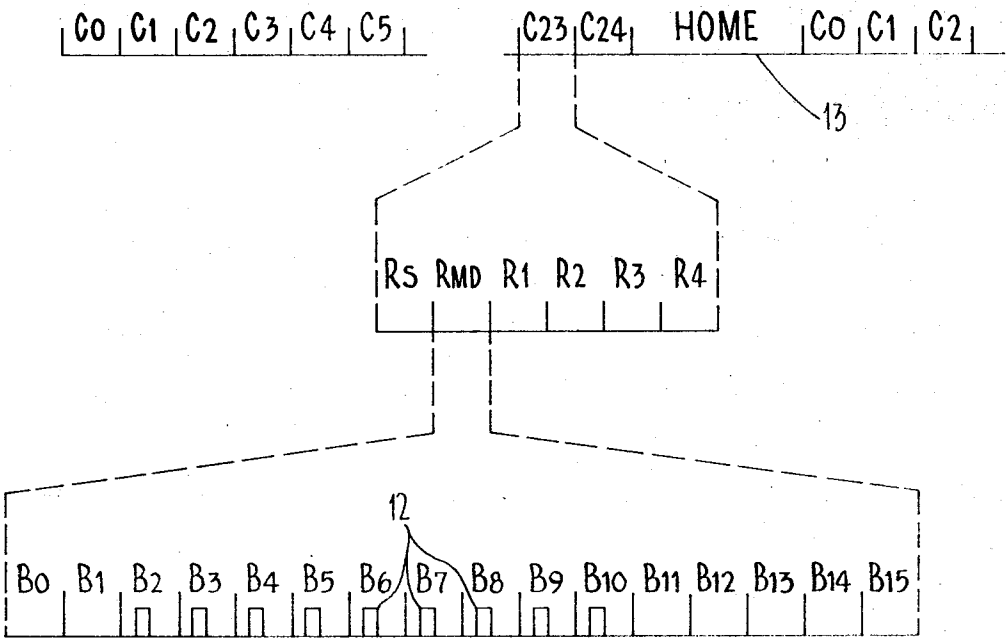


FIG. 2

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SHIFT TIMING

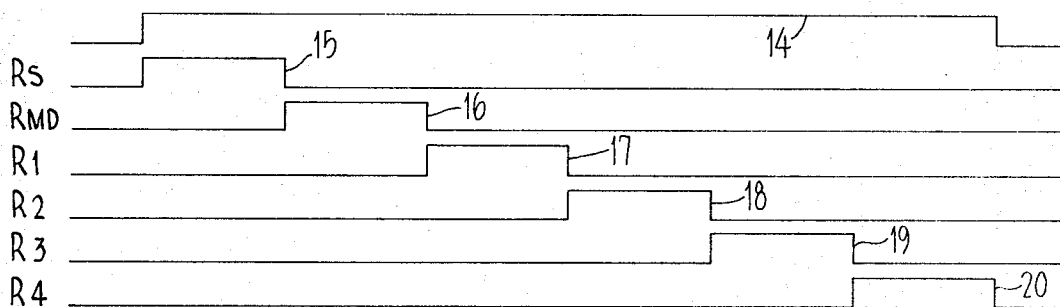


FIG. 3A

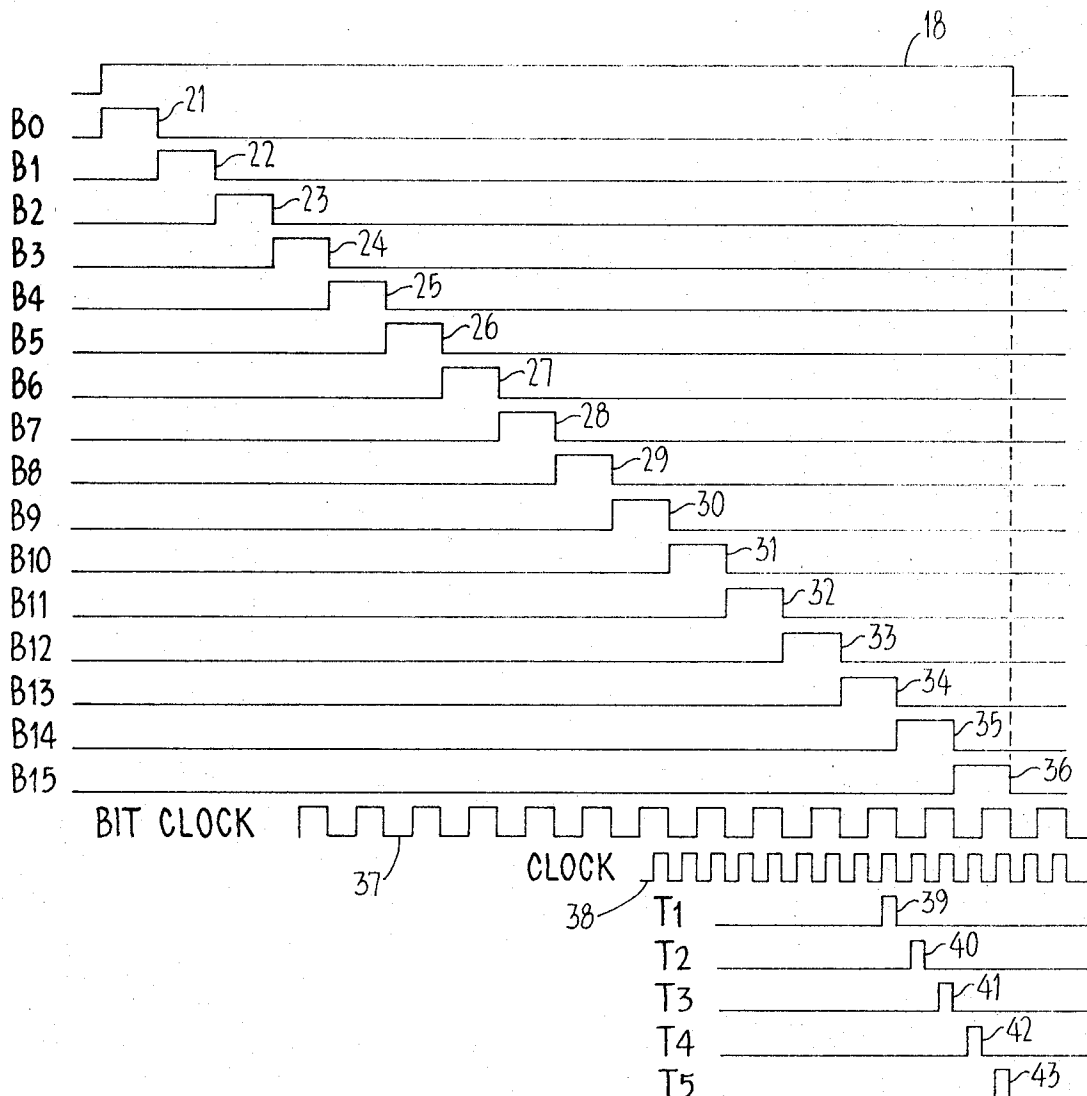


FIG. 3B

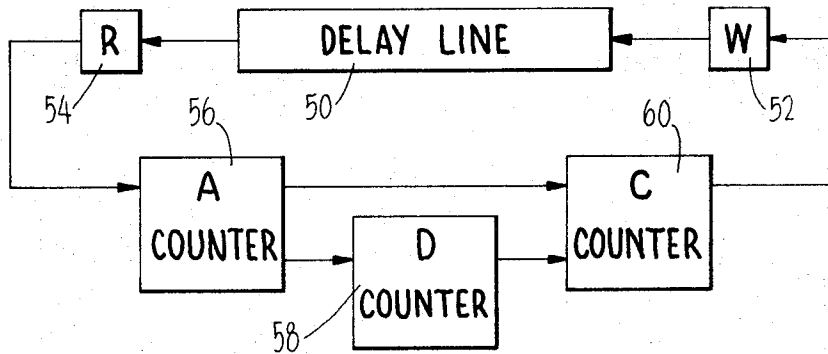


FIG. 4

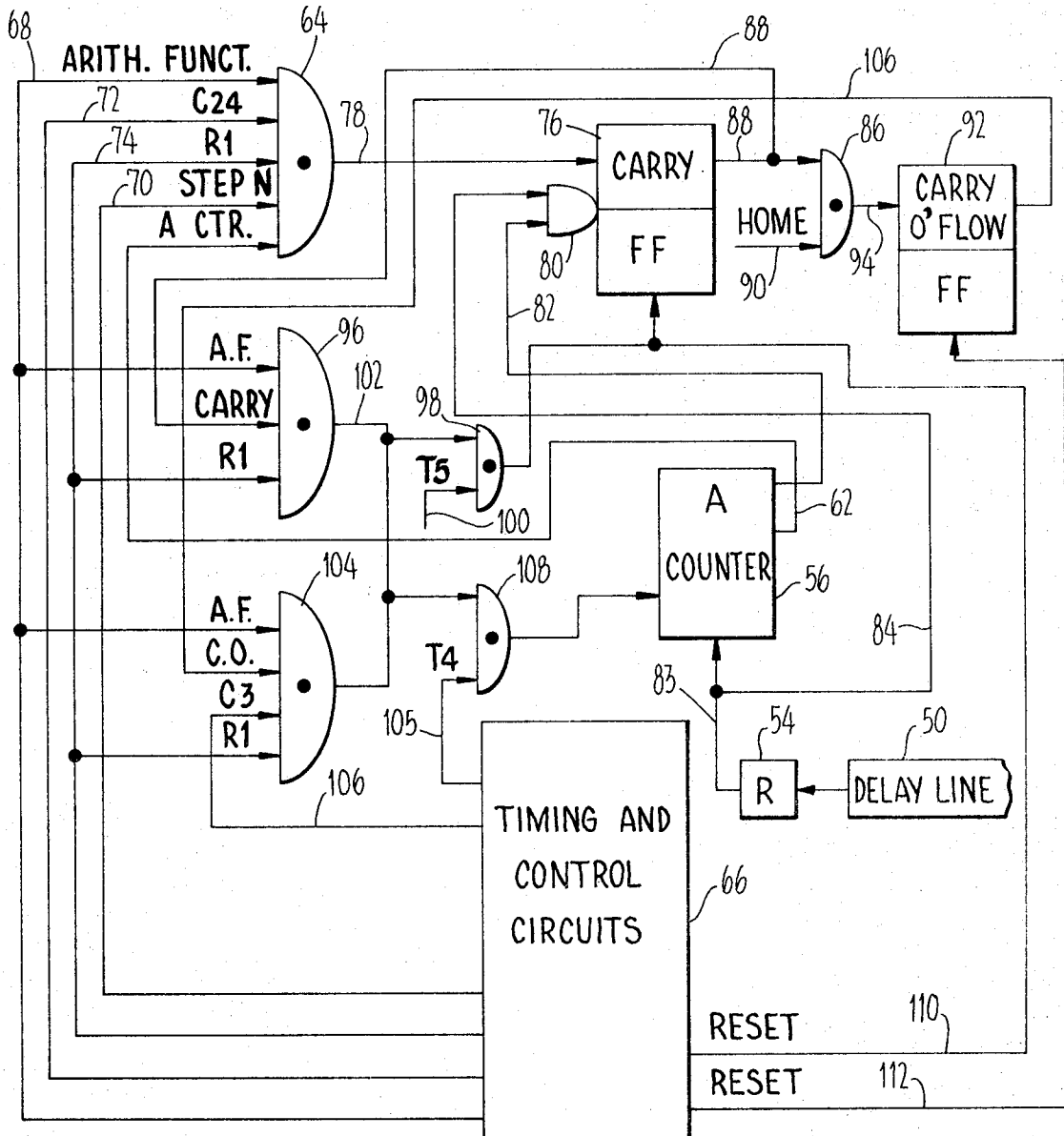


FIG. 5

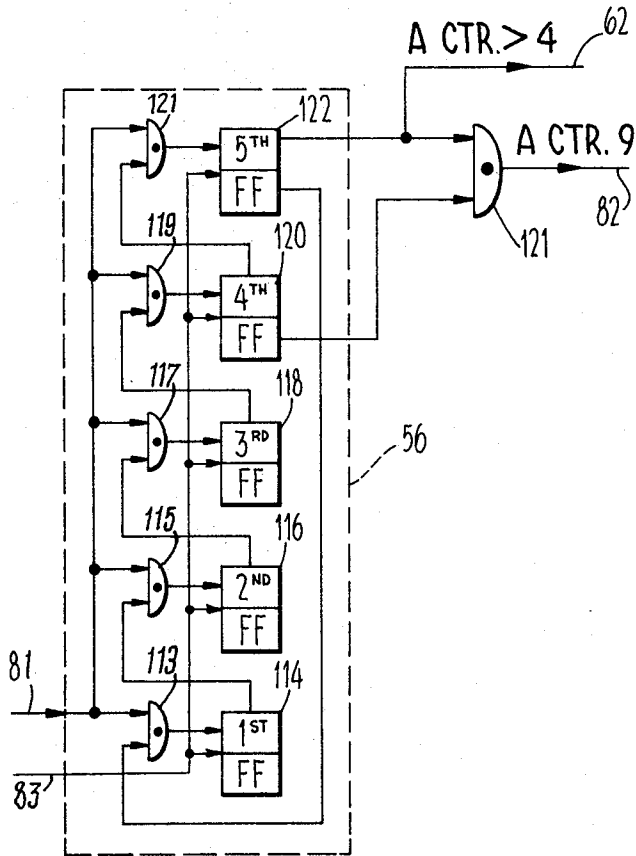


FIG. 6A

	1	2	3	4	5
0					
1	1				
2	1	1			
3	1	1	1		
4	1	1	1	1	
5	1	1	1	1	1
6		1	1	1	1
7			1	1	1
8				1	1
9					1

FIG. 6B

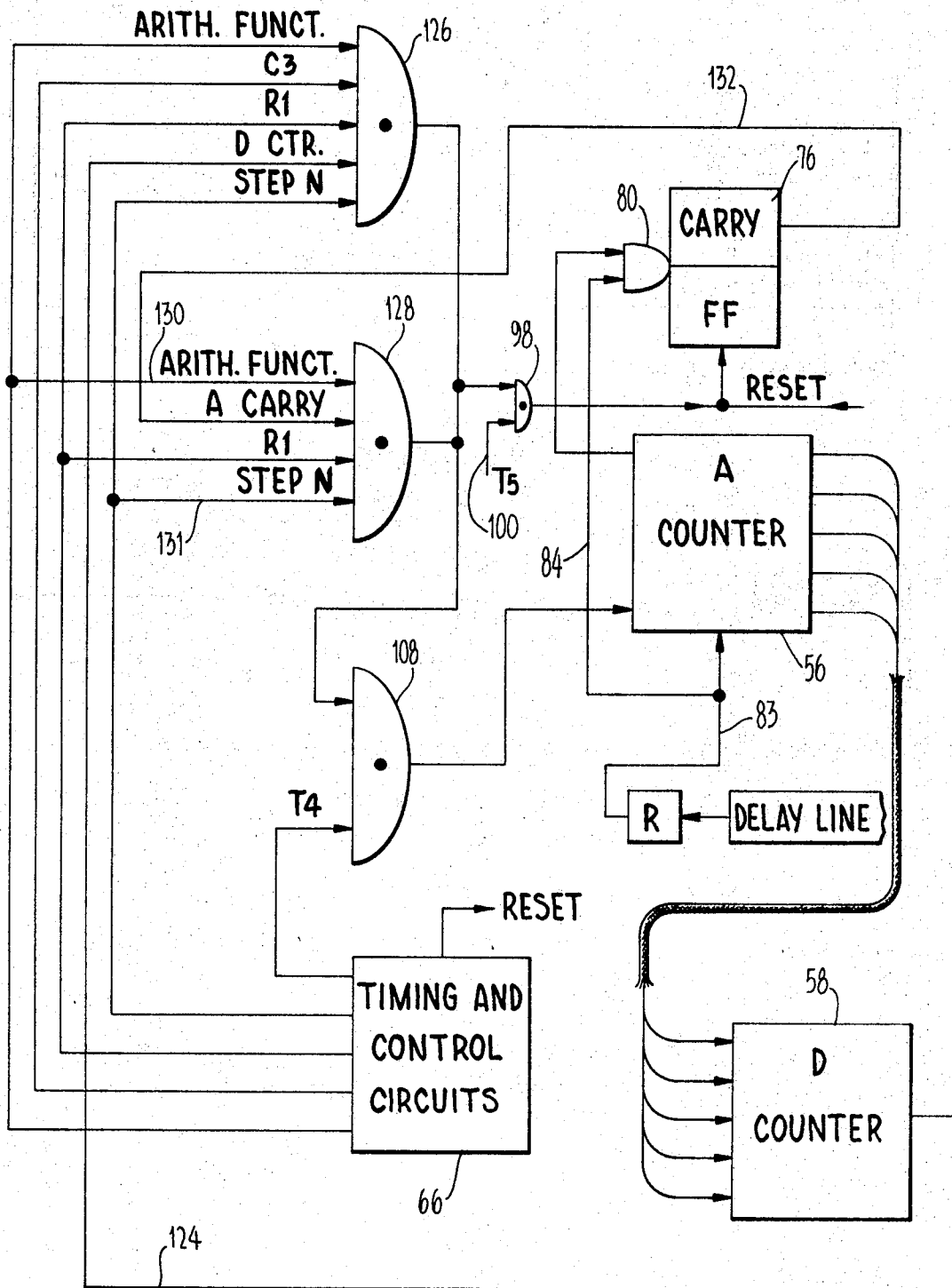


FIG. 2

ROUND OFF APPARATUS FOR ELECTRONIC CALCULATORS

BACKGROUND OF INVENTION

1. Field of Invention

This invention relates to electronic desk top calculators, and more particularly to apparatus for rounding off numbers in an electronic calculator having data positions that are accessible in accordance with a predetermined sequence.

2. Description of the Prior Art

In recent years, relatively small desk top electronic calculators have increasingly been utilized for performing arithmetic operations suitable for accounting, scientific, and like uses. For many purposes it is desirable to be able to perform a round off operation. For example, for accounting purposes it is desirable to perform a five cent round off after a multiplication or division operation. Large scale computers can readily be programmed to perform round off. However, most electronic desk top calculators have no such ability. In order to reduce the complexity, and therefore improve the reliability and cost factor of desk top electronic calculators, it is necessary that the round off operation require as little additional circuitry as possible.

SUMMARY OF THE INVENTION

Briefly described, the present invention is directed to an electronic desk top calculator having a plurality of registers, each capable of storing a number having a plurality of digits, and repetitively occurring control signals indicative of at least some of said digit positions. Round off in such a calculator is accomplished, in accordance with this invention, with a minimum of additional circuitry by utilizing existing circuitry in the calculator that also performs other functions. More specifically, round off is accomplished by means operably associated with the registers for recirculating the digit positions of at least some of the registers according to a predetermined sequence, sensing means operatively associated with the control signals determine whether the next least significant digit position following the least significant digit of interest is greater than four, storage means coupled to the sensing means temporarily stores the condition of a numeral greater than four appearing in the next least significant digit position, and gating means coupled to the storage means and to the control signals rounds off the numeral appearing in the least significant digit position of interest by the end of a subsequent occurrence of the least significant digit position of interest in response to the storage means containing a condition indicative of a numeral greater than four in the next least significant digit position.

Accordingly, one object of this invention is to provide round off apparatus for an electronic desk top calculator.

Another object of this invention is to provide round off apparatus for an electronic desk top calculator which requires a minimum of additional circuitry by utilizing, as much as practical, calculator circuitry also having functions other than a round off operation.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a schematic illustration of a plurality of registers each having a plurality of digit positions;

FIG. 2 is a schematic illustration showing the digit positions of the registers of FIG. 1 interlaced on a serial data train, together with the constituent locations of each digit position;

FIGS. 3A and 3B illustrate idealized waveshapes of control signals which may be utilized with the serial data train of FIG. 2;

FIG. 4 is a block diagram illustration of an electronic desk top calculator system which may utilize the round off apparatus of this invention;

FIG. 5 is a block diagram illustration of round off apparatus in accordance with one embodiment of the present invention;

FIG. 6A is a block diagram illustration of a digit counter which may be utilized as the A counter of FIGS. 4 and 5;

FIG. 6B illustrates in tabular form the state of binary devices in the counter shown in FIG. 6A;

FIG. 7 is a block diagram illustration of round off apparatus in accordance with still another embodiment of the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring now to the drawings, wherein like reference characters designate like or corresponding parts throughout the several views, there is shown in FIG. 1 an organization of a plurality of registers R_S , R_{MD} , R_1 , R_2 , R_3 and R_4 , each having a plurality of data, or digit, positions C_0 through C_{24} . As will be apparent to those skilled in the art, this organization may be achieved in various ways, such as by a magnetic core memory (with the number of cores at each data location being determined by the code used), one or more tracks on a magnetic drum, or the like. In accordance with one embodiment of this invention, the register organization of FIG. 1 was realized by a serial data train which was recirculated through a suitable delay device, such as an acoustic delay line. This serial data train was arranged, as shown in FIG. 2, with the data locations of the registers interlaced such that like orders C of data, or digit, positions of each register occur as a group with the lowest order data locations being first in time and the highest order data locations being last in time. For example, as shown by FIG. 2, column time C_{23} includes the like order data locations of each register R_S , R_{MD} , R_1 , R_2 , R_3 and R_4 with the lowermost register R_S data position occurring first and the uppermost register R_4 data position occurring last. Each complete occurrence of the data train C_0 — C_{24} is followed by a home period 13 during which time no signals or data occur and after which the entire data train is repeated.

In an electronic desk top calculator system in which the apparatus of the present invention was employed, the first column C_0 contained a start pulse or signal which indicated the end of the home period and the beginning of a new serial data train C_0 — C_{24} , the data positions of the column C_1 designated the sign of the numeral, if any, in the associated registers R_S , R_{MD} , R_1 , R_2 , R_3 and R_4 , the data positions of the column C_2 contained the decimal point location data of the numeral, if any, in the associated registers R_S , R_{MD} , R_1 , R_2 , R_3 and R_4 , and the data locations of each of the remaining columns C_3 — C_{24} contained the digits of the number, if any, in the associated registers. Each digit, or data, position utilized a pulse count notation such as is illustrated in FIG. 2 for the twenty-third order C_{23} of the registers R_{MD} . Each data position contained 16 B_0 — B_{15} time spaces, only nine of which, B_2 — B_{10} , were used to provide pulse count notation for each of the digits 0 through 9. For example, a 1 is denoted by a pulse 12 in the time period B_2 , a 2 is denoted by a pulse 12 in each time period B_2 and B_3 , a 3 is denoted by a pulse 12 in each time period B_2 , B_3 and B_4 , etc., with a 0 being indicated by an absence of a pulse in the time periods B_2 — B_{10} . It is clear, then, that FIG. 2 illustrates a 9 in the C_{23} digit position of the register R_{MD} .

The register organization illustrated in FIG. 1 may be accessible in an interlaced, serial manner as shown in FIG. 2 by means of recurring control and timing signals such as illustrated by FIGS. 3A and 3B. Referring now to FIG. 3A, there is illustrated a single column C signal 14. For purposes of simplicity and clarity, only one column signal 14 is illustrated. As will be apparent to those skilled in the art, however, the column signal 14 will occur sequentially, there being one such signal 14 for each of the positions C_0 — C_{24} . For each column signal 14 there are six independently occurring register signals 15, 16, 17, 18, 19 and 20, one for each of the six registers R_S , R_{MD} , R_1 , R_2 , R_3 and R_4 , respectively, with the register R_S control signal 15 occurring first in time and the register R_4 control signal 20 occurring last in time, as shown in FIG. 3A. As will now be apparent, the simultaneous occurrence of a

column C signal and one register signal 15, 16, 17, 18, 19 or 20 determines the occurrence, or accessibility of a particular data position C0—C24 of a particular register R_s, R_{MD}, R1, R2, R3 or R4, with like order register digit positions occurring consecutively for each column position.

As discussed above, each register data position includes 16 B0—B15 time spaces. Access to such positions may be accomplished by 16 independent and consecutively occurring signals 21 through 36 as illustrated in FIG. 3B for the register R2 control signal 18 of FIG. 3A. FIGS. 3A and 3B illustrate control signals that may correspond to each of the 16 positions of each register digit position and each digit position of each register. Depending upon the means used to achieve the data organization illustrated in FIG. 2, it is not necessary to utilize all of these control signals. For example, by utilizing the system shown in FIG. 4 (and described hereinbelow) which uses a recirculating data train and serial pulse count notation as shown in FIG. 2, only a portion of the control signals discussed above were required.

The signals illustrated in FIGS. 3A and 3B can be generated by any number of well-known means such as by applying the output 38 of a square wave oscillator, or clock, to a series of counters the outputs of selected stages of which are gated. In accordance with one apparatus which utilized the present invention, the clock signal 38 generator was activated by the start of the serial data train C0—C24 and inactivated during the time interval between successive data trains, i.e., during the occurrence of the home period 13. An example of appropriate timing signal generating means is that utilized by the Friden Division of The Singer Company in their Model 130 electronic calculator which was marketed at least as early as 1965. Also, for reasons that will be apparent from the description that follows, subsequent to the time period for each digit position during which the serial pulse count notation may occur (B2 through B11), but before the end of the digit position time period, a series of five independent, consecutively occurring T signals, 39, 40, 41, 42 and 43 were generated. These signals, T1 through T5 denoted by the reference numerals 39 through 43, respectively, were used to set various counters to zero, transfer digit information from one counter to another, add a 1 to a digit counter due to a round off operation as described below in detail, and the like.

It is to be understood that the timing and control signals shown in FIGS. 3A and 3B merely illustrate one way of accessing a register organization as shown in FIG. 1 and that various other signal arrangements may be devised to accomplish the same purpose.

FIG. 4 illustrates a general organization, in block diagram form, of an electronic desk top calculator which may utilize the round off apparatus of this invention. A serial memory device, such as an acoustic delay line 50, has write 52 and read 54 transducers associated with opposite ends thereof. Associated with the delay line are three registers, or counters, 56, 58 and 60, for providing two external data recirculation paths for a data train, such as is illustrated in FIG. 2. Each counter is adapted to store a single digit (0 through 9). The A counter 56 receives the serial data emanating from the delay line 50 and is adapted to be counted either up or down. Digit data in the A counter can be transferred in parallel to the C counter 60 which is adapted to be counted down in order to serially place the data therein onto the delay line. The data recirculating through the delay line, A counter and C counter, can be further delayed, for reasons discussed below, by being transferred in parallel from the A counter to the D counter 58, and therefrom in parallel to the C counter.

The operation of the apparatus of FIG. 4 is such that each digit emerging from the delay line 50 is counted into the A counter such that each pulse of the digit causes the A counter to advance one count. The digit is then shifted, in parallel, into the C counter which is counted down to a zero configuration. Each down count of the C counter results in a pulse being launched on the delay line. After the digit is shifted from the A counter to the C counter, the A counter is caused to be zero

set so that the next digit to emerge from the delay line may be counted into the A counter. Addition of two digits is accomplished by control logic (not shown) that inhibits the zero setting of the A counter. Accordingly, a second digit emerging from the delay line is added to a first digit already contained in the counter. For subtraction, the control logic inhibits the zero set signal and as the pulses of the second digit emerge from the delay line, the control logic will cause the A counter to be counted down instead of up as is done in addition. Multiplication and division can be accomplished by successive addition and subtraction, respectively.

The results of arithmetic operations may be displayed by means of a cathode ray tube or a printed paper output. Referring now to FIGS. 1 and 2, one calculator which utilized the present invention displayed the digit positions C3 through C15 (13 digit positions) of the number registers R1, R2, R3 and R4. For purposes of describing the present invention, it will be assumed that the result of arithmetic operations are developed in the number register R2. It can be seen that delaying the digits of a number by one column C time, by means of the digit counter D (FIG. 4) causes the number to be shifted left one digit position. Conversely, delaying all of the numbers by one digit position time R causes the numbers to be shifted up into the next number register position. That is, from register R1 into R2, R2 into R3, etc.

For purposes of describing this invention, it will be assumed that numbers having up to 13 digits may be entered and operated upon with the decimal point being located anywhere among the 13 digit positions. Accordingly, by fixing the decimal point of the answer anywhere among the 13 digit positions C3 through C15 of the number register R2 indicated by the heavy outline 11, it can be seen that the answer may contain one or more higher order digit positions above the C15 digit position which results in an overflow condition. Also, the answer may contain one or more lower order digit positions below the C3 digit position. Due to the arrangement of data shown in FIGS. 1 and 2, such lower order digits would appear in the most significant digit positions of the number register R1. The subject invention relates to rounding off the answer number in the number register R2 by sensing the next least significant digit position, which appears in the most significant digit position C24 of the number register R1, following the least significant digit of interest, which appears in the least significant digit position C3 of the number register R2. This round off operation is desirable for accounting purposes when the decimal point of the answer is located between the C5 and C4 digit positions which results in two significant digit positions to the right of the decimal point. Round off is also desirable for scientific and general calculations where the developed answers have lower order digits below the C3 digit position regardless of the location of the decimal point.

Round off apparatus in accordance with this invention is illustrated in FIG. 5 which shows a portion of the delay line 50 of FIG. 4, the A counter 56 and the read transducer 54. For purposes of clarity and simplicity, the interconnections from the A counter to the D and C counters 58 and 56, respectively, of FIG. 4, are not shown. A lead 62 emanating from the A counter 56 indicates when a digit greater than 4 is in the A counter and constitutes one input of an AND gate 64. Other inputs to the AND gate 64 are provided by well-known timing and control circuits 66, such as an indication on a lead 68 that the calculator is performing an arithmetic function, an indication on lead 70 that the arithmetic function has progressed to the point where the answer appears in the R2 register, a timing or control signal (such as described above) corresponding to the occurrence of the C24 column time appears on the lead 72, and a timing or control signal (such as described above) corresponding to the occurrence of the R1 register appears on the lead 74. Accordingly, the AND gate 64 is enabled whenever, during an arithmetic operation, the next least significant digit position C24R1 following the least significant digit position of interest C3R2 of the answer contains a number greater than 4. When enabled, the AND gate 64 sets a carry flip-flop 76 by way of the lead 78.

The carry flip-flop 76 can also be set by enabling an AC or dynamic gate 80. One input to the dynamic gate 80 comprises a lead 82 emanating from the A counter which indicates that the count in the A counter is going from 9 to 0. The other input to the dynamic gate 80 comprises information emanating from the delay line and appearing on the lead 84. When set, the carry flip-flop enables one input of an AND gate 86 by way of the lead 88 with the other input being the lead 90 which is activated whenever the home period occurs. Accordingly, the AND gate 86 is enabled whenever the carry flip-flop is set at the time the home period occurs. When enabled, the AND gate 86 sets a carry overflow flip-flop 92 by way of the lead 94. When set, the carry flip-flop 76 also activates one input to an AND gate 96 by way of the lead 88. The other inputs to this AND gate 96 comprise the occurrence of an arithmetic function on lead 68 and the occurrence of a register R1 digit position control signal on the lead 74. AND gate 96 is enabled when, as a result of a round off operation, it is necessary to add a 1 to the next higher significant digit position, or positions. This is accomplished by an AND gate 108, which is enabled at T4 time whenever the AND gate 96 is also enabled, by way of leads 105 and 102, respectively, to add 1 to the A counter in a manner as described below.

When the carry overflow flip-flop 92 is set, it activates one input to the AND gate 104 by way of the lead 106. Other inputs to this AND gate comprise the occurrence of an arithmetic function by way of lead 68, and the occurrence of the least significant digit position C3 of the R1 register by way of leads 106 and 74, respectively. In a manner as described below, the AND gate 104 is enabled when the next least significant digit position C24R1 following the least significant digit position of interest C3R2 is greater than 4. When enabled, the AND gate 104 enables one input of the AND gate 108 such that the next occurrence of the T4 signal (described hereinabove) causes a 1 to be added to the contents of the A counter such that the least significant digit position C3R2 is increased by 1. The 1 added to the A counter by way of the AND gate 108 between digits. That is, at T4 time after a digit has been transferred out of the A counter at T1, T2 or T3 time, but before the following digit of interest arrives from the delay line. In this manner, a 1 is added to the C3R2 digit position by placing a 1 into the A counter during the occurrence of C3R1 at T4 time with the C3R1 digit having been transferred out of the A counter during the occurrence of C3R1 at T1, T2 or T3 time. In a like manner, when the AND gate 108 is enabled to perform a carry operation due to the AND gate 96 being enabled, a 1 count is entered into the A counter during a R1 digit time at the occurrence of a T4 pulse, but after the R1 digit has been transferred out of the A counter. When the corresponding order R2 digit occurs, it is counted into the A counter. Since the A counter already contains a 1 count, the R2 digit is added to the 1 count, thereby causing the R2 digit to be increased by one.

Briefly described, the operation of the apparatus of FIG. 5 is such that when the next least significant digit position C24R1 following the least significant digit position C3R2 of interest of a developed answer is greater than 4, the AND gate 64 is enabled to set the carry flip-flop 76. During the next home period prior to the next occurrence of the data train, the AND gate 86 is enabled to set the carry overflow flip-flop 92. This causes the AND gate 104 to be enabled at the next C3R1 time such that a 1 is added to the C3R2 digit position, as described above, resulting in a round off of the answer appearing in the answer register R2. If this results in the digit appearing in the least significant digit position of interest C3R2 becoming 0, a carry operation is required and the carry flip-flop 76 is again set by means of the dynamic gate 80. This results in the AND gate 96 being enabled during the next higher order, or next most higher significant digit position C4 adjacent the least significant digit position C3 of the R1 register which, in a manner as described above, causes a 1 to be entered into the A counter such that the corresponding digit position of the R2 register is increased by one. This carry operation will continue as long as arithmetically required. The timing and control cir-

uits 66 provide a reset pulse on the lead 110 to reset the carry flip-flop at the beginning of each train of data, i.e., at the end of each home period, and a reset pulse on the lead 112 to reset the carry overflow flip-flop at the end of each data train, i.e., at the beginning of each home period. Also, by means of the AND gate 98, the carry flip-flop is reset each time a 1 is entered into the A counter by way of AND gates 108 and 104 or AND gates 96 and 108 at the following T5 time after the T4 time during which a 1 count was entered into the A counter.

Before describing the operation of the apparatus of FIG. 5 in detail, reference is made to FIG. 6A which shows, within the dotted outline 56, a schematic representation of the A counter of FIGS. 4 and 5 as comprising five flip-flops 114, 116, 118, 120 and 122 interconnected, in a well-known manner, to provide a 0 to 9 serial counter. The serial output of the delay line 50 enters the A counter by way of the lead 83 and the leads for transferring the data in the A counter in parallel to either the C or D counters 60 and 58, respectively, are not shown for purposes of simplifying the drawing but, as is well known, would emanate from each of the flip-flops 114, 116, 118, 120 and 122.

The counter 56 is enabled by application of a potential on the lead 81 that tends to enable the AND gates 113, 115, 117, 119 and 121 associated with the flip-flops 114, 116, 118, 120 and 122 respectively.

FIG. 6B is a truth table which illustrates the state of each of the five flip-flops 114, 116, 118, 120 and 122 for each of the 10 counts (0 through 9) which can be set into the A counter 56.

Referring to FIGS. 6A and 6B, it can be seen that the fifth flip-flop 122 is always set whenever the A counter 56 contains a number greater than 4 which causes the lead 62 to be enabled. Also, as shown by FIG. 6B, the fourth flip-flop 120 is reset and the fifth flip-flop 122 is set only when the A counter 56 contains the numeral 9. Accordingly, by utilizing the set side of the fifth flip-flop 122 and the reset side of the fourth flip-flop 120 as the inputs to an AND gate 121, the lead 82 is enabled whenever the A counter contains the numeral 9.

Briefly described, the operation of the counter 56 is such that a pulse on the lead 83 will cause a flip-flop to be set if its associated AND gate is enabled and reset if its associated AND gate is disabled. Therefore, assuming that an enabling potential appears on lead 81 and that all the flip-flops 114, 116, 118, 120 and 122 are reset, a first pulse on the lead 83 will cause the first flip-flop 114 to be set because its AND gate 113 is enabled by the reset condition of the fifth flip-flop 122. All the other AND gates are disabled prior to the arrival of the first pulse because they are coupled to the set output of reset flip-flops 114, 116, 118 and 120. The first flip-flop 114 being set will cause the AND gate 115 associated with the second flip-flop 116 to be enabled so that a second pulse on the lead 83 causes the second flip-flop to become set. This continues until the arrival of a fifth pulse on the lead 83 at which time all five flip-flops are set and the counter 56 contains a count of five.

When all flip-flops 114, 116, 118, 120 and 122 are set, the reset output of the fifth flip-flop 122 disables the AND gate 113 associated with the first flip-flop 114. Accordingly, the occurrence of a sixth pulse on the lead 83 will reset the first flip-flop thereby disabling the AND gate 115 associated with the second flip-flop so that a seventh pulse on the lead 83 will disable the second flip-flop 116. This continues until a tenth pulse appears on the lead 83 which causes the fifth flip-flop to be reset at which time all five flip-flops are reset and the counter contains a count of zero.

Referring now to FIG. 5, assume that an arithmetic function is occurring with the answer being properly decimally aligned in the R2 register and there being no overflow to the left, i.e., the answer does not contain a numeral (1 through 9) in any of the digit positions C24R2 through C16R2. For this condition the lead 68 denoting an arithmetic function is enabled as is the lead 70 which denotes that the step of rounding off the answer can take place, if arithmetically required. At this time the en-

tire data train passes serially through the A counter. Each time a digit greater than 4 occurs in the A counter, the input to the AND gate 64 on the lead 62 is enabled, as described hereinabove in conjunction with FIGS. 6A and 6B. However, the AND gate 64 will only be enabled if the C24R1 digit position contains a numeral greater than 4 when the additional leads 72 and 74 are enabled during the occurrence of the C24R1 digit position which corresponds to the next least significant digit position of the answer following the least significant digit position of interest C3R2. Accordingly, if the C24R1 digit position contains a numeral greater than 4, the AND gate 64 is enabled during the occurrence of the C24R1 digit position in the A counter which causes the carry flip-flop 76 to be set. When set, the carry flip-flop enables the lead 88, which constitutes one input to the AND gate 96. However, since the other input to the AND gate 96 on the lead 74 is only enabled during the occurrence of a register R1 digit position, and since no further R1 digit positions occur in a particular data train after the C24R1 digit position, the AND gate 96 cannot be enabled until the occurrence of a subsequent data train. However, the carry flip-flop 76 is reset at the beginning of each new data train as described above, such that the carry flip-flop will again be set only if a carry operation is required because of round off as described below.

At the end of the data train the home period occurs which enables lead 90 to cause the AND gate 86 to be enabled, thereby setting the carry overflow flip-flop 92. When set, the carry overflow flip-flop enables the lead 106 which constitutes one input to the AND gate 104. The input to the AND gate 104 appearing on the lead 68 has previously been enabled due to the fact that an arithmetic function is taking place. It can be seen that when the C3R1 digit position of a subsequent data train occurs, the leads 106 and 74 are also enabled, thereby enabling the AND gate 104, which results in one input to the AND gate 108 to be enabled by way of the lead 102. During the occurrence of the C3R1 digit position the numeral corresponding thereto occurs in the A counter 56. However, as discussed above, the occurrence of the associated T1, T2 or T3 timing signal causes the numeral contained in the A counter to be transferred into the C or D counters. Subsequently, and during the occurrence of the C3R1 digit position, the associated T4 pulse occurs on the lead 105 to enable the AND gate 108 which results in a 1 count being entered into the A counter. This 1 count remains in the A counter such that when the next digit position occurs, that is, the least significant digit of interest, C3R2, the pulse count notation representing the numeral therein is counted onto the 1 previously set in the A counter to increase the numeral in the C3R2 digit position by one to provide round off.

If the numeral appearing in the C3R2 digit position prior to round off was less than 9, round off is complete and the arithmetic operation may be terminated. However, if the C3R2 digit position contains a 9 prior to round off, the lead 82 is enabled when the A counter contains a count of 9 which corresponds to the eighth pulse of the nine pulses comprising the numeral 9 in the C3R2 digit position. When the ninth pulse leaves the delay line, it is applied by way of the lead 84 as one input to the dynamic gate 80. As the count in the A counter goes from 9 to 0 the lead 82 goes from an enabled to disabled condition, which enables the dynamic gate 80 and sets the carry flip-flop 76 in a well-known manner. This enables the lead 88 which comprises one input to the AND gate 96. Since an arithmetic function is taking place, the input to the AND gate 96 appearing on lead 68 is also enabled. Accordingly, the next occurring R1 digit position timing pulse appearing on the lead 74 enables the AND gate 96. It should be noted that the inputs to the AND gate 96 are not limited by a column C timing signal which allows the AND gate 96 to be enabled by each subsequent occurring R1 digit position during which the carry flip-flop 76 is set. When enabled, the AND gate 96 causes a 1 to be placed into the A counter at T4 time of the next R1 digit position which causes a 1 to be added to the numeral in the next most significant digit position of the

R2 register. During the time the AND gate 96 is enabled, the occurrence of a T5 signal, subsequent to the T4 signal which causes a 1 to be entered into the A counter, enables the AND gate 98 by way of the lead 100 to reset the carry flip-flop. When reset, the carry flip-flop will prohibit any further carry operations unless the 1 added to the A counter during the occurrence of the T4 pulse during the R1 digit position causes the R2 digit position numeral to go to 0 from 9 which results in setting of the carry flip-flop by way of the dynamic gate 80, in a manner as described above. The AND gate 98 is also enabled when round off occurs in the C3R2 digit position. However, since the carry flip-flop has previously been reset by way of the lead 110 at the end of the home period, enabling of the AND gate 98 at this time has no effect on the state of the carry flip-flop 76.

As will be apparent from the above description, if no further carry operations are to take place, enabling of the AND gate 98 resets the carry flip-flop 76 and the round off operation is complete. Once this occurs it will be noted that the carry overflow flip-flop 92, which has previously been set, remains in a set condition. However, since no further R1C3 digit positions can occur during this particular data train, it is not possible to enable the AND gate 104 during the remainder of the data train and upon the termination of the data train, the carry overflow flip-flop is reset to its normal position by way of the lead 112.

Referring now to FIG. 7, another embodiment of the present invention is illustrated which, by utilizing the D counter 58, enables the carry overflow flip-flop 92, the associated AND gate 86 and one of the AND gates 64, 96 or 104 of FIG. 5 to be eliminated. The operation of the apparatus of FIG. 7 is such that the C24R1 digit position, which corresponds to the next least significant digit of interest, of each data train is caused to be nondestructively copied into the D counter 58 from the A counter 56 in a well-known manner. If this numeral is 5 or greater, the lead 124 is enabled in a manner as described above and comprises one input to the AND gate 126. The inputs to the AND gate 126 are such that it is enabled during the next occurring C3R1 digit position of a data train only if the C24R1 digit position of the previous data train cycle is greater than 4. When enabled, the AND gate 126 causes the AND gate 108 to be enabled during the occurrence of the T4 pulse of the C3R1 digit position, thereby entering a 1 into the A counter during the occurrence of the C3R1 digit position, but after the numeral corresponding to the C3R1 digit position has been transferred out of the A counter exactly as described above. If setting a 1 into the A counter causes a numeral in the least significant digit position of interest C3R2 to go from 9 to 0, the carry flip-flop 76 is set by way of the dynamic gate 80, as described above. When set, the carry flip-flop enables the lead 132, which comprises one input of the AND gate 128. Another input to the AND gate 128 appears on the lead 130 and corresponds to the occurrence of an arithmetic function and is thereby enabled. Another input to the AND gate 128 appearing on the lead 131 corresponds to the step of an arithmetic function during which round off occurs as arithmetically required and is also enabled. Accordingly, if rounding off the C3R2 digit position causes the numeral therein to go from 9 to 0, the AND gate 128 is enabled during the subsequently occurring R1 digit position thereby enabling the AND gate 108, at the occurrence of the T4 pulse of the next R1 digit position to perform a carry operation, as described hereinabove. The occurrence of a T5 pulse on the lead 100 to the AND gate 98 will reset the carry flip-flop each time a 1 is added to the A counter during the occurrence of an R1 digit position. The output of the AND gate 98 can also be used to set the D counter 58 to 0 after round off of the C3R2 digit position. However, each time the count in the A counter goes from 9 to 0 due to a 1 being entered into the A counter by way of the AND gate 108, the carry flip-flop is set by way of the dynamic gate 80. Accordingly, as is the case of the apparatus illustrated in FIG. 5, the carry operation will continue in a given data train as long as arithmetically required.

From the above description it is clear that the present invention provides round off apparatus for an electronic desk top calculator in such a manner that a minimum of additional circuitry is required by utilizing circuits having functions other than a round off operation. For example, the A counter 56 and D counter 58 have many other functions other than that of round off. The carry 76 and carry overflow flip-flop 92 and some of the AND gates associated therewith are utilized in performing arithmetic operations other than that required for a round off function.

It should be understood, of course, that the foregoing detailed description relates only to preferred embodiments of the present invention and that numerous modifications or alterations may be made thereof without departing from the spirit and scope of the invention, as set forth in the following claims.

What I claim is:

1. Apparatus for rounding off a number comprising:

a memory having a plurality of registers each capable of storing a number having a plurality of digits,

means for successively recirculating the digits of at least some of said numbers through a closed loop which includes said memory to provide a serial recirculating data train with a predetermined time interval between the end of said data train and the beginning of said data train,

said closed loop including a temporary single digit storage device,

said single digit storage device providing a first output when the digit therein is greater than 4,

a first bistable device outside of said closed loop,

first gating means coupled between said first output of said digit storage device and said first bistable device for causing said first bistable device to be placed into a predetermined one of its stable states when the digit following the least significant digit of interest of a number is greater than 4 when it appears in said digit storage device,

a second bistable device,

second gating means coupled between said first and second bistable devices for causing said second bistable device to be placed into a predetermined one of its stable states during said predetermined interval when said first bistable device indicates said digit following the least significant digit of interest is greater than 4, and

third gating means coupled between said second bistable device and said digit storage device to cause said least significant digit of interest to be incremented by one when it occurs in said digit storage device and when said second bistable device indicates the digit following said least significant digit is greater than 4.

2. The apparatus of claim 1 wherein

said digit storage device provides a second output when a digit therein is incremented from 9 to 0,

fourth gating means coupled between said second output of said digit storage device and said first bistable device to place said first bistable device into said predetermined one of its stable states when a digit is incremented from 9

to 0 while in said digit storage device,

fifth gating means coupled between said first bistable device and said digit storage device to increment the next most significant digit by one when it occurs in said digit storage device and when said first bistable device indicates that the digit in said digit storage device has been incremented from 9 to 0.

3. The apparatus of claim 1 wherein, said closed loop includes said memory.

4. The apparatus of claim 1 wherein, the digit positions of numbers recirculated are interlaced.

5. The apparatus of claim 1 wherein, said memory includes an acoustic delay line.

6. Apparatus for rounding off a number comprising:

a memory having a plurality of registers each capable of storing a number having a plurality of digits,

means for successively recirculating the digits of at least some of said numbers through a closed loop which includes said memory to provide a serial recirculating data train,

said closed loop including a first temporary single digit storage device,

a second temporary single digit storage device coupled to said first digit storage device and not in said closed loop for having the digit following the least significant digit of interest of a number nondestructively copied therein when said digit occurs in said first digit storage device, said second digit storage device providing an output when the digit therein is greater than 4, and

first gating means coupled between said second digit storage device and said first digit storage device to cause said least significant digit of interest to be incremented by one when it occurs in said first digit storage device and when said second digit storage device indicates the digit following said least significant digit is greater than 4.

7. The apparatus of claim 6 wherein,

said first digit storage device provides an output when a digit therein is incremented from 9 to 0,

a bistable device,

Second gating means coupled between said output of said first digit storage device and said bistable device to place said bistable device into a predetermined one of its stable states when a digit is incremented from 9 to 0 while in said first digit storage device

third gating means coupled between said bistable device and said first digit storage device to increment the next most significant digit by one when it occurs in said first digit storage device and when said bistable device indicates that the digit in said first digit storage device has been incremented from 9 to 0.

8. The apparatus of claim 6 wherein, said closed loop includes said memory.

9. The apparatus of claim 6 wherein, the digit position of members recirculated are interlaced.

10. The apparatus of claim 6 wherein, said memory includes an acoustic delay line.