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(54) **Method and apparatus for decision threshold control in an optical signal receiver**

Verfahren und Vorrichtung zum Verstellen der Entscheidungsschwelle in einem optischen Signalempfänger

Procédé et dispositif pour régler le seuil de décision dans un récepteur de signaux optiques

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(73) Proprietor: **Tyco Electronics Subsea Communications LLC**
Morristown NJ 07960 (US)

(72) Inventors:
- **Domagala, Jerzy**
  Red Bank, NJ 07701 (US)
- **Cai, Yi**
  Eatontown, NJ 07724 (US)
- **Kerfoot III, Franklin Webb**
  Red Bank, NJ 07701 (US)
- **Valvo, Gregory**
  Wall, NJ 07719 (US)

(74) Representative: **Brookes Batchellor LLP**
102-108 Clerkenwell Road
London
EC1M 5SA (GB)

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Description

Technical Field

[0001] The present application relates to optical transmission of information and, more particularly, to a method and apparatus for decision threshold control in an optical signal receiver.

Background

[0002] Reliable optical communication systems require mechanisms for minimizing the effects of signal degradation occurring between associated transmitters and receivers. Signal degradation occurs due to a variety of factors that cannot be completely eliminated; and is exacerbated by the long-haul transmission distances and high optical channel counts required in many applications. Due to signal degradation, some transmitted data may be incorrectly interpreted at a receiver. If data is misinterpreted at a rate above that which is acceptable, the efficacy and viability of the system may be lost.

[0003] A variety of techniques for minimizing the effects of signal degradation have been investigated. Forward Error Correction (FEC) is one technique used to help compensate for signal degradation and provide "margin improvements" to the system. Margin improvements generally allow an increase in amplifier spacing and/or increase in system capacity. In a Wavelength Division Multiplexing (WDM) system, for example, margin improvements obtained through FEC techniques allow an increase in the bit rate of each WDM channel and/or a decrease the spacing between WDM channels. This translates directly into an increased system data capacity.

[0004] FEC typically involves insertion of a suitable error correction code into a transmitted data stream to facilitate detection and correction of data errors about which there is no previously known information. Error correction codes are generated in an FEC encoder for the data stream, and are sent to a receiver including an FEC decoder. The FEC decoder recovers the error correction codes and uses them to correct any errors in the received data stream.

[0005] Of course, the efficacy of FEC techniques is impacted by the ability of the optical signal receiver to correctly detect transmitted data and error correction codes. Improvements in receiver signal detection thus translate to improved performance of FEC codes in providing correction of bit errors. A known receiver configuration includes a decision circuit for converting the received data signal into a binary electrical signal, e.g. including logic ones and zeros representative of the transmitted data. The decision circuit may, for example, include a comparator for comparing the received data signal with a predetermined voltage level (the decision threshold). If the voltage level of the received data signal is above the decision threshold at a particular sample time, the comparator may output a logic one. If, however, the voltage level of the received data signal is below the decision threshold, the comparator may output a logic zero.

[0006] The decision circuit thus makes an initial decision as to the data bit values of the received data stream. The FEC decoder detects and corrects errors in the data stream established by the decision circuit. Certainly, therefore, optimal setting of the decision threshold in the decision circuit is important in achieving optimal system bit error rate (BER).

[0007] In a known configuration an optimal decision threshold is established by minimizing the total number of corrected errors reported by the FEC decoder. The total number of corrected errors is provided as feedback to a decision threshold control circuit which causes adjustment of the decision threshold to minimize the total number of corrected errors.

[0008] For example, EP 1324555 discloses a data regenerator for regenerating a data signal, including a convertor for converting a received data signal into a binary data signal in dependence on conversion parameters, an error corrector for correcting errors in the binary data signal based on error correction code contained in the binary data signal to produce a corrected binary data signal, and a performance monitor for comparing the corrected binary data signal with an uncorrected representation of the binary data signal to determine information about the relative number of logic "1"s and logic "0"s that have been corrected by the error corrector and output a feedback signal representative of the relative number, wherein the convertor adjusts at least some of the conversion parameters in dependence on the feedback signal.

[0009] A difficulty associated with this approach is that the direction of correction for the decision threshold is typically unknown. As such, the initial decision threshold correction may be implemented in an incorrect direction, resulting in an increase in the total number of corrected errors. The increase in errors may be corrected by the feedback loop in the next sample period, but is nonetheless inefficient.

[0010] Accordingly, there is a need for a method and apparatus for decision threshold control in an optical signal receiver, which is capable of efficiently controlling a decision threshold.

[0011] Such a method and apparatus is disclosed in the appended claims.

Brief Description of the Drawings

[0012] These and other features and advantages of the present invention will be better understood by reading the following detailed description, taken together with the drawings wherein:

FIG. 1 is a schematic block diagram of an optical communication system including decision threshold

adjustment consistent with one embodiment of the present invention;

FIG. 2 is an exemplary eye diagram illustrating decision threshold adjustment in a manner consistent with the invention; and

FIG. 3 is a block flow diagram illustrating an exemplary decision threshold adjustment process consistent with the present invention.

Detailed Description

[0013] FIG. 1 shows an optical communication system 100 including an apparatus and method for decision threshold adjustment consistent with one embodiment of the present invention. The system is capable of optimizing a decision threshold by balancing the number of binary ones ("1"s) corrected by an FEC decoder with the number of zeros ("0"s) corrected by the FEC decoder. Although exemplary embodiments are described in the context of an optical system, and are useful in connection with a long-haul WDM optical system, the broad concepts discussed herein may be implemented in other communication systems transmitting and receiving other types of signals.

[0014] The optical communication system 100 may include a transmitter 102 for transmitting an encoded optical signal 108 and a receiver 104 for receiving the encoded optical signal 108. Those of ordinary skill in the art will recognize that the depicted system is highly-simplified for ease of explanation. For example, the transmitter 102 and the receiver 104 may be configured as one or more transceivers capable of performing both transmitting and receiving functions. The illustrated embodiments herein are provided only by way of explanation, not of limitation.

[0015] The transmitter 102 may include an FEC encoder 112 that encodes a data stream 110 with an error correction code and a modulator 114 that modulates an optical signal with the encoded data stream. The data stream 110 may be a binary data stream including a series of bits. Numerous FEC codes are known, each with different properties related to how the codes are generated and consequently how they perform. Examples of known error correcting codes include the linear and cyclic Hamming codes, the cyclic Bose-Chaudhuri-Hocquenghem (BCH) codes, the convolutional (Viterbi) codes, the cyclic Golay and Fire codes, and some newer codes such as the Turbo convolutional and product codes (TCC, TPC). Hardware and software configurations for implementing various error correcting codes in the encoder 112 and a corresponding decoder are known to those ordinary skill in the art.

[0016] The modulator 114 may be implemented using optical modulation techniques and equipment known to those skilled in the art. The modulator 114 may modulate encoded data on an optical wavelength, e.g. from a continuous-wave laser source, using any modulation format known in the art, including, but not limited to, On-Off-Keying (OOK), Phase Shift Keying (PSK), and Differential Phase-Shift-Keying (DPSK) formats. These formats may be implemented in one or more known variations including, but not limited to, Return-to-Zero (RZ), Non-Return to Zero (NRZ) and Chirped-Return-to-Zero (CRZ) variations. For example, DPSK formats, such as RZ-DPSK, have proven advantageous in connection with long-haul optical communication systems.

[0017] The receiver 104 includes a demodulator 120, a decision circuit 124, a FEC decoder 126, and a decision threshold adjuster 128. The demodulator 120 demodulates the encoded optical signal 108 to provide a demodulated signal 130, and may be implemented using techniques and equipment known to those skilled in the art. The decision circuit 124 receives the demodulated signal 130 as an input signal. The decision circuit 124 quantizes the signal 130 using a decision threshold, then re-times the quantized data stream to produce an output signal 132 including a stream of data bits, i.e. logic "1"s and "0"s. The decision circuit 124 may be implemented using techniques and detection circuitry known to those skilled in the art. In one embodiment, the decision circuit may include a comparator for comparing the signal 130 with a decision threshold and quantizing it to the stream of "1's" and "0's", followed by a re-timing circuit. In another embodiment, the decision circuit may include a D-Flip Flop (D-FF) with an input allowing for decision threshold adjustment and a clock recovery circuit. In yet another embodiment, the decision circuit may include a known Clock & Data Recovery circuit (CDR) with a decision threshold adjustment input.

[0018] The FEC decoder 126 receives the detected and re-timed signal 132 and decodes the signal 132 consistent with the implemented FEC scheme. The FEC decoder 126 provides one or more feedback signals, e.g. on feedback path 140, to the decision threshold adjuster 128. The feedback provided from the FEC decoder 126 to the decision threshold adjuster 128 includes information indicating the total number of "1"s and the total number of "0"s that were corrected by the FEC decoder 126 in particular sampling period, e.g. 1 second.

[0019] The total number of errors corrected by the FEC decoder 126 in a particular sampling period may be determined by adding the total number of corrected "1"s to the total number of corrected "0"s, or may be derived separately from information in the feedback signal from the FEC decoder 126. In one embodiment, adjustment of the decision threshold may occur only if the total number of reported errors over one or more sampling periods exceeds a predetermined error threshold. This approach may prevent unnecessary adjustments of the decision threshold when the total number of errors is very low (e.g. high Q) and the statistical validity of the information from the FEC is low. In another embodiment, adjustment may be performed continuously without regard to the total number of reported errors.

[0020] The decision threshold adjuster 128 is configured for adjusting the decision threshold in response to the feedback signal from the FEC decoder 126 to balance the number of corrected "1"s and the number of corrected "0"s. For any particular sampling period or group of sampling periods; the number of corrected "1"s may not exactly equal the number of corrected "0"s. As such, "balance" or "balancing" as used herein with reference to operation of decision threshold means to reduce the difference between the number of corrected "1"s and the number of corrected "0"s. In most systems, balancing the number of corrected "1's" and corrected "0's" reduces the total number of errors, thus improving the system performance:

[0021] FIG. 2 is an eye diagram 200 associated with a receiver consistent with the invention. Equipment for observing an eye diagram associated with a data signal is well known and commercially available. It is well known, for example, that an eye diagram associated with data signal may be observed on an oscilloscope by monitoring the data signal voltage on the vertical input of the oscilloscope and triggering on the data clock. An eye diagram is open or closed to an extent associated with signal degradation. An open eye diagram represents less signal degradation. Coriversely, a closed eye diagram represents more signal degradation.

[0022] As shown in FIG. 2, the decision threshold may be set to an initial value indicated on the eye diagram 200 by the dashed line 202. In the illustrated exemplary embodiment, the number of corrected "1"s may be greater than the number of corrected "0"s. This would indicate that the decision threshold is set too high. The decision threshold adjuster 128 may therefore decrease the decision threshold by a predetermined step to an adjusted value indicated by the solid line 204. In the succeeding sampling periods, the FEC decoder may provide feedback to the decision threshold adjuster indicating a smaller difference between the number of corrected "1"s and the number of corrected "0"s, e.g. more sampling periods may be required before the error threshold is exceeded.

[0023] FIG. 3 is a block flow diagram of one example of a decision threshold adjustment process 300 consistent with the present invention. The block flow diagram is illustrated with a particular sequence of steps. It can be appreciated, however, that the sequence of steps merely provides an example of how the general functionality described herein can be implemented. Further, each sequence of steps does not have to be executed in the order presented unless otherwise indicated.

[0024] In the illustrated exemplary embodiment, the decision threshold may be set to an initial predetermined voltage level 302, e.g. a mid-range vale. The total number of errors corrected by the FEC decoder 126 may be identified 304 and accumulated by the decision threshold adjuster 128 until a predetermined error threshold is reached 306. Accumulating errors until the error threshold is exceeded avoids consecutive threshold corrections in high Q systems wherein the number of errors reported in a particular sampling period is too low to be statistically important. As long at the total number of errors is not greater than a predetermined error threshold, flow may pass back to step 304 to continuously accumulate the errors until the total number of errors exceeds the predetermined error threshold.

[0025] The decision threshold update rate may thus be determined by the rate of errors. For systems operating a high Q (low level of errors) numerous sampling periods may pass before a total number of errors exceeds the predetermined error threshold. However for systems operating a low Q, the error threshold may be exceeded in the first sampling period, e.g. in 1 second.

[0026] Once the total number of errors exceeds the predetermined error threshold, the number of "1"s and the number of "0"s corrected by the FEC decoder 126 may be identified 308. If the total number of corrected "1 "s is equal to, or within a predetermined acceptable difference from, the total number of corrected "0"s 310, then the error counters may be reset 311 and flow may pass back to step 304. If the total number of corrected "1 "s is not equal to, or within the predetermined acceptable difference from the total number of corrected "0"s, then the decision threshold may be modified 312 to balance number of corrected "1"s with the number of corrected "0"s. The error counters may then be reset 311 and flow may pass back to step 304.

[0027] In one embodiment, the decision threshold may be modified proportionally to the ratio of corrected "1"s to corrected "0"s. This allows for large adjustments of the decision threshold when the ratio of corrected "1"s to corrected "0"s is large and smaller adjustments of the decision threshold when the difference is small. For example, the ratio of a difference between the total number of corrected "1"s and the total number of corrected "0"s to the total number of errors corrected, i.e. the error balance Er_bal, may be determined by:

$$Er\_bal = (Er1 - Er0)/(Er1 + Er0).$$

The decision threshold may be adjusted by calculating an incremental step that is proportional to the magnitude of the error balance Er_bal, e.g. by multiplying a default step value by the error balance Er_bal value. If the step is within predetermined acceptable range, the decision threshold may be adjusted by the calculated step. In receivers with fixed data polarity determined by the hardware configuration (e.g. true data stream applied to the decision circuit, or inverted data stream applied to the decision circuit), the direction of the adjustment (increment or decrement) may be determined by the sign of the error balance Er_bal.

[0028] In a system wherein data is modulated using a DPSK format, the polarity of the demodulated data, i.e. true or inverted, depends on the operating point of the DPSK demodulator. The direction of the threshold ad-

justment depends on the polarity of the data. In one embodiment, to account for unknown demodulated data polarity, the FEC decoder 126 may continuously flip the received data polarity until it identifies and decodes a frame. The feedback from the FEC decoder 126 to the decision threshold adjuster 128 may then indicate the polarity of the data. The polarity of the data at the input to the decision circuit, in conjunction with the sign of the error balance Er_bal, may determine the direction of the decision threshold adjustment. In another embodiment, the demodulator may be configured to alternate between valid operating points until an FEC frame is detected.

[0029] There is thus provided a method and apparatus for decision threshold control in an optical signal receiver in which there is provided an apparatus including a decision circuit for receiving an input signal and providing an output signal representing logic ones and zeros in response to comparison of the input signal with a decision threshold; a FEC decoder configured to decode the output signal and to provide a feedback signal representative of a number of errors corrected by the FEC decoder; and a decision threshold adjuster. The decision threshold adjuster is configured to adjust the decision threshold in response to the feedback signal to balance a number of ones corrected by the FEC decoder with a number of zeros corrected by the FEC decoder.

[0030] According to another aspect of the invention, there is provided an apparatus including a decision circuit for receiving an input signal and providing an output signal representing logic ones and zeros in response to comparison of the input signal with a decision threshold; a FEC decoder configured to decode the output signal and to provide a feedback signal representative of a number of errors corrected by the FEC decoder for each of a plurality of sampling periods; and a decision threshold adjuster. The decision threshold adjuster is configured to add the number errors corrected by the FEC decoder for each of the sampling periods to determine a total number of errors corrected by the FEC decoder over the plurality of sampling periods, the total number of errors including a total number of ones corrected by the FEC decoder over the plurality of sampling periods and a total number of zeros corrected by the FEC decoder over the plurality of sampling periods. The decision threshold adjuster is further configured to adjust the decision threshold to balance the total number of ones with the total number of zeros when the total number of the errors exceeds a predetermined error threshold.

[0031] According to another aspect of the invention there is provided a method of adjusting a decision threshold in an optical signal receiver. The method includes identifying a number of ones and a number of zeros corrected by an FEC decoder over a time period; and modifying the decision threshold in response to the number of ones and zeros corrected by the FEC decoder over the time period.

[0032] According to another aspect of the invention there is provided an optical communication system including an optical signal transmitter including an encoder for encoding a binary data stream and a modulator for modulating the encoded binary data stream to produce an encoded optical signal; and an optical signal receiver for receiving the encoded optical signal. The optical signal receiver includes a demodulator for demodulating the encoded optical signal to provide an input signal; a decision circuit for receiving the input signal and providing an output signal representing logic ones and zeros in response to comparison of the input signal with a decision threshold; a FEC decoder configured to decode the output signal and to provide a feedback signal representative of a number of errors corrected by the FEC decoder; and a decision threshold adjuster. The decision threshold adjuster is configured to adjust the decision threshold in response to the feedback signal to balance a number of ones corrected by the FEC decoder with a number of zeros corrected by the FEC decoder.

[0033] While the principles of the invention have been described herein, it is to be understood by those skilled in the art that this description is made only by way of example and not as a limitation as to the scope of the invention. Other embodiments are contemplated within the scope of the present invention in addition to the exemplary embodiments shown and described herein. Modifications and substitutions by one of ordinary skill in the art are considered to be within the scope of the present invention, which is not to be limited except by the following claims.

Claims

1. An apparatus comprising:

a decision circuit (124) for receiving an input signal (130) and providing an output signal (132) representing logic ones and zeros in response to comparison of said input signal with a decision threshold;

a FEC decoder (126) configured to determine a polarity of said input signal and decode said output signal and to provide feedback (140) representative of a number of errors corrected by said FEC decoder and indicating said polarity of said input signal; and

a decision threshold adjuster (128) configured to adjust said decision threshold in response to said feedback to balance a number of said ones corrected by said FEC decoder with a number of said zeros corrected by said FEC decoder,

characterised in that said decision threshold adjuster is configured to adjust said decision threshold in a direction determined by a sign of a difference between said total number of said ones and said total number of zeros and said polarity of said input signal indicated by said feedback.

2. An apparatus according to claim 1, wherein said decision threshold adjuster (128) is configured to adjust said decision threshold in proportion to a ratio of said number of said ones corrected by said FEC decoder (126) to said number of said zeros corrected by said FEC decoder.

3. An apparatus according to claim 1, wherein said number of said ones corrected by said FEC decoder (126) comprises a total number of said ones corrected by said FEC decoder over a plurality of sampling periods, and wherein said number of said zeros corrected by said FEC decoder comprises a total number of said zeros corrected by said FEC decoder over said plurality of sampling periods.

4. An apparatus according to claim 1, wherein said decision threshold adjuster (128) is configured to add said number errors corrected by said FEC decoder (126) over one or more sampling periods to determine a total number of said errors corrected by said FEC decoder over said one or more sampling periods, and wherein said decision threshold adjuster is configured to adjust said decision threshold when said total number of said errors exceeds a predetermined error threshold.

5. An apparatus according to claim 4, wherein said total number of said errors comprises a total number of said ones corrected by said FEC decoder (126) over said one or more sampling periods and a total number of said zeros corrected by said FEC decoder over said one or more sampling periods, and wherein said decision threshold adjuster (128) is configured to adjust said decision threshold to balance said total number of said ones with said total number of said zeros.

6. An apparatus according to claim 5, wherein said decision threshold adjuster (128) is configured to adjust said decision threshold in proportion to a ratio of a difference between said total number of said ones and said total number of said zeros to said total number of errors.

7. An apparatus according to claim 6, wherein said decision threshold adjuster (128) is configured to adjust said decision threshold in a direction determined by a sign of said difference between said total number of said corrected ones and said total number of corrected zeros.

8. A method of adjusting a decision threshold in an optical signal receiver, said method comprising:

receiving an input signal (130),
providing an output signal (132) representing logic ones and zeros in response to comparison of the input signal with a decision threshold;
decoding said output signal and determining a polarity of said input signal in an FEC decoder;
providing feedback (140) from said FEC decoder identifying a number of ones and a number of zeros corrected by an FEC decoder over a time period and indicating said polarity of input signal; and **characterized by** the step of
adjusting said decision threshold in a direction determined by a sign of a difference between said total number of said ones and said total number of zeros and said polarity of said input signal indicated by said feedback.

9. A method according to claim 8, said method further comprising identifying a total number of errors corrected by said FEC decoder over said time period, and wherein said modifying said decision threshold comprises modifying said decision threshold when said total number of errors exceeds a predetermined error threshold.

10. A method according to claim 8, wherein said modifying comprises modifying said decision threshold to balance said number of said ones with said number of said zeros.

11. A method according to claim 8, wherein said modifying comprises modifying said decision threshold in proportion to a ratio of said number of said ones to said number of said zeros.

12. An optical communication system comprising:

an optical signal transmitter (102) comprising an encoder (112) for encoding a binary data stream and a modulator (114) for modulating said encoded binary data stream to produce an encoded optical signal (108);
an optical signal receiver (104) for receiving said encoded optical signal, said optical signal receiver comprising:

a demodulator (120) for demodulating said encoded optical signal to provide an input signal (130);
a decision circuit (124) for receiving said input signal and providing an output signal (132) representing logic ones and zeros in response to comparison of said input signal with a decision threshold;
a FEC decoder (126) configured to determine a polarity of said input signal and decode said output signal and to provide feedback (140) representative of a number of errors corrected by said FEC decoder and indicating said polarity of said input signal; and

a decision threshold adjuster (128) configured to adjust said decision threshold in response to said feedback to balance a number of said ones corrected by said FEC decoder with a number of said zeros corrected by said FEC decoder,
characterised in that said decision threshold adjuster is configured to adjust said decision threshold in a direction determined by a sign of a difference between said number of said ones and said number of said zeros and said polarity of said input signal indicated by said feedback.

13. A system according to claim 12, wherein said decision threshold adjuster (128) is configured to adjust said decision threshold in proportion to a ratio of a difference between said number of said ones and said number of said zeros to a total number of errors.

14. A system according to claim 13, wherein said decision threshold adjuster (128) is configured to adjust said decision threshold in a direction determined by a sign of said difference between said number of said ones and said number of said zeros.

15. A system according to claim 12, wherein said number of said ones corrected by said FEC decoder (126) comprises a total number of said ones corrected by said FEC decoder over a plurality of sampling periods, and wherein said number of said zeros corrected by said FEC decoder comprises a total number of said zeros corrected by said FEC decoder over said plurality of sampling periods.

16. A system according to claim 12, wherein said decision threshold adjuster (128) is configured to add said number errors corrected by said FEC decoder (126) over one or more sampling periods to determine a total number of said errors corrected by said FEC decoder over said one or more sampling periods, and wherein said decision threshold adjuster is configured to adjust said decision threshold when said total number of said errors exceeds a predetermined error threshold.

17. A system according to claim 16, wherein said total number of said errors comprises a total number of said ones corrected by said FEC decoder (126) over said one or more sampling periods and a total number of said zeros corrected by said FEC decoder over said one or more sampling periods, and wherein said decision threshold adjuster (128) is configured to adjust said decision threshold to balance said total number of said ones with said total number of said zeros.

18. A system according to claim 17, wherein said decision threshold adjuster (128) is configured to adjust said decision threshold in proportion to a ratio of a difference between said total number of said ones and said total number of said zeros to the total number of errors.

Patentansprüche

1. Vorrichtung, umfassend:

eine Entscheidungsschaltung (124), um ein Eingangssignal (130) zu empfangen und als Reaktion auf einen Vergleich des Eingangssignals mit einem Entscheidungsschwellenwert ein Ausgangssignal (132) zu liefern, das logische Einsen und Nullen darstellt;
einen FEC-Decoder (126), der derart ausgebildet ist, dass er eine Polarität des Eingangssignals feststellt, das Ausgangssignal decodiert und ein Regelungssignal (140) liefert, das repräsentativ für eine Anzahl von Fehlern ist, die von dem FEC-Decoder korrigiert werden und welche die Polarität des Eingangssignals anzeigt; und
einen Entscheidungsschwellenwert-Regler (128), der derart ausgebildet ist, dass er den Entscheidungsschwellenwert als Reaktion auf das Regelungssignal anpasst, um eine Anzahl der vom FEC-Decoder korrigierten Einsen mit einer Anzahl der vom FEC-Decoder korrigierten Nullen abzugleichen,
dadurch gekennzeichnet, dass der Entscheidungsschwellenwert-Regler derart ausgebildet ist, dass er den Entscheidungsschwellenwert in eine Richtung anpasst, die durch ein Vorzeichen einer Differenz zwischen der Gesamtanzahl der Einsen und der Gesamtanzahl der Nullen und die Polarität des Eingangssignals bestimmt wird, welche durch das Regelungssignal angezeigt wird.

2. Vorrichtung nach Anspruch 1, wobei der Entscheidungsschwellenwert-Regler (128) derart ausgebildet ist, dass er den Entscheidungsschwellenwert proportional zu einem Verhältnis der Anzahl der vom FEC-Decoder (126) korrigierten Einsen zu der Anzahl der vom FEC-Decoder korrigierten Nullen anpasst.

3. Vorrichtung nach Anspruch 1, wobei die Anzahl der vom FEC-Decoder (126) korrigierten Einsen eine Gesamtanzahl von Einsen umfasst, die vom FEC-Decoder über eine Vielzahl von Abtastzeiträumen korrigiert werden, und wobei die Anzahl der vom FEC-Decoder korrigierten Nullen eine Gesamtanzahl von Nullen umfasst, die vom FEC-Decoder über die Vielzahl von Abtastzeiträumen korrigiert werden.

4. Vorrichtung nach Anspruch 1, wobei der Entscheidungsschwellenwert-Regler (128) derart ausgebildet ist, dass er die Anzahl der Fehler addiert, die vom FEC-Decoder (126) über einen oder mehrere Abtastzeiträume korrigiert werden, um eine Gesamtanzahl der Fehler zu bestimmen, die vom FEC-Decoder über den einen oder die mehreren Abtastzeiträume korrigiert werden, und wobei der Entscheidungsschwellenwert-Regler derart ausgebildet ist, dass er den Entscheidungsschwellenwert anpasst, wenn die Gesamtanzahl der Fehler einen Vorbestimmten Fehlerschwellenwert übersteigt.

5. Vorrichtung nach Anspruch 4, wobei die Gesamtanzahl der Fehler eine Gesamtanzahl der Einsen umfasst, die vom FEC-Decoder (126) über den einen oder die mehreren Abtastzeiträume korrigiert werden, und eine Gesamtanzahl der Nullen umfasst, die vom FEC-Decoder über den einen oder die mehreren Abtastzeiträume korrigiert werden und wobei der Entscheidungsschwellenwert-Regler (128) derart ausgebildet ist, dass er den Entscheidungsschwellenwert anpasst, um die Gesamtanzahl der Einsen mit der Gesamtanzahl der Nullen abzugleichen.

6. Vorrichtung nach Anspruch 5, wobei der Entscheidungsschwellenwert-Regler (128) derart ausgebildet ist, dass er den Entscheidungsschwellenwert proportional zu einem Verhältnis einer Differenz zwischen der Gesamtanzahl der Einsen und der Gesamtanzahl der Nullen zur Gesamtanzahl von Fehlern anpasst.

7. Vorrichtung nach Anspruch 6, wobei der Entscheidungsschwellenwert-Regler (128) derart ausgebildet ist, dass er den Entscheidungsschwellenwert in einer Richtung anpasst, die durch ein Vorzeichen der Differenz zwischen der Gesamtanzahl der korrigierte Einsen und der Gesamtanzahl der korrigierten Nullen bestimmt wird.

8. Verfahren zum Anpassen eines Entscheidungsschwellenwerts in einem optischen Signalempfänger, wobei das Verfahren umfasst:

das Empfangen eines Eingangssignals (130),
das Liefern eines Ausgangssignals (132), welches logische Einsen und Nullen darstellt, als Reaktion auf einen Vergleich des Eingangsignals mit einem Entscheidungsschwellenwert;
das Decodieren des Ausgangssignals und das Bestimmen einer Polarität des Eingangssignals in einem FEC-Decoder,
das Liefern eines Regelungssignals (140) vom FEC-Decoder, welches eine Anzahl von Einsen und eine Anzahl von Nullen identifiziert, die von einem FEC-Decoder über einen Zeitraum korrigiert werden, und welche die Polarität des Eingangssignals anzeigt; **gekennzeichnet durch** den folgenden Schritt:

das Anpassen des Entscheidungsschwellenwerts in einer Richtung, die **durch** ein Vorzeichen einer Differenz zwischen der Gesamtanzahl der Einsen und der Gesamtanzahl der Nullen und die Polarität des Eingangssignals bestimmt wird, welche durch das Regelungssignal angezeigt wird.

9. Verfahren nach Anspruch 8, wobei das Verfahren darüber hinaus das Identifizieren einer Gesamtanzahl von Fehlern umfasst, die vom FEC-Decoder über den Zeitraum korrigiert werden, und wobei das Modifizieren des Entscheidungsschwellenwerts ein Modifizieren des Entscheidungsschwellenwerts umfasst, wenn die Gesamtanzahl von Fehlern einen Vorbestimmten Fehlerschwellenwert übersteigt.

10. Verfahren nach Anspruch 8, wobei das Modifizieren ein Modifizieren des Entscheidungsschwellenwerts umfasst, um die Anzahl der Einsen mit der Anzahl der Nullen abzugleichen.

11. Verfahren nach Anspruch 8, wobei das Modifizieren ein Modifizieren des Entscheidungsschwellenwerts proportional zu einem Verhältnis der Anzahl der Einsen zur Anzahl der Nullen umfasst.

12. Optisches Kommunikationssystem, umfassend:

einen optischen Signalsender (102), umfassend einen Codierer (112) zum Codieren eines binären Datenstroms und einen Modulator (114) zum Modulieren des codierten binären Datenstroms, um ein codiertes optisches Signal (108) zu erzeugen;
einen optischen Signalempfänger (104) zum Empfangen des codierten optischen Signals, wobei der optische Signalempfänger umfasst:

einen Demodulator (120) zum Demodulieren des codierten optischen Signals, um ein Eingangssignal (130) zu liefern;
eine Entscheidungsschaltung (124), um das Eingangssignal zu empfangen und als Reaktion auf einen Vergleich des Eingangssignals mit einem Entscheidungsschwellenwert ein Ausgangssignal (132) zu liefern, welches logische Einsen und Nullen darstellt;
einen FEC-Decoder (126), der derart ausgebildet ist, dass er eine Polarität des Eingangssignals feststellt, das Ausgangssignal decodiert und ein Regelungssignal (140) liefert, das repräsentativ für eine Anzahl von Fehlern ist, die von dem FEC-De-

coder korrigiert werden, und welche die Polarität des Eingangssignals anzeigt; und
einen Entscheidungsschwellenwert-Regler (128), der derart ausgebildet ist, dass er den Entscheidungsschwellenwert als Reaktion auf das Regelungssignal anpasst, um eine Anzahl der vom FEC-Decoder korrigierten Einsen mit einer Anzahl der vom FEC-Decoder korrigierten Nullen abzugleichen,
dadurch gekennzeichnet, dass der Entscheidungsschwellenwert-Regler derart ausgebildet ist, dass er den Entscheidungsschwellenwert in eine Richtung anpasst, die durch ein Vorzeichen einer Differenz zwischen der Anzahl der Einsen und der Anzahl der Nullen und durch die Polarität des Eingangssignals bestimmt wird, welche durch das Regelungssignal angezeigt wird.

13. System nach Anspruch 12, wobei der Entscheidungsschwellenwert-Regler (128) derart ausgebildet ist, dass er den Entscheidungsschwellenwert proportional zu einem Verhältnis einer Differenz zwischen der Anzahl der Einsen und der Anzahl der Nullen zu einer Gesamtanzahl von Fehlern anpasst.

14. System nach Anspruch 13, wobei der Entscheidungsschwellenwert-Regler (128) derart ausgebildet ist, dass er den Entscheidungsschwellenwert in eine Richtung anpasst, die durch ein Vorzeichen der Differenz zwischen der Anzahl der Einsen und der Anzahl der Nullen bestimmt wird.

15. System nach Anspruch 12, wobei die Anzahl der vom FEC-Decoder (126) korrigierten Einsen eine Gesamtanzahl der Einsen umfasst, die vom FEC-Decoder über eine Vielzahl von Abtastzeiträumen korrigiert werden, und wobei die Anzahl der vom FEC-Decoder korrigierten Nullen eine Gesamtanzahl von Nullen umfasst, die vom FEC-Decoder über die Vielzahl von Abtastzeiträumen korrigiert werden.

16. System nach Anspruch 12, wobei der Entscheidungsschwellenwert-Regler (128) derart ausgebildet ist, dass er die Anzahl der Fehler addiert, die vom FEC-Decoder (126) über einen oder mehrere Abtastzeiträume korrigiert werden, um eine Gesamtanzahl der Fehler zu bestimmen, die vom FEC-Decoder über den einen oder die mehreren Abtastzeiträume korrigiert werden, und wobei der Entscheidungsschwellenwert-Regler derart ausgebildet ist, dass er den Entscheidungsschwellenwert anpasst, wenn die Gesamtanzahl der Fehler einen Vorbestimmten Fehlerschwellenwert übersteigt.

17. System nach Anspruch 16, wobei die Gesamtanzahl der Fehler eine Gesamtanzahl der Einsen umfasst, die vom FEC-Decoder (126) über den einen oder die mehreren Abtastzeiträume korrigiert werden, und eine Gesamtanzahl der Nullen umfasst, die vom FEC-Decoder über den einen oder die mehreren Abtastzeiträume korrigiert werden und wobei der Entscheidungsschwellenwert-Regler (128) derart ausgebildet ist, dass er den Entscheidungsschwellenwert anpasst, um die Gesamtanzahl der Einsen mit der Gesamtanzahl der Nullen abzugleichen.

18. System nach Anspruch 17, wobei der Entscheidungsschwellenwert-Regler (128) derart ausgebildet ist, dass er den Entscheidungsschwellenwert proportional zu einem Verhältnis einer Differenz zwischen der Gesamtanzahl der Einsen und der Gesamtanzahl der Nullen zur Gesamtanzahl der Fehler anpasst.

Revendications

1. Dispositif comprenant :

- un circuit de décision (124) destiné à recevoir un signal d'entrée (130) et à fournir un signal de sortie (132) représentant des zéros et des uns logiques, en réponse à la comparaison dudit signal d'entrée à un seuil de décision ;
- un décodeur FEC (126) configuré de façon à définir la polarité dudit signal d'entrée et à décoder ledit signal de sortie, et à fournir un retour d'informations (140) représentatif du nombre d'erreurs corrigées par ledit décodeur FEC et indiquant la polarité dudit signal d'entrée ; et
- un dispositif d'ajustement (128) du seuil de décision configuré de façon à ajuster ce seuil de décision en réponse audit retour d'informations, afin d'équilibrer le nombre desdits uns corrigés par ledit décodeur FEC et le nombre desdits zéros corrigés par ledit décodeur FEC,
caractérisé en ce que ledit dispositif d'ajustement du seuil de décision est configuré de façon à ajuster ce seuil de décision en fonction du signe de la différence entre ledit nombre total de uns et ledit nombre total de zéros, et de la polarité dudit signal d'entrée indiqués par ledit retour d'informations.

2. Dispositif selon la revendication 1, dans lequel ledit dispositif d'ajustement (128) du seuil de décision est configuré de façon à ajuster ce seuil de décision proportionnellement au rapport du nombre desdits uns corrigés par ledit décodeur FEC sur le nombre desdits zéros corrigés par ledit décodeur FEC.

3. Dispositif selon la revendication 1, dans lequel le nombre desdits uns corrigés par ledit décodeur FEC (126) comprend le nombre total desdits uns corrigés par ledit décodeur FEC sur une pluralité de périodes

d'échantillonnage, et dans lequel le nombre desdits zéros corrigés par ledit décodeur FEC comprend le nombre total desdits zéros corrigés par ledit décodeur FEC sur ladite pluralité de périodes d'échantillonnage.

4. Dispositif selon la revendication 1, dans lequel ledit dispositif d'ajustement (128) du seuil de décision est configuré de façon à ajouter ledit nombre d'erreurs corrigées par ledit décodeur FEC (126) sur une ou plusieurs périodes d'échantillonnage, afin de définir le nombre total desdites erreurs corrigées par ledit décodeur FEC sur ladite une ou plusieurs périodes d'échantillonnage, et dans lequel ledit dispositif d'ajustement du seuil de décision est configuré de façon à ajuster ce seuil de décision lorsque le nombre total desdites erreurs dépasse un seuil d'erreurs prédéfini.

5. Dispositif selon la revendication 4, dans lequel ledit nombre total d'erreurs comprend le nombre total desdits uns corrigés par ledit décodeur FEC (126) sur ladite une ou plusieurs périodes d'échantillonnage, et le nombre total desdits zéros corrigés par ledit décodeur FEC sur ladite une ou plusieurs périodes d'échantillonnage, et dans lequel ledit dispositif d'ajustement (128) du seuil de décision est configuré de façon à ajuster ce seuil de décision afin d'équilibrer ledit nombre total de uns et ledit nombre total de zéros.

6. Dispositif selon la revendication 5, dans lequel ledit dispositif d'ajustement (128) du seuil de décision est configuré de façon à ajuster ce seuil de décision proportionnellement au rapport de la différence entre ledit nombre total de uns et ledit nombre total de zéros, sur ledit nombre total d'erreurs.

7. Dispositif selon la revendication 6, dans lequel ledit dispositif d'ajustement (128) du seuil de décision est configuré de façon à ajuster ce seuil de décision en fonction du signe de la différence entre ledit nombre total de uns corrigés et ledit nombre total de zéros corrigés.

8. Procédé d'ajustement du seuil de décision dans un récepteur de signaux optiques, ledit procédé consistant à :

- recevoir un signal d'entrée (130) ;
- fournir un signal de sortie (132) représentant des zéros et des uns logiques, en réponse à la comparaison du signal d'entrée à un seuil de décision ;
- décoder ledit signal de sortie et déterminer la polarité dudit signal d'entrée dans un décodeur FEC ;
- fournir à partir dudit décodeur FEC un retour d'informations (140) identifiant le nombre de uns et le nombre de zéros corrigés par le décodeur FEC sur une certaine période et indiquant la polarité du signal d'entrée ; et **caractérisé par** l'étape consistant à :

ajuster ledit seuil de décision en fonction du signe de la différence entre ledit nombre total de uns et ledit nombre total de zéros, et de la polarité dudit signal d'entrée indiqués par ledit retour d'informations.

9. Procédé selon la revendication 8, consistant en outre à identifier le nombre total d'erreurs corrigées par ledit décodeur FEC sur ladite période, et dans lequel ladite modification dudit seuil de décision consiste à modifier celui-ci lorsque ledit nombre total d'erreurs dépasse un seuil d'erreurs prédéfini.

10. Procédé selon la revendication 8, dans lequel ladite modification consiste à modifier ledit seuil de décision afin d'équilibrer ledit nombre de uns et ledit nombre de zéros.

11. Procédé selon la revendication 8, dans lequel ladite modification consiste à modifier ledit seuil de décision proportionnellement au rapport dudit nombre de uns sur ledit nombre de zéros.

12. Système de communication optique comprenant :

- un émetteur de signaux optiques (102) comprenant un encodeur (112) destiné à encoder un flux de données binaires, et un modulateur (114) destiné à moduler ledit flux de données binaires encodé afin de produire un signal optique encodé (108) ;
- un récepteur de signaux optiques (104) destiné à recevoir ledit signal optique encodé, ledit récepteur de signaux optiques comprenant :

• un démodulateur (120) destiné à démoduler ledit signal optique encodé pour fournir un signal d'entrée (130) ;
• un circuit de décision (124) destiné à recevoir ledit signal d'entrée et à fournir un signal de sortie (132) représentant des zéros et des uns logiques, en réponse à la comparaison dudit signal d'entrée à un seuil de décision ;
• un décodeur FEC (126) configuré de façon à définir la polarité dudit signal d'entrée et à décoder ledit signal de sortie, et à fournir un retour d'informations (140) représentatif du nombre d'erreurs corrigées par ledit décodeur FEC et indiquant la polarité dudit signal d'entrée ; et
• un dispositif d'ajustement (128) du seuil

de décision configuré de façon à ajuster ce seuil de décision en réponse audit retour d'informations, afin d'équilibrer le nombre desdits uns corrigés par ledit décodeur FEC et le nombre desdits zéros corrigés par ledit décodeur FEC,

caractérisé en ce que ledit dispositif d'ajustement du seuil de décision est configuré de façon à ajuster ce seuil de décision en fonction du signe de la différence entre ledit nombre total de uns et ledit nombre total de zéros, et de la polarité dudit signal d'entrée indiqués par ledit retour d'informations.

13. Système selon la revendication 12, dans lequel ledit dispositif d'ajustement (128) du seuil de décision est configuré de façon à ajuster ce seuil de décision proportionnellement au rapport de la différence entre ledit nombre de uns et ledit nombre de zéros, sur le nombre total d'erreurs.

14. Système selon la revendication 13, dans lequel ledit dispositif d'ajustement (128) du seuil de décision est configuré de façon à ajuster ce seuil de décision en fonction du signe de la différence entre ledit nombre de uns et ledit nombre de zéros.

15. Système selon la revendication 12, dans lequel ledit nombre de uns corrigés par ledit décodeur FEC (126) comprend le nombre total de uns corrigés par ledit décodeur FEC sur une pluralité de périodes d'échantillonnage, et dans lequel ledit nombre de zéros corrigés par ledit décodeur FEC comprend le nombre total de zéros corrigés par ledit décodeur FEC sur ladite pluralité de périodes d'échantillonnage.

16. Système selon la revendication 12, dans lequel ledit dispositif d'ajustement (128) du seuil de décision est configuré de façon à ajouter ledit nombre d'erreurs corrigées par ledit décodeur FEC (126) sur une ou plusieurs périodes d'échantillonnage, afin de définir le nombre total desdites erreurs corrigées par ledit décodeur FEC sur ladite une ou plusieurs périodes d'échantillonnage, et dans lequel ledit dispositif d'ajustement du seuil de décision est configuré de façon à ajuster ce seuil de décision lorsque ledit nombre total d'erreurs dépasse un seuil d'erreurs prédéfini.

17. Système selon la revendication 16, dans lequel ledit nombre total desdites erreurs comprend le nombre total de uns corrigés par ledit décodeur FEC (126) sur ladite une ou plusieurs périodes d'échantillonnage, et le nombre total de zéros corrigés par ledit décodeur FEC sur ladite une ou plusieurs périodes d'échantillonnage, et dans lequel ledit dispositif d'ajustement (128) du seuil de décision est configuré de façon à ajuster ce seuil de décision afin d'équilibrer ledit nombre total de uns et ledit nombre total de zéros.

18. Système selon la revendication 17, dans lequel ledit dispositif d'ajustement (128) du seuil de décision est configuré de façon à ajuster ce seuil de décision proportionnellement au rapport de la différence entre ledit nombre total de uns et ledit nombre total de zéros, sur le nombre total d'erreurs.

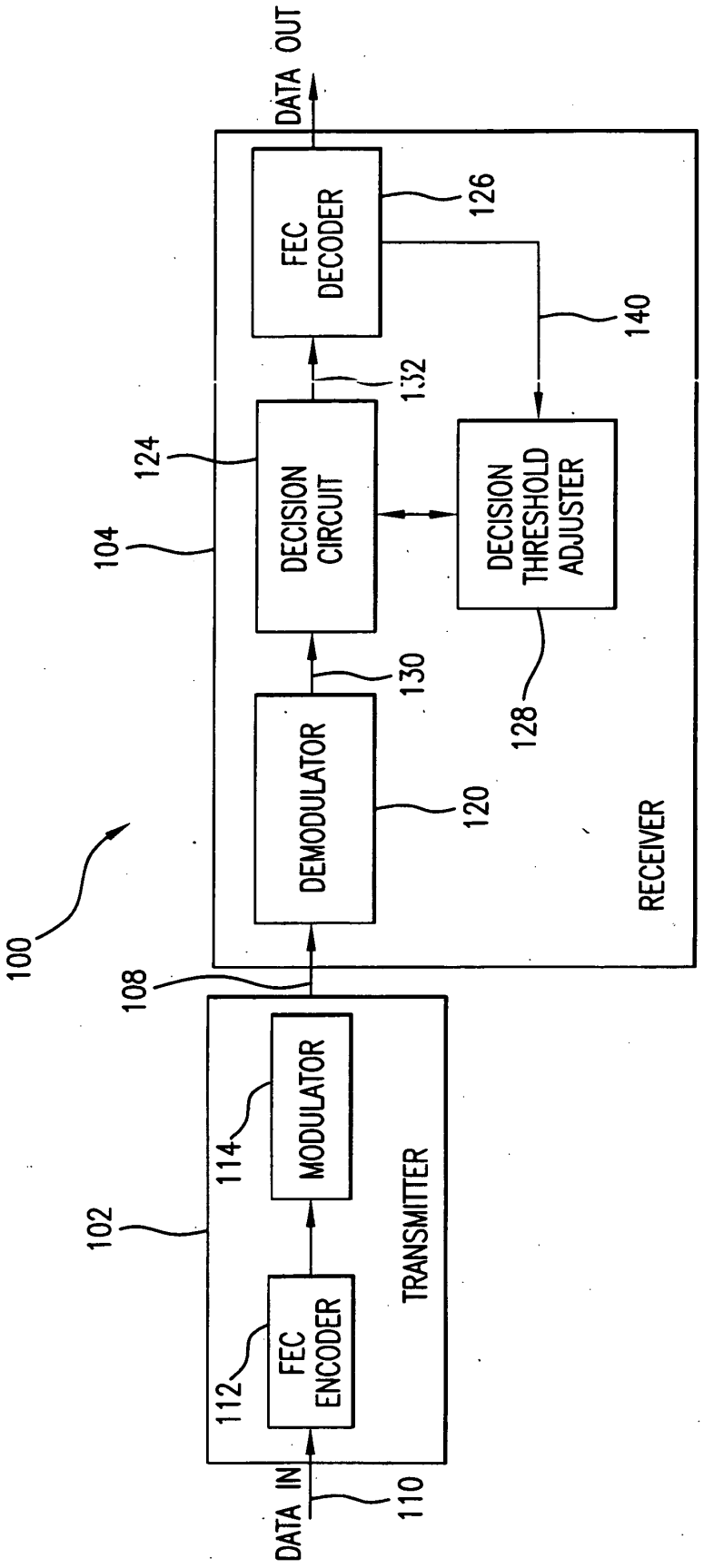
DATA OUT
FEC DECODER
126
140
132
124
DECISION CIRCUIT
DECISION THRESHOLD ADJUSTER
104
130
128
DEMODULATOR
120
RECEIVER
100
108
MODULATOR
114
102
TRANSMITTER
FEC ENCODER
112
DATA IN
110

FIG. 1

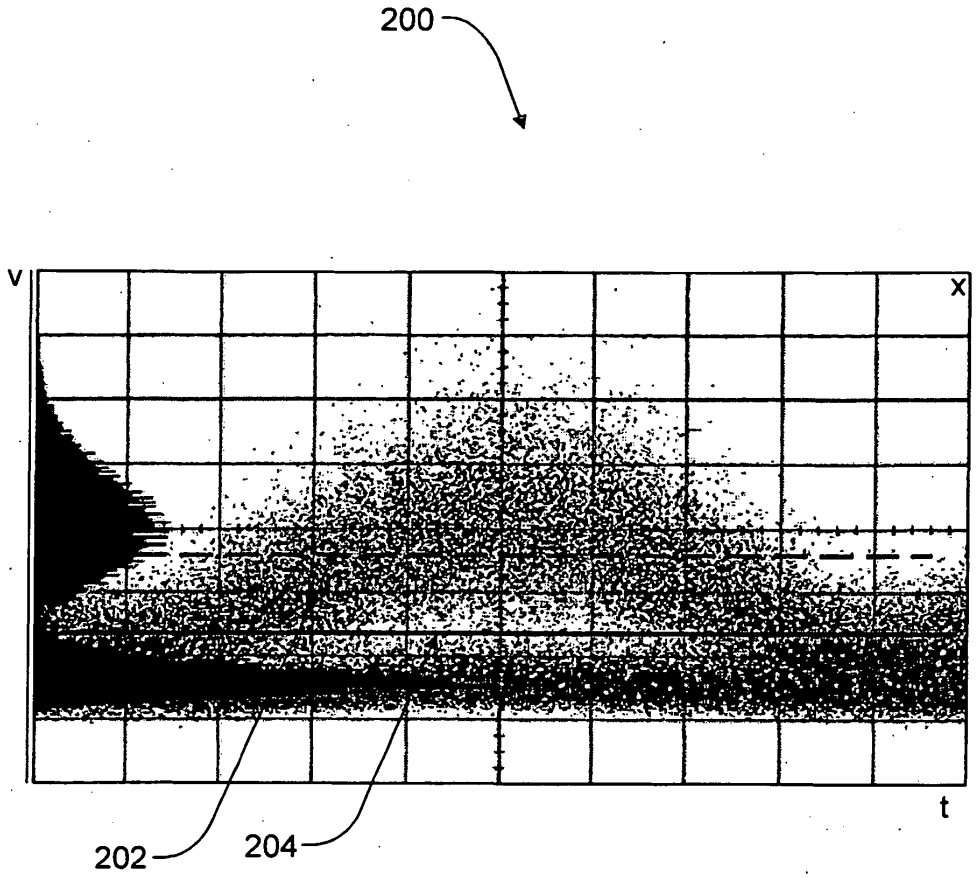

FIG.2

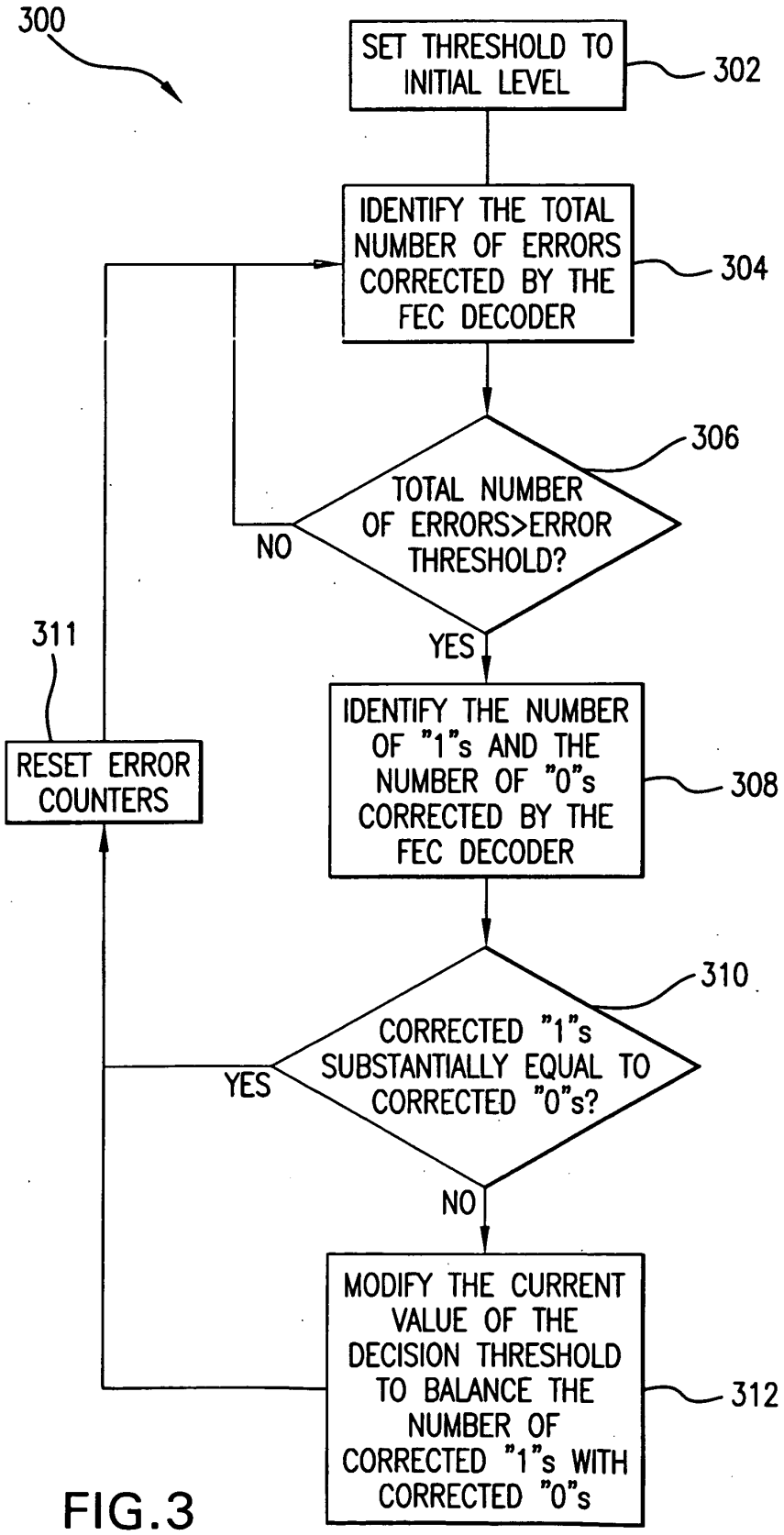
300
SET THRESHOLD TO INITIAL LEVEL
302
IDENTIFY THE TOTAL NUMBER OF ERRORS CORRECTED BY THE FEC DECODER
304
306
TOTAL NUMBER OF ERRORS>ERROR THRESHOLD?
NO
YES
311
RESET ERROR COUNTERS
IDENTIFY THE NUMBER OF "1"s AND THE NUMBER OF "0"s CORRECTED BY THE FEC DECODER
308
310
CORRECTED "1"s SUBSTANTIALLY EQUAL TO CORRECTED "0"s?
YES
NO
MODIFY THE CURRENT VALUE OF THE DECISION THRESHOLD TO BALANCE THE NUMBER OF CORRECTED "1"s WITH CORRECTED "0"s
312

FIG.3

REFERENCES CITED IN THE DESCRIPTION

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Patent documents cited in the description

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