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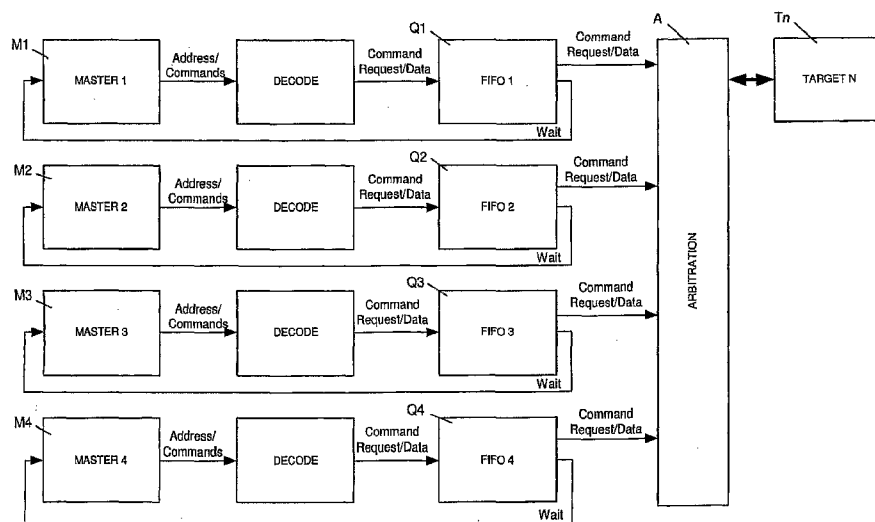
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(57) Abstract: A system and method for slave-side arbitration includes a plurality of master devices, a target device, and an arbitrator for arbitrating access to the target device by the master devices. Queuing devices, such as FIFO buffers, are respectively associated with master devices and communicate information regarding retained target device access requests to the arbitrator. The information may be communicated to the arbitrator by sending it to the arbitrator, or may be provided as status information that is accessed by the arbitrator. The arbitrator uses an arbitration scheme and information regarding retained transaction requests to determine which master device should be granted access to the target device. The arbitration system and method can be used in an integrated circuit with multiple embedded processors, and can be implemented in a document processing system to improve overall system performance over conventional slave-side arbitration schemes.

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**INTERNATIONAL SEARCH REPORT**

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| <b>A. CLASSIFICATION OF SUBJECT MATTER</b><br>INV. G06F13/16  |   |                       |
| According to International Patent Classification (IPC) or to both national classification and IPC   |   |                       |
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| Electronic data base consulted during the international search (name of data base and, where practical, search terms used)<br>EPO-Internal, WPI Data  |   |                       |
| <b>C. DOCUMENTS CONSIDERED TO BE RELEVANT</b>   |   |                       |
| Category*   | Citation of document, with indication, where appropriate, of the relevant passages  | Relevant to claim No. |
| X   | WO 01/16770 A (INTEL CORP [US]; ADILETTA MATTHEW J [US]; WHEELER WILLIAM [US]; WOLRIC) 8 March 2001 (2001-03-08)<br>page 1, line 26 - page 2, line 7; figures 1-4<br>page 33, line 7 - page 35, line 20<br>page 37  | 1-30                  |
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| <input type="checkbox"/> Further documents are listed in the continuation of Box C. <span style="margin-left: 200px;"><input checked="" type="checkbox"/> See patent family annex.</span>   |   |                       |
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