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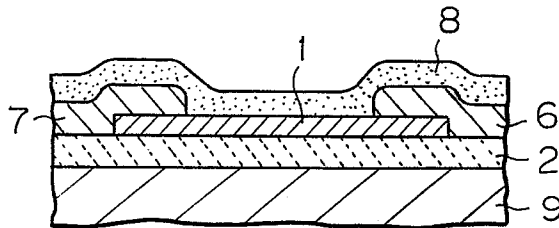
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54 **Method of blowing fuses in an IC, for example for writing information into a fuse-type ROM.**

57 Fuses (1) are formed on an insulating film (2), are connected to conductor lines (6, 7) and are covered by a protective film (8). A ramp voltage is applied so as to blow the fuses without breaking the protective film.



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METHOD OF BLOWING FUSES IN AN IC, FOR EXAMPLE
FOR WRITING INFORMATION INTO A FUSE-TYPE ROM

The present invention relates to a method of blowing
fuses in an IC, for example a fuse-type ROM,
5 more particularly to a method of electrically blowing
(i.e., opening) a fuse formed in a memory device for
programming.

Semiconductor memory devices provided with fuses
10 include a fuse-type ROM and a random access memory (RAM)
with redundant circuits. In a fuse-type ROM (i.e., a
fuse-link-programmable ROM), the fuses are selectively
blown in order to write information, and in a RAM with
redundant circuits, the fuses are selectively blown in
15 order to replace a row or column containing a bad bit
(i.e., defective memory cell) with a spare row or column:
the replaced portion of the RAM can be regarded as a ROM
portion. The fuse blowout is achieved by applying
excess current and voltage to the fuse.

20 In general, a fuse in the memory device is made of
a fusible material, e.g., polycrystalline silicon, is
formed on an insulating film, and is covered with a
protective film, e.g., a phosphosilicate glass (PSG)
film (reference example, cf. David W. Greve, "Programming
25 Mechanism of Polysilicon Resistor Fuses", IEEE Transac-
tions on Electron Devices, vol. ED-29, No. 4, April 1982,
pp. 719 to 724, particularly, Fig. 1b). Usually the
fuse has the shape of a bow-tie, i.e., a long narrow
center portion and two wider pad portions. The two pad
30 portions are joined by the center portion and are
connected with conductor lines, e.g., aluminum lines,
respectively.

The fuse is blown by feeding it an excess current,

and a pulse voltage is adopted as the applied voltage. When the fuse is blown, it bursts in such a manner that the protective PSG film is also broken, forming an opening in the film. This opening must be filled by
5 re-forming the protective PSG film to prevent the ingress of contaminants.

An embodiment of the present invention can provide a method of electrically blowing a fuse without breaking a
10 protective film formed on the fuse, in order to write information into a memory device.

This and other features of an embodiment of the present invention are attained by a method of writing information into a fuse-type ROM provided with fuses by selectively
15 and electrically blowing the fuses which are formed on an insulating film on a substrate, are connected to conductor lines, and are covered by a protective film, characterized in that a ramp voltage is used as an applied voltage for blowing the fuses, to blow the fuses
20 without breaking the protective film.

It is preferable that the ramp voltage increase, e.g. linearly, in value at a rate of from 10^3 to 10^5 V/sec to a peak value. If the increase rate for the voltage is more than 10^5 V/sec, such voltage is similar to a
25 pulse voltage and the protective film covering the fuses will be broken in such a manner as to form openings in the film. If the increase rate for the voltage is from about 10 to 10^3 V/sec, according to experiments carried out by the inventor, the protective film is sometimes
30 broken. Furthermore, if the increase rate for the voltage is less than 5 V/sec, the aluminum positive pole line of the conductor lines becomes molten and flows to form a very thin aluminum film, so that a short condition occurs and the fuse is not blown.

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The present invention will be more apparent from the description of the exemplary embodiments set forth

below, with reference to the accompanying drawings, in which:

Fig. 1 is a partial plan view of a memory device provided with a fuse;

5 Fig. 2 is a sectional view taken on line II-II in Fig. 1;

Fig. 3 is a waveform diagram of a ramp voltage for blowing fuses according to an embodiment of the present invention;

10 Fig. 4 is an another wave form diagram of a ramp voltage according to an embodiment of the present invention ;

Fig. 5 is a waveform diagram of a conventional pulse voltage for blowing fuses;

Fig. 6 is a partial plan view of a memory device provided with a fuse, used for experiments;

15 Fig. 7 is an scanning electron microscope (SEM) photograph of a fuse after it has been blown with a pulse voltage;

Fig. 8 is an enlarged SEM photograph of the fuse shown in Fig. 7;

20 Fig. 9 is an SEM photograph of a fuse after it has been blown with a ramp voltage;

Fig. 10 is a microphotograph of a fuse with a protective film after it has been blown with a ramp voltage.

25 Referring to Figs. 1 and 2, a fuse section of a memory device comprises, in general, a fuse 1 (of, e.g., polycrystalline silicon), an insulating film 2 (of, e.g., SiO₂) under the fuse, a protective film 8 (of, e.g., PSG) on the fuse, and conductor lines 6 and 7 (of, e.g., aluminum) connected with the fuse. The fuse 1 has a bow-tie shape consisting of a long narrow center portion 3 and two wider pad portions 4 and 5 which are joined to the center portion and are connected with the conductor lines 6 and 7, respectively. The insulating layer 2 is formed on a substrate 9 (of, e.g., single crystalline silicon). Figure 1 shows the fuse section

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without the protective film 8.

The fuse section is produced in accordance with a conventional process as follows. First, the SiO_2 insulating film 2 is formed on the silicon substrate (wafer) 9 by a thermal oxidizing method or a chemical vapor deposition (CVD) method. A polycrystalline silicon layer is formed on the insulating film 2 and is shaped into a fuse 1, as shown in Fig. 1, by a conventional lithographic method (e.g., a photoetching method). The shape of the fuse 1 usually consists of a long narrow center portion 3, which is the portion to be broken, and square pad portions 4 and 5, which are joined by the center portion 3. It is possible to use nickel-chromium alloy (NiCr), titanium-tungsten alloy (TiW), or platinum silicide (PtSi) as the fuse material instead of polycrystalline silicon.

Next, in order to form the conductor lines 6 and 7, an aluminum or aluminum-base alloy (e.g., Al-2% Si, Al-1% Cu) is deposited on the exposed surface and is shaped into a predetermined pattern by a conventional lithographic method (e.g., a photoetching method). The aluminum conductor lines 6 and 7 are electrically connected to the pad portions 4 and 5 of the fuse 1. It is possible to form each of the conductor lines 6 and 7 as a doped polycrystalline silicon line and an aluminum (or an aluminum-base alloy) piece which lies on each of the pad portions and on each doped polycrystalline silicon line, connecting them together.

Finally, the PSG protective film 8 is formed on the exposed surfaces of the fuse 1, the conductor lines 6 and 7, and the insulating film 2, by a CVD method. It is possible to use silicon dioxide or silicon nitride as the material for the protective film instead of PSG.

A ramp voltage is applied to the formed polycrystalline silicon fuse 1. This ramp voltage is increased at a constant rate of from 10^3 to 10^5 V/sec, according to the present invention, so as to blow the

center portion 3 of the fuse 1. The ramp voltage has, for example, a waveform as shown in Fig. 3, and such a ramp voltage can be obtained by a ramp generator. Since the fuse 1 is blown before the ramp voltage attains its peak value, the ramp voltage may have another waveform, e.g. as shown in Fig. 4. When the fuse 1 is blown in accordance with the present invention, it is found that an opening is not formed at the portion of the PSG protective film 8 corresponding to the blown portion of the fuse 1. From observation of the blown fuse 1, it is found that aluminum flows thinly from the positive pole side of the conductor line 6 (or 7) to the negative pole side of the other conductor line 7 (or 6) for an instant at the initial stage of the melting of the polycrystalline silicon of the fuse 1, forming a very thin aluminum film, and subsequently the fuse is blown. It is thought that part of the current flows through this very thin aluminum film, thereby decreasing the heating rate immediately before the blowout, so that the PSG protective film 8 is not broken.

Where the formed fuse is blown by applying a pulse voltage, as shown in Fig. 5, a thin aluminum film is not formed, as there is no flow of aluminum, and an opening is formed at a portion of the PSG protective film 8 corresponding to the blown portion of the fuse 1.

Example

A polycrystalline silicon fuse, as shown in Fig. 6, is produced and is electrically blown with a pulse voltage or a ramp voltage.

An SiO_2 film 32 (having a thickness of $1.0 \mu\text{m}$) is formed on a silicon wafer (not shown) by a thermal oxidizing method. Two grooves 38 and 39 (having a depth of $0.7 \mu\text{m}$, a width A of $5 \mu\text{m}$, and a distance B between the grooves of $6 \mu\text{m}$) are formed by selectively etching the SiO_2 film 32. A polycrystalline silicon layer (having a thickness of $0.4 \mu\text{m}$) is deposited on the SiO_2 film 32 and is selectively etched to form a bow-tie

shaped fuse 31 (Fig. 6). The fuse 31 consists of a long narrow center portion 33 (having a width W of $6 \mu\text{m}$) and two pad portions 34 and 35. An aluminum film (having a thickness of $1.0 \mu\text{m}$) is deposited on the surfaces of the SiO_2 film 32 and the fuse 31 by a vapor deposition method and is selectively etched to form two conductor lines 36 and 37. The end portion of each of the aluminum conductor lines 36 and 37 corresponds to and lies on about half of the pad portions 34 and 35, respectively. A PSG protective film (not shown) having a thickness of $1.0 \mu\text{m}$ is formed on the exposed surfaces of the fuse 31, the SiO_2 film 32, and the aluminum conductor lines 36 and 37, by a CVD method.

When a pulse voltage, as shown in Fig. 5, is applied across the conductor lines 36 and 37 to blow the formed polycrystalline fuse 31, the center portion 33 is blown between the grooves 38 and 39 and simultaneously the PSG film is also broken to form an opening, as can be seen in the SEM photographs shown in Figs. 7 and 8.

When a ramp voltage which is increased at a constant rate of 10^4 V/sec to a peak value of 34 V is applied across the conductor lines 36 and 37, in accordance with the present invention, the center portion 33 is blown at a voltage of 27 V , but there is no corresponding opening in the PSG film on the blown fuse, as can be seen in the SEM photograph shown in Fig. 9. The fuse is examined with an optical microphotograph. The result of this examination can be seen in the photograph shown in Fig. 10. The center portion 33 of polycrystalline silicon is clearly broken (opened), and the conductor lines 36 and 37 are disconnected.

In the case of the method of blowing a fuse according to the present invention, the fuse can be blown without breaking the protective film formed on the fuse, so that it is not necessary to re-form the protective film.

It will be obvious that the present invention is

not restricted to the above-mentioned embodiments and that many variations are possible for persons skilled in the art without departing from the scope of the invention.

CLAIMS

1. A method of blowing fuses in an integrated circuit provided with fuses which are formed on an insulating film on a substrate, are connected to conductor
5 lines, and are covered by a protective film, comprising the step of selectively and electrically blowing said fuses without breaking said protective film by using a ramp voltage as an applied voltage.
2. A method according to claim 1, wherein said
10 ramp voltage increases linearly in value at a rate of from 10^3 to 10^5 V/sec to a peak value.
3. A method according to claim 2, wherein said fuse is blown before said applied voltage attains the peak value.
- 15 4. A method according to any preceding claim, wherein said fuses are made of a material selected from the group consisting of polycrystalline silicon, NiCr, TiW and PtSi.
5. A method according to any preceding claim,
20 wherein at least parts of respective said conductor lines are made of a metal selected from the group consisting of aluminium and aluminium-base alloy.
6. A method according to any preceding claim,
25 wherein each of said conductor lines comprises a doped polycrystalline silicon line and an aluminium piece connecting the fuse and the doped polycrystalline silicon line.
7. A method according to claim 1, wherein said protective film is made of a material selected from the
30 group consisting of phosphosilicate glass, silicon dioxide, and silicon nitride.
8. A method according to any preceding claim, employed for writing information into a fuse type ROM.

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Fig. 1

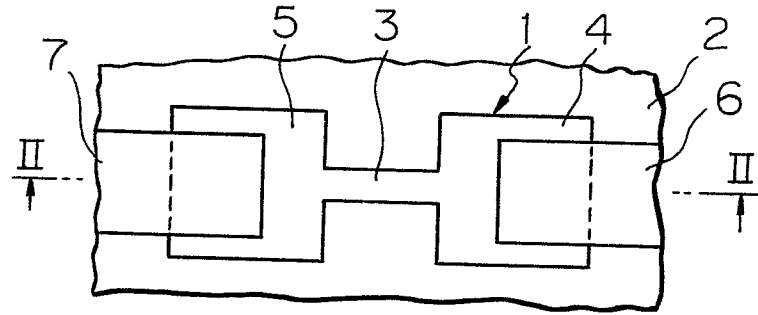


Fig. 2

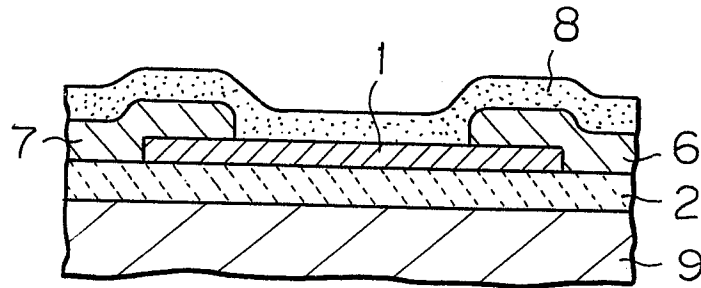


Fig. 3

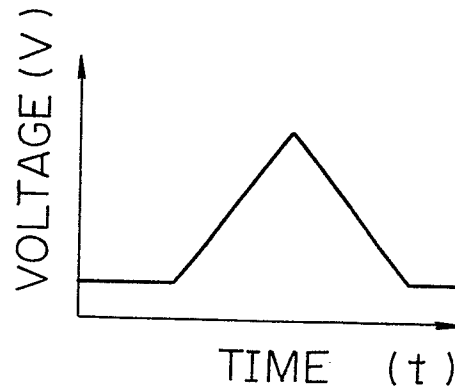
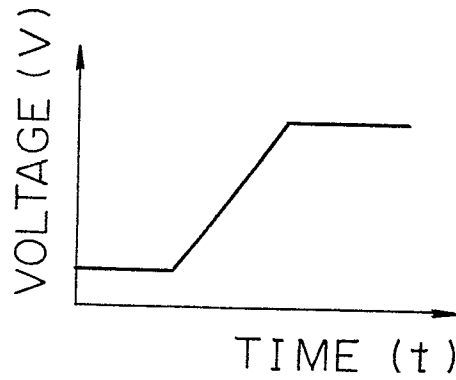
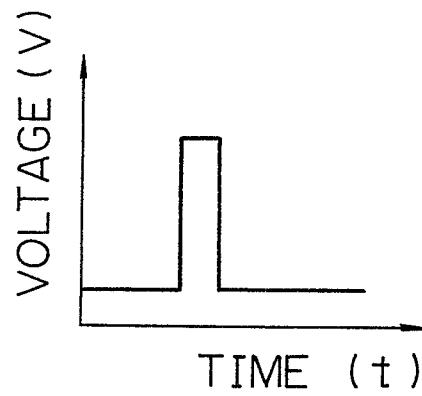
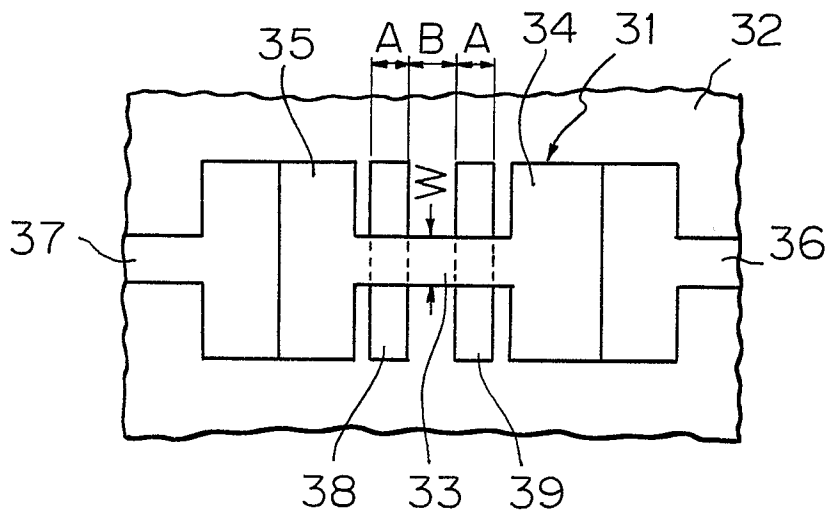


Fig. 4



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Fig. 5*Fig. 6*

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Fig. 7



Fig. 8



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Fig. 9



Fig. 10





DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl. ³)
A	GB-A-1 453 858 (R. BOSCH GMBH) * Page 1, line 72 - page 2, line 5 *	1	H 01 L 21/90 H 01 L 21/326
A, D	<p style="text-align: center;">---</p> IEEE TRANSACTIONS ON ELECTRON DEVICES, vol. ED-29, no. 4, April 1982, New York D.W. GREVE "Programming mechanism of polysilicon resistor fuses", pages 719-724 * Section II; figure 3 * <p style="text-align: center;">-----</p>	4, 5, 7	
			TECHNICAL FIELDS SEARCHED (Int. Cl. ³)
			G 11 C 17/00 H 01 L 21/326 H 01 L 21/90 H 01 L 23/52 H 01 L 27/10
The present search report has been drawn up for all claims			
Place of search BERLIN		Date of completion of the search 15-02-1984	Examiner GIBBS C.S.
CATEGORY OF CITED DOCUMENTS X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document		T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons & : member of the same patent family, corresponding document	