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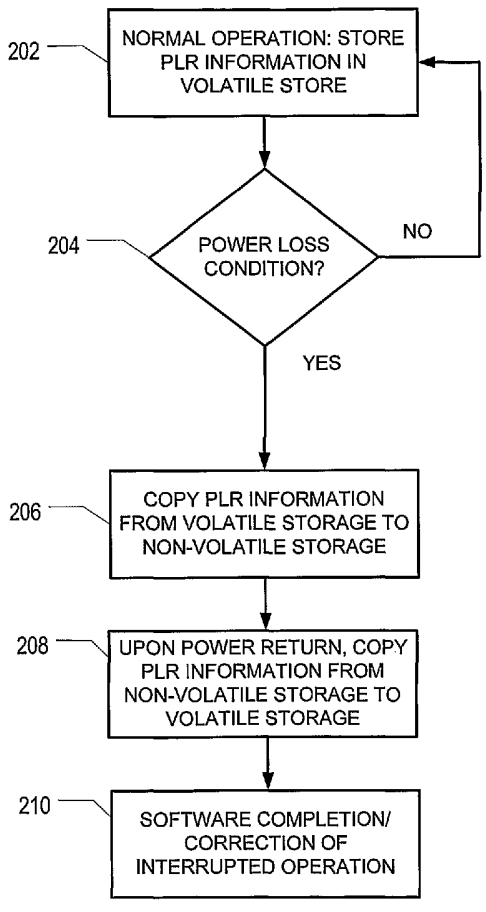
*[Continued on next page]*

(54) Title: VOLATILE STORAGE BASED POWER LOSS RECOVERY MECHANISM




(57) Abstract: According to some embodiments, power loss recovery information related to an active operation is stored in volatile memory. Upon detection of a power loss condition, the power loss recovery information is copied to non-volatile memory. Upon a return of power, the power loss recovery information is used to complete or correct the interrupted operation.

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# VOLATILE STORAGE BASED POWER LOSS RECOVERY MECHANISM

## Description of the Related Art

[0001] Non-volatile storage has the ability to retain data despite a loss of power. Due to its non-volatile nature, flash memory is an enabling technology for many portable and wireless devices, for example, cell phones, lap top computers, and personal data assistants.

[0002] An operation to non-volatile storage, for example a data write operation, may take many cycles to complete. In addition to writing data, formatting information is often updated during the operation. For example, a flash media is a system with various configurations of flash memory devices that may include hardware with additional decoding logic to manage and coordinate the various arrays of flash memory devices. Typically, a flash memory block of a flash media is divided into individual data units or sectors, with each sector having an associated header or identifying a sectors status. A sudden loss of power may occur during an active operation, for example, if a cell phone is dropped and the battery is disconnected, causing data or formatting information to be lost. Loss of formatting information can be catastrophic to flash media and result in the inability to access any data stored in the particular sector of the flash media.

[0003] Current power loss recovery mechanisms include bit twiddling, where status bits are used to track file system operations. For example, one bit may be set to indicate the start of a write operation and another may be set upon completion of a write operation. Thus, a full write operation occurs to write one bit (or cell). Upon power recovery, software scans these bits to determine if a write operation was interrupted so that any errors can be dealt with and/or corrected. The bit operations are expensive in terms of

performance and in code complexity. A more efficient power loss recovery solution is sought.

## BRIEF DESCRIPTION OF THE DRAWINGS

[0004] The present invention may be better understood, and its numerous features and advantages made apparent to those skilled in the art by referencing the accompanying drawings.

[0005] FIG. 1 illustrates a portion of a computing system according to an embodiment of the present invention.

[0006] FIG. 2 illustrates a power loss recovery flow diagram according to an embodiment of the present invention.

[0007] The use of the same reference symbols in different drawings indicates similar or identical items.

## DESCRIPTION OF THE EMBODIMENT(S)

[0008] In the following description, numerous specific details are set forth. However, it is understood that embodiments of the invention may be practiced without these specific details. In other instances, well-known methods, structures and techniques have not been shown in detail in order not to obscure an understanding of this description.

[0009] References to "one embodiment," "an embodiment," "example embodiment," "various embodiments," etc., indicate that the embodiment(s) of the invention so described may include a particular feature, structure, or characteristic, but not every embodiment necessarily includes the particular feature, structure, or characteristic. Further, repeated

use of the phrase "in one embodiment" does not necessarily refer to the same embodiment, although it may.

**[0010]** As used herein, unless otherwise specified the use of the ordinal adjectives "first," "second," "third," etc., to describe a common object, merely indicate that different instances of like objects are being referred to, and are not intended to imply that the objects so described must be in a given sequence, either temporally, spatially, in ranking, or in any other manner.

**[0011]** Unless specifically stated otherwise, as apparent from the following discussions, it is appreciated that throughout the specification discussions utilizing terms such as "processing," "computing," "calculating," or the like, refer to the action and/or processes of a computer or computing system, or similar electronic computing device, that manipulate and/or transform data represented as physical, such as electronic, quantities into other data similarly represented as physical quantities.

**[0012]** In a similar manner, the term "processor" may refer to any device or portion of a device that processes electronic data from registers and/or memory to transform that electronic data into other electronic data that may be stored in registers and/or memory. A "computing platform" may comprise one or more processors.

**[0013]** FIG. 1 illustrates a portion of a computing system 100 according to an embodiment of the present invention. Processor 102 may issue commands and data to memory system 104 over bus 106. Memory system 104 includes a memory controller 108 and one or more blocks 110(1)-(N) of non-volatile memory. Memory controller 108 may receive the commands, store the address indicators, configure the control signals, and perform an operation on selected ones of blocks 110(1)-(N).

[0014] Memory system 104 further includes volatile memory 122, power loss recovery controller 124, non-volatile memory 126, and charge storage 128. Volatile memory 122 may include flip-flops, random access memory (RAM) or other volatile storage that is not persistent during power loss. Blocks 110 and non-volatile memory 126 may include, for example, FLASH memory, EEPROM, EPROM, ferromagnetic digital memory, phase-change memory, Chalcogenide memory, polymer memory, and/or the like.

[0015] During an active write operation or other such operation, power loss recovery (PLR) information is stored in volatile memory 122. Upon detection of a power loss condition, power loss recovery controller 124 utilizes power stored in charge storage 128 to write the PLR information from volatile memory 122 to non-volatile memory 126. Upon return of power, power loss recovery controller 124 copies the PLR information back to volatile memory 122 from non-volatile memory 126. PLR information is used by software operating on processor 102 to track progress of active operations to selected ones of blocks 110 such that if power is lost during an active operation the operation can be completed or backed out of upon restoration of power. For example, PLR information may include one or more bits that are set to indicate an active write operation and that are cleared to indicate completion of the active write operation. Additionally or alternatively, PLR information may include address information related to the active write operation.

[0016] Charge storage 128 may include one or more capacitors. The number of bits of PLR information available is limited by the charge stored for copying these bits to non-volatile memory after loss of power. Charge storage 128 may also provide power to volatile memory 122 until the power loss recovery information has been stored in non-volatile memory 126. Additionally, upon return of power, software operating on processor 102 may check the power loss recovery information stored in volatile memory 122 and

take appropriate action to complete or correct the interrupted operation. Multiple power losses are handled by not clearing non-volatile memory 126 until after the interrupted operation is complete. Charge storage 128 may be integrated into a single piece of silicon composing memory system 104, may be inside the packaging of memory system 104 or may be an external component provided by, for example, an original equipment manufacturer (OEM).

**[0017]** Volatile memory 122 can provide fast write capability, unlimited cycling, and low energy writes. In one embodiment of the present invention, PLR information may include any type of information that is rewritten often that must be maintained upon power loss. For example, PLR information stored may include a current random number in a security application where random numbers are continuously generated and the previous number is used as a seed to generate the next random number. Other types of information may include call timer information, session keys with a host server, most recent radio settings, power loss recovery bits for data stored in another device in the system, the present value of a monotonic counter and the like.

**[0018]** In one embodiment of the present invention, PLR information may include a status bit that indicates whether the PLR information is in-use or idle. In the event that power is lost and the PLR information is in-use, the contents of the PLR information including the status bit is copied to non-volatile memory 126 where it is stored until power is restored. On power-up, if the status bit indicates the PLR information is in-use, the PLR information is copied to volatile memory 122 where software can utilize the PLR information to recover from the power loss event.

[0019] Although illustrated as separate components, it should be understood that volatile memory 122 may be part of power loss recovery controller 124. Further, power loss recovery controller 124 may be part of memory controller 108. Further, non-volatile memory 126 may be part of memory blocks 110. The invention is not limited in this context.

[0020] It should be understood that, in addition to a write operation, there are various other commands that may be issued by processor 102 to memory system 104 over bus 106, such as Block Erase, Read Data, Read Status, and the like. The detection of power loss may be performed during these other commands as well as or instead of during write operations. The invention is not limited in this context.

[0021] Computing system 100 is intended to represent any number of computing and communication systems, including, but not limited to, mainframes, minicomputers, servers, workstations, personal computers, notepads, personal digital assistants, cell phones, various wireless communication devices that may include one or more antenna(e) 112 and embedded systems, just to name a few.

[0022] FIG. 2 illustrates a power loss recovery flow diagram according to an embodiment of the present invention. During normal system operation, power loss recovery information related to a current operation, for example, a write operation, is stored in volatile storage, block 202. A power loss condition is monitored for, block 204. If a power loss condition is not detected, normal operation continues, block 202. Upon the detection of a power loss condition, the power loss recovery information is copied from volatile storage to non-volatile storage using a stored energy source, block 206. Upon return of power, the power loss recovery information is copied from non-volatile storage

to volatile storage, block 208. Software determines if an active operation was interrupted and if so, takes actions to complete or correct the operation, block 210.

[0023] In an alternate embodiment of the present invention, upon power loss, the power loss recovery information stored in volatile storage is first checked to determine if an active operation was interrupted. If so, the power loss recovery information is copied to non-volatile storage. If not, no action occurs. The invention is not limited in this context.

[0024] In another alternate embodiment of the present invention, upon power recovery, a determination is made if an active operation was interrupted. If so, the power loss recovery information is copied to volatile storage. If not, no action occurs. The invention is not limited in this context.

[0025] In another alternate embodiment of the present invention, upon power recovery, software reads PLR information directly from the non-volatile memory, eliminating the need to copy the information back to the volatile memory. Software may clear the non-volatile memory after taking action to complete or correct the operation. The invention is not limited in this context.

[0026] The operations referred to herein may be modules or portions of modules (e.g., software, firmware, or hardware modules). For example, the software modules discussed herein may include script, batch or other executable files, or combinations and/or portions of such files. The software modules may include a computer program or subroutines thereof encoded on computer-readable media.

[0027] Additionally, those skilled in the art will recognize that the boundaries between modules are merely illustrative and alternative embodiments may merge modules or

impose an alternative decomposition of functionality of modules. For example, the modules discussed herein may be decomposed into sub-modules to be executed as multiple computer processes. Moreover, alternative embodiments may combine multiple instances of a particular module or sub-module. Furthermore, those skilled in the art will recognize that the operations described in various embodiments are for illustration only. Operations may be combined or the functionality of the operations may be distributed in additional operations in accordance with the invention.

**[0028]** Realizations in accordance with the present invention have been described in the context of particular embodiments. These embodiments are meant to be illustrative and not limiting. Many variations, modifications, additions, and improvements are possible. Accordingly, plural instances may be provided for components described herein as a single instance. Boundaries between various components, operations and data stores are somewhat arbitrary, and particular operations are illustrated in the context of specific illustrative configurations. Other allocations of functionality are envisioned and may fall within the scope of claims that follow. Finally, structures and functionality presented as discrete components in the various configurations may be implemented as a combined structure or component. These and other variations, modifications, additions, and improvements may fall within the scope of the invention as defined in the claims that follow.

**WHAT IS CLAIMED IS:**

1. A method comprising:

storing power loss recovery information related to an active operation in non-volatile storage in response to detection of a power loss condition.

2. The method as recited in Claim 1, further comprising:

storing the power loss recovery information in volatile storage during the active operation.

3. The method as recited in Claim 2, wherein the storing the power loss recovery information in the non-volatile storage comprises copying the power loss recovery information from the volatile storage.

4. The method as recited in Claim 1, further comprising:

copying the power loss recovery information to volatile storage from the non-volatile storage upon power recovery.

5. The method as recited in Claim 1, further comprising:

storing a charge prior to the power loss condition to provide power for the copying the power loss recovery information to non-volatile storage.

6. The method as recited in Claim 1, wherein the active operation comprises a block write operation to a large non-volatile memory array.

7. The method as recited in Claim 1, wherein the power loss recovery information includes a status bit indicating the active operation has not completed.

8. The method as recited in Claim 1, wherein the power loss recovery information includes one or more address bits of the active operation.

9. The method as recited in Claim 1, wherein the power loss recovery information includes a status bit indicating a completion status of the active operation.

10. The method as recited in Claim 1, wherein the power loss recovery information includes a current random number generated by a security application.

11. The method as recited in Claim 1, wherein the power loss recovery information includes information that is updated frequently during normal operation and that must be retained upon the detection of the power loss condition.

12. The method as recited in Claim 1, wherein the non-volatile memory includes a flash memory array.

13. The method as recited in Claim 1, wherein the non-volatile memory includes a polymer memory array.

14. The method as recited in Claim 1, wherein the non-volatile memory includes a phase change memory array.

15. The method as recited in Claim 1, further comprising utilizing the power loss recovery information to complete the active operation upon a return of power.

16. The method as recited in Claim 15, wherein the power loss recovery information is read directly from the non-volatile memory.

17. The method as recited in Claim 15, further comprising copying the power loss recovery information to volatile storage from the non-volatile storage upon power recovery prior to the utilizing the power loss recovery information.

18. The method as recited in Claim 1, wherein the active operation is a format information write operation.

19. An apparatus comprising:

volatile storage to store power loss recovery information related to an active operation;

non-volatile storage; and

a controller to copy the power loss recovery information from the volatile storage to the non-volatile storage upon detection of a power loss condition.

20. The apparatus as recited in Claim 19, further comprising:

a charge storage to store a charge prior to the detection of the power loss condition, the charge to power the controller during the power loss condition.

21. The apparatus as recited in Claim 19, the controller further to copy the power loss recovery information to the volatile storage from the non-volatile storage upon power recovery.

22. The apparatus as recited in Claim 19, wherein the active operation comprises a block write operation to a large non-volatile memory array.

23. The apparatus as recited in Claim 19, wherein the power loss recovery information includes a status bit indicating the active operation has not completed.

24. The apparatus as recited in Claim 19, wherein the power loss recovery information includes one or more address bits of the active operation.

25. The apparatus as recited in Claim 19, wherein the power loss recovery information includes a status bit indicating a completion status of the active operation.

26. The apparatus as recited in Claim 19, wherein the power loss recovery information includes a current random number generated by a security application.

27. The apparatus as recited in Claim 19, wherein the power loss recovery information includes information that is updated frequently during normal operation and that must be retained upon the detection of the power loss condition..

28. The apparatus as recited in Claim 19, wherein the non-volatile memory includes a flash memory array.

29. The apparatus as recited in Claim 19, wherein the non-volatile memory includes a polymer memory array.

30. The apparatus as recited in Claim 19, wherein the power loss recovery information is used to complete the active operation upon a return of power.

31. The apparatus as recited in Claim 29, wherein the power loss recovery information used to complete the active operation is read directly from the non-volatile memory.

32. The apparatus as recited in Claim 19, wherein the active operation is a format information write operation.

33. A system comprising:

a processor; and

a memory device coupled to the processor, the memory device comprising:

volatile storage to store power loss recovery information related to an active operation;

non-volatile storage; and

a controller to copy the power loss recovery information from the volatile storage to the non-volatile storage upon detection of a power loss condition.

34. The system as recited in Claim 33, the memory device further comprising:

a charge storage to store a charge prior to the detection of the power loss condition, the charge to power the controller during the power loss condition.

35. The system as recited in Claim 33, the controller further to copy the power loss recovery information to the volatile storage from the non-volatile storage upon power recovery.

36. The system as recited in Claim 33, wherein the active operation comprises a block write operation to a large non-volatile memory array.

37. The system as recited in Claim 33, wherein the power loss recovery information includes a status bit indicating the active operation has not completed.

38. The system as recited in Claim 33, wherein the power loss recovery information includes one or more address bits of the active operation.

39. The system as recited in Claim 33, wherein the power loss recovery information includes a status bit indicating a completion status of the active operation.

40. The system as recited in Claim 33, wherein the power loss recovery information includes a current random number generated by a security application.

41. The system as recited in Claim 33, wherein the non-volatile memory includes a flash memory array.

42. The system as recited in Claim 33, wherein the non-volatile memory includes a polymer memory array.

43. The system as recited in Claim 33, wherein the power loss recovery information is used to complete the active operation upon a return of power.

44. The system as recited in Claim 33, wherein the active operation is a format information write operation.

45. The system as recited in Claim 33, further comprising an antenna coupled to the processor.

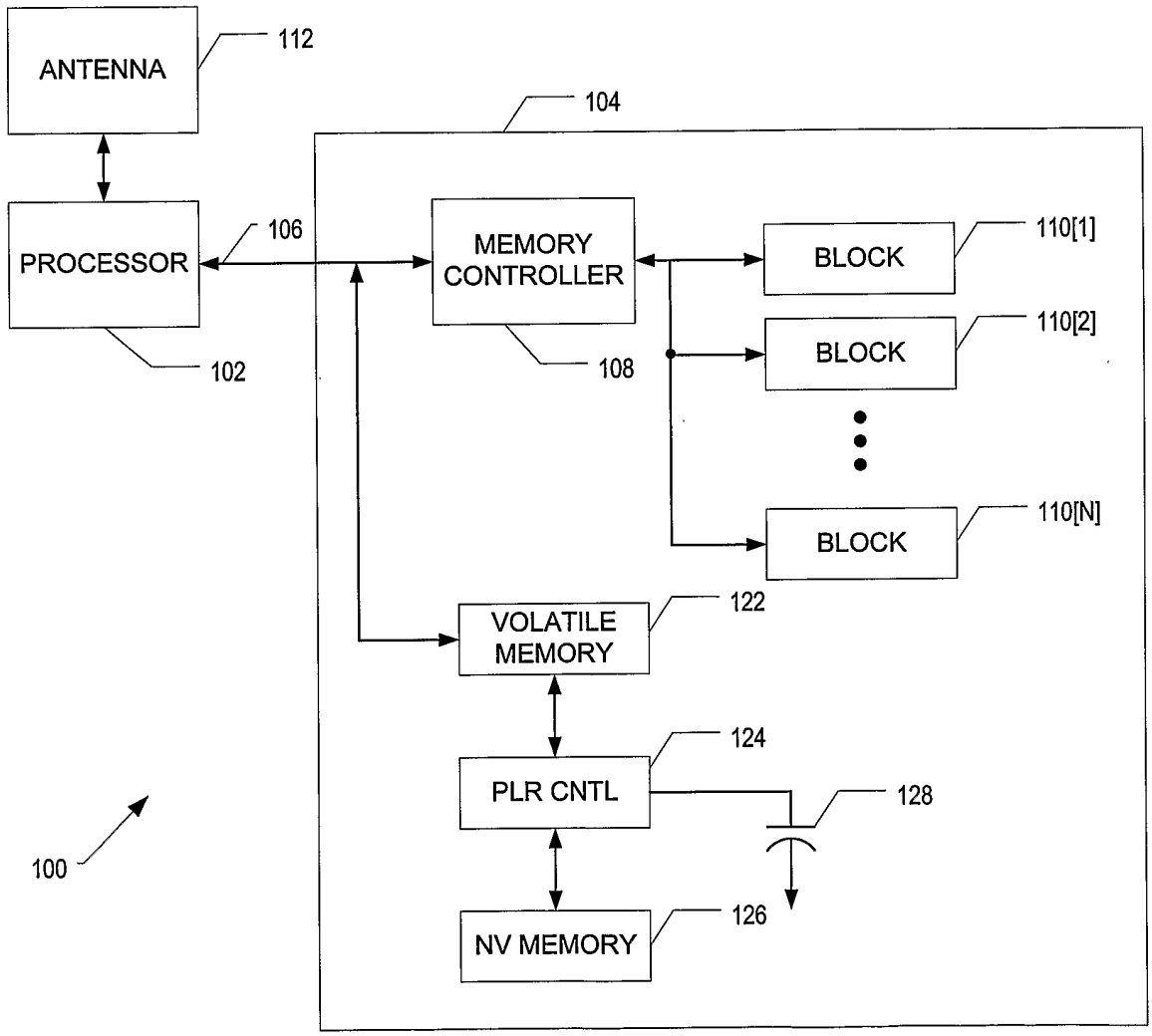
ANTENNA
112
104
PROCESSOR
106
MEMORY CONTROLLER
BLOCK
110[1]
BLOCK
110[2]
BLOCK
110[N]
102
108
VOLATILE MEMORY
122
PLR CNTL
124
128
NV MEMORY
126
100

*FIG. 1*

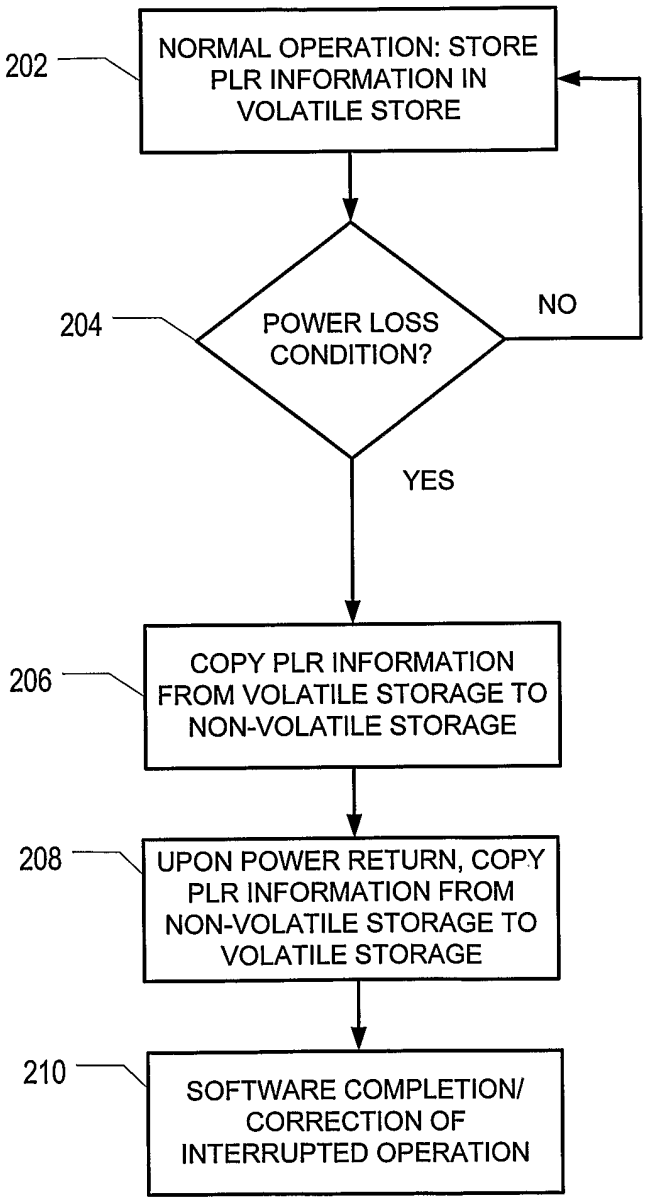
202
NORMAL OPERATION: STORE PLR INFORMATION IN VOLATILE STORE
204
POWER LOSS CONDITION?
NO
YES
206
COPY PLR INFORMATION FROM VOLATILE STORAGE TO NON-VOLATILE STORAGE
208
UPON POWER RETURN, COPY PLR INFORMATION FROM NON-VOLATILE STORAGE TO VOLATILE STORAGE
210
SOFTWARE COMPLETION/ CORRECTION OF INTERRUPTED OPERATION

*FIG. 2*

# INTERNATIONAL SEARCH REPORT

International application No
PCT/US2005/028916

A. CLASSIFICATION OF SUBJECT MATTER
G06F11/14 G11C16/00

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
G06F G11C

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, WPI Data, IBM-TDB, INSPEC, COMPENDEX

C. DOCUMENTS CONSIDERED TO BE RELEVANT

| Category* | Citation of document, with indication, where appropriate, of the relevant passages | Relevant to claim No. |
|---|---|---|
| X | EP 0 953 984 A (STMICROELECTRONICS S.R.L)<br>3 November 1999 (1999-11-03)<br>paragraphs '0001!, '0006! - '0014!,<br>'0017!, '0019! - '0031!, '0041! | 1-45 |
| X | US 6 295 577 B1 (ANDERSON DAVID B ET AL)<br>25 September 2001 (2001-09-25)<br>claims 7-9 | 1-4,6,8,<br>11-19,<br>21,22,<br>24,<br>27-33,<br>35,36,<br>38,41-45 |
| A | US 6 170 066 B1 (SEE DEBORAH)<br>2 January 2001 (2001-01-02)<br>column 2, lines 25-51 | 18,32,44 |

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

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| Date of the actual completion of the international search | Date of mailing of the international search report |
|---|---|
| 1 February 2006 | 08/02/2006 |
| Name and mailing address of the ISA/<br>European Patent Office, P.B. 5818 Patentlaan 2<br>NL – 2280 HV Rijswijk<br>Tel. (+31-70) 340-2040, Tx. 31 651 epo nl,<br>Fax: (+31-70) 340-3016 | Authorized officer<br>Lanchès, P |

# INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/US2005/028916

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| US 6170066 B1 | 02-01-2001 | NONE | |