

Aug. 1, 1967

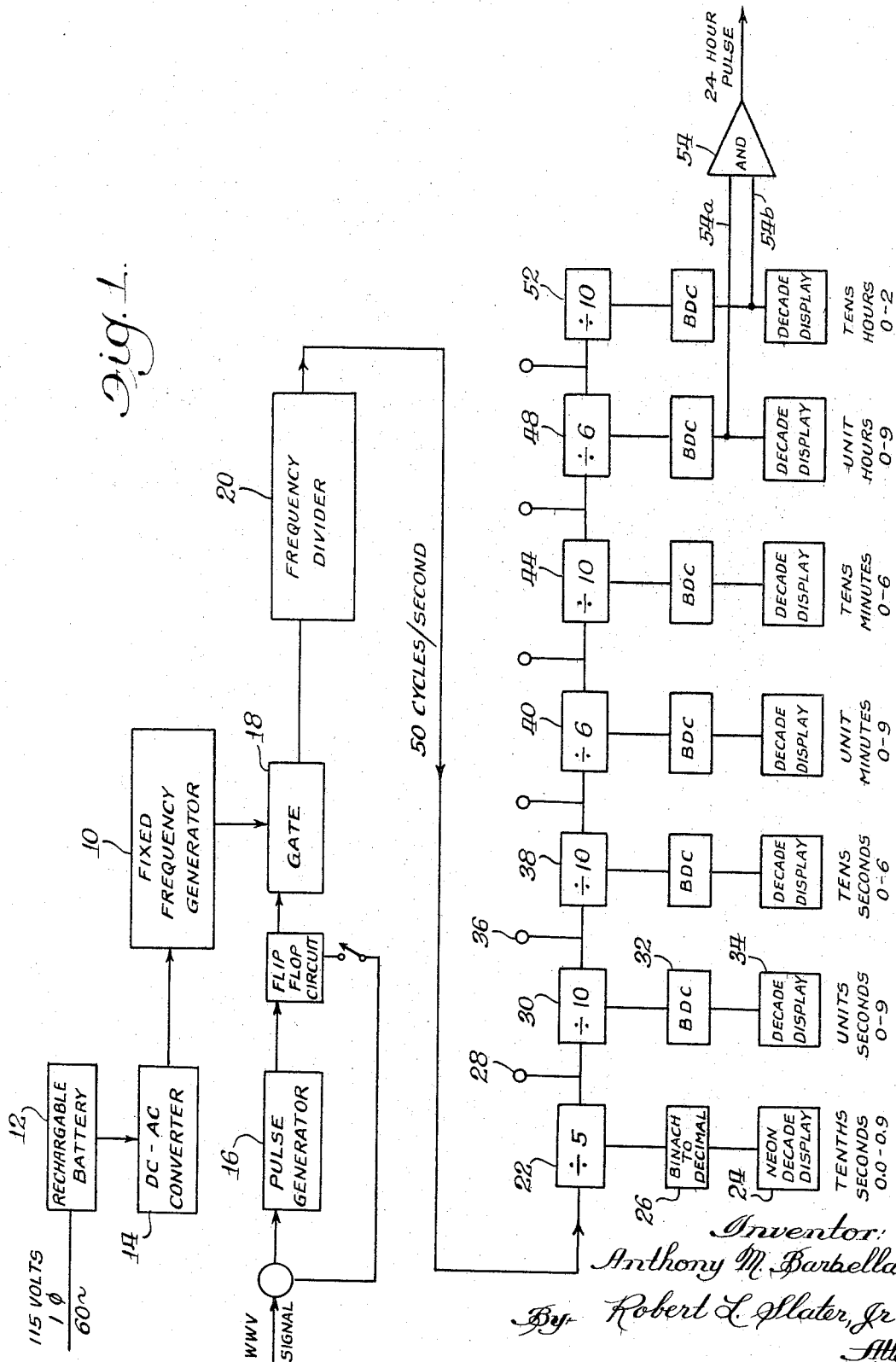
A. M. BARBELLA

3,333,410

ELECTRONIC CLOCK-CALENDAR

Filed April 2, 1965

4 Sheets-Sheet 1



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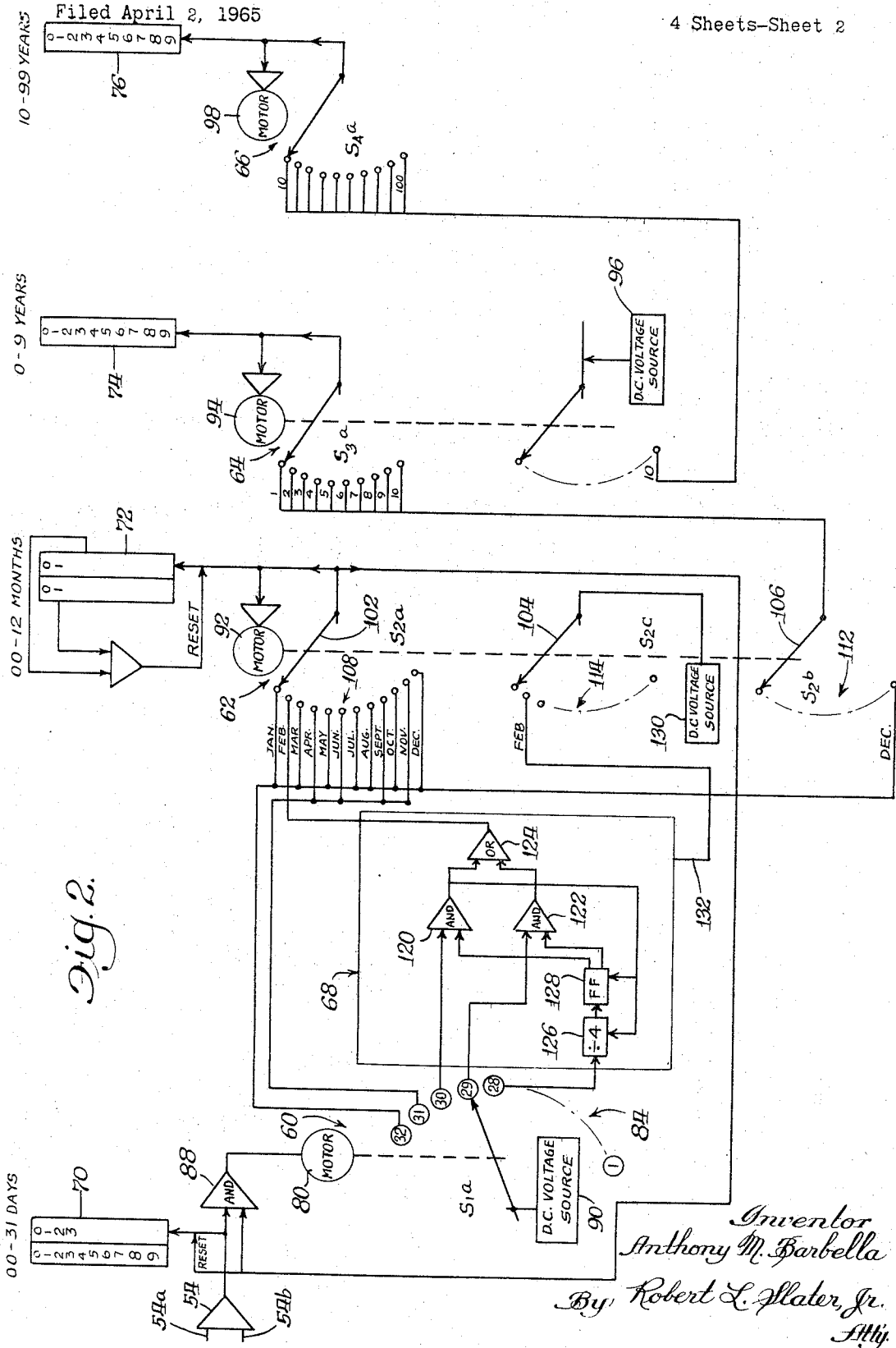
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4 Sheets-Sheet 2



Inventor
Anthony M. Barbella
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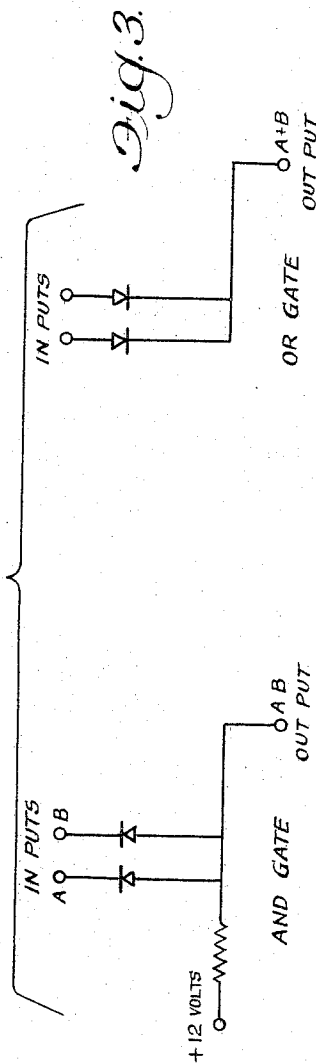
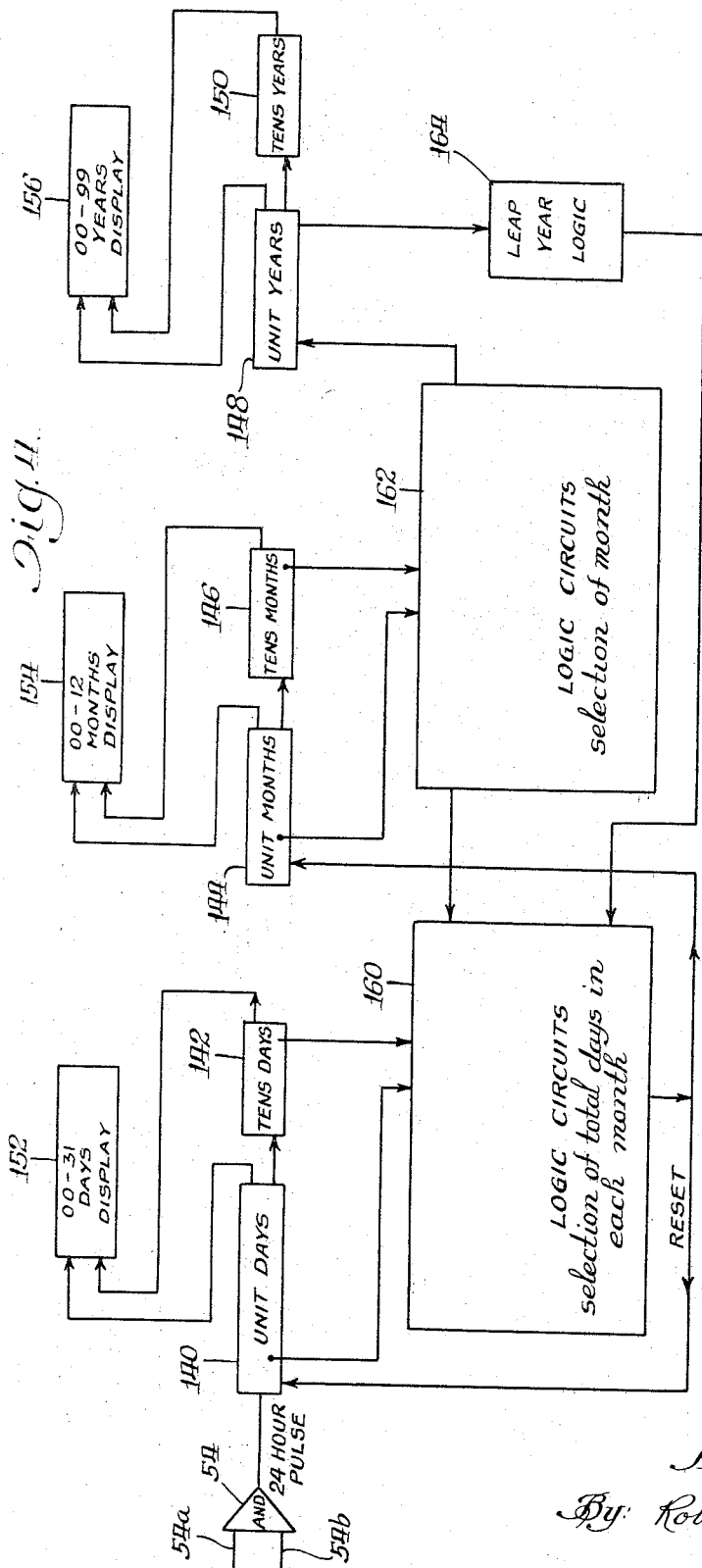
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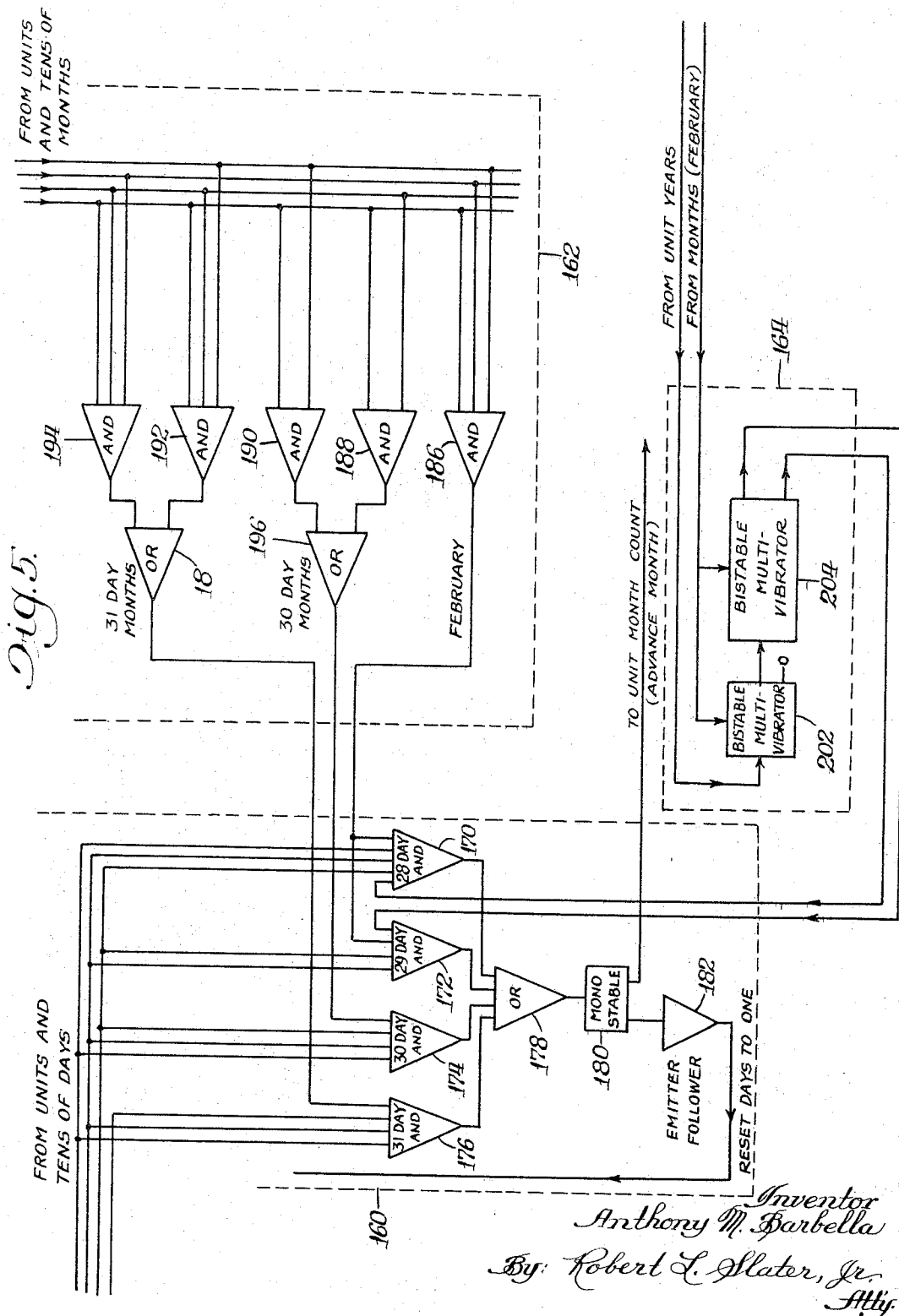
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ELECTRONIC CLOCK-CALENDAR

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Filed Apr. 2, 1965, Ser. No. 445,176

3 Claims. (Cl. 58—4)

This invention relates to a time indicating device; more particularly, it relates to an automatic combination clock and calendar.

The units of time in general use today are derived from pre-history social custom. The dimensions of our units of time are based upon observable natural astronomical cycles. For instance, the day, hour, minute, and second are derived from the period of rotation of the Earth upon its axis, the month from the revolution of the Moon on its orbit about the Earth, and the year from the revolution of the Earth in its orbit about the Sun. Unfortunately, for those constructing time keeping and time indicating devices, none of these natural cycles used as fundamental time units is divisible one into another by integral number values.

Heretofore, time units derived from the daily rotation of the Earth about its axis have reached a high state of perfection in mechanical, electro-mechanical and, more recently, electronic clocks. Because of the inconvenient relationships of the longer units of time, namely, the day, the month, the months of the year, and consequently, the seasons and the year, little or no attention has been given to developing automatic clock and perpetual calendar combination devices. Mechanical calendars have been disclosed by earlier inventors, but these earlier efforts all depend upon human discretion at critical points of time to adjust the mechanical calendar device to keep it in step with real time.

In commercial practice where clerical help is present, and in the circumstances in which most people live and work, it has been the practice to consult a clock to determine the hour of the day and a calendar to determine the day of the month and the year. With the factor of human discretion present, considerable amount of confusion regularly results from human error in applying date and time marks to records, commercial papers, receipt stamps, etc. Even when clock-driven time markers are used to stamp records, the date is regularly adjusted each day by the worker using the stamp after he has consulted a calendar.

With increasing automation in business records, production and monitoring of instrumentation, there is need for reliable, entirely unambiguous, automated devices for marking and displaying the time of day and the date. As commercial practice becomes increasingly automated, the risks of improper abuse of records by machine attendants is increased and reliability of unambiguous time markings on records derived from automated production and data handling equipment becomes an important audit tool.

Moreover, there are minor disturbances in the period of the natural cycles upon which our time units are based such that certain scientific procedures are best accomplished with time keeping and time unit display or indicating devices independent of natural cycles.

For instance, many scientific experiments are conducted with instruments positioned at inaccessible locations remote from the experimenter. Such instruments develop records that depend for their usefulness upon the accuracy with which time is measured in both very small fractions of a second as well as in periods of time longer than a year. Such instrumentation requires time keeping and time indicating devices which are completely self-contained and unambiguous for extended periods of time measurable in months and years. Remote instrumentation

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equipment which requires high accuracy and unambiguous time markings is best controlled by time keeping devices which depend upon a single fundamental unit of time such as oscillation of a fixed frequency crystal or other readily reproducible natural phenomena other than the natural cycles upon which the conventional units of time are based.

There is, therefore, a need for an automated combination clock and perpetual calendar for use in various applications in commerce, regulation of automated production devices, automated data handling equipment, and for use in long duration scientific experiments.

One object of this invention is to provide a novel combination clock and perpetual calendar.

Another object of this invention is to provide a fully automated perpetual calendar.

Still another object of this invention is to provide a means for actuating a perpetual calendar utilizing a signal derived from a clock.

Another object of this invention is to provide a calendar adapted to function without adjustment or correction through the course of tens of years.

These and other objects and advantages will be apparent from the following drawings, specification, and claims.

FIGURES 1 and 2 considered together illustrate a preferred embodiment of my novel combination automatic clock and perpetual calendar.

FIGURE 3 illustrates circuit diagrams of logic components utilized in preferred embodiments of my invention.

FIGURE 4 is a schematic block diagram showing a second preferred embodiment of my invention.

FIGURE 5 is a detailed diagram of a portion of the embodiment of my invention shown in FIGURE 4.

Our present-day calendar is based on the length of the solar year, the lunar cycle having been eliminated as a unit of time measure. However, we have retained from the ancient lunar cycle calendars the concept of the months of the year. The variable length in the months has been handed down from earlier calendars that adjusted the length of months to arbitrarily fit the lunar cycles to the solar year. The leap year adjustment, which in our calendar requires that the month of February be lengthened to twenty-nine days for 97 years out of each 400 years, adjusts our calendar for the fact that the solar year contains 365 days, 5 hours, 48 minutes and 46 seconds rather than an integral whole number of solar days. Under the rules of our present calendar, the average calendar year is only twenty-six seconds longer than the solar year and will be correct within an error of less than one day throughout the next 3300 years. It is also significant here to note that under present calendar rules the next leap year day to be omitted from our calendar falls in the year 2100 A.D.

The present invention is referred to here as comprising a perpetual calendar. It is understood that the cumulative positive error of 26 seconds per year in our calendar rules is not eliminated in the present invention; and that the one day adjustment in the year 2100 A.D. is not programmed into the present invention. Except for these above noted exclusions, however, my clock-calendar invention is programmed for perpetual use. The embodiment of my invention illustrated in FIGURES 1 and 2 is comprised of two separate but cooperating parts, the first being a clock and the second being a perpetual calendar driven by a pulse signal derived from the clock.

The clock as shown in the illustrations is comprised of a fixed frequency generator 10. Numerous kinds of fixed frequency generators are described in detail in the literature which could serve for a frequency standard in my invention. A commonly used stable frequency generator employs a crystal controlled oscillator powered by an

alternating or direct current source. In the embodiment of my invention shown, a rechargeable battery 12 powers a DC to AC converter 14 which in turn supplies power to a precision crystal controlled oscillator mounted within the fixed frequency synthesizer 10. If the precision crystal controlled oscillator requires a DC source, the DC to AC converter 14 may be eliminated. I have found one megacycle a convenient frequency reference to use in my invention; however, any frequency between 1 mc. and 50 sc. will readily serve the purpose. The accuracy of the clock is directly related to the precision of the frequency generator output. A higher frequency standard permits greater tolerance in the pulse repetition rate of the frequency standard without lessening the precision of the clock output signals. Moreover, the higher frequency standard permits greater accuracy in synchronizing the fixed frequency generator signal with a standard such as the WWV broadcast time standard.

To facilitate calibration of the frequency standard used in the illustrated embodiment of my invention, a pulse generator 16 responsive to standard signals is connected to actuate a signal gate 18 which connects the output signal of the fixed frequency standard 10 to a frequency divider 20. Calibration is indicated in the illustration as being a WWV signal; however, other time standard sources would serve equally well.

The frequency divider 20 is adapted to provide a positive 6 to 12 volt output signal pulse with a precision pulse repetition rate of fifty cycles per second. Frequency divider circuits described in the literature have been designed using various circuit principles. One commonly used frequency divider arrangement suitable for small divisor frequency divisions employs a series of bistable circuits or flip flops in a cascaded arrangement, each bistable stage providing one output pulse for each two input pulses. In order to divide higher frequencies by larger divisors, numerous circuit arrangements described in the literature, but not in detail here, have been disclosed to provide large divisor frequency division with great economy of component steps in the process.

The illustrated embodiment of the clock portion of my invention is provided with time unit display means which range from $\frac{1}{10}$ second to one day. The display means which I have illustrated are neon lamp indicators arranged in decades with automatic reset circuits. It is clear that other time unit display methods may be substituted for the neon lamp decades and will serve equally well. For instance, incandescent lamps, rotating hands on dials, or solenoid operated vanes appropriately marked may be triggered by the respective time interval pulse signals to rotate into view for the proper time interval.

The 50 cycle per second pulse repetition rate signal at the output of the frequency divider 20 is passed through a small frequency divider 22 which reduces the pulse repetition rate to ten per second. The ten pulse per second signal is passed to the tenth second display decade 24, through a conventional binary to decimal converter circuit 26, to the next succeeding pulse signal frequency divider 30, and to a ten pulse per second output terminal 28.

As shown in FIGURE 1, the frequency divider 30 passes a one pulse per second signal through a binary to decimal converter circuit 32 and from there to a unit seconds decade display 34. The one pulse per second signal is also passed to the one second pulse output terminal 36 and to the next succeeding frequency divider 38 which emits one pulse per ten seconds. Successive stages of time units comprising a frequency divider, binary to decimal conversion circuit and a decade display are provided for unit minutes at 40, tens of minutes at 44, unit hours at 48, and tens of hours at 52.

An AND gate 54 is connected to the unit hours and the tens of hours stages as indicated below to provide an output pulse once each twenty-four hours. The AND gate 54 may be connected so that the two input leads 54a and 54b simultaneously receive input pulses respectively

from the hour connections to the display decades for the unit hours and tens of hours stages.

The output of the twenty-four hour pulse AND gate 54 is shown in FIGURES 1 and 2 as being fed to the input terminal of a preferred electromechanical embodiment of the calendar portion of my invention. As shown in the illustration, the electromechanical perpetual calendar portion of my invention is comprised of a combination of four motor driven stepping switches 60, 62, 64 and 66, a logic circuit 68 for leap year adjustment, and neon decade display means 70, 72, 74 and 76 for displaying, respectively, number of days in the month, the month, unit years, and tens of years.

The calendar unit is actuated by a pulse signal derived from the twenty-four hour pulse AND gate 54 which, when connected to the clock as shown in FIGURE 1, generates one output pulse at the termination of each twenty-four hour period. The twenty-four hour pulse is amplified by the pulse amplifier 88.

The twenty-four hour pulse signal via the pulse amplifier 88 actuates the motor 80 of stepping switch 60 advancing the movable electrode 82, each pulse advancing the movable electrode one position. Stepping switch 60 is comprised of one movable electrode which progressively contacts thirty-two stationary electrodes, shown at 84. Each of the stationary electrodes is numbered from one to thirty two, the first thirty-one contacts being the analog from a switching logic viewpoint of one day. The electrode numbered thirty two is a special switching electrode that actuates the month indicator stepping switch 62 following the thirty-first day of those months having 31 days; that is, the months of January, March, May, July, August, October and December.

The twenty-four hour pulse signal originates in the AND circuit 54 and is fed into a pulse amplifier 88, which may be a complementary emitter-follower that provides a momentary high current source for powering the motor 80. The twenty-four hour pulse is also fed into the neon decimal display 70 adapted to indicate the day of the month.

The movable electrode 82 of stepping switch 60 connects to a DC voltage source 90. The voltage when appropriately connected through contacts in stepping switches 60, 62 and 64 furnishes the power to actuate the motors 92 and 94 of switches 62 and 64 respectively. A second DC voltage source 96 connects through selected contacts described below of stepping switch 64 and powers the motor 98 of stepping switch 66.

Stepping switch 60 is comprised of one bank of thirty-two stationary contacts 84 and one movable electrode 82. The movable electrode 82 passes successively into contact with each of the first thirty-one contacts for those aforesaid months having thirty-one days. The motor 80 of stepping switch 60 is, during thirty day months, namely April, June, September and November, programmed to return or "reset" the movable electrode 82 in position to contact the first stationary electrode contact 84 upon the arrival of the thirty-first twenty-four hour pulse during any of the aforesaid thirty day months.

The month of February is, in non-leap years, twenty-eight days long. The twenty-ninth contact in the stationary electrode bank 84 is connected to reset the movable electrode 82 back to the first "day" contact on the arrival of the twenty-ninth twenty-four hour pulse during three of each four "February" switch configurations.

Stepping switch 62 is comprised of two parallel ganged switches having, respectively, movable electrodes 102 and 106 and two banks of twelve stationary electrodes 108 and 112. For clarity and brevity, the switch banks of switch 62 will be referred to as S_{2a} and S_{2b} , respectively.

The twelve stationary contacts of S_{2a} are analogs, in the logic switching sense, of the twelve months of the year. Switch bank S_{2b} is a one active contact switch which connects the thirty-second twenty-four hour pulse signal

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in the month of December to stepping switch 64 that in turn actuates the unit years switching and display means.

The thirty-second twenty-four hour pulse in December through S_{2a} pulses the stepping switch 62, motor 92, the month of the year display 72, and the reset connections in the day of the month display 70 and stepping switch 60 and motor 80.

The leap year adjustment requires that the February month during three of each four years be twenty-eight days long and in the fourth year twenty-nine days long. The logic circuit indicated at 68 and described below provides the necessary pulse switch logic.

A first AND gate 120, having two input terminals and one output terminal, and a second AND gate 122, also having two input terminals and one output terminal, are connected in a parallel cascaded arrangement to an OR gate 124. The OR gate 124 has two input terminals to which the outputs of the AND gates 120 and 122 are connected. The output of the OR gate 124 is connected to the "February" stationary electrode 108 of switch bank S_{2a} of stepping switch 62. The OR gate 124 output signal as actuated by the logic circuit 68 provides the proper number of days count for February in the month stepping switch 62.

A pulse frequency divider circuit 126 is provided in the logic circuit 68 with two input and one output terminals. The divider circuit is constructed to provide one output pulse for each four input pulses. A multistable vibrator or "flip flop" circuit 128 is provided with two input terminals and two output terminals. The output terminal of the pulse frequency divider 126 is connected to one input terminal of the flip flop circuit 128. One each of the output terminals of the flip flop circuit 128 is connected respectively to an input terminal in the AND circuits 120 and 128.

The stationary electrodes 84 of stepping switch 60 corresponding to the 28th, 29th and 30th days are connected respectively, as may be more readily seen in the illustrations, to an input terminal of the pulse frequency divider 126, an input terminal of the second AND gate 122, and an input terminal of the first AND gate 120. Finally, the output of AND gate 120 connecting to the OR gate 124 also is connected to one input terminal of the pulse frequency divider 126 and the flip flop circuit 128.

Operation of the leap year logic circuit 68 is best described by following the switching sequence from a leap year day, February 29. On midnight of a leap year day, the movable electrode 82 of stepping switch 60 will move to contact the fixed electrode 84 corresponding to the 30th day. That would place a plus one signal at one input to the AND gate 120. The previous condition of the flip flop circuit 128 would have been such that a plus one pulse would be present at the second input terminal of the first AND gate 120. The AND gate 120 then emits a plus one pulse which first activates the OR gate 124 causing a pulse to energize switch bank S_{2a} , rotating the movable electrode 102 of switch 62 to the "March" position. The second consequence of the AND gate 120 pulse is to provide a pulse at the input of the pulse frequency divider 126 and at the input of the flip flop circuit 128. The next three "February" months following leap year are twenty-eight day months that require activation of the OR gate 124 and consequent switching of the stepping switch 62 to the "March" position upon the arrival of the 29th day pulse. At midnight of the 28th day of February, the required next three pulses to actuate the OR gate 124 are derived from the second AND gate 122 which is connected at one input to the 29th day of the fixed electrode bank 84, the second input terminal of the AND gate 122 having been previously supplied by the flip flop circuit 128 output.

Upon the next occurrence of leap year, the pulse frequency divider circuit 126 will on the 28th day of February emit an output pulse which switches the flip flop circuit 128 to the output thereof connected to the input of

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AND circuit 120, initiating the above-described leap year switching sequence at midnight of the 29th day.

The leap year correction logic circuit 68 is powered and activated only during the times that stepping switch 62 is in the "February" position. Switch bank S_{2c} then connects a DC voltage source 130 to the power input 132 of logic circuit 68. By this arrangement, the rotation of stepping switch 60 past the 28th, 29th and 30th day positions in months other than February will not result in actuation of the circuit components described above in connection with logic circuit 68.

The operation of the "year" stepping switch 64 is achieved at the expiration of the 31st day of each December month by energizing the switch bank S_{3b} of stepping switch 62 which in turn energizes the switch motor 94 and provides the correct neon decade lamp indication in the "years" display.

Similarly the tens of years are actuated upon the last instant of the December month in the tenth year by powering the fixed electrode 140 in bank S_{3b} of switch 64, whereupon the decade years stepping switch 66 is actuated and the decade years display 76 is appropriately energized.

The logic modules, that is, the AND gates 54, 120 and 122, and the OR gate 124 may be conventional diode gates. FIGURE 3 illustrates a diode OR gate and a diode AND gate such as may be used in my invention. Descriptions of the operation of conventional OR and AND gates such as illustrated are available in numerous earlier reference works. The multistable vibrator 128 may be constructed in accordance with any of a number of standard multivibrator circuits fully described in electronic engineering literature. Similarly, the pulse frequency divider circuits are available in various well known embodiments described in earlier reference works.

A second preferred embodiment of my invention which utilizes only electronic circuit switching means, thereby eliminating all mechanical switching components, is illustrated in FIGURES 4 and 5. The total embodiment of my invention comprises the combination of an electronic clock and a perpetual calendar. The electronic clock such as illustrated in FIGURE 1 and described in connection with the first embodiment above is also combined with the present embodiment illustrated in FIGURES 4 and 5.

FIGURE 4 illustrates in functional block diagram form a perpetual calendar comprised of electronic switch logic components actuated by pulse signals. Unit days are counted in a "unit days" counting circuit 140, tens of days in a "tens of days" counting circuit 142, unit months in counting circuit 144, tens of months in counting circuit 146, unit years in counting circuit 148, and tens of years in counting circuit 150. Visual display of the status of the above day, month and year counting circuits is provided by a first through thirty-one days display 152, a January through December display 154, and a first through ninety-nine years display 156.

The electronic counting circuits 140 and 142, 144 and 146, and 148 and 150 for counting, respectively, days, months and years are conventional counting circuits comprised of flip flop circuits in appropriate well known cascaded arrangements in which reset circuits clear the counter and return the display indication to zero whereupon the counting processes are repeated.

Excepting for the presence of the logic circuits 160 for selection of the total number days of the month, 162 for selection of the month of the year and 164 for leap year correction, the electronic circuit calendar counters 140 and 142, 144 and 146, and 148 and 150 are conventional linear counting circuits connected in the cascaded arrangement shown in FIGURE 4.

In the unit and tens of days counters 140 and 142, the reset circuits must be actuated on the thirty-first twenty-four hour pulse in the months of April, June, September and November; actuated on the thirty-second twenty-four hour pulse in the months of January, March, May, July,

August, October and December; and finally the reset circuits must be actuated on the twenty-ninth or thirtieth twenty-four hour pulse in February, depending upon the year and the leap year correction.

In the unit months and tens of months counting circuits 144 and 146, the reset circuits are actuated by the logic circuit 162 in which the selection of the month is accomplished by way of signal input into logic circuit 160 which in turn passes a reset signal to the unit and tens of months counting circuits.

The leap year correction circuit 164 derives an annual pulse signal from the unit years counting circuit 148 and once each four years provides a pulse to the logic circuit 160 in order to adjust February from twenty-eight to twenty-nine days in length.

FIGURE 5 illustrates in greater detail the circuit connections within and between the logic circuits 160 for selection of the total number of days in each month, circuit 162 for selection of the month, and circuit 164 for leap year correction.

Circuit 160 for selection of the number of days in each month is comprised of four parallel AND gates 170, 172, 174 and 176 labeled in the illustration and associated, respectively, with switching at the close of the 28th, 29th, 30th and 31st day of the month. The above four AND gates each have one output terminal, all of which are connected to input terminals of an OR gate 178. Upon the emission of a pulse signal from any one of the four AND gates 170, 172, 174 and 176, the OR gate 178 may be actuated and caused to pass a pulse signal from the one output terminal thereof.

A single-shot multivibrator 180, having a single input and a single output terminal, is connected to receive the output pulse from the OR gate 178. Output of the single-shot multivibrator 180 is fed simultaneously to the unit month counting circuit 144 and to the reset of the unit days and tens of days counters 140 and 142. An emitter follower circuit 182 may be inserted in the reset line to assure proper loading of the circuits and consistent signal strength. The single-shot multivibrator 180 and emitter 182 do not enter into the logical function of the circuit.

Any one of the four AND gates 170, 172, 174 and 176 may be actuated upon simultaneous arrival of four signal pulses at the four input terminals associated with each AND gate. Moreover, each of the AND gates 170, 172, 174 and 176 receives input signals from the unit days and tens of days counting circuits 140 and 142. Such input signals are derived from the counting circuits 140 and 142 through fixed connections so that the 28th day AND gate 170 receives pulse signals at two input terminals on the expiration of the 28th day of the month; the 29th day AND gate 172 receives two input pulse signals upon the expiration of the 29th day of the month; and the 30th day AND gate 174 receives three input pulse signals and the 31st day AND gate 176 receives three input pulse signals on the expiration of the 30th and 31st day, respectively, of the month. The aforesaid day counter pulse signals can not alone actuate any of the AND circuits 170, 172, 174 and 176; additional complementary input signals, which are in each instance derived from the selection of the month circuit 162, are required to actuate these AND gates.

Selection of the months is regulated by circuit 162 which is comprised of five AND gates 186, 188, 190, 192 and 194 and two OR gates 196 and 198. The AND gates 192 and 194 and in turn OR gate 198 are connected to the month counting circuits 144 and 146 so that the OR gate 198 emits a pulse during the 1st, 3rd, 5th, 7th, 8th, 10th or 12th months, these being the thirty-one day months, January, March, May, July, August, October and December. The AND gates 188 and 190 and in turn OR gate 196 are connected to the month counters 144 and 146 so that the OR gate 196 is actuated during the 4th, 6th, 9th or 11th months, these being the thirty day months of April, June, September and November.

During the thirty-one day months the OR gate 198 is actuated and emits a pulse signal that is fed into the thirty-one day AND gate 176. During the thirty day months, OR gate 196 is actuated and furnishes the thirty day AND gate 174 with a plus one input pulse.

Finally, during the second or February month AND gate 186 is actuated and emits a pulse which is fed simultaneously to an input of the 28th day AND gate 170 and an input of the 29th day AND gate 172. Selection of the 28th or 29th day AND gate 170 or 172 during the second or February month is determined by input from the leap year logic circuit 164 which is described next below.

The leap year logic circuit 164 comprises two bistable multivibrators 202 and 204 arranged in cascade, each of which has two inputs and two output terminals. The first stage bistable 202 has one input connected to the unit years counting circuit 148 and receives one pulse signal per year. The second input terminal of both bistables 202 and 204 are connected to the unit month counting circuit 144 and receive a unit pulse during each second or February month. The first output terminal of the first stage bistable 202 is connected to the first input terminal of the second stage bistable 204. The second output terminal of the bistable 202 is not utilized. The two output terminals of the second stage bistable 204 comprise the leap year logic circuit output and are connected, respectively, to an input of the 28th day AND gate 170 and an input of the 29th day AND gate 172. The bistables 202 and 204, arranged as described, will furnish a unit pulse during the second or February month to the 28th day AND gate 170 for three successive years and on the fourth year to the 29th day AND gate 172.

With the above-described arrangement, the 28th day AND gate 170 during three second or February months will be actuated by the presence simultaneously of four input signals derived, respectively, from AND gate 186, bistable 204, and two from the unit and days counting circuits 140 and 142. On the fourth year, bistable 204 switches output terminals and the 29th day AND gate 172 will be actuated by the presence then of four simultaneous input signals derived, respectively, from the AND gate 186, bistable 204, and the unit and tens of days counting circuits 140 and 142.

AND gates requiring two, three, four or more simultaneous pulse signals to actuate are well known and described in earlier electronic engineering literature. The AND and OR gates, multivibrators, emitter follower, and flip flop circuits used in the embodiment of my invention described above are solid state diode and transistor circuits of conventional design and are not described in detail here. Both vacuum tube and solid state circuit components may be advantageously utilized in the above described embodiment of my invention.

The embodiments of my invention shown in the drawings and described above are merely illustrative of my invention, the scope of which is set forth in the following claims.

I claim:

1. In combination with an automatic clock and calendar of the type wherein there are provided: a fixed frequency oscillator; a plurality of frequency dividing circuits, each having an input terminal and an output terminal, the frequency dividing circuits being connected in series, the oscillator being connected to the input terminal of the first frequency dividing circuit in the series; a plurality of visual display means adapted to display units of time including number of days, the display means being provided with reset means for recycling the display means, the display means being selectively connected to output terminals of the frequency divider circuits; a first switch having a single input terminal on a first side and twelve output terminals on a second side, each of the twelve switch states corresponding to a month of the year; and a second switch having a single input terminal on a first side and having thirty-one output terminals on a second side,

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the second switch output terminals being connected to the number-of-days display reset means;

The improvement which comprises:

- a third switch having a single input terminal and four output terminals, the third switch being connected to advance one state each full cycle of the first switch, the third switch being connected to cycle the twenty-nine day terminal of the second switch each fourth complete cycle of the second switch and in the remaining three states to cycle the twenty-eight day terminal of the second switch;

whereby an automatic visual display clock and calendar is provided which correctly indicates the year, month, day of the month, including mid-century leap year correction, and the correct time of the day, utilizing only one pulse signal source.

2. In combination with an automatic clock and calendar of the type wherein there are provided: a fixed frequency oscillator; a cascaded multiple stage frequency dividing circuit having multiple output terminals, the oscillator being connected to the first stage of the frequency divider circuit; visual display means connected to the frequency divider output terminals, the display means having reset signal responsive means wherewith the display means is continuously recycled and visually displays the output pulses of the frequency divider circuits corresponding to units of time including number of days; a first switch having twelve states, each state corresponding to a month of the year; a second switch having a plurality of states corresponding to the number of days in the months of the year ranging from twenty-eight through thirty-one, the second switch being connected to the number-of-days display corresponding to the number of days in the indicated month, the first switch being actuated to change states in response to the reset signal in the number-of-days display means;

The improvement which comprises:

- a third switch having four states connected to the first switch, the third switch being adapted to cycle the second switch state corresponding to the twenty-ninth day each four cycles of the first switch state corresponding to the second month position;

whereby units of time coordinated with the mid-century calendar, ranging from parts of a second to years, may be precisely counted and displayed.

3. In combination with an automatic clock and calendar of the type wherein there are provided: a fixed frequency generator; a plurality of pulse frequency divider circuits connected in cascade, the frequency generator being connected to actuate the divider circuits; a plurality of counting circuits and display means connected to the divider circuit outputs wherewith periods of time ranging from fractions of a second to years may be counted and displayed;

The improvement which comprises:

- logical means for altering each fourth year which is counted and displayed by the addition of one

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day at the end of the second month, the logical means including:

- a second AND circuit having a first input terminal connected to the output terminal of the divider circuit corresponding to the twenty-ninth day, a second input terminal, and an output terminal;

- a second AND circuit having a first input terminal connected to the output terminal of the divider circuit corresponding to the thirtieth day, a second input terminal, and an output terminal;

- an OR circuit having a first input terminal connected to the output terminal of the first AND circuit, a second input terminal connected to the output terminal of the second AND circuit, and an output terminal corresponding to the second month;

- a bistable switch having a first output terminal corresponding to the first switch state and connected to the second input terminal of the first AND circuit, a second output terminal corresponding to the second switch state and connected to the second input terminal of the second AND circuit, a first input terminal connected to the output terminal of the second AND circuit, and a second input terminal; and

frequency divider means for emitting one output pulse for each four input pulses, connected between the output terminal of the divider circuit corresponding to the twenty-eighth day and the second input terminal of the bistable switch, such that the bistable switch will emit a pulse to the second input terminal of the first AND circuit upon the incidence of three consecutive pulses corresponding to the twenty-eighth day of the second month, whereupon incidence of a pulse to the first input terminal of the first AND circuit on the twenty-ninth day will cause the first AND circuit to emit a pulse to the OR circuit which accordingly will emit a pulse, and such that the bistable switch will emit a pulse to the second input terminal of the second AND circuit upon the incidence of the fourth pulse corresponding to the twenty-eighth day of the second month, whereupon incidence of a pulse to the first input terminal of the second AND circuit on the thirtieth day will cause the second AND circuit to emit a pulse to the OR circuit which accordingly will emit a pulse.

No references cited.

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