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[Continued on next page]

(54) Title: DIFFERENTIAL AMPLIFIER SYSTEM

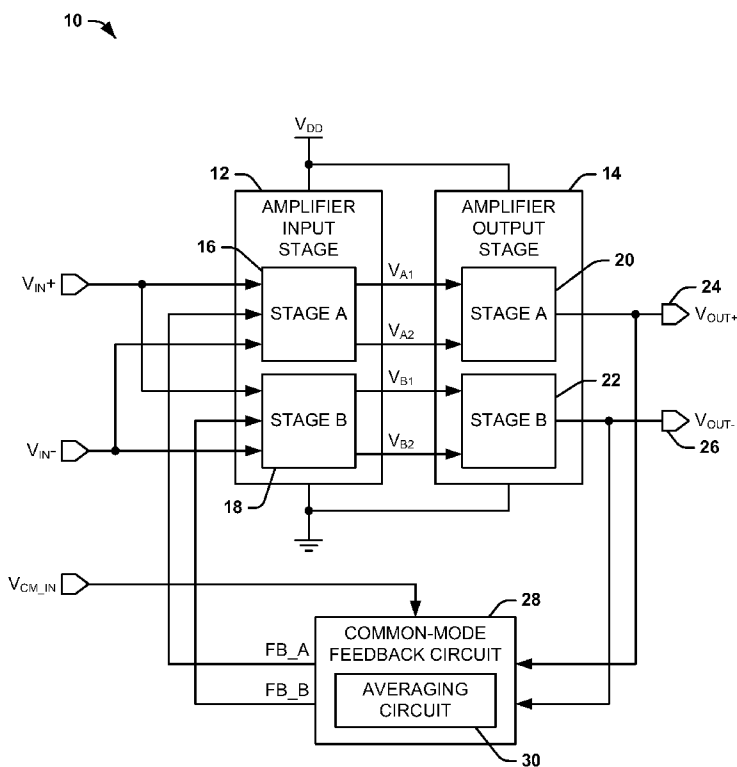


FIG. 1

(57) Abstract: One embodiment of the invention includes a differential amplifier circuit (10). A first input stage (16) generates first and second control voltages in response to a differential input signal. A second input stage (18) generates third and fourth control voltages in response to the differential input signal. The first and second control voltages can be inversely proportional and the third and fourth control voltages can be inversely proportional. The circuit also includes a first output stage (20) that is configured to set a magnitude of a first output voltage of a differential output signal at a first output node in response to the first and second control voltages. The circuit further includes a second output stage (22) that is configured to set a magnitude of a second output voltage of the differential output signal at a second output node in response to the third and fourth control voltages.

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**A. CLASSIFICATION OF SUBJECT MATTER****H03F 3/45(2006.01)i, H03F 3/68(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

**B. FIELDS SEARCHED**

Minimum documentation searched (classification system followed by classification symbols)

IPC: H03F 3/45

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

KOREAN UTILITY MODELS AND APPLICATIONS FOR UTILITY MODELS SINCE 1975

JAPANESE UTILITY MODELS AND APPLICATIONS FOR UTILITY MODELS SINCE 1975

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKIPASS, PAJ; differential amplifier circuit, input stage, output stage

**C. DOCUMENTS CONSIDERED TO BE RELEVANT**

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2006/0152282 A1 (HALBERT, J.M. et al.) 13 July 2006. see abstract; paragraphs [0041]-[0066]; figures 3-9; claim 1	1-14
A	US 2005/0116777 A1 (BOGNER, P.) 02 June 2005. see abstract; paragraphs [0021]-[0033]; figure 3; claim 15	1-14
A	US 2005/0174171 A1 (OSWAL, S. et al.) 11 August 2005. see abstract; paragraphs [0019]-[0026]; figures 3-5; claim 1	1-14
A	US 6888407 B2 (RAMAZAN, E. et al.) 03 May 2005. see abstract; column 2 line 20-column 3 line 13; figure 2; claim 1	1-14
A	JP 2007-181026 A (NEC ELECTRONICS CO.) 12 July 2007. see abstract; paragraphs <76>-<112>; figures 1-8; claim 1	1-14

 Further documents are listed in the continuation of Box C. See patent family annex.

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**INTERNATIONAL SEARCH REPORT**

Information on patent family members

International application No.

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Patent document cited in search report	Publication date	Patent family member(s)	Publication date
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