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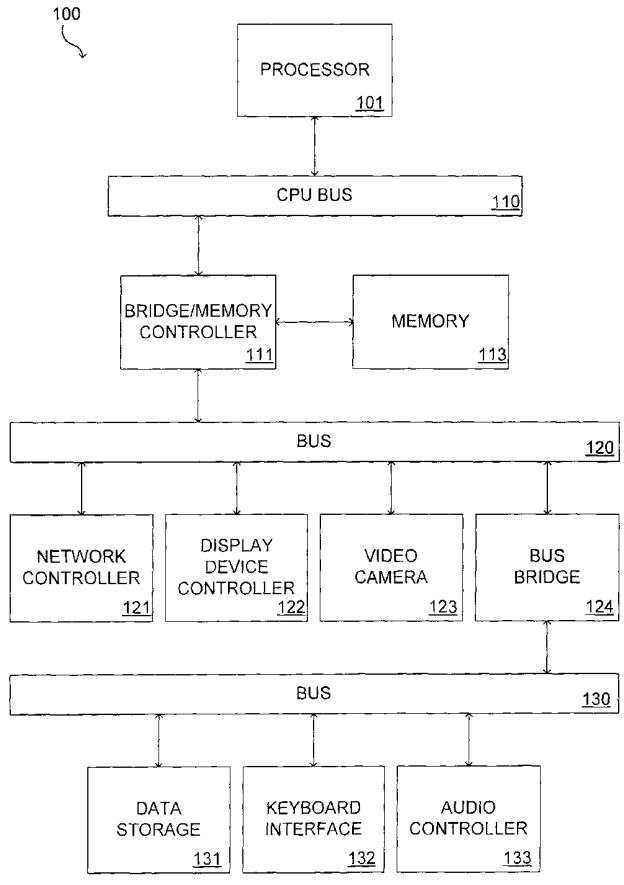

(57) Abstract: A plurality of memory modules interface through a daisy-chain providing a point-to-point connection for each memory module. The first and last memory module in the daisy chain each connect to a separate memory controller port forming a ring circuit. A distinct set of signals connect the memory modules in each direction. A junction circuit in each memory module provides line isolation, a coupling to the adjoining memory modules in the daisy chain, or in the case of the first and last memory module in the daisy chain, a memory module and a memory controller, and a data synchronization circuit. Each junction circuit provides as well as voltage conversion so that the memory devices on a memory module operate at a different voltage than the memory controller, and multiplexing/de-mulitplexing so that a lesser number of lines interfaces with each junction circuit.

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APPARATUS FOR IMPLEMENTING A BUFFERED DAISY-CHAIN RING CONNECTION BETWEEN A MEMORY CONTROLLER AND MEMORY MODULES

FIELD OF THE INVENTION

The present invention relates to memory systems in computer systems. More specifically, the present invention relates to an apparatus for implementing a buffered daisy chain ring connection between a memory controller and memory modules.

BACKGROUND OF THE INVENTION

Memory modules such as the Dual In-Line Memory Module (DIMM) have become a popular memory packaging design. DIMMs are small printed circuit boards mounted with a plurality of memory devices. DIMMs have leads accessible via both sides of a printed circuit board's electrical connector unlike its predecessor, the Single In-Line Memory Module (SIMM), which has leads on only one side of the printed circuit board's electrical connector. DIMMs are inserted into small socket connectors that are soldered onto a larger printed circuit board, or motherboard. A plural number of memory modules are usually typically directly connected to a memory controller via multi-drop connections to a memory bus that is coupled to the memory side of the memory controller. The memory controller transmits and receives memory data via the memory bus. Each of the memory modules includes a plurality of memory devices mounted on the memory module. The memory devices typically are Dynamic Random Access Memory (DRAM).

Figure 3 illustrates an end on view of a conventional multi-drop routing between a memory controller 111 and two exemplary memory modules 210-211. The memory bus 310 connects to each of the memory devices 210a and 210b through a stub. Stub 310a connects the bus 310 to memory devices 310a. Stub 310b connects the bus 310 to memory devices 211b. The stub introduces a capacitive load discontinuities to the signal being carried to the memory devices 211a and 211b by the bus 310. Furthermore, the

stubs directly connect to the memory devices without any intermediary signal conditioning including a voltage translation.

A drawback to memory modules directly connected to a memory bus via multi-drop connections is that there is no voltage level isolation between the memory devices and the memory controller. This lack of voltage isolation does not permit a variance between the voltage level of memory device inputs and memory controller outputs on the one hand, and memory device outputs and memory controller inputs on the other hand. Thus, in a system in which the signal level of a memory controller is below the memory device permissible range, the memory device will not recognize inputs, and memory device outputs will exceed the safe operating level of the memory controller or a coupled CPU.

Another drawback to memory modules directly connecting to a memory bus via multi-drop connections is that there is no capacitive load isolation between the multi-drop bus and the memory devices causing memory device operation that is slower than it would be without the multi-drop line capacitive load.

Another drawback to memory modules coupled to a memory bus via multi-drop connections is that the peak data rate per line on the memory bus is smaller than it would otherwise be because the discontinuities on a multi-point bus have an impedance that increases with frequency. This lower peak data rate per line places a higher floor on the number of pins connecting to a memory module for a given signal that would otherwise be for a point-to-point connection.

SUMMARY

According to an embodiment, a memory module includes at least one memory device and a junction circuit. The junction circuit has a first port to couple to a bus from alternatively a memory controller and a daisy-chained other memory module. The junction circuits has a second port coupled to the memory devices, and a third port to couple to a bus from alternatively a memory controller or a daisy-chained other memory

module. The junction circuit sends data received from the first port to the second port and the third port, sends data received from the second port to the first port and the third port, and send data received from the third port to the second port and the first port. The junction circuit also includes an isolation circuit to provide a point-to-point connection to the first port and the third port, and a data synchronization circuit in electrical communication with the first port, the second port, and the third port to synchronize the data input to the first port with the data input to the third port.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention is illustrated by way of example and not by way of limitation in the figures of the accompanying drawings in which:

Figure 1 is a block diagram of a computer system implementing an embodiment of the present invention;

Figure 2 illustrates a memory system mounted on a motherboard according to an embodiment of the present invention;

Figure 3 illustrates an end on view of a conventional multi-drop routing between a memory controller and two exemplary memory modules;

Figure 4 illustrates a bus routing and wiring topology for a memory system according to an embodiment of the present invention;

Figure 5 illustrates a junction circuit according to an embodiment of the present invention.

DETAILED DESCRIPTION

Figure 1 illustrates a computer system 100 upon which an embodiment of the present invention can be implemented. Referring to Figure 1, the computer system 100 includes a processor 101 that processes data signals. The processor 101 may be a complex instruction set computer (CISC) microprocessor, a reduced instruction set computing (RISC) microprocessor, a very long instruction word (VLIW) microprocessor, a processor

implementing a combination of instruction sets, or other processor device. Figure 1 shows an example of the present invention implemented on a single processor computer system 100. However, it is understood that the present invention may be implemented in a computer system having multiple processors. The processor 101 is coupled to a central processing unit CPU bus 110 that transmits data signals between processor 101 and other components in the computer system 100.

The computer system 100 includes a memory system 113. The memory system 113 may include a dynamic random access memory (DRAM) device, a synchronous direct random access memory (SDRAM) device, a double data rate (DDR) SDRAM, a quad data rate (QDR) SDRAM a D^3DDR SDRAM or other memory device (not shown). The memory system 113 may store instructions and code represented by data signals that may be executed by the processor 101. According to an embodiment of the computer system 100, the memory system 113 comprises a plurality of memory modules 210-212 (portrayed in Figure 2), portrayed as an exemplary three memory modules. Each printed circuit board generally operates as a daughter card insertable into a socket connector that is connected to the computer system 100.

A bridge memory controller 111 is coupled to the CPU bus 110 and the memory 113. The bridge memory controller 111 directs data signals between the processor 101, the memory system 113, and other components in the computer system 100 and bridges the data signals between the CPU bus 110, the memory system 113, and a first I/O bus 120. The processor 101, CPU bus 110, bridge/memory controller 111, and memory system 113 are together generally mounted on a common motherboard and are collectively referred to as the computer chipset 200 portrayed with reference to Figure 2.

The first I/O bus 120 may be a single bus or a combination of multiple buses. As an example, the first I/O bus 120 may comprise a Peripheral Component Interconnect (PCI) bus, a Personal Computer Memory Card International Association (PCMCIA) bus, a NuBus, or other buses. The first I/O bus 120 provides communication links between

components in the computer system 100. A network controller 121 is coupled to the first I/O bus 120. The network controller 121 links the computer system 100 to a network of computers (not shown in Figure 1) and supports communication among the machines. A display device controller 122 is coupled to the first I/O bus 120. The display device controller 122 allows coupling of a display device (not shown) to the computer system 100 and acts as an interface between the display device and the computer system 100. The display device controller 122 may be a monochrome display adapter (MDA) card, a color graphics adapter (CGA) card, an enhanced graphics adapter (EGA) card, an extended graphics array (XGA) card or other display device controller. The display device may be a television set, a computer monitor, a flat panel display or other display device. The display device receives data signals from the processor 101 through the display device controller 122 and displays the information and data signals to the user of the computer system 100. A video camera 123 is coupled to the first I/O bus 120.

A second I/O bus 130 may be a single bus or a combination of multiple buses. As an example, the second I/O bus 130 may comprise a PCI bus, a PCMCIA bus, a NuBus, an Industry Standard Architecture (ISA) bus, or other buses. The second I/O bus 130 provides communication links between components in the computer system 100. A data storage device 131 is coupled to the second I/O bus 130. The data storage device 131 may be a hard disk drive, a floppy disk drive, a CD-ROM device, a flash memory device or other mass storage device. A keyboard interface 132 is coupled to the second I/O bus 130. The keyboard interface 132 may be a keyboard controller or other keyboard interface. The keyboard interface 132 may be a dedicated device or can reside in another device such as a bus controller or other controller. The keyboard interface 132 allows coupling of a keyboard (not shown) to the computer system 100 and transmits data signals from a keyboard to the computer system 100. An audio controller 133 is coupled to the second I/O bus 130. The audio controller 133 operates to coordinate the recording and playing of sounds is also coupled to the I/O bus 130. A bus bridge 124 couples the first I/O bus 120

to the second I/O bus 130. The bus bridge 124 operates to buffer and bridge data signals between the first I/O bus 120 and the second I/O bus 130.

Figure 2 illustrates a memory system 113 according to an embodiment of the present invention. Referring to Figure 2. the memory system 113 generally resides on a motherboard 200 of the computer system 100. The motherboard 200 is a printed circuit board that interconnects components of the computer system 100 such as the bridge memory controller 111, the processor 101 and other components. The memory system 113 includes a plurality of memory modules 210-212. Each of the memory modules 210-212 comprises a printed circuit board 210a-212a mounting a plurality of memory devices 210b-212b. The memory system also generally includes a plurality of socket connectors 220-222 mounted on the motherboard 200. The memory modules 210-212 are insertable into the socket connectors 220-222. Electrical connectors on the memory module interface with electrical contacts in the socket connector. The electrical connectors and the electrical contacts allow components on the motherboard 200 to access the memory devices on the memory module. It should be appreciated that any number of socket connectors may be mounted on the motherboard to receive any number of memory modules. It should also be appreciated that any number of memory devices may be mounted on each memory module. The memory system 113 may be implemented in a computer system which partitions I/O structures differently than the one illustrated in Figure 1.

Figure 4 illustrates a bus routing and topology for the present invention for an embodiment having more than one memory modules, here portrayed as daisy-chained memory modules 310a and 310b, wherein each memory module is connected in a daisy-chain according to the interfaces portrayed herein, and wherein the daisy-chained memory modules 310a and 310b are connected in a ring with the memory controller 111. The first memory module 310a in the daisy-chain is connected on a first port 314a to the memory controller 111 via a separate bus 320, and the last memory module 310b in the daisy-chain

is connected on a third port 315b to the memory controller 111 via a separate bus 330. The bus 320 transmits and receives to and from the memory modules in the daisy-chain a first set of data including at least one of at least one memory-data line and one non-memory data line. The bus 330 data transmits and receives to and from the memory modules in the daisy-chain a second set of data including at least one of at least one memory-data line and one non-memory data line. The non-memory data signals may include at least one of address lines, command lines, and clock lines.

The memory module 310a includes the junction circuit 312a, also referred to as a buffer. The bus 320 is coupled to a first port 314a of the junction circuit 312a. The junction circuit 312a is coupled to memory devices 311a by a bus from port 313a of junction circuit 312a to port 316a of the memory devices 311a, wherein the port 316a is representative of each of the separate memory devices that populate the memory module 311a. The junction circuit 312a is further coupled by a bus 325 between a port 315a of the junction circuit 312a to a port 314b of the junction circuit 312b. The data input to the junction circuit 312a from bus 320 is routed by the junction circuit 312a to port 315a and transmitted through bus 325 to junction circuit 312b. The data input to the junction circuit 312a on port 315a from the junction circuit 312b is routed through port 315a to the bus 320.

The memory module 310b includes the junction circuit 312b. The junction circuit 320b is coupled by a bus from a port 313b to the memory devices 311b, wherein the port 316b is representative of each of the separate memory devices that populate the memory module 310b. The data input to the junction circuit 312b at port 314b from junction circuit 312a is routed by the junction circuit 312b to port 315b and transmitted via bus 330 to the memory controller 111. The data input to the junction circuit 312b from the memory controller 111 via bus 330 is input and routed through port 315b to the bus 325. The data transmitted to and from junction circuit 312b is routed through bus 330 to and from the memory controller 111. The data transmitted from the memory devices 311a and

311b are routed through bus 320 for data conforming to the first set of data, and are routed through bus 330 for data conforming to the second set of data.

Figure 5 is a block diagram of a junction circuit 500 also referred to as a buffer according to an embodiment of the present invention. Referring to Figure 5, it is understood that the junction circuit 500 includes other circuitry well known in the art such as signal regeneration circuitry and signal synchronization circuitry. Each of blocks 510, 520, 530, and 540 represents a separate circuit function of the present invention. However, it is understood that more than one function can be performed by the same circuit elements, such as a voltage translation circuit can also provide a capacitive isolation to a signal line. Moreover, it is understood that the sequence of process functions represented by the blocks 510, 520, 530, and 540 may be varied.

It is understood that because block 530 represents a voltage translation circuit that includes both a voltage raising function and a voltage lowering function, the voltage raising circuitry and the voltage lowering circuit include separate circuitry that can each be coupled in different positions in the data path. Moreover it is understood that because block 540 represents a multiplexing/de-multiplexing function that includes both a multiplexing function and a de-multiplexing function, the multiplexing circuit and the de-multiplexing circuit include separate circuitry that can each be coupled in different positions in the data path.

It is preferred that the de-multiplexing function represented by multiplexing/de-multiplexing block 540 be performed after the voltage translation function represented by block 530, and that the multiplexing function represented by block 540 be performed before the voltage translation function represented by block 530. This is because the de-multiplexing functions translates an input signal on a given number of lines into an output signal on a greater number of lines, and the multiplexing function translates an input signal on a given number of lines into an output signal on a lesser number of lines. Thus, by de-multiplexing after the voltage translation results in a smaller number of circuits to perform

the voltage translation function, and by multiplexing before the voltage translation results in a smaller number of circuits to perform the voltage translation function.

Moreover the voltage translation function represented by block 530 to raise the data signal to a level in accordance with the requirements of memory devices can be performed on the data signal carried by bus 503a by performing a voltage raising function represented by block 530 on the data signal before it is ported out to bus 503a, then the voltage of the data signal carried by bus 503a must then be lowered by the voltage translation function represented by block 530 by placement of voltage lowering circuitry in the bus 503a data path.

A memory bus 550 couples to the junction circuit 500 at port 501. The memory bus 550 includes a plurality of lines that includes at least one of at least one memory-data lines and at least one non-memory data lines that may include addressing lines, command lines, and clock lines, and that shall be referred to hereafter as ADD/CMD lines. The memory bus 550 transmits to the junction circuit 500 (and other memory devices on other memory modules (not shown) and the memory controller (not shown)) a first set of data lines. The memory bus 550 receives from the junction circuit 500 (and other memory modules (not shown) and the memory controller (not shown)) data for a second set data lines. The preferred embodiment first set of data lines and second set of data lines are exclusive and together constitutes the total data lines needed for the memory devices 560.

A memory bus 570 couples to the junction circuit at port 503. The memory bus 550 includes a plurality of lines that includes at least one of at least one memory-data lines and at least one ADD/CMD lines. The memory bus 570 transmits to the junction circuit 500 (and other memory devices on other memory modules (not shown) and the memory controller (not shown)) a third set of data lines (not shown). The memory bus 550 receives from the junction circuit 500 (and other memory modules (not shown) and the memory controller (not shown)) data for a fourth set data lines (not shown). The preferred embodiment third set of data lines and fourth set of data lines are exclusive and together

constitutes the total data lines needed for the memory devices 560. The first data set, second data set, third data set, and fourth data together constitute a transmission and a reception of the total data lines needed for the memory devices 560 (and all other data devices in the ring).

The bus lines 550 and 570 are each coupled to a capacitive isolation circuit represented by block 510 to isolate the junction circuit 500 from the buses 550 and 570, resulting in a point to point connection between the junction circuit 500 and the other memory modules and memory controller on the ring topology daisy chain, rather than the conventional multi-drop configuration for a circuit having a plurality of memory modules as portrayed with reference to Figure 3. The data transmitted to the junction circuit 500 from the bus 570 is routed to bus 503a and transmitted on bus 570 to a port 501 of a daisy-chained junction circuit. The data from the daisy-chained junction circuit is received by junction circuit 500 on bus 570 at port 503, and routed to the port 501 to the bus 550. The capacitive isolation circuit 510 provides a termination for the bus 550 and allows the bus 550 to achieve much higher frequencies due to very limited impedance discontinuities on the bus 550. Impedance discontinuities cause reflections in the waveform limiting the maximum frequency on the bus 550. With lower discontinuities on the bus, the frequency of the bus can be increased to a much higher rate over existing multi-drop memory buses. Also, given that the junction circuit 500 buffering contains all of the high speed interface, the memory devices 560 are freed of the burden of having the high speed logic and can be made less expensively. The isolation circuit 510 is coupled to both a data synchronization circuit 520 via bus 510a, and an output port 503 via bus 503a.

The bus 510a for the purpose of this embodiment transmits data to the data synchronization circuit 520 for the memory devices 560. The synchronization circuit 520 synchronized the data received from the bus 550 with the data received from the bus 570, because the total data transmission from bus 550 and 570 constitutes the total data signal to the memory devices 560. Because the data from bus 550 and from bus 570 each pass

through a not necessarily equal number of memory modules (if any) before reception by the memory junction circuit 500, they arrive at different times because there is at least a one clock delay to transit a memory module. The data synchronization circuit synchronizes the two data streams depending upon the difference in arrival time caused by the number of intermediate other memory modules the data input to ports 501 and 503 each pass through before input to the junction circuit 500, and transmit the synchronized data to the memory devices through the voltage translation circuit in this embodiment. The bus 510b for the purpose of this embodiment transmits data from the memory devices to the isolation circuit 510, because a synchronization is preferably applied only to the data transmitted to the memory devices 560.

The bus 520a for the purpose of this embodiment transmits data to the voltage translation circuit 530 for the memory devices 560, and the bus 510b transmits data to the isolation circuit 510 from the memory devices 560. The voltage translation function 530 includes a voltage raising circuit to translate the voltage range of each separate signal input to the junction circuit 500 from bus 550 (dependent upon the position of the de-multiplexing circuit) from a range commensurate with a transmission from a memory controller or CPU, to a range commensurate with an input to the memory devices 560. The voltage translation function 530 includes a voltage lowering circuit to translate the voltage range of each separate signal output from the memory devices (dependent upon the position of the multiplexing circuit) from a range commensurate with a transmission from a memory device, to a range commensurate with an input to a memory controller or a CPU.

The bus 530a for the purpose of this embodiment transmits data to the de-multiplexing circuit of the multiplexing/de-multiplexing function 540 from the voltage translation function 530 and from the multiplexing circuit of the multiplexing/de-multiplexing function 540 to the voltage translation function 530. The de-multiplexing circuit processes an input having n lines, and de-multiplexes the input so that the output

has m lines, wherein n is less than m (where m and n can be expressed alternatively as p and q). Thus, the input bit rate on each line is decreased by a ratio of n/m to maintain the same bandwidth on the input side as on the output side of the de-multiplexer circuit. Thus, the present invention enables a smaller number of data lines input to the junction circuit 500 than the memory devices 560 require allowing a narrower connecting bus 550 and 570. Moreover, because only a portion of the data is received and transmitted on each bus 550 and 570, each of the buses may have a lower bandwidth and a smaller number of lines than would otherwise be necessary. This lowers the number of required pins on the memory module 560. Furthermore, the present invention enables lower frequencies on the input bus 501, thus decreases the power lost to capacitive load. The bus 540a for the purpose of this embodiment transmits data from the junction circuit port 502 to the multiplexing circuit of the multiplexing/de-multiplexing function 540, and transmits data from the de-multiplexing circuit of the multiplexer/de-multiplexer function 540 to the junction circuit port 502. The multiplexing circuit processes an input having m lines, and de-multiplexes the input so that the output has n lines, wherein n is less than m. Thus, the output bit rate on each line is increased by a ratio of m/n to maintain the same bandwidth on the input side as on the output side of the multiplexer circuit. Thus, the present invention enables a smaller number of data lines input to the junction circuit 500 than the memory devices 560 require. This lowers the number of required pins on the memory module. Furthermore, the present invention enables a lower frequencies on the input bus 501, thus decreased the power lost to capacitive load.

From junction circuit port 502, data is input and output to the memory devices 560 over the individual buses 560a-560h, and ADD/CMD data is input to the memory devices over the bus 560i. It is specifically understood that the need to signal condition individual ADD/CMD lines, and to signal condition memory data lines is different because of the possible differing requirements with regard to voltage translation and multiplexing/de-multiplexing. Accordingly, it is specifically contemplated that different multiplexer, de-

multiplexer, and voltage translation circuits will be used for each. Furthermore, different embodiments of the present invention may not apply the isolation functions, the voltage translation functions, or the multiplexing/de-multiplexing functions to both the memory-data and the ADD/CMD data. Additionally, an embodiment of the present invention may not include the CMD/ADD data being transmitted from a junction circuit 500 from a port 501, and accordingly will not require the isolation function, the voltage lowering function, and the multiplexing function to a return ADD/CMD signal. A preferred embodiment includes two physically separate memory-data processing circuits, each memory-data circuit coupled to an exclusive subset of the memory devices 560, and one physically separate ADD/CMD processing circuit, each circuit including according to the embodiment the voltage translation, the isolation, and the multiplexing/de-multiplexing circuits. The two separate memory data-circuits enabling a data line topology that is more straightforward than would be the case with a unitary device.

In the foregoing description, the invention is described with reference to specific exemplary embodiments thereof. It will, however, be evident that various modifications and changes may be made thereto without departing from the broader spirit and scope of the present invention as set forth in the appended claims. The specification and drawings are to be regarded in an illustrative rather than a restrictive sense.

CLAIMS

What is claimed is:

1. A memory module comprising:

at least one first memory device;

a junction circuit coupled to the a first port and a second port and coupled to a memory port, wherein the memory port is coupled to the at least one first memory device, and wherein the junction circuit has at least one function selected from isolation, data synchronization for the first port and the second port, voltage translation, and multiplexing/de-multiplexing; and

wherein the first port and the second port comprise connections to a communications bus function.

2. The memory module according to claim 1, further comprising:

a front-end bus line in communication to the first port; and

a back-end bus line in communication to the second port.

3. The memory module according to claim 2 wherein the back-end bus line is disposed between the at least one first memory device and at least one second memory device.

4. The memory module according to claim 2, further comprising:

a long memory bus coupled between the at least one second memory device, and

wherein the front-end memory bus line and the long memory bus are coupled to a memory control function.

5. A first memory module comprising:

at least one memory device;

a junction circuit having a first port to couple to a bus from at least one of a memory controller and at least one daisy-chained memory module that includes first data lines characterized by at least one of at least one memory-data line and at least one non-memory-data line; a second port coupled to the memory devices; a third port to couple to a bus from at least one of a memory controller and at least one daisy-chained memory module that includes second data lines characterized by at least one of at least one memory-data line and at least one non-memory data line; to send data received from the first port to the second port and the third port, to send data received from the second port to the first port and the third port, and to send data received from the third port to the second port and the first port, and that includes

an isolation circuit to provide a point-to-point connection to the first port and the third port, and

a data synchronization circuit in electrical communication with the first port, the second port, and the third port to synchronize the data input to the first port with the data input to the third port, depending upon the difference in arrival time between the data input to port 1 and the data input to port 2 caused by the number of intermediate other memory modules the data input to port 1 and the data input to port 2 each pass through before input to the junction circuit, and transmit the synchronized data to the third port.

6. The memory module defined in claim 5 wherein the junction circuit further includes a voltage translation circuit to raise the voltage of each line input on the first port and the third port and output on the second port from a voltage range commensurate with a transmission by a memory controller to a voltage range commensurate with the memory devices, and to lower the voltage of each line input on the second port and output on the first port and the third port from a voltage range commensurate with the memory devices to a voltage range commensurate with a reception by the memory controller, the voltage

translation circuit being in electrical communication with the first port, the second port, and the third port.

7. The memory module defined in claim 5 wherein the junction circuit further includes:

a de-multiplexer circuit in electrical communication with the first port, the second port, and the third port to de-multiplex a signal input on the memory data lines to the first port and the third port having a first bandwidth transmitted on n input lines, each input line having a bit rate of m, to a data signal having the first bandwidth transmitted on n-prime lines having a bit rate of m-prime wherein n is less than n-prime and m is greater than m-prime; and

a multiplexer circuit in electrical communication with the first port, the second port, and the third port to de-multiplex a signal input on the memory-data lines to the second port having a first bandwidth transmitted on n-prime input lines, each input line having a bit rate of m-prime, to a data signal having the first bandwidth transmitted on n lines having a bit rate of m wherein n is less than n-prime and m is greater than m-prime.

8. The memory module defined in claim 5 wherein the junction circuit further includes:

a de-multiplexer circuit in electrical communication with the first port, the second port, and the third port to de-multiplex a signal input on the non-memory data lines to the first port and the third port having a first bandwidth transmitted on q input lines, each input line having a bit rate of p, to a data signal having the first bandwidth transmitted on q-prime lines having a bit rate of p-prime wherein q is less than q-prime and p is greater than p-prime; and

a multiplexer circuit in electrical communication with the first port, the second port. and the third port to de-multiplex a signal input on the non-memory-data lines to the

second port having a first bandwidth transmitted on q-prime input lines, each input line having a bit rate of p-prime, to a data signal having the first bandwidth transmitted on q lines having a bit rate of p wherein q is less than q-prime and p is greater than p-prime.

9. A memory system having a plural number of memory modules

wherein each memory module comprises:

at least one memory device and

a junction circuit having a first port to couple to a bus from at least one of a memory controller and at least one daisy-chained memory module that includes first data lines characterized by at least one of at least one memory-data line and at least one non-memory-data line; a second port coupled to the memory devices; a third port to couple to a bus from at least one of a memory controller and at least one daisy-chained memory module that includes second data lines characterized by at least one of at least one memory-data line and at least one non-memory data line; to send data received from the first port to the second port and the third port, to send data received from the second port to the first port and the third port, and to send data received from the third port to the second port and the first port, and that includes

an isolation circuit to provide a point-to-point connection to the first port and the third port, and

a data synchronization circuit in electrical communication with the first port, the second port, and the third port to synchronize the data input to the first port with the data input to the third port, depending upon the difference in arrival time between the data input to port 1 and the data input to port 2 caused by the number of intermediate other memory modules the data input to port 1 and the data input to port 2 each pass through before input to the junction circuit, and transmit the synchronized data to the third port.

wherein the memory modules are connected in a daisy-chain that includes a memory module third port coupled by a bus to a succeeding memory module first port

wherein the first port of the first memory module in the daisy-chain is to be coupled by a first bus that includes a first exclusive set of data lines to a first port of a memory controller, and the third port of the last memory module in the daisy chain is to be coupled by a second bus that includes a second exclusive set of data lines to a second port of the memory controller.

10. The memory system defined in claim 9 wherein the junction circuit further includes a voltage translation circuit to raise the voltage of each line input on the first port and the third port and output on the second port from a voltage range commensurate with a transmission by a memory controller to a voltage range commensurate with the memory devices, and to lower the voltage of each line input on the second port and output on the first port and the third port from a voltage range commensurate with the memory devices to a voltage range commensurate with a reception by the memory controller, the voltage translation circuit being in electrical communication with the first port, the second port, and the third port.

11. The memory system defined in claim 9 wherein the junction circuit further includes:

a de-multiplexer circuit in electrical communication with the first port, the second port, and the third port to de-multiplex a signal input on the memory data lines to the first port and the third port having a first bandwidth transmitted on n input lines, each input line having a bit rate of m, to a data signal having the first bandwidth transmitted on n-prime lines having a bit rate of m-prime wherein n is less than n-prime and m is greater than m-prime; and

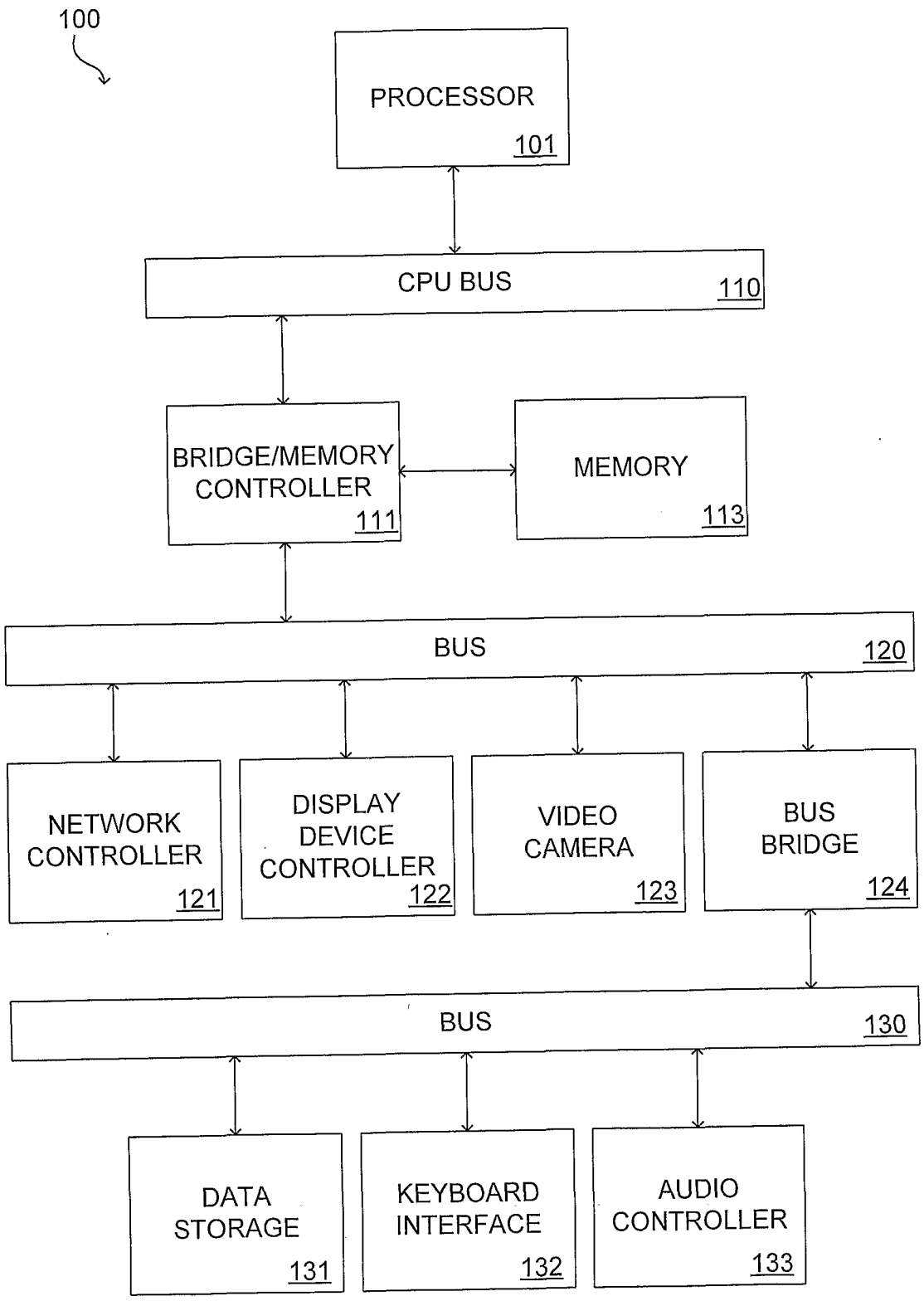
a multiplexer circuit in electrical communication with the first port, the second port, and the third port to de-multiplex a signal input on the memory-data lines to the second port having a first bandwidth transmitted on n-prime input lines, each input line

having a bit rate of m-prime, to a data signal having the first bandwidth transmitted on n lines having a bit rate of m wherein n is less than n-prime and m is greater than m-prime.

12. The memory system defined in claim 9 wherein the junction circuit further includes:

a de-multiplexer circuit in electrical communication with the first port, the second port, and the third port to de-multiplex a signal input on the non-memory data lines to the first port and the third port having a first bandwidth transmitted on q input lines, each input line having a bit rate of p, to a data signal having the first bandwidth transmitted on q-prime lines having a bit rate of p-prime wherein q is less than q-prime and p is greater than p-prime; and

a multiplexer circuit in electrical communication with the first port, the second port. and the third port to de-multiplex a signal input on the non-memory-data lines to the second port having a first bandwidth transmitted on q-prime input lines, each input line having a bit rate of p-prime, to a data signal having the first bandwidth transmitted on q lines having a bit rate of p wherein q is less than q-prime and p is greater than p-prime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PROCESSOR
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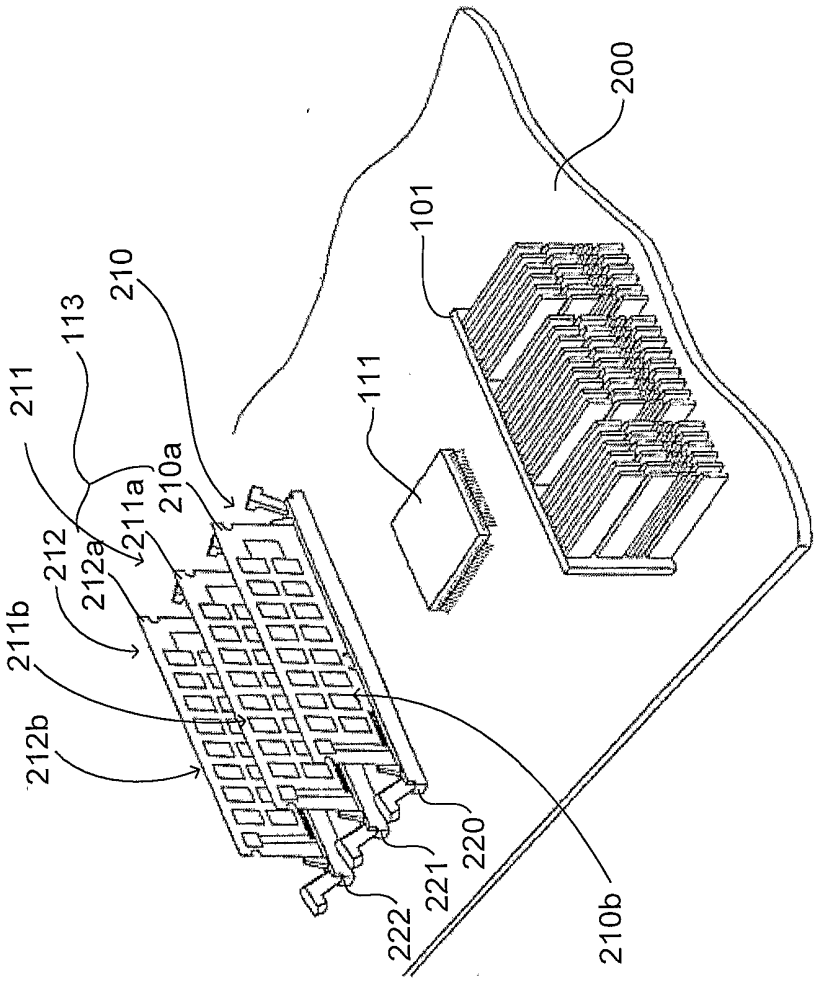
CPU BUS
110
BRIDGE/MEMORY CONTROLLER
111
MEMORY
113
BUS
120
NETWORK CONTROLLER
121
DISPLAY DEVICE CONTROLLER
122
VIDEO CAMERA
123
BUS BRIDGE
124
BUS
130
DATA STORAGE
131
KEYBOARD INTERFACE
132
AUDIO CONTROLLER
133

FIGURE 1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212b
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222
210b

FIGURE 2

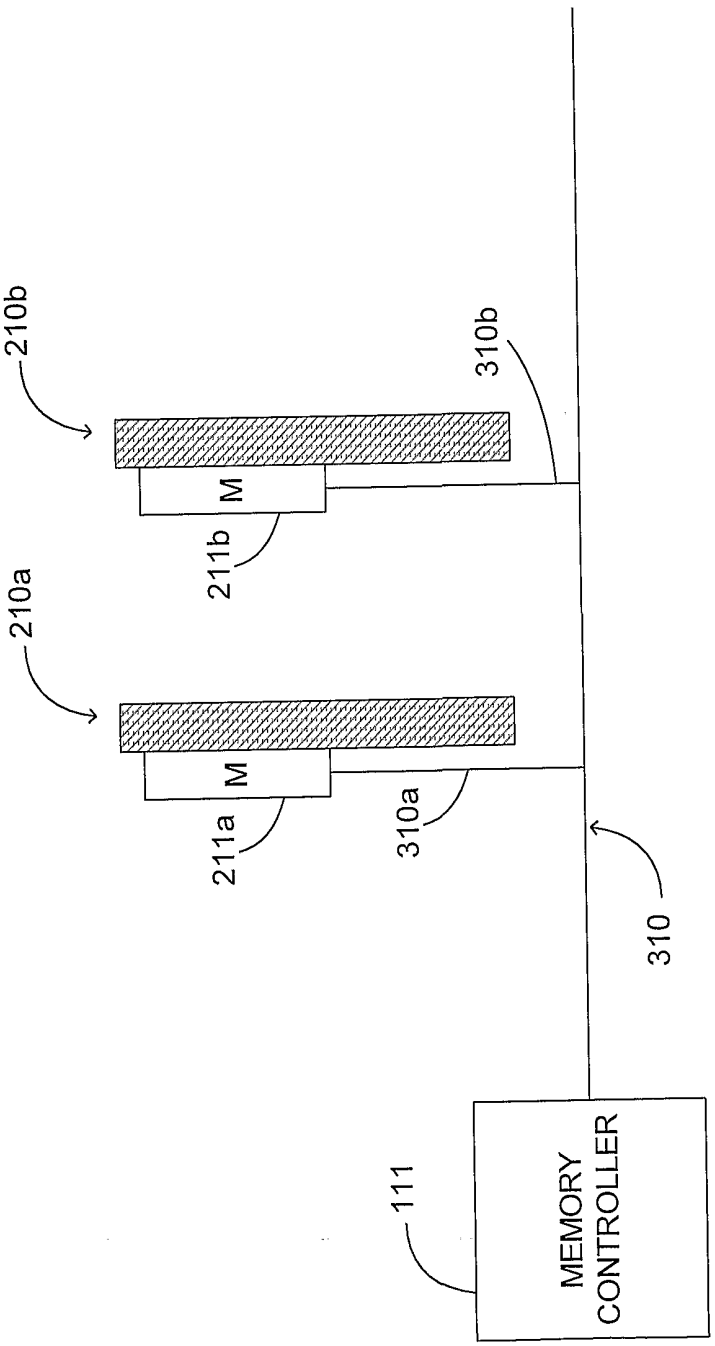
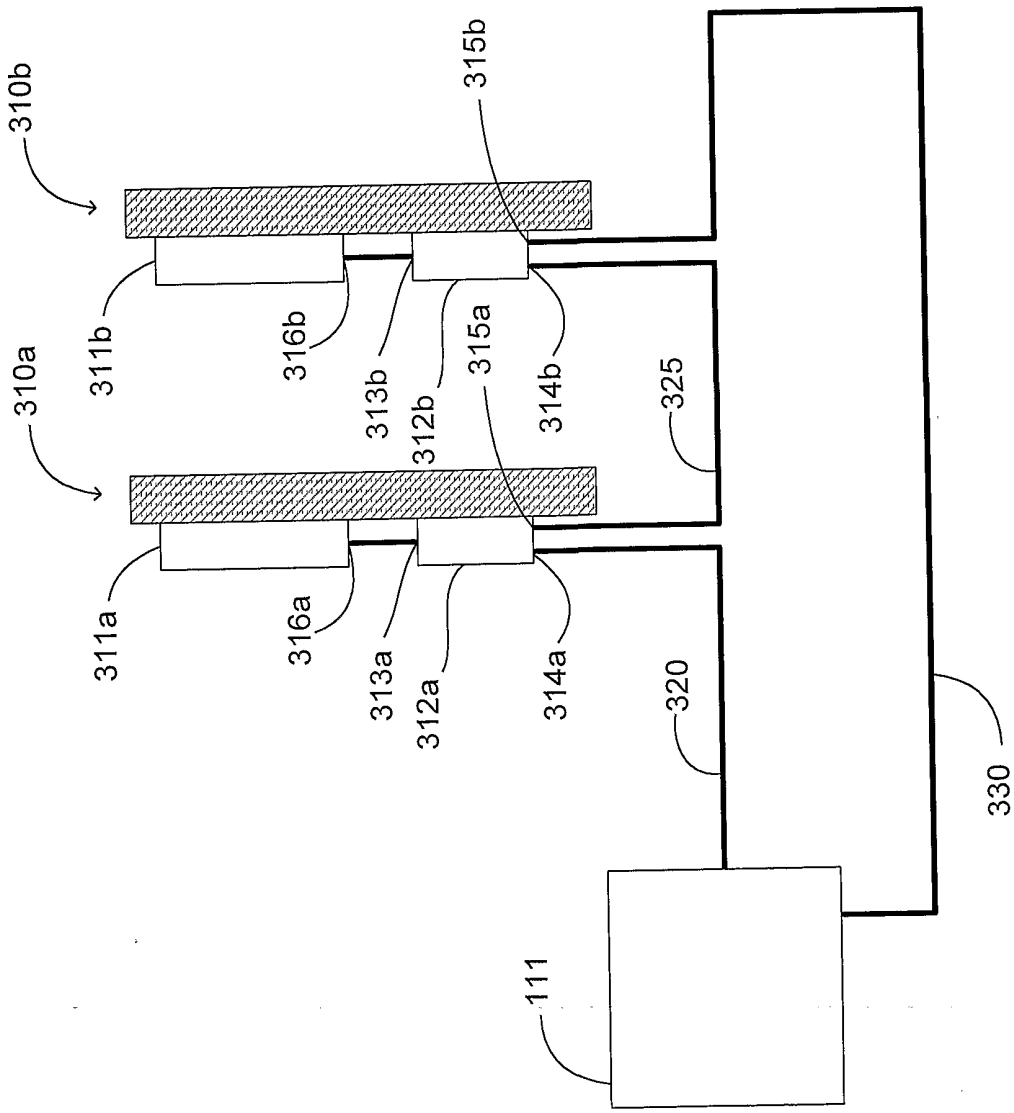


FIGURE 3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311b
316b
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312b
315a
314b
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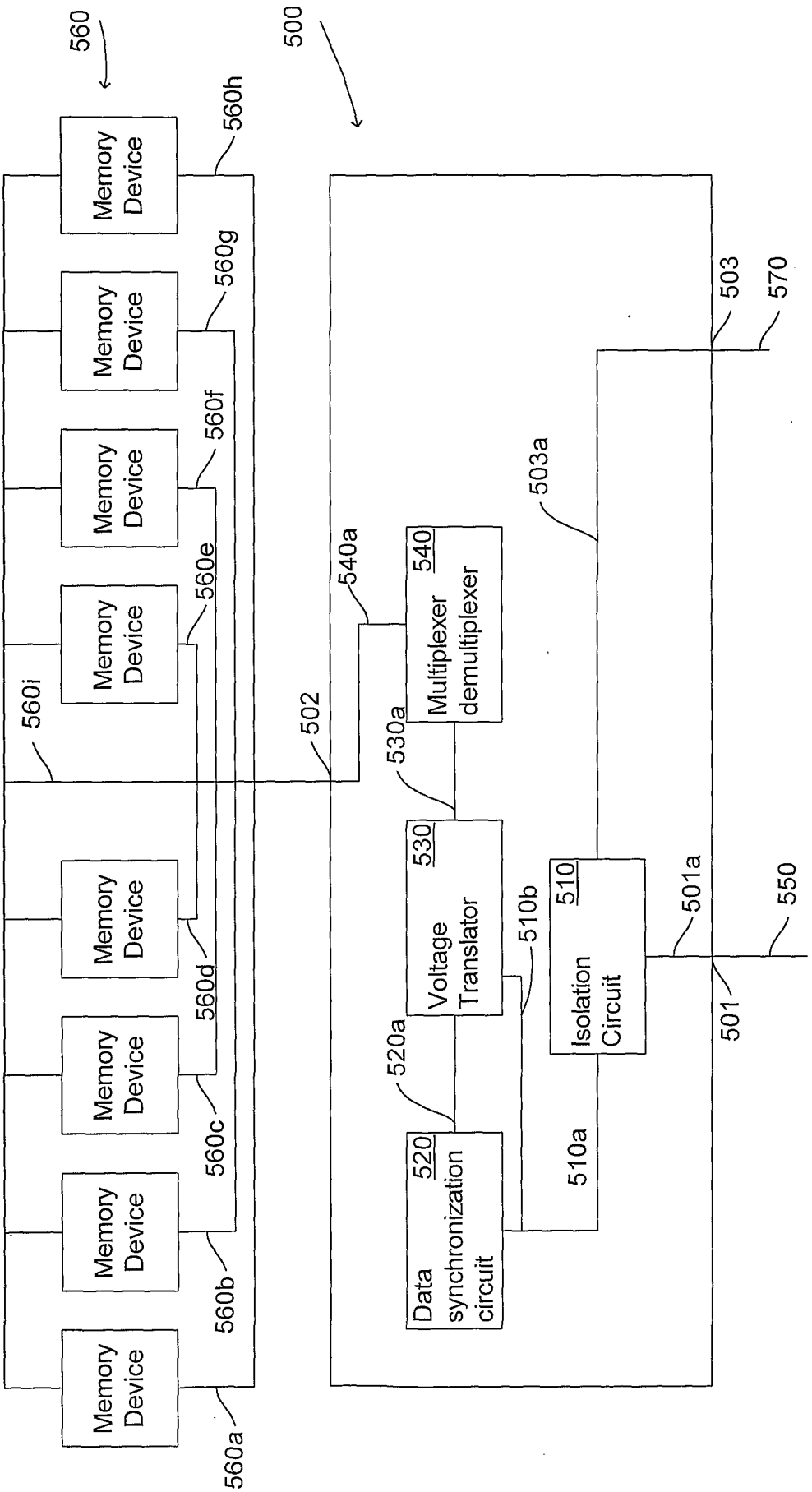
310a
311a
316a
313a
312a
314a
320
330
111

FIGURE 4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Memory Device
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560g
560f
560e
560d
560c
560b
560a
560i
502
540a
Multiplexer demultiplexer 540
530a
Voltage Translator 530
520a
Data synchronization circuit 520
510b
Isolation Circuit 510
510a
503a
503
570
501a
550
501

FIGURE 5