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(54) **Low output noise density low power ldo voltage regulator**

Leistungsarmer LDO-Spannungsregler mit geringer Ausgangsrauschdichte

Régulateur de tension LDO à faible puissance et bruit de sortie à faible densité

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CN-A- 102 681 584 **US-A- 5 325 045**

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Description

BACKGROUND

Technical Field

[0001] The present invention generally relates to Low-Dropout (LDO) voltage regulators used in the design of Integrated Circuits (IC), and more particularly to such regulators having low output noise density and low internal power consumption.

Related Art

[0002] The approaches described in this section could be pursued, but are not necessarily approaches that have been previously conceived or pursued. Therefore, unless otherwise indicated herein, the approaches described in this section are not prior art to the claims in this application and are not admitted to be prior art by inclusion in this section.

[0003] LDO regulators work in the same way as all linear voltage regulators. However, LDO regulators utilize open collector or open drain output transistor (also named "pass transistor"), instead of the emitter follower pass transistor used in non-LDO regulators. Thus, the output transistor of LDO regulators operates in the saturation range. The result which is achieved is that the voltage drop from the unregulated voltage to the regulated voltage can be as low as the saturation voltage across the output transistor. In other words, and as their name suggests, LDO voltage regulators are characterized by their low drop-out voltage.

[0004] To avoid any degradation of the served functional blocks, also named "IP blocks" in the art of IC design, a LDO regulator should provide a regulated voltage with a very low output noise density while limiting the internal power consumption. Integrated capacitors may be used to stabilize the structure, because a strong current is necessary to obtain low noise output voltage. Consequently, the size of the LDO is strongly increased. However, keeping the silicon area used by the integrated circuit as low as possible is an additional, general constraint for all ICs. Reference EP1624357 discloses a typical LDO voltage regulator topology, which uses a band-gap reference voltage generator, a comparator, and a power output stage. These three elements are independent of each other, with only one return path from the output stage to one of the comparator inputs. The output stage comprises a resistor voltage divider for generating a feedback voltage for the return path. The band-gap reference voltage generator can have a single *Vbe* structure or a double *Vbe* structure. Despite some performance limits, such structures are very simple to implement to provide regulated voltages independent of temperature. A lot of variants of this type of LDO regulator are available. Some are described in further prior art references such as EP0715238, EP1336912, and EP1865397.

[0005] An enhancement of the above structure is described, for instance, in document US7362081, EP1229419, EP1191416, and EP1365302. Such enhancement consists in using a filter on the reference voltage or in the return path. Being controlled by the output stage, this filter can ensure good noise attenuation while not jeopardizing the stability of the system. This filter can be an active filter, suitable for compensating, in particular, noise from the power supply.

[0006] Still other structures, as illustrated for instance in reference US7030598, include two integrated band-gap reference voltage generators. One generator exhibits a double *Vbe* structure and is adapted to provide low noise current, while the other has a single *Vbe* structure and ensures the regulated output voltage reference. This allows very low noise voltage with strong stability at the cost, however, of a high complexity and thus wide silicon area. Double *Vbe* band-gap structures (also known as "stacked *Vbe* band-gap" structures) have become widely used to get very low noise and temperature compensated output voltage LDOs. In most application requiring low power (without output voltage divider), such structure provides an output voltage regulated corresponding only to a multiple of band gap voltage, namely $k \times Vbg$ where k is an integral number. Moreover additional integrated capacitors may be needed to stabilize the structure because a strong current is necessary to obtain low noise output voltage. Consequently the size of the LDO is strongly increased.

[0007] In view of the above, there is still a need for LDO regulators having low output noise density and low internal power consumption, which exhibit better performances in terms of output voltage stability and integration capability, namely the size of the area occupied on the silicon substrate.

SUMMARY

[0008] To address these needs, a first aspect of the present invention relates to a low drop-out voltage regulating circuit comprising, arranged in parallel between a first power supply node and a second power supply node:

- an output node;
- a band-gap voltage reference stage having double *Vbe* structure, adapted to provide a band-gap voltage and a

double band-gap voltage; and,

- an output stage having a pass device controlled by the double band-gap voltage and adapted to drive current into a load connected to the output node under a regulated output voltage, and having circuitry for generating a feedback voltage representative of said output voltage; and,

- a comparator stage having a first input for receiving the band-gap voltage from the reference stage and a second input for receiving the feedback voltage from the output stage, and adapted to control band-gap voltage reference stage.

[0009] Thus, the circuit has a first feedback DC loop adapted to set the current in the band-gap reference stage, in order to provide low noise and temperature compensation. The circuit further comprises a second feedback DC loop adapted to control the pass device of the output stage, in order to provide low drop-out regulated voltage at the output of the circuit. The first and second feedback DC loops are independent one from the other and operate simultaneously. The stability can be ensured by a single capacitor at the output of the circuit, which may be external to the circuit..

[0010] Thanks to the novel structure of the LDO voltage regulating circuit, the controlled output voltage can be tuned from almost the supply voltage down to one time the band-gap voltage (*Vbg*), e.g. approximately 1.2 volt (V), with temperature compensation.

[0011] The proposed structure provides very low noise regulated voltage with a high integration level of components compared to typical regulator structures

[0012] Output capacitor provides good stability to the system and double *Vbe* structure provides low noise. No additional filter is required on the reference voltage, nor in the feedback loop.

[0013] A second aspect of the present invention relates to an integrated circuit comprising a low dropout voltage regulating circuit according to the first aspect.

[0014] The circuit may be, for instance, a frequency synthesizer, a Digital-to-Analog Converter (DAC), a radiofrequency modulator, a power amplifier, etc.

BRIEF DESCRIPTION OF THE DRAWINGS

[0015] Embodiments of the present invention are illustrated by way of example, and not by way of limitation, in the figures of the accompanying drawings, in which like reference numerals refer to similar elements and in which:

- FIG. 1 is a schematic diagram of an embodiment of a low drop-out (LDO) voltage regulating circuit according to the present invention.

- FIG. 2 is a schematic block diagram of the circuit of FIG.1 showing the first DC path alone.

- FIG. 3 is a schematic block diagram of the circuit of FIG.1 showing the second DC path alone.

- FIG. 4 is a schematic block diagram of the circuit of FIG.1 showing the first DC path and the second DC path superposed.

DESCRIPTION OF PREFERRED EMBODIMENTS

[0016] Referring to **FIG.1**, there is shown therein a schematic diagram of an embodiment of a low drop-out (LDO) voltage regulating circuit 1 according to embodiments of the present invention.

[0017] The circuit 1 may be part of an Integrated Circuit (IC) chip. The chip may be, for instance, a frequency synthesizer, a Digital-to-Analog Converter (DAC), a radiofrequency modulator, a power amplifier, etc. It will be appreciated that this list is non exhaustive. Such chips are used, e.g., in radio and television sets, portable telephone, and more generally all wireless applications.

[0018] The LDO regulator 1 mainly comprises first, second and third stages 10, 20 and 30, respectively. Stages 10, 20 and 30 are arranged in parallel between a first power supply node receiving a high supply voltage VDD and a second power supply node receiving a low supply voltage or the ground GND as shown. These nodes may be coupled to respective terminals of the IC, e.g. for receiving the high supply voltage from the exterior of the IC.

[0019] The LDO regulator is operable to generate a regulated output voltage Vout at an output node 2 of the circuit, which is independent of the current sunk by a load (not shown) which can be coupled to said output node 2, and which is not or little sensitive to variations of the high power supply VDD and of temperature. To that end, an output device is controlled by control circuitry to provide the required voltage level for a wide range of current sunk by the load, as required

by the application.

Double Vbe band-gap voltage reference stage

[0020] To that end, stage 10 typically comprises a reference voltage generator having band-gap architecture, hereinafter referred to as the band-gap reference stage or band-gap reference. In the shown example, the reference voltage generator is a so called "double *Vbe*" band-gap reference adapted to provide a first reference voltage *Vbg* and a second band-gap reference voltage *2xVbg*, where *Vbg* is substantially equal to the silicon band-gap voltage.

[0021] The band-gap voltage reference circuit comprises first and second branches respectively including first and second groups of transistors of different emitter current conduction areas, and current sources for running the first and second groups of transistors at different emitter current densities to generate respective base-emitter voltages.

[0022] More precisely, the branches of the double *Vbe* band-gap reference comprises transistors BN5 and BN6, respectively, for instance bipolar transistors, e.g. of the N conduction type (i.e., NPN transistors). The respective base of BN5 and BN6 are coupled one to each other, and to the collector of BN6. The emitter of BN5 is coupled to the ground GND through a first resistor R1 and a second resistor R2 in series. The emitter of BN6 is coupled to the ground GND directly (namely not through R1) through the second resistor R2. A pair of cross-coupled transistors BN3 and BN4 of the same type as BN5 and BN6 (i.e., NPN), is inserted between resistors R1 and R2 one hand, and transistors BN5 and BN6 on the other hand. More precisely, transistors BN3 and BN4 are so arranged that the emitter-collector path of BN3 is inserted between the emitter of BN5 and resistor R1, and the emitter-collector path of BN4 is inserted between the emitter of BN6 and resistor R2. In addition, the base of BN3 is coupled to the collector of BN4, and vice versa.

[0023] Finally, the collector of BN5 is coupled to VDD through e.g. a MOS transistor MP4 of the P type (or PMOS), and the collector of BN6 is coupled to VDD through e.g. a PMOS transistor MP5. MP4 and MP5 have a respective transistor size (length/width) of *n* and *m*, respectively, where *m* is different from *n*. The transistors MP4 and MP5 have their respective gates coupled one to each other. The current I0 and I1 in their respective branches are thus different one form the other.

[0024] In one embodiment, the transistors may be designed so that $m>n$. Thus, it will be appreciated by the one with ordinary skills in the art that it is convenient to have a high current I0 in order to achieve higher noise rejection from the output regulated voltage Vout. On the other hand, it will become apparent from the remaining of the description that there is no need to have much current for controlling the gate of the pass device MP1, and thus current I1 can be lower. In one example *m* and *n* may be selected so that, approximately, *m* equals twice *n* ($m \cong 2n$). This allows saving current consumption in the IC.

[0025] The voltage difference between the p-n junctions of BN5 and BN4 on one hand, and BN6 (which is connected as a diode) and BN3 on the other hand, operated at different current densities, so that a base emitter voltage difference ΔVbe is generated. This generates a Proportional to Absolute Temperature (PTAT) current in resistor R1. This current is used to generate a voltage in the second resistor R2. This voltage is added to the *Vbe* voltages of the p-n junctions of transistors BN6 and BN3. Now, the voltage across a diode operated at constant current, or here with a PTAT current, is complementary to absolute temperature (Complementary to Absolute Temperature, CTAT), namely it reduces with increasing temperature. By properly choosing the ratio between the R1 and R2, the first order effects of the temperature dependency of BN6 and the PTAT current will cancel out. The resulting voltage *Vbg* at the collector of BN4 is about 1.2-1.3 V, depending on the particular technology and circuit design, and is close to the theoretical 1.22 V band-gap of silicon at a temperature of 0 K. Further, the resulting voltage at the collector of BN5 is *2xVbg.* The remaining voltage change over the operating temperature of typical integrated circuits is on the order of a few millivolts only.

Comparator stage

[0026] The band-gap reference 10 is controlled by a regulation error amplifier of the second stage 20, as will be described in more details below with reference to FIG.3.

[0027] The second stage 20, indeed, comprises a differential transistor pair operable as a voltage comparator.

[0028] The differential transistor pair comprises first and second transistors BN1 and BN2, respectively, for example bipolar transistors, e.g. of the N-conduction type (NPN transistors). The common emitters of BN1 and BN2 are coupled to the ground GND through a resistor Rdiff.

[0029] The differential pair is biased by a PTAT current *Idiff* matched with the band-gap current of the reference stage 10.

[0030] The collector of BN1 is coupled to VDD through a diode-connected transistor MP3, for instance a MOS transistor of e.g. P-conductivity type. MP3 is connected as a diode, having its base connected to its gate.

[0031] The gate of MP3 is further connected to the gate of transistors MP4 and MP5 of the first stage 10, whereby these three transistors are current-mirrored. These elements form current regulation means for the reference stage 10.

[0032] The collector of BN2 is coupled to VDD through a transistor MP2, for example a transistor of same type as MP3, namely a PMOS transistor in the shown example. In one embodiment, MP3 has the same size (length/width) *p*

as MP3. What is achieved is that the two branches of the comparator stage 20 operate under the same DC conditions, and thus the comparator is well balanced.

[0033] The comparator stage 20 receives reference voltage *Vbg* from the reference stage 10 and a feedback voltage *Vf* from the output stage 30. More precisely, voltages *Vbg* and *Vf* are provided to the base terminals of transistors BN2 and BN1 respectively, of the comparator 20.

[0034] In operation, comparator 20 provides a control signal back to the band-gap reference generator 10 through transistors BN1, MP3, MP4 and MP5, as will be further explicated below with reference to FIG.2, such that the feedback voltage *Vf* equals the first reference voltage *Vbg*, resulting in the required output voltage Vout. This control signal operates by modifying current I0 in the branch of the band-gap reference stage 10 which comprises transistor BN6.

[0035] In addition, comparator 20 provides another control signal back to the band-gap reference generator 10 through transistors BN1, MP3 and MP4, as will be further explicated below with reference to FIG.3. This control signal operates by modifying current I1 in the branch of the band-gap reference stage 10 which comprises transistor BN5.

[0036] The above element constitute a first DC regulation loop and a second DC regulation loop, respectively which provide enhanced voltage regulation, as will become more apparent from the remaining of the present description.

Output stage

[0037] The output or buffer stage is adapted to generate the regulated output voltage Vout. To that end, it comprises a pass device. In the shown example, the pass device comprises a transistor, for exempla a MOS transistor MP1 of e.g. the P conductivity type (i.e., a PMOS transistor).

[0038] The source of MP1 is coupled to VDD, for example through a direct connection, and its drain is connected to the output node 2 in order to drive current to the load.

[0039] The pass device may be coupled to a large bypass (or decoupling) capacitor Cstab, connected through the output node 2 and the ground. The value of capacitor Cstab is selected so as to provide stability of the output voltage Vout over a wide range of load current changes. In some embodiments, capacitor Cstab may be an external capacitor of, for example, a few hundreds nanofarads (nF), e.g. 100 nF.

[0040] The output stage 30 further comprises means to feed an image of the output Voltage back to the error amplifier of the comparator stage 20. In one example, such feedback is achieved by a voltage divider operable to generate the feedback voltage *Vf*. The voltage divider may comprise first and second resistors R3 and R4, respectively, arranged in series between the output node 2 and the ground GND. The node between resistors R3 and R4 is coupled to the base of transistor BN1 of the differential transistor pair of the comparator stage 20, to provide a voltage indicative of the actual output voltage Vout.

[0041] The resistance values of resistors R3 and R4 are selected so as to be sufficiently high to avoid deviating too much current from the output node 2 to the ground GND, in other to save current consumption.

[0042] The pass transistor MP1 is controlled by the reference voltage generator 10. More precisely, the gate of MP1 is coupled to the band-gap generator for receiving the second band-gap voltage *2xVbg* from the collector of transistor BN5. For example, this coupling comprises a direct connection, as shown in FIG.1.

[0043] LDO regulator is controlled by two independent feedback DC loops operating simultaneously. A first loop sets the current I0 in the band-gap reference stage 10 to provide low noise and temperature compensation. The second loop controls the pass device MP1 of an output stage 30 to provide low drop-out regulated voltage Vout at the output 2 of the circuit. The stability is ensured by a single capacitor Cstab at the output of the circuit, which may be external to the circuit.

[0044] The operation of the two above mentioned feedback DC loops will now be described in further details.

First and second DC feedback loops

[0045] With reference to the schematic circuit diagram of **FIG.2**, a first feedback DC loop 100 is adapted to set the current I0 in the band-gap reference stage 10, in order to provide low noise and temperature compensation. Loop 100 starts from the differential transistor pair BN1, BN2. Any error current flowing through the collector of BN1 is copied through mirrored transistors MP3 and MP5 with the effect that I0 is modified in order to cancel the error by modifying the band-gap voltage *Vbg* on the base of BN2. This feedback operates until the unbalance between both branches of the differential transistor pair is cancelled.

[0046] With reference now to the schematic circuit diagram of **FIG.3**, a second feedback DC loop 200 is adapted to control gate of the pass device MP1 of the output stage 30, in order to provide low drop-out regulated voltage Vout at the output 2 of the circuit. Starting from the output node 2, the loop 200 generates the image voltage Vf of the output voltage which, through transistors BN1, MP3 and MP4 is operable to cause the current I1 to increase when voltage Vout drifts.

[0047] Turning now to the circuit diagram of **FIG.4**, it will be noted that the two DC feedback loops have some path

portions in common. Indeed, they both use some part of the current regulating means comprising PMOS transistors MP3, MP4 and MP5.

[0048] However, it can be calculated that, neglecting base currents of bipolar transistors, the current I1 is independent of I0. Thus, assuming that the MOS transistor size (width/length) ratio is MP5:MP4:MP3(P2)=m:n:p, the relationship between the currents ratio and the resistor elements of the circuit is given by the following relation:

$$\frac{i_0}{i_1} = \frac{R_1 + R_2}{\frac{2p}{m} R_{diff} - R_2} \qquad (1)$$

[0049] It will be appreciated from above relation (1) that the ratio I0/I1 does not depend on *n*, the size (width/length) of transistor MP4. Thus, I1 does not vary when I0 varies as a function of temperature due to the DC feedback loop 100. Conversely, I1 can vary as a function of the current sunk by the load due to the DC feedback loop 200. In other words, the DC feedback loops are independent one from each other.

[0050] To summarize, the proposed architecture of which embodiments have been described above, is an ultra-low noise and low power LDO based on a double band-gap reference structure. This system has the capability to provide regulated output voltage down to one *Vbg.* More precisely, the controlled output voltage Vout can be tuned from almost the supply voltage VDD down to *Vbg,* i.e. approximately 1.2 V. Furthermore integrated capacitors are not needed to ensure the stability of the system (only one external capacitor at the output).

[0051] In the shown example, the circuit 1 is implemented in a submicron CMOS technology, but this is not limitative.

[0052] In the shown example, there has been described an embodiment in which the pass device and current regulating means comprise MOS transistors, for example MOSFETs. This is convenient because MOS transistors are good candidates for matching currents, as they operate as voltage controlled current sources. However, other types of transistors, in particular bipolar transistors, JFETs, etc... can be used as well.

[0053] Whilst necessary thanks to the excellent performances of the proposed circuits in terms of noise attenuation, in some embodiments one or more small integrated capacitors could be provided at the output of the LDO circuit for providing further voltage fluctuation compensation.

[0054] Finally, alternative comparator structure could also be used in replacement of the simple differential pair of the comparator stage 20 as shown.

[0055] Expressions such as "comprise", "include", "incorporate", "contain", "is" and "have" are to be construed in a non-exclusive manner when interpreting the description and its associated claims, namely construed to allow for other items or components which are not explicitly defined also to be present. Reference to the singular is also to be construed in be a reference to the plural and vice versa.

[0056] While there has been illustrated and described what are presently considered to be the preferred embodiments of the present invention, it will be understood by those skilled in the art that various other modifications may be made, and equivalents may be substituted, without departing from the true scope of the present invention. Additionally, many modifications may be made to adapt a particular situation to the teachings of the present invention without departing from the central inventive concept described herein. Furthermore, an embodiment of the present invention may not include all of the features described above. Therefore, it is intended that the present invention not be limited to the particular embodiments disclosed, but that the invention include all embodiments falling within the scope of the appended claims.

[0057] A person skilled in the art will readily appreciate that various parameters disclosed in the description may be modified and that various embodiments disclosed and/or claimed may be combined without departing from the scope of the invention.

[0058] It is stipulated that the reference signs in the claims do not limit the scope of the claims, but are merely inserted to enhance the legibility of the claims.

Claims

1. A low drop-out, LDO voltage regulating circuit comprising, arranged in parallel between a first power supply node (VDD) and a second power supply node (GND):

   - an output node (2);
   - a band-gap voltage reference stage (10) having double *Vbe* structure, adapted to provide a band-gap voltage (*Vbg*) and a double band-gap voltage (*2xVbg*); and,
   - an output stage (30) having a pass device (MP1) controlled by the double band-gap voltage and adapted to

drive current into a load connected to the output node under a regulated output voltage (Vout), and having circuitry for generating a feedback voltage (*Vf*) representative of said output voltage; and,
- a comparator stage (20) having a first input for receiving the band-gap voltage (*Vbg*) from the reference stage and a second input for receiving the feedback voltage from the output stage, and adapted to control band-gap voltage reference stage.

2. The circuit of claim 1, having, in operation, a first feedback DC loop adapted to set the current in the band-gap voltage reference stage.

3. The circuit of claim 1 or 2, having, in operation, a second feedback DC loop adapted to control the pass device of the output stage, the first and second feedback DC loops being independent one from the other and operating simultaneously.

4. The circuit of any one of claims 1 to 3, comprising a direct connection between a control terminal of the pass device of the output stage and a node of the band-gap voltage reference stage (10) providing the double band-gap voltage *(2xVbg).*

5. The circuit of any one of claims 1 to 4, being adapted to be operated with at least one bypass capacitor connected at the output of the circuit.

6. The circuit of claim 5, wherein the capacitor is external to the circuit.

7. The circuit of any one of claims 1 to 6, wherein the pass device of the output stage comprises a MOS transistor.

8. The circuit of any one of claims 1 to 7, wherein the pass device of the output stage is a transistor of P-conductivity type.

9. The circuit of anyone of claims 1 to 8, further comprising current regulating MOS transistors (MP3,MP4,MP5) arranged for regulating currents (I0,I1) in the band-gap voltage reference stage (10) with respect to currents in the comparator stage (20).

10. Integrated Circuit, IC, comprising a low drop-out, LDO, voltage regulating circuit according to any one of claims 1 to 9.

Patentansprüche

1. LDO Spannungsregulierungsschaltung mit geringem Spannungsabfall, welche parallel zwischen einem ersten Energieversorgungspunkt (VDD) und einem zweiten Energieversorgungspunkt (GND) angeordnet ist, aufweisend:

- einen Ausgabepunkt (2);
- eine Bandabstandsreferenzspannungsstufe (10), welche eine doppelte Vbe-Struktur hat, und eingerichtet ist, eine Bandabstandsspannung (Vbg) und eine doppelte Bandabstandsspannung (2xVbg) zu liefern; und
- eine Ausgabestufe (30), welche eine Durchlichteinrichtung (MP1) hat, welche durch die doppelte Bandabstandsspannung geregelt ist und eingerichtet ist, um Strom mit einer regulierten Ausgabespannung (Vout) in eine Last, welche mit dem Ausgabepunkt verbunden ist, zu leiten und mit einer Schaltung zum Erzeugen einer Feedbackspannung (Vf), welche repräsentativ für die Ausgabespannung ist; und
- eine Vergleichsstufe (20) mit einem ersten Eingang zum Erhalten der Bandabstandsspannung (Vbg) von der Referenzstufe und einem zweiten Eingang zum Erhalten der Feedbackspannung von der Ausgabestufe und welche eingerichtet ist, die Bandabstandsspannungsreferenzstufe zu regeln.

2. Schaltung nach Anspruch 1,
mit einem ersten Gleichstromfeedbackkreis im Betriebszustand, welcher eingerichtet ist, den Strom in der Bandabstandsspannungsreferenzstufe zu bestimmen.

3. Schaltung nach Anspruch 1 oder 2,
mit einem zweiten Gleichstromfeedbackkreis im Betriebszustand, welcher eingerichtet ist, die Durchleiteinrichtung der Ausgabestufe zu regeln, wobei der erste und der zweite Gleichstromfeedbackloop unabhängig voneinander sind und gleichzeitig arbeiten.

4. Schaltung nach einem der Ansprüche 1 bis 3,
aufweisend eine direkte Verbindung zwischen einem Regelanschluss, der Durchleiteinrichtung der Ausgabestufe und einem Punkt der Bandabstandsreferenzspannungsstufe (10), welcher die doppelte Bandabstandsspannung (2xVbg) liefert.

5. Schaltung nach einem der Ansprüche 1 bis 4,
eingerichtet, um mit mindestens einem Bypasskondensator, welcher mit der Ausgabe der Schaltung verbunden ist, betrieben zu werden.

6. Schaltung nach Anspruch 5,
wobei der Kondensator außerhalb der Schaltung ist.

7. Schaltung nach einem der Ansprüche 1 bis 6,
wobei die Durchgleiteinrichtung der Ausgabestufe einen MOS-Transistor aufweist.

8. Schaltung nach einem der Ansprüche 1 bis 7,
wobei die Durchlasseinrichtung der Ausgabestufe ein Transistor vom P-Leitfähigkeitstyp ist.

9. Schaltung nach einem der Ansprüche 1 bis 8,
des Weiteren aufweisend stromregulierende MOS-Transistoren (MP3, MP4, MP5), eingerichtet zum Regeln des Stroms (10, I1) in der Bandabstandsspannungsreferenzstufe (10) bezüglich des Stroms in der Vergleichsstufe (20).

10. Integrierte Schaltung, IC, aufweisend eine LDO spannungsregulierende Schaltung nach einem der Ansprüche 1 bis 9 mit geringem Spannungsabfall.

Revendications

1. Circuit de régulation de tension à faible chute de tension, LDO, comprenant, disposés en parallèle entre un premier noeud d'alimentation (VDD) et un deuxième noeud d'alimentation (GND) :

   - un noeud de sortie (2) ;
   - un étage de référence de tension de bande interdite (10) comportant une structure *Vbe* double, apte à fournir une tension de bande interdite (*Vbg*) et une tension de bande interdite double (2 x *Vbg*) ; et
   - un étage de sortie (30) comportant un dispositif passant (MP1) commandé par la tension de bande interdite double et apte à piloter le courant dans une charge connectée au noeud de sortie (2) sous une tension de sortie régulée (Vout), et comportant des circuits pour générer une tension de rétroaction (*Vf*) représentative de ladite tension de sortie ; et
   - un étage comparateur (20) comportant une première entrée pour recevoir la tension de bande interdite (*Vbg*) en provenance de l'étage de référence et une deuxième entrée pour recevoir la tension de rétroaction en provenance de l'étage de sortie, et apte à commander l'étage de référence de tension de bande interdite.

2. Circuit de la revendication 1, comportant, en fonctionnement, une première boucle de rétroaction à courant continu apte à établir le courant dans l'étage de référence de tension de bande interdite.

3. Circuit de la revendication 1 ou 2, comportant, en fonctionnement, une deuxième boucle de rétroaction à courant continu apte à commander le dispositif passant de l'étage de sortie, les première et deuxième boucles de rétroaction à courant continu étant indépendantes l'une de l'autre et fonctionnant simultanément.

4. Circuit de l'une quelconque des revendications 1 à 3, comprenant une connexion directe entre une borne de commande du dispositif passant de l'étage de sortie et un noeud de l'étage de référence de tension de bande interdite (10) fournissant la tension de bande interdite double (2 x *Vbg*).

5. Circuit de l'une quelconque des revendications 1 à 4, qui est apte à être mis en fonctionnement avec au moins un condensateur de dérivation connecté à la sortie du circuit.

6. Circuit de la revendication 5, dans lequel le condensateur est externe au circuit.

7. Circuit de l'une quelconque des revendications 1 à 6, dans lequel le dispositif passant de l'étage de sortie comprend un transistor MOS.

8. Circuit de l'une quelconque des revendications 1 à 7, dans lequel le dispositif passant de l'étage de sortie est un transistor avec une conductivité de type P.

9. Circuit de l'une quelconque des revendications 1 à 8, comprenant en outre des transistors MOS de régulation de courant (MP3, MP4, MP5) organisés pour réguler des courants (10, I1) dans l'étage de référence de tension de bande interdite (10) par rapport aux courants dans l'étage comparateur (20).

10. Circuit Intégré, IC, comprenant un circuit de régulation de tension à faible chute de tension, LDO, selon l'une quelconque des revendications 1 à 9.

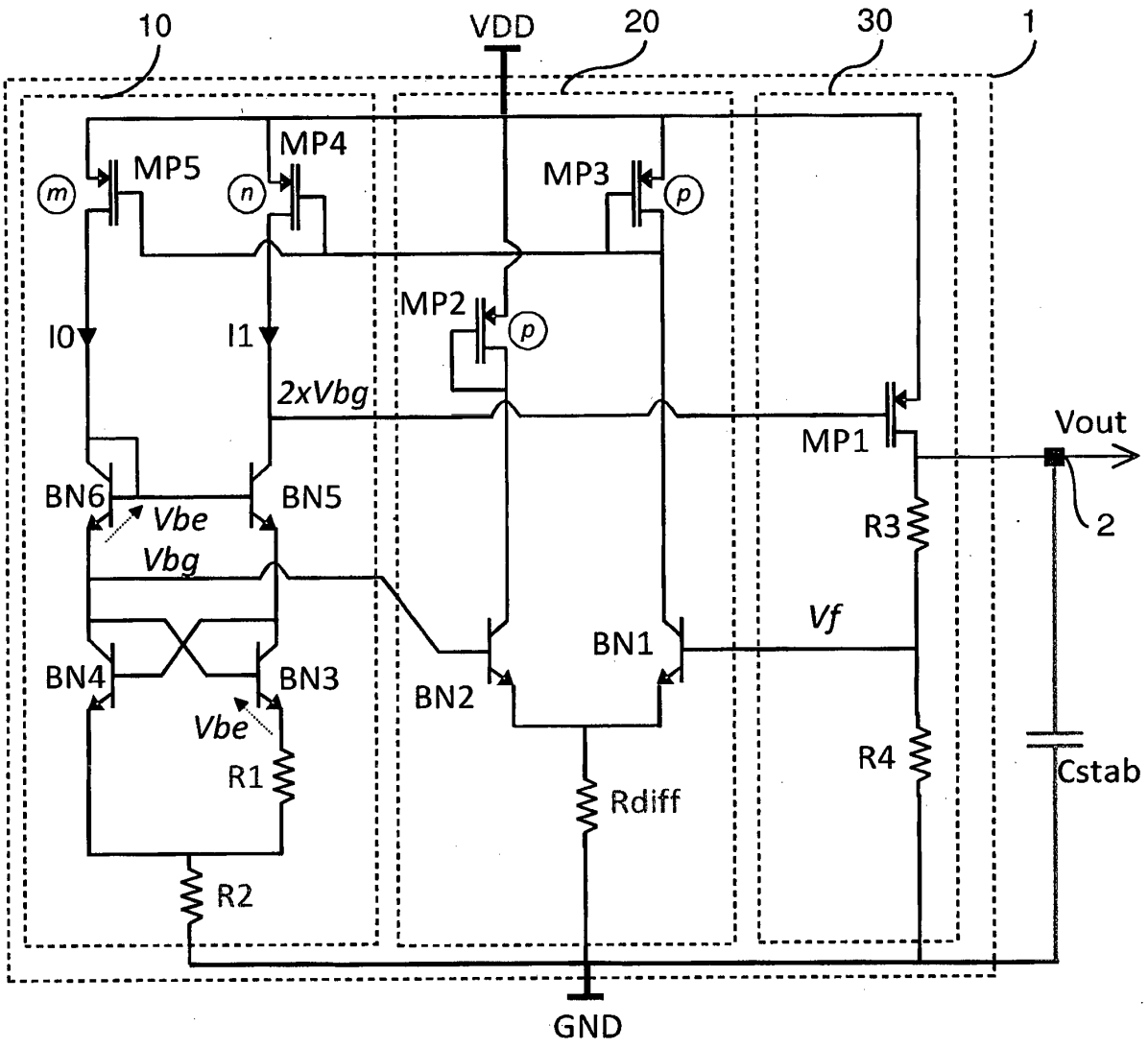
10
VDD
20
30
1
MP5
MP4
MP3
m
n
p
MP2
I0
I1
2xVbg
MP1
Vout
BN6
BN5
Vbe
Vbg
R3
2
Vf
BN1
BN4
BN3
BN2
Vbe
R1
R4
Cstab
Rdiff
R2
GND

FIG.1

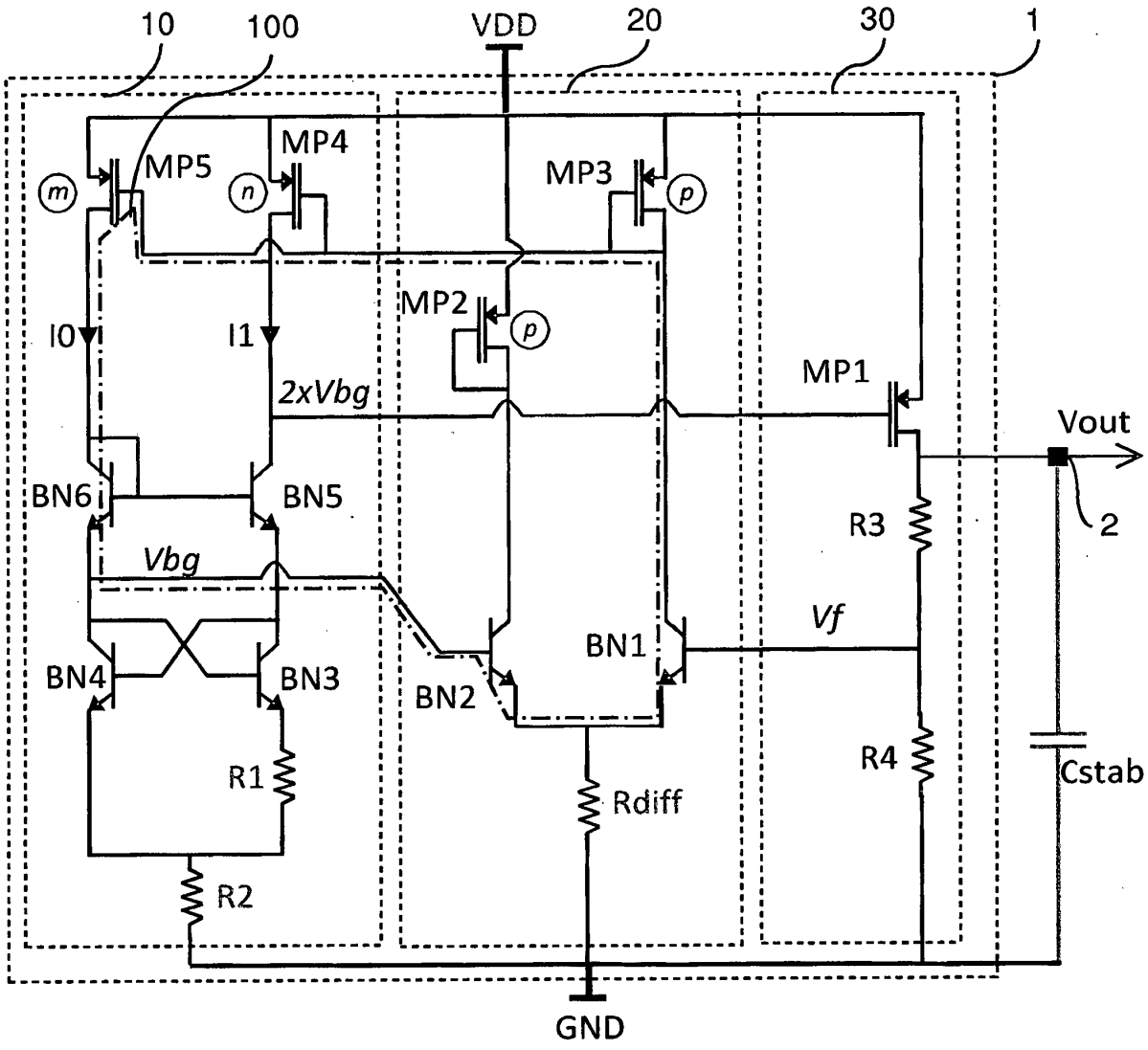
10
100
VDD
20
30
1
MP5
MP4
MP3
MP2
MP1
m
n
p
p
I0
I1
2xVbg
Vout
BN6
BN5
R3
2
Vbg
Vf
BN1
BN4
BN3
BN2
R1
Rdiff
R4
Cstab
R2
GND

FIG.2

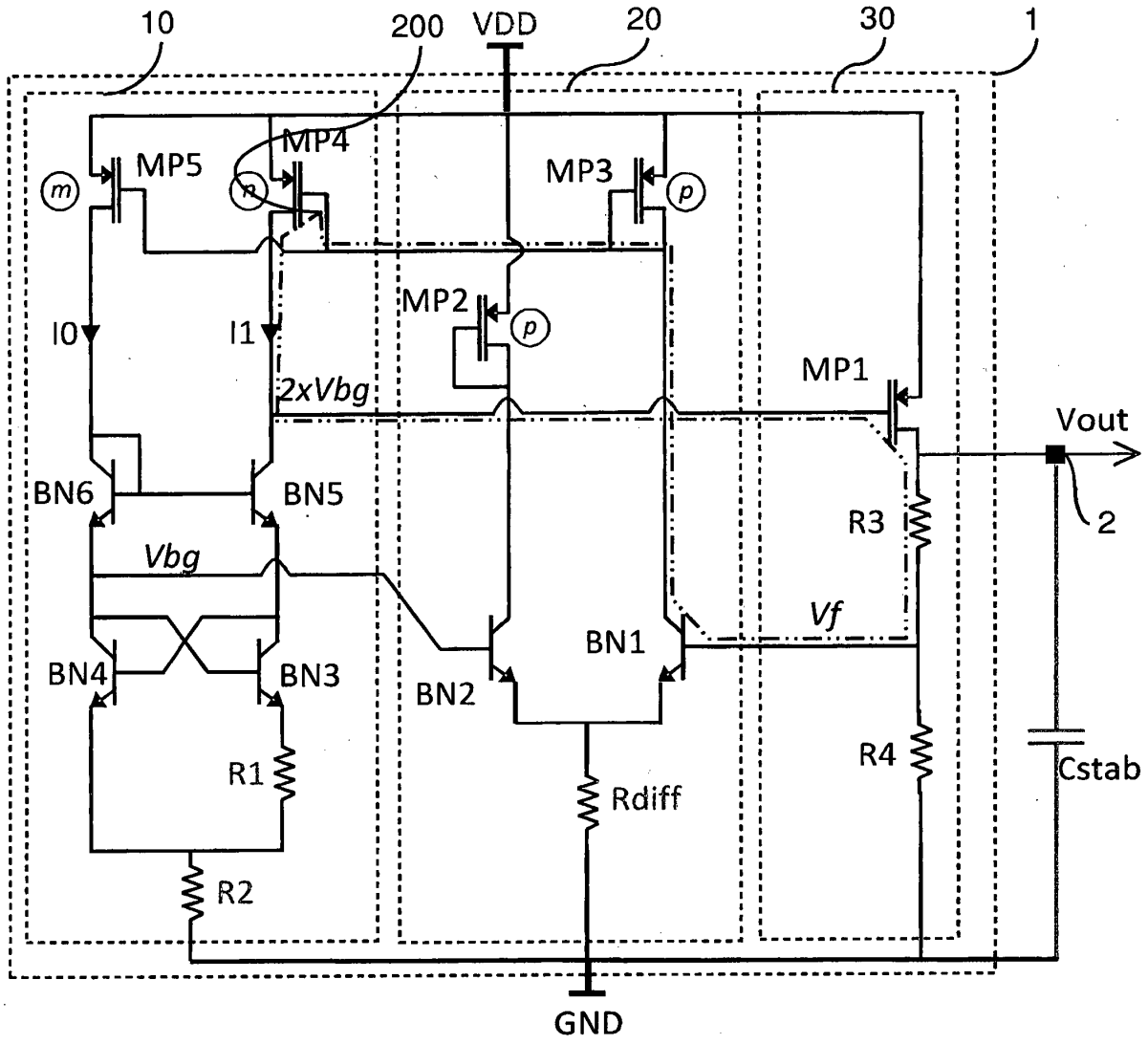
10
200
VDD
20
30
1
MP5
MP4
MP3
MP2
MP1
m
n
p
p
p
I0
I1
2xVbg
Vout
BN6
BN5
R3
2
Vbg
Vf
BN4
BN3
BN2
BN1
R4
Cstab
R1
Rdiff
R2
GND

FIG.3

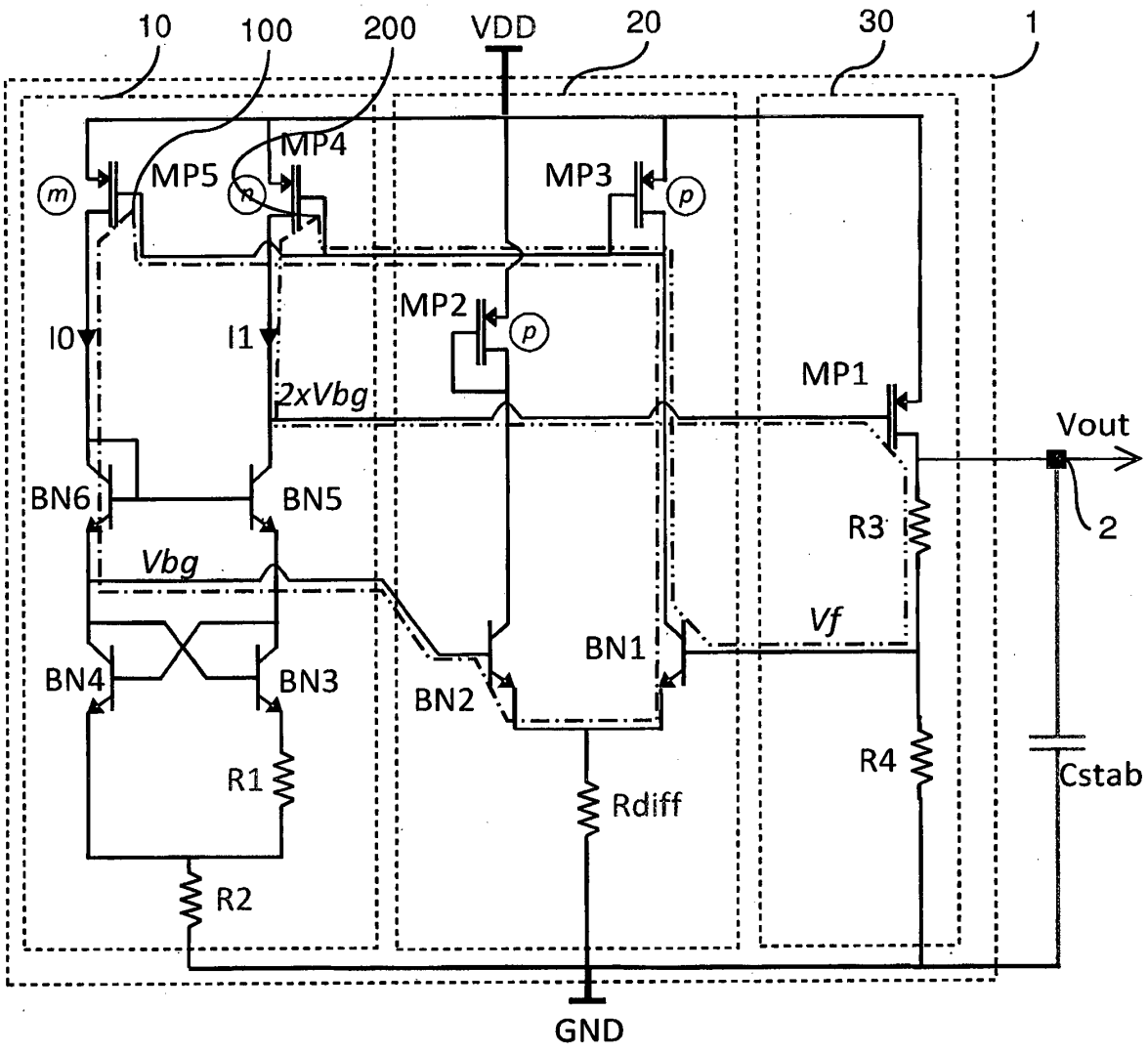
10
100
200
VDD
20
30
1
MP5
MP4
MP3
MP2
MP1
m
n
p
p
p
I0
I1
2xVbg
Vout
2
BN6
BN5
R3
Vbg
Vf
BN1
BN4
BN3
BN2
R1
R4
Cstab
Rdiff
R2
GND

FIG.4

REFERENCES CITED IN THE DESCRIPTION

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