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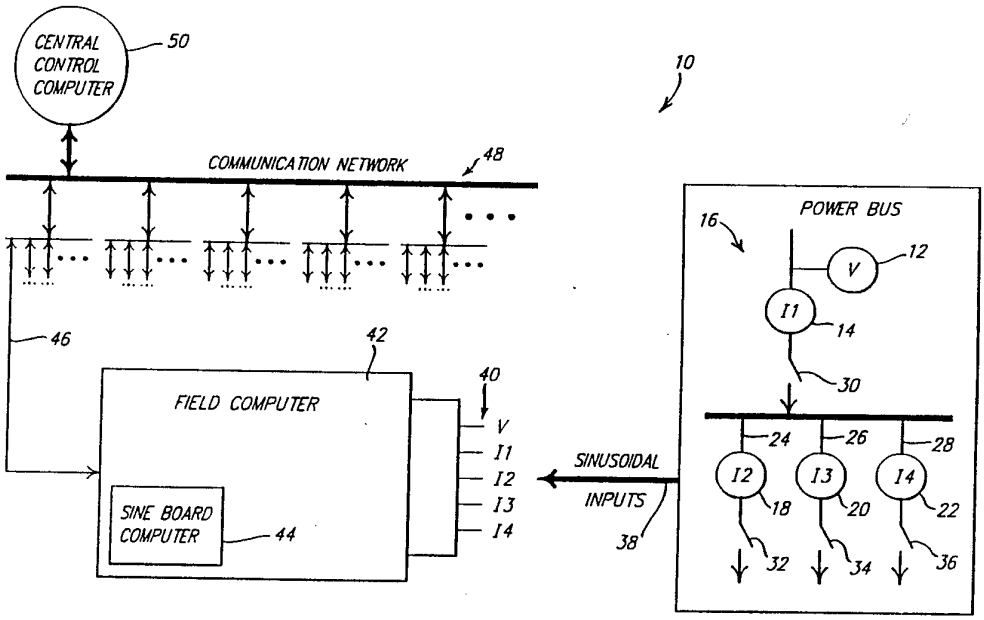

(57) Abstract

A method and apparatus for rapidly and continuously sampling AC voltage and current signals in a plurality of power distribution circuits. The sampled signals are then analyzed in a sine board computer to derive the number of fundamental electrical variables. These variables include frequency, RMS volts, RMS amps and a phase angular relationship between the voltage and currents in the system. The computer also performs calibration and compensation functions. From these fundamental variables, other useful parameters can be calculated such as watts, watt-hours, VARS, and power factor.

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HIGH SPEED POWER ANALYZER

BACKGROUND AND SUMMARY OF THE INVENTION

The present invention relates generally to systems for monitoring electrical power circuits and particularly to a programmable system for measuring and calculating electrical parameters from multiple power circuits.

The monitoring of electrical power is important to ensure that this energy resource is effectively generated, distributed and utilized. Utilities need to measure power coming out of a generation station or going into a power station. In addition, to minimize power transmission losses, it is important to minimize the phase relationship between the current and voltage waveforms of the power being transmitted. In industrial control applications, it is important to be able to continuously monitor the current and phase of the power into a machine which may vary with the machine load.

Traditional systems for monitoring power circuits require the installation of individual measuring devices to measure a specific power system parameter; for example, Watts, Vars, Amps, or Volts. These devices typically comprise discrete analog transducers which convert AC voltage and current signals from a power system into DC output signals proportional to the true power on the system. For example, typical utility revenue kilowatt hour meters measure power in an analog fashion. Where a data acquisition system must measure numerous circuits, requiring separate measuring devices for each circuit can

add greatly to the overall cost of the system. Also, where a number of circuits are being remotely monitored for computer processing and display, the individual devices must be connected to a data acquisition device and suitably processed to interface with the computer. Further, multiple measuring devices greatly increase the overall error of the system.

Accordingly, it is a principle objective of the present invention to provide a simplified system for measuring various parameters in multiple power circuits to reduce the cost of purchasing, installing and maintaining the system.

More specifically, it is an objective of the present invention to provide a system in which a single measuring device measures the fundamental parameters in a power system so that subsequent derived parameters can be computed in a controller data processing computer, thereby eliminating the necessity of multiple measuring devices.

It is another objective of the present invention to provide a power analyzer which reduces the cost of maintenance of the overall system.

It is an additional objective of the present invention to provide a power analyzer which has very high precision through self calibration and a non-synchronous measurement technique.

It is still another objective of the present invention to provide a microprocessor controlled power analyzer that can continuously and rapidly monitor a plurality of circuits.

To achieve these foregoing objectives, the present invention provides a high speed power analyzer which utilizes voltage and current input devices, such as transformers, for transmitting signals proportional to the voltage and current levels in the circuits being measured. The signals are transmitted to a multiplexer and the output of the multiplexer is coupled to an analog to digital (A to D) converter for converting the voltage and current signals

into a digital representation of same. A digital processor circuit is coupled to the multiplexer for selecting which inputs are coupled to the multiplexer outputs. The processor circuit also is coupled to the A to D converter to receive the digital voltage and current signals. The processor circuit continuously samples and stores the voltage and current signals at regular intervals of time and also calculates and stores a plurality of electrical variables related to the power used by the circuits. For example, these electrical variables may include frequency, RMS volts, RMS amps, and the phase angular relationship between the voltage and the currents in the system.

In one form of the present invention, the system includes a host computer coupled to the digital processor circuit for performing additional calculations on the electrical variables to thereby derive electrical parameters relating to the performance of the power circuits. These parameters may include Watts, Watt-hours, Vars, Power Factor, etc.

Another feature of the present invention, is that the software of the processor circuit performs continuous functions such as calibration, drift and offset compensation and zero cross detection. In addition, the system samples the input devices rapidly and continuously in a manner which is not synchronized to the power waveforms being sampled. Specifically, in one form of the present invention, the system samples five channels at a rate of 1199 times each second.

Additional advantages and features of the present invention will become apparent from a reading of the detailed description of the preferred embodiment which makes reference to the following set of drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a diagram of the overall power analyzer system in accordance with the present invention.

Figure 2 is a block diagram of the major components of the sine board computer shown in Figure 1.

Figure 3A-3B provide an illustration of representative sine waves showing the measurement techniques in accordance with the present invention.

Figures 4A-4E comprise flowcharts for the processing performed by the sine board computer in accordance with the present invention.

Figures 5A-5D comprise flowcharts the processing of the host computer in accordance with the present invention.

Figures 6A-6F comprise schematic diagrams for the circuits contained in the sine board computer shown in Figure 1.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring to Figure 1, a block diagram of a high speed power analyzer system 10 according to the present invention is shown. The power analyzer system 10 utilizes a voltage transformer 12 and a current transformer 14 for sensing voltage and current at the input of a power bus 16 at one phase of a power substation. It will be appreciated that in general there will be three phases in each power substation, however, for simplicity only one phase is shown. Additional current transformers 18, 20 and 22 sense the current flowing through circuits 24, 26 and 28 respectively which each lead to final load devices (not shown). Conventional circuit breakers 30, 32, 34 and 36 are employed for circuit protection. Sinusoidally varying signals from the potential transformer 12 and the current transformers 14, 18, 20 and 22, are transmitted along the input bus 38 to the five input channels 40 of a field or host computer 42. The host computer 42 comprises generally a host processor which communicates with at least one sine board computer 44 and other input/output devices.

It will be appreciated that a passive resistor divider circuit (not shown) is preferably connected to the

potential transformer 12. Thus, the signal reaching the field computer 42 is a reduced signal proportional to the bus 16 voltage. That is, V sensed = K X V bus; where K is proportional to the resistance of the resistor divider circuit. In addition, a shunt resistor (not shown) is installed with the current transformers 14, 18, 20, 22. The shunt is selected to develop 0.707 VRMS at a 6 Amps current transformer loop current. Again, the voltage measured across the shunt resistor is proportional to the current flowing in the current transformer loop. That is, V sensed = K2 X V shunt; where K2 is proportional to the resistance of the shunt resistor. Also, V shunt = R shunt X I current transformer loop.

In general, the sine board computer 44 samples the voltage input and each current input to compute the RMS voltage and RMS currents. Next, the sine board computer 44 measures the phase relationship between the voltage and each of the currents. The sine board computer 44 samples each input channel 1199 times each second and determines all zero crossing points for each input signal. The precise time base of a microprocessor in the sine board computer 44 is used to measure the time difference between zero crossings to calculate the phase relationships. This information is then transmitted to the field computer 42 where it is transmitted along bus 46 to a communication network 48 that is coupled to a central control computer 50. Referring now to Figure 2, the sine board computer 44 is shown in more detail. The potential transformer 12 and one of the current transformers 14 is depicted, each having plus and minus inputs 52 and 54 entering the sine board computer 44 where they are coupled to a multiplex device 56. While only one current transformer 44 is shown in Figure 2 for simplicity, it will be appreciated that the other current transformers 18, 20 and 22 are likewise connected to the multiplexer 56 inputs. Multiplexer 56 may comprise, for example, a type 507A multiplex circuit manufactured by Harris Corp.

A microprocessor 58, such as an 80C31, manufactured by Intel Corp., with its associated circuitry is coupled to the multiplexer 56 along line 60 for permitting the microprocessor 58 to select which of the inputs to the multiplexer 56 are directed to the multiplexer output lines 62 and 64. Under control of the microprocessor 58, the signal from either the potential transformer 12 or any of the current transformers 14, 18, 20 and 22 may be directed to the multiplex output lines 62 and 64. The multiplex output 62, 64 is directed to a differential amplifier circuit 66 which takes the difference between the multiplex outputs 62 and 64, amplifies this difference signal by ten and transmits it along output line 68. An A to D converter 70, which may be, for example, an AD578 manufactured by Analog Devices Inc., accepts the amplified difference signal along line 68 as its input and converts this sinusoidally varying analog signal to a 12 bit digital signal. The digitized 12 bit signal is then transmitted along bus 72 to the microprocessor 58. The microprocessor 58 is also connected to the A to D converter 70 through its associated circuitry 74 (shown in Fig. 6D), which provides a command to convert (CTC) line 76 which is used to initiate the conversion sequence after settling.

Referring now to Figures 4A-4E, the primary software processing steps of the sine board 44 are depicted. Figure 4A is a flowchart of the sine board 44 main loop as performed by the microprocessor 58. In particular, sine board main loop 78 initially resets and reconfigures the hardware as required in step 80. In addition, in step 80 the microprocessor 58 will read/write test all memory. Finally, in step 80 the data read interrupt is enabled. The data read interrupt is the means by which the microprocessor 58 samples data from the potential transformer 12 and current transformers 14, 18, 20 and 22. This sampling occurs 1199 times per second (i.e., at fixed 834 microsecond intervals) for each of the

five input channels 40. That is, the data read interrupt takes a total of 1199 X 5 samples per second. Further details of the data read interrupt will be discussed below in connection with Figure 4B. The sine board process 78 also determines whether there has been a host data request in decision diamond 82. In other words, between interrupts the processor checks to see if the host computer 42 has requested a data update. Such requests will generally occur once per second and are described in more detail below in connection with Figure 5A.

If there is a host data request, the processor proceeds to step 84 where the data in a transmit buffer is sent to the host 42. Also a "calibration read" flag is set. The process then proceeds along line 86 back to decision diamond 82. If there is no host data request, the process then proceeds to decision diamond 88 where it is determined whether there is data to be processed. Thus, when an interrupt has been performed and data has been read, there will be data from one or more samples to be processed, in which case the data process sub-routine 90 will process the data read during the interrupt. The data processing sub-routine will be described below in connection with 4C. If decision diamond 88 determines that there is no data to be processed, the process proceeds along line 86 back to decision diamond 82. It will be appreciated that the data processing sub-routine 90 will be performed once per data read interrupt.

Referring now to Figure 4B, a flowchart of the data read interrupt 92 is shown. Initially in step 94, the next interrupt is scheduled for t + 834 microseconds, where t is the current time, to maintain the accuracy needed for precise phase measurements. It should be noted that this frequency yields a sample rate that is not a multiple of 60 hertz (i.e., 1199 samples/sec. as opposed to 1200 samples/sec.). Where the sinusoidal inputs to be measured are 60 hertz, it is an advantage of the present invention to sample at a different frequency rate. This is because

if the sample rate was synchronous with the power waveform, the same points along the waveform would be measured from cycle to cycle. Consequently, spikes in the signal would be measured each time. In accordance with the present invention, the non-synchronous sampling rate causes the sampling to move across the wave form from cycle to cycle so that artifacts, such as spikes, are not measured each time. Step 94 then sets a "data to be processed" flag. This flag is then detected after the interrupt is complete, in decision diamond 88, shown in Figure 4A. Next, step 96 will read and store the data presently in channels 1-5 40. This data may be stored in a raw read buffer in the associated memory of microprocessor 58, where it will be available for the data process routine 90. In this regard, it should be noted that data for a full cycle is stored (i.e., no data is thrown away) in this buffer. After a full cycle of data has been accumulated, it is sent to another buffer of the memory to permit averaging with a larger set of data. As discussed above, this data will be transmitted to the microprocessor 58 along bus 72 from the A to D converter 70. Next, the process determines if the "calibration read" flag has been set. That is, in step 84 shown in Figure 4A the calibration read flag will be set after each host data request (e.g., once/second). If the calibration read flag is not set, decision diamond 98 proceeds back to the interrupt return 100 which directs the processing back to step 82 in Figure 4A. If the calibration read flag has been set, step 102 is performed to clear the calibration read flag, read/store the precision voltage reference, and read/store the ground reference. In particular, the voltage reference signal on line 208 and the ground reference signal on line 209 are provided to the multiplexer 56 as shown in Figure 6A in order to provide the data necessary for compensation/calibration of the multiplexer 56 and amplifier 66 due to environmental changes. The voltage and ground reference data are used during the data processing

sub-routine 90 to be discussed presently. The process then returns to the main loop 78.

Referring now to Figure 4C the data processing sub-routine 90 for one of the five channels begins with step 104, which initially indexes a data number by an increment of one over the previous data point that was read in the previous interrupt. Next, step 104 takes the absolute value of the data. Then, the DC offset (value of ground reference) is subtracted from the absolute value of each data point. This value is then added to the RMS sum. The RMS sum will be used to calculate average RMS, as discussed below in connection with Figure 5B. Next, the process proceeds to the "detect" zero cross sub-routine 106, discussed below in connection with 4D. If a zero cross is not detected in sub-routine 106, decision diamond 108 will return along line 110 to the sine board main loop line 86 shown in Figure 4A. If, on the other hand, decision diamond 108 determines that a zero cross has been detected, step 112 will index a number of waves of data associated with that sine wave by one, and proceed to the "calculate zero cross" sub-routine 114, shown in Figure 4E. The number of the wave will be used in the frequency calculation, discussed below in connection with Figure 5C. It should be noted that step 112 also updates the transmit sum buffer with the addition of another wave number, and the wave buffer is reset to zero. This is because the sine board computer 44 only sends completed wave information to the field computer 42. The sine board computer holds the data for incomplete waves until the next time data is requested by the field computer 42.

Decision diamond 116 next determines if the present channel is a voltage channel by the fact that it is the number one channel used in this application. If it is, step 118 calculates a period summation equal to the previous period sum plus the zero cross time difference (Diff.). "Diff" is calculated in the "calculate zero cross" sub-routine 114, as the time of the current zero

cross, minus the time of the previous zero cross point. If decision diamond 116 determines that the present channel is not a voltage channel, then step 120 is performed which adds the "Diff" value to the phase angle PHI. The phase angle PHI is equal to the time between the zero cross of the current and the zero cross of the most recent voltage signal. After step 120, the data processing sub-routine 90 proceeds back to the sine board main loop 78.

The detect zero cross sub-routine 106 is described in more detail on Figure 4D. Initially, step 122 gets the present data's sign and the present channel's status. In general, the detect zero cross sub-routine 106 waits for a case when two positive data points have followed two negative data points. This condition will set the "cross detected" flag. In more detail, step 124 determines if the present data is positive. If it is, the number of negative data values ("Num Neg") is set to zero in step 126. If the data is negative, step 128 will set the number of positive data points ("Num Pos") to zero. Next, decision diamond 130 checks to see if the "got 2 neg" flag is set. This will have occurred through a previous iteration through the steps to be described below. If the "got 2 neg" flag is not set, step 132 will index the number of negative points ("Num Neg") by one, and step 134 will determine if the number of negative points is equal to two. If it is, step 136 will set the "got 2 neg" flag, and the detect zero cross sub-routine will return to the data processing routine 90 described or shown on Figure 4C. Likewise, if step 130 determines that the "got 2 neg" flag was set, or if step 134 determines that the number of negative data points was not equal to 2, the process would return back to the data processing sub-routine 90.

Where the decision diamond 124 determines that the data was positive, after step 126 sets the num neg to zero, decision diamond 138 will determine if the "got 2 neg" flag has been set by a previous iteration of step 136. If not, the process returns to the data processing sub-

routine 90. If it has been set, step 140 will index the number of positive data points by one and step 142 will determine if this number is two. If it is not, step 142 will direct the process back to the data processing sub-routine 90. If the number is two, on the other hand step 144 will set the "cross detected" flag indicating that two positive data points have followed two negative data points.

The calculate zero cross sub-routine 114 is shown on Figure 4E. In general, this sub-routine uses a straight line approximation Y = Mx + B between the pair of data points that straddle the zero line to approximate the cross over point for the sine wave. This process is illustrated in Figure 3A where the sine wave 146 is shown divided up by vertical lines intersecting the sine wave 146 at data points 148 which are taken every 834 micro seconds. The zero cross point is found as shown in Figure 3B by drawing a straight line 150 between a pair of data points that straddle the zero line. The point at which line 150 crosses the zero line 152 is the approximate zero cross point. While Figure 3B illustrates zero crossing detection on the positive to negative transition, it will be apparent from the description below that the detection may also take place in the negative to positive transition.

Referring again to Figure 4E, the calculate zero cross sub-routine 114 begins with step 154 to initially find the straddling data points; that is, the negative voltage and the positive voltage on either side of the zero crossing point. This may be, for example, point 156 and 158 shown on Figure 3B. Next, step 154 determines the time of the negative and positive points shown at 160 and 162, respectively, on Figure 3B. Next, step 154 gets the known time difference between point 162 and 160, or delta t. Next, in step 163 the voltage of the negative point 158 is divided by the voltage of the negative point plus the voltage of the positive point 156 to calculate the slope. The zero cross is then set to be equal to the time of the

negative point 162 plus the zero point crossing time plus a percentage of the delta t that has occurred. Next, step 163 calculates the difference between the zero cross just calculated and the previous voltage zero cross. The calculate zero cross sub-routine then proceeds back to the data process sub-routine 90 where the difference (Diff) is used in subsequent steps 118 and 120.

The data finishing functions are performed by the field computer 42. A flowchart of the data finishing process 164 is shown in Figure 5A. Initially, in step 166 the host processor requests and receives the data received and processed in the steps discussed above in connection with Figures 4A-4e from the sine board computer 44. Step 166 is preferably performed once per second, and corresponds to a host data request step 82 in Figure 4A. Next, an RMS calibration and calculation sub-routine 168 is performed. Then, a frequency calculation sub-routine 170 and a phase angle compensation calculation sub-routine 172 have performed. Finally, step 174 stores the RMS, frequency and phase angle data.

In more detail, the RMS calibration and calculation sub-routine 168 for each of the five channels is shown on Figure 5B. In general the RMS calibration and calculation sub-routine 168 calibrates the RMS sum by multiplication with a gain calibration ratio, which is a calibration for any analog/gain error associated with the multiplexer and amplifier circuits. If the analog/gain error is more than 10 percent, then a calibration error is reported by the host computer 42 and the sine board computer 44 waits for a reset signal from the host computer 42 to continue operations. Thus, in this embodiment, the host computer 42 is programmed to see whether the reference voltage signal being read is within plus or minus 10 percent of its known value. If the reference voltage is within tolerance, then the RMS answers are adjusted to compensate for the error characterized by the calibration ratio in step 176. In particular, step 176 first

determines the calibration ratio as the voltage reference divided by the voltage reference read minus the ground reference read. Next, step 176 multiplies the calibration ratio by the RMS sum which was determined above in step 104 for each of the voltage and current signals being sampled. This yields the calibrated RMS sum. Next, step 178 calculates an RMS constant which is pi divided by the square root of 8 and the calibrated average RMS is then determined by multiplying the calibrated sum by the RMS constant divided by the total number of samples. Sub-routine 168 then returns to the host data finishing process 164 which proceeds to the frequency calculation sub-routine 170 shown on Figure 5C.

The frequency calculation sub-routine 170 calculates the average frequency by inverting the period sum divided by the total number of voltage waves received. That is, step 180 divides the total number of waves received by the period sum to determine the frequency. It will be appreciated that the period sum was determined in step 118 in the flowchart on Figure 4C and the number of waves was determined in step 112 on Figure 4C. Next, the frequency calculation sub-routine 170 proceeds back to the data finishing process 164 which directs the process to the phase angle compensation and calculation sub-routine 172 shown on Figure 5D for each of the four current channels. This sub-routine is used to convert the time domain phase information received from the sine board computer 44 into phase angle degrees. In this regard, the sub-routine calculates a compensated PHI sum by addition with the time between channel reads constant. This provides compensation for the fact that the channels are sampled at deterministically different times. In particular, step 182 defines the channel diff constant as the time between the channel two read minus the time between the channel one read. Next, step 184 calculates the PHI sum as the PHI sum (calculated in step 120) plus the channel diff constant times j where j is defined as the channel number minus one.

Thus, it should be appreciated that j indexes from one to four as the program advances through the current signal channels. Next, step 184 calculates the PHI divisor as the period sum (found in step 118) multiplied by the number of waves divided by k, where k is proportional to the full scale of the A to D converter and the full scale of finished values of the parameters being monitored. The period is needed at this juncture, because the invention may be employed with power systems using different frequencies (e.g., 50 or 60 hertz). Next, step 186 determines the average phase angle as the compensated PHI sum divided by the PHI divisor. Sub-routine 172 then proceeds back to the host data finishing process and the RMS, frequency and phi data are stored in step 174. These stored parameters are then available to a central control computer 50, shown in Figure 1, by means of bus 46, in communication with the communication network 48. It will be appreciated that from these fundamental parameters (RMS volts/amps frequency and phase data) the central control computer 50 can derive useful system parameters such as watts, watt-hours, VARS, power factor, etc.

Referring now to Figures 6A-6F, a schematic view of a preferred embodiment of the sine board computer 44 is shown. The channel one inputs 188 and 190 comprise the negative and positive inputs from the potential transformer 12 respectively. Likewise the channel 2, 3, 4 and 5 inputs comprise the negative 191, 194, 198, 202, and positive 192, 196, 198, 200, 204 inputs from the four current transformers 14, 18, 20 and 22. Each input channel includes a pair of resistors 203 and 205 and a capacitor 206 which together serve to filter out noise and resist surges of the incoming analog input signals. The channel 1-5 inputs are fed to the input lines in the multiplex device 56, which is provided with a .909 voltage reference 208, plus and minus 15 volt supply 210 and 212, respectively, while the ground pin as well as pins 6a, 7a, 8a, 6b, 7b, 8b are grounded. Address lines 60 as well as

mux enable line 214 are supplied from latch 216 shown on Figure 6D. Latch 216 may be a 74HC374, which is coupled to the micro processor 58 shown on Figure 6C for controlling the multiplex device 56. The multiplex device 56 provides two outputs 218 and 220, comprising the plus and minus signals respectively. Output signals 218 and 220 are fed to a differential amplifier circuit 66. It will be appreciated that differential amplifier circuit 66 takes a difference between the voltages on lines 218 and 220, amplifies this difference by ten, and transmits this amplified difference as a single sinusoidally varying voltage level to line 68 which is then fed to the A to D converter 70 input. The 12 bit digital output of A to D converter 70 is transmitted along bus 72 to the microprocessor 58 inputs. The microprocessor circuit controls the A to D converter by means of the CTC line 76 shown in Figure 6A and 6D. Figure 6B shows the memory and I/O controller PLD which decodes and provides strobe signals as well as memory circuits 222, 224, 226 used for program memory. Figure 6C illustrates the memory address latch 226 and Figure 6D shows the memory and I/O controller 228 for controlling interaction between the microprocessor 58 and the program memory as well as A to D converter by means of the CTC command signal. Figure 6B shows the power supply 230. Figure 6E shows a diagnostic light emitting diode 232 which is tied to the reset line driven by the field computer to indicate whether the sine board computer 44 is functioning properly. Figure 6F shows the connector 254 for transmitting data to the field computer 42. It will be appreciated that the high speed power analyzer system 10 described above provides a rapid measurement of power circuit parameters that is independent of frequency and voltage. It also provides uninterrupted continuous sampling of five input channels at 1199 hertz at each channel and automatically performs calibration, and compensation continuously.

The various embodiments which have been set forth above were for the purpose of illustration and were not intended to limit the invention. It will be appreciated by those skilled in the art that various changes and modifications may be made to these embodiments described in this specification without departing from the spirit and scope of the invention as defined by the appended claims.

CLAIMS

1. A high speed power analyzer for measuring electrical parameters in an alternating waveform power system, comprising:

input means for receiving a plurality of analog input signals which represent electrical parameters of the power system, where at least one of said analog input signals represents a voltage signal and another of said analog input signals represents a current signal;

multiplexer means connected to said input means for sampling each of said analog input signals by individually transmitting selected ones of said analog input signals;

converter means, connected to said multiplexer means, for converting sampled analog input signals received from said multiplexer means into a digital representation of said analog input signals; and

processor circuit means, coupled to said multiplexer means and said converter means, for controlling the sampling of said analog input signals by said multiplexer means in accordance with a predetermined sampling schedule which is nonsynchronous with the waveform of said power system, and for processing said digital representations of said analog input signals received from said converter means to produce a plurality of output signals which are indicative of predetermined electrical variables related to the power being used in said power system.

2. The invention according to Claim 1, wherein said analog input signals vary sinusoidally at a given frequency, and said analog input signals include at least one voltage signal and a plurality of current signals.

3. The invention according to Claim 2, wherein said predetermined sampling schedule requires that each of

said analog input signals be sampled over 1000 times per second.

4. The invention according to Claim 3, wherein the sampling frequency of said predetermined sampling schedule is not a multiple of the given frequency of said analog input signals.

5. The invention according to Claim 1, wherein said predetermined variables include the phase difference between said voltage and current signals, the frequency of said voltage signal, and the RMS values of each of said analog input signals.

6. A high speed power analyzer for measuring electrical parameters in an alternating waveform power system, comprising:

input means for receiving a plurality of analog input signals which represent electrical parameters of the power system, where at least one of said analog input signals represents a voltage signal and another of said analog input signals represents a current signal;

multiplexer means connected to said input means for sampling each of said analog input signals by individually transmitting selected ones of said analog input signals;

converter means, connected to said multiplexer means, for converting sampled analog input signals received from said multiplexer means into a digital representation of said analog input signals; and

processor circuit means, coupled to said multiplexer means and said converter means, for controlling the sampling of said analog input signals by said multiplexer means in accordance with a predetermined sampling schedule, and for processing said digital representations of said analog input signals received from said converter means to produce a plurality of output

signals which are indicative of predetermined electrical variables related to the power being used in said power system, said processor circuit means including means for determining a zero crossing time in the waveform of at least two of said analog input signals by first detecting that a predetermined number of sampled data points of one numeric sign for an analog input signal have followed a predetermined number of sampled data points of the opposite numeric sign for said analog input signal, and then determining said zero crossing time from a linear extrapolation between the two sampled data points closest to the zero crossing of said analog input signal.

7. The invention according to Claim 6, wherein said one numeric sign is positive and said other numeric sign is negative.

8. The invention according to Claim 6, wherein said predetermined number of sampled data points for both of said numeric signs is two.

9. A high speed power analyzer for measuring electrical parameters in an alternating waveform power system, comprising:

input means for receiving a plurality of reference signals and a plurality of analog input signals which represent electrical parameters of the power system, where at least one of said analog input signals represents a voltage signal and another of said analog input signals represents a current signal;

multiplexer means connected to said input means for sampling each of said analog input signals by individually transmitting selected ones of said analog input signals;

amplifier means, connected to said multiplexer means, for amplifying the magnitude of sampled analog input signals received from said multiplexer means;

converter means, connected to said amplifier means, for converting sampled analog input signals received from said amplifier means into a digital representation of said analog input signals; and

processor circuit means, coupled to said multiplexer means and said converter means, for controlling the sampling of said reference signals and said analog input signals by said multiplexer means in accordance with a predetermined sampling schedule, and for processing said digital representation of said analog input signals received from said converter means to produce a plurality of output signals which are indicative of predetermined electrical variables related to the power being used in said power system, said processor circuit means including means for calibrating the conversion coefficients of said converter means by sampling said reference signals in accordance with said predetermined sampling schedule, adjusting said conversion coefficients when said adjustments are within a predetermined limit, and generating an error signal when said adjustments exceed said predetermined limit.

10. The invention according to Claim 9, wherein said reference signals are sampled at least once per second.

11. The invention according to Claim 6, wherein said predetermined sampling schedule is nonsynchronous with the waveform of said power system.

12. The invention according to Claim 9, wherein said predetermined sampling schedule is nonsynchronous with the waveform of said power system.

13. The invention according to Claim 12 wherein said processor circuit means includes means for determining a zero crossing time in the waveform of at least two of

said analog input signals by first detecting that a predetermined number of sampled data points of one numeric sign for an analog input signal have followed a predetermined number of sampled data points of the opposite numeric sign for said analog input signal, and then determining said zero crossing time from a linear extrapolation between the two sampled data points closest to the zero crossing of said analog input signal.

14. The invention according to Claim 9, wherein said processor circuit means includes means for determining a zero crossing time in the waveform of at least two of said analog input signals by first detecting that a predetermined number of sampled data points of one numeric sign for an analog input signal have followed a predetermined number of sampled data points of the opposite numeric sign for said analog input signal, and then determining said zero crossing time from a linear extrapolation between the two sampled data points closest to the zero crossing of said analog input signal.

15. The invention according to Claim 10, wherein said predetermined sampling schedule requires that each of said analog input signals be sampled over 1000 times per second.

16. The invention according to Claim 1, wherein said processor circuit means includes means for compensating for the difference between the times that said analog input signals are sampled.

17. The invention according to Claim 6, wherein said processor circuit means includes means for compensating for the difference between the times that said analog input signals are sampled.

18. The invention according to Claim 9, wherein said processor circuit means includes means for compensating for the difference between the times that said analog input signals are sampled.

19. A method of measuring electrical parameters in an alternating waveform power system, comprising the steps of:

receiving a plurality of analog input signals which represent electrical parameters of the power system, where at least one of said analog input signals represents a voltage signal and another of said analog input signals represents a current signal;

sampling each of said analog input signals in accordance with a predetermined sampling schedule which is nonsynchronous with the waveform of said power system;

converting said sampled analog input signals into a digital representation of said analog input signals; and

producing a plurality of output signals which are indicative of predetermined electrical variables related to the power being used in said power system.

20. The invention according to Claim 19, further including the step of determining a zero crossing time in the waveform of at least two of said analog input signals.

21. The invention according to Claim 20, wherein said zero crossing time is determined by first detecting that a predetermined number of sampled data points of one numeric sign for an analog input signal have followed a predetermined number of sampled data points of the opposite numeric sign for said analog input signal, and then performing a linear extrapolation between the two sampled data points closest to the zero crossing of said analog input signal.

22. The invention according to Claim 19, further including the steps of periodically sampling a plurality of reference signals, calibrating the coefficients used during said analog to digital conversion step from the measurement of said reference signals, adjusting said conversion coefficients when said adjustments are within a predetermined limit, and generating an error signal when said adjustments exceed said predetermined limit.

23. The invention according to Claim 19, further including the steps of sampling said analog input signals at different times, and compensating for the difference in times that said analog signals are sampled.

24. The invention according to Claim 19, wherein said predetermined variables include the phase difference between said voltage and current signals, the frequency of said voltage, and the RMS values of each of said analog input signals.

25. A method of measuring electrical parameters in an alternating waveform power system, comprising the steps of:

receiving a plurality of analog input signals which represent electrical parameters of the power system, where at least one of said analog input signals represents a voltage signal and another of said analog input signals represents a current signal;

sampling each of said analog input signals in accordance with a predetermined sampling schedule, said analog input signals being sampled at different times;

converting said sampled analog input signals into a digital representation of said analog input signals;

compensating for the difference in times that said analog signals are sampled; and

producing a plurality of output signals which are indicative of predetermined electrical variables related to the power being used in said power system.

26. The invention according to Claim 25, wherein said predetermined variables include the phase difference between said voltage and current signals, the frequency of said voltage, and the RMS values of each of said analog input signals.

27. A method of measuring electrical parameters in an alternating waveform power system, comprising the steps of:

receiving a plurality of analog input signals which represent electrical parameters of the power system, where at least one of said analog input signals represents a voltage signal and another of said analog input signals represents a current signal;

sampling each of said analog input signals in accordance with a predetermined sampling schedule;

converting said sampled analog input signals into a digital representation of said analog input signals;

determining a zero crossing time in the waveform of at least two of said analog input signals by first detecting that a predetermined number of sampled data points of one numeric sign for an analog input signal have followed a predetermined number of sampled data points of the opposite numeric sign for said analog input signal, and then performing a linear extrapolation between the two sampled data points closest to the zero crossing of said analog input signal; and

producing a plurality of output signals which are indicative of predetermined electrical variables related to the power being used in said power system.

28. The invention according to Claim 27, wherein said predetermined variables include the phase difference between said voltage and current signals, the frequency of said voltage, and the RMS values of each of said analog input signals.

29. A method of measuring electrical parameters in an alternating waveform power system, comprising the steps of:

receiving a plurality of analog input signals which represent electrical parameters of the power system, where at least one of said analog input signals represents a voltage signal and another of said analog input signals represents a current signal;

sampling each of said analog input signals in accordance with a predetermined sampling schedule;

converting said sampled analog input signals into a digital representation of said analog input signals;

periodically sampling a plurality of reference signals, calibrating the coefficients used during said analog to digital conversion step from the measurement of said reference signals, adjusting said conversion coefficients when said adjustments are within a predetermined limit, and generating an error signal when said adjustments exceed said predetermined limit; and

producing a plurality of output signals which are indicative of predetermined electrical variables related to the power being used in said power system.

30. The invention according to Claim 29, wherein said predetermined variables include the phase difference between said voltage and current signals, the frequency of said voltage, and the RMS values of each of said analog input signals.

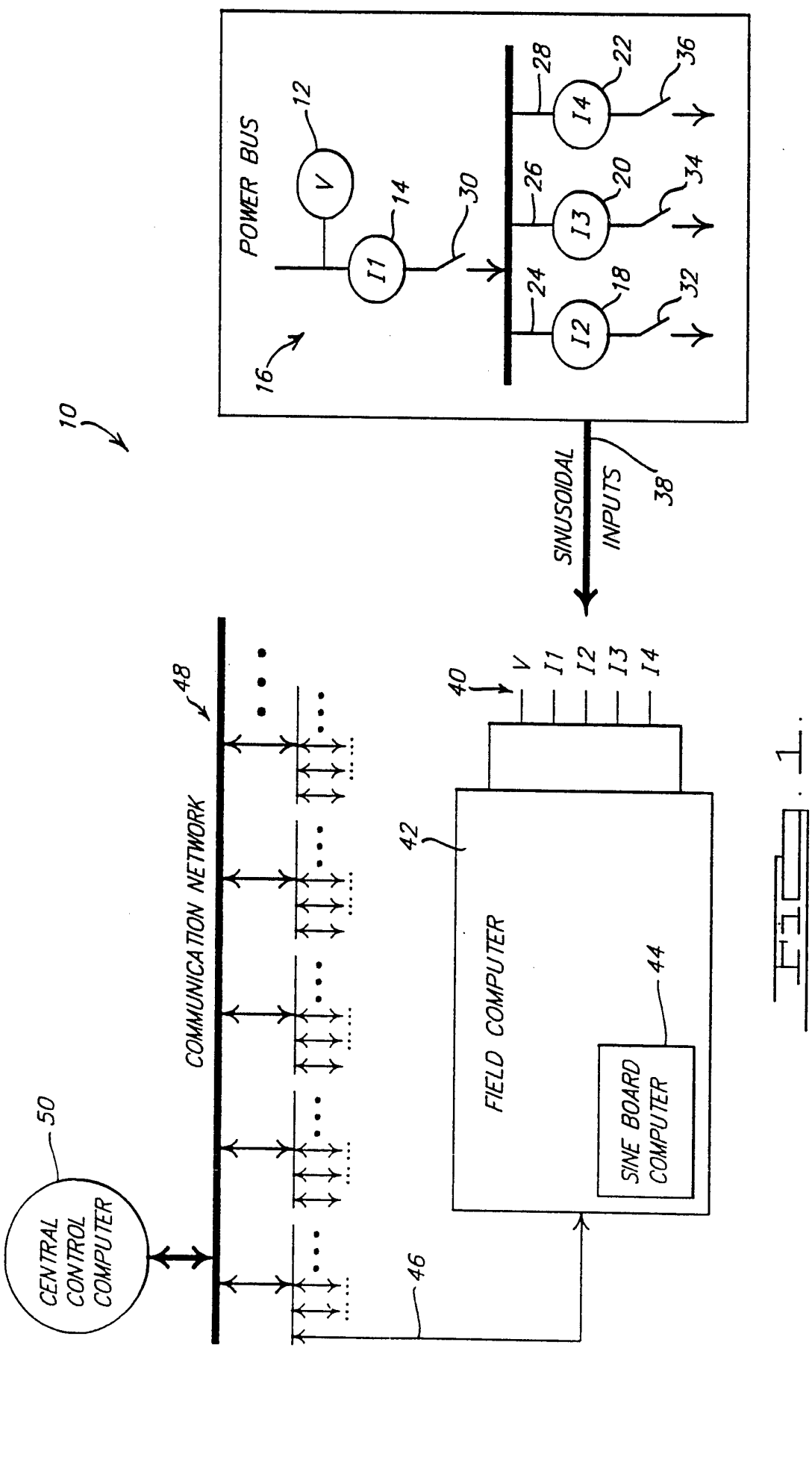
10
POWER BUS
16
V
12
I1
14
30
I2
18
24
32
I3
20
26
34
I4
22
28
36
SINUSOIDAL INPUTS
38
V
I1
I2
I3
I4
40
42
FIELD COMPUTER
SINE BOARD COMPUTER
44
46
48
COMMUNICATION NETWORK
50
CENTRAL CONTROL COMPUTER

Fig. 1.

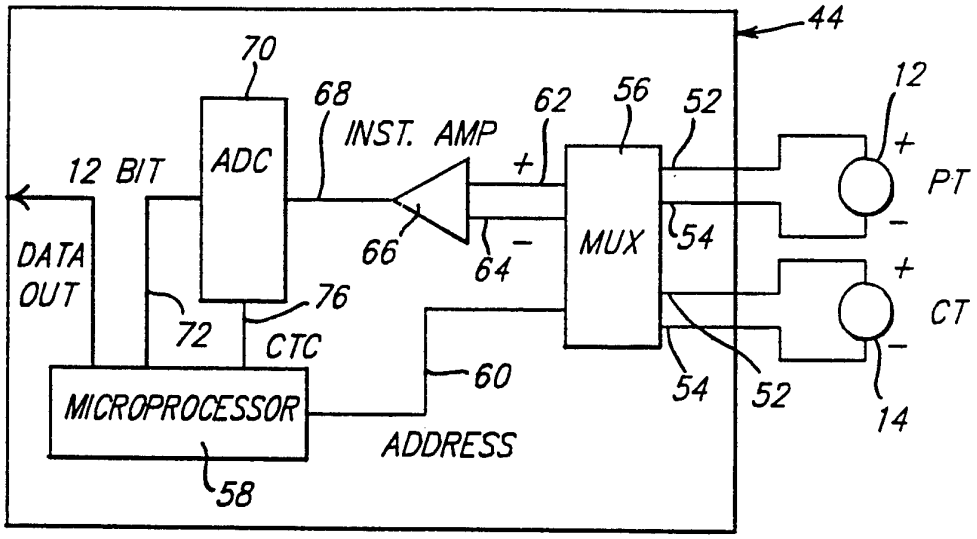

FIG. 2.

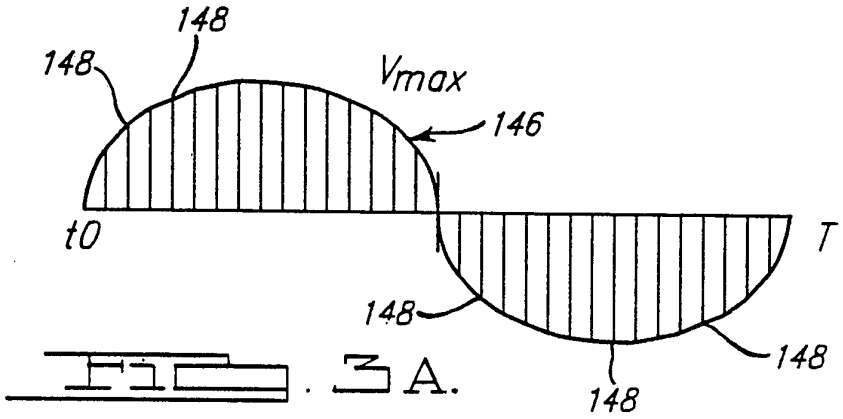

FIG. 3A.

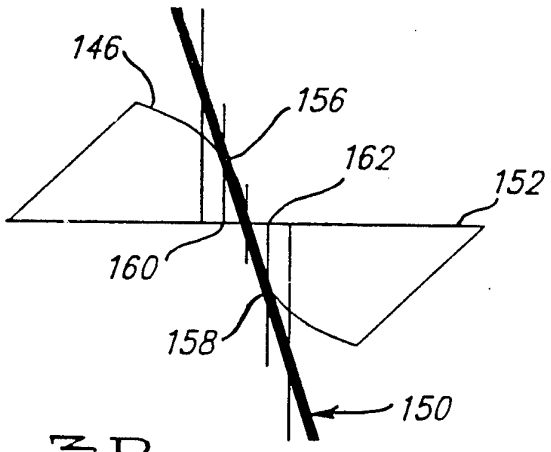

FIG. 3B.

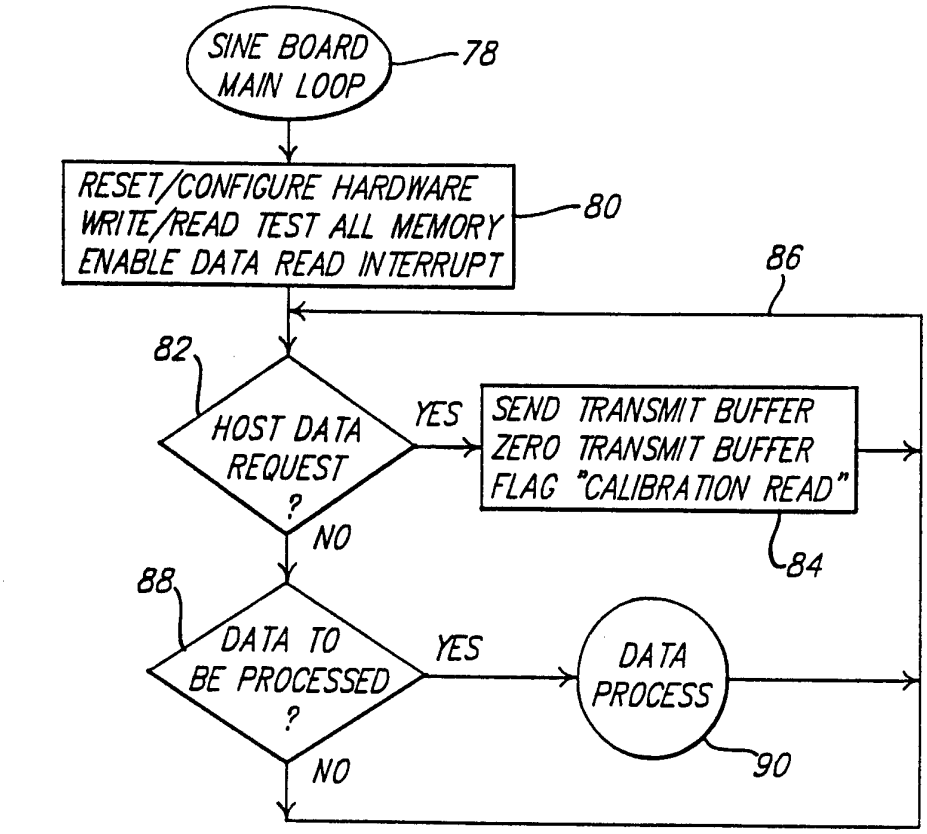
SINE BOARD MAIN LOOP
78
RESET/CONFIGURE HARDWARE
WRITE/READ TEST ALL MEMORY
ENABLE DATA READ INTERRUPT
80
86
82
HOST DATA REQUEST ?
YES
SEND TRANSMIT BUFFER
ZERO TRANSMIT BUFFER
FLAG "CALIBRATION READ"
84
NO
88
DATA TO BE PROCESSED ?
YES
DATA PROCESS
90
NO

Fig. 4A.

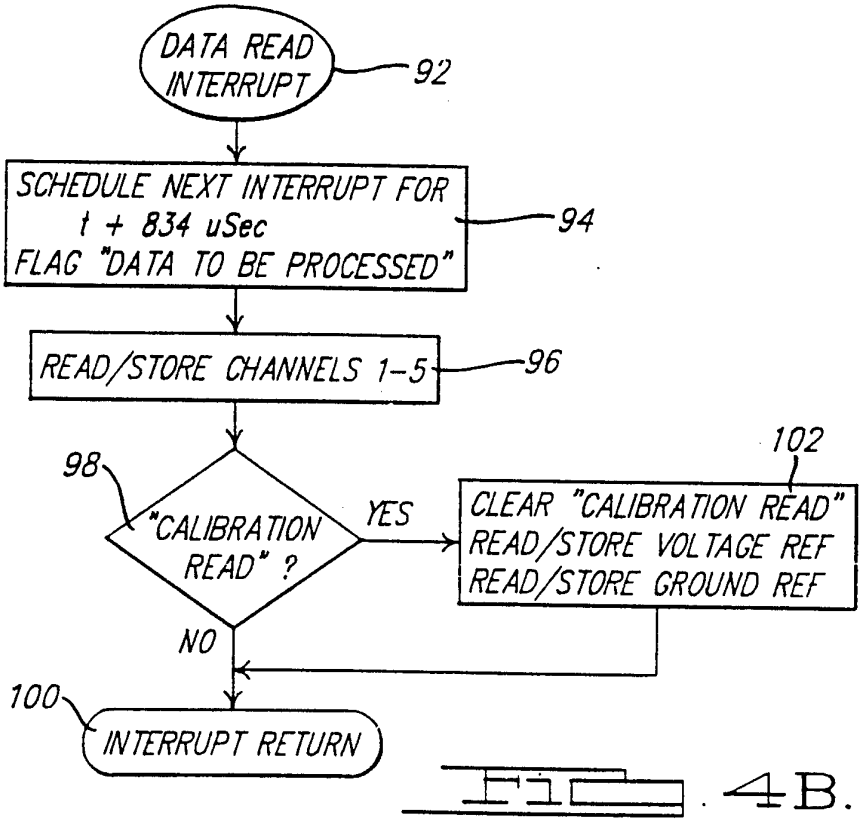
DATA READ INTERRUPT
92
SCHEDULE NEXT INTERRUPT FOR
t + 834 uSec
FLAG "DATA TO BE PROCESSED"
94
READ/STORE CHANNELS 1-5
96
102
98
"CALIBRATION READ" ?
YES
CLEAR "CALIBRATION READ"
READ/STORE VOLTAGE REF
READ/STORE GROUND REF
NO
100
INTERRUPT RETURN

Fig. 4B.

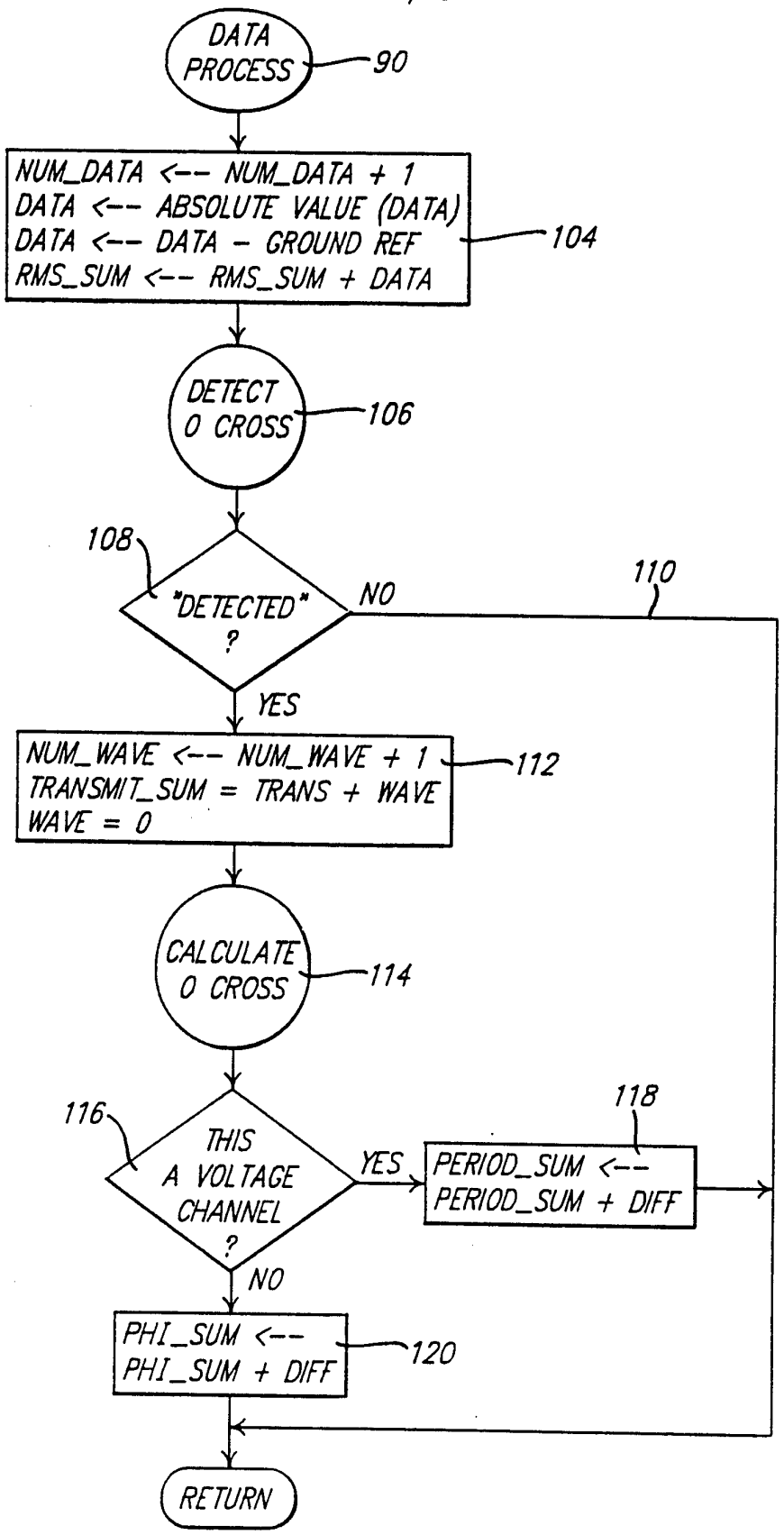
DATA PROCESS
90
NUM_DATA <-- NUM_DATA + 1
DATA <-- ABSOLUTE VALUE (DATA)
DATA <-- DATA - GROUND REF
RMS_SUM <-- RMS_SUM + DATA
104
DETECT 0 CROSS
106
108
"DETECTED" ?
NO
110
YES
NUM_WAVE <-- NUM_WAVE + 1
TRANSMIT_SUM = TRANS + WAVE
WAVE = 0
112
CALCULATE 0 CROSS
114
116
THIS A VOLTAGE CHANNEL ?
YES
118
PERIOD_SUM <-- PERIOD_SUM + DIFF
NO
PHI_SUM <-- PHI_SUM + DIFF
120
RETURN

FIG. 4C.

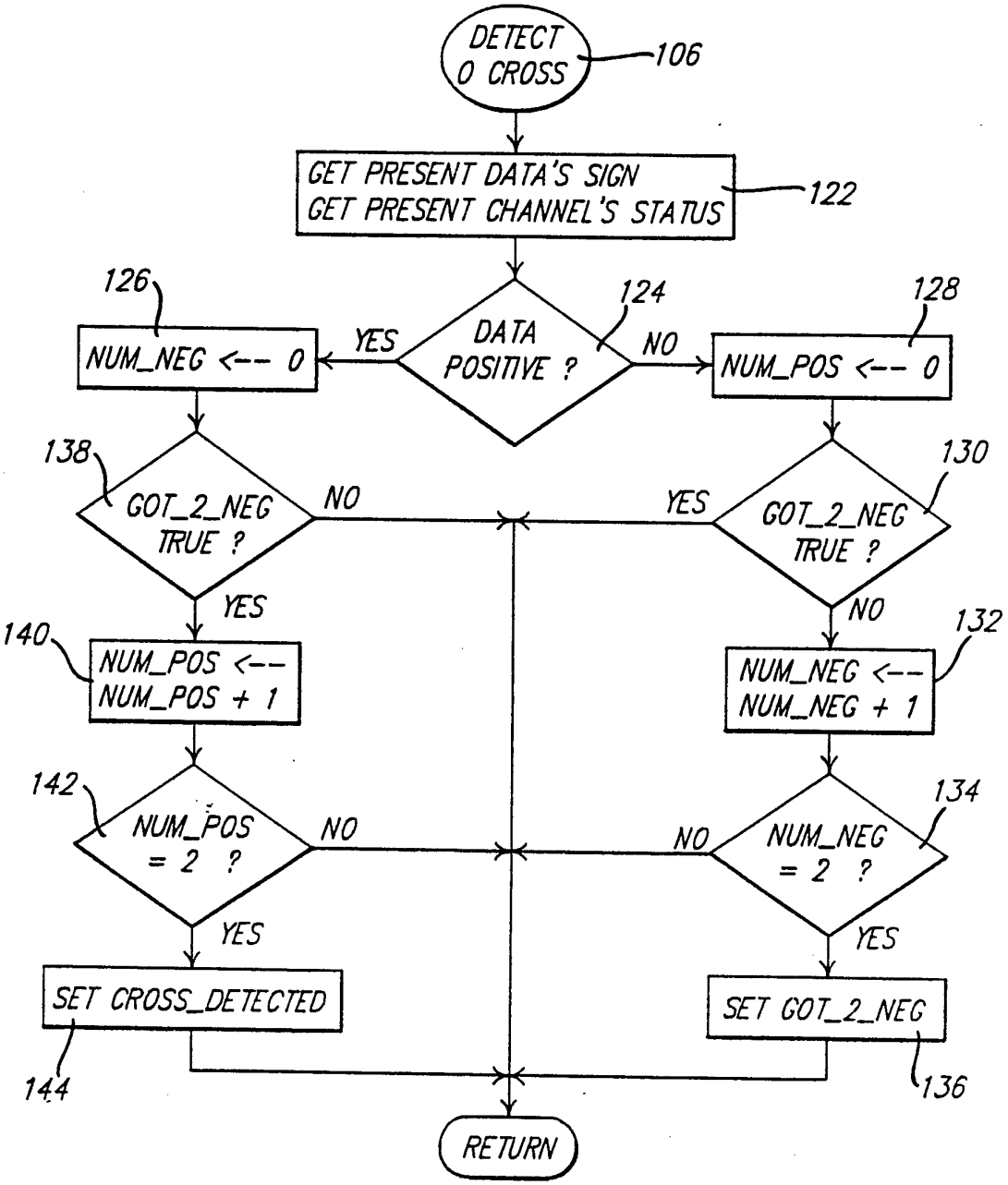
DETECT 0 CROSS
106
GET PRESENT DATA'S SIGN
GET PRESENT CHANNEL'S STATUS
122
DATA POSITIVE ?
124
YES
NO
126
NUM_NEG <-- 0
128
NUM_POS <-- 0
138
GOT_2_NEG TRUE ?
NO
YES
130
GOT_2_NEG TRUE ?
YES
NO
140
NUM_POS <-- NUM_POS + 1
132
NUM_NEG <-- NUM_NEG + 1
142
NUM_POS = 2 ?
NO
NO
134
NUM_NEG = 2 ?
YES
YES
SET CROSS_DETECTED
144
SET GOT_2_NEG
136
RETURN

FIG. 4D.

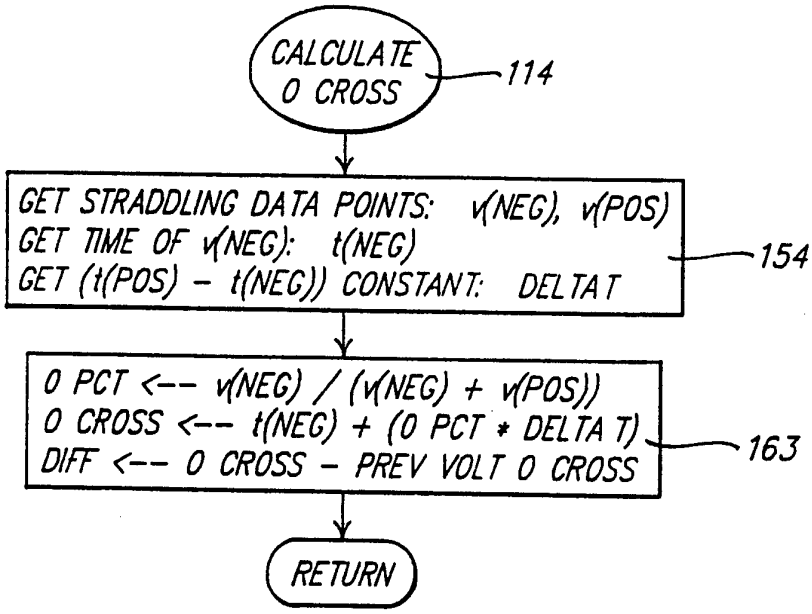
CALCULATE 0 CROSS
114
GET STRADDLING DATA POINTS: v(NEG), v(POS)
GET TIME OF v(NEG): t(NEG)
GET (t(POS) - t(NEG)) CONSTANT: DELTAT
154
0 PCT <-- v(NEG) / (v(NEG) + v(POS))
0 CROSS <-- t(NEG) + (0 PCT * DELTA T)
DIFF <-- 0 CROSS - PREV VOLT 0 CROSS
163
RETURN

Fig. 4E.

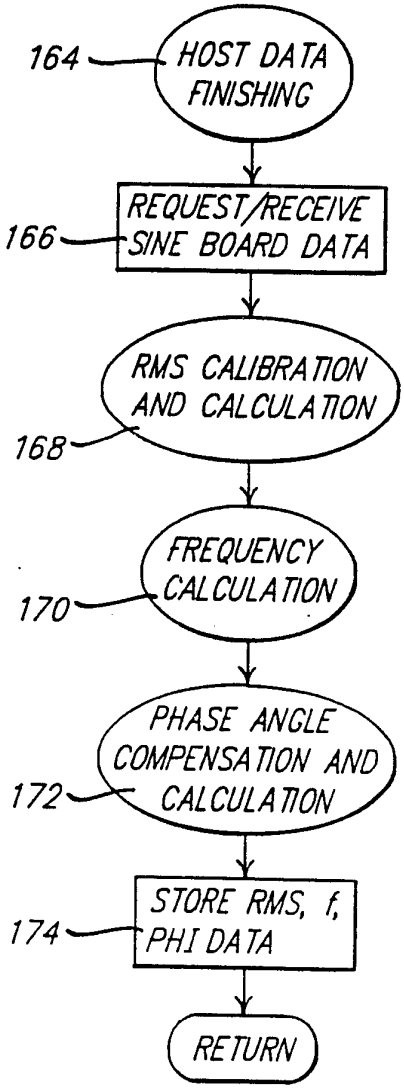
164
HOST DATA FINISHING
REQUEST/RECEIVE SINE BOARD DATA
166
RMS CALIBRATION AND CALCULATION
168
FREQUENCY CALCULATION
170
PHASE ANGLE COMPENSATION AND CALCULATION
172
STORE RMS, f, PHI DATA
174
RETURN

Fig. 5A.

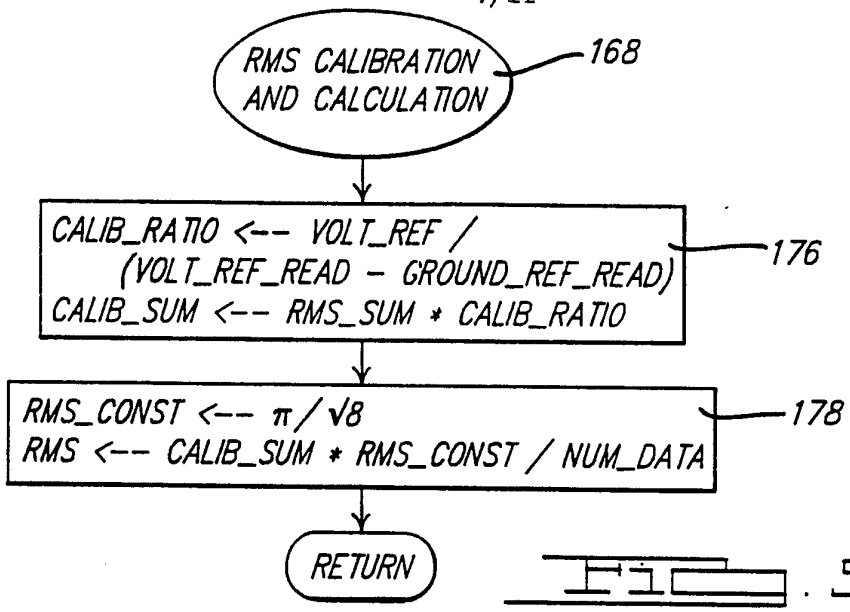

Fig. 5B.

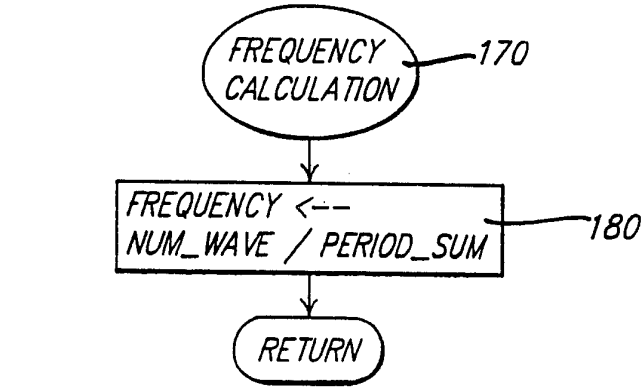

Fig. 5C.

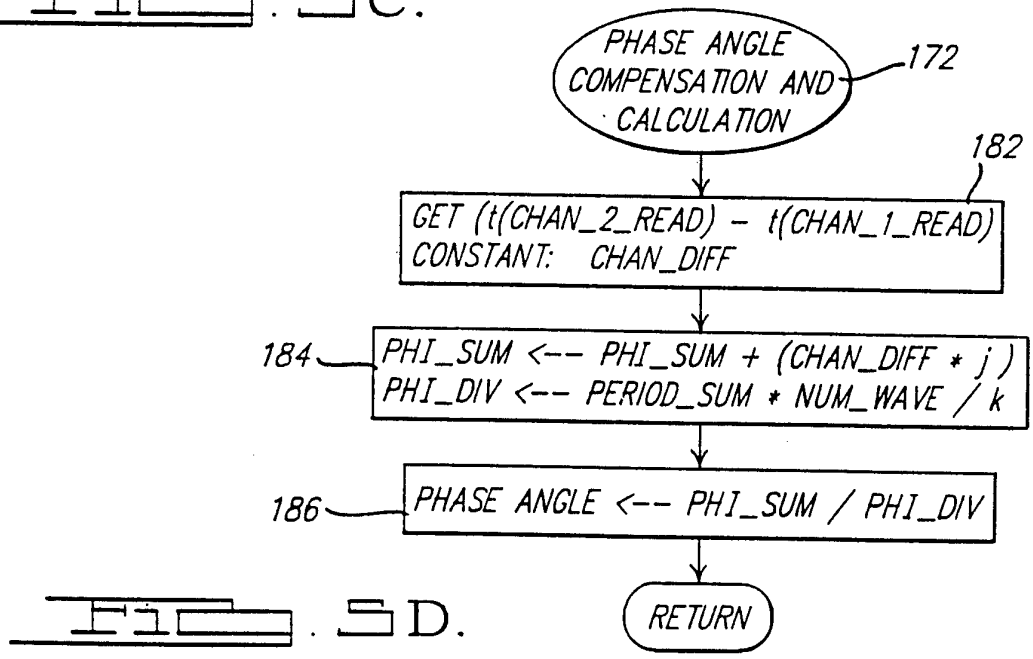

Fig. 5D.

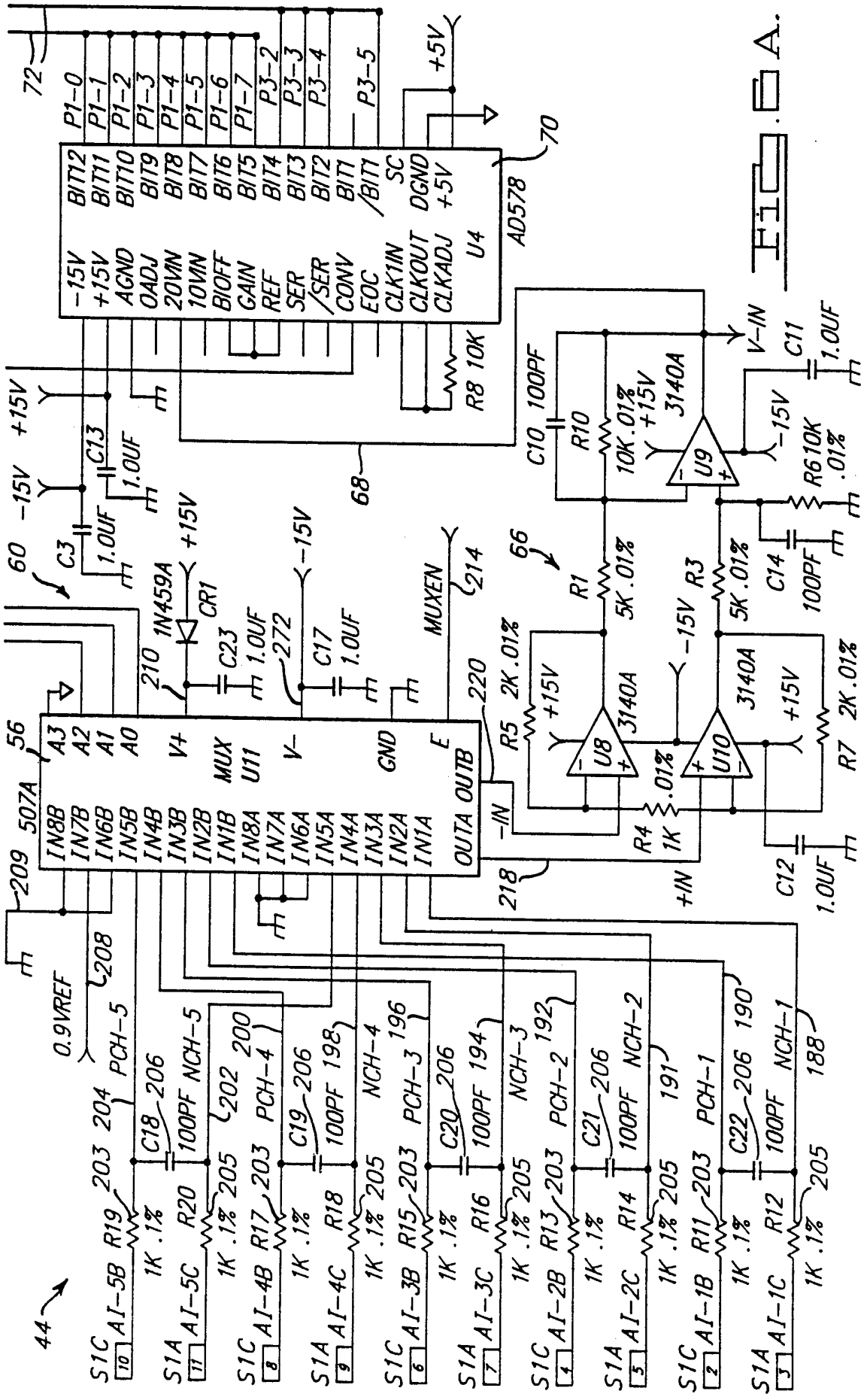
72
P1-0
P1-1
P1-2
P1-3
P1-4
P1-5
P1-6
P1-7
P3-2
P3-3
P3-4
P3-5
+5V
70
AD578
U4
BIT12
BIT11
BIT10
BIT9
BIT8
BIT7
BIT6
BIT5
BIT4
BIT3
BIT2
BIT1
/BIT1
SC
DGND
+5V
-15V
+15V
AGND
OADJ
20VIN
10VIN
BIOFF
GAIN
REF
SER
/SER
CONV
EOC
CLK1IN
CLKOUT
CLKADJ
R8 10K
68
+15V
-15V
C13
1.0UF
C3
1.0UF
60
1N459A
CR1
C23
1.0UF
210
272
C17
1.0UF
MUXEN
214
220
56
507A
A3
A2
A1
A0
V+
MUX
U11
V-
GND
E
OUTB
OUTA
IN8B
IN7B
IN6B
IN5B
IN4B
IN3B
IN2B
IN1B
IN8A
IN7A
IN6A
IN5A
IN4A
IN3A
IN2A
IN1A
209
208
0.9VREF
218
-IN
+IN
66
R1
5K .01%
R3
5K .01%
R5
2K .01%
R7
2K .01%
R4
1K .01%
U8
3140A
U10
3140A
C10
100PF
R10
10K .01%
U9
3140A
V-IN
C11
1.0UF
R6 10K
.01%
C14
100PF
C12
1.0UF
PCH-5
NCH-5
PCH-4
NCH-4
PCH-3
NCH-3
PCH-2
NCH-2
PCH-1
NCH-1
204
202
200
198
196
194
192
191
190
188
C18
C19
C20
C21
C22
206
100PF
203
205
R19
R20
R17
R18
R15
R16
R13
R14
R11
R12
1K .1%
44
S1C
S1A
AI-5B
AI-5C
AI-4B
AI-4C
AI-3B
AI-3C
AI-2B
AI-2C
AI-1B
AI-1C
10
11
8
9
6
7
4
5
2
3

FIG. 6A.

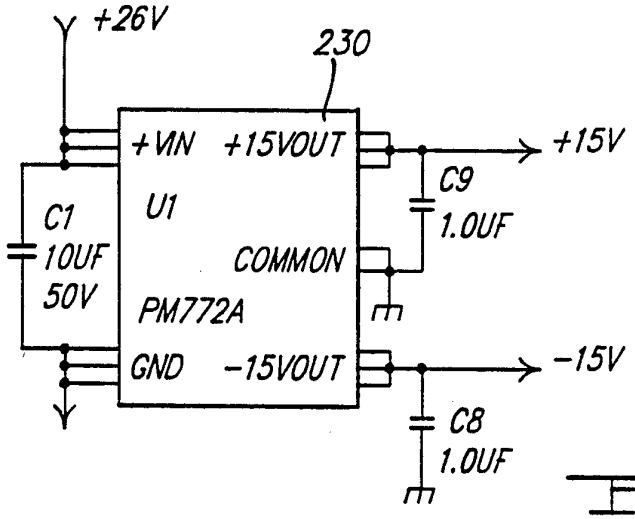

FIG. 6B.

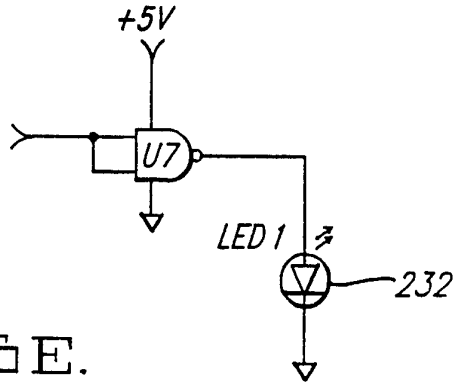

FIG. 6E.

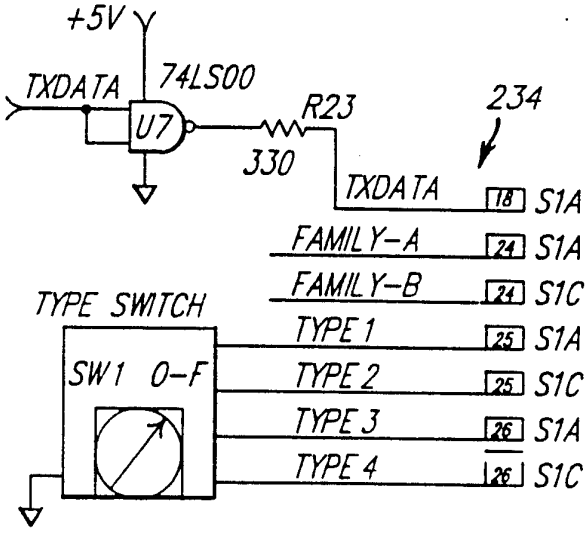

FIG. 6F.

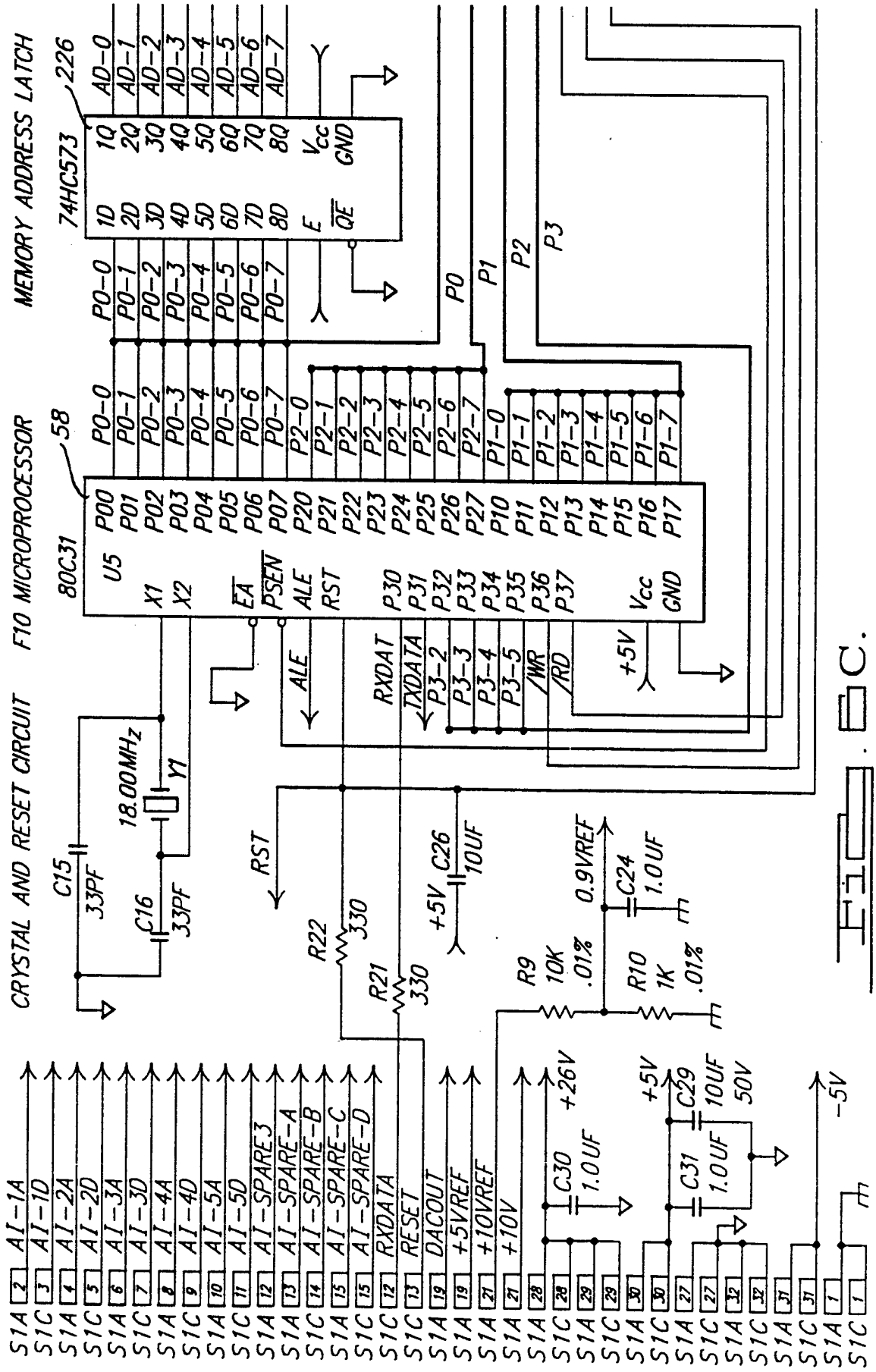
CRYSTAL AND RESET CIRCUIT
F10 MICROPROCESSOR
MEMORY ADDRESS LATCH
80C31
74HC573
18.00MHz
Y1
C15 33PF
C16 33PF
C26 10UF
C24 1.0UF
C30 1.0UF
C31 1.0UF
C29 10UF 50V
R22 330
R21 330
R9 10K .01%
R10 1K .01%
+5V
+26V
-5V
0.9VREF
RST
ALE
RXDAT
TXDATA
/WR
/RD
AD-0
AD-1
AD-2
AD-3
AD-4
AD-5
AD-6
AD-7
P0
P1
P2
P3
A1-1A
A1-1D
A1-2A
A1-2D
A1-3A
A1-3D
A1-4A
A1-4D
A1-5A
A1-5D
A1-SPARE3
A1-SPARE-A
A1-SPARE-B
A1-SPARE-C
A1-SPARE-D
RXDATA
RESET
DACOUT
+5VREF
+10VREF
+10V

FIG. 6C.

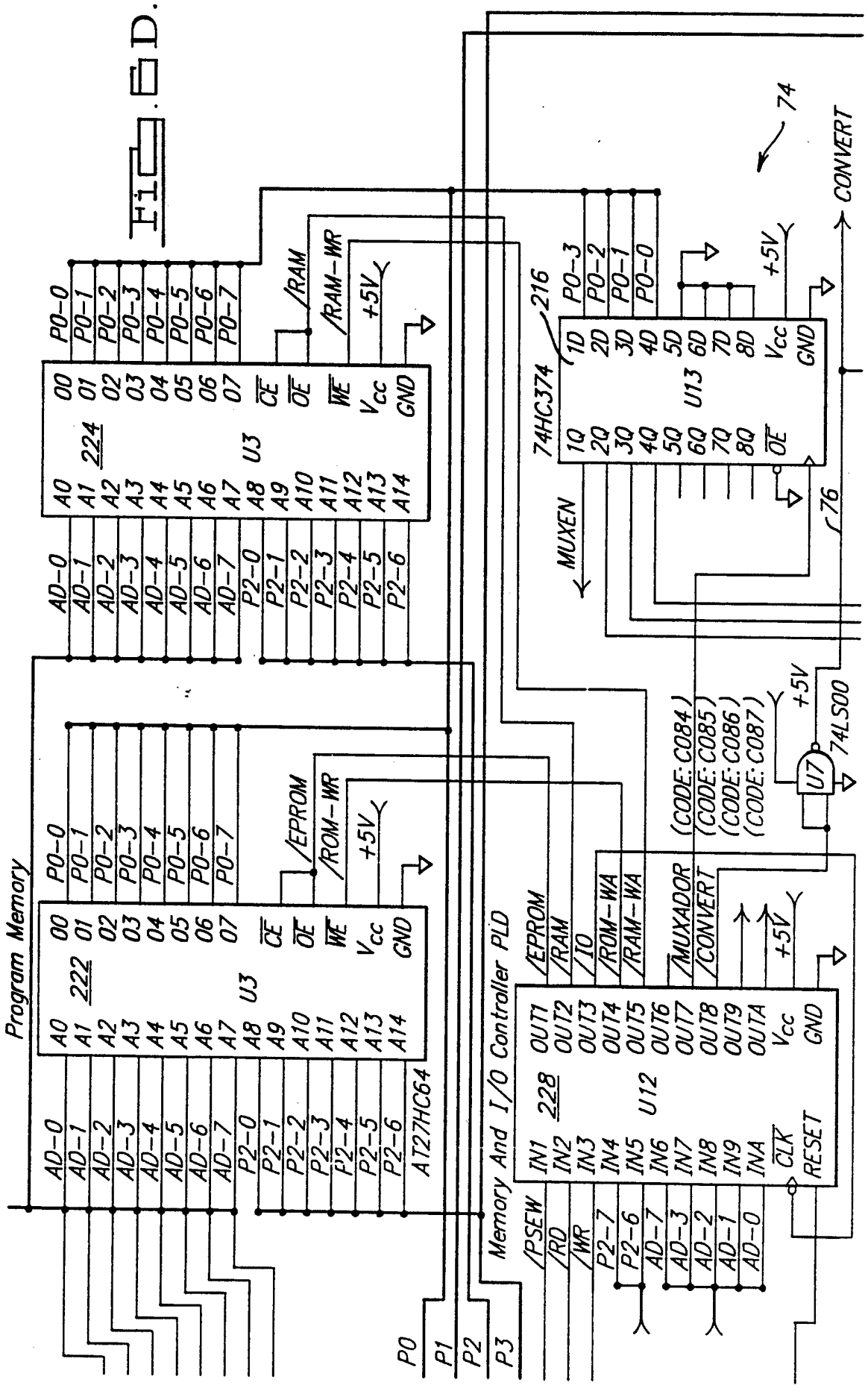
Program Memory
222
U3
AT27HC64
224
U3
/EPROM
/ROM-WR
/RAM
/RAM-WR
+5V
Memory And I/O Controller PLD
228
U12
/PSEW
/RD
/WR
/EPROM
/RAM
/IO
/ROM-WA
/RAM-WA
/MUXADOR
/CONVERT
(CODE: C084)
(CODE: C085)
(CODE: C086)
(CODE: C087)
74HC374
216
U13
MUXEN
74
76
CONVERT
74LS00
U7
P0
P1
P2
P3

FIG. 6D.

INTERNATIONAL SEARCH REPORT

International Application No PCT/US 92/06439

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all)[6]

According to International Patent Classification (IPC) or to both National Classification and IPC

Int.Cl. 5 G01R21/133; G01R35/04; G01R19/175

II. FIELDS SEARCHED

Minimum Documentation Searched[7]

Classification System	Classification Symbols
Int.Cl. 5	G01R ; H04N

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched[8]

III. DOCUMENTS CONSIDERED TO BE RELEVANT[9]

Category °	Citation of Document,[11] with indication, where appropriate, of the relevant passages[12]	Relevant to Claim No.[13]
X Y	US,A,4 672 555 (HART ET AL.) 9 June 1987 see column 1, line 51 - column 2, line 27; figures 1,2	25 1-4,6,7, 9,10,15, 16,19, 26,27,29
A		5,11,12, 17,18, 24,26, 28,30
Y	US,E,31 774 (FLETCHER ET AL.) 18 December 1984 see column 1, line 27 - line 37; figure 1	1-4,19

-/--

° Special categories of cited documents :[10]

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

IV. CERTIFICATION

Date of the Actual Completion of the International Search	Date of Mailing of this International Search Report
10 MAY 1993	26.05.93
International Searching Authority	**Signature of Authorized Officer**
EUROPEAN PATENT OFFICE	IWANSSON K.G.

III. DOCUMENTS CONSIDERED TO BE RELEVANT (CONTINUED FROM THE SECOND SHEET)

Category °	Citation of Document, with indication, where appropriate, of the relevant passages	Relevant to Claim No.
Y	EP,A,0 400 730 (PHILIPS ELECTRONIC) 5 December 1990	6,7,27
A	see page 2, line 18 - line 24	8,13,14, 20,21
	see page 3, line 14 - line 40; figure 1	
Y	WO,A,9 110 146 (VALTION TEKNILLINEN) 11 July 1991	9,10,15, 29
A	see page 10, line 32 - page 11, line 26	5,22,24, 26,28,30
	see page 12, line 7 - line 14	
	see page 19, line 34 - line 37; figures 3,6,7	
X	EP,A,0 462 045 (TRANSDATA) 18 December 1991	25
Y	see abstract	16
A	see column 3, line 16 - line 19	9,17,18, 23,26, 28,30
	see column 8, line 1 - line 25; figure 1	
Y	EP,A,0 243 835 (MASCHINENFABRIKREINHAUSEN) 4 November 1987	26
A	see column 1, line 15 - line 7	5-7,13, 14,20, 21,24, 27,28,30
	see column 1, line 35 - page 2, line 5; figures 1,2	
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