

(19) World Intellectual Property Organization
International Bureau



(43) International Publication Date
10 November 2011 (10.11.2011)

(10) International Publication Number
WO 2011/139503 A1

(51) International Patent Classification:
H04L 7/033 (2006.01)

(21) International Application Number:
PCT/US2011/032338

(22) International Filing Date:
13 April 2011 (13.04.2011)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
61/330,221 30 April 2010 (30.04.2010) US

(71) Applicant (for all designated States except US): **RAMBUS INC.** [US/US]; 1050 Enterprise Way, Suite 700, Sunnyvale, CA 94089 (US).

(72) Inventor; and

(75) Inventor/Applicant (for US only): **ZERBE, Jared, L.** [US/US]; 431 Hillside Drive, Woodside, CA 94062 (US).

(74) Agent: **KREISMAN, Lance, M.**; Mahamedi Paradise Kreisman LLP, 550 South Winchester Blvd., Suite 605, San Jose, CA 95128 (US).

(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO,

DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PE, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Declarations under Rule 4.17:

— of inventorship (Rule 4.17(iv))

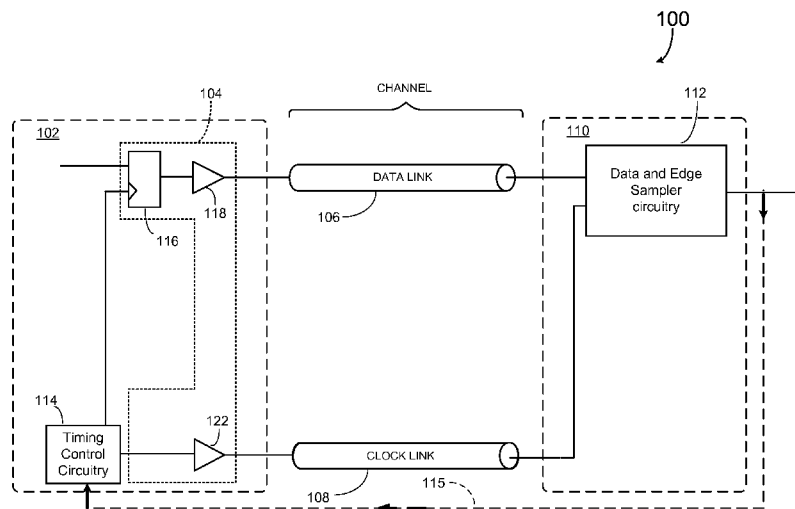
Published:

— with international search report (Art. 21(3))

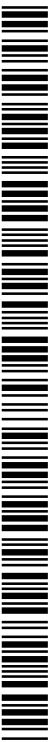
— before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments (Rule 48.2(h))

(54) Title: LOW POWER EDGE AND DATA SAMPLING

FIG. 1



(57) Abstract: An integrated circuit receiver is disclosed comprising a data receiving circuit responsive to a timing signal to detect a data signal and an edge receiving circuit responsive to the timing signal to detect a transition of the data signal. One of the data or edge receiving circuits comprises an integrating receiver circuit while the other of the data or edge sampling circuits comprises a sampling receiver circuit.



WO 2011/139503 A1

LOW POWER EDGE AND DATA SAMPLING

TECHNICAL FIELD

[0001] The disclosure herein relates to signaling systems and more particularly to receiver circuits having edge and data samplers.

BACKGROUND

[0002] Tracking timing between data and an associated timing signal, such as a clock signal, is important for high-speed signaling systems. Conventionally, identical edge and data samplers are often used to maintain clock/data timing, each responsive to respective clock signals offset in phase by approximately 90 degrees. While this can work well for its intended applications, generating the additional 90 degree clock signal often presents pin and/or requires additional power at the receiver end. Thus, the need exists for a pin and power-efficient tracking solution for high-speed signaling systems.

BRIEF DESCRIPTION OF THE DRAWINGS

[0003] Embodiments of the disclosure are illustrated by way of example, and not by way of limitation, in the figures of the accompanying drawings and in which like reference numerals refer to similar elements and in which:

Figure 1 illustrates a block diagram of a signaling system according to an embodiment;

Figure 2 illustrates a block diagram of an embodiment of a receiver apparatus within the signaling system of Figure 1;

Figure 3 illustrates a timing diagram relating to the receiver apparatus of Figure 2;

Figure 4 illustrates a block diagram of an embodiment of a receiver apparatus within the system of Figure 1; and

Figure 5 illustrates a timing diagram relating to the receiver apparatus of Figure 4.

DETAILED DESCRIPTION

[0004] Embodiments of integrated circuit receivers are disclosed herein. One embodiment of the receiver comprises a data receiving circuit and an edge receiving circuit. The data receiving circuit responds to a timing signal to detect a data signal at a location with significant timing margins, while the edge receiving circuit responds to the timing signal to detect a transition of the data signal and give a determination of the data being 'early' or 'late' compared to an ideal phase position for sampling data. One of the data or edge receiving circuits comprises an integrating receiver circuit while the other of the data or edge receiving circuits comprises a sampling receiver circuit. Employing an integrating receiver and a sampling receiver circuit together in the integrated circuit receiver improves efficiencies in both power and pin count.

[0005] In one embodiment, a method of operation in an integrated circuit receiver is presented. The method includes receiving a data signal having a valid data region and a transition region. A timing signal is also received, such that a data value in the valid data region is detected in response to the timing signal. An edge value in the transition region is also detected in response to the timing signal to generate early/late information. One of detecting the data or edge value comprises integrating in response to the timing signal.

[0006] In a further embodiment, a signaling system is described. The system comprises a first integrated circuit device including a transmitter circuit to transmit a data signal and an accompanying timing signal. A second integrated circuit device is employed and includes a receiver circuit to receive the data signal and the timing signal. The receiver circuit includes a first receiving circuit responsive to a timing signal to detect a valid data region of a data signal. A second receiving circuit responds to the timing signal to detect a transition region associated with the data signal. One of the first or second receiver circuits comprises an integrating receiver circuit, while the other of the first or second receiver circuits comprises a sampling receiver circuit.

[0007] Figure 1 illustrates a block diagram of a signaling system 100 according to an embodiment. The signaling system 100 includes a clock and data recovery (CDR) loop including a first integrated circuit device (IC) 102 and a second IC device 110. Transmitter circuitry 104 on the first IC device 102 drives a data symbol, or signal, along a data link or path 106. An associated source-synchronous timing reference, such as a clock signal, is transmitted by the transmitter circuitry 104 along a timing reference link, such as clock path 108. Timing control circuitry 114 disposed on the first integrated circuit device 102 controls adjustment of the relative phases of the clock and data signals. Receiver circuitry 112, in the form of respective data and edge receiver circuits, is disposed on the second integrated circuit

device (IC) 110, to receive and detect data and edge values of the data signals (received via data link 106) in response to the clock signals (received via clock path 108).

[0008] The transmitter circuitry 104 employs a data transmitter in the form of a clocked storage element 116, such as a flip-flop, having a data input to receive a serial data stream and a clock input to receive a clock signal. The flip-flop generates data in response to the clock, where it is buffered and driven across the data link 106 by an optional output buffer 118. In some embodiments, the transmitter circuitry 104 may include an equalizer (not shown) to provide transmit-side equalization that modifies the data signal to minimize the effects of anticipated inter-symbol-interference. While only one data link 106 is shown for purposes of clarity, a plurality of data links configured as a parallel bus may be employed, each with its own associated transmitter and receiver circuitry.

[0009] To provide the source-synchronous timing reference, the transmitter circuitry 104 includes a clock driver 122 coupled to the timing control circuitry 114. The clock driver generally includes an input to receive a timing reference, such as a clock signal, from the timing control circuitry and an output to drive the clock signal across the clock link 108. The timing control circuitry 114 generates the clock signals for the data and clock drivers and controls and adjusts the phase relationship between the respective clock signals to correspondingly adjust the timing relationships between the data transmitted on the data link and the clock signal transmitted on the clock link. While many of the embodiments described herein illustrate a source-synchronous context for the teachings herein, it should be understood that a variety of timing architectures are suitable for the data and edge receiver circuits described. For instance, the data and timing reference may be embedded together, or take on a mesochronous or pleisiochronous relationship. Further, while a clock signal is described throughout the disclosure, the timing reference may take the form of an aperiodic strobe signal.

[0010] In some embodiments, an optional back-channel 115 (in phantom) provides a path for communicating phase error information from the second integrated circuit device 110 to the first integrated circuit device 102. The phase error information enables the timing control circuitry 114 to carry out adaptive, continuous, or periodically updated phase adjustments between clock and data. Other embodiments may employ the timing control circuitry on the second integrated circuit device 110, in which case the optional backchannel may comprise a straightforward feedback path completely routed on the second IC 110.

[0011] With continued reference to Figure 1, the data and edge receiver circuitry 112 of the second IC 110 receives the data from the data link 106 to generate data and edge values that, when compared to each other, may be used to indicate phase error information. Generally speaking, taking data values involves detecting the data signal level in response to the timing signal within a valid data range. In contrast, taking edge values involves detecting the signal level in one of the transition regions located on each end of the valid data region. As more fully described below, in some embodiments, data and edge receiving is accomplished without the need for a second timing reference accompanying the data receiver. This desirably reduces power consumption and increases pin efficiency for the second IC 110.

[0012] Figure 2 illustrates a block diagram of one embodiment of a data and edge receiver circuitry 200. The data and edge receiver circuitry 200 employs an integrating receiver circuit 202 to provide edge information while a conventional first direct sampler (a non-integrating receiver) 204 performs a data sampler role. From a topological perspective, data propagating along the data link 106 follows respective edge and data receiver paths 207 and 205 to the inputs of the edge and data receivers 202 and 204 respectively. The clock link 108 feeds the clock signal through buffer circuitry 209 (optional) where it fans out from node 211 to respective precharge and sense integrating receiver edge clock paths 212 and 214, and a data clock path 216.

[0013] The integrating receiver circuit 202 includes an integrator 206 with a data input that receives a version of the data signal from an optional input buffer 208 via path 207, and a second direct sampler 210 to sample an output of the integrator 206. To receive respective precharge and sense portions of the edge clock, the integrator 206 and the second direct sampler 210 include respective opposing edge-triggered clock inputs. The integrator 206 may take various forms, including a saturating integrator, window integrator (with appropriately configured precharge and sense clocks skewed relative to each other by a delay in the precharge path), or the like. When using the integrator circuit as an edge receiver, a saturating integrator often provides optimum performance well-suited for balancing the time the data bit precedes the clock edge versus the time the data bit follows the clock edge.

[0014] The first direct sampler 204 includes a data input to receive the data signal from the optional input buffer 208 via the data sample path 205. The direct sampler 204 includes a data clock input that receives a version of the clock signal via the data clock path 216. As more fully described below, in some instances, the data clock signal may be delayed to compensate either for propagation delays incurred through the data buffer 208 or for a setup time difference between the integrator 206 and the data sampler 204. In the embodiment of Figure 2, the first IC 102 (Figure 1) transmits the clock signal and data signal along respective data and clock links 106 and 108 (corresponding to the data and clock links 106 and 108 of Figure 1) in a quadrature relationship (offset in phase by approximately 90 degrees). The phase offset allows the clock to trigger sampling of the data by the data sampler 204 near the center of the data eye.

[0015] Further referring to Figure 2, various matching delay elements may be employed to account for first and second order delays attributable to differing propagation times for clock and data signals, and other similar effects. For example, first order matching may be accomplished by employing identical circuitry for the first and second direct samplers 204 and

210. This maintains consistent and predictable setup and hold timing between the two direct samplers. In some embodiments, a delay line 213 may be employed to delay the data clock signal to the first direct data sampler 204 by an amount corresponding to the delay incurred by the data signal through the front-end buffer 208 and switches or other circuitry affecting the setup time of the integrator 206.

[0016] Figure 3 illustrates a timing diagram illustrating operation of the data and edge receiver circuit 200 of Figure 2. Various data, clock and integrator output waveforms are shown having the same timing scale along the X-axis, with voltage represented along the Y-axis to denote logic signal levels “0” and “1” and analog voltage levels. A data waveform 302 reflects a DDR data signal with a single bit framed as a reference to illustrate a data eye. A first valid data region 304 lies between a first edge transition region 305 and a second edge transition region 306. A second valid data region 307 is adjacent the second edge transition region. As the timing input to the data sampler 204, a rising edge 308 of a clock signal 310 triggers sampling of the data signal (within the first valid data region 304). For purposes of this example, the clock signal 310 has an optimal 90 degree relationship with respect to the data bit. When clocking the integrator 206, the clock rising edge, at 308, represents a release of precharge of the integrator and thus the beginning of the integration period, while the falling edge of the clock, at 312, represents an activation of a sense-amp (not shown), and thus effectively ending the integration. For non-windowing integrators, the precharge and sense edges are reversed for the second data bit within the same clock signal. For windowed integrators, polarity inversion works on adjacent (odd/even) bits. Note that the same clock edge triggers precharge of the integrator 206 and sampling by the first direct sampler 204. Once activated by the precharge signal, the integrator 206 begins integrating the data by ramping from a zero differential (precharged) value to a maximum differential output value. When the data transitions to the opposite polarity during the second edge transition 306, such as indicated at 314, the integrator begins ramping the output differential voltage in the

opposite direction. The sense edge triggers sampling of the integrator output by the second direct sampler 210. If the clock and data reflect the desired 90 degree offset, the integrator output value will be very near zero at the activation of sense, and the second direct sampler will end up sampling at the very edge of the integrator eye, possibly sampling a logic 1 or 0. A balanced integration interval is illustrated by the on-time integrator output waveform 316.

[0017] Further referring to Figure 3, should the clock and data relationship be skewed, such that the clock is earlier in time than desired (shown by the early clock waveform 318), then the data sampler samples earlier in the first valid data range 304 (potentially overlapping into the first edge transition region 305). The integrator also correspondingly begins integrating earlier and continues increasing the integrator value until changing direction at the second data transition 306, at time 314. The integrator then decreases the integrator value until resetting. Just prior to reset, and responsive to the sense signal at 320, the integrator output is still relatively high, such that the sampled value indicates the output level of the first bit, as shown in the integrator output waveform 322.

[0018] Conversely, if the clock and data deskew such that the clock reflects a “late” relationship with respect to the first valid data region 304 (as shown by the late clock waveform 324), the data sampler 204 samples later in the valid data range (potentially overlapping into the second edge transition region 306), and the integrator 206 ramps up a positive integration value for a shorter duration, beginning a decrease at 326 when the data transition occurs. At 328, the continued decrease in the differential integration output value goes negative in magnitude. Consequently, when the second direct sampler 210 samples the integration output, the value is a logic 0, as shown in the integration output waveform 330.

[0019] The sampled integration values (or edge sampling values) may be accumulated over time and compared to the sampled data values to indicate whether the data and clock signals maintain a desired phase relationship. Alternately, the comparisons may be done

directly in 'real time' and the value of the comparisons accumulated or averaged in order to create an 'early' or 'late' indication. For example, if multiple data samples indicate logic 1s, and multiple integrations (edge values) indicate logic 1s, then the clock can be assumed to be early relative to the data. Similarly, multiple disagreeing data and integration values may be assumed to indicate a late clock. In one embodiment, this information may be fed back to the timing control circuitry 114 (Figure 1) to pre-skew the clock and data phase relationship in the desired manner to eliminate the receiver-side skew and effect a more precise quadrature relationship at the receiver. While a one-to-one correspondence between a data pin and a clock pin is shown and described above, yet other embodiments may employ a number of clock links less than the number of data links. Further, in a parallel bus environment where relative link timings may be similar, one or more data/edge sampling pins may share timing information with other data/edge pins. Sharing timing information in this fashion may enable significant power savings at the receiver. Other embodiments may employ even fewer pin resources by embedding the timing information with the data, and utilizing appropriate clock and data recovery techniques. Further, a variety of ways exist to utilize the phase data generated by edge and data receivers that are well-known to those having ordinary skill in the art, and warrant no further detail herein.

[0020] Figure 4 illustrates another embodiment of a data and edge receiver circuit, generally designated 400. Although structurally similar to the sampling circuit 200 of Figure 2, the integrating and non-integrating circuit roles for the data and edge receivers are reversed. In this respect, the sampling circuit 400 employs an integrating data receiver circuit 402 as the data receiver, while a first direct sampler (a non-integrating receiver) 404 takes the role of the edge receiver. The integrating receiver circuit 402 includes an integrator 406 having an output coupled to a second direct sampler 410. One embodiment of the integrator 406 takes the form of a windowing integrator, in that the integration interval may be varied by adjusting delays associated with the precharge and sense signals. This allows framing the integration interval

over an optimal data sampling region. Further detail concerning windowing integrators may be found, for instance, in U.S. Patent No. 6,396,329.

[0021] Further referring to Figure 4, the first and second direct samplers 404 and 410 include clock inputs responsive to rising edges of clock signals SENSE and CLK propagating along clock paths 414 and 416, respectively. The integrator 406, in contrast, employs a clock input PRECHARGE_B where a low input will serve to precharge-null the integrator's differential output from the portion of the clock signal propagating along path 412.

[0022] One of the fundamental differences between the receiver circuit 400 of Figure 4, and the receiver circuit 200 of Figure 2 involves the phase relationship between the clock and data signals. Since the integrator carries on the data receiving role for the circuit 400, and incurs an inherent 90 degree delay in its output, a 90 degree delay in the clock is not used when receiving the data with optimum timing margin. Thus in this embodiment the clock accompanies the data in-phase and is not centered within the data bit.

[0023] With continued reference to Figure 4, the receiver circuit 400 may optionally employ one or more of a variety of delay circuits 418, 420, and 422 disposed in the respective clock paths 412, 414, and 416 to compensate for delays incurred by the data signals. For instance, delay circuit 418 delays the precharge_B portion of the clock signal by a time interval sufficient to compensate for the data delay through an optional amplifier and a desired precharge-specific window delay to affect where the integrator initiates its integration operation. Delay circuit 420 performs similarly by applying a variable delay to the sense portion of the clock signal. Typically when windowing the integration window down from a full 1-UI setting precharge delay 418 is increased relative to sense delay 420. The edge clock delay circuit 422 delays the clock signal by half the delay applied to the precharge signal by delay circuit 418. This is performed to support the window integrating function while still allowing the first direct (data) sampler to sample in the middle of the transition region. The

delay circuits may take the form of delay lines, verniers, FIFO's or the like in order to impart the desired delay. In some embodiments the delay of sense delay block 422 is set to be half of that of precharge delay 418 in order to compensate for the relative positions of the window within the eye vs. the transition region as seen by sampler 404.

[0024] Figure 5 illustrates a timing diagram showing the operation of data and edge sampling circuit 400 in a DDR environment. The timing diagram is similar to the diagram illustrated in Figure 3, with the X-axis representing time, and the Y-axis representing voltage levels such as logic signal levels and/or analog voltage levels. A variety of data, clock and integrator output waveforms are shown along the same time scale. The data signal of interest in the data waveform 502 corresponds to an "even" data bit accompanied by an in phase transmit clock signal 504.

[0025] With continued reference to Figure 5, operation of the data and edge receiving circuit 400 generally involves receiving the data and clock signals that are transmitted from a first integrated circuit transmitter, such as the IC 102 shown in Figure 1. The data 502 and transmit clock 504 waveforms illustrate the in phase relationship between the signals, where the transmit clock edges 504 are substantially aligned with the centers of the data transition regions, at 514 and 516.

[0026] Further referring to Figure 5, in one embodiment the data receiver (the integrator circuit 402) detects the data in a windowing manner. Generally, windowing involves pre-adjusting the incoming transmit clock waveform on the transmit IC such that the firing of the sense signal, shown as waveform 506, is time-aligned with the right-most side of the valid data window or left-most side of the transition region (represented by phantom line 518). Usually, the data is delayed by a value in order to set this sense timing. The incoming clock waveform is then split, with the precharge signal being controlled with its own delay circuit 418. While Figure 5 illustrates edge receiving and delays with reference to the right-side transition region

516 of the data bit, the sampler and associated timing could just as well be referenced to the left side of the data bit with minor changes, depending on the CDR logic.

[0027] As the integrator 406 receives the data signal from along path 407, the prechargeB signal, at 508, is delayed by the precharge delay line 418 a predetermined timing interval to frame the start of the integration, shown by the integration output waveform, at 510. The sense signal also undergoes a delay (controlled by delay line 420), that together with the precharge delay, defines the width of the uncertainty region to frame the end of the integration interval, and triggers the second direct sampler 410 to sample the integrator output.

[0028] While the data receiver 402 carries out its integrating function, the edge receiver (the first direct sampler 404) responds to the rising edge 514 of the edge clock waveform 516, optionally delayed by half the delay applied to the precharge signal by delay block 422, to take an edge sample within the transition region of the data eye. The respective data and edge values may then be compared, evaluated, and employed in various ways to effect phase corrections between the data and clock signals as was previously discussed.

[0029] The edge and data receivers described above provide significant power savings and pin efficiency, primarily as they eliminate the need for 90-degree clocks to be used directly to generate edge and data information. Additionally, optional CDR logic may be employed to selectively disable the edge sampler when not in use. This is especially convenient in certain mesochronous systems where the phase information is often only periodically updated. Moreover, because a separate 90 degree clock is unnecessary, the use of power-hungry PLLs may be minimized on the receive-side IC. Additionally, eliminating the second 90 degree clock corresponds to a direct reduction in pin count for the IC. Finally, with PLLs eliminated or minimized, the receive-side IC clocks can more rapidly be enabled and disabled, allowing for more effective duty-cycling of the link's active and power-savings states.

[0030] It should be noted that the various circuits disclosed herein may be described using computer aided design tools and expressed (or represented), as data and/or instructions embodied in various computer-readable media, in terms of their behavioral, register transfer, logic component, transistor, layout geometries, and/or other characteristics. Formats of files and other objects in which such circuit expressions may be implemented include, but are not limited to, formats supporting behavioral languages such as C, Verilog, and VHDL, formats supporting register level description languages like RTL, and formats supporting geometry description languages such as GDSII, GDSIII, GDSIV, CIF, MEBES and any other suitable formats and languages. Computer-readable media in which such formatted data and/or instructions may be embodied include, but are not limited to, non-volatile storage media in various forms (e.g., optical, magnetic or semiconductor storage media) and carrier waves that may be used to transfer such formatted data and/or instructions through wireless, optical, or wired signaling media or any combination thereof. Examples of transfers of such formatted data and/or instructions by carrier waves include, but are not limited to, transfers (uploads, downloads, e-mail, etc.) over the Internet and/or other computer networks via one or more data transfer protocols (e.g., HTTP, FTP, SMTP, etc.).

[0031] When received within a computer system via one or more computer-readable media, such data and/or instruction-based expressions of the above described circuits may be processed by a processing entity (e.g., one or more processors) within the computer system in conjunction with execution of one or more other computer programs including, without limitation, net-list generation programs, place and route programs and the like, to generate a representation or image of a physical manifestation of such circuits. Such representation or image may thereafter be used in device fabrication, for example, by enabling generation of one or more masks that are used to form various components of the circuits in a device fabrication process.

[0032] In the foregoing description and in the accompanying drawings, specific terminology and drawing symbols have been set forth to provide a thorough understanding of the present invention. In some instances, the terminology and symbols may imply specific details that are not required to practice the invention. For example, any of the specific numbers of bits, signal path widths, signaling or operating frequencies, component circuits or devices and the like may be different from those described above in alternative embodiments. Also, the interconnection between circuit elements or circuit blocks shown or described as multi-conductor signal links may alternatively be single-conductor signal links, and single conductor signal links may alternatively be multi-conductor signal links. Signals and signaling paths shown or described as being single-ended may also be differential, and vice-versa. Similarly, signals described or depicted as having active-high or active-low logic levels may have opposite logic levels in alternative embodiments. Component circuitry within integrated circuit devices may be implemented using metal oxide semiconductor (MOS) technology, bipolar technology or any other technology in which logical and analog circuits may be implemented. With respect to terminology, a signal is said to be “asserted” when the signal is driven to a low or high logic state (or charged to a high logic state or discharged to a low logic state) to indicate a particular condition. Conversely, a signal is said to be “deasserted” to indicate that the signal is driven (or charged or discharged) to a state other than the asserted state (including a high or low logic state, or the floating state that may occur when the signal driving circuit is transitioned to a high impedance condition, such as an open drain or open collector condition). A signal driving circuit is said to “output” a signal to a signal receiving circuit when the signal driving circuit asserts (or deasserts, if explicitly stated or indicated by context) the signal on a signal line coupled between the signal driving and signal receiving circuits. A signal line is said to be “activated” when a signal is asserted on the signal line, and “deactivated” when the signal is deasserted. Additionally, the prefix symbol “/” attached to signal names indicates that the signal is an active low signal (i.e., the asserted state

is a logic low state). A line over a signal name (e.g., '< signal name >') is also used to indicate an active low signal. The term "coupled" is used herein to express a direct connection as well as a connection through one or more intervening circuits or structures. Integrated circuit device "programming" may include, for example and without limitation, loading a control value into a register or other storage circuit within the device in response to a host instruction and thus controlling an operational aspect of the device, establishing a device configuration or controlling an operational aspect of the device through a one-time programming operation (e.g., blowing fuses within a configuration circuit during device production), and/or connecting one or more selected pins or other contact structures of the device to reference voltage lines (also referred to as strapping) to establish a particular device configuration or operation aspect of the device. The term "exemplary" is used to express an example, not a preference or requirement.

[0033] While the invention has been described with reference to specific embodiments thereof, it will be evident that various modifications and changes may be made thereto without departing from the broader spirit and scope of the invention. For example, features or aspects of any of the embodiments may be applied, at least where practicable, in combination with any other of the embodiments or in place of counterpart features or aspects thereof. Accordingly, the specification and drawings are to be regarded in an illustrative rather than a restrictive sense.

CLAIMS

1. An integrated circuit receiver comprising:
 - a data receiving circuit responsive to a timing signal to detect a data signal;
 - an edge receiving circuit responsive to the timing signal to detect a transition of the data signal; and
 - wherein one of the data or edge receiving circuits comprises an integrating receiver circuit, and the other of the data or edge receiving circuits comprises a sampling receiver circuit.

2. The integrated circuit receiver according to claim 1 wherein:
 - the data receiving circuit detects a data value in a valid data region of the data signal; and
 - the edge receiving circuit detects an edge value in a transition region of the data signal.

3. The integrated circuit receiver according to claims 1 or 2 wherein the timing signal includes a precharge interval and a sense interval and wherein:
 - the integrating receiver circuit includes a saturating integrator responsive to the precharge interval and a second sampling receiver circuit coupled to the saturating integrator and responsive to the sense interval.

4. The integrated circuit receiver according to claim 3 wherein:
 - the timing signal accompanies the data signal in a quadrature relationship.

5. The integrated circuit receiver according to claims 3 or 4 wherein:
 - the sampling receiver circuit includes a first setup and hold parameter; and
 - the second sampling receiver circuit includes a second setup and hold parameter that substantially matches the first setup and hold parameter.
6. The integrated circuit receiver according to any of claims 3-5 and further including:
 - logic to selectively disable the saturating integrator.
7. The integrated circuit receiver according to claims 1-6 wherein the edge receiving circuit generates early/late information based on detecting a transition of the data signal, the early/late information for use by a timing control circuit to adjust the relative phases of the timing signal and the data symbol.
8. The integrated circuit receiver according to claim 7 wherein the timing control circuit is disposed in the integrated circuit receiver.
9. The integrated circuit receiver according to claims 1 or 2 wherein the timing signal includes a precharge interval and a sense interval, and wherein:
 - the integrating receiver circuit includes a windowed integrator responsive to a selectively delayed precharge interval and a selectively delayed sense interval.
10. The integrated circuit receiver according to claim 9 wherein the sampling receiver circuit is responsive to a delayed timing signal.
11. The integrated circuit receiver according to claim 10 wherein the delayed timing signal is based on the delayed precharge interval.

12. The integrated circuit receiver according to any of claims 9-11 wherein the timing signal accompanies the data signal in an in-phase relationship.
13. The integrated circuit receiver according to any of claims 1-12 wherein the timing signal comprises a clock signal.
14. The integrated circuit receiver according to any of claims 1-12 wherein the timing signal comprises a strobe signal.
15. A method of operation in an integrated circuit receiver, the method comprising:
 - receiving a data signal having a valid data region and a transition region;
 - receiving a timing signal;
 - detecting a data value in the valid data region in response to the timing signal;
 - detecting an edge value in the transition region in response to the timing signal to generate early/late information;
 - wherein one of detecting a data value in the valid data region or detecting an edge value in the transition region comprises integrating in response to the timing signal.
16. The method according to claim 15 wherein the data signal and the timing signal are received in a quadrature relationship, and wherein detecting an edge value in the transition region comprises:
 - integrating over an interval corresponding to respective precharge and sense portions of the timing signal;
 - generating an integrated output; and
 - sampling the integrated output to generate the early/late information.

17. The method according to claims 15 or 16 wherein detecting a data value in the valid data region comprises directly sampling the valid data region.

18. The method according to any of claims 15-17 wherein the data signal and timing signal are received in-phase, and wherein detecting a data value in the valid data region comprises:
 - integrating over an interval corresponding to respective precharge and sense portions of the timing signal;
 - generating an integrated output; and
 - sampling the integrated output to generate the early/late information.

19. The method according to any of claims 15-18 wherein detecting an edge value in the transition region comprises directly sampling the transition region.

20. The method according to claim 15 wherein integrating comprises:
 - windowing an integration interval by delaying at least one of a precharge portion of the timing signal or a sense portion of the timing signal.

21. The method according to claim 20 wherein:
 - delaying at least one of a precharge portion of the timing signal or a sense portion of the timing signal comprises delaying the detecting of the edge value in the transition region by half the delay of the precharge portion of the timing signal.

22. A signaling system comprising:
- a first integrated circuit device including a transmitter circuit to transmit a data signal and an accompanying timing signal;
 - a second integrated circuit device including a receiver circuit to receive the data signal and timing signal, the receiver circuit comprising
 - a first receiving circuit responsive to a timing signal to detect a valid data region of a data signal;
 - a second receiving circuit responsive to the timing signal to detect a transition region associated with the data signal; and
 - wherein one of the first or second receiving circuits comprises an integrating receiver circuit, and the other of the first or second receiver circuits comprises a sampling receiver circuit.
23. The signaling system according to claim 22 wherein the transmitter circuit transmits the timing signal and the data signal to the receiver circuit in quadrature, and wherein:
- the integrating receiver circuit includes a saturating integrator responsive to a precharge interval of the timing signal and a third sampler circuit coupled to the integrator and responsive to a sense interval of the timing signal.
24. The signaling system according to claim 22 wherein the transmitter circuit transmits the timing and data signals in phase, and wherein:
- the integrating receiver circuit includes a windowed integrator responsive to adjustable precharge and sense portions of the timing signal.

25. The signaling system according to any of claims 22-24 and further including:
 - a backchannel for communicating early/late information from the second integrated circuit to the first integrated circuit.

26. The signaling system according to claim 25 and further including:
 - timing control logic to adjust the relative phases of the timing signal and the data signal based on the early/late information.

FIG. 1

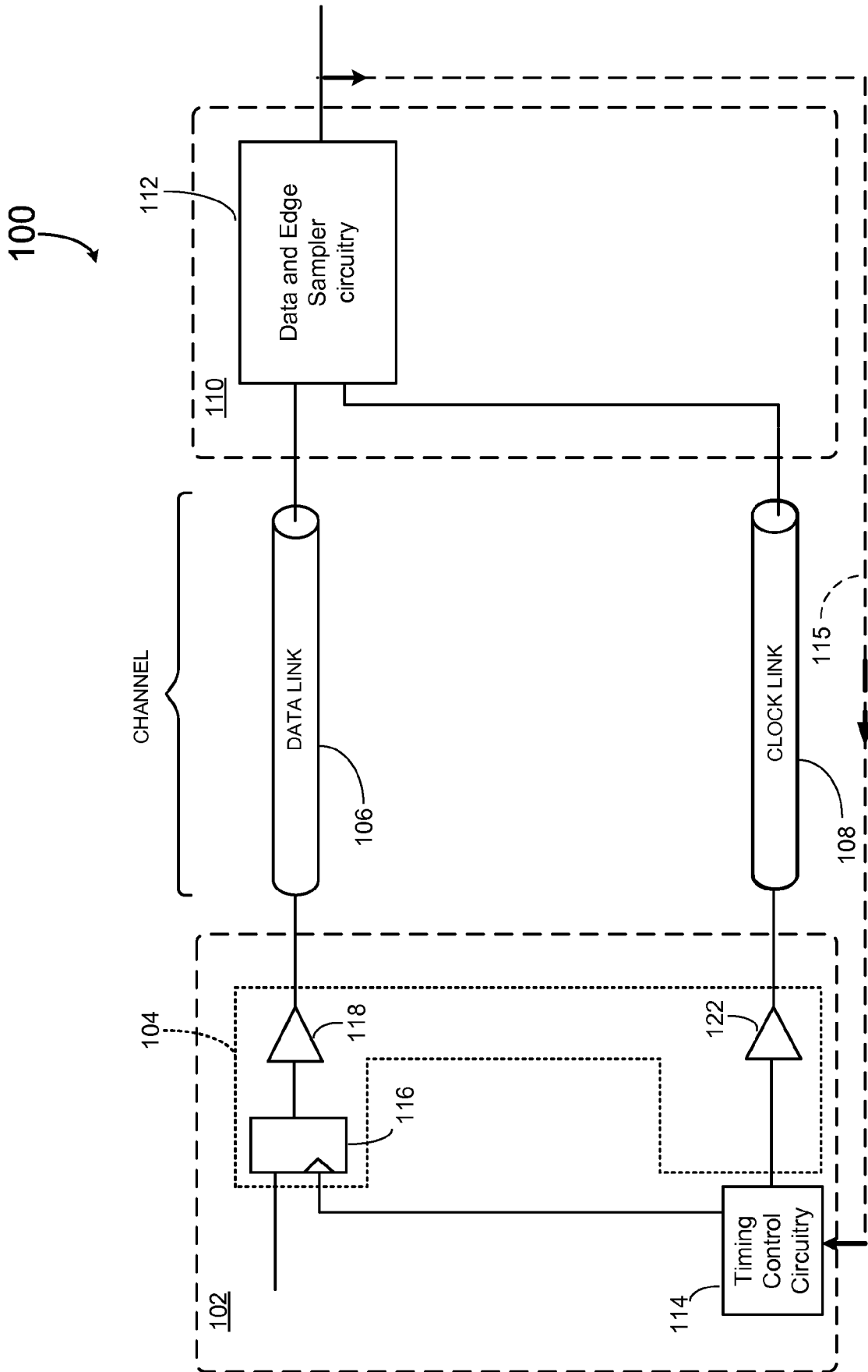


FIG. 2

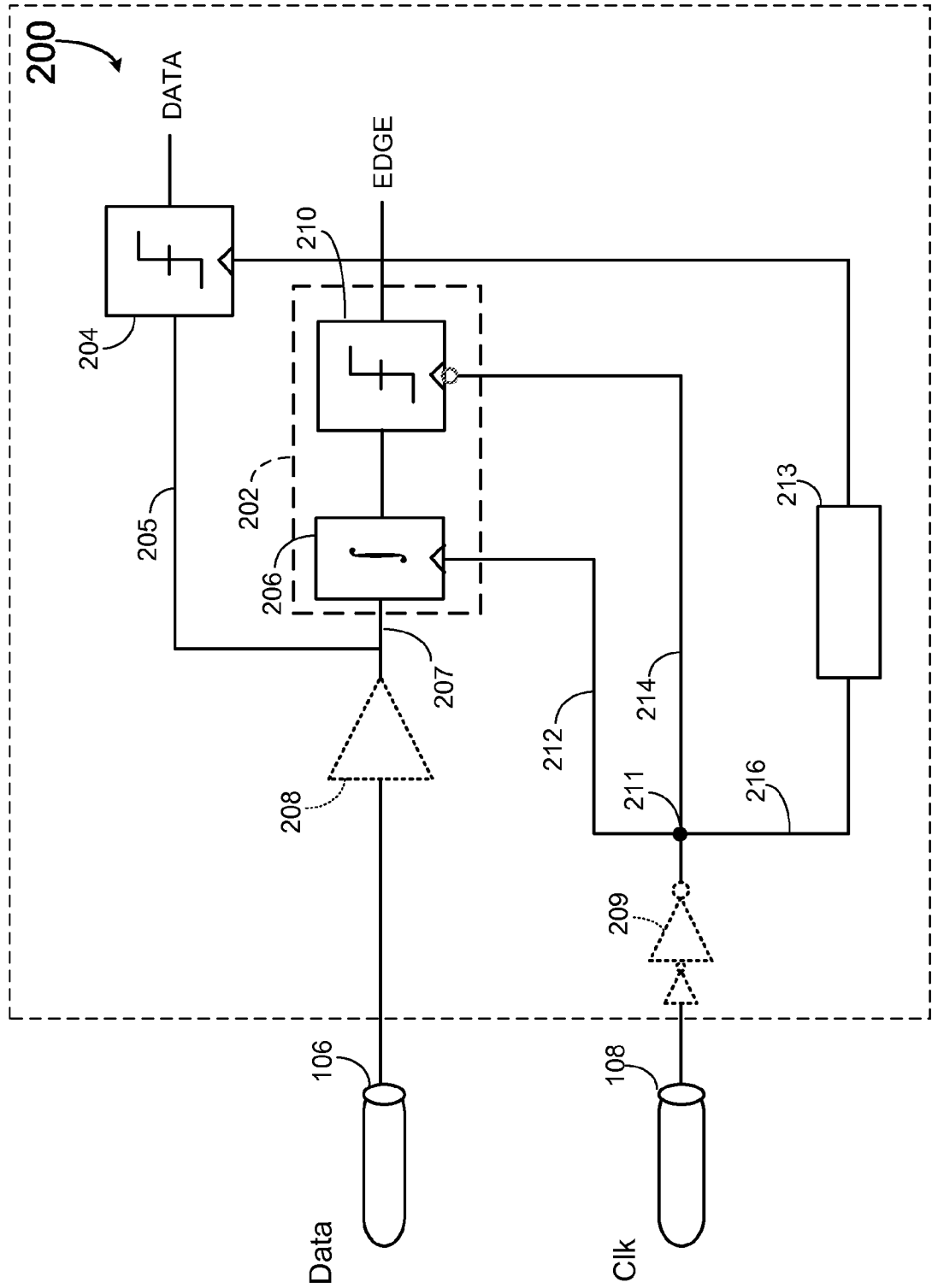


Fig. 3

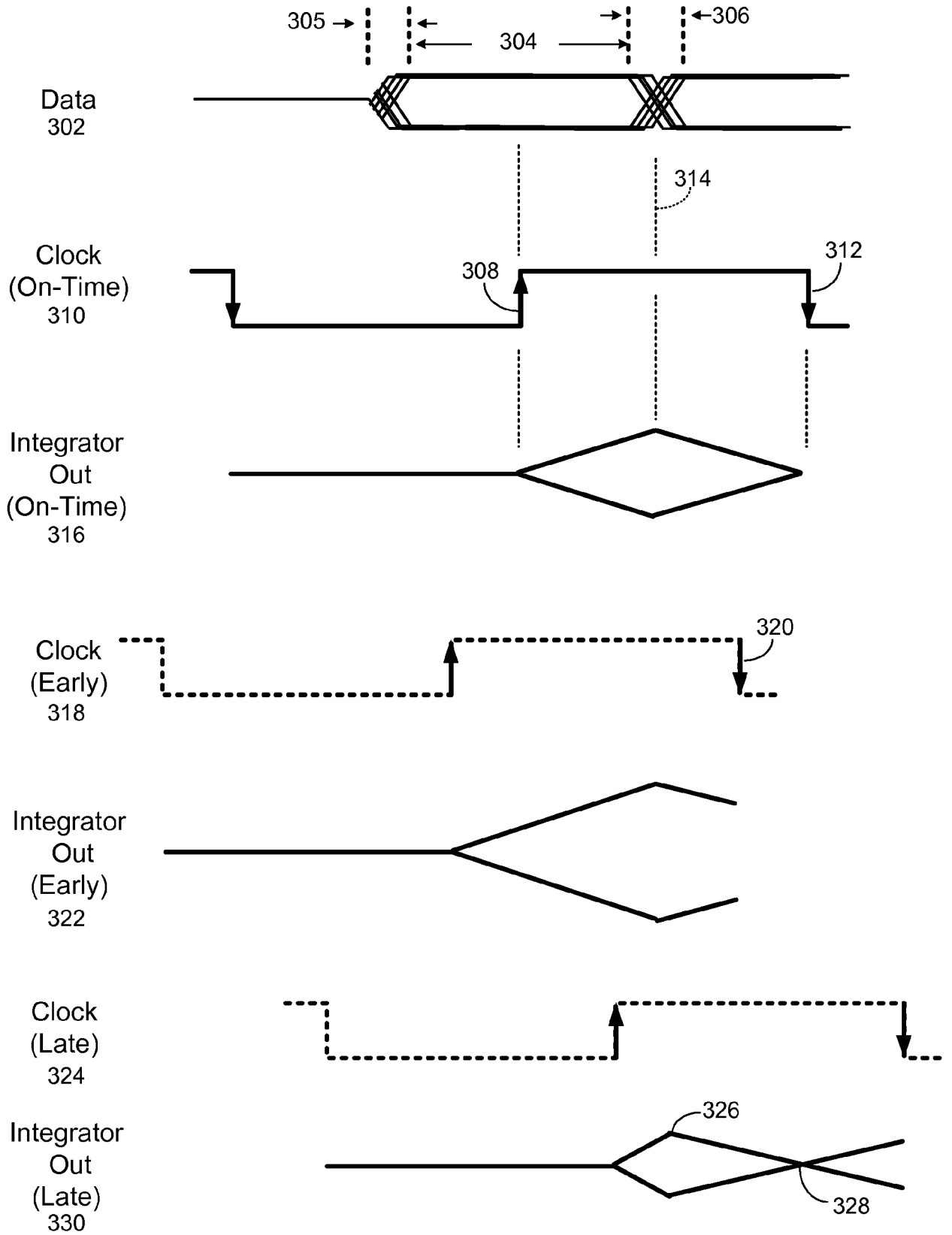


Fig. 4

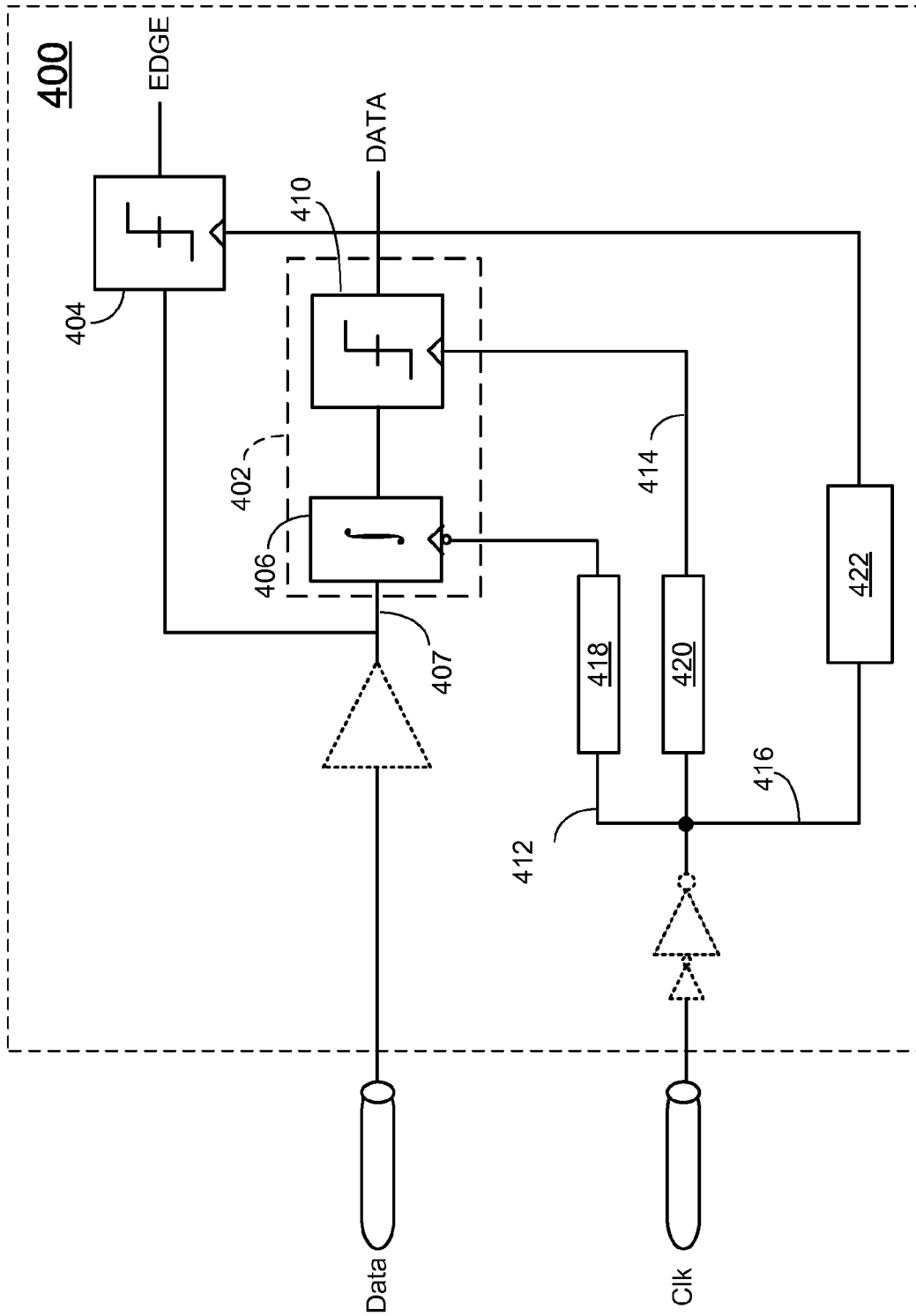
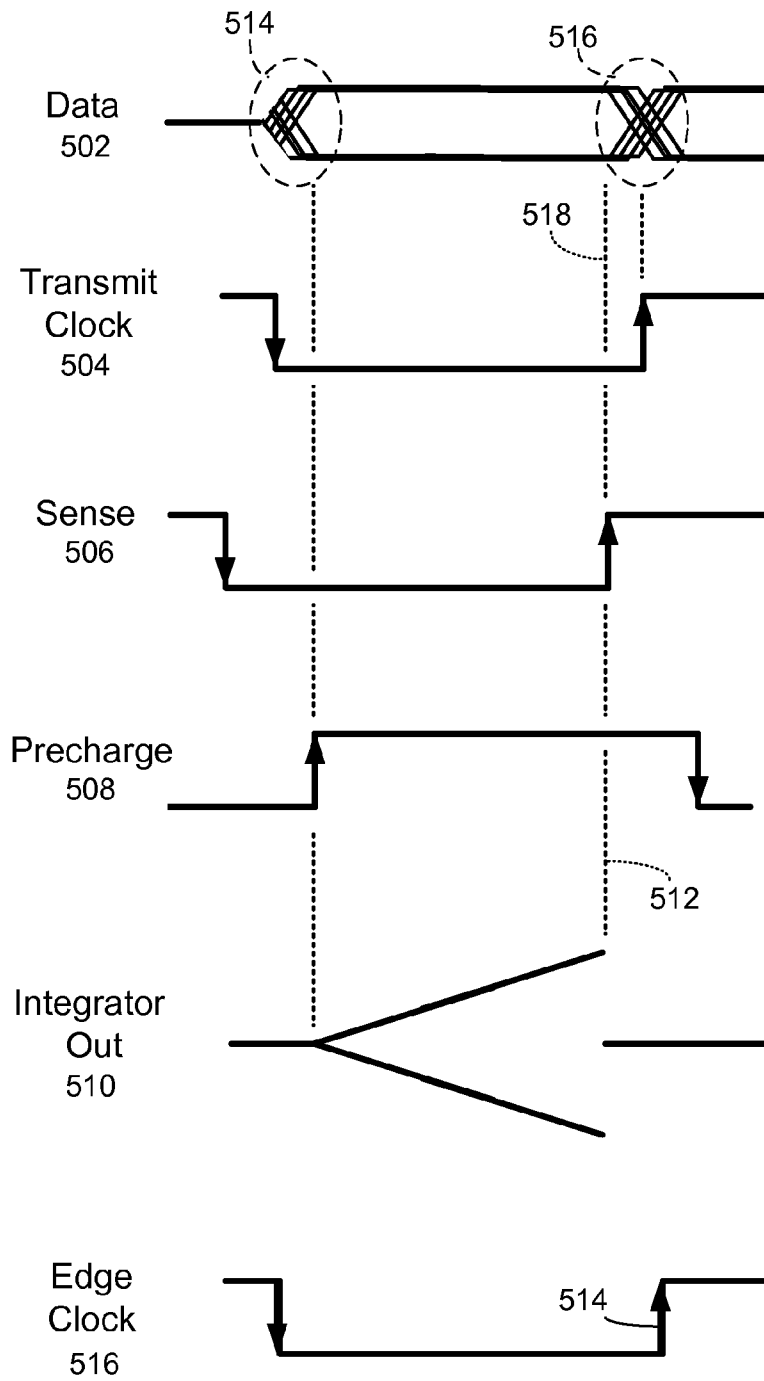


Fig. 5



INTERNATIONAL SEARCH REPORT

International application No
PCT/US2011/032338

A. CLASSIFICATION OF SUBJECT MATTER
INV. H04L7/033
ADD.
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED
Minimum documentation searched (classification system followed by classification symbols)
H04L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2004/096013 A1 (LATURELL DONALD R [US] ET AL) 20 May 2004 (2004-05-20) abstract paragraph [0020] - paragraph [0068] figures 1-4,6,7	1-6,15, 22,23
A	US 5 309 483 A (OLIBONI MARK L [US] ET AL) 3 May 1994 (1994-05-03) abstract column 2, line 47 - column 4, line 28 figure 2	1-6,15, 22,23
A	US 5 127 026 A (KELLY RICHARD J [US] ET AL) 30 June 1992 (1992-06-30) abstract column 3, line 7 - column 5, line 17 figures 1,2	1-6,15, 22,23

Further documents are listed in the continuation of Box C.

See patent family annex.

* Special categories of cited documents :

- "A" document defining the general state of the art which is not considered to be of particular relevance
- "E" earlier document but published on or after the international filing date
- "L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
- "O" document referring to an oral disclosure, use, exhibition or other means
- "P" document published prior to the international filing date but later than the priority date claimed

- "T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
- "X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
- "Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.
- "&" document member of the same patent family

Date of the actual completion of the international search 5 August 2011	Date of mailing of the international search report 19/10/2011
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Name and mailing address of the ISA/ European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Authorized officer Moser, Jochen
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INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2011/032338

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

see additional sheet

1. As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.
2. As all searchable claims could be searched without effort justifying an additional fees, this Authority did not invite payment of additional fees.
3. As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:
4. No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

3-6, 23(completely); 1, 2, 15, 22(partially)

Remark on Protest

- The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.
- The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.
- No protest accompanied the payment of additional search fees.

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/US2011/032338

Patent document cited in search report	Publication date	Patent family member(s)	Publication date	
US 2004096013	A1	20-05-2004	US 2007147566 A1	28-06-2007
US 5309483	A	03-05-1994	NONE	
US 5127026	A	30-06-1992	NONE	

FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

This International Searching Authority found multiple (groups of) inventions in this international application, as follows:

1. claims: 3-6, 23(completely); 1, 2, 15, 22(partially)
saturating integrator

2. claims: 9-12, 20, 21, 24(completely); 1, 2, 15, 22(partially)
windowed integrator

3. claims: 7, 8, 25, 26(completely); 1, 2, 15, 22(partially)
generating early/late information for phase adjustment

4. claims: 13(completely); 1, 2, 15, 22(partially)
clock signal as timing signal

5. claims: 14(completely); 1, 2, 15, 22(partially)
strobe signal as timing signal

6. claims: 16, 17(completely); 1, 2, 15, 22(partially)
integrated edge information, directly sampled data
information

7. claims: 18, 19(completely); 1, 2, 15, 22(partially)
intgrated data information, directly sampled edge
information
