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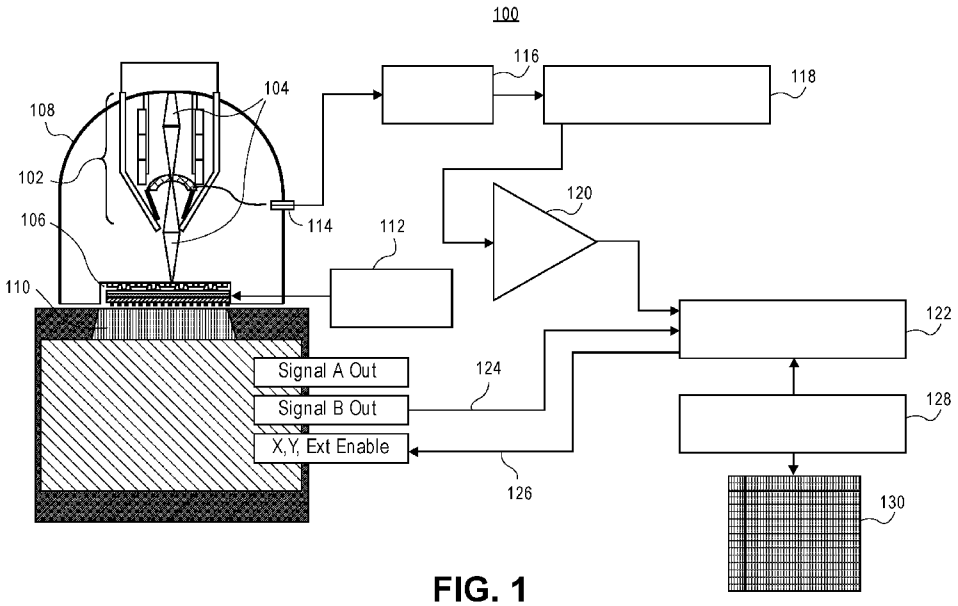


FIG. 1

(57) Abstract: Apparatuses and methodologies for electron beam probing for chip debug and fault isolation are described. In an example, a method of electron-beam signal image mapping (ESIM) includes, scanning an electron beam over an area on a chip containing an integrated circuit structure, toggling a gate electrode of the integrated circuit structure at a frequency, amplifying a secondary electron signal and sending the amplified secondary electron signal to a lock-in amplifier or spectrum analyzer tuned to the frequency, feeding an output of the lock-in amplifier or spectrum analyzer into a scan control unit that rasters over the area, and illuminating a portion of the integrated circuit structure with the electron beam to modulate the secondary electron signal.

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ELECTRON BEAM PROBING FOR CHIP DEBUG AND FAULT ISOLATION

TECHNICAL FIELD

Embodiments of the disclosure are in the field of defect analysis and, in particular, apparatuses and methodologies for electron beam probing for chip debug and fault isolation.

BACKGROUND

For the past several decades, the scaling of features in integrated circuits has been a driving force behind an ever-growing semiconductor industry. Scaling to smaller and smaller features enables increased densities of functional units on the limited real estate of semiconductor chips.

Electron beam (E-beam) probers were widely used in the semiconductor industry over 15 years ago. Optical probers replaced the electron beam prober. However the resolution of the optical tools is at least an order of magnitude worse than the electron beam offered by current generation of scanning electron microscopes (SEMs).

Product debug, yield improvement and reliability improvement all depend on the capability and speed of isolating the failing circuit and device. Current techniques do not provide adequate capability due to device scaling for the 7nm and 5 nm nodes.

Thus, improvements are needed in the area of apparatuses and methodologies for electron beam probing for chip debug and fault isolation.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a schematic of an e-beam prober with electron-beam signal image mapping (ESIM) capability, in accordance with an embodiment of the present disclosure.

Figure 2 includes (a) an exemplary scanning electron microscope (SEM) image and (b) an exemplary electron-beam signal image mapping (ESIM) image from an e-beam prober such as an e-beam prober of Figure 1, in accordance with an embodiment of the present disclosure.

Figure 3 is a schematic of an e-beam prober with e-beam logic state imaging (ELSI) capability, in accordance with an embodiment of the present disclosure.

Figure 4 includes plots and corresponding circuit schematics representing possible outcomes from an analysis performed on an e-beam prober such as e-beam prober of Figure 3, in accordance with an embodiment of the present disclosure.

Figure 5 is a schematic of an e-beam prober with optical-electrical fault mapping (OEFM) capability, in accordance with an embodiment of the present disclosure.

Figure 6 includes (a) a determination schematic and (b) corresponding location

determination schematic determined from plots and representing possible outcomes from an analysis performed on an e-beam prober such as an e-beam prober of Figure 5, in accordance with an embodiment of the present disclosure.

Figure 7 is a cross-sectional schematic representation of an e-beam column of an electron beam lithography apparatus.

Figure 8 illustrates a plan view and corresponding cross-sectional view of a previous layer metallization structure, in accordance with an embodiment of the present disclosure.

Figure 9A illustrates a cross-sectional view of a non-planar semiconductor device having fins, in accordance with an embodiment of the present disclosure.

Figure 9B illustrates a plan view taken along the a-a' axis of the semiconductor device of Figure 9A, in accordance with an embodiment of the present disclosure.

Figure 10 illustrates a computing device in accordance with one implementation of the disclosure.

Figure 11 illustrates a block diagram of an exemplary computer system, in accordance with an embodiment of the present disclosure.

Figure 12 is an interposer implementing one or more embodiments of the disclosure.

Figure 13 is a computing device built in accordance with an embodiment of the disclosure.

DESCRIPTION OF THE EMBODIMENTS

Apparatuses and methodologies for electron beam probing for chip debug and fault isolation are described. In the following description, numerous specific details are set forth, such as specific tooling and integration regimes, in order to provide a thorough understanding of embodiments of the present disclosure. It will be apparent to one skilled in the art that embodiments of the present disclosure may be practiced without these specific details. In other instances, well-known features are not described in detail in order to not unnecessarily obscure embodiments of the present disclosure. Furthermore, it is to be understood that the various embodiments shown in the Figures are illustrative representations and are not necessarily drawn to scale. In some cases, various operations will be described as multiple discrete operations, in turn, in a manner that is most helpful in understanding the present disclosure, however, the order of description should not be construed to imply that these operations are necessarily order dependent. In particular, these operations need not be performed in the order of presentation.

One or more embodiments described herein are directed to electron beam probing for chip debug and fault isolation. In accordance with an embodiment of the present disclosure, apparatuses and methods described herein provide superior capability to resolve ever smaller

features of integrated circuit devices and provide a more direct way to sense and modulate the integrated circuit devices of interest. Embodiments may be applicable to ion beam or any charged particle beam, applicable in in outer space device debug and fault isolation in a vacuum environment, and/or applicable to package and 3D structure device debug and fault isolation, or any other electronic device that could be operated in a vacuum.

To provide context, for fin-FET devices, the silicon consists of individual narrow fins instead of state-of-the-art silicon diffusion areas. The use of silicon fins make it challenging for current techniques to resolve. The ability to isolate a defect or malfunction to the individual fin level can provide an enormous advantage in the speed of process development, as well as in yield improvement and reliability improvement. Such capabilities and speed may translate into faster time to market, better profit margin and higher product quality.

Fault isolation (FI) and failure analysis (FA) are critical parts of (1) product design validation and debug, (2) process development, (3) production yield improvement, (4) reliability testing and (5) product certification and product reliability qualification (PRQ). The ability to identify and isolate the failing circuits and devices often defines the success or failure of a product launch.

Currently FI and FA is achieved by using optical tools such as Laser Assisted Device Alternation (LADA), Thermal Induced Voltage Alteration (TIVA), or Laser Voltage Probe (LVP)/Laser Timing Module (LTM) to locate the failing devices or circuit. The resolution of the optical approach may be limited by the optical system resolution in IR range where silicon is transparent since the signal needs to go through the silicon to reach the devices, or come from the device to reach the imaging system. The state-of-the-art resolution of such optical systems is about 240 nanometers using a 3.0 N.A. solid immersion lens. Electron beam approaches provide better resolution in imaging but the beam modulation volume is typically larger than the beam size due to the charging effect and electron scattering. The sensing of an integrated circuit structure for all of the above techniques is indirectly through the reflectance change or heating effect or charge effect from the beam used.

To provide further context, conventional e-beam probers are capable of imaging an integrated circuit structure state using voltage contrast, measuring the voltage on the metal traces and obtaining waveforms on the signal lines, and offering adequate spatial resolution. However, conventional e-beam probers have mainly been used for front side probing and the resolution is typically at best 100 nanometers. The conventional e-beam probers were replaced by optical techniques because the flip chip packaging technology that became widely used does not provide access to the metal lines that the previous generation of e-beam probers rely on for the analysis.

In accordance with one or more embodiments of the present disclosure, e-beam probing

is applied from either the backside (e.g., from the silicon side) or front side of a device or interconnects after special sample preparation that exposes silicon fins or diffusion or metal interconnects. In an embodiment, e-beam probing described herein offers advantages that conventional generation e-beam prober were not capable of. Embodiments may be directed to one or more of the following approaches or techniques: (1) electron-beam signal image mapping (ESIM), (2) e-beam logic state imaging (ELSI), (3) optical-electrical fault mapping (OEFM), or (4) e-beam device perturbation (EDP) for critical timing analysis.

In a first aspect, electron-beam signal image mapping (ESIM) is described. In an embodiment, using an ESIM approach, an electron beam is scanned over an area containing an integrated circuit structure or device of interest. A gate electrode of the device of interest is toggled at a specific frequency. A secondary electron signal is amplified and then sent to a lock-in amplifier or spectrum analyzer tuned to the specific frequency. The output of the lock-in amplifier or spectrum analyzer is fed into a scan control unit that rasters over the area. When the electron beam illuminates part of circuit element such as a metal line or silicon under a device, the secondary electron emission is modulated by the electrical signal. This effect, which is due to active voltage contrast, produces a modulating signal at the secondary electron detector which is then routed to the lock-in amplifier. In an embodiment, the location where there is signal from the lock-in amplifier or spectrum analyzer indicates the position of the device carrying the oscillating signal. Devices that toggle show the contrast against the background, allowing for mapping of devices that toggle at the driving frequency. In an embodiment, by comparing with a computer assisted design (CAD) layout, all defective devices can be found if the devices are operated at the given frequency but do not show the modulated secondary electron signal.

It is to be appreciated that conventional electron beam prober offers static voltage contrast by putting integrated circuit structures of devices in a certain state and performing voltage contrast imaging. A conventional electron beam prober also offers stroboscopic waveform acquisition to collect waveforms on specific nodes. However, in accordance with an embodiment of the present disclosure, ESIM is used to detect a dynamic response of integrated circuit structures or devices and to provide a map of the integrated circuit structures or devices where the signal is observed. It is to be appreciated that although optical tools could possibly provide signal image mapping (SMI) function using a laser beam but the resolution would be an order of magnitude lower poorer, as described above.

Figure 1 is a schematic of an e-beam prober 100 with electron-beam signal image mapping (ESIM) capability, in accordance with an embodiment of the present disclosure. Referring to Figure 1, the e-beam prober 100 includes an e-beam column 102 (such as a scanning electron microscope (SEM) column), for delivering a beam 104 to a device under test

(DUT) 106. The e-beam column 102, or at least a portion of the e-beam column 102 may be housed in a chamber 108, and the device under test (DUT) 106 may be supported by a stage 110, as is depicted.

In the e-beam prober 100, a signal generator 112 is coupled to the DUT 106. A detector 114 which is in the path of beam 104 or by the side of the e-beam column 102 is coupled to a sensing module 116. The sensing module 116 is coupled to a lock-in amplifier or spectrum analyzer 118 which is coupled to an operation amplifier 120. A scan module 122 is coupled to the operation amplifier 120 and can receive Scanning Electron Microscope (SEM) image signal 124 or send external x-y scan control signals 126 to the control board of electron column 102. A computer controller 128 can produce scanning electron microscope (SEM) images or electron-beam signal image mapping (ESIM) images 130.

Figure 2 includes (a) an exemplary scanning electron microscope (SEM) image and (b) an exemplary signal image mapping (SMI) image from an e-beam prober such as e-beam prober 100 of Figure 1, in accordance with an embodiment of the present disclosure. Devices that shows the signal modulations are indicated by the ovals in both images.

In a second aspect, e-beam logic state imaging (ELSI) is described. In an embodiment, using an ELSI approach, an e-beam logic state imaging technique allows detection and display of the logic state of integrated circuit structures or devices of interest. In an embodiment, one of two approaches is used to achieve detection of the logic state of the integrated circuit structures or devices. In a first ELSI approach, static e-beam logic state imaging (SELSI) is used. In a second ELSI approach, dynamic e-beam logic state imaging (DELSI) is used. It is to be appreciated that optical tools using a laser beam could may be configured to provide logic state imaging on devices of interest but the resolution is an order of magnitude lower. Conventional e-beam probers do not offer dynamic logic state imaging.

In an embodiment, using the SELSI technique in an ELSI approach, the integrated circuit structure or device of interest is put in a specific state by halting a tester pattern. A secondary electron image of the integrated circuit structures or devices is collected. The integrated circuit structures or devices show different contrast at high or low voltage states, allowing identification of the individual device logic states. In an embodiment, the SELSI approach is applicable for both P-type and N-type integrated circuit structures or devices. In an embodiment, images collected for conductive structures (e.g., interconnects on the front side) of devices toggled with different logic states reveal the following: lower voltage shows brighter contrast and higher voltages shows darker contrast due to differing amounts of secondary electrons produced from the structures at different voltages.

In another embodiment, using the DELSI technique in an ELSI approach, an electron

beam is scanned over an area containing the device of interest. Instead of gate modulation, Vcc power supply of the integrated circuit structures or devices of interest is modulated at a specific frequency. The secondary electron signal is amplified then sent to a lock-in amplifier or spectrum analyzer tuned to the specific frequency. The output of the lock-in amplifier or spectrum analyzer is fed into a scan control unit that raster over the area. In an embodiment, a signal from the lock-in amplifier or spectrum analyzer is be brighter than the rest of the area or areas scanned. Since the Vcc is modulated, only the integrated circuit structure or device that is on (e.g., connected to Vcc) shows the modulation in the secondary electron detector. The result allows mapping of devices that are turned on enables mapping of the logic states. In an embodiment, one subtle effect is that in an inverter chain the Vcc modulation can cause the output of the inverters to also modulate leading to modulation on the gate of the downstream invertor. In an embodiment, by comparing with a CAD layout and a test pattern defective integrated circuit structures or devices can be located and identifies as being in an incorrect logic state.

Figure 3 is a schematic of an e-beam prober 300 with e-beam logic state imaging (ELSI) capability, in accordance with an embodiment of the present disclosure. Referring to Figure 3, the e-beam prober 300 includes an e-beam column 302 (such as a scanning electron microscope (SEM) column), for delivering a beam 304 to a device under test (DUT) 306. The e-beam column 302, or at least a portion of the e-beam column 302 may be housed in a chamber 308, and the device under test (DUT) 306 may be supported by a stage 310, as is depicted.

In the e-beam prober 300, a signal generator 312 is coupled to the DUT 306. A detector 314 which is in the path of beam 304 or by the side of the e-beam column 302 is coupled to a sensing module 316. The sensing module 316 is coupled to a lock-in amplifier or spectrum analyzer 318 which is coupled to an operation amplifier 320. A scan module 322 is coupled to the operation amplifier 320 and can receive Scanning Electron Microscope (SEM) image signal 324 or send external x-y scan control signals 326 to the control board of electron column 302. A computer controller 328 can produce scanning electron microscope (SEM) images or electron-beam signal image mapping (ESIM) images 330.

Figure 4 includes plots and corresponding circuit schematics representing possible outcomes from an analysis performed on an e-beam prober such as e-beam prober 300 of Figure 3, in accordance with an embodiment of the present disclosure. Referring to Figure 4, plot 402 of a pass/fail analysis indicates a FAIL based on the determined state of the devices of the circuit 404. By contrast, plot 452 of a pass/fail analysis indicates a PASS based on the determined state of the devices of the circuit 454.

In a third aspect, optical-electrical fault mapping (OEFM) is described. In an

embodiment, an electron beam is used for ESIM (Electron-beam signal image mapping) or ELSI (E-beam Logic State Imaging) while testing the chip at the boundary of a pass and fail state (e.g., at specific voltage or frequency). In one embodiment, a laser beam is used to illuminate an area that includes integrated circuit structures or devices of interest to modulate the integrated circuit structures or devices. In a particular embodiment, the laser beam is in a large area illumination mode. In another embodiment, the laser beam is rastered from spot to spot across the area of interest while the electron beam is scanned across the whole area, or parked at specific devices, or rastered together with the laser beam.

In either case, in an embodiment, the laser modulation alters the defective device enough to change the testing chip from pass to fail, or vice versa. In one such embodiment, such altering allows for detection and localization of failing device(s) or cell(s) that responsible for marginal fail at a specific range in voltage or frequency. The device alteration using a laser together with an electron beam may be performed to detect the state and the fail, while using the laser to modulate the devices. It is to be appreciated that the laser does not need to be highly focused as in the optical tools, and the resolution is understood as being primarily determined by the electron beam instead of the laser optical beam.

In accordance with an embodiment of the present disclosure, for OEFM, an electron beam is used for ESIM or ELSI while a test pattern is looped continuously and the voltage and frequency (or temperature) is adjusted such that the tester pattern is at the passing and failing boundary. A laser beam is used to illuminate the area that contains the devices of interest to modulate the devices. The modulation may perturb the defective device enough to change the chip from pass to fail, or fail to pass. In an exemplary embodiment, on a scan chain test, when the DUT is at passing state all circuit elements in the scan chain show ESIM signal. However, when the laser perturbs the defective device to fail, the downstream circuit elements do not show the ESIM signal. In an embodiment, by comparing the ESIM maps with and without the laser illumination the location of the defective device can be determined. In an embodiment, OEFM offers two independent knobs for fault isolation: the laser modulation and electron beam detection.

Figure 5 is a schematic of an e-beam prober 500 with optical-electrical fault mapping (OEFM) capability, in accordance with an embodiment of the present disclosure. Referring to Figure 5, the e-beam prober 500 includes an e-beam column (such as a scanning electron microscope (SEM) column) for delivering a beam 504 to a device under test (DUT) 506. The e-beam column, or at least a portion of the e-beam column may be housed in a chamber 508, and the device under test (DUT) 506 may be supported by a stage 510, as is depicted. A laser source 507A is included together with the e-beam column in the e-beam prober 500. The laser source

507A is configured to output a laser beam 507B directed to the DUT 506, as is depicted.

In the e-beam prober 500, a signal generator 512 is coupled to the DUT 506. A detector 514 which is in the path of beam 504 is coupled to a sensing module 516. The sensing module 516 is coupled to a lock-in amplifier or spectrum analyzer 518 which is coupled to an operation amplifier 520. A scan module 522 is coupled to the operation amplifier 520 and can receive Scanning Electron Microscope (SEM) image signal 524 or send external x-y scan control signals 526 to the control board of electron column 502. A computer controller 528 can produce scanning electron microscope (SEM) images or electron-beam signal image mapping (ESIM) images 530.

Figure 6 includes (a) a determination schematic 602 and (b) corresponding location determination schematic 604 determined from plots 608 and 610 representing possible outcomes from an analysis performed on an e-beam prober such as e-beam prober 500 of Figure 5, in accordance with an embodiment of the present disclosure. Referring to Figure 6, an exemplary pass to fail determination 602 is determined for a location 606 in an area 604. The determination may be made based on analysis of a resulting response, such as plot 608 of a pass/fail analysis indicating a FAIL, or plot 610 of a pass/fail analysis indicating a PASS.

In a fourth aspect, E-beam device perturbation (EDP) is described. In an embodiment, a chip is placed under test at the boundary of pass and fail (e.g., at specific temperature, voltage or frequency) and an electron beam is used for device perturbation. The electron beam is rastered over the area of interest while the chip is running a specific pattern at the pass/fail boundary condition. When the electron beam hits a device and changes the chip from passing to fail (or vis versa), the location of the marginal device is recorded.

In an embodiment, EPD is similar to (OEFM) with the exception that integrated circuit structure or device perturbation is performed by the electron beam itself. The beam is scanned over the area of interest and the ESIM (Electron-beam signal image mapping) or ELSI (E-beam Logic State Imaging) signal is collected pixel by pixel, thus allowing mapping of defective devices. However, a test pattern is looped continuously and the voltage and frequency are adjusted such that the tester pattern and DUT is at the passing and failing boundary similar to OEFM. In an embodiment, the test pattern loop is synchronized with the electron beam scanning while the tester continuously monitors the pass to fail or fail to pass transitions of the DUT. In a particular embodiment, the electron beam is at an energy sufficiently low to not permanently alter the DUT. The electron beam is used to slightly perturb the timing of critical devices that are on a speed path. In a specific embodiment, the perturbation is on the order of 100 to 200 picoseconds. In an embodiment, when the electron beam hits the “timing critical” devices, the tester loop pattern transitions for pass or fail or from fail to pass. When this “transition” occurs,

the tester sends out a voltage signal which is sent into the second channel of the electron beam scanning/imaging system.

In an embodiment, using an EPD approach, a SEM image (e.g., ESIM and/or SELSI and/or DELSI), and an electron perturbation hit image is generated and synchronized pixel by pixel. In one such embodiment, this approach enables pinpointing of an exact location of the critical timing devices. In an embodiment, a resolution of approximately 5 nanometers or smaller is achieved.

In accordance with an embodiment of the present disclosure, referring to all four aspects described above, an electron beam is used to provide superior resolution compared to state-of-the-art optical tools. For example, optical tools may provide approximately 240 nanometers resolution, and possibly as small as 120 nanometers resolution. However, the wavelength of the light makes further improvement much more difficult if not impossible. By contrast, in an embodiment, electron beam systems described herein provide resolution in the range of 1-10 nanometers which allows detection at an individual device fin level. The capability to detect an individual failing fin within the device is advantageous. It is to be appreciated that the techniques described herein may be very powerful for advanced semiconductor development, debug and manufacturing. Embodiments described herein may be implemented for a wide range of semiconductor products.

In another aspect, one or more embodiments described herein are directed to lithographic approaches and tooling involving or suitable for complementary e-beam lithography (CEBL), including semiconductor processing considerations when implementing such approaches and tooling. Particular embodiments are directed to implementation of an underlying absorbing and/or conducting layer for e-beam direct write (EBDW) lithography.

Complementary lithography draws on the strengths of two lithography technologies, working hand-in-hand, to lower the cost of patterning critical layers in logic devices at 20nm half-pitch and below, in high-volume manufacturing (HVM). The most cost-effective way to implement complementary lithography is to combine optical lithography with e-beam lithography (EBL). The process of transferring integrated circuit (IC) designs to the wafer entails the following: optical lithography to print unidirectional lines (either strictly unidirectional or predominantly unidirectional) in a pre-defined pitch, pitch division techniques to increase line density, and EBL to “cut” the lines. EBL is also used to pattern other critical layers, notably contact and via holes. Optical lithography can be used alone to pattern other layers. When used to complement optical lithography, EBL is referred to as CEBL, or complementary EBL. CEBL is directed to cutting lines and holes. By not attempting to pattern all layers, CEBL plays a complementary but crucial role in meeting the industry’s patterning

needs at advanced (smaller) technology nodes (e.g., 10nm or smaller such as 7nm or 5nm technology nodes). CEBL also extends the use of current optical lithography technology, tools and infrastructure.

In an embodiment, complementary lithography as described herein involves first fabricating a gridded layout by conventional or state-of the-art lithography, such as 193nm immersion lithography (193i). Pitch division may be implemented to increase the density of lines in the gridded layout by a factor of n. Gridded layout formation with 193i lithography plus pitch division by a factor of n can be designated as 193i + P/n Pitch Division. Patterning of the pitch divided gridded layout may then be patterned using electron beam direct write (EBDW) "cuts," as is described in greater detail below. In one such embodiment, 193nm immersion scaling can be extended for many generations with cost effective pitch division. Complementary EBL is used to break gratings continuity and to pattern vias.

More specifically, embodiments described herein are directed to patterning features during the fabrication of an integrated circuit. In one embodiment, CEBL is used to pattern openings for forming vias. Vias are metal structures used to electrically connect metal lines above the vias to metal lines below the vias. In another embodiment, CEBL is used to form non-conductive spaces or interruptions along the metal lines. Conventionally, such interruptions have been referred to as "cuts" since the process involved removal or cutting away of portions of the metal lines. However, in a damascene approach, the interruptions may be referred to as "plugs" (also known in the art as blocking mask) which are regions along a metal line trajectory that are actually not metal at any stage of the fabrication scheme, but are rather preserved regions where metal cannot be formed. In either case, however, use of the terms cuts or plugs may be done so interchangeably. Via opening and metal line cut or plug formation is commonly referred to as back end of line (BEOL) processing for an integrated circuit. In another embodiment, CEBL is used for front end of line (FEOL) processing. For example, the scaling of active region dimensions (such as fin dimensions) and/or associated gate structures can be performed using CEBL techniques as described herein.

As described above, electron beam (e-beam) lithography may be implemented to complement standard lithographic techniques in order to achieved desired scaling of features for integrated circuit fabrication. An electron beam lithography tool may be used to perform the e-beam lithography. In an exemplary embodiment, Figure 4 is a cross-sectional schematic representation of an e-beam column of an electron beam lithography apparatus.

Referring to Figure 7, an e-beam column 700 includes an electron source 702 for providing a beam of electrons 704. The beam of electrons 704 is passed through a limiting aperture 706 and, subsequently, through high aspect ratio illumination optics 708. The outgoing

beam 710 is then passed through a slit 712 and may be controlled by a slim lens 714, e.g., which may be magnetic. Ultimately, the beam 704 is passed through a shaping aperture 716 (which may be a one-dimensional (1-D) shaping aperture) and then through a blanker aperture array (BAA) 718. The BAA 718 includes a plurality of physical apertures therein, such as openings formed in a thin slice of silicon. It may be the case that only a portion of the BAA 718 is exposed to the e-beam at a given time. Alternatively, or in conjunction, only a portion 720 of the e-beam 704 that passes through the BAA 718 is allowed to pass through a final aperture 722 (e.g., beam portion 721 is shown as blocked) and, possibly, a stage feedback deflector 724.

Referring again to Figure 7, the resulting e-beam 726 ultimately impinges as a spot 728 on a surface of a wafer 730, such as a silicon wafer used in IC manufacture. Specifically, the resulting e-beam may impinge on a photo-resist layer on the wafer, but embodiments are not so limited. A stage scan 732 moves the wafer 730 relative to the beam 726 along the direction of the arrow 734 shown in Figure 7. It is to be appreciated that an e-beam tool in its entirely may include numerous columns 700 of the type depicted in Figure 7. Also, as described in some embodiments below, the e-beam tool may have an associated base computer, and each column may further have a corresponding column computer.

It is to be appreciated that, in some embodiments, an e-beam column 700 as described above may also include other features in addition to those described in association with Figure 7. For example, in an embodiment, the sample stage can be rotated by 90 degrees to accommodate alternating metallization layers which may be printed orthogonally to one another (e.g., rotated between X and Y scanning directions). In another embodiment, an e-beam tool is capable of rotating a wafer by 90 degrees prior to loading the wafer on the stage. Furthermore, it is to be appreciated that the e-beam column described in association with Figure 7 is only one exemplary e-beam write apparatus that can be implemented to perform approaches described in association with embodiments disclosed herein. In yet other embodiments, the e-beam column has e-beam probing capability, such as described above in association with e-beam probing apparatuses 100, 300 or 500.

More generally, referring to all of the above aspects of embodiments of the present disclosure, it is to be appreciated that a metallization layer having lines with line cuts (or plugs) and having associated vias may be fabricated above a substrate and, in one embodiment, may be fabricated above a previous metallization layer. Such metallization layers may also used as signal lines to facilitate in e-beam probing of underlying devices. As an example, Figure 8 illustrates a plan view and corresponding cross-sectional view of a previous layer metallization structure, in accordance with an embodiment of the present disclosure. Referring to Figure 8, a starting structure 800 includes a pattern of metal lines 802 and interlayer dielectric (ILD) lines

804. The starting structure 800 may be patterned in a grating-like pattern with metal lines spaced at a constant pitch and having a constant width, as is depicted in Figure 8. Although not shown, the lines 802 may have interruptions (i.e., cuts or plugs) at various locations along the lines. The pattern, for example, may be fabricated by a pitch halving or pitch quartering approach, as described above. Some of the lines may be associated with underlying vias, such as line 802' shown as an example in the cross-sectional view.

In an embodiment, fabrication of a metallization layer on the previous metallization structure of Figure 8 begins with formation of an interlayer dielectric (ILD) material above the structure 800. A hardmask material layer may then be formed on the ILD layer. The hardmask material layer may be patterned to form a grating of unidirectional lines orthogonal to the lines 802 of 800. In one embodiment, the grating of unidirectional hardmask lines is fabricated using conventional lithography (e.g., photoresist and other associated layers) and may have a line density defined by a pitch-halving, pitch-quartering etc. approach as described above. The grating of hardmask lines leaves exposed a grating region of the underlying ILD layer. It is these exposed portions of the ILD layer that are ultimately patterned for metal line formation, via formation, and plug formation. For example, in an embodiment, via locations are patterned in regions of the exposed ILD using EBL as described above. The patterning may involve formation of a resist layer and patterning of the resist layer by EBL to provide via opening locations which may be etched into the ILD regions. The lines of overlying hardmask can be used to confine the vias to only regions of the exposed ILD, with overlap accommodated by the hardmask lines which can effectively be used as an etch stop. Plug (or cut) locations may also be patterned in exposed regions of the ILD, as confined by the overlying hardmask lines, in a separate EBL processing operation. The fabrication of cuts or plugs effectively preserve regions of ILD that will ultimately interrupt metal lines fabricated therein. Metal lines may then be fabricated using a damascene approach, where exposed portions of the ILD (those portions between the hardmask lines and not protected by a plug preservation layer, such as a resist layer patterned during "cutting") are partially recessed. The recessing may further extend the via locations to open metal lines from the underlying metallization structure. The partially recessed ILD regions are then filled with metal (a process which may also involve filling the via locations), e.g., by plating and CMP processing, to provide metal lines between the overlying hardmask lines. The hardmask lines may ultimately be removed for completion of a metallization structure. It is to be appreciated that the above ordering of line cuts, via formation, and ultimate line formation is provided only as an example. It is to be appreciated that a variety of processing schemes may be accommodated using EBL cuts and vias.

In an embodiment, as used throughout the present description, interlayer dielectric (ILD)

material is composed of or includes a layer of a dielectric or insulating material. Examples of suitable dielectric materials include, but are not limited to, oxides of silicon (e.g., silicon dioxide (SiO2)), doped oxides of silicon, fluorinated oxides of silicon, carbon doped oxides of silicon, various low-k dielectric materials known in the arts, and combinations thereof. The interlayer dielectric material may be formed by conventional techniques, such as, for example, chemical vapor deposition (CVD), physical vapor deposition (PVD), or by other deposition methods.

In an embodiment, as is also used throughout the present description, interconnect material is composed of one or more metal or other conductive structures. A common example is the use of copper lines and structures that may or may not include barrier layers between the copper and surrounding ILD material. As used herein, the term metal includes alloys, stacks, and other combinations of multiple metals. For example, the metal interconnect lines may include barrier layers, stacks of different metals or alloys, etc. The interconnect lines are also sometimes referred to in the arts as traces, wires, lines, metal, or simply interconnect.

In an embodiment, as is also used throughout the present description, hardmask materials are composed of dielectric materials different from the interlayer dielectric material. In some embodiments, a hardmask layer includes a layer of a nitride of silicon (e.g., silicon nitride) or a layer of an oxide of silicon, or both, or a combination thereof. Other suitable materials may include carbon-based materials. In another embodiment, a hardmask material includes a metal species. For example, a hardmask or other overlying material may include a layer of a nitride of titanium or another metal (e.g., titanium nitride). Potentially lesser amounts of other materials, such as dopants or surface oxidation, may be included in one or more of these layers. Alternatively, other hardmask layers known in the arts may be used depending upon the particular implementation. The hardmask layers maybe formed by ALD, CVD, PVD, or by other deposition methods.

It is to be appreciated that the layers and materials described in association with Figure 8 are typically formed on or above an underlying semiconductor substrate or structure, such as underlying device layer(s) of an integrated circuit. In an embodiment, an underlying semiconductor substrate represents a general workpiece object used to manufacture integrated circuits. The semiconductor substrate often includes a wafer or other piece of silicon or another semiconductor material. Suitable semiconductor substrates include, but are not limited to, single crystal silicon, polycrystalline silicon and silicon on insulator (SOI), as well as similar substrates formed of other semiconductor materials, such as gallium arsenide. The semiconductor substrate, depending on the stage of manufacture, often includes transistors, integrated circuitry, and the like. The substrate may also include semiconductor materials, metals, dielectrics, dopants, and other materials commonly found in semiconductor substrates. Furthermore, the

structure depicted in Figure 8 may be fabricated on underlying lower level interconnect layers.

In another embodiment, e-beam probing is used during the fabrication of semiconductor devices, such as PMOS or NMOS devices of an integrated circuit. As an example of a completed device, Figures 9A and 9B illustrate a cross-sectional view and a plan view (taken along the a-a' axis of the cross-sectional view), respectively, of a non-planar semiconductor device having a plurality of fins, in accordance with an embodiment of the present disclosure.

Referring to Figure 9A, a semiconductor structure or device 900 includes a non-planar active region (e.g., a fin structure including protruding fin portion 904 and sub-fin region 905) formed from substrate 902, and within isolation region 906. A gate line 908 is disposed over the protruding portions 904 of the non-planar active region as well as over a portion of the isolation region 906. As shown, gate line 908 includes a gate electrode 950 and a gate dielectric layer 952. In one embodiment, gate line 908 may also include a dielectric cap layer 954. A gate contact 914, and overlying gate contact via 916 are also seen from this perspective, along with an overlying metal interconnect 960, all of which are disposed in inter-layer dielectric stacks or layers 970. Also seen from the perspective of Figure 9A, the gate contact 914 is, in one embodiment, disposed over isolation region 906, but not over the non-planar active regions.

Referring to Figure 9B, the gate line 908 is shown as disposed over the protruding fin portions 904. Source and drain regions 904A and 904B of the protruding fin portions 904 can be seen from this perspective. In one embodiment, the source and drain regions 904A and 904B are doped portions of original material of the protruding fin portions 904. In another embodiment, the material of the protruding fin portions 904 is removed and replaced with another semiconductor material, e.g., by epitaxial deposition. In either case, the source and drain regions 904A and 904B may extend below the height of dielectric layer 906, i.e., into the sub-fin region 905.

In an embodiment, the semiconductor structure or device 900 is a non-planar device such as, but not limited to, a fin-FET or a tri-gate device. In such an embodiment, a corresponding semiconducting channel region is composed of or is formed in a three-dimensional body. In one such embodiment, the gate electrode stacks of gate lines 908 surround at least a top surface and a pair of sidewalls of the three-dimensional body.

Embodiments disclosed herein may be used to manufacture a wide variety of different types of integrated circuits and/or microelectronic devices. Examples of such integrated circuits include, but are not limited to, processors, chipset components, graphics processors, digital signal processors, micro-controllers, and the like. In other embodiments, semiconductor memory may be manufactured. Moreover, the integrated circuits or other microelectronic devices may be used in a wide variety of electronic devices known in the arts. For example, in

computer systems (e.g., desktop, laptop, server), cellular phones, personal electronics, etc. The integrated circuits may be coupled with a bus and other components in the systems. For example, a processor may be coupled by one or more buses to a memory, a chipset, etc. Each of the processor, the memory, and the chipset, may potentially be manufactured using the approaches disclosed herein.

Figure 10 illustrates a computing device 1000 in accordance with one implementation of the disclosure. The computing device 1000 houses a board 1002. The board 1002 may include a number of components, including but not limited to a processor 1004 and at least one communication chip 1006. The processor 1004 is physically and electrically coupled to the board 1002. In some implementations the at least one communication chip 1006 is also physically and electrically coupled to the board 1002. In further implementations, the communication chip 1006 is part of the processor 1004.

Depending on its applications, computing device 1000 may include other components that may or may not be physically and electrically coupled to the board 1002. These other components include, but are not limited to, volatile memory (e.g., DRAM), non-volatile memory (e.g., ROM), flash memory, a graphics processor, a digital signal processor, a crypto processor, a chipset, an antenna, a display, a touchscreen display, a touchscreen controller, a battery, an audio codec, a video codec, a power amplifier, a global positioning system (GPS) device, a compass, an accelerometer, a gyroscope, a speaker, a camera, and a mass storage device (such as hard disk drive, compact disk (CD), digital versatile disk (DVD), and so forth).

The communication chip 1006 enables wireless communications for the transfer of data to and from the computing device 1000. The term "wireless" and its derivatives may be used to describe circuits, devices, systems, methods, techniques, communications channels, etc., that may communicate data through the use of modulated electromagnetic radiation through a non-solid medium. The term does not imply that the associated devices do not contain any wires, although in some embodiments they might not. The communication chip 1006 may implement any of a number of wireless standards or protocols, including but not limited to Wi-Fi (IEEE 802.11 family), WiMAX (IEEE 802.16 family), IEEE 802.20, long term evolution (LTE), Ev-DO, HSPA+, HSDPA+, HSUPA+, EDGE, GSM, GPRS, CDMA, TDMA, DECT, Bluetooth, derivatives thereof, as well as any other wireless protocols that are designated as 3G, 4G, 5G, and beyond. The computing device 1000 may include a plurality of communication chips 1006. For instance, a first communication chip 1006 may be dedicated to shorter range wireless communications such as Wi-Fi and Bluetooth and a second communication chip 1006 may be dedicated to longer range wireless communications such as GPS, EDGE, GPRS, CDMA, WiMAX, LTE, Ev-DO, and others.

The processor 1004 of the computing device 1000 includes an integrated circuit die packaged within the processor 1004. In some implementations of the disclosure, the integrated circuit die of the processor includes one or more structures tested using an e-beam probing apparatus or methodology, in accordance with implementations of embodiments of the disclosure. The term "processor" may refer to any device or portion of a device that processes electronic data from registers and/or memory to transform that electronic data into other electronic data that may be stored in registers and/or memory.

The communication chip 1006 also includes an integrated circuit die packaged within the communication chip 1006. In accordance with another implementation of embodiments of the disclosure, the integrated circuit die of the communication chip includes one or more structures tested using an e-beam probing apparatus or methodology, in accordance with implementations of embodiments of the disclosure.

In further implementations, another component housed within the computing device 1000 may contain an integrated circuit die that includes one or more structures tested using an e-beam probing apparatus or methodology, in accordance with implementations of embodiments of the disclosure.

In various implementations, the computing device 1000 may be a laptop, a netbook, a notebook, an ultrabook, a smartphone, a tablet, a personal digital assistant (PDA), an ultra mobile PC, a mobile phone, a desktop computer, a server, a printer, a scanner, a monitor, a set-top box, an entertainment control unit, a digital camera, a portable music player, or a digital video recorder. In further implementations, the computing device 1000 may be any other electronic device that processes data.

Embodiments of the present disclosure may be provided as a computer program product, or software, that may include a machine-readable medium having stored thereon instructions, which may be used to program a computer system (or other electronic devices) to perform a process according to embodiments of the present disclosure. In one embodiment, the computer system is coupled with an e-beam tool such as described in association with Figures 1 (e-beam prober 100), 3 (e-beam prober 300), 5 (e-beam prober 500) or 7 (column 700). A machine-readable medium includes any mechanism for storing or transmitting information in a form readable by a machine (e.g., a computer). For example, a machine-readable (e.g., computer-readable) medium includes a machine (e.g., a computer) readable storage medium (e.g., read only memory ("ROM"), random access memory ("RAM"), magnetic disk storage media, optical storage media, flash memory devices, etc.), a machine (e.g., computer) readable transmission medium (electrical, optical, acoustical or other form of propagated signals (e.g., infrared signals, digital signals, etc.)), etc.

Figure 11 illustrates a diagrammatic representation of a machine in the exemplary form of a computer system 1100 within which a set of instructions, for causing the machine to perform any one or more of the methodologies described herein (such as end-point detection), may be executed. In alternative embodiments, the machine may be connected (e.g., networked) to other machines in a Local Area Network (LAN), an intranet, an extranet, or the Internet. The machine may operate in the capacity of a server or a client machine in a client-server network environment, or as a peer machine in a peer-to-peer (or distributed) network environment. The machine may be a personal computer (PC), a tablet PC, a set-top box (STB), a Personal Digital Assistant (PDA), a cellular telephone, a web appliance, a server, a network router, switch or bridge, or any machine capable of executing a set of instructions (sequential or otherwise) that specify actions to be taken by that machine. Further, while only a single machine is illustrated, the term "machine" shall also be taken to include any collection of machines (e.g., computers) that individually or jointly execute a set (or multiple sets) of instructions to perform any one or more of the methodologies described herein.

The exemplary computer system 1100 includes a processor 1102, a main memory 1104 (e.g., read-only memory (ROM), flash memory, dynamic random access memory (DRAM) such as synchronous DRAM (SDRAM) or Rambus DRAM (RDRAM), etc.), a static memory 1106 (e.g., flash memory, static random access memory (SRAM), etc.), and a secondary memory 1118 (e.g., a data storage device), which communicate with each other via a bus 1130.

Processor 1102 represents one or more general-purpose processing devices such as a microprocessor, central processing unit, or the like. More particularly, the processor 1102 may be a complex instruction set computing (CISC) microprocessor, reduced instruction set computing (RISC) microprocessor, very long instruction word (VLIW) microprocessor, processor implementing other instruction sets, or processors implementing a combination of instruction sets. Processor 1102 may also be one or more special-purpose processing devices such as an application specific integrated circuit (ASIC), a field programmable gate array (FPGA), a digital signal processor (DSP), network processor, or the like. Processor 1102 is configured to execute the processing logic 1126 for performing the operations described herein.

The computer system 1100 may further include a network interface device 1108. The computer system 1100 also may include a video display unit 1110 (e.g., a liquid crystal display (LCD), a light emitting diode display (LED), or a cathode ray tube (CRT)), an alphanumeric input device 1112 (e.g., a keyboard), a cursor control device 1114 (e.g., a mouse), and a signal generation device 1116 (e.g., a speaker).

The secondary memory 1118 may include a machine-accessible storage medium (or more specifically a computer-readable storage medium) 1132 on which is stored one or more

sets of instructions (e.g., software 1122) embodying any one or more of the methodologies or functions described herein. The software 1122 may also reside, completely or at least partially, within the main memory 1104 and/or within the processor 1102 during execution thereof by the computer system 1100, the main memory 1104 and the processor 1102 also constituting machine-readable storage media. The software 1122 may further be transmitted or received over a network 1120 via the network interface device 1108.

While the machine-accessible storage medium 1132 is shown in an exemplary embodiment to be a single medium, the term "machine-readable storage medium" should be taken to include a single medium or multiple media (e.g., a centralized or distributed database, and/or associated caches and servers) that store the one or more sets of instructions. The term "machine-readable storage medium" shall also be taken to include any medium that is capable of storing or encoding a set of instructions for execution by the machine and that cause the machine to perform any one or more of the methodologies of the present disclosure. The term "machine-readable storage medium" shall accordingly be taken to include, but not be limited to, solid-state memories, and optical and magnetic media.

Implementations of embodiments of the disclosure may be formed or carried out on a substrate, such as a semiconductor substrate. In one implementation, the semiconductor substrate may be a crystalline substrate formed using a bulk silicon or a silicon-on-insulator substructure. In other implementations, the semiconductor substrate may be formed using alternate materials, which may or may not be combined with silicon, that include but are not limited to germanium, indium antimonide, lead telluride, indium arsenide, indium phosphide, gallium arsenide, indium gallium arsenide, gallium antimonide, or other combinations of group III-V or group IV materials. Although a few examples of materials from which the substrate may be formed are described here, any material that may serve as a foundation upon which a semiconductor device may be built falls within the spirit and scope of the present disclosure.

A plurality of transistors, such as metal-oxide-semiconductor field-effect transistors (MOSFET or simply MOS transistors), may be fabricated on the substrate. In various implementations of the disclosure, the MOS transistors may be planar transistors, nonplanar transistors, or a combination of both. Nonplanar transistors include FinFET transistors such as double-gate transistors and tri-gate transistors, and wrap-around or all-around gate transistors such as nanoribbon and nanowire transistors. Although the implementations described herein may illustrate only planar transistors and FinFET, it should be noted that the disclosure may also be carried out using nonplanar transistors.

Each MOS transistor includes a gate stack formed of at least two layers, a gate dielectric layer and a gate electrode layer. The gate dielectric layer may include one layer or a stack of

layers. The one or more layers may include silicon oxide, silicon dioxide (SiO_2) and/or a high-k dielectric material. The high-k dielectric material may include elements such as hafnium, silicon, oxygen, titanium, tantalum, lanthanum, aluminum, zirconium, barium, strontium, yttrium, lead, scandium, niobium, and zinc. Examples of high-k materials that may be used in the gate dielectric layer include, but are not limited to, hafnium oxide, hafnium silicon oxide, lanthanum oxide, lanthanum aluminum oxide, zirconium oxide, zirconium silicon oxide, tantalum oxide, titanium oxide, barium strontium titanium oxide, barium titanium oxide, strontium titanium oxide, yttrium oxide, aluminum oxide, lead scandium tantalum oxide, and lead zinc niobate. In some embodiments, an annealing process may be carried out on the gate dielectric layer to improve its quality when a high-k material is used.

The gate electrode layer is formed on the gate dielectric layer and may consist of at least one P-type workfunction metal or N-type workfunction metal, depending on whether the transistor is to be a PMOS or an NMOS transistor. In some implementations, the gate electrode layer may consist of a stack of two or more metal layers, where one or more metal layers are workfunction metal layers and at least one metal layer is a fill metal layer.

For a PMOS transistor, metals that may be used for the gate electrode include, but are not limited to, ruthenium, palladium, platinum, cobalt, nickel, and conductive metal oxides, e.g., ruthenium oxide. A P-type metal layer will enable the formation of a PMOS gate electrode with a workfunction that is between about 4.9 eV and about 5.2 eV. For an NMOS transistor, metals that may be used for the gate electrode include, but are not limited to, hafnium, zirconium, titanium, tantalum, aluminum, alloys of these metals, and carbides of these metals such as hafnium carbide, zirconium carbide, titanium carbide, tantalum carbide, and aluminum carbide. An N-type metal layer will enable the formation of an NMOS gate electrode with a workfunction that is between about 3.9 eV and about 4.2 eV.

In some implementations, the gate electrode may consist of a "U"-shaped structure that includes a bottom portion substantially parallel to the surface of the substrate and two sidewall portions that are substantially perpendicular to the top surface of the substrate. In another implementation, at least one of the metal layers that form the gate electrode may simply be a planar layer that is substantially parallel to the top surface of the substrate and does not include sidewall portions substantially perpendicular to the top surface of the substrate. In further implementations of the disclosure, the gate electrode may consist of a combination of U-shaped structures and planar, non-U-shaped structures. For example, the gate electrode may consist of one or more U-shaped metal layers formed atop one or more planar, non-U-shaped layers.

In some implementations of the disclosure, a pair of sidewall spacers may be formed on opposing sides of the gate stack that bracket the gate stack. The sidewall spacers may be formed

from a material such as silicon nitride, silicon oxide, silicon carbide, silicon nitride doped with carbon, and silicon oxynitride. Processes for forming sidewall spacers are well known in the art and generally include deposition and etching process steps. In an alternate implementation, a plurality of spacer pairs may be used, for instance, two pairs, three pairs, or four pairs of sidewall spacers may be formed on opposing sides of the gate stack.

As is well known in the art, source and drain regions are formed within the substrate adjacent to the gate stack of each MOS transistor. The source and drain regions are generally formed using either an implantation/diffusion process or an etching/deposition process. In the former process, dopants such as boron, aluminum, antimony, phosphorous, or arsenic may be ion-implanted into the substrate to form the source and drain regions. An annealing process that activates the dopants and causes them to diffuse further into the substrate typically follows the ion implantation process. In the latter process, the substrate may first be etched to form recesses at the locations of the source and drain regions. An epitaxial deposition process may then be carried out to fill the recesses with material that is used to fabricate the source and drain regions. In some implementations, the source and drain regions may be fabricated using a silicon alloy such as silicon germanium or silicon carbide. In some implementations the epitaxially deposited silicon alloy may be doped in situ with dopants such as boron, arsenic, or phosphorous. In further embodiments, the source and drain regions may be formed using one or more alternate semiconductor materials such as germanium or a group III-V material or alloy. And in further embodiments, one or more layers of metal and/or metal alloys may be used to form the source and drain regions.

One or more interlayer dielectrics (ILD) are deposited over the MOS transistors. The ILD layers may be formed using dielectric materials known for their applicability in integrated circuit structures, such as low-k dielectric materials. Examples of dielectric materials that may be used include, but are not limited to, silicon dioxide (SiO2), carbon doped oxide (CDO), silicon nitride, organic polymers such as perfluorocyclobutane or polytetrafluoroethylene, fluorosilicate glass (FSG), and organosilicates such as silsesquioxane, siloxane, or organosilicate glass. The ILD layers may include pores or air gaps to further reduce their dielectric constant.

Figure 12 illustrates an interposer 1200 that includes one or more embodiments of the disclosure. The interposer 1200 is an intervening substrate used to bridge a first substrate 1202 to a second substrate 1204. The first substrate 1202 may be, for instance, an integrated circuit die. The second substrate 1204 may be, for instance, a memory module, a computer motherboard, or another integrated circuit die. Generally, the purpose of an interposer 1200 is to spread a connection to a wider pitch or to reroute a connection to a different connection. For example, an interposer 1200 may couple an integrated circuit die to a ball grid array (BGA) 1206

that can subsequently be coupled to the second substrate 1204. In some embodiments, the first and second substrates 1202/1204 are attached to opposing sides of the interposer 1200. In other embodiments, the first and second substrates 1202/1204 are attached to the same side of the interposer 1200. And in further embodiments, three or more substrates are interconnected by way of the interposer 1200.

The interposer 1200 may be formed of an epoxy resin, a fiberglass-reinforced epoxy resin, a ceramic material, or a polymer material such as polyimide. In further implementations, the interposer may be formed of alternate rigid or flexible materials that may include the same materials described above for use in a semiconductor substrate, such as silicon, germanium, and other group III-V and group IV materials.

The interposer may include metal interconnects 1208 and vias 1210, including but not limited to through-silicon vias (TSVs) 1212. The interposer 1200 may further include embedded devices 1214, including both passive and active devices. Such devices include, but are not limited to, capacitors, decoupling capacitors, resistors, inductors, fuses, diodes, transformers, sensors, and electrostatic discharge (ESD) devices. More complex devices such as radio-frequency (RF) devices, power amplifiers, power management devices, antennas, arrays, sensors, and MEMS devices may also be formed on the interposer 1200.

In accordance with embodiments of the disclosure, apparatuses or processes disclosed herein may be used in the fabrication of interposer 1200.

Figure 13 illustrates a computing device 1300 in accordance with one embodiment of the disclosure. The computing device 1300 may include a number of components. In one embodiment, these components are attached to one or more motherboards. In an alternate embodiment, these components are fabricated onto a single system-on-a-chip (SoC) die rather than a motherboard. The components in the computing device 1300 include, but are not limited to, an integrated circuit die 1302 and at least one communication chip 1308. In some implementations the communication chip 1308 is fabricated as part of the integrated circuit die 1302. The integrated circuit die 1302 may include a CPU 1304 as well as on-die memory 1306, often used as cache memory, that can be provided by technologies such as embedded DRAM (eDRAM) or spin-transfer torque memory (STTM or STTM-RAM).

Computing device 1300 may include other components that may or may not be physically and electrically coupled to the motherboard or fabricated within an SoC die. These other components include, but are not limited to, volatile memory 1310 (e.g., DRAM), non-volatile memory 1312 (e.g., ROM or flash memory), a graphics processing unit 1314 (GPU), a digital signal processor 1316, a crypto processor 1342 (a specialized processor that executes cryptographic algorithms within hardware), a chipset 1320, an antenna 1322, a display or a

touchscreen display 4024, a touchscreen controller 1326, a battery 1329 or other power source, a power amplifier (not shown), a global positioning system (GPS) device 1328, a compass 1330, a motion coprocessor or sensors 1332 (that may include an accelerometer, a gyroscope, and a compass), a speaker 1334, a camera 1336, user input devices 1338 (such as a keyboard, mouse, stylus, and touchpad), and a mass storage device 1340 (such as hard disk drive, compact disk (CD), digital versatile disk (DVD), and so forth).

The communications chip 1308 enables wireless communications for the transfer of data to and from the computing device 1300. The term "wireless" and its derivatives may be used to describe circuits, devices, systems, methods, techniques, communications channels, etc., that may communicate data through the use of modulated electromagnetic radiation through a non-solid medium. The term does not imply that the associated devices do not contain any wires, although in some embodiments they might not. The communication chip 1308 may implement any of a number of wireless standards or protocols, including but not limited to Wi-Fi (IEEE 802.11 family), WiMAX (IEEE 802.16 family), IEEE 802.20, long term evolution (LTE), Ev-DO, HSPA+, HSDPA+, HSUPA+, EDGE, GSM, GPRS, CDMA, TDMA, DECT, Bluetooth, derivatives thereof, as well as any other wireless protocols that are designated as 3G, 4G, 5G, and beyond. The computing device 1300 may include a plurality of communication chips 1308. For instance, a first communication chip 1308 may be dedicated to shorter range wireless communications such as Wi-Fi and Bluetooth and a second communication chip 4008 may be dedicated to longer range wireless communications such as GPS, EDGE, GPRS, CDMA, WiMAX, LTE, Ev-DO, and others.

The processor 1304 of the computing device 1300 includes one or more structures tested using an e-beam probing apparatus or methodology, in accordance with implementations of embodiments of the disclosure. The term "processor" may refer to any device or portion of a device that processes electronic data from registers and/or memory to transform that electronic data into other electronic data that may be stored in registers and/or memory.

The communication chip 1308 may also include one or more structures tested using an e-beam probing apparatus or methodology, in accordance with implementations of embodiments of the disclosure.

In further embodiments, another component housed within the computing device 1300 may contain one or more structures tested using an e-beam probing apparatus or methodology, in accordance with implementations of embodiments of the disclosure.

In various embodiments, the computing device 1300 may be a laptop computer, a netbook computer, a notebook computer, an ultrabook computer, a smartphone, a tablet, a personal digital assistant (PDA), an ultra mobile PC, a mobile phone, a desktop computer, a

server, a printer, a scanner, a monitor, a set-top box, an entertainment control unit, a digital camera, a portable music player, or a digital video recorder. In further implementations, the computing device 1300 may be any other electronic device that processes data.

Thus, apparatuses and methodologies for electron beam probing for chip debug and fault isolation have been disclosed.

The above description of illustrated implementations of embodiments of the disclosure, including what is described in the Abstract, is not intended to be exhaustive or to limit the disclosure to the precise forms disclosed. While specific implementations of, and examples for, the disclosure are described herein for illustrative purposes, various equivalent modifications are possible within the scope of the disclosure, as those skilled in the relevant art will recognize.

These modifications may be made to the disclosure in light of the above detailed description. The terms used in the following claims should not be construed to limit the disclosure to the specific implementations disclosed in the specification and the claims. Rather, the scope of the disclosure is to be determined entirely by the following claims, which are to be construed in accordance with established doctrines of claim interpretation.

Example embodiment 1: A method of electron-beam signal image mapping (ESIM) includes, scanning an electron beam over an area on a chip containing an integrated circuit structure, toggling a gate electrode of the integrated circuit structure at a frequency, amplifying a secondary electron signal and sending the amplified secondary electron signal to a lock-in amplifier or spectrum analyzer tuned to the frequency, feeding an output of the lock-in amplifier or spectrum analyzer into a scan control unit that rasters over the area, and illuminating a portion of the integrated circuit structure with the electron beam to modulate the secondary electron signal.

Example embodiment 2: The method of example embodiment 1, wherein modulate the secondary electron signal includes active voltage contrast to produce a modulating signal at a secondary electron detector, the modulating signal routed to the lock-in amplifier or spectrum analyzer.

Example embodiment 3: The method of example embodiment 2, wherein a location of a signal from the lock-in amplifier or spectrum analyzer indicates a position of the integrated circuit structure carrying an oscillating signal.

Example embodiment 4: The method of example embodiment 3, wherein a mapping of the integrated circuit structure is compared against a computer assisted design (CAD) layout to determine a defective device of the integrated circuit structure.

Example embodiment 5: The method of example embodiment 1, 2, 3 or 4, wherein illuminating a portion of the integrated circuit structure with the electron beam includes

illuminating a metal line of the integrated circuit structure.

Example embodiment 6: The method of example embodiment 1, 2, 3 or 4, wherein illuminating a portion of the integrated circuit structure with the electron beam includes illuminating a silicon fin of the integrated circuit structure.

Example embodiment 7: The method of example embodiment 1, 2, 3, 4, 5 or 6, wherein scanning the electron beam over the area and illuminating the portion of the integrated circuit structure with the electron beam to modulate the secondary electron signal includes performing chip debug or fault isolation in the area.

Example embodiment 8: A method of static e-beam logic state imaging (SELSI) includes scanning an electron beam over an area on a chip containing an integrated circuit structure, putting the integrated circuit structure in a specific state by halting a tester pattern, collecting a secondary electron image of the integrated circuit structure, the integrated circuit structure exhibiting different contrast at high or low voltage states upon toggling the integrated circuit structure. The method also includes identifying an individual device logic state of the integrated circuit structure based on the toggling.

Example embodiment 9: The method of example embodiment 8, further including collecting images for a conductive structure of the toggled integrated circuit structure toggled with different logic states to reveal a brighter contrast or darker contrast.

Example embodiment 10: The method of example embodiment 8 or 9, wherein collecting the secondary electron image of the integrated circuit structure includes collecting the secondary electron image of a metal line of the integrated circuit structure.

Example embodiment 11: The method of example embodiment 8 or 9, wherein collecting the secondary electron image of the integrated circuit structure includes collecting the secondary electron image of a silicon fin of the integrated circuit structure.

Example embodiment 12: The method of example embodiment 8, 9, 10 or 11, wherein scanning the electron beam over the area and identifying the individual device logic state of the integrated circuit structure includes performing chip debug or fault isolation in the area.

Example embodiment 13: A method of dynamic e-beam logic state imaging (DELSI) includes scanning an electron beam over an area on a chip containing an integrated circuit structure, modulating Vcc power supply of the integrated circuit structure at a frequency, amplifying a secondary electron signal and sending the amplified signal to a lock-in amplifier or spectrum analyzer tuned to the frequency, feeding an output of the lock-in amplifier or spectrum analyzer into a scan control unit that rasters over the area, and mapping a logic state of the integrated circuit structure based on brightness of a location of the area.

Example embodiment 14: The method of example embodiment 13, wherein amplifying

the secondary electron signal includes amplifying the secondary electron signal of a metal line of the integrated circuit structure.

Example embodiment 15: The method of example embodiment 13, wherein amplifying the secondary electron signal includes amplifying the secondary electron signal of a silicon fin of the integrated circuit structure.

Example embodiment 16: The method of example embodiment 13, 14 or 15, wherein scanning the electron beam over the area and mapping the logic state of the integrated circuit structure includes performing chip debug or fault isolation in the area.

Example embodiment 17: A method of optical-electrical fault mapping (OEFM) including scanning an electron beam over an area on a chip containing an integrated circuit structure, illuminating the integrated circuit structure with a laser beam to modulate the integrated circuit structure, testing the integrated circuit structure at a boundary of a pass and fail state of the integrated circuit structure, and identifying a defective integrated circuit structure based on a change in the pass and fail state.

Example embodiment 18: The method of example embodiment 17, wherein illuminating the integrated circuit structure with the laser beam includes illuminating a metal line of the integrated circuit structure.

Example embodiment 19: The method of example embodiment 17, wherein illuminating the integrated circuit structure with the laser beam includes illuminating a silicon fin of the integrated circuit structure.

Example embodiment 20: The method of example embodiment 17, 18 or 19, wherein scanning the electron beam over the area and testing the integrated circuit structure includes performing chip debug or fault isolation in the area.

CLAIMS

What is claimed is:

1. A method of electron-beam signal image mapping (ESIM), the method comprising:

scanning an electron beam over an area on a chip containing an integrated circuit structure;

toggling a gate electrode of the integrated circuit structure at a frequency;

amplifying a secondary electron signal and sending the amplified secondary electron signal to a lock-in amplifier or spectrum analyzer tuned to the frequency;

feeding an output of the lock-in amplifier or spectrum analyzer into a scan control unit that rasters over the area; and

illuminating a portion of the integrated circuit structure with the electron beam to modulate the secondary electron signal.

2. The method of claim 1, wherein modulate the secondary electron signal comprises active voltage contrast to produce a modulating signal at a secondary electron detector, the modulating signal routed to the lock-in amplifier or spectrum analyzer.

3. The method of claim 2, wherein a location of a signal from the lock-in amplifier or spectrum analyzer indicates a position of the integrated circuit structure carrying an oscillating signal.

4. The method of claim 3, wherein a mapping of the integrated circuit structure is compared against a computer assisted design (CAD) layout to determine a defective device of the integrated circuit structure.

5. The method of claim 1, wherein illuminating a portion of the integrated circuit structure with the electron beam comprises illuminating a metal line of the integrated circuit structure.

6. The method of claim 1, wherein illuminating a portion of the integrated circuit structure with the electron beam comprises illuminating a silicon fin of the integrated circuit structure.

7. The method of claim 1, wherein scanning the electron beam over the area and illuminating the portion of the integrated circuit structure with the electron beam to modulate the secondary electron signal comprises performing chip debug or fault isolation in the area.

8. A method of static e-beam logic state imaging (SELSI), the method comprising:

scanning an electron beam over an area on a chip containing an integrated circuit structure;

putting the integrated circuit structure in a specific state by halting a tester pattern;

collecting a secondary electron image of the integrated circuit structure, the integrated circuit structure exhibiting different contrast at high or low voltage states upon toggling the integrated circuit structure; and

identifying an individual device logic state of the integrated circuit structure based on the toggling.

9. The method of claim 8, further comprising:

collecting images for a conductive structure of the toggled integrated circuit structure toggled with different logic states to reveal a brighter contrast or darker contrast.

10. The method of claim 8, wherein collecting the secondary electron image of the integrated circuit structure comprises collecting the secondary electron image of a metal line of the integrated circuit structure.

11. The method of claim 8, wherein collecting the secondary electron image of the integrated circuit structure comprises collecting the secondary electron image of a silicon fin of the integrated circuit structure.

12. The method of claim 8, wherein scanning the electron beam over the area and identifying the individual device logic state of the integrated circuit structure comprises performing chip debug or fault isolation in the area.

13. A method of dynamic e-beam logic state imaging (DELSI), the method comprising:

scanning an electron beam over an area on a chip containing an integrated circuit structure;

modulating Vcc power supply of the integrated circuit structure at a frequency;

amplifying a secondary electron signal and sending the amplified signal to a lock-in amplifier or spectrum analyzer tuned to the frequency;

feeding an output of the lock-in amplifier or spectrum analyzer into a scan control unit that rasters over the area; and

mapping a logic state of the integrated circuit structure based on brightness of a location

of the area.

14. The method of claim 13, wherein amplifying the secondary electron signal comprises amplifying the secondary electron signal of a metal line of the integrated circuit structure.

15. The method of claim 13, wherein amplifying the secondary electron signal comprises amplifying the secondary electron signal of a silicon fin of the integrated circuit structure.

16. The method of claim 13, wherein scanning the electron beam over the area and mapping the logic state of the integrated circuit structure comprises performing chip debug or fault isolation in the area.

17. A method of optical-electrical fault mapping (OEFM), the method comprising:

scanning an electron beam over an area on a chip containing an integrated circuit structure;

illuminating the integrated circuit structure with a laser beam to modulate the integrated circuit structure;

testing the integrated circuit structure at a boundary of a pass and fail state of the integrated circuit structure; and

identifying a defective integrated circuit structure based on a change in the pass and fail state.

18. The method of claim 17, wherein illuminating the integrated circuit structure with the laser beam comprises illuminating a metal line of the integrated circuit structure.

19. The method of claim 17, wherein illuminating the integrated circuit structure with the laser beam comprises illuminating a silicon fin of the integrated circuit structure.

20. The method of claim 17, wherein scanning the electron beam over the area and testing the integrated circuit structure comprises performing chip debug or fault isolation in the area.

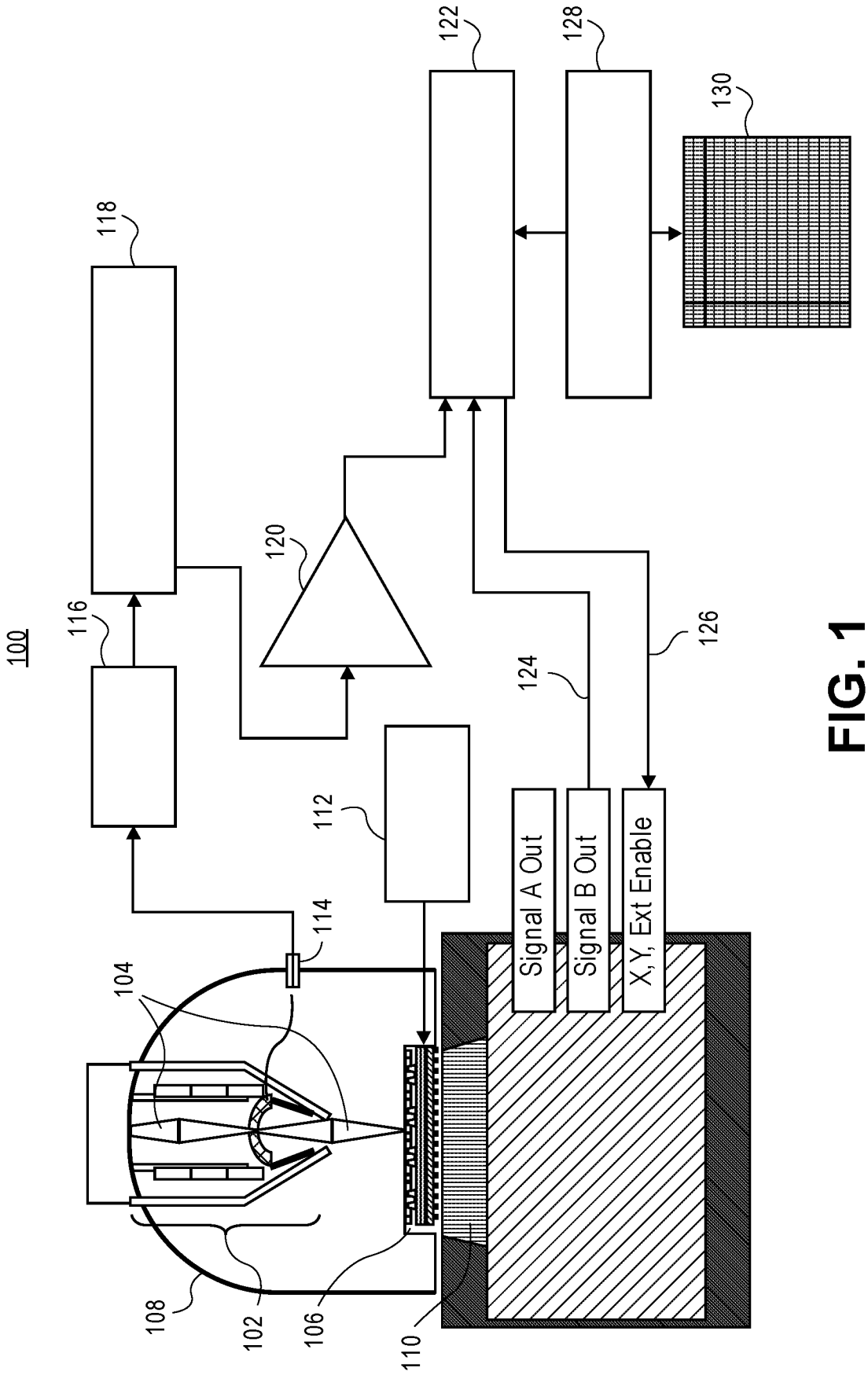

100
102
104
106
108
110
112
114
116
118
120
122
124
126
128
130
Signal A Out
Signal B Out
X,Y, Ext Enable

FIG. 1

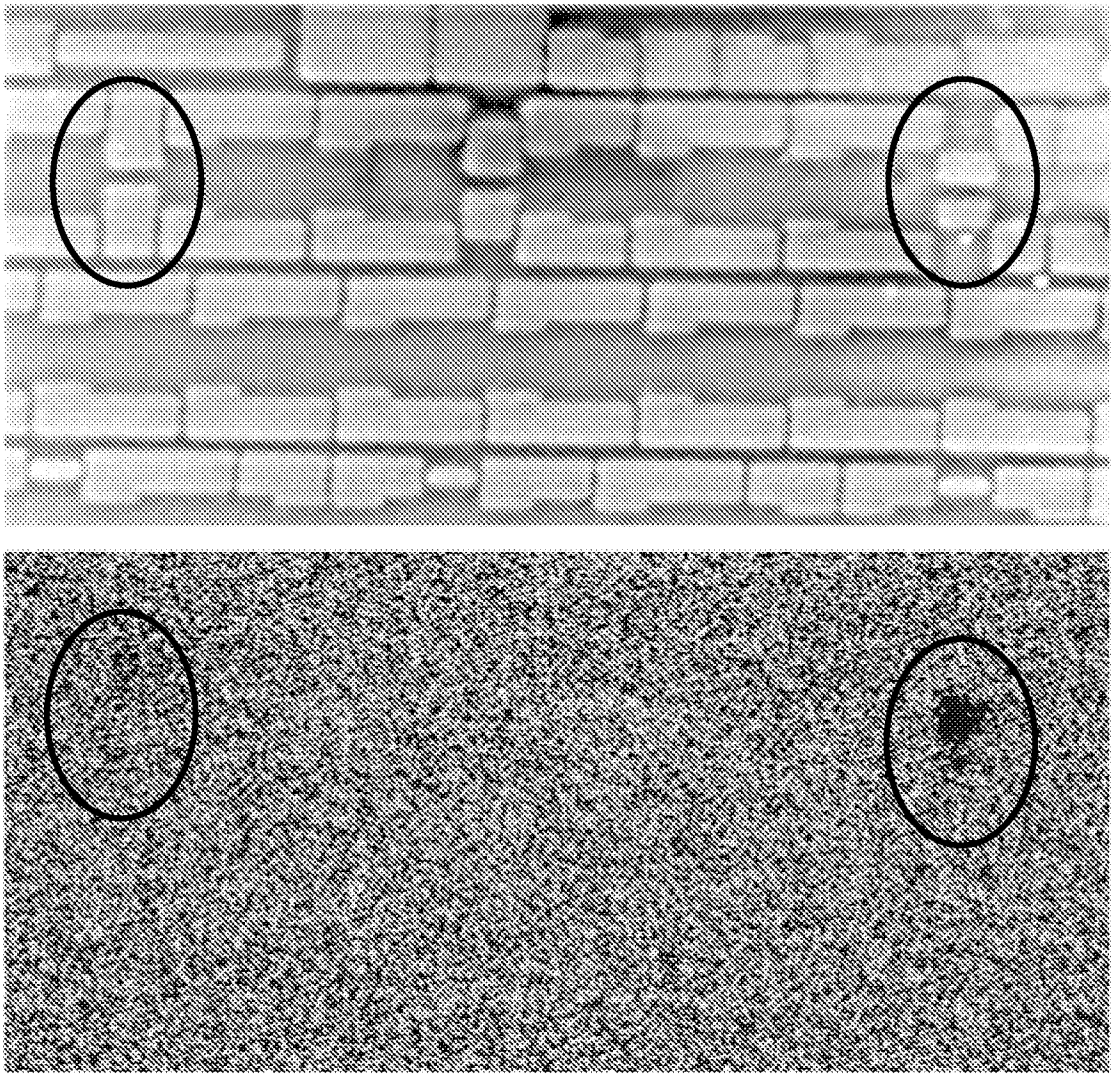


FIG. 2

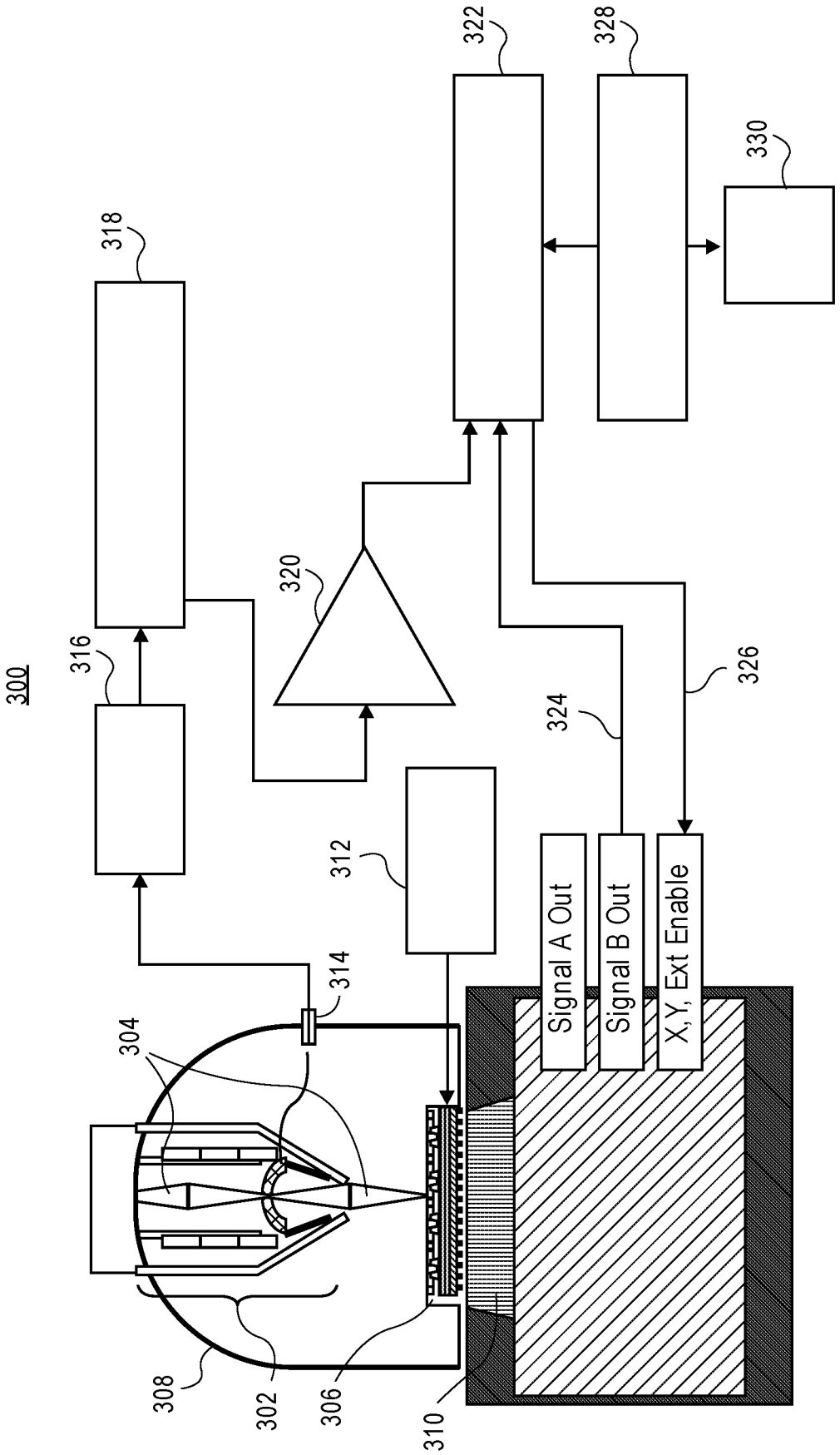

300
302
304
306
308
310
312
314
316
318
320
322
324
326
328
330
Signal A Out
Signal B Out
X, Y, Ext Enable

FIG. 3

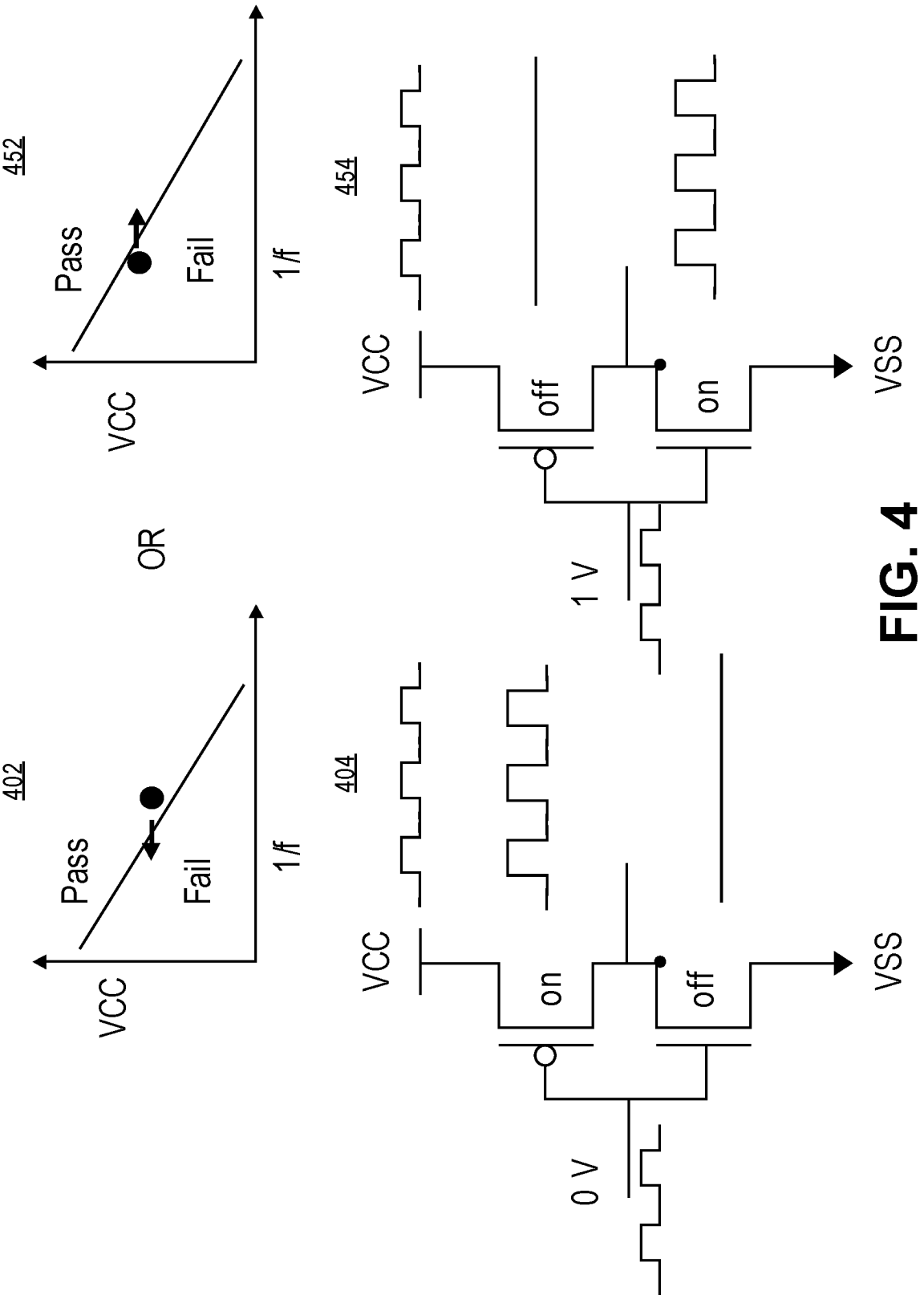

452
Pass
Fail
1/f
VCC
OR
402
Pass
Fail
1/f
VCC
454
VCC
off
on
VSS
1 V
404
VCC
on
off
VSS
0 V

FIG. 4

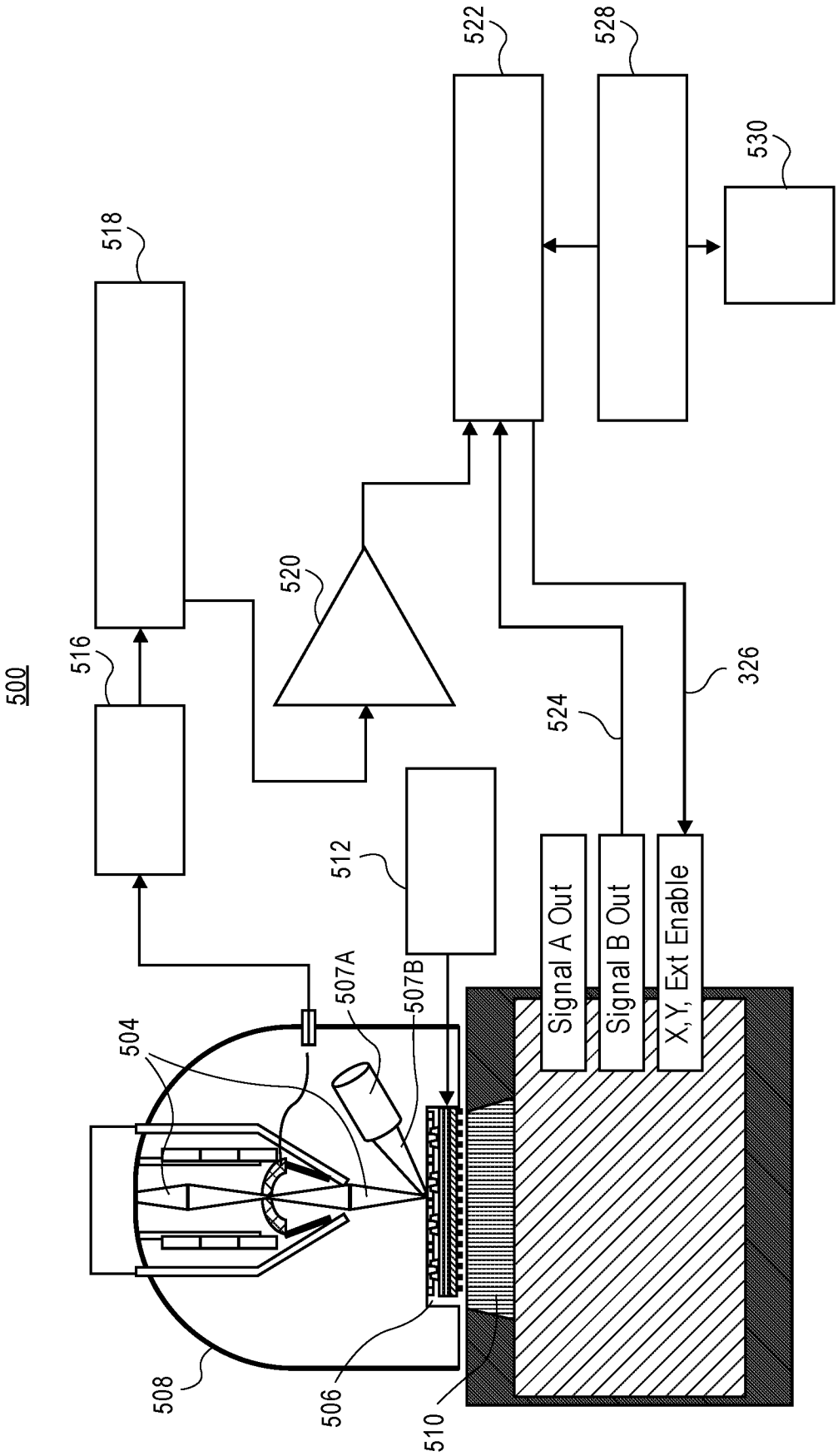

500
516
518
520
522
528
530
326
524
512
504
507A
507B
508
506
510
Signal A Out
Signal B Out
X, Y, Ext Enable

FIG. 5

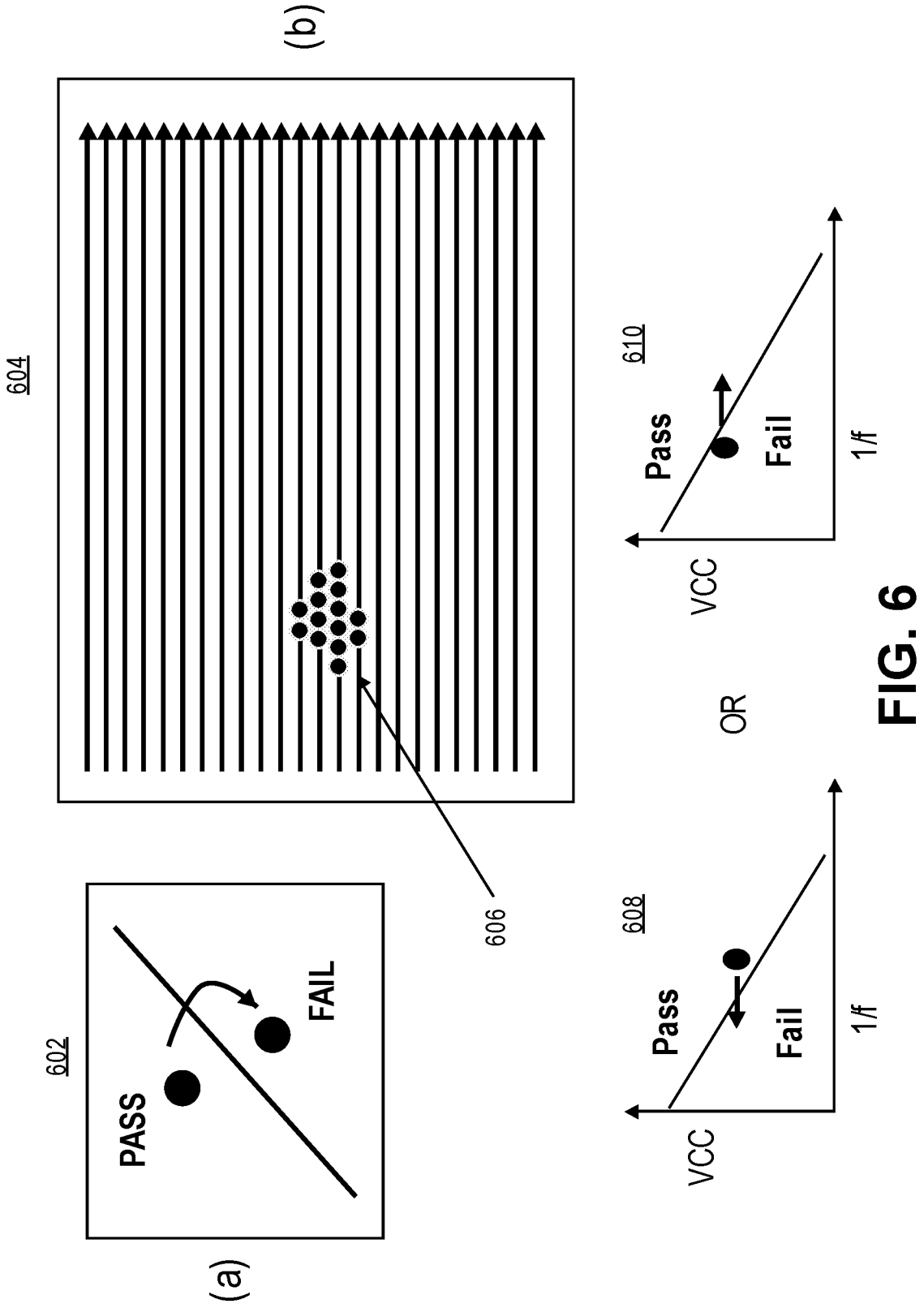

(a)
602
PASS
FAIL
(b)
604
606
608
Pass
Fail
VCC
1/f
OR
610
Pass
Fail
VCC
1/f

FIG. 6

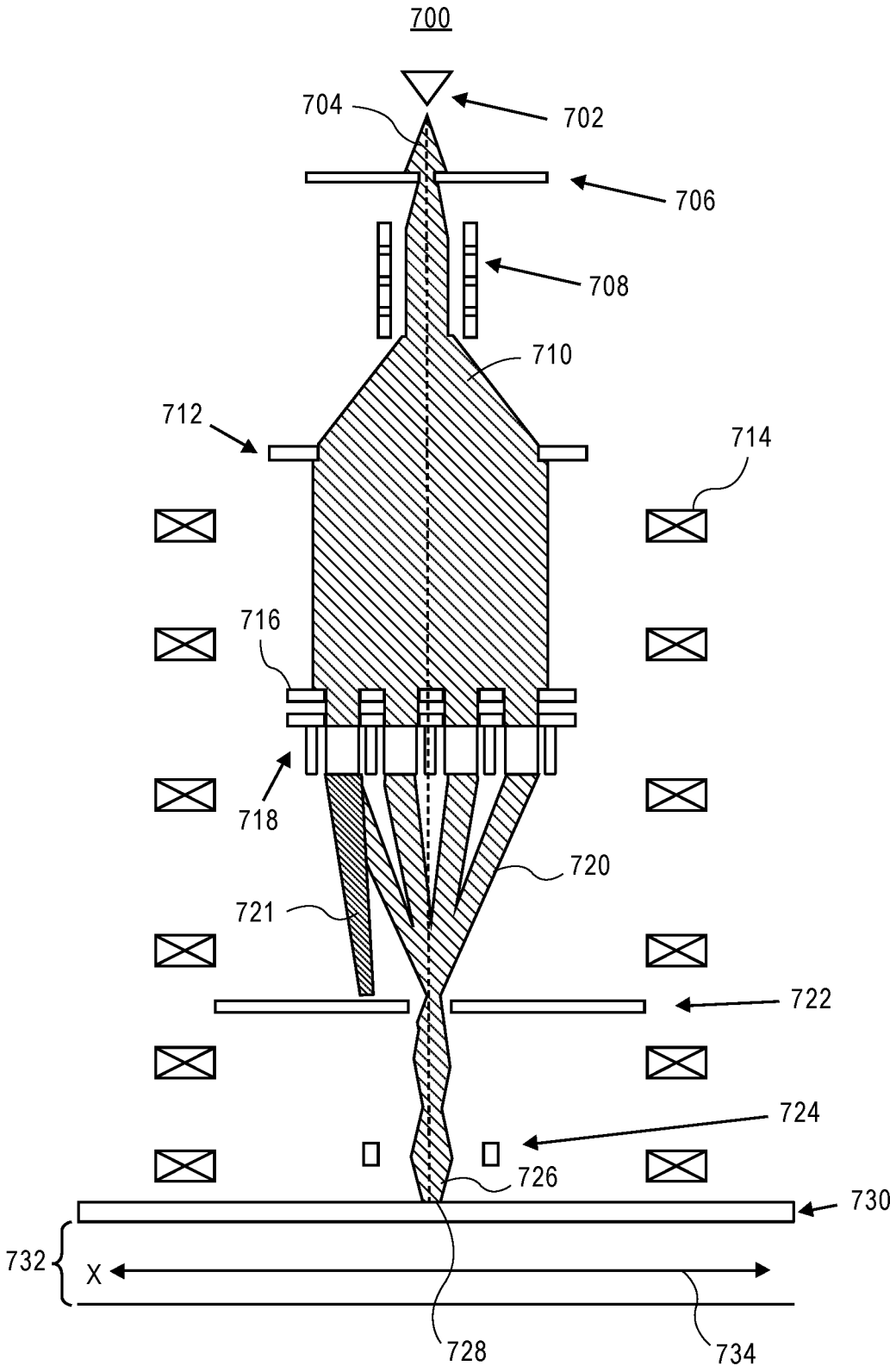

700
704
702
706
708
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712
714
716
718
720
721
722
724
726
730
732
X
728
734

FIG. 7

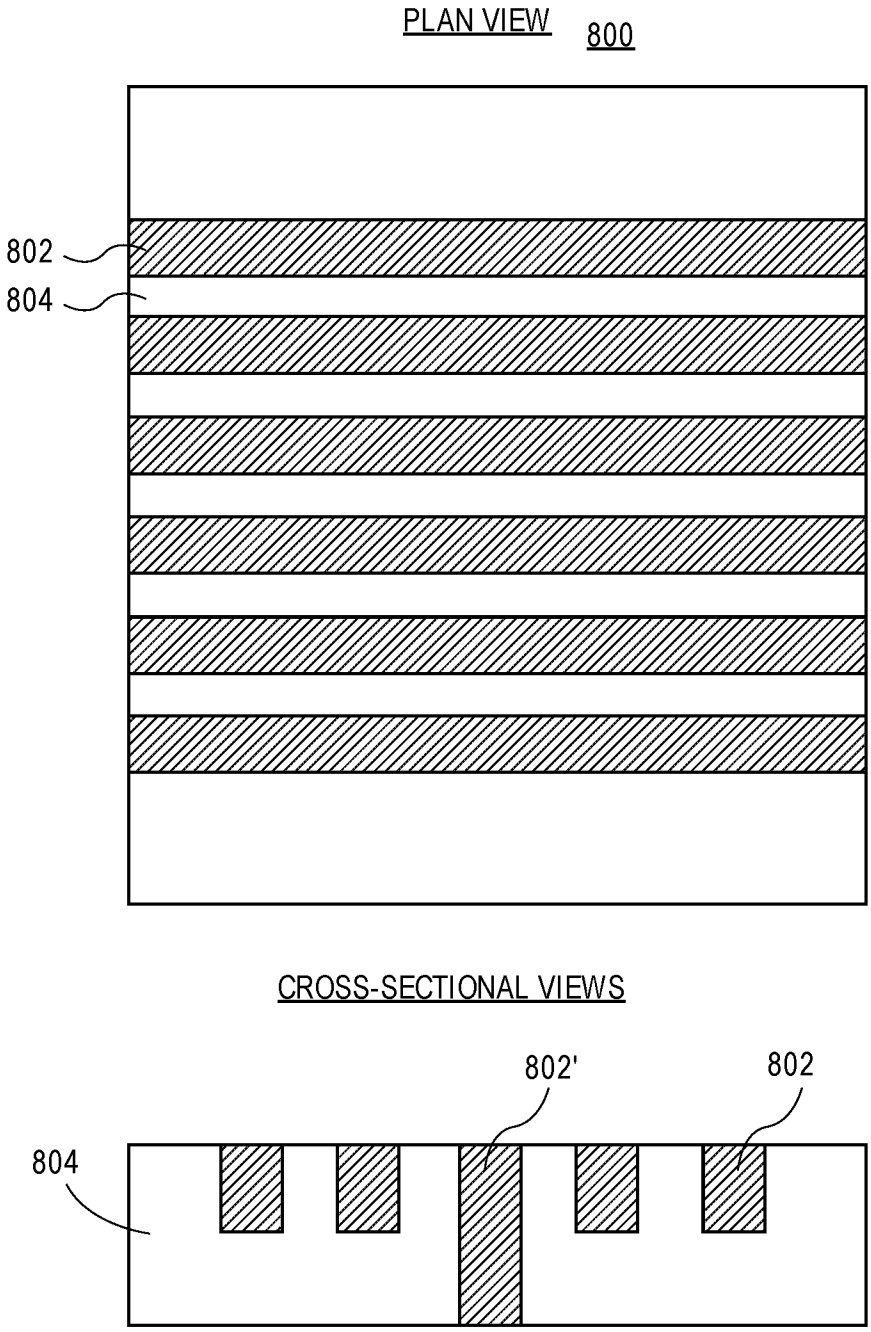


FIG. 8

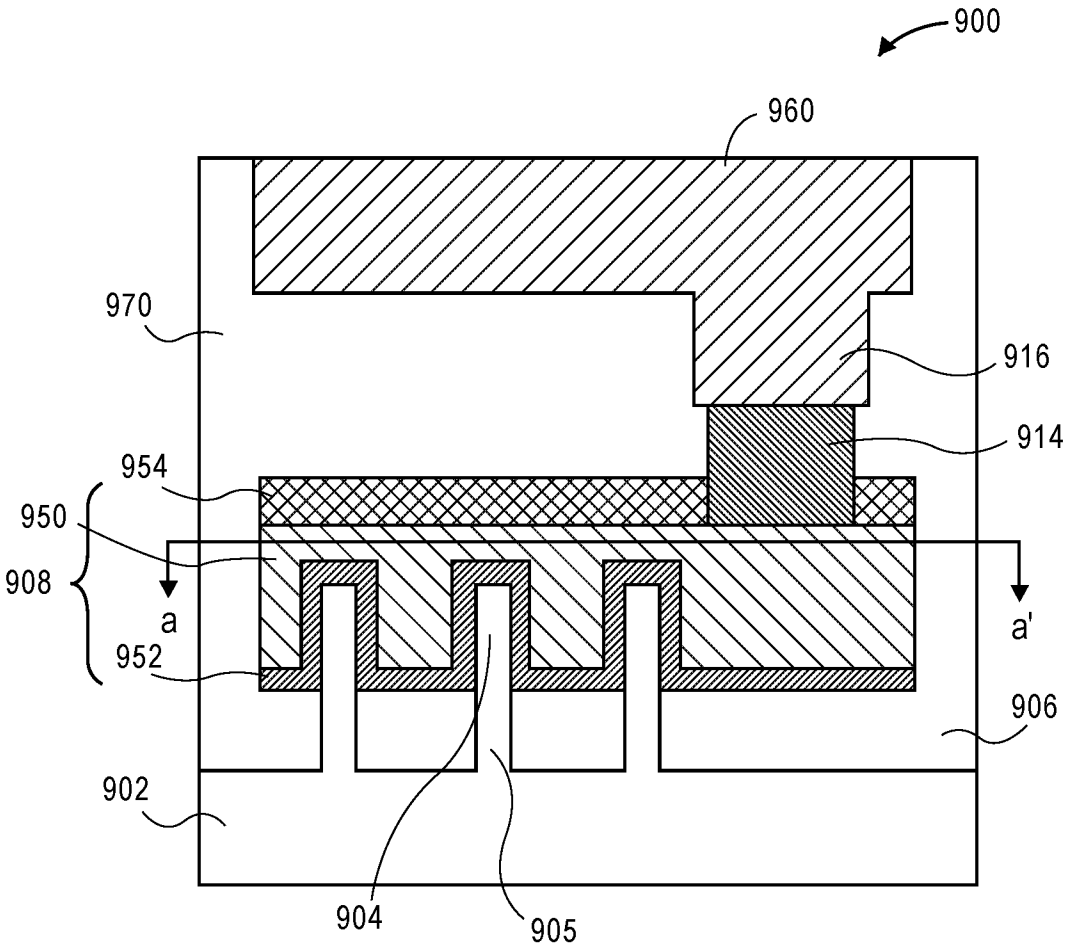

900
960
970
916
914
954
950
908
a
a'
952
906
902
904
905

FIG. 9A

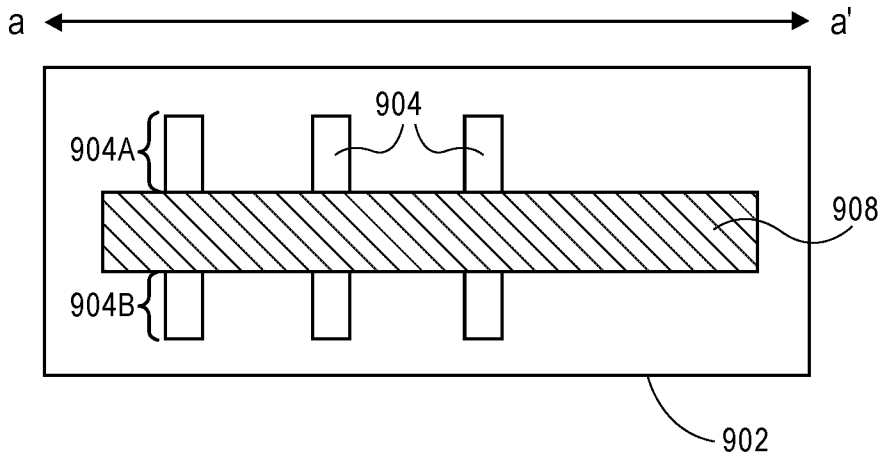

a
a'
904
904A
908
904B
902

FIG. 9B

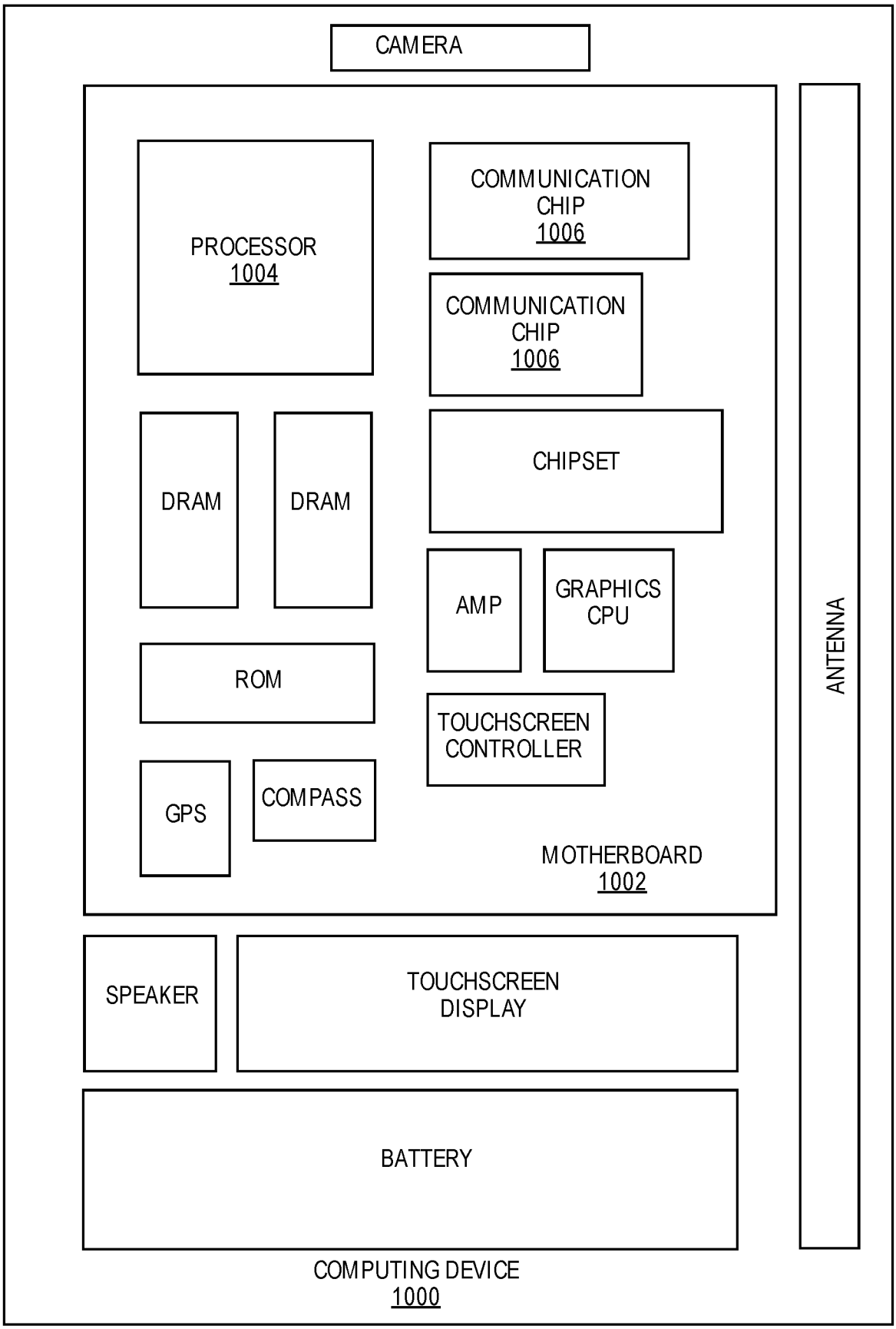

CAMERA
PROCESSOR
1004
COMMUNICATION
CHIP
1006
COMMUNICATION
CHIP
1006
DRAM
DRAM
CHIPSET
AMP
GRAPHICS
CPU
ROM
TOUCHSCREEN
CONTROLLER
GPS
COMPASS
MOTHERBOARD
1002
ANTENNA
SPEAKER
TOUCHSCREEN
DISPLAY
BATTERY
COMPUTING DEVICE
1000

FIG. 10

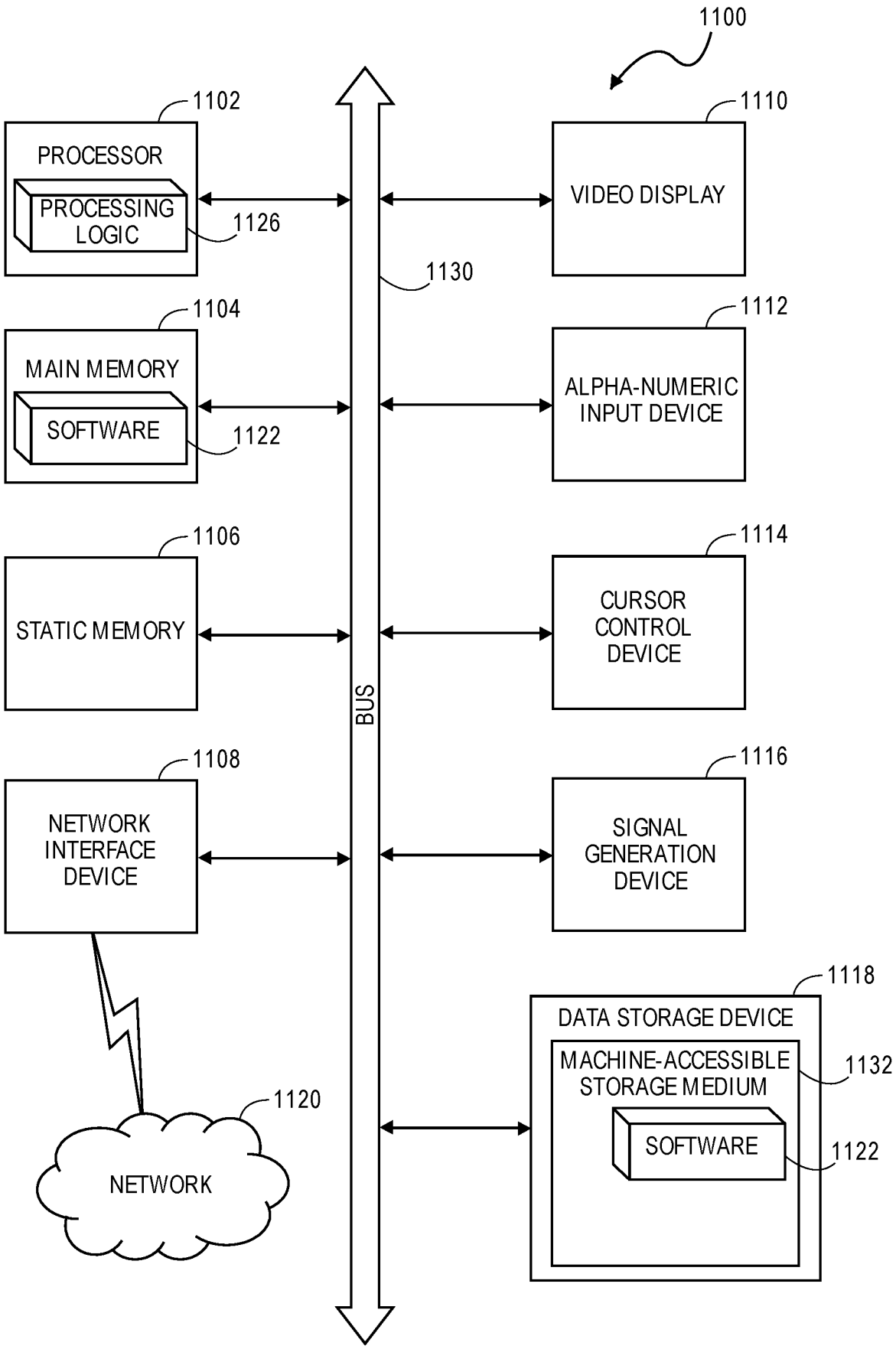

1100
1102
PROCESSOR
PROCESSING LOGIC
1126
1104
MAIN MEMORY
SOFTWARE
1122
1106
STATIC MEMORY
1108
NETWORK INTERFACE DEVICE
1120
NETWORK
BUS
1130
1110
VIDEO DISPLAY
1112
ALPHA-NUMERIC INPUT DEVICE
1114
CURSOR CONTROL DEVICE
1116
SIGNAL GENERATION DEVICE
1118
DATA STORAGE DEVICE
MACHINE-ACCESSIBLE STORAGE MEDIUM
1132
SOFTWARE
1122

FIG. 11

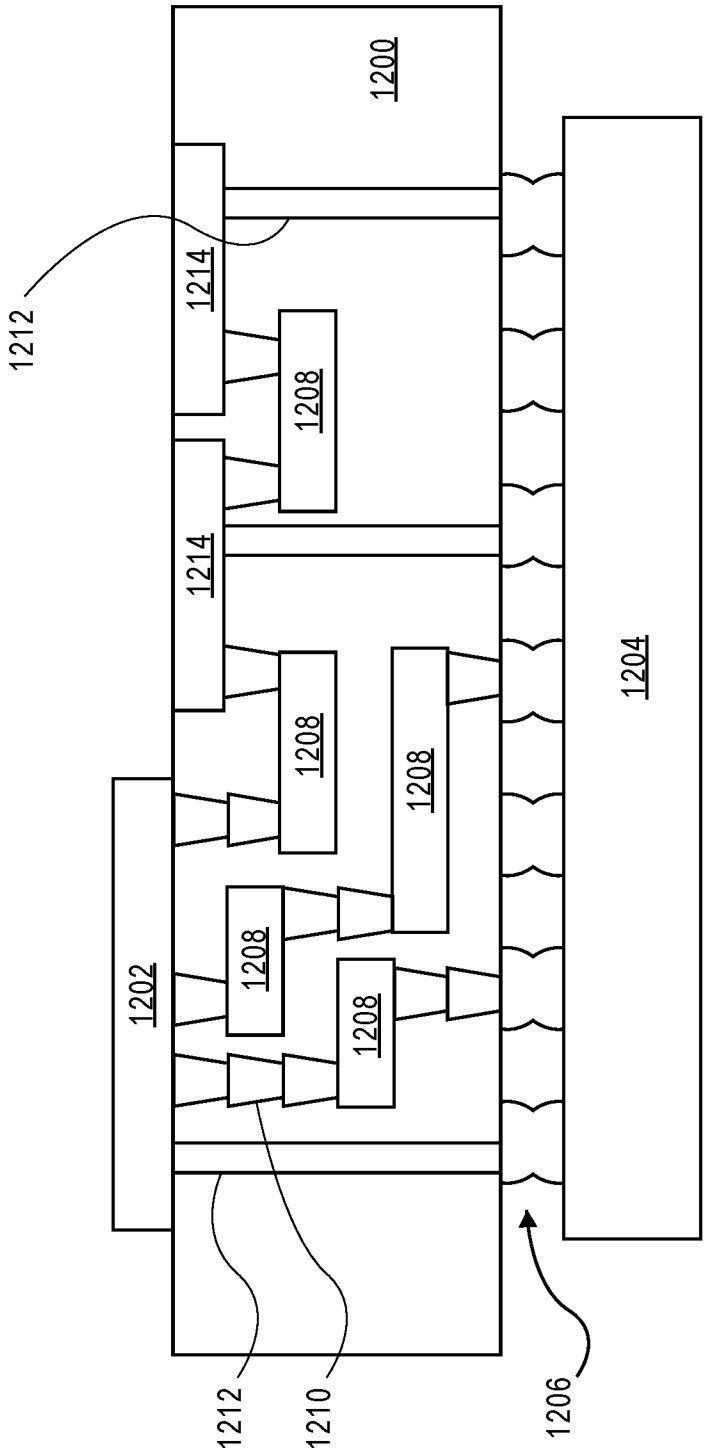

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1212
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1208
1214
1208
1208
1202
1208
1208
1204
1212
1210
1206

FIG. 12

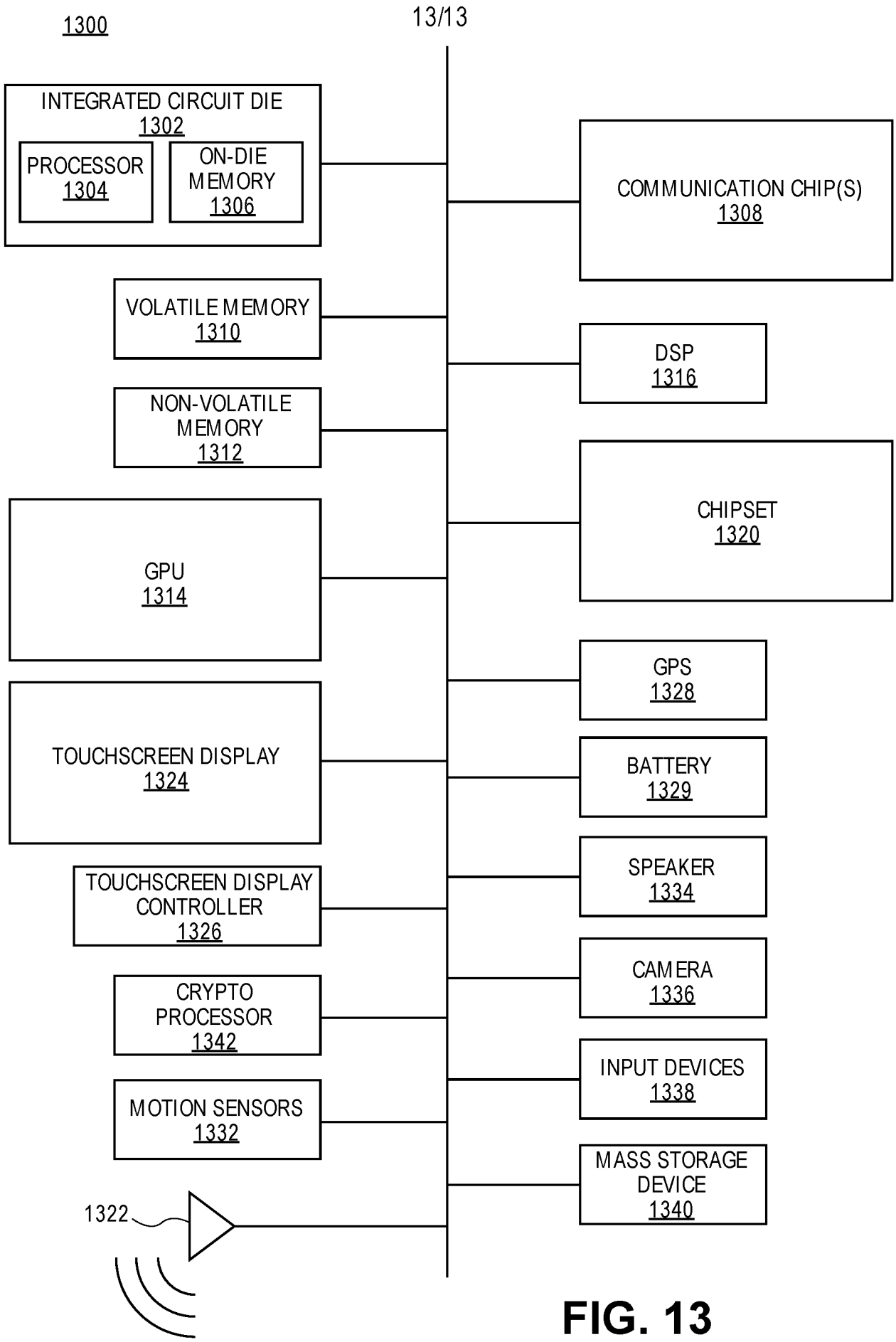

1300
INTEGRATED CIRCUIT DIE
1302
PROCESSOR
1304
ON-DIE
MEMORY
1306
VOLATILE MEMORY
1310
NON-VOLATILE
MEMORY
1312
GPU
1314
TOUCHSCREEN DISPLAY
1324
TOUCHSCREEN DISPLAY
CONTROLLER
1326
CRYPTO
PROCESSOR
1342
MOTION SENSORS
1332
1322
COMMUNICATION CHIP(S)
1308
DSP
1316
CHIPSET
1320
GPS
1328
BATTERY
1329
SPEAKER
1334
CAMERA
1336
INPUT DEVICES
1338
MASS STORAGE
DEVICE
1340

FIG. 13

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2017/053704

A. CLASSIFICATION OF SUBJECT MATTER

G01R 31/305(2006.01)i, H01J 37/26(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
G01R 31/305; G01R 31/3177; H01M 10/48; C25B 3/00; G01R 31/303; G01R 31/307; H01J 37/26

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords: electron, beam, integrated-circuit, image, illuminate

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2014-0331098 A1 (UNITED STATES OF AMERICA AS REPRESENTED BY THE SECRETARY OF THE NAVY) 06 November 2014 See paragraphs [17], [27]-[52]; claim 1; and figures 2, 5.	8-12
Y		1-7,13-20
Y	US 2014-0149811 A1 (ROSS et al.) 29 May 2014 See paragraphs [89]-[118]; claim 1; and figure 1A.	1-7,13-20
A	US 2016-0370425 A1 (DCG SYSTEMS INC.) 22 December 2016 See paragraphs [34]-[40]; claim 1; and figure 1.	1-20
A	US 2013-0186767 A1 (CASTRO et al.) 25 July 2013 See paragraphs [133]-[140]; claim 39; and figures 9, 10.	1-20
A	KR 10-2014-0101337 A (KABUSHIKI KAISHA NIHON MICRONICS et al.) 19 August 2014 See paragraphs [73]-[75]; claim 1; and figure 7.	1-20

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:
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"E" earlier application or patent but published on or after the international filing date
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"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
27 June 2018 (27.06.2018)	**27 June 2018 (27.06.2018)**

Name and mailing address of the ISA/KR
International Application Division
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Authorized officer
LEE, Myung Jin
Telephone No. +82-42-481-8474

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.
PCT/US2017/053704

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
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