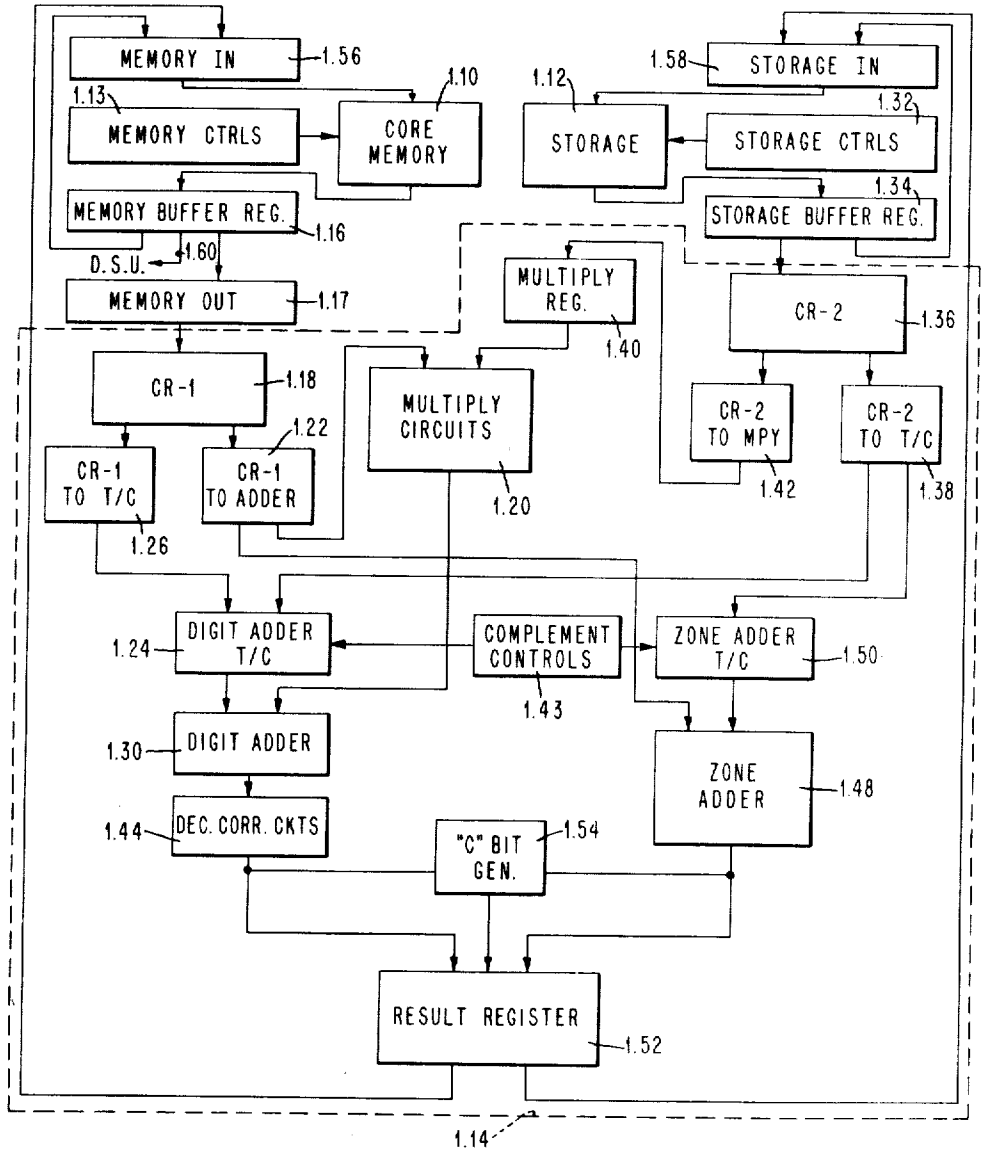
Oct. 16, 1962 W. R. DEMMER 3,059,222

TRANSFER INSTRUCTION

Filed Dec. 31, 1958 382 Sheets-Sheet 1

FIG. 1



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ATTORNEY

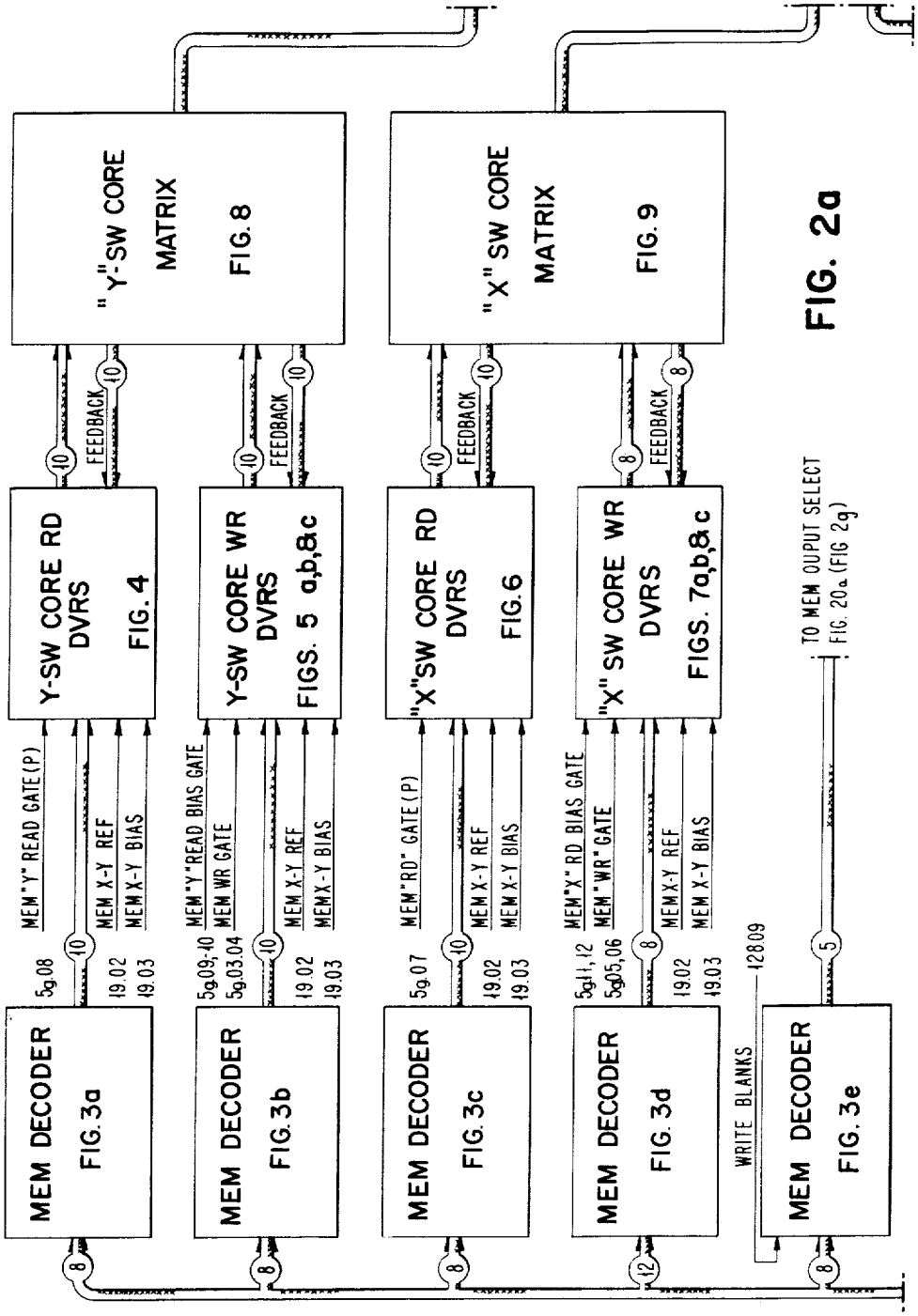
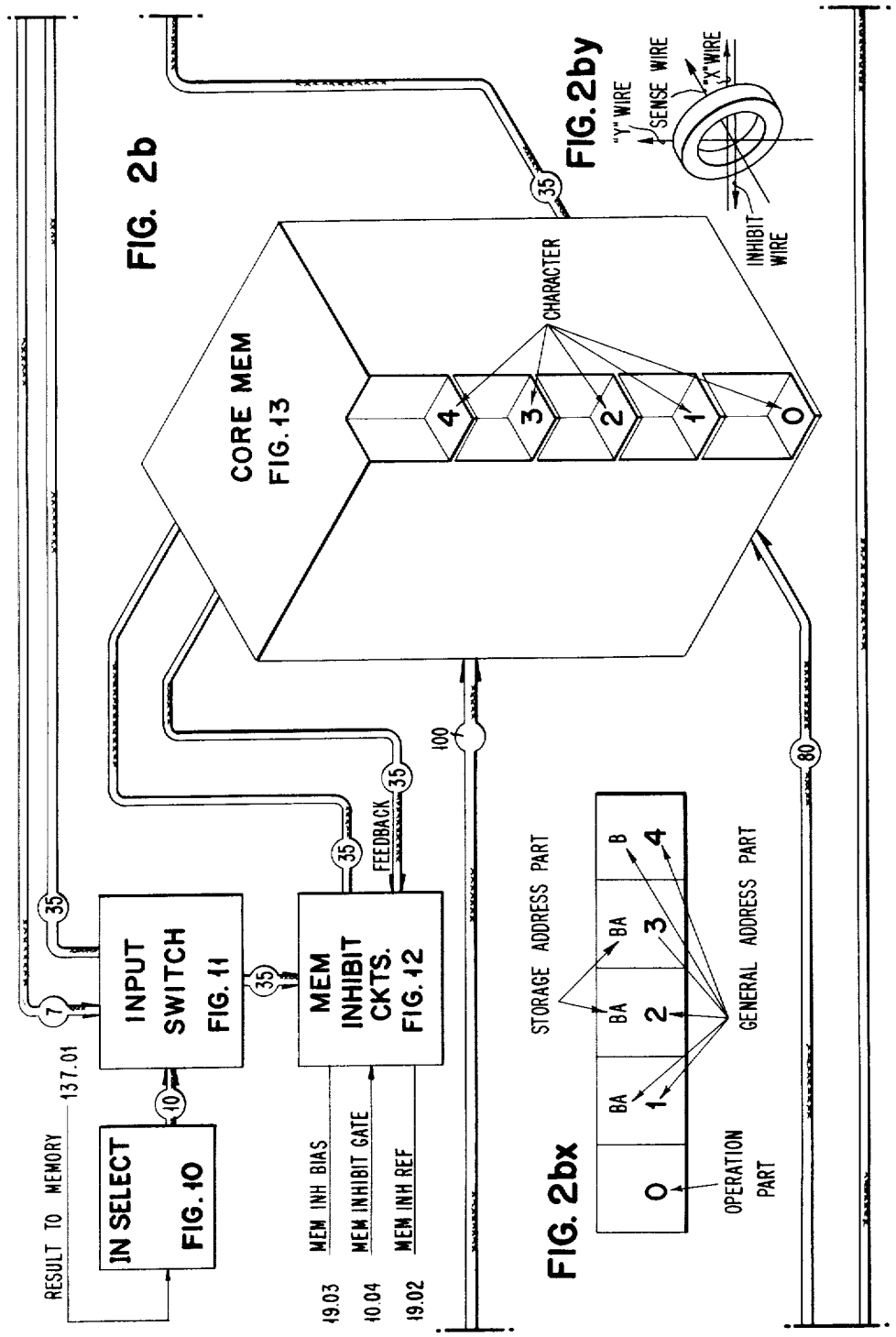

"Y"-SW CORE MATRIX FIG. 8
"X" SW CORE MATRIX FIG. 9
Y-SW CORE RD DVRS FIG. 4
Y-SW CORE WR DVRS FIGS. 5 a,b,&c
"X"SW CORE RD DVRS FIG. 6
"X" SW CORE WR DVRS FIGS. 7a,b,&c
FEEDBACK
MEM DECODER FIG. 3a
MEM DECODER FIG. 3b
MEM DECODER FIG. 3c
MEM DECODER FIG. 3d
MEM DECODER FIG. 3e
MEM "Y" READ GATE (P)
MEM "Y" READ BIAS GATE
MEM WR GATE
MEM "RD" GATE (P)
MEM "X" RD BIAS GATE
MEM "WR" GATE
MEM X-Y REF
MEM X-Y BIAS
WRITE BLANKS
TO MEM OUPUT SELECT FIG. 20a (FIG 2g)

FIG. 2a


FIG. 2b
FIG. 2by
"Y" WIRE
SENSE WIRE
"X" WIRE
INHIBIT WIRE
CHARACTER
CORE MEM
FIG. 13
4
3
2
1
0
35
100
80
FEEDBACK
INPUT SWITCH FIG. 11
MEM INHIBIT CKTS. FIG. 12
IN SELECT FIG. 10
RESULT TO MEMORY
137.01
MEM INH BIAS
MEM INHIBIT GATE
MEM INH REF
49.03
10.04
19.02
STORAGE ADDRESS PART
GENERAL ADDRESS PART
OPERATION PART
BA
B
FIG. 2bx

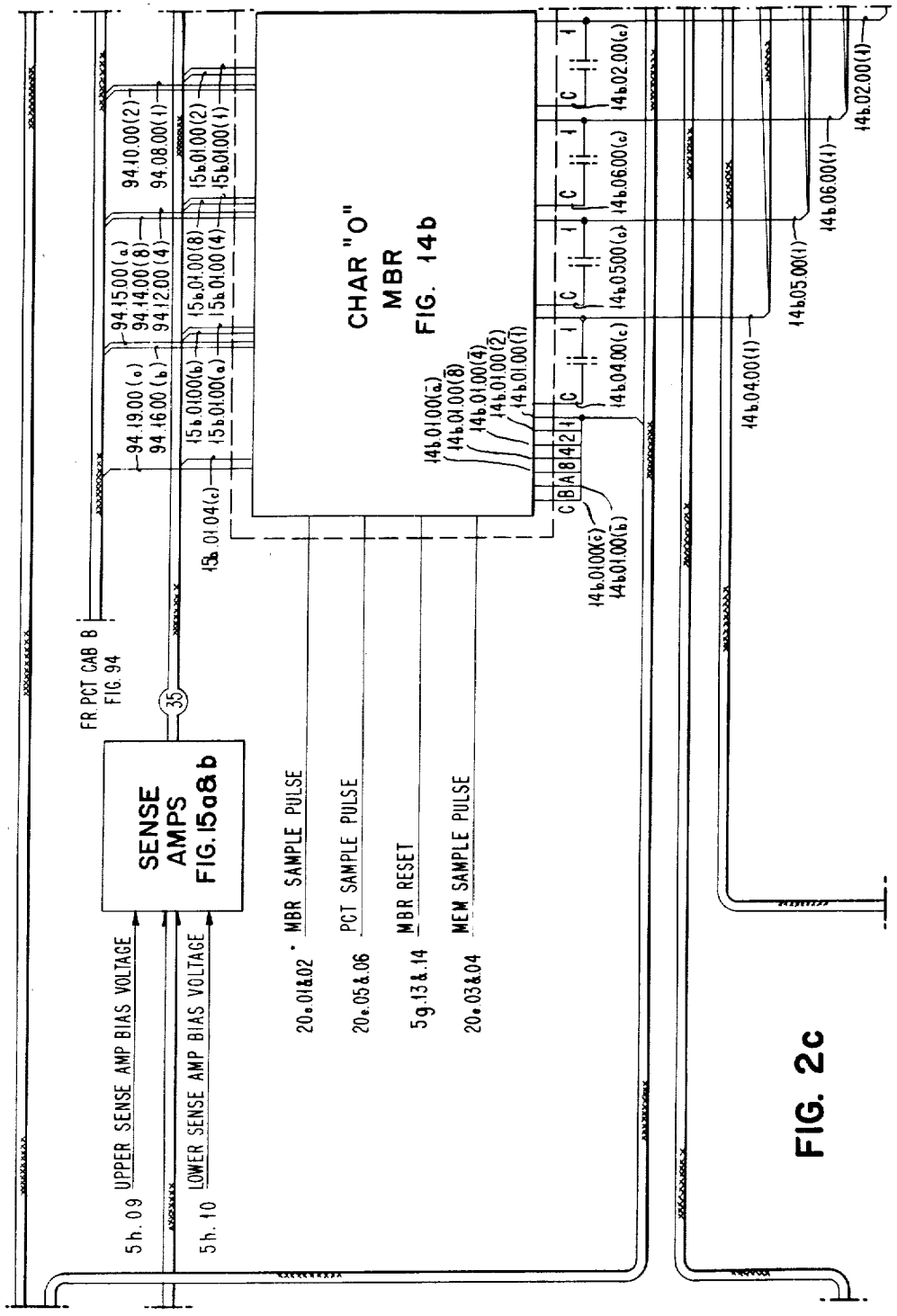
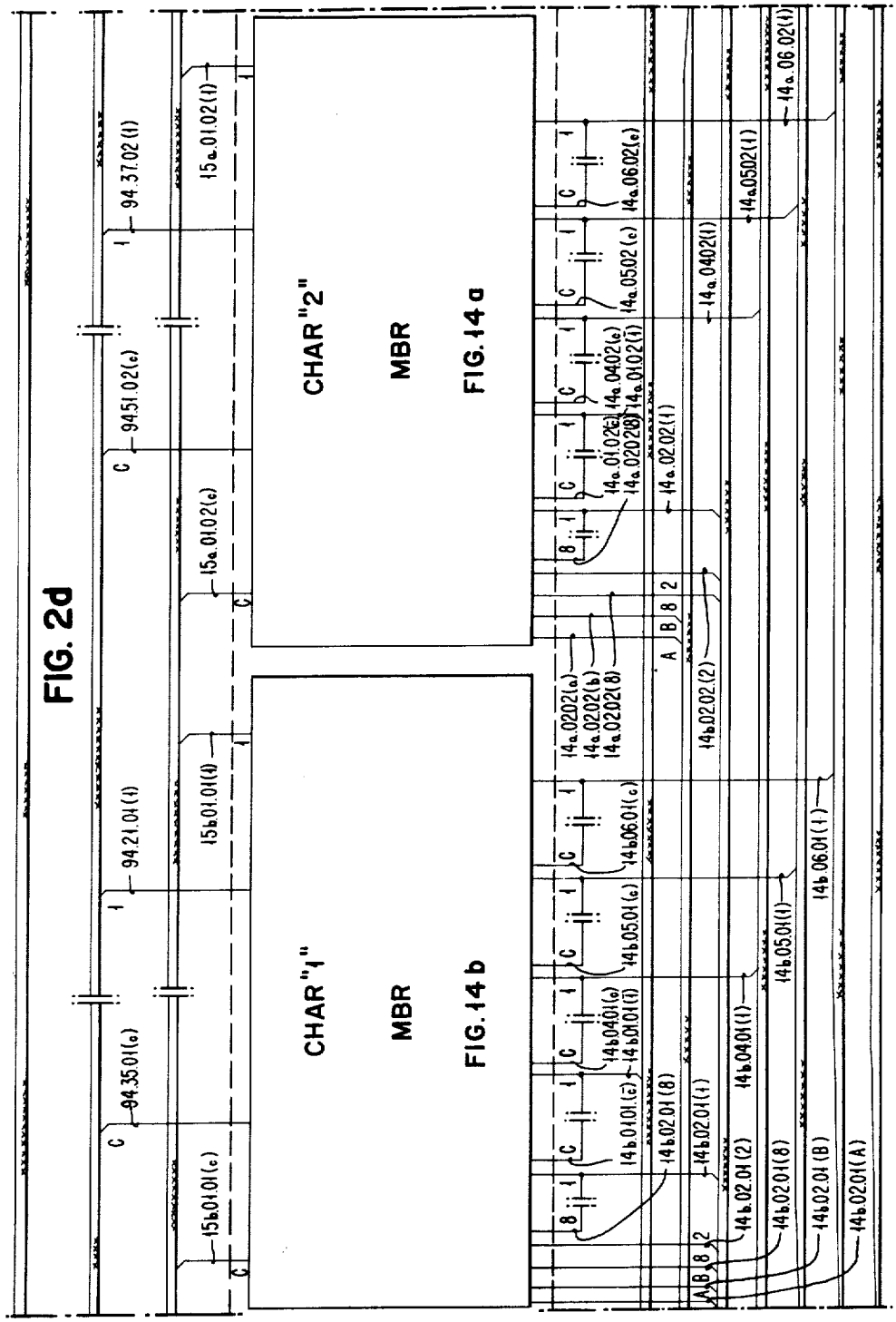

CHAR "O"
MBR
FIG. 14b
SENSE AMPS FIG. 15a&b
FR PCT CAB B FIG 94
5h.09 UPPER SENSE AMP BIAS VOLTAGE
5h.10 LOWER SENSE AMP BIAS VOLTAGE
20.01&02 MBR SAMPLE PULSE
20.05&06 PCT SAMPLE PULSE
5g.13&14 MBR RESET
20.03&04 MEM SAMPLE PULSE
94.19.00(a)
94.16.00(b)
94.15.00(a)
94.14.00(8)
94.12.00(4)
94.10.00(2)
94.08.00(1)
15b.01.04(c)
15b.01.00(a)
15b.01.00(b)
15b.01.00(4)
15b.01.00(8)
15b.01.00(2)
15b.01.00(1)
14b.01.00(a)
14b.01.00(8)
14b.01.00(4)
14b.01.00(2)
14b.01.00(1)
14b.01.00(c)
14b.01.00(b)
14b.04.00(c)
14b.05.00(c)
14b.06.00(c)
14b.02.00(c)
14b.04.00(1)
14b.05.00(1)
14b.06.00(1)
14b.02.00(1)

FIG. 2c


FIG. 2d
CHAR "2"
MBR
FIG. 14 a
CHAR "1"
MBR
FIG. 14 b

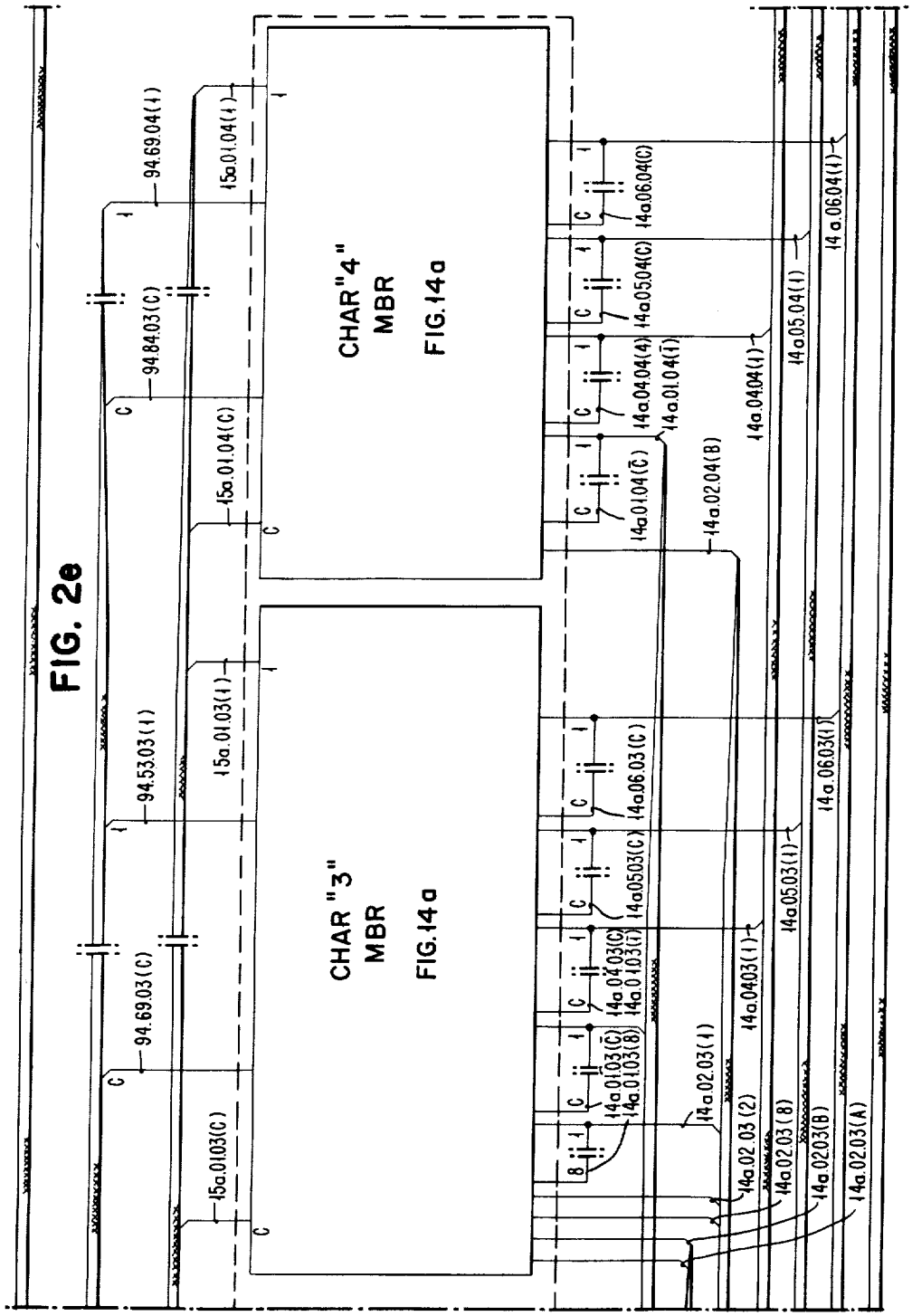

CHAR "4" MBR FIG. 14a
CHAR "3" MBR FIG. 14a
94.69.04(1)
15a.01.04(1)
94.84.03(C)
15a.01.04(C)
94.53.03(1)
15a.01.03(1)
94.69.03(C)
15a.0103(C)
14a.06.04(C)
14a.05.04(C)
14a.04.04(4)
14a.01.04(1)
14a.01.04(C)
14a.02.04(B)
14a.04.04(1)
14a.05.04(1)
14a.06.04(1)
14a.06.03(C)
14a.05.03(C)
14a.04.03(C)
14a.01.03(1)
14a.01.03(C)
14a.01.03(B)
14a.02.03(1)
14a.04.03(1)
14a.05.03(1)
14a.06.03(1)
14a.02.03(2)
14a.02.03(8)
14a.02.03(B)
14a.02.03(A)

FIG. 2e

FIG. 2f

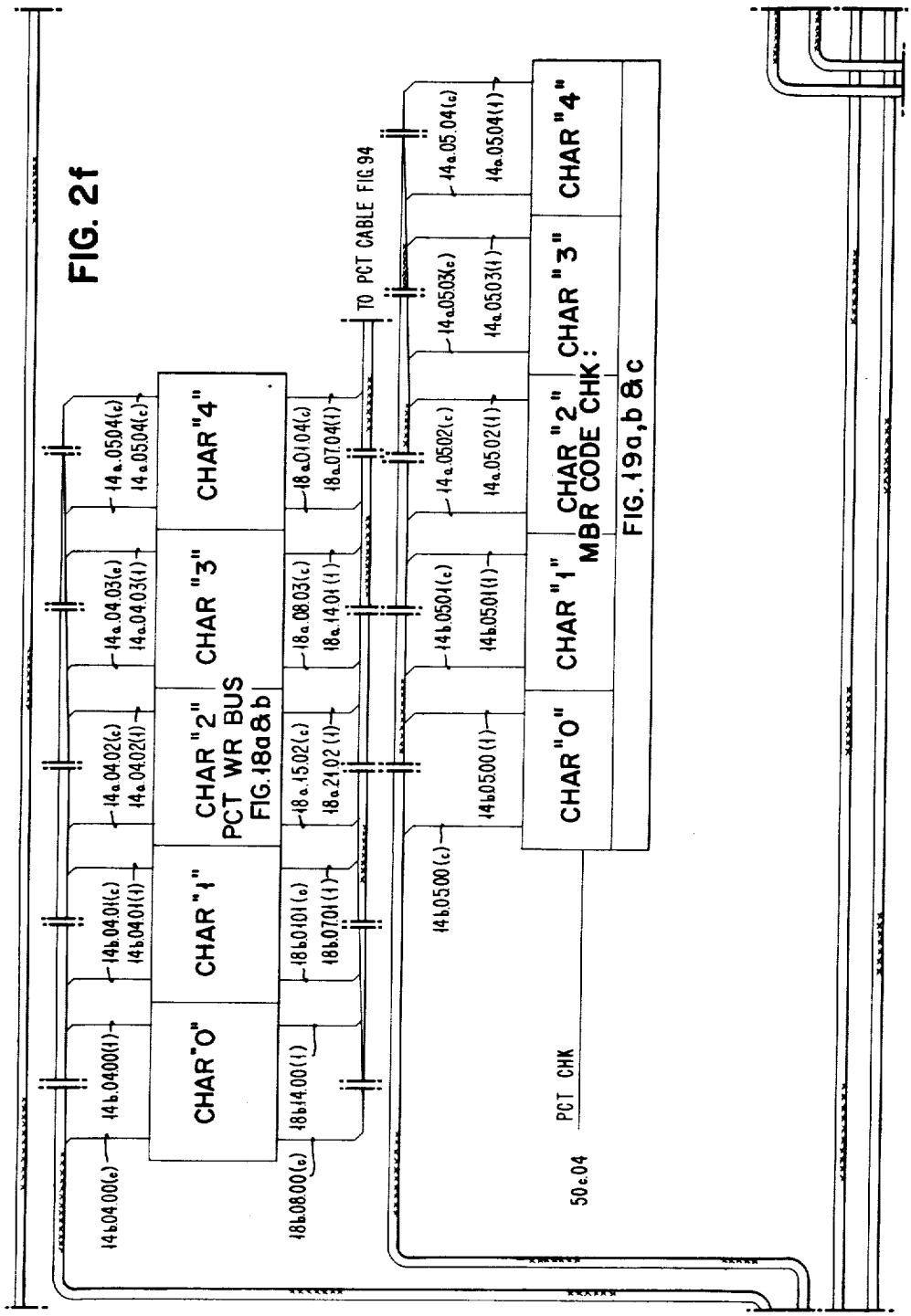

CHAR "0"
CHAR "1"
CHAR "2"
PCT WR BUS
FIG. 18a & b
CHAR "3"
CHAR "4"
CHAR "0"
CHAR "1"
CHAR "2"
MBR CODE CHK:
CHAR "3"
CHAR "4"
FIG. 19a, b & c
TO PCT CABLE FIG. 9A
PCT CHK
50.c.04
14b.0400(1)
14b.0401(1)
14a.0402(1)
14a.0403(1)
14a.0504(1)
14b.0500(1)
14b.0501(1)
14a.0502(1)
14a.0503(1)
14a.0504(1)
18b.0800(c)
18b.1400(1)
18b.0101(c)
18b.0701(1)
18a.2102(1)
18a.1401(1)
18a.0704(1)

FIG. 2g

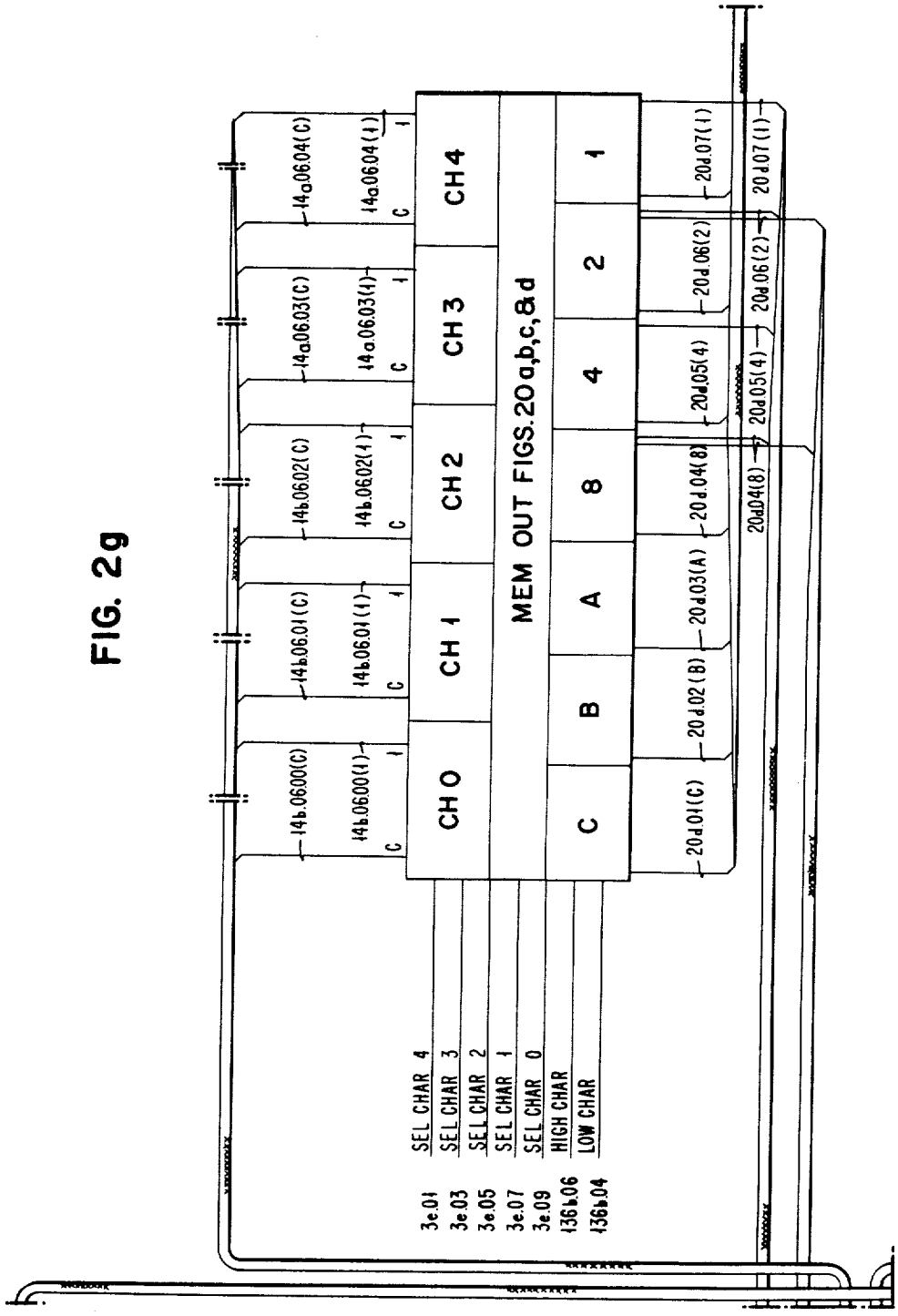

MEM OUT FIGS. 20a,b,c,&d
CH 0
CH 1
CH 2
CH 3
CH 4
C
B
A
8
4
2
1
14b.06.00(C)
14b.06.00(1)
14b.06.01(C)
14b.06.01(1)
14b.06.02(C)
14b.06.02(1)
14a.06.03(C)
14a.06.03(1)
14a.06.04(C)
14a.06.04(1)
20d.01(C)
20d.02(B)
20d.03(A)
20d.04(8)
20d.05(4)
20d.06(2)
20d.07(1)
SEL CHAR 4
SEL CHAR 3
SEL CHAR 2
SEL CHAR 1
SEL CHAR 0
HIGH CHAR
LOW CHAR
3e.01
3e.03
3e.05
3e.07
3e.09
136b.06
136b.04

FIG. 2h

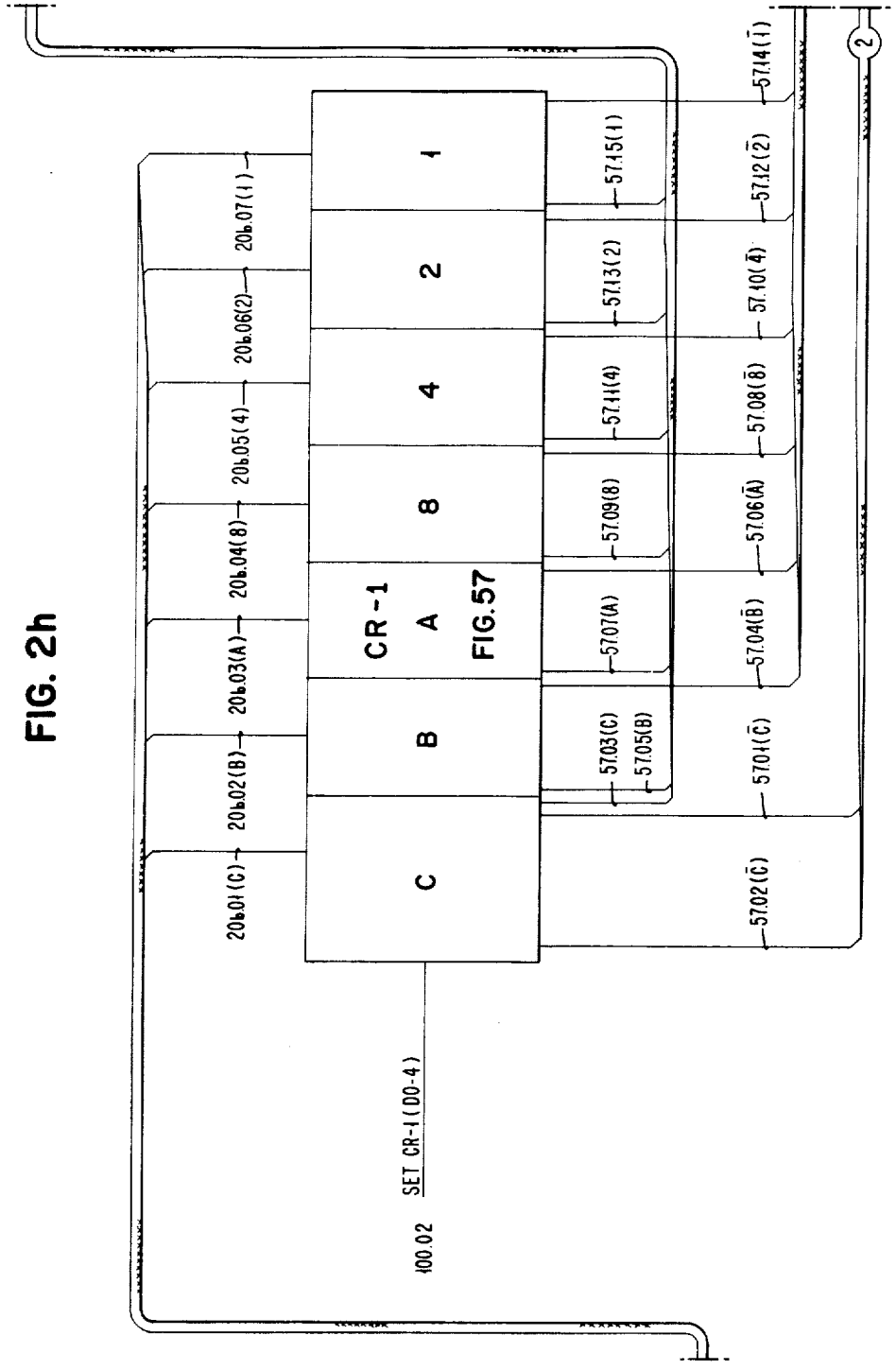

CR-1
A
B
C
1
2
4
8
FIG. 57
206.01(C)
206.02(B)
206.03(A)
206.04(8)
206.05(4)
206.06(2)
206.07(1)
57.01(C̄)
57.02(C̄)
57.03(C)
57.04(B̄)
57.05(B)
57.06(Ā)
57.07(A)
57.08(8̄)
57.09(8)
57.10(4̄)
57.11(4)
57.12(2̄)
57.13(2)
57.14(1̄)
57.15(1)
2
100.02
SET CR-1 (00-4)

FIG. 2i

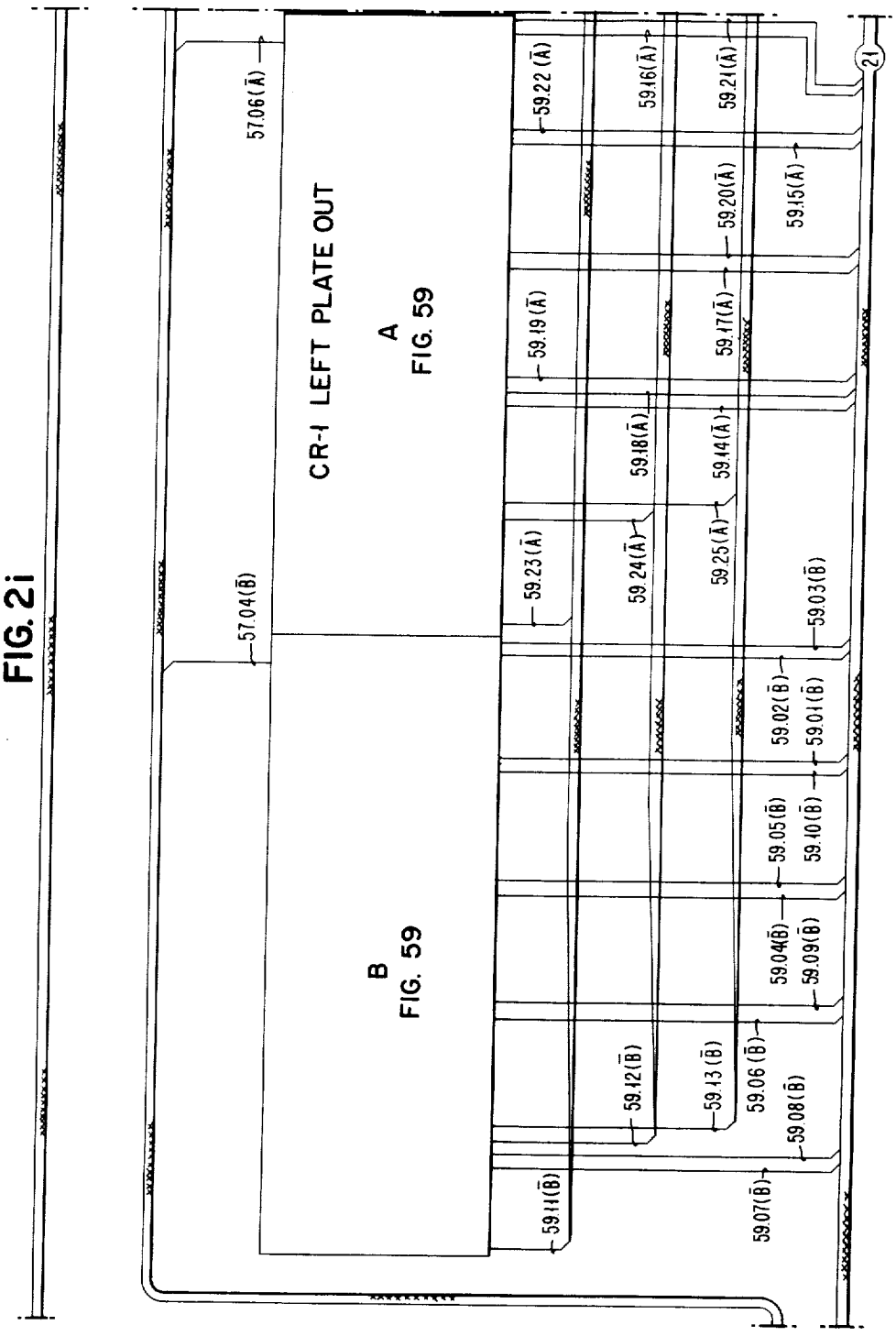

CR-1 LEFT PLATE OUT
A
FIG. 59
B
FIG. 59
57.06(Ā)
57.04(B̄)
59.22(Ā)
59.16(Ā)
59.21(Ā)
59.15(Ā)
59.20(Ā)
59.19(Ā)
59.17(Ā)
59.18(Ā)
59.14(Ā)
59.23(Ā)
59.24(Ā)
59.25(Ā)
59.03(B̄)
59.02(B̄)
59.01(B̄)
59.05(B̄)
59.10(B̄)
59.04(B̄)
59.09(B̄)
59.12(B̄)
59.13(B̄)
59.06(B̄)
59.08(B̄)
59.11(B̄)
59.07(B̄)
21

FIG. 2j

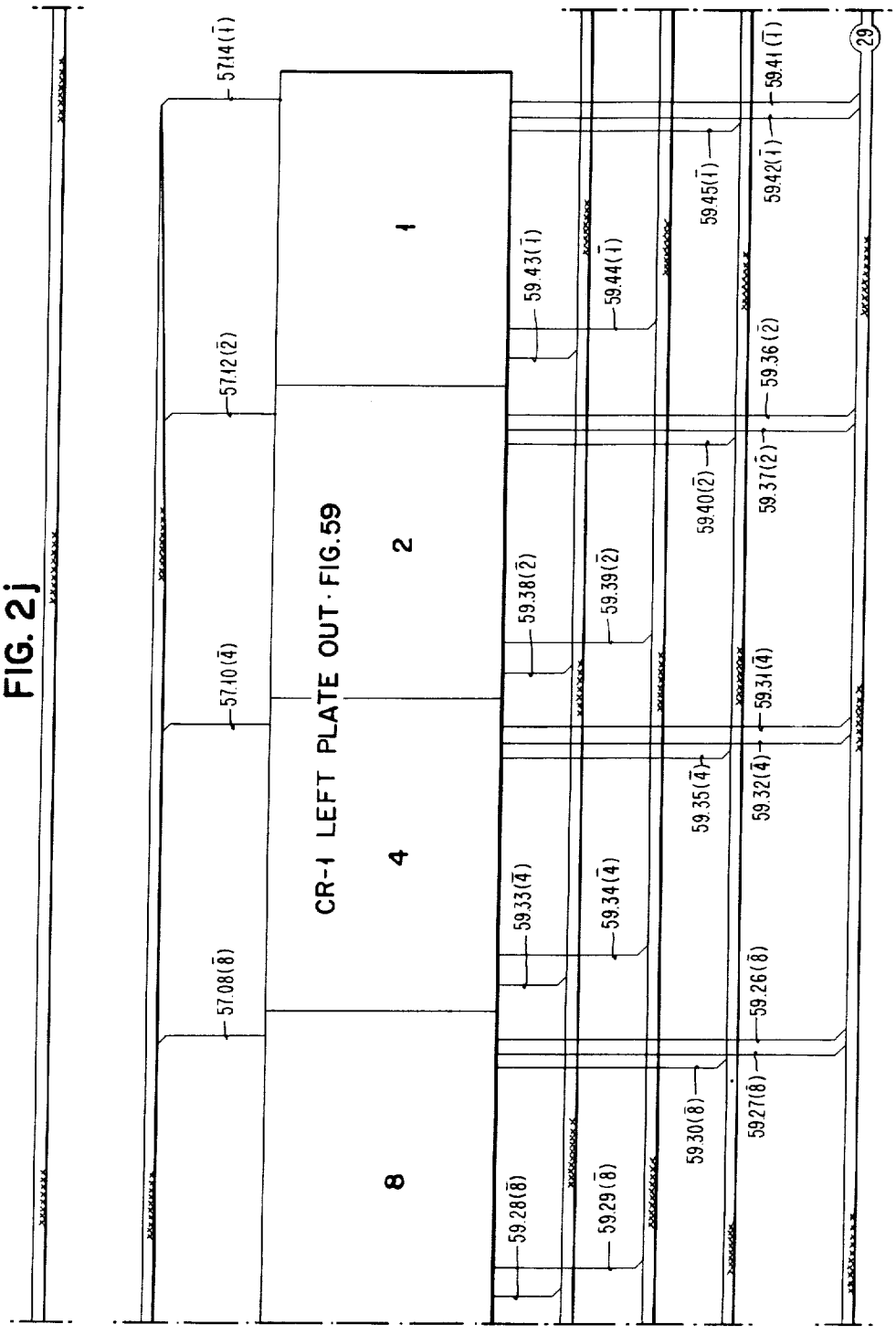

CR-1 LEFT PLATE OUT · FIG.59
1
2
4
8
57.14(1̄)
57.12(2̄)
57.10(4̄)
57.08(8̄)
59.43(1̄)
59.44(1̄)
59.45(1̄)
59.42(1̄)
59.41(1̄)
59.38(2̄)
59.39(2̄)
59.40(2̄)
59.37(2̄)
59.36(2̄)
59.33(4̄)
59.34(4̄)
59.35(4̄)
59.32(4̄)
59.31(4̄)
59.28(8̄)
59.29(8̄)
59.30(8̄)
59.27(8̄)
59.26(8̄)
29

FIG. 2k

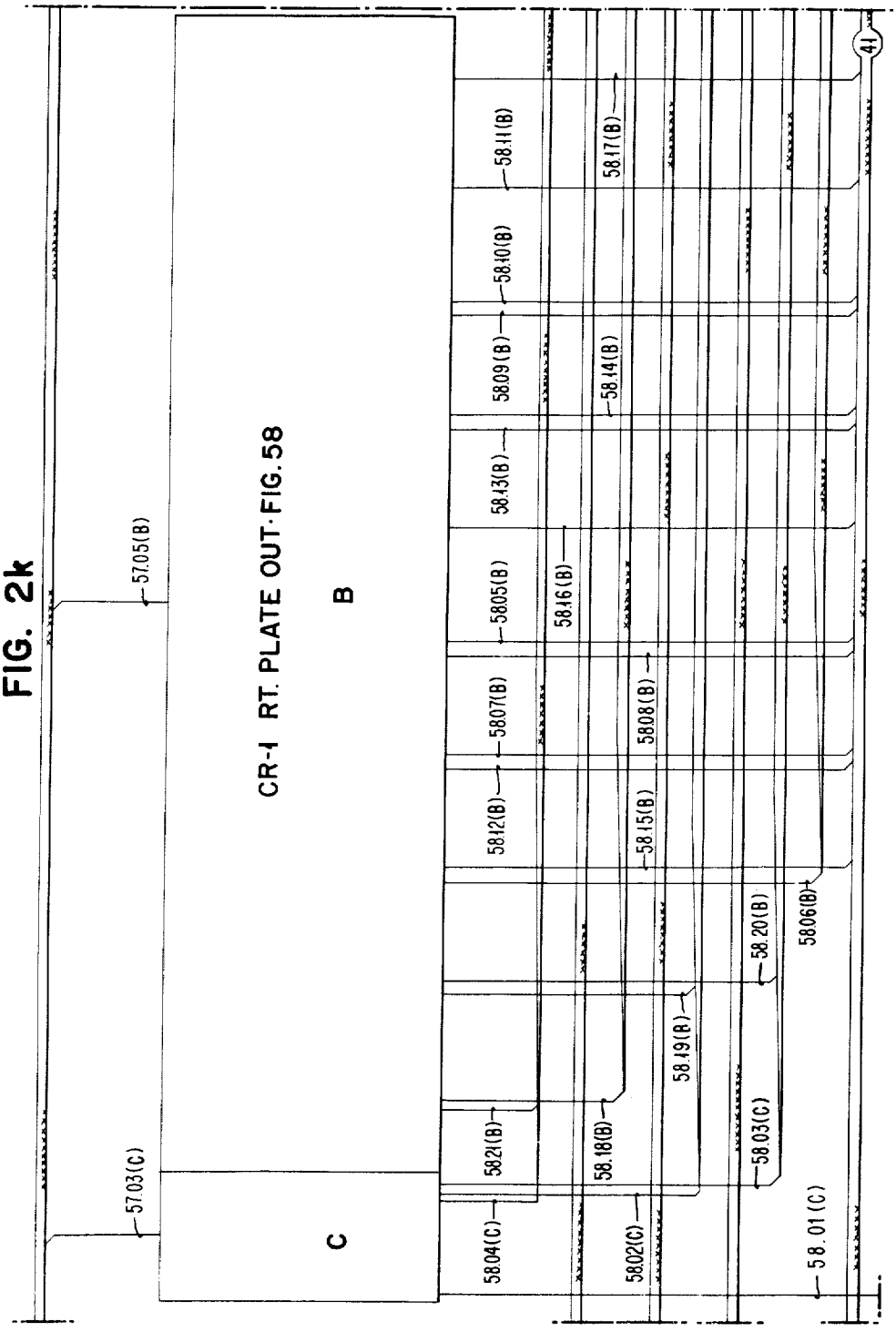

CR-1 RT. PLATE OUT-FIG. 58
B
C
57.05(B)
57.03(C)
58.11(B)
58.17(B)
58.10(B)
58.09(B)
58.14(B)
58.13(B)
58.16(B)
58.05(B)
58.07(B)
58.08(B)
58.12(B)
58.15(B)
58.06(B)
58.20(B)
58.19(B)
58.18(B)
58.21(B)
58.03(C)
58.04(C)
58.02(C)
58.01(C)
41

FIG. 21

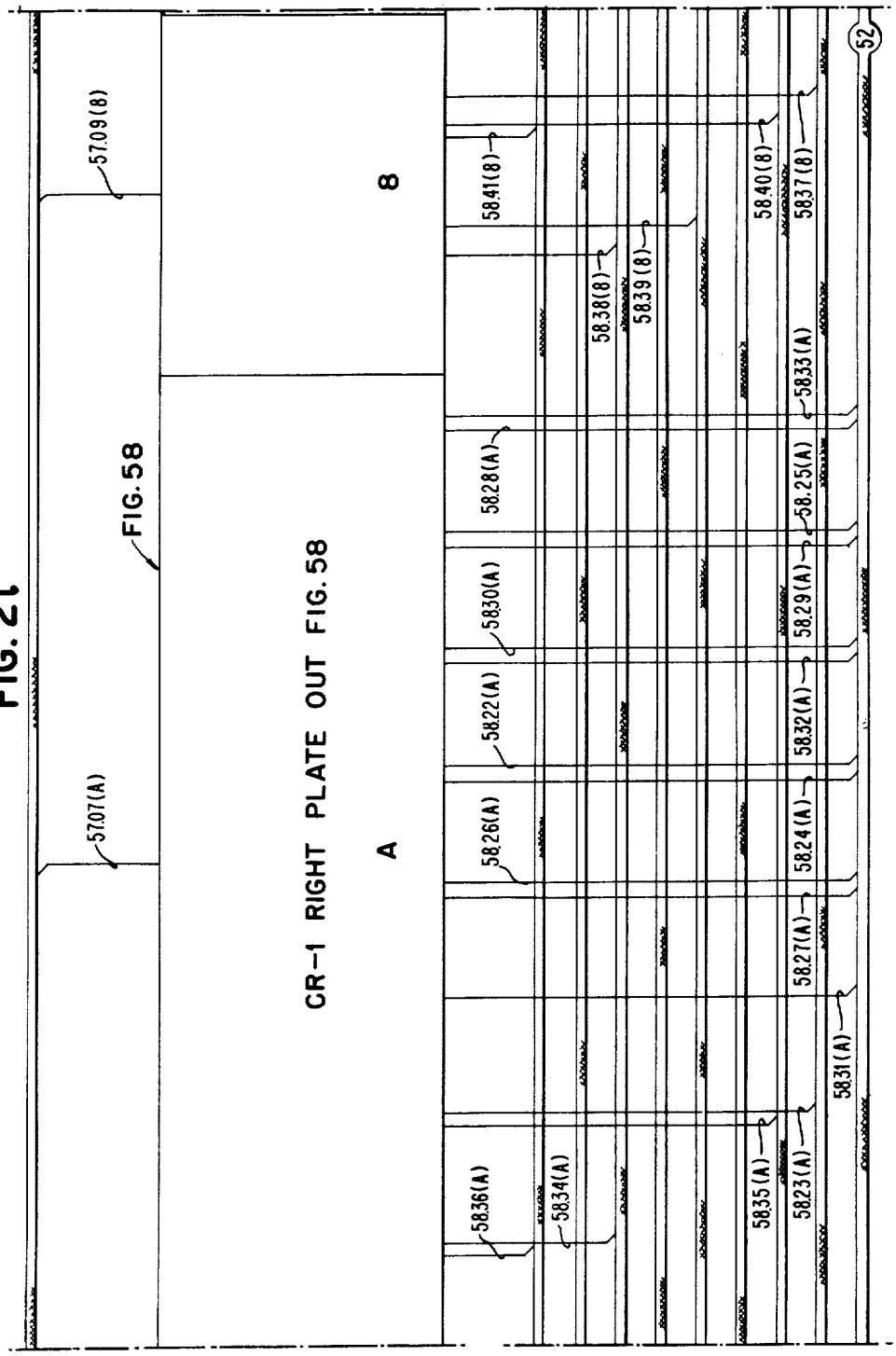

FIG. 58
57.09(8)
57.07(A)
8
A
CR-1 RIGHT PLATE OUT FIG. 58
58.41(8)
58.38(8)
58.39(8)
58.40(8)
58.37(8)
58.28(A)
58.33(A)
58.25(A)
58.30(A)
58.29(A)
58.22(A)
58.32(A)
58.26(A)
58.24(A)
58.27(A)
58.31(A)
58.36(A)
58.34(A)
58.35(A)
58.23(A)
52

FIG. 2m

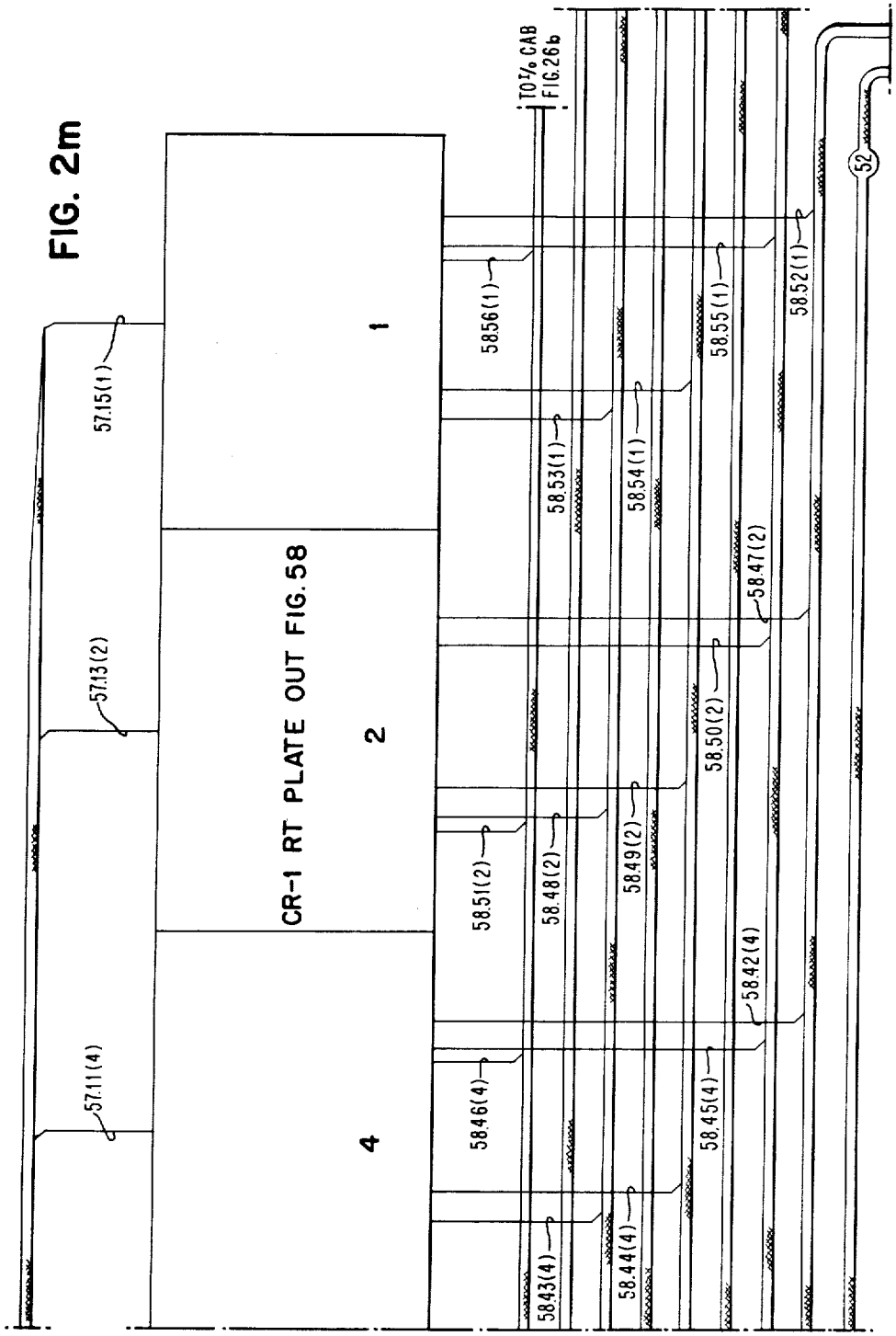
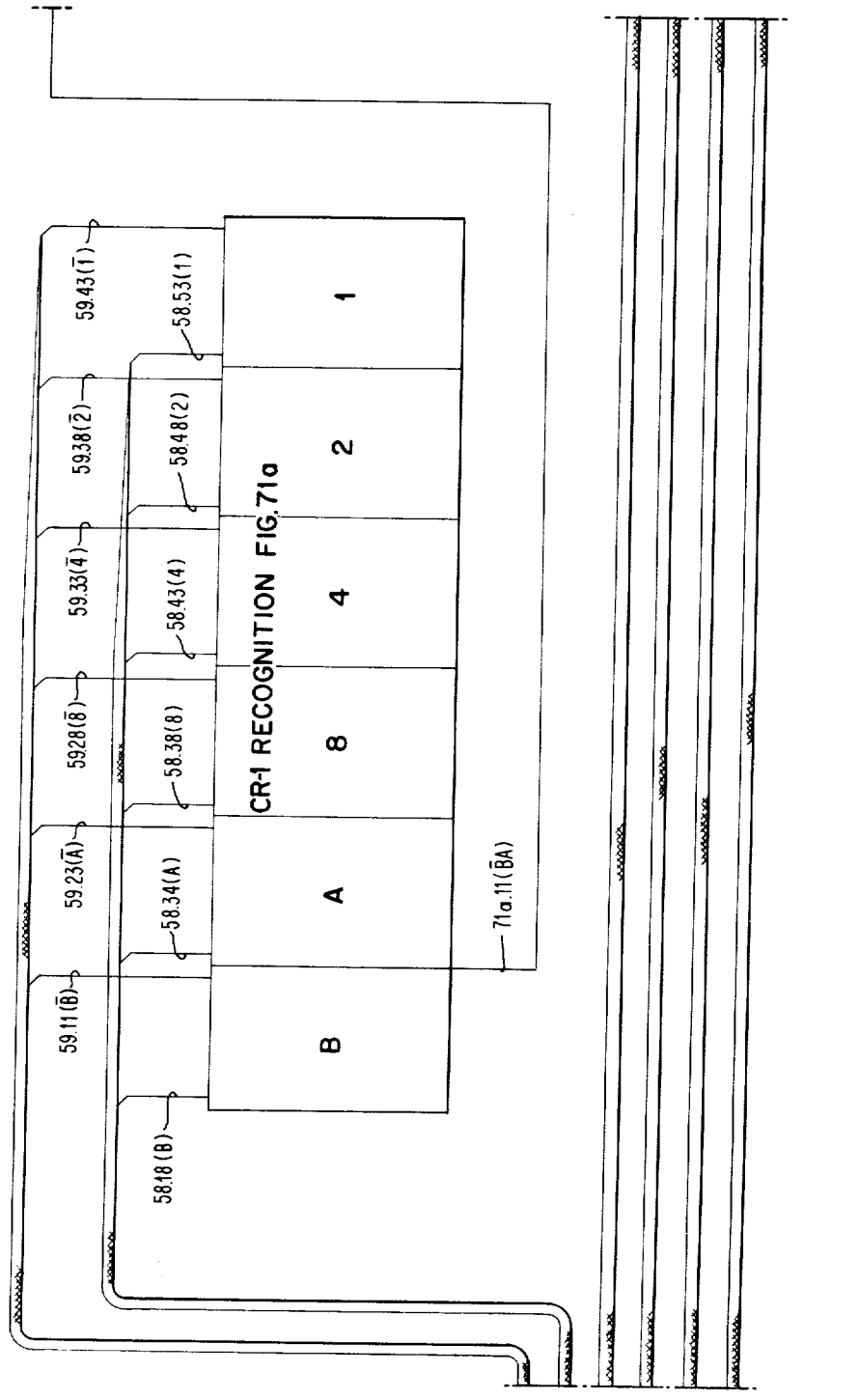

TO 1% CAB FIG. 26b
52
58.56(1)
58.55(1)
58.52(1)
58.53(1)
58.54(1)
58.47(2)
58.50(2)
58.51(2)
58.48(2)
58.49(2)
58.42(4)
58.46(4)
58.45(4)
58.43(4)
58.44(4)
57.15(1)
57.13(2)
57.11(4)
1
2
4
CR-1 RT PLATE OUT FIG. 58

FIG. 2n


59.43(1̄)
58.53(1)
59.38(2̄)
58.48(2)
59.33(4̄)
58.43(4)
59.28(8̄)
58.38(8)
59.23(Ā)
58.34(A)
59.11(B̄)
58.18(B)
CR-1 RECOGNITION FIG. 71a
1
2
4
8
A
B
71a.11(B̄A)

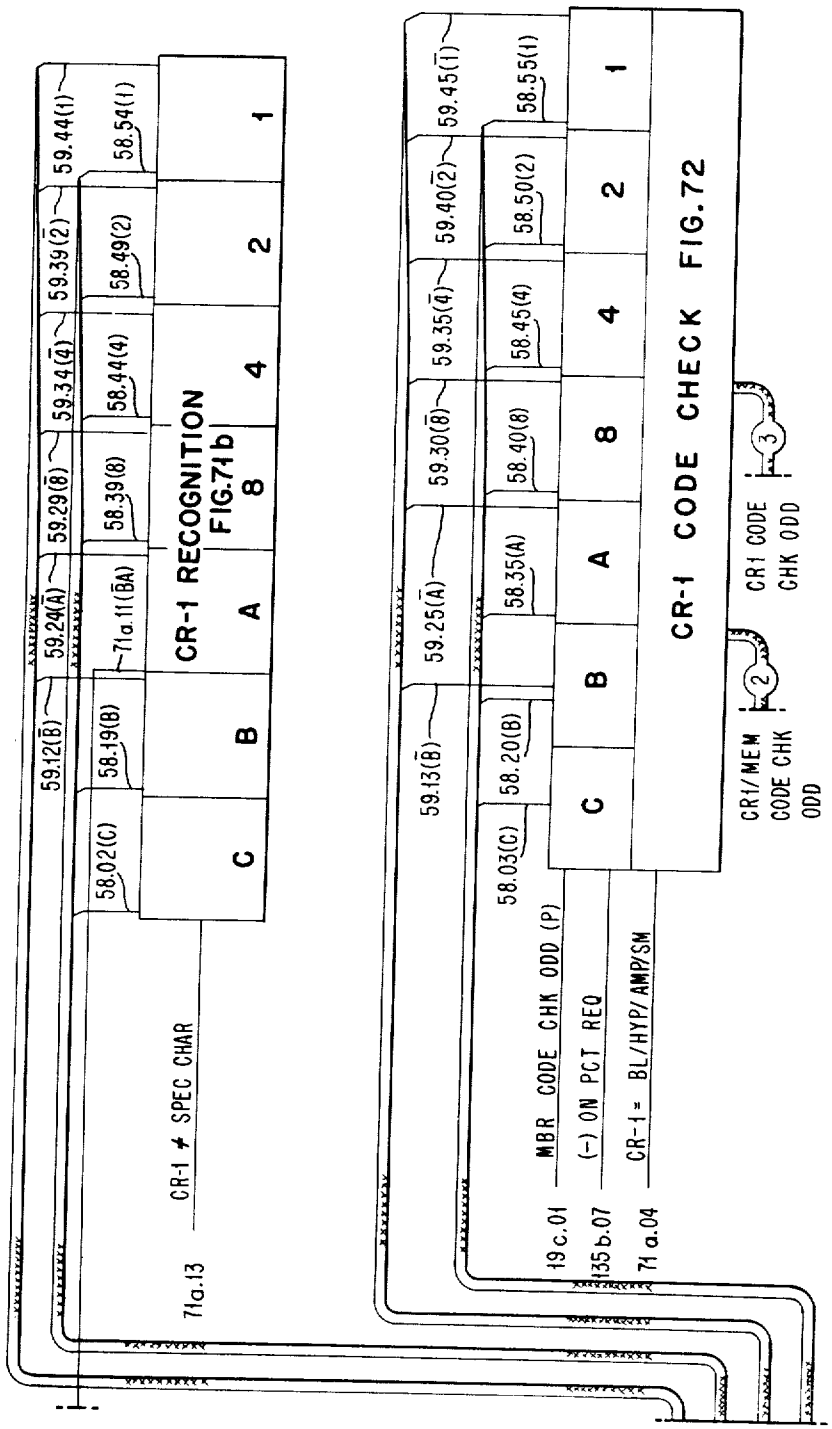

CR-1 RECOGNITION FIG.71b
C
B
A
8
4
2
1
59.12(B̄)
59.24(Ā)
59.29(8̄)
59.34(4̄)
59.39(2̄)
59.44(1)
58.02(C)
58.19(B)
71a.11(BA)
58.39(8)
58.44(4)
58.49(2)
58.54(1)
CR-1 ≠ SPEC CHAR
71a.13
CR-1 CODE CHECK FIG.72
59.13(B̄)
59.25(Ā)
59.30(8̄)
59.35(4̄)
59.40(2̄)
59.45(1̄)
58.03(C)
58.20(B)
58.35(A)
58.40(8)
58.45(4)
58.50(2)
58.55(1)
MBR CODE CHK ODD (P)
19c.01
(-) ON PCT REQ
135b.07
CR-1 = BL/HYP/AMP/SM
71a.04
CR1/MEM CODE CHK ODD
CR1 CODE CHK ODD
2
3

FIG. 20

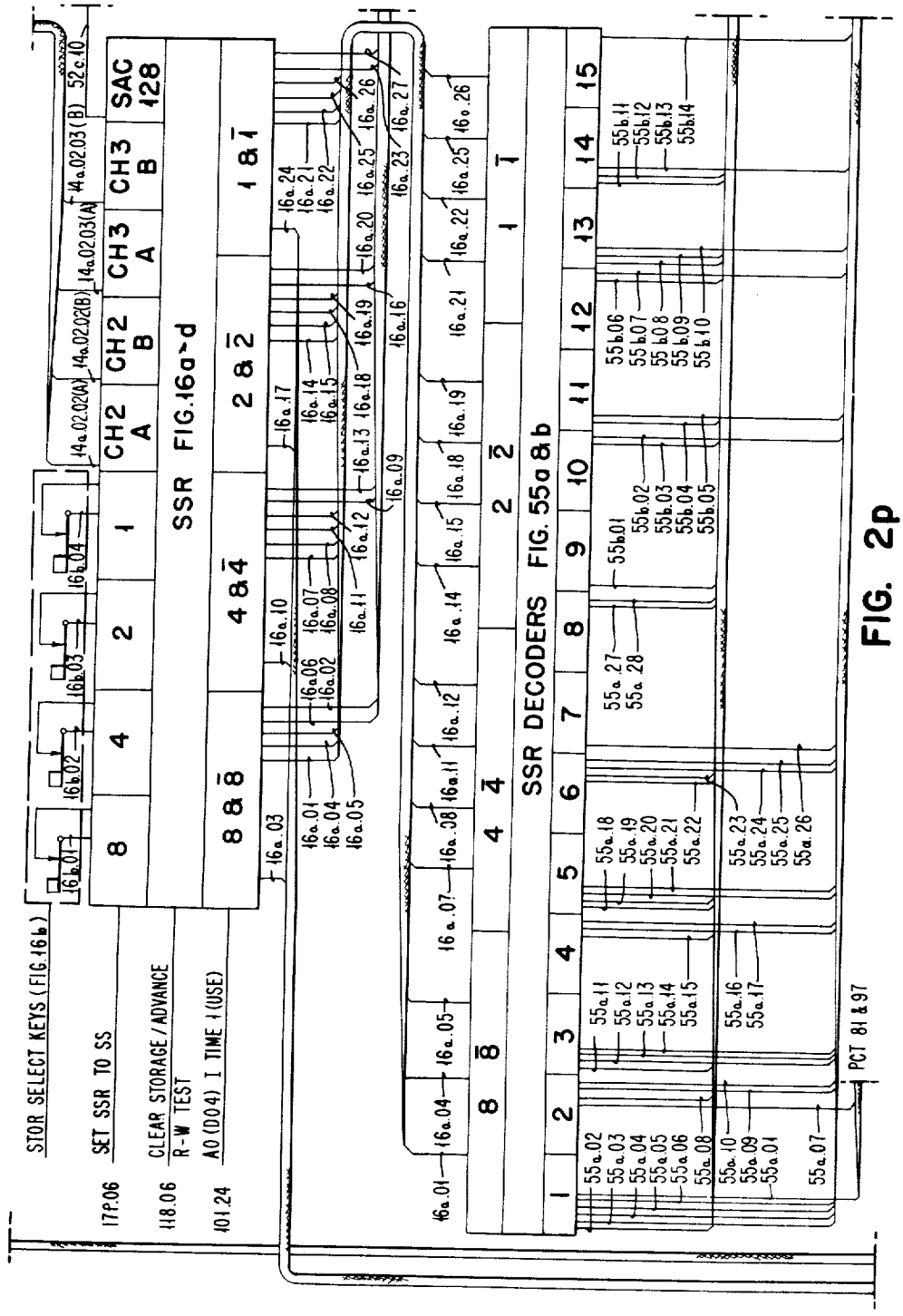
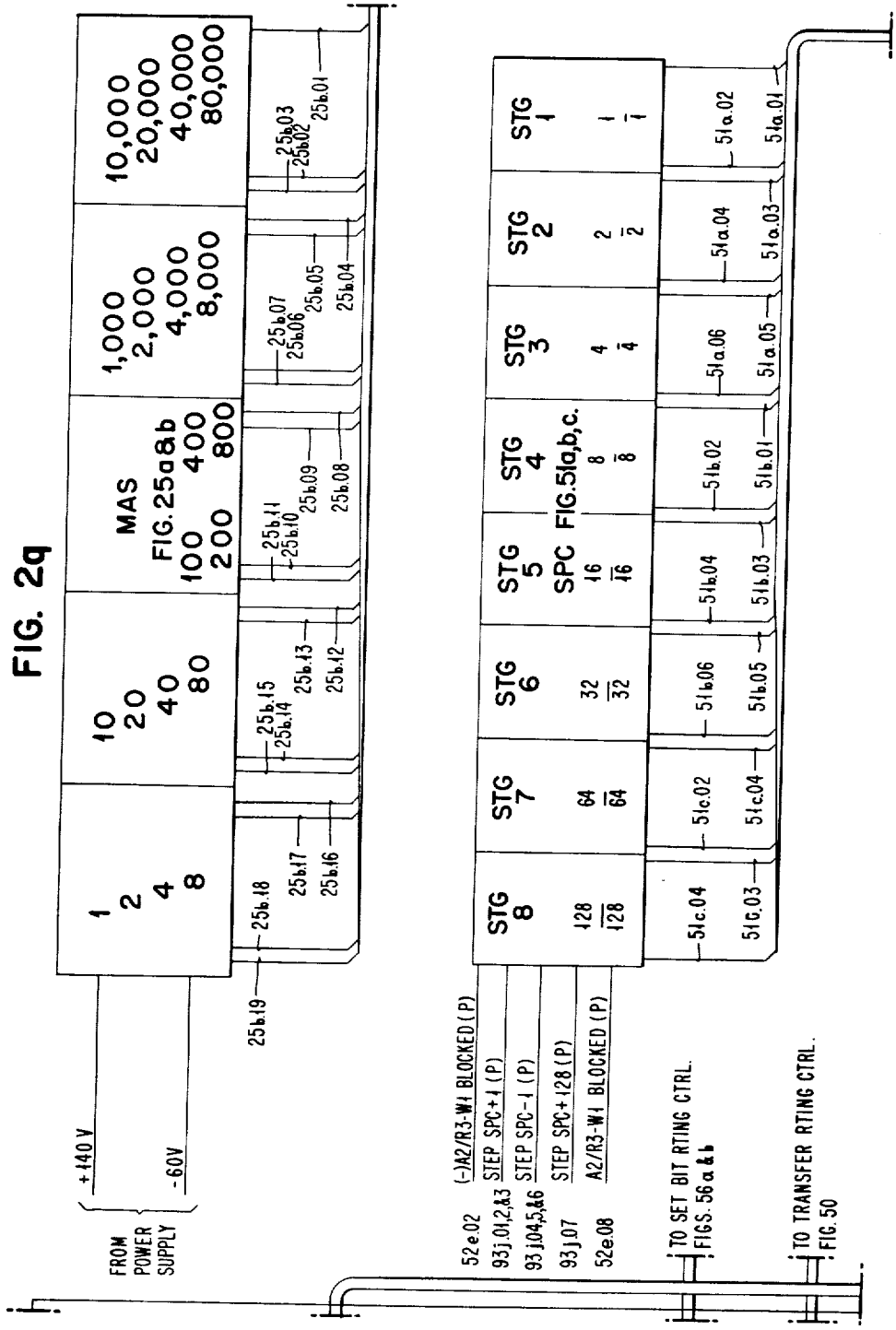

STOR SELECT KEYS (FIG.16b)
SET SSR TO SS
CLEAR STORAGE / ADVANCE R-W TEST
A0 (D04) I TIME 1 (USE)
SSR FIG.16a-d
SSR DECODERS FIG. 55a & b
CH2 A
CH2 B
CH3 A
CH3 B
SAC 128
PCT 81 & 97

FIG. 2p

FIG. 2q


1 2 4 8
10 20 40 80
MAS FIG. 25a&b 100 200 400 800
1,000 2,000 4,000 8,000
10,000 20,000 40,000 80,000
+140 V
-60V
FROM POWER SUPPLY
STG 8
STG 7
STG 6
STG 5 SPC
STG 4
STG 3
STG 2
STG 1
FIG. 51a,b,c.
(-)A2/R3-W1 BLOCKED (P)
STEP SPC+1 (P)
STEP SPC-1 (P)
STEP SPC+128 (P)
A2/R3-W1 BLOCKED (P)
52e.02
93j.01,2,A3
93j.04,5,A6
93j.07
52e.08
TO SET BIT RTING CTRL. FIGS. 56a & b
TO TRANSFER RTING CTRL. FIG. 50

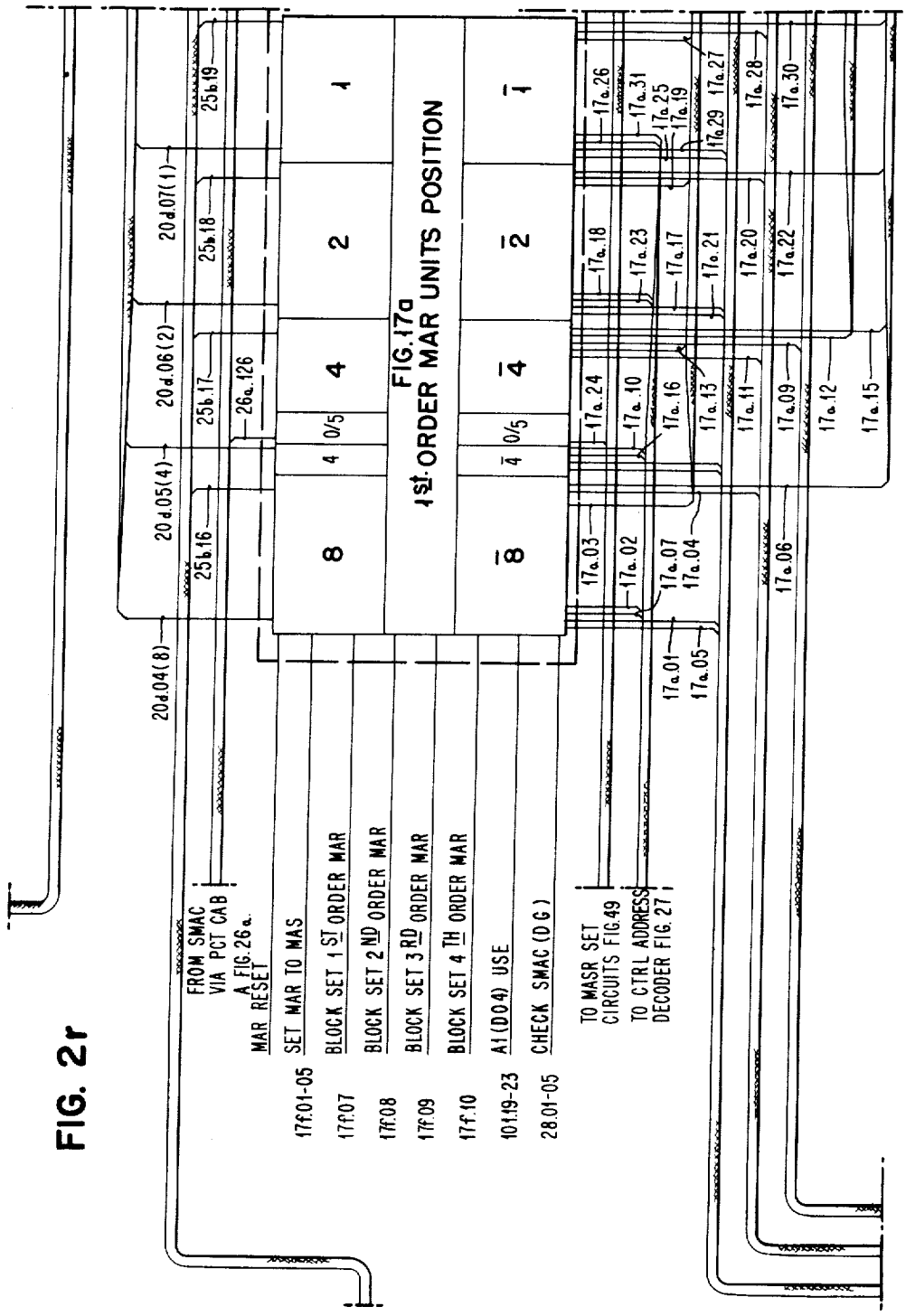
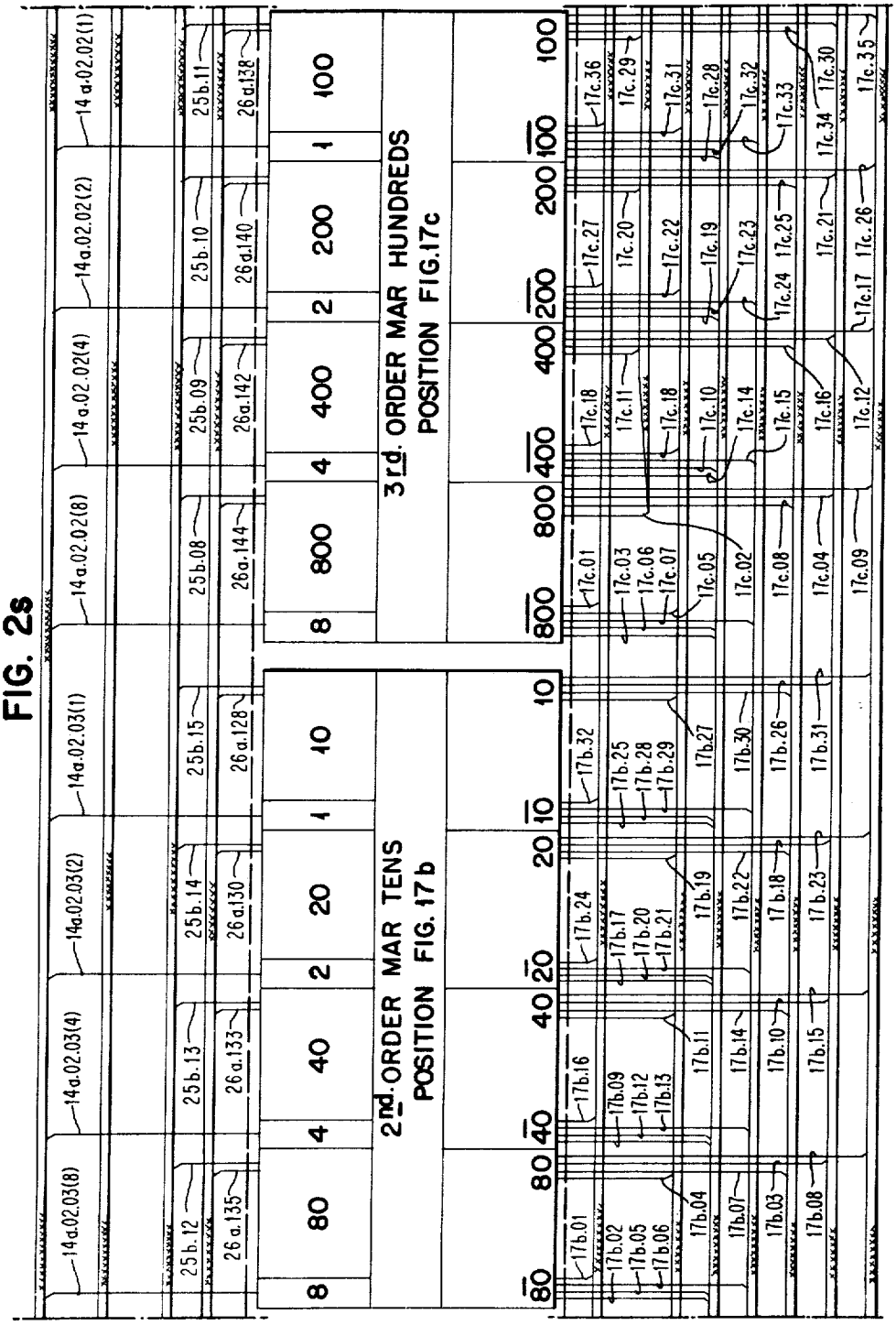

FIG. 17a
1st. ORDER MAR UNITS POSITION
8 4 2 1
0/5
8 4 2 1
FROM SMAC VIA PCT CAB A FIG. 26a.
MAR RESET
SET MAR TO MAS
BLOCK SET 1ST ORDER MAR
BLOCK SET 2ND ORDER MAR
BLOCK SET 3RD ORDER MAR
BLOCK SET 4TH ORDER MAR
A1(D04) USE
CHECK SMAC (D G)
TO MASR SET CIRCUITS FIG. 49
TO CTRL ADDRESS DECODER FIG. 27
17f.01-05
17f.07
17f.08
17f.09
17f.10
10.19-23
28.01-05
20d.04(8)
20d.05(4)
20d.06(2)
20d.07(1)
25b.16
25b.17
25b.18
25b.19
26a.126
17a.01
17a.02
17a.03
17a.04
17a.05
17a.06
17a.07
17a.09
17a.10
17a.11
17a.12
17a.13
17a.15
17a.16
17a.17
17a.18
17a.19
17a.20
17a.21
17a.22
17a.23
17a.24
17a.25
17a.26
17a.27
17a.28
17a.29
17a.30
17a.31

FIG. 2r

FIG. 2s

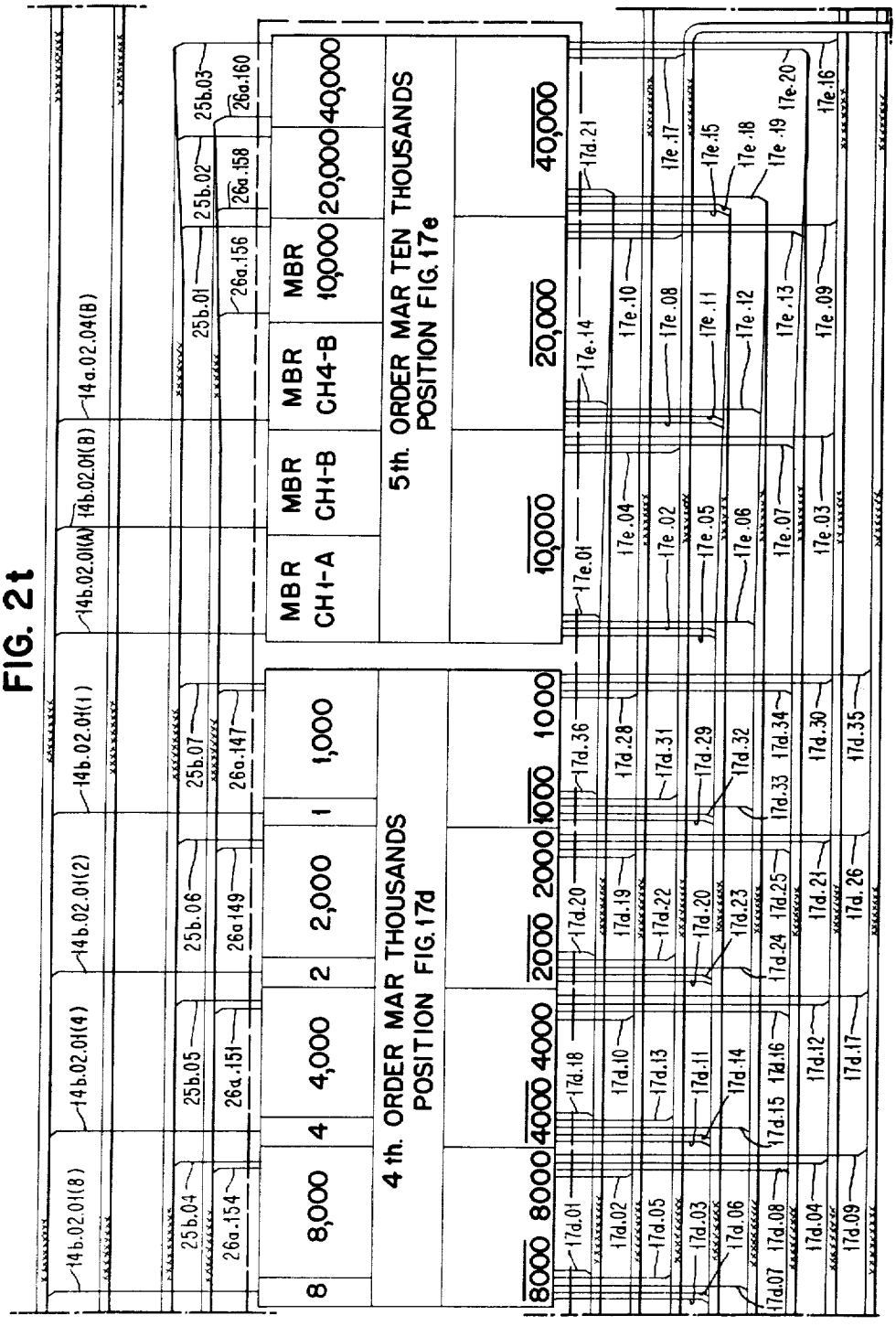

14a.02.03(8)
14a.02.03(4)
14a.02.03(2)
14a.02.03(1)
14a.02.02(8)
14a.02.02(4)
14a.02.02(2)
14a.02.02(1)
25b.12
25b.13
25b.14
25b.15
25b.08
25b.09
25b.10
25b.11
26a.135
26a.133
26a.130
26a.128
26a.144
26a.142
26a.140
26a.138
8 80 4 40 2 20 1 10
2nd. ORDER MAR TENS
POSITION FIG. 17b
8 800 4 400 2 200 1 100
3rd. ORDER MAR HUNDREDS
POSITION FIG.17c
80 40 20 10
800 400 200 100
17b.01 17b.02 17b.05 17b.06 17b.04 17b.07 17b.03 17b.08
17b.16 17b.09 17b.12 17b.13 17b.11 17b.14 17b.10 17b.15
17b.24 17b.17 17b.20 17b.21 17b.19 17b.22 17b.18 17b.23
17b.32 17b.25 17b.28 17b.29 17b.27 17b.30 17b.26 17b.31
17c.01 17c.03 17c.06 17c.07 17c.05 17c.02 17c.08 17c.04
17c.18 17c.11 17c.18 17c.10 17c.14 17c.15 17c.16 17c.09
17c.27 17c.20 17c.22 17c.19 17c.23 17c.24 17c.25 17c.21
17c.36 17c.29 17c.31 17c.28 17c.32 17c.33 17c.34 17c.26
17c.12 17c.17 17c.30 17c.35

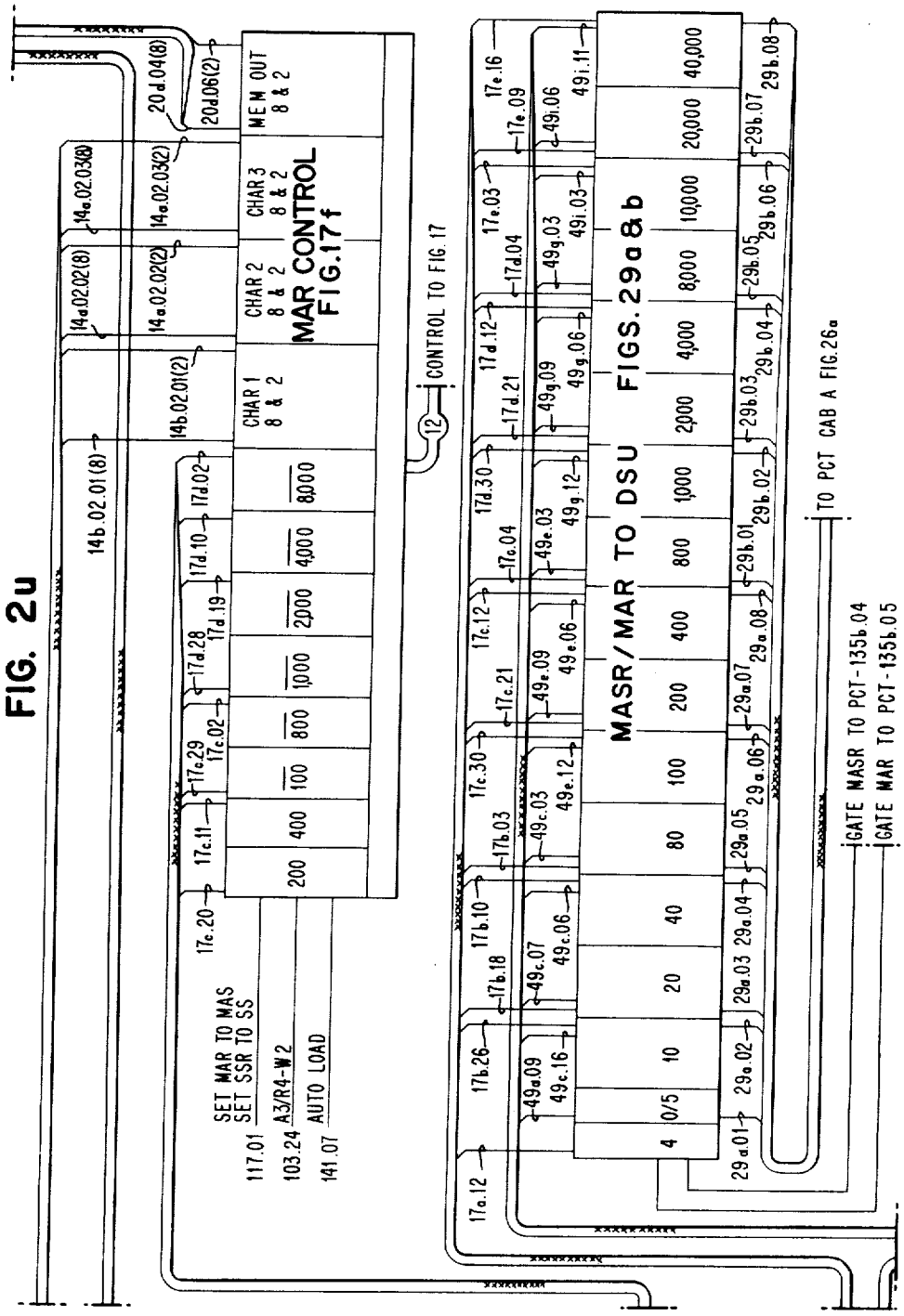
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TRANSFER INSTRUCTION

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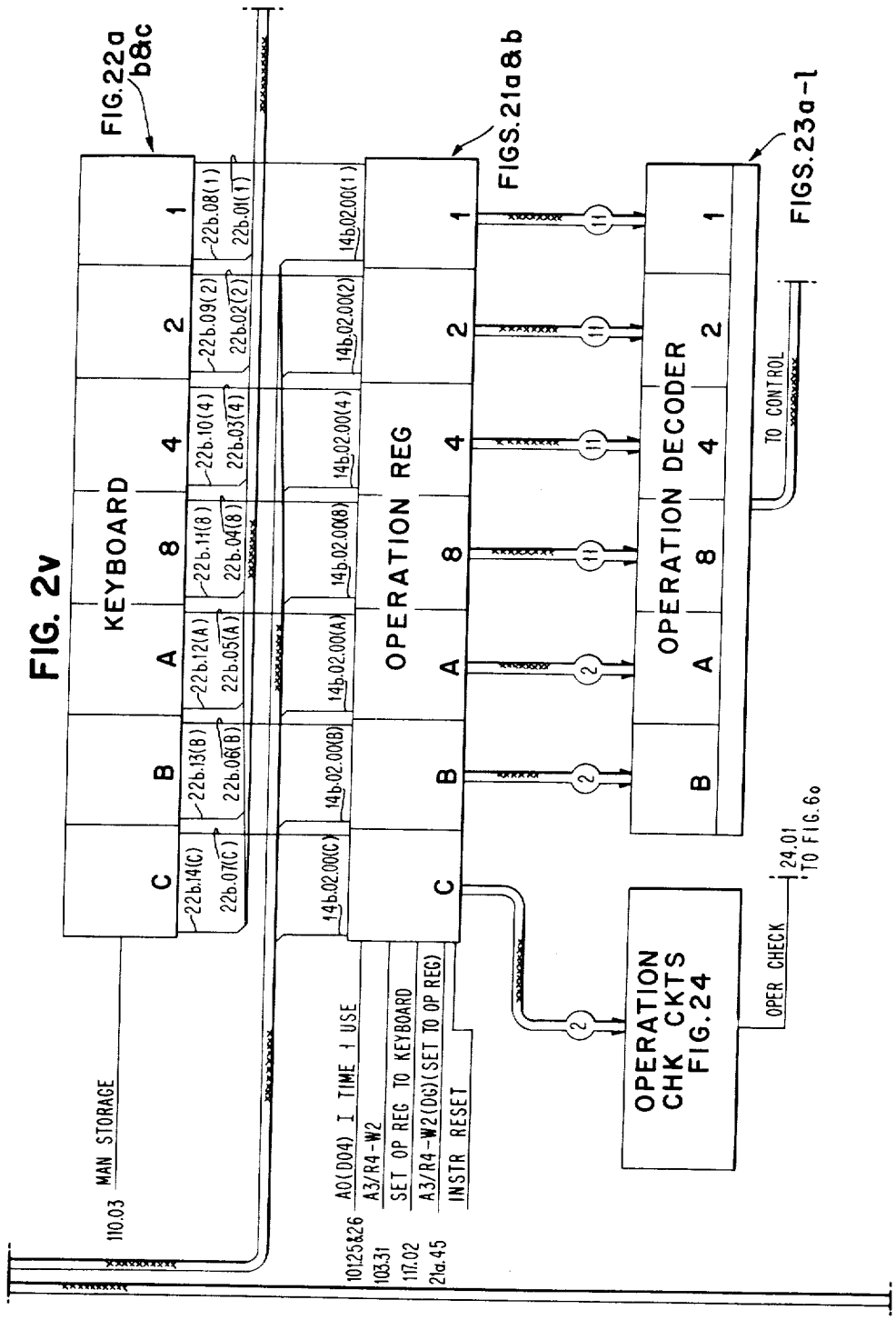
FIG. 21




FIG. 2u
MAR CONTROL FIG.17f
MASR/MAR TO DSU FIGS. 29a & b
CONTROL TO FIG. 17
TO PCT CAB A FIG.26a
GATE MASR TO PCT-135b.04
GATE MAR TO PCT-135b.05
SET MAR TO MAS
SET SSR TO SS
A3/R4-W2
AUTO LOAD
MEM OUT 8 & 2
CHAR 3 8 & 2
CHAR 2 8 & 2
CHAR 1 8 & 2

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FIG. 2v



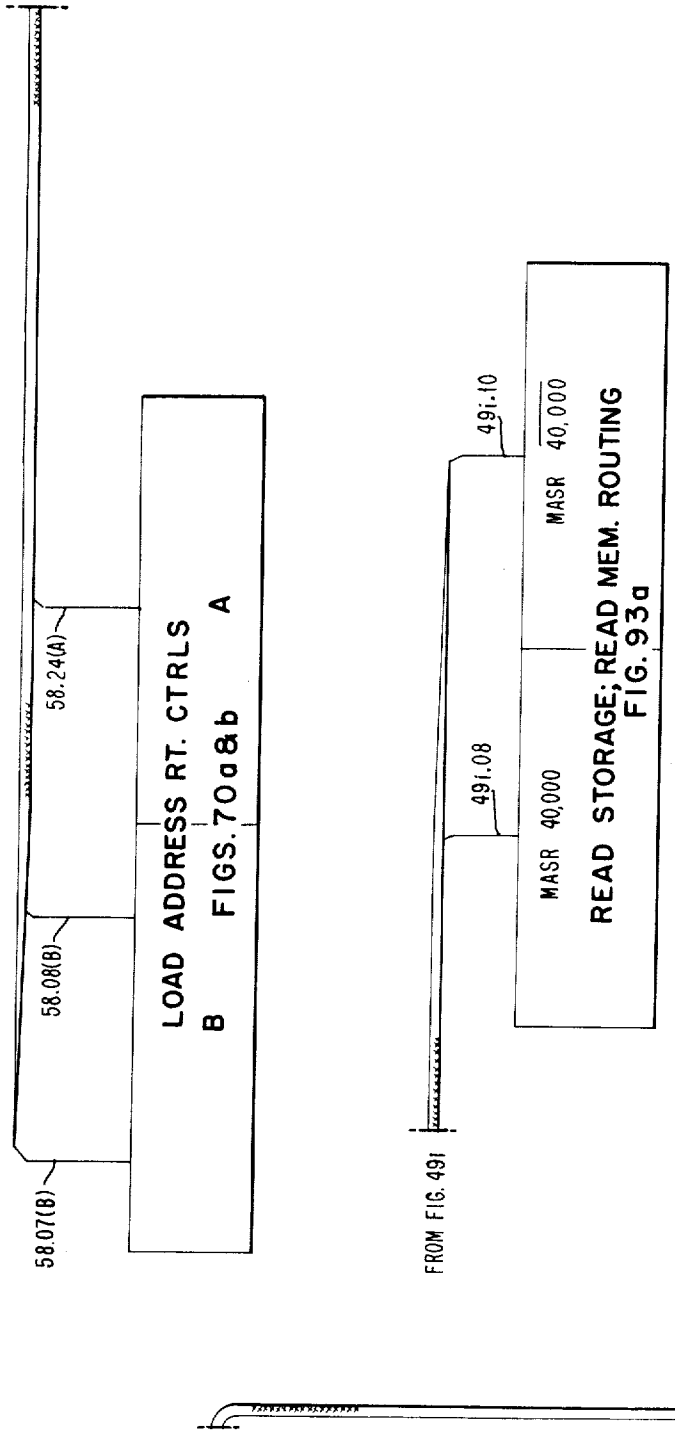

LOAD ADDRESS RT. CTRLS
B FIGS. 70a&b A
58.24(A)
58.08(B)
58.07(B)
FROM FIG. 49I
49I.08
MASR 40,000
READ STORAGE; READ MEM. ROUTING
FIG. 93a
49I.10
MASR 40,000

FIG. 2w

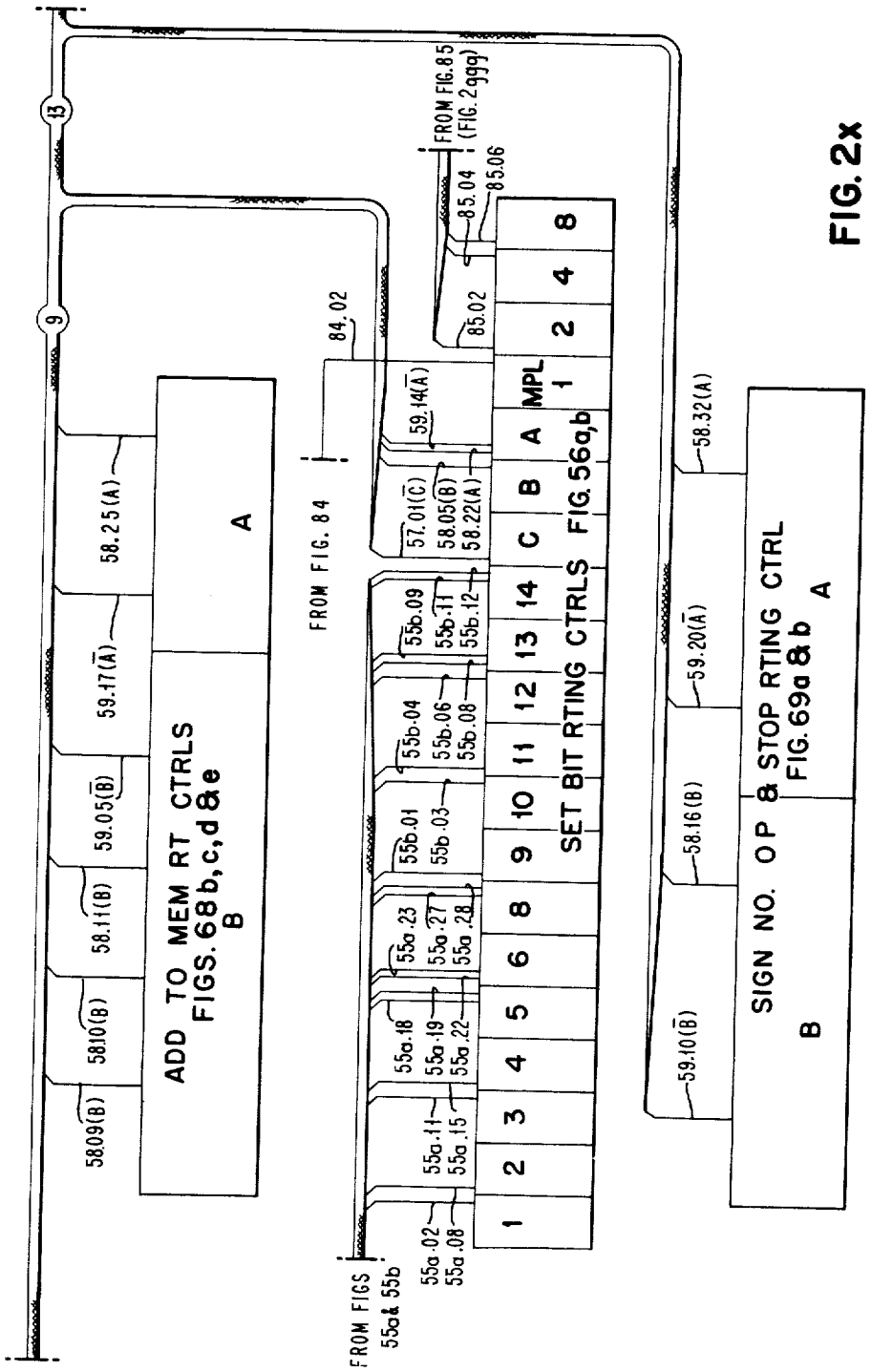

FROM FIGS 55a & 55b
55a.02
55a.08
55a.11
55a.15
55a.18
55a.19
55a.22
55a.23
55a.27
55a.28
55b.01
55b.03
55b.04
55b.06
55b.08
55b.09
55b.11
55b.12
FROM FIG. 84
84.02
57.01(C)
58.05(B)
58.22(A)
59.14(A)
FROM FIG. 85 (FIG. 2ggg)
85.04
85.06
85.02
1 2 3 4 5 6 8 9 10 11 12 13 14 C B A MPL 1 2 4 8
SET BIT RTING CTRLS FIG. 56a,b
ADD TO MEM RT CTRLS FIGS. 68b,c,d & e
A
B
58.09(B)
58.10(B)
58.11(B)
59.05(B)
59.17(A)
58.25(A)
SIGN NO. OP & STOP RTING CTRL FIG. 69a & b
A
B
58.32(A)
59.20(A)
58.16(B)
59.10(B)
9
13

FIG. 2x

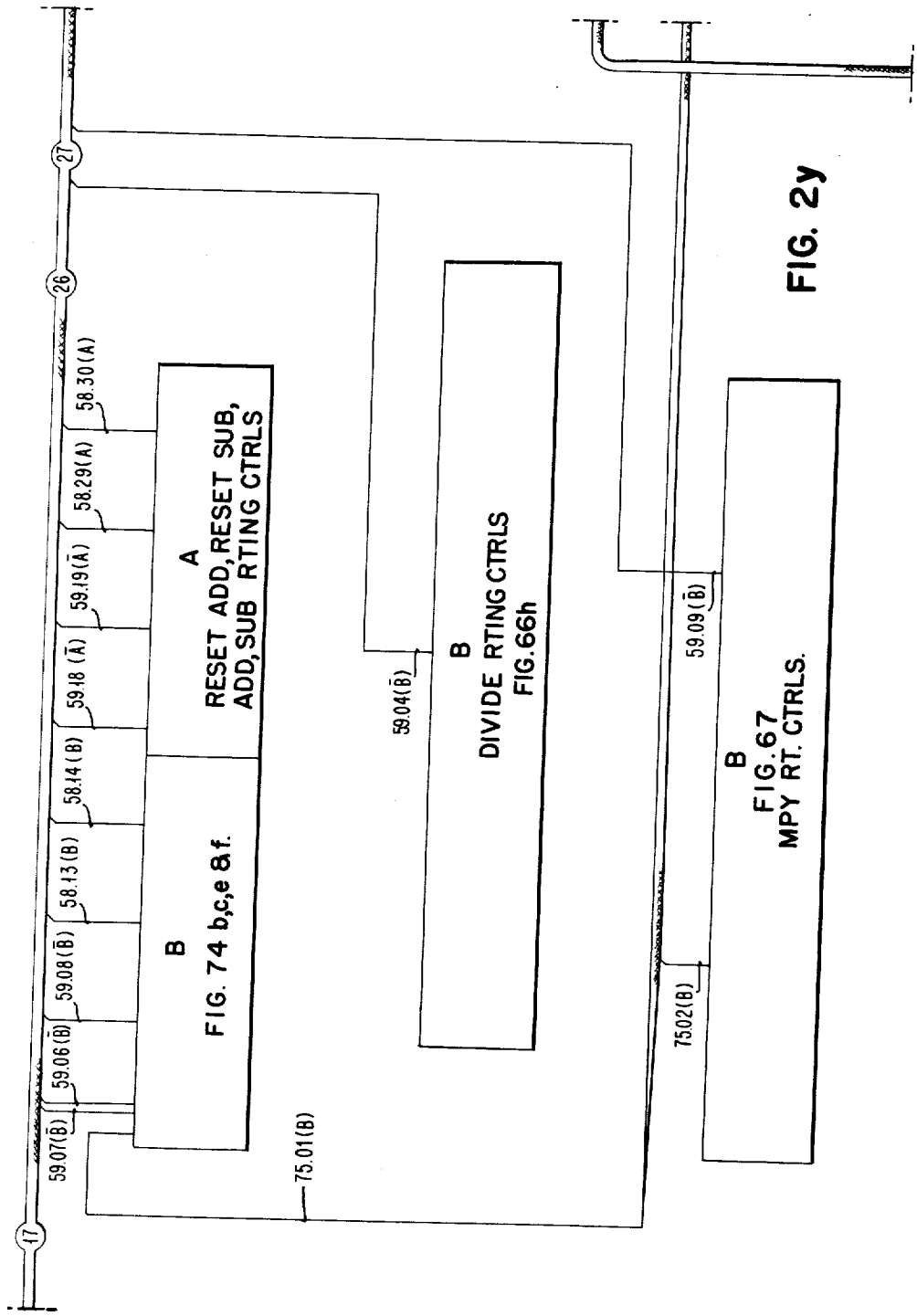

27
26
17
58.30(A)
58.29(A)
59.19(Ā)
59.18(Ā)
58.14(B)
58.13(B)
59.08(B̄)
59.06(B̄)
59.07(B̄)
A
RESET ADD, RESET SUB, ADD, SUB RTING CTRLS
B
FIG. 74 b,c,e & f.
75.01(B)
59.04(B̄)
B
DIVIDE RTING CTRLS
FIG. 66h
59.09(B̄)
75.02(B)
B
FIG. 67
MPY RT. CTRLS.

FIG. 2y

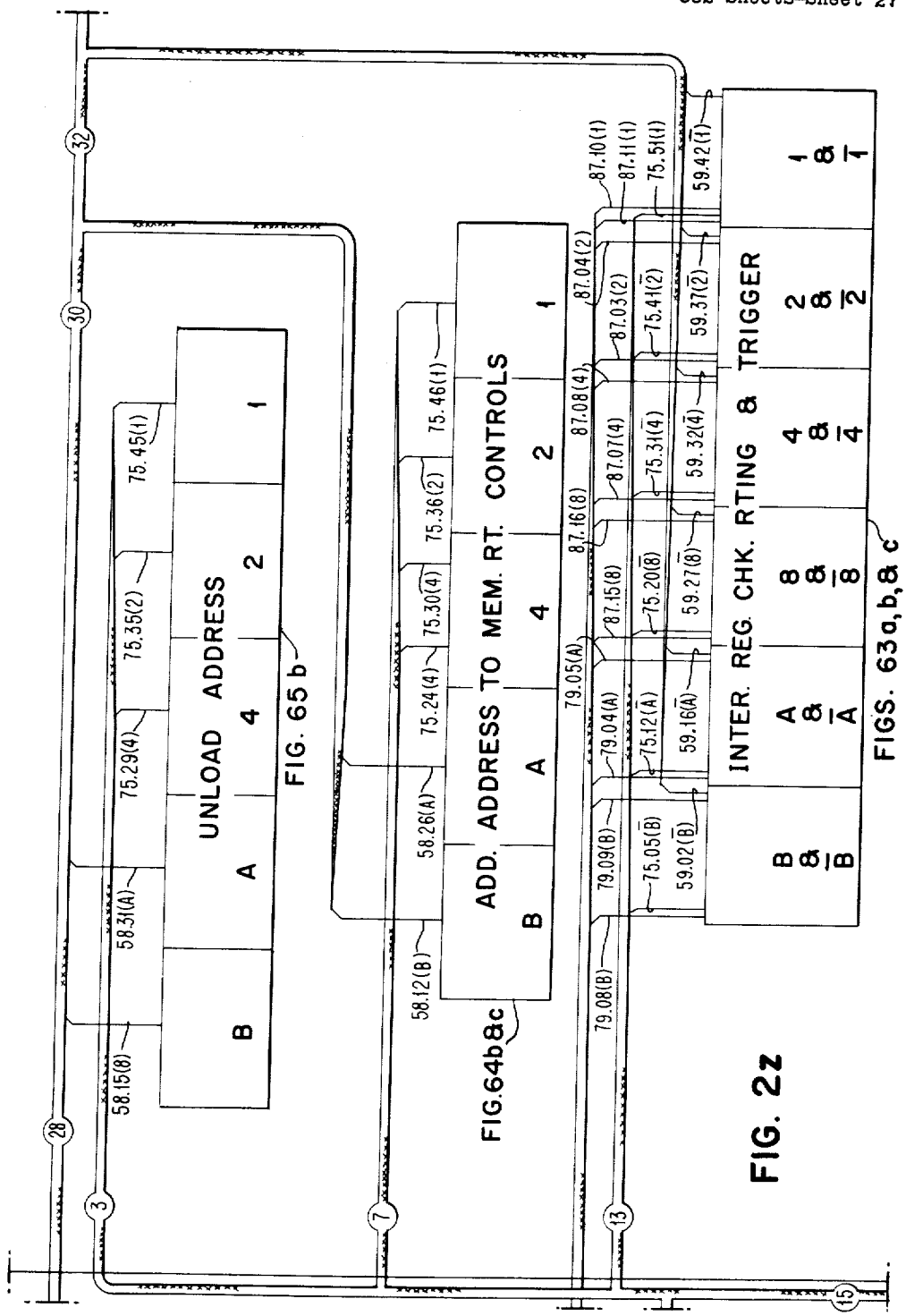

UNLOAD ADDRESS
B A 4 2 1
ADD. ADDRESS TO MEM. RT. CONTROLS
B A 4 2 1
INTER. REG. CHK. RTING & TRIGGER
B Ā B̄ A Ā 8 8̄ 4 4̄ 2 2̄ 1 1̄
FIG. 65 b
FIG. 64b8c
FIGS. 63a,b,8 c
58.15(8)
58.31(A)
75.29(4)
75.35(2)
75.45(1)
58.12(B)
58.26(A)
75.24(4)
75.30(4)
75.36(2)
75.46(1)
79.08(B)
79.09(B)
79.04(A)
79.05(A)
87.16(8)
87.08(4)
87.04(2)
87.10(1)
75.05(B̄)
59.02(B̄)
75.12(Ā)
59.16(Ā)
75.20(8̄)
59.27(8̄)
75.31(4̄)
59.32(4̄)
75.41(2̄)
59.37(2̄)
75.51(1̄)
59.42(1̄)
87.15(8)
87.07(4)
87.03(2)
87.11(1)
28
3
7
13
15
30
32

FIG. 2z

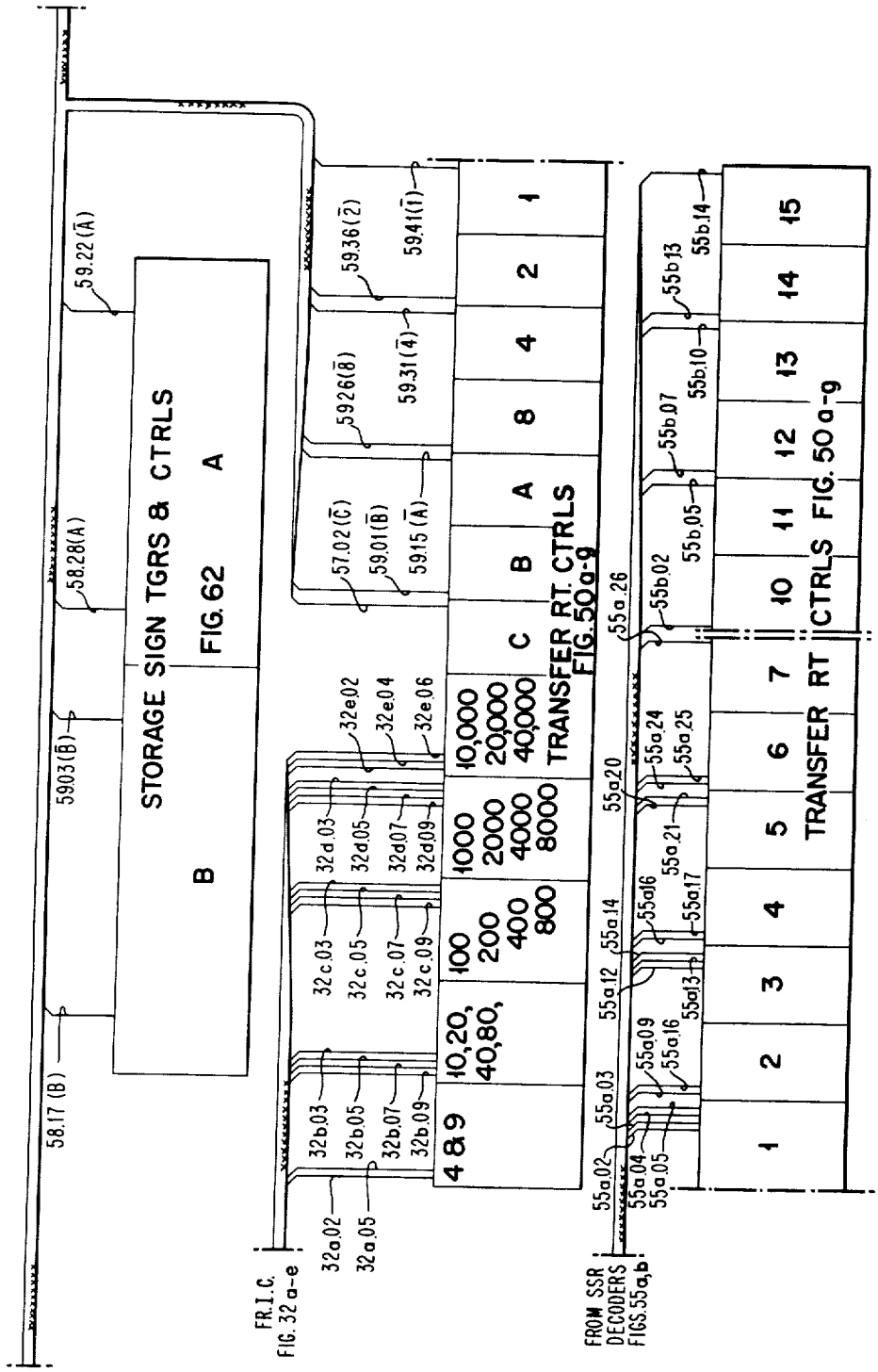

STORAGE SIGN TGRS & CTRLS
B
FIG. 62
A
58.17 (B)
58.28(A)
59.22(Ā)
5903(B̄)
59.41(1̄)
59.36(2̄)
59.31(4̄)
59.26(8̄)
59.15(Ā)
59.01(B̄)
57.02(C̄)
TRANSFER RT. CTRLS FIG. 50a-9
C B A 8 4 2 1
10,000 20,000 40,000
1000 2000 4000 8000
100 200 400 800
10,20, 40,80,
4 8 9
32e.02 32e.04 32e.06
32d.03 32d.05 32d.07 32d.09
32c.03 32c.05 32c.07 32c.09
32b.03 32b.05 32b.07 32b.09
32a.02 32a.05
FR.I.C. FIG. 32 a-e
55a.26 55a.20 55a.14 55a.12 55a.03
55a.02 55a.04 55a.05
55a.09 55a.16
55a13 55a16 55a17 55a.21
55a.24 55a.25
55b.02 55b.05 55b.07 55b.10 55b.13 55b.14
TRANSFER RT CTRLS FIG. 50 a-9
15 14 13 12 11 10 7 6 5 4 3 2 1
FROM SSR DECODERS FIGS. 55a,b

FIG. 2aa

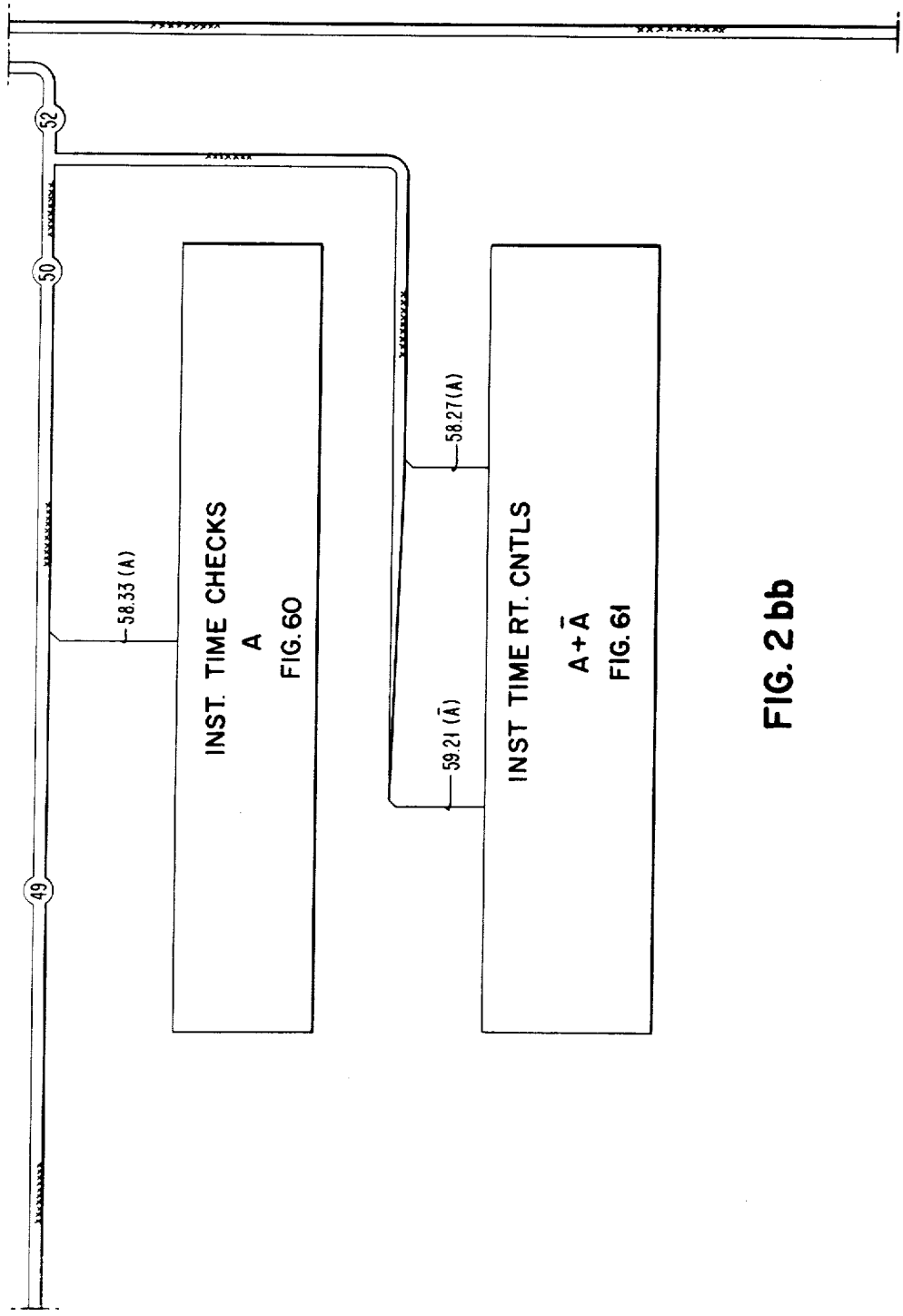

52
50
49
58.33 (A)
INST. TIME CHECKS
A
FIG. 60
58.27 (A)
59.21 (Ā)
INST TIME RT. CNTLS
A + Ā
FIG. 61

FIG. 2bb

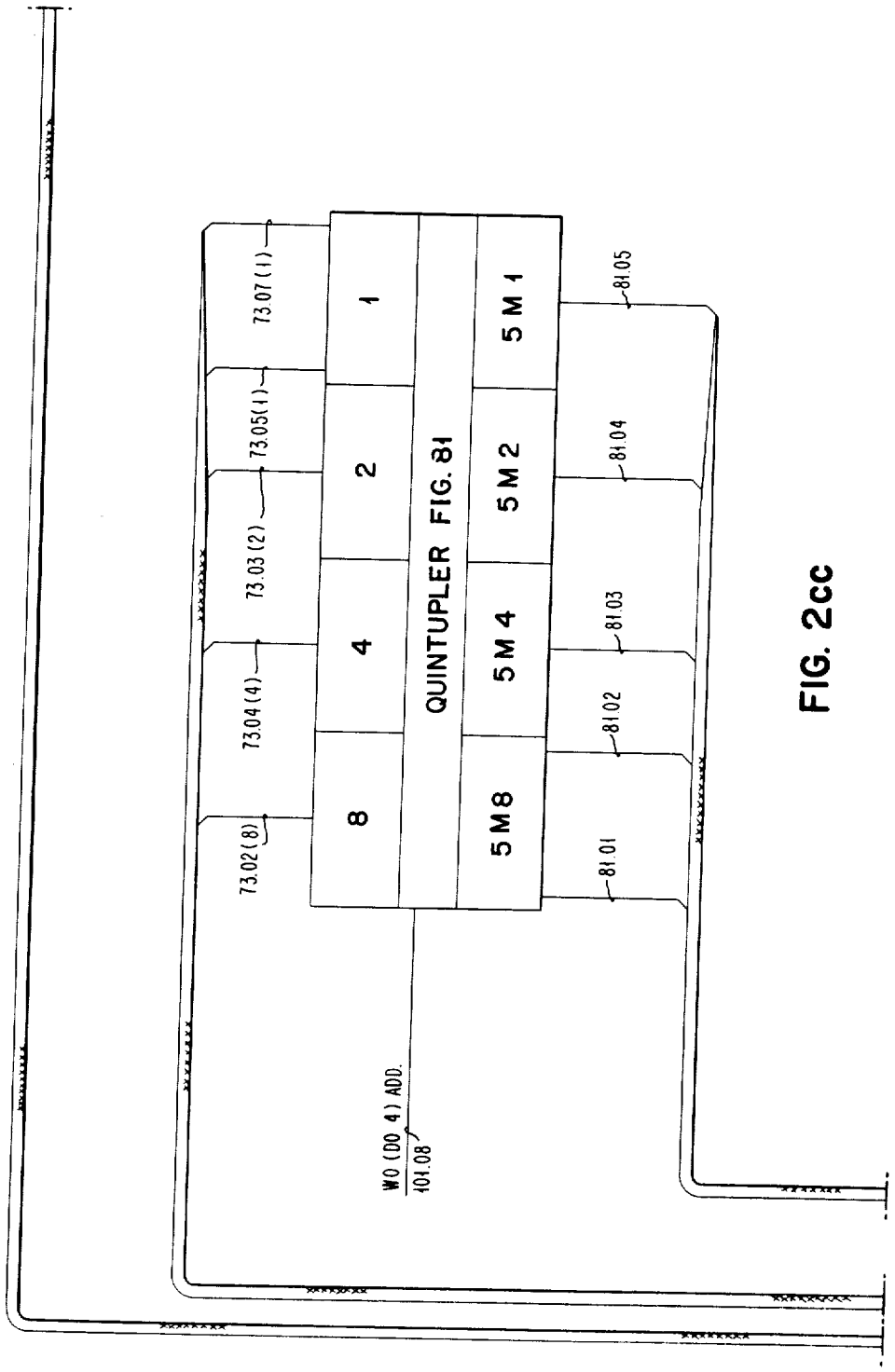

73.07(1)
73.05(1)
73.03(2)
73.04(4)
73.02(8)
1
2
4
8
QUINTUPLER FIG. 81
5M1
5M2
5M4
5M8
81.05
81.04
81.03
81.02
81.01
WO (DO 4) ADD.
101.08

FIG. 2cc

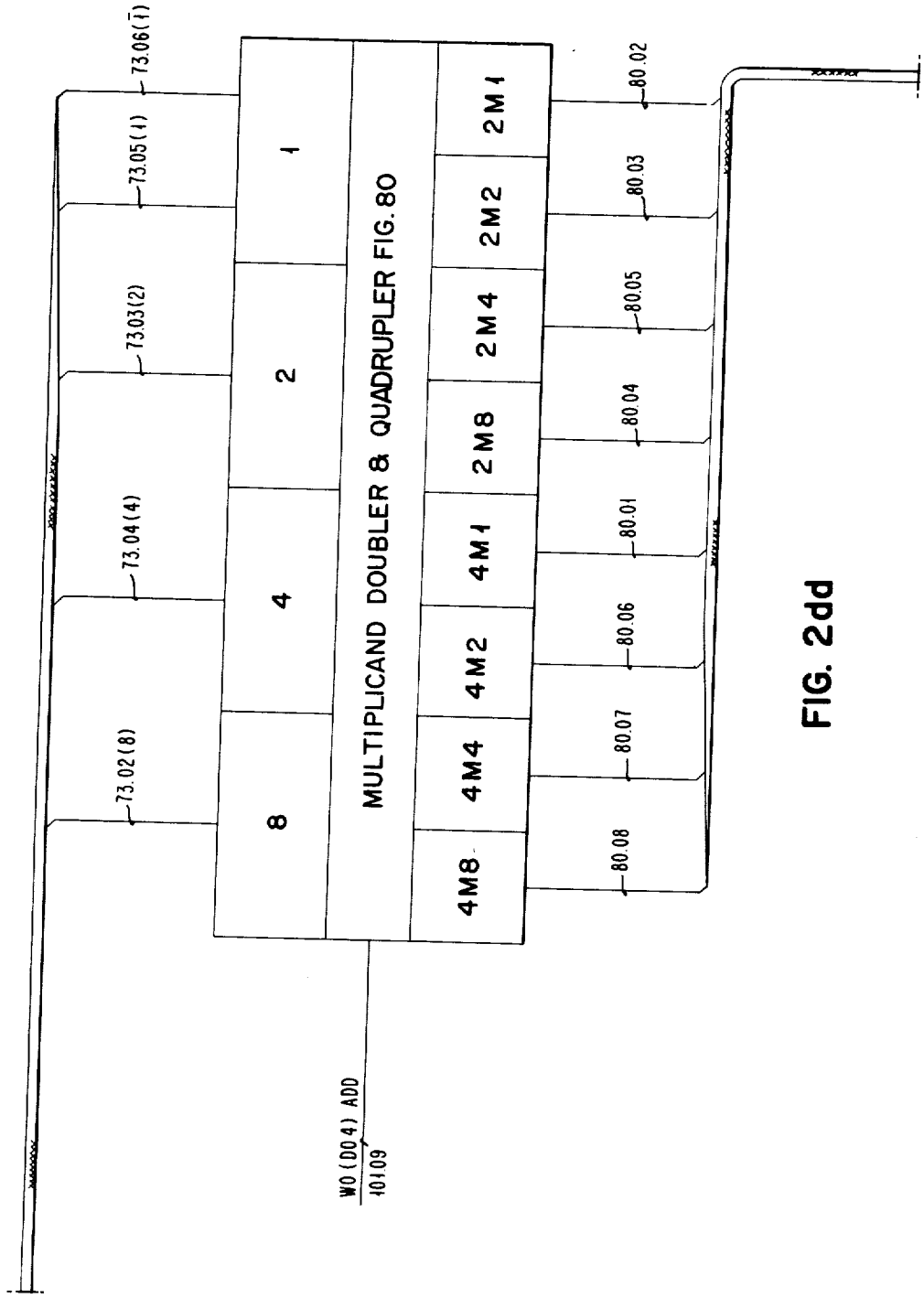
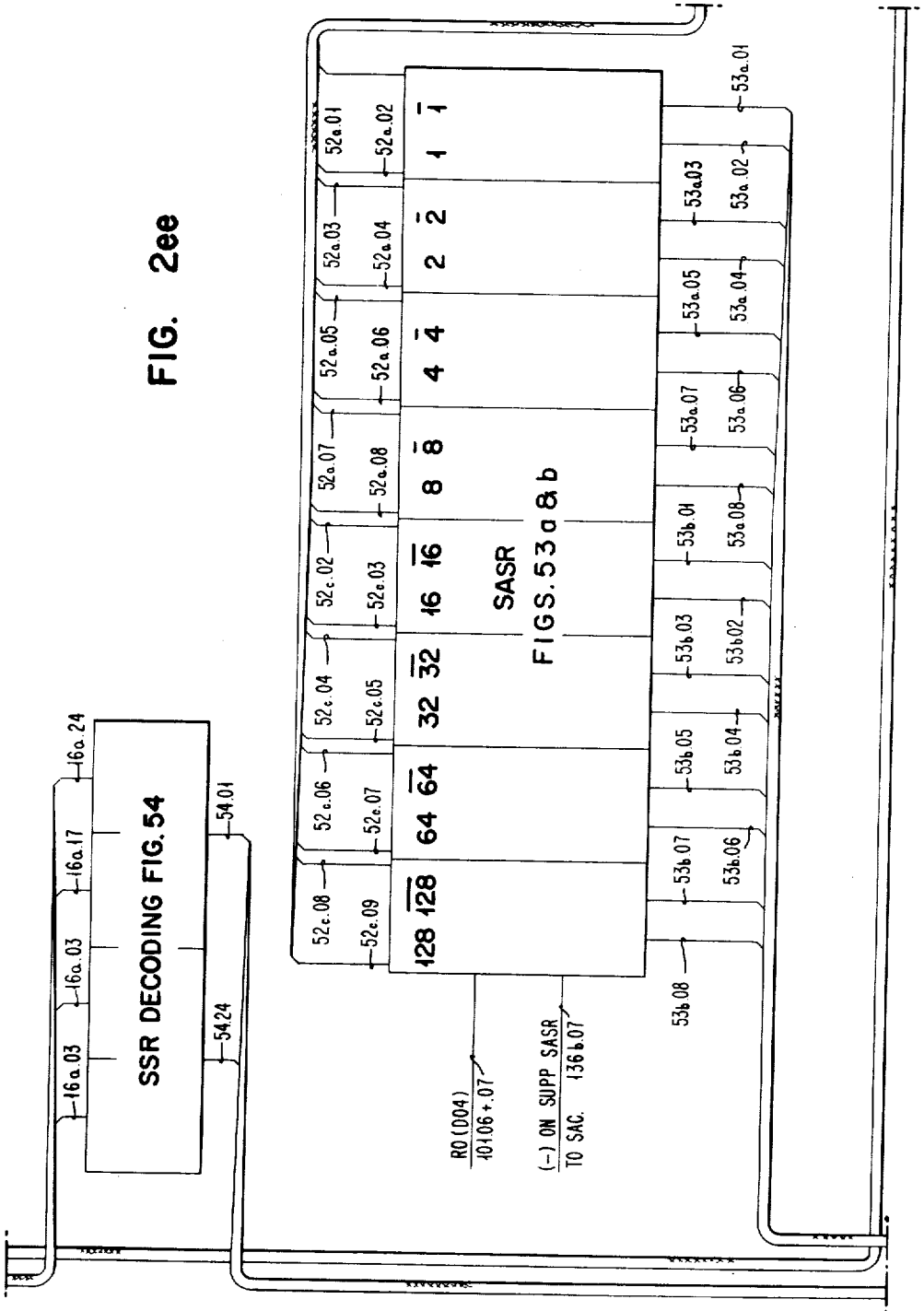

73.06(1)
73.05(1)
73.03(2)
73.04(4)
73.02(8)
1
2
4
8
MULTIPLICAND DOUBLER & QUADRUPLER FIG. 80
2M1
2M2
2M4
2M8
4M1
4M2
4M4
4M8
80.02
80.03
80.05
80.04
80.01
80.06
80.07
80.08
WO (0044) ADD
10109

FIG. 2dd

FIG. 2ee


SSR DECODING FIG. 54
16a.24
16a.17
16a.03
16a.03
54.01
54.24
SASR
FIGS. 53a & b
1 1
2 2
4 4
8 8
16 16
32 32
64 64
128 128
52a.01
52a.02
52a.03
52a.04
52a.05
52a.06
52a.07
52a.08
52c.02
52c.03
52c.04
52c.05
52a.06
52a.07
52c.08
52c.09
53a.01
53a.02
53a.03
53a.04
53a.05
53a.06
53a.07
53a.08
53b.01
53b.02
53b.03
53b.04
53b.05
53b.06
53b.07
53b.08
RO (004)
401.06 + .07
(-) ON SUPP SASR
TO SAC. 136 b.07

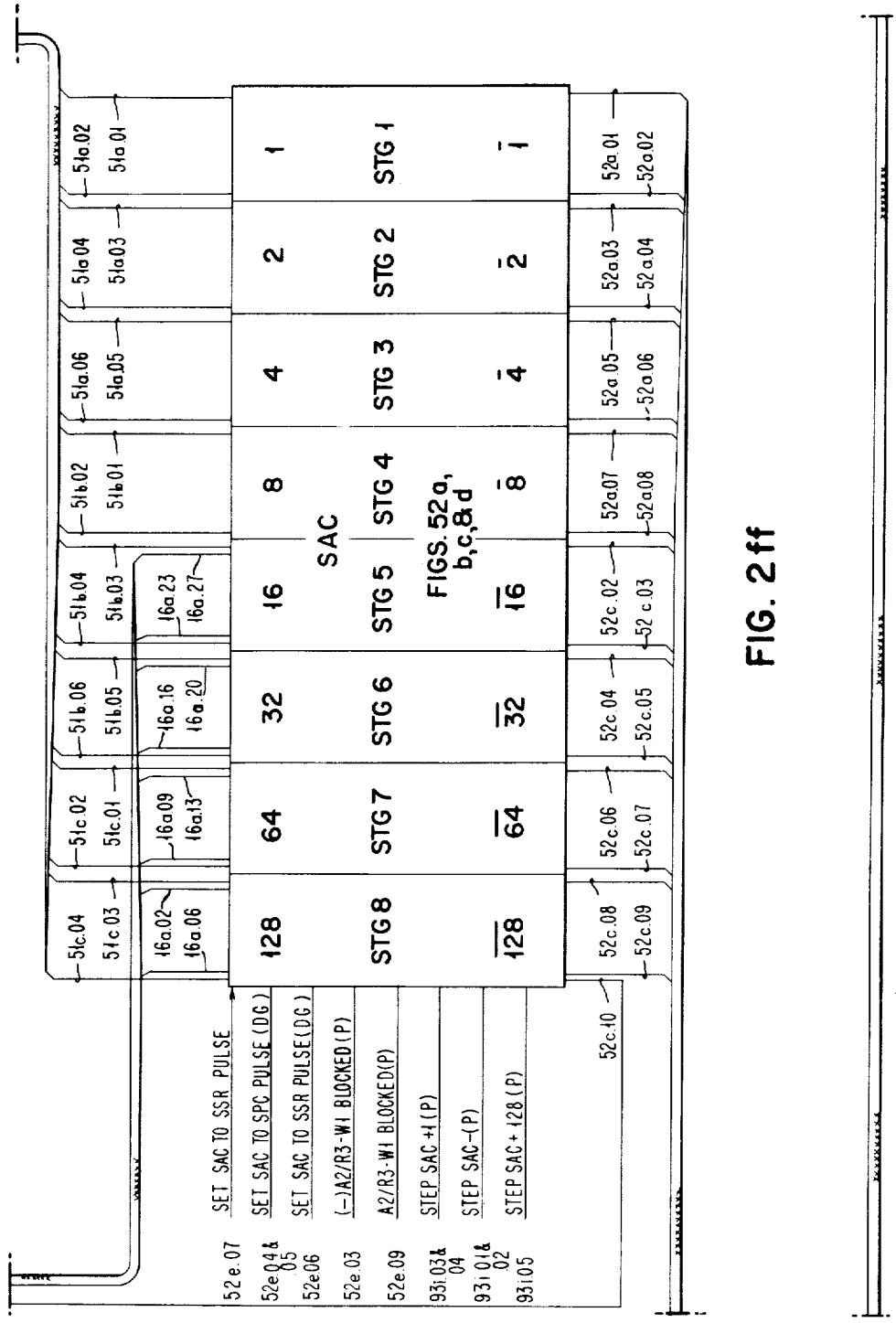

SAC
FIGS. 52a, b,c,&d
STG 1
STG 2
STG 3
STG 4
STG 5
STG 6
STG 7
STG 8
1
2
4
8
16
32
64
128
SET SAC TO SSR PULSE
SET SAC TO SPC PULSE (DG)
SET SAC TO SSR PULSE(DG)
(-)A2/R3-W1 BLOCKED(P)
A2/R3-W1 BLOCKED(P)
STEP SAC+1(P)
STEP SAC-(P)
STEP SAC+128(P)

FIG. 2ff

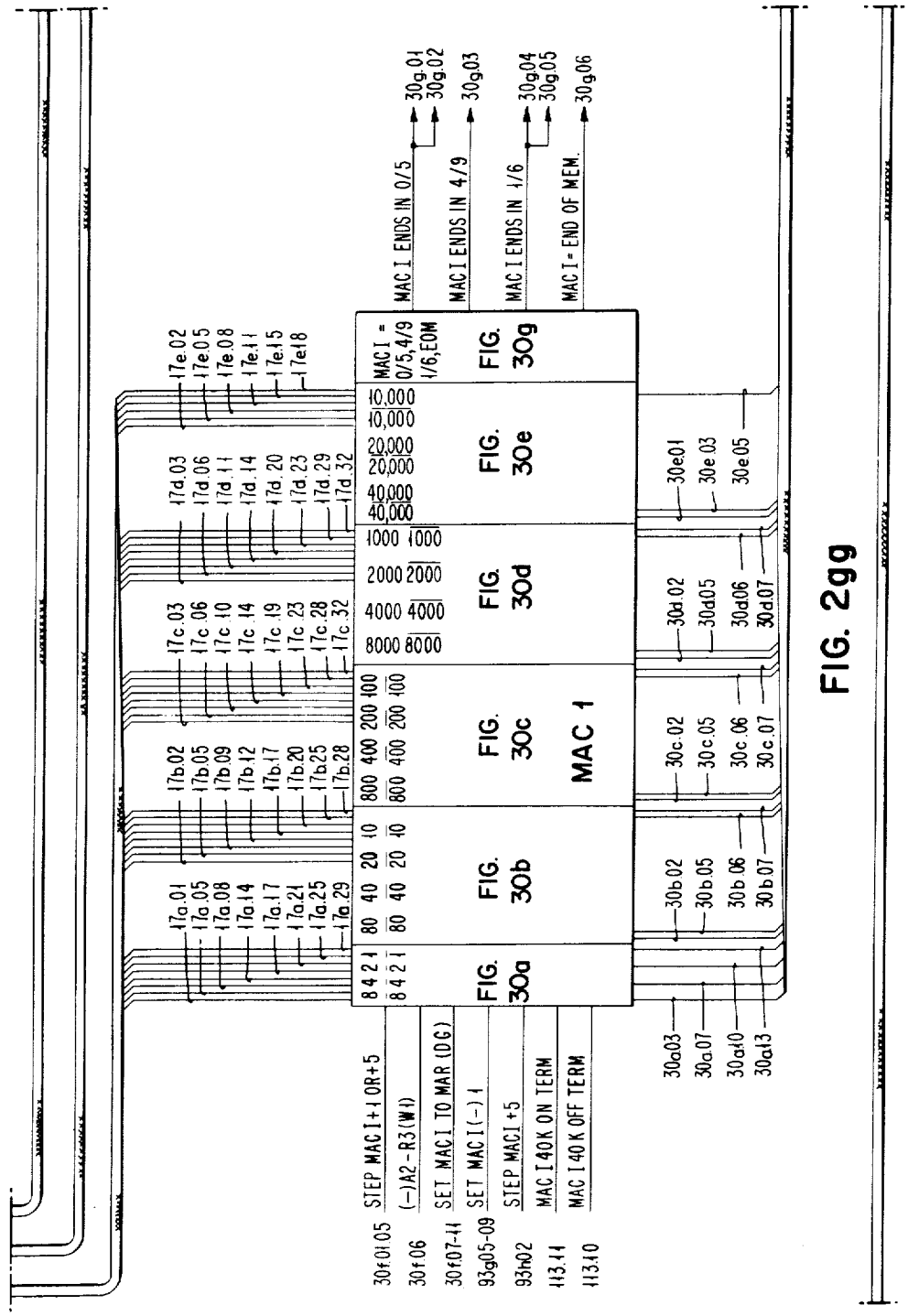
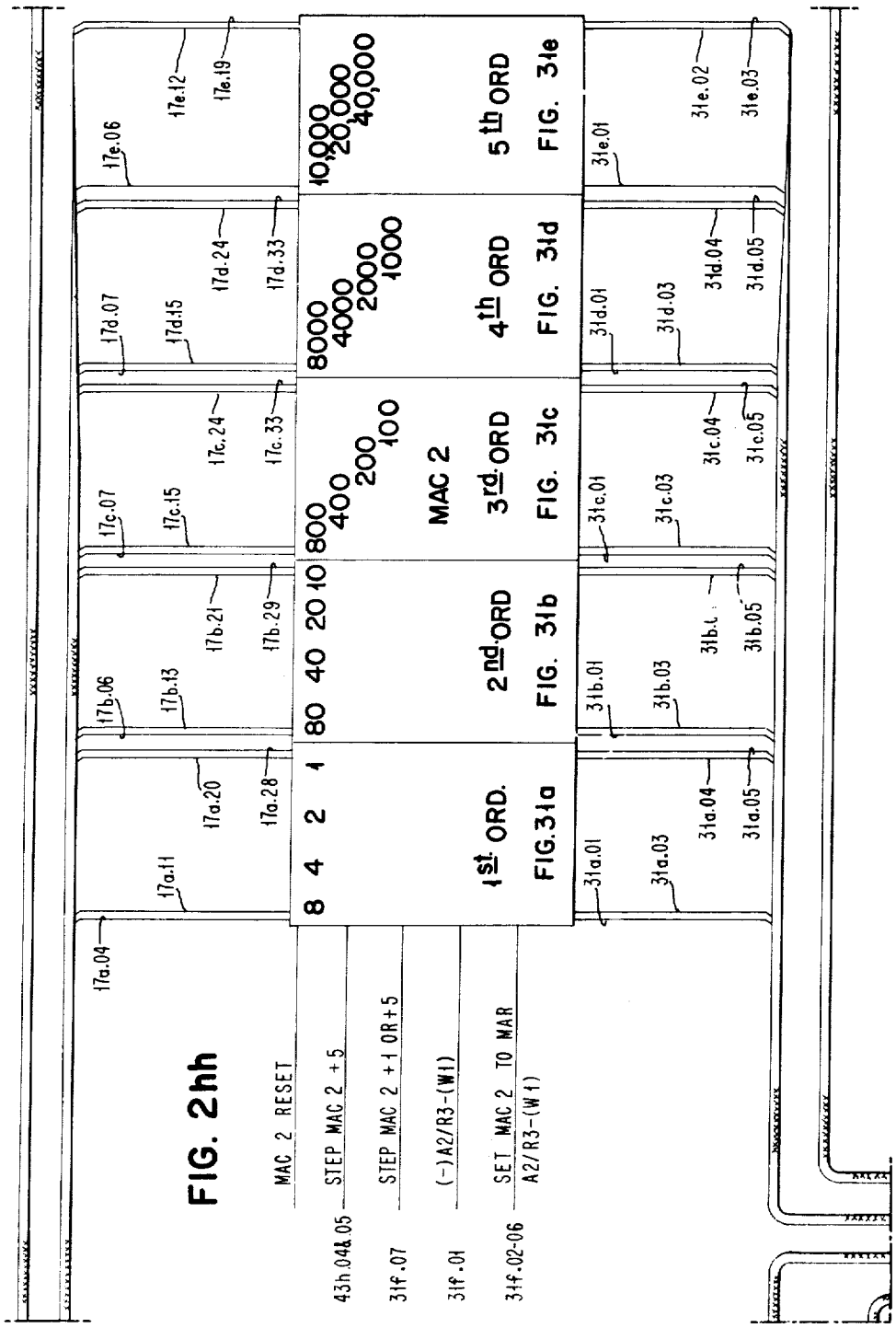

MAC I ENDS IN 0/5
MAC I ENDS IN 4/9
MAC I ENDS IN 1/6
MAC I = END OF MEM.
MAC I = 0/5,4/9 1/6,EOM
FIG. 30g
FIG. 30e
FIG. 30d
FIG. 30c
FIG. 30b
FIG. 30a
MAC 1
STEP MAC I+1 OR+5
(-)A2-R3(W1)
SET MAC I TO MAR (DC)
SET MAC I(-)1
STEP MAC I+5
MAC I 40K ON TERM
MAC I 40 K OFF TERM

FIG. 2gg

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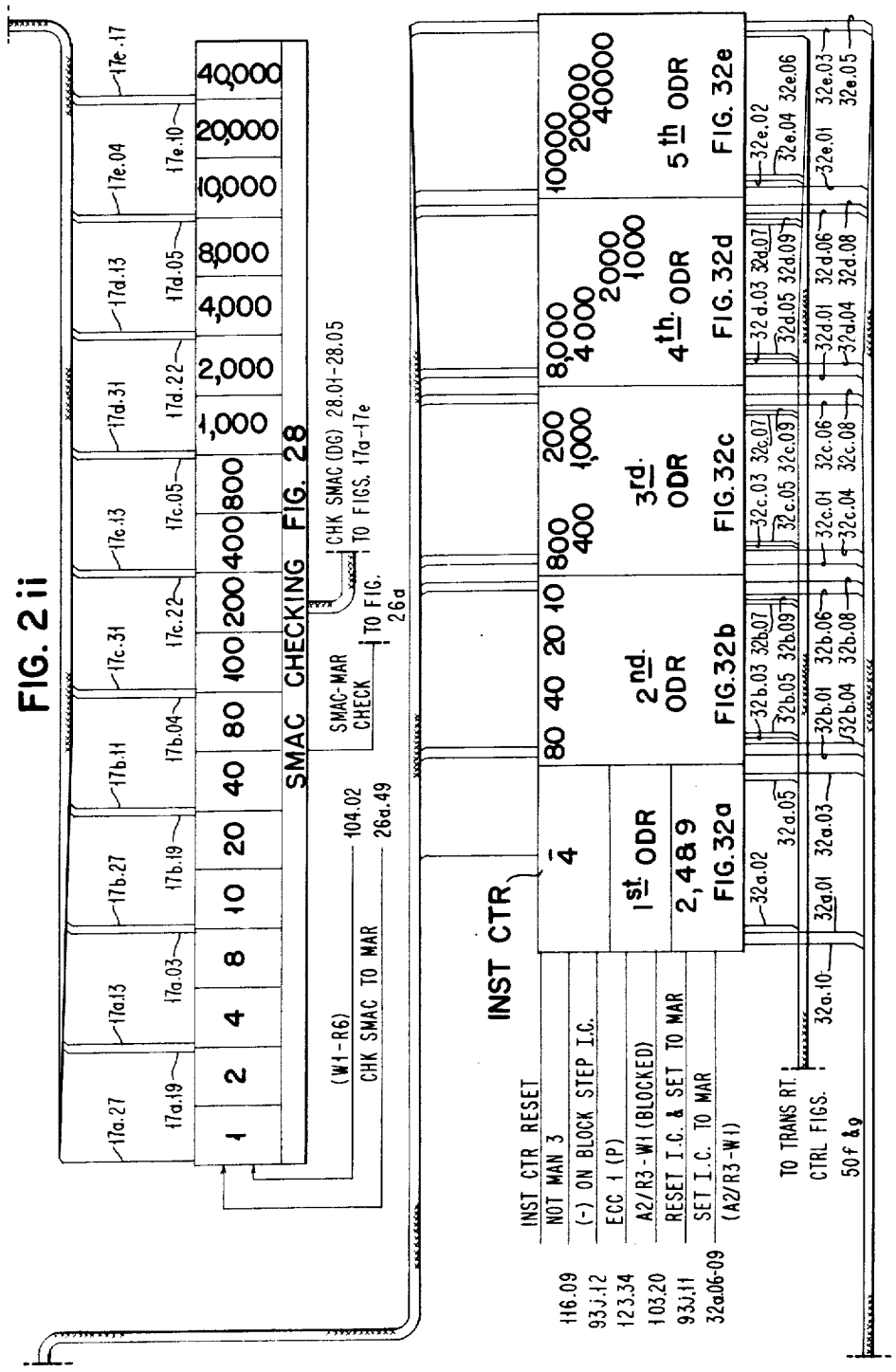

FIG. 2ii
SMAC CHECKING FIG. 28
1 2 4 8 10 20 40 80 100 200 400 800 1,000 2,000 4,000 8,000 10,000 20,000 40,000
SMAC-MAR CHECK
CHK SMAC (DG) 28.01-28.05
TO FIGS. 17a-17e
TO FIG. 26a
(W1-R6) 104.02
CHK SMAC TO MAR 26a.49
INST CTR
INST CTR RESET
NOT MAN 3
(-) ON BLOCK STEP I.C.
ECC 1 (P)
A2/R3-W1 (BLOCKED)
RESET I.C. & SET TO MAR
SET I.C. TO MAR
(A2/R3-W1)
116.09
93J.12
123.34
103.20
93J.11
32a.06-09
4
1st ODR
2,4,8,9
FIG. 32a
80 40 20 10
2nd ODR
FIG. 32b
800 400 200 1,000
3rd ODR
FIG. 32c
8,000 4,000 2,000 1000
4th ODR
FIG. 32d
10000 20000 40000
5th ODR
FIG. 32e
TO TRANS RT.
CTRL FIGS. 50f &9

FIG. 2 jj

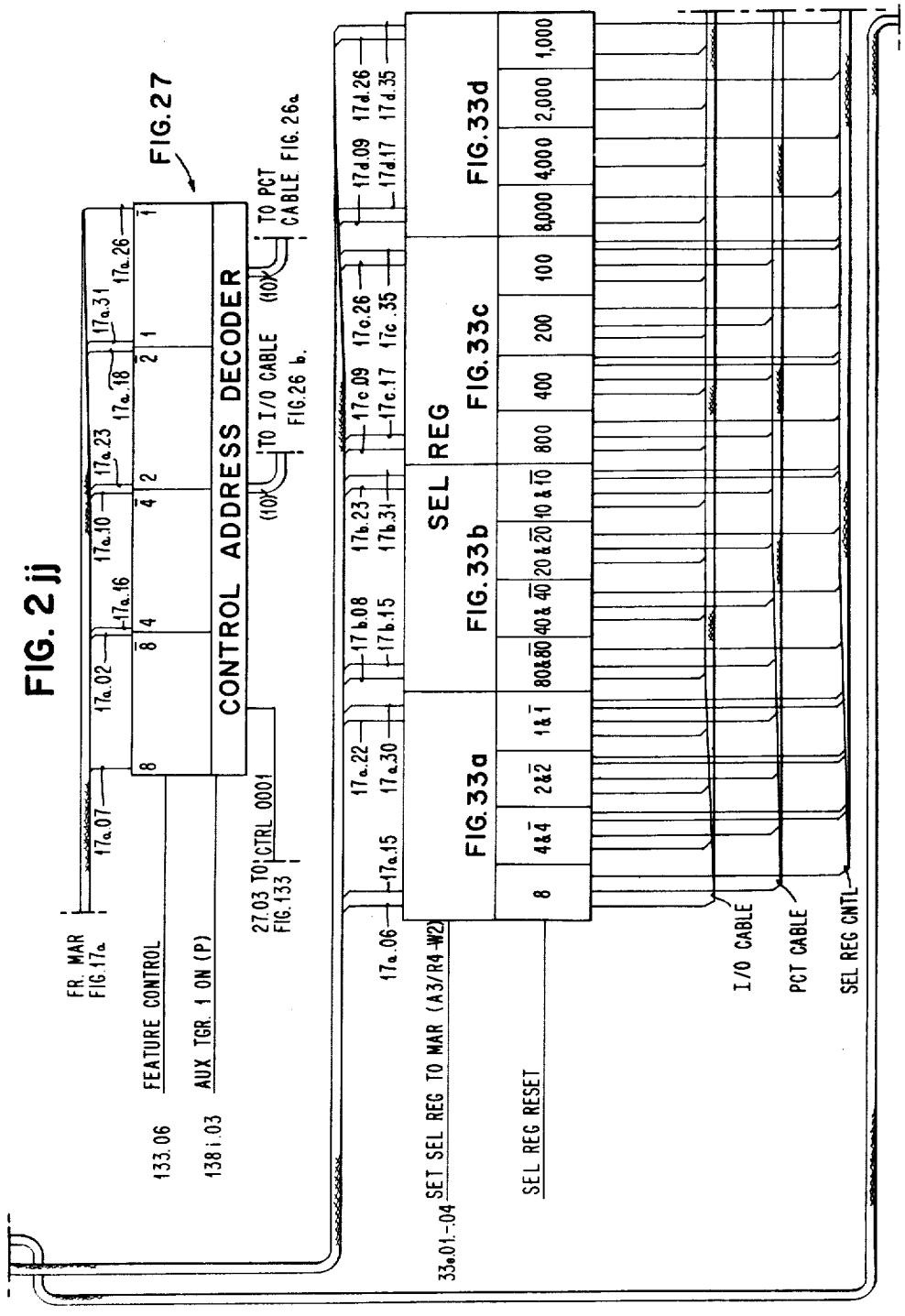

FIG. 27
CONTROL ADDRESS DECODER
TO PCT CABLE FIG. 26a
TO I/O CABLE FIG. 26 b.
FR. MAR FIG. 17a
FEATURE CONTROL
AUX TGR. 1 ON (P)
133.06
138i.03
27.03 TO: CTRL 0001 FIG. 133
SEL REG
FIG. 33a
FIG. 33b
FIG. 33c
FIG. 33d
SET SEL REG TO MAR (A3/R4→W2)
SEL REG RESET
I/O CABLE
PCT CABLE
SEL REG CNTL

FIG. 2kk

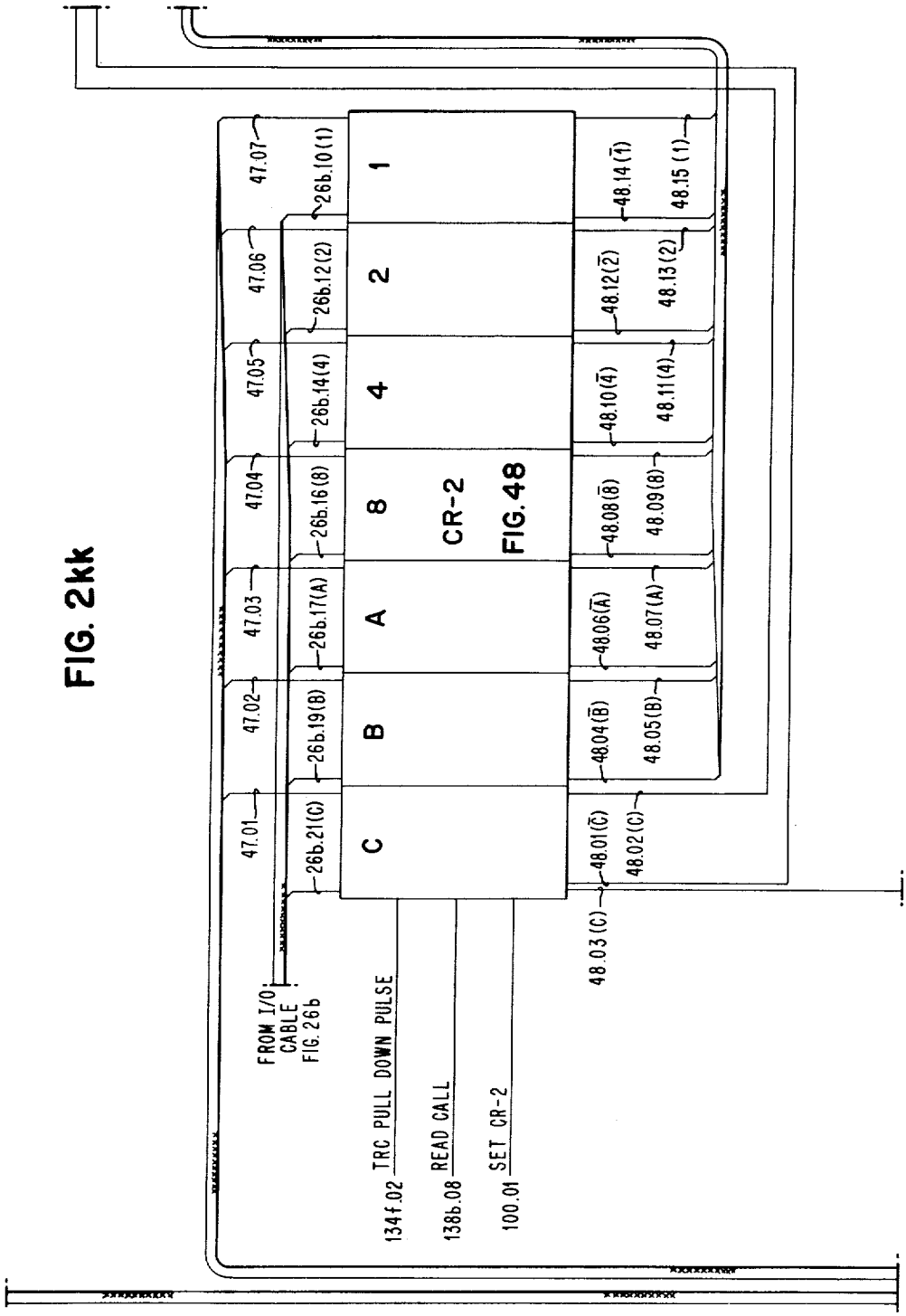

FIG. 48
CR-2
1
2
4
8
A
B
C
47.07
47.06
47.05
47.04
47.03
47.02
47.01
26b.10(1)
26b.12(2)
26b.14(4)
26b.16(8)
26b.17(A)
26b.19(B)
26b.21(C)
48.14(1̄)
48.15(1)
48.12(2̄)
48.13(2)
48.10(4̄)
48.11(4)
48.08(8̄)
48.09(8)
48.06(Ā)
48.07(A)
48.04(B̄)
48.05(B)
48.01(C̄)
48.02(C)
48.03(C)
FROM I/O CABLE FIG. 26b
134f.02 TRC PULL DOWN PULSE
138b.08 READ CALL
100.01 SET CR-2

FIG. 211

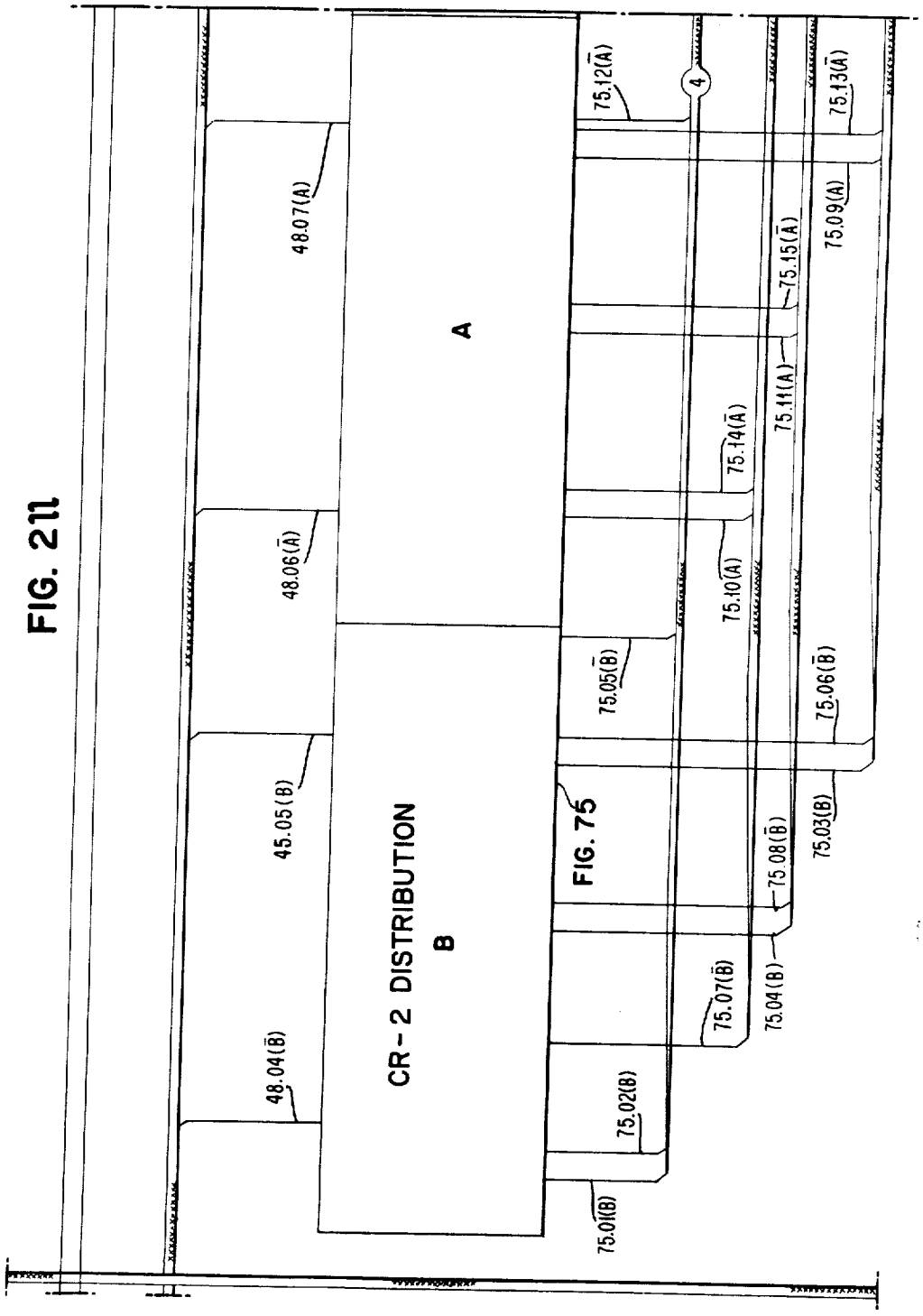

48.07(A)
48.06(Ā)
45.05(B)
48.04(B̄)
A
CR-2 DISTRIBUTION
B
FIG. 75
75.12(Ā)
4
75.13(Ā)
75.09(A)
75.15(Ā)
75.11(A)
75.14(Ā)
75.10(A)
75.05(B̄)
75.06(B̄)
75.03(B)
75.08(B̄)
75.04(B)
75.07(B̄)
75.02(B)
75.01(B)

FIG. 2mm

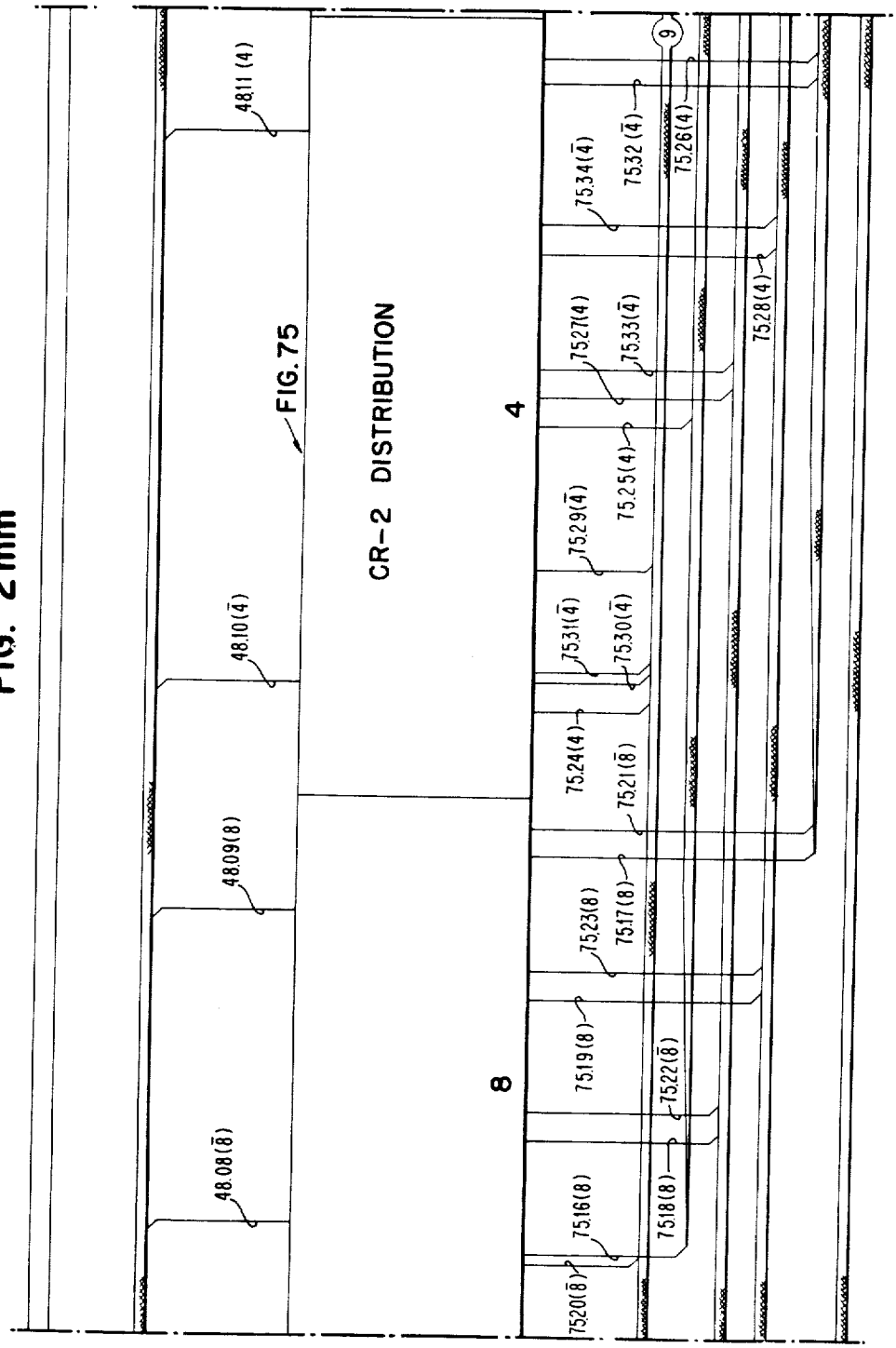
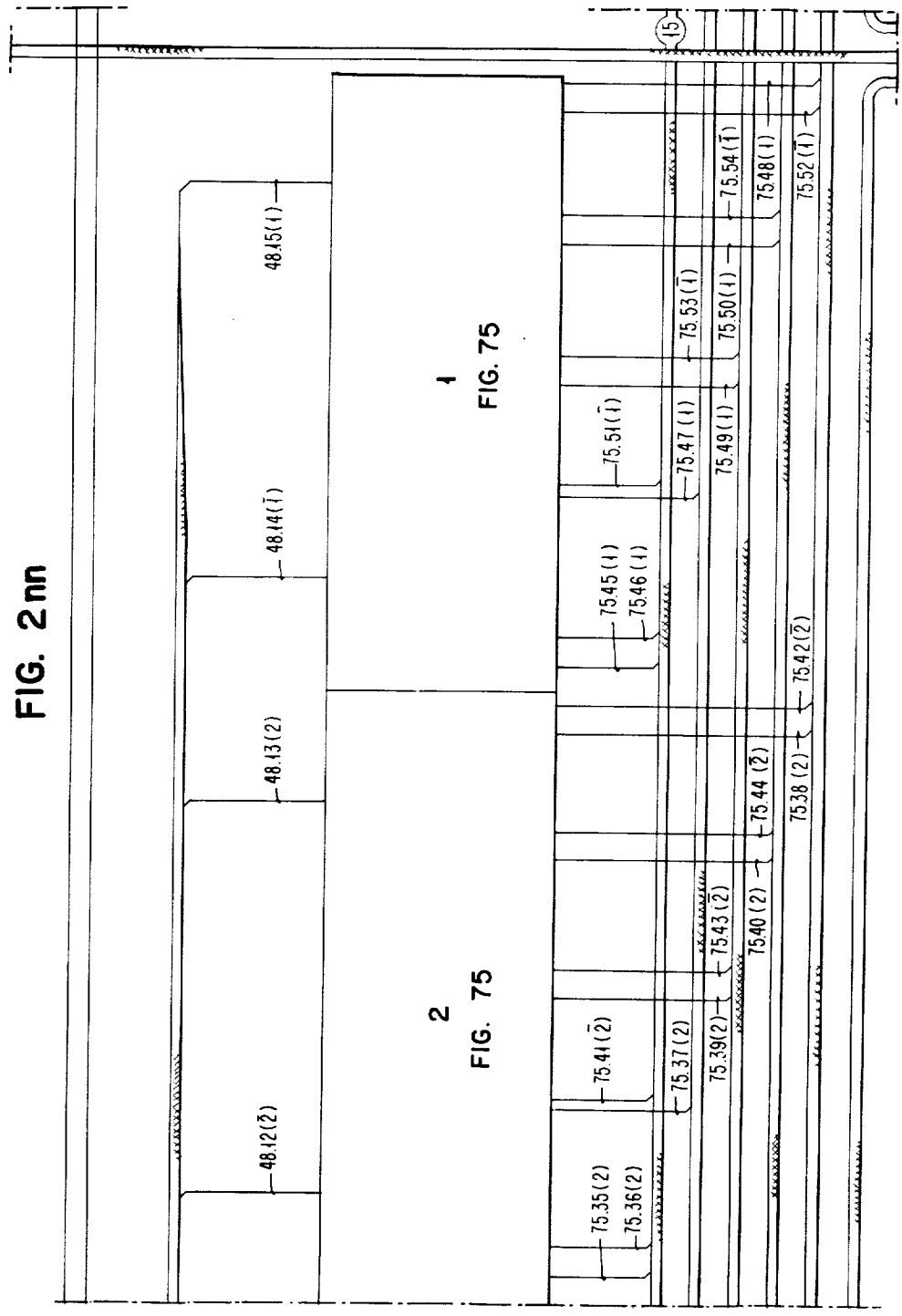

FIG. 75
CR-2 DISTRIBUTION
4
8
9
48.11(4)
48.10(4̄)
48.09(8)
48.08(8̄)
75.16(8)
75.17(8)
75.18(8)
75.19(8)
75.20(8̄)
75.21(8̄)
75.22(8̄)
75.23(8)
75.24(4)
75.25(4)
75.26(4)
75.27(4)
75.28(4)
75.29(4̄)
75.30(4)
75.31(4̄)
75.32(4̄)
75.33(4̄)
75.34(4̄)

FIG. 2nn


15
1
FIG. 75
2
FIG. 75
48.15(1)
48.14(1̄)
48.13(2)
48.12(2̄)
75.35(2)
75.36(2)
75.41(2̄)
75.37(2)
75.39(2)
75.43(2̄)
75.40(2)
75.44(2̄)
75.38(2)
75.42(2̄)
75.45(1)
75.46(1)
75.51(1̄)
75.47(1)
75.49(1)
75.53(1̄)
75.50(1)
75.54(1̄)
75.48(1)
75.52(1̄)

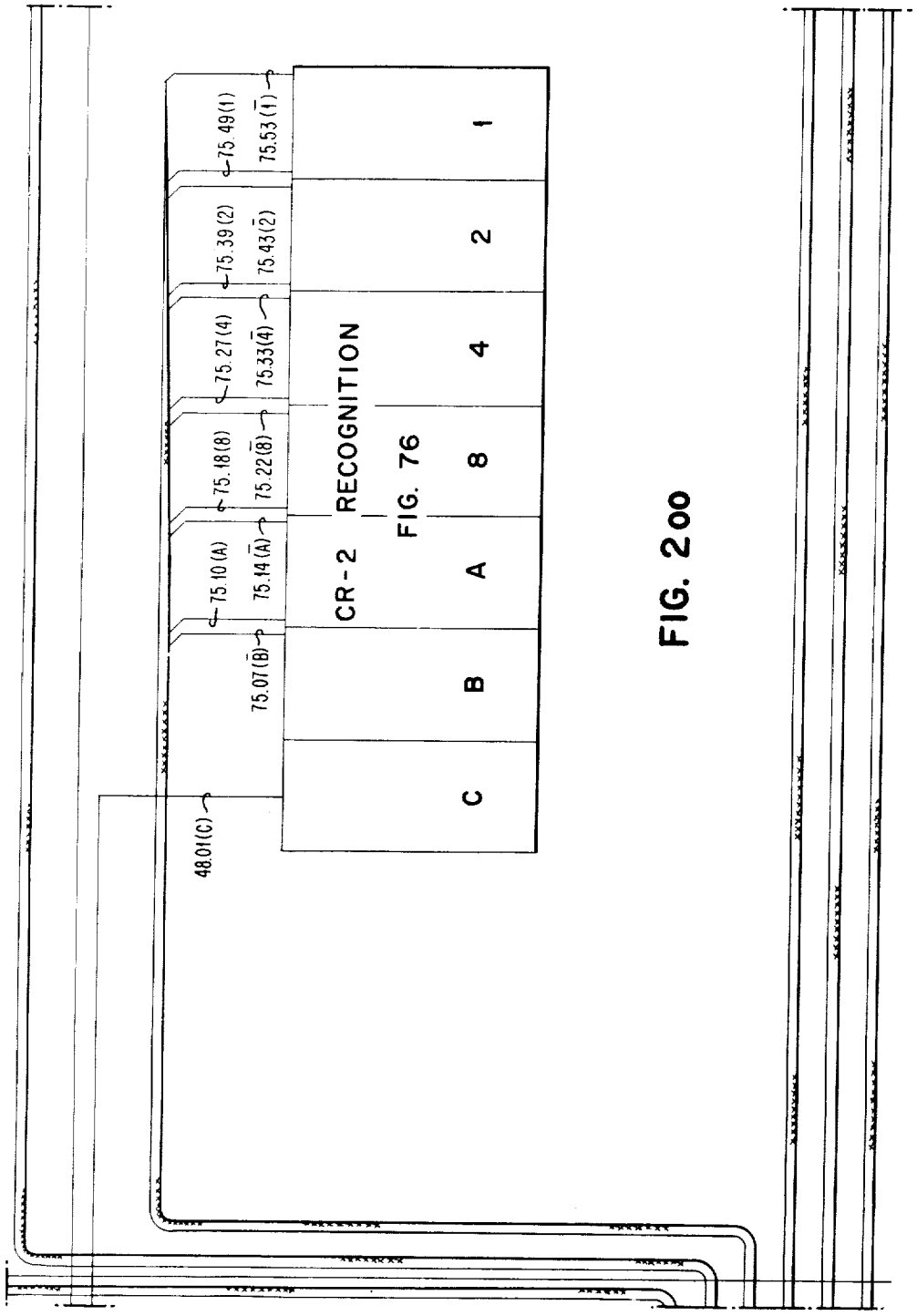

75.49(1)
75.53(1̄)
75.39(2)
75.43(2̄)
75.27(4)
75.33(4̄)
75.18(8)
75.22(8̄)
75.10(A)
75.14(Ā)
75.07(B̄)
48.01(C)
CR-2 RECOGNITION
FIG. 76
1
2
4
8
A
B
C

FIG. 200

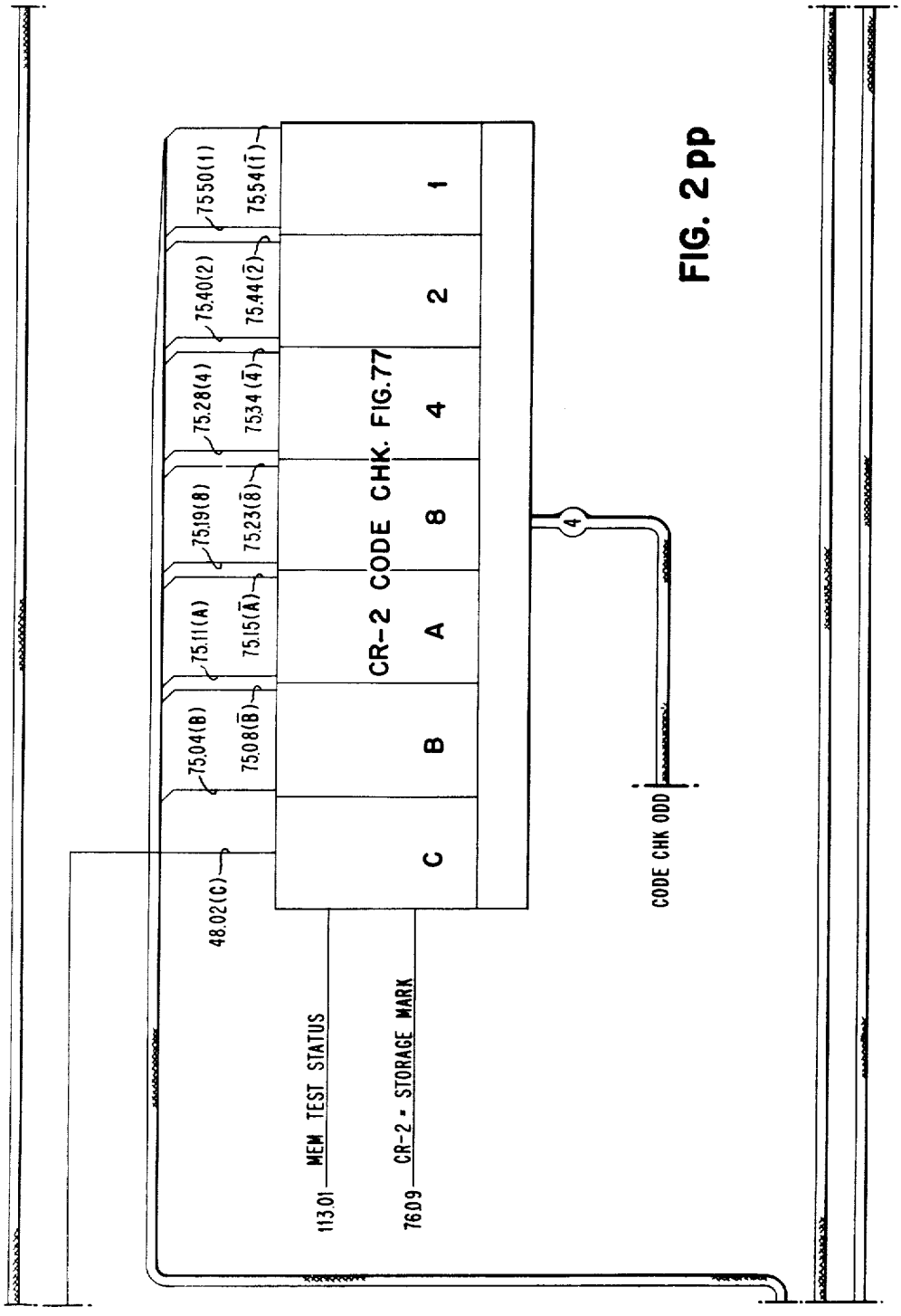

CR-2 CODE CHK. FIG. 77
C
B
A
8
4
2
1
75.04(B)
75.08(B̄)
75.11(A)
75.15(Ā)
75.19(8)
75.23(8̄)
75.28(4)
75.34(4̄)
75.40(2)
75.44(2̄)
75.50(1)
75.54(1̄)
48.02(C)
113.01 MEM TEST STATUS
76.09 CR-2 - STORAGE MARK
CODE CHK ODD
4

FIG. 2pp

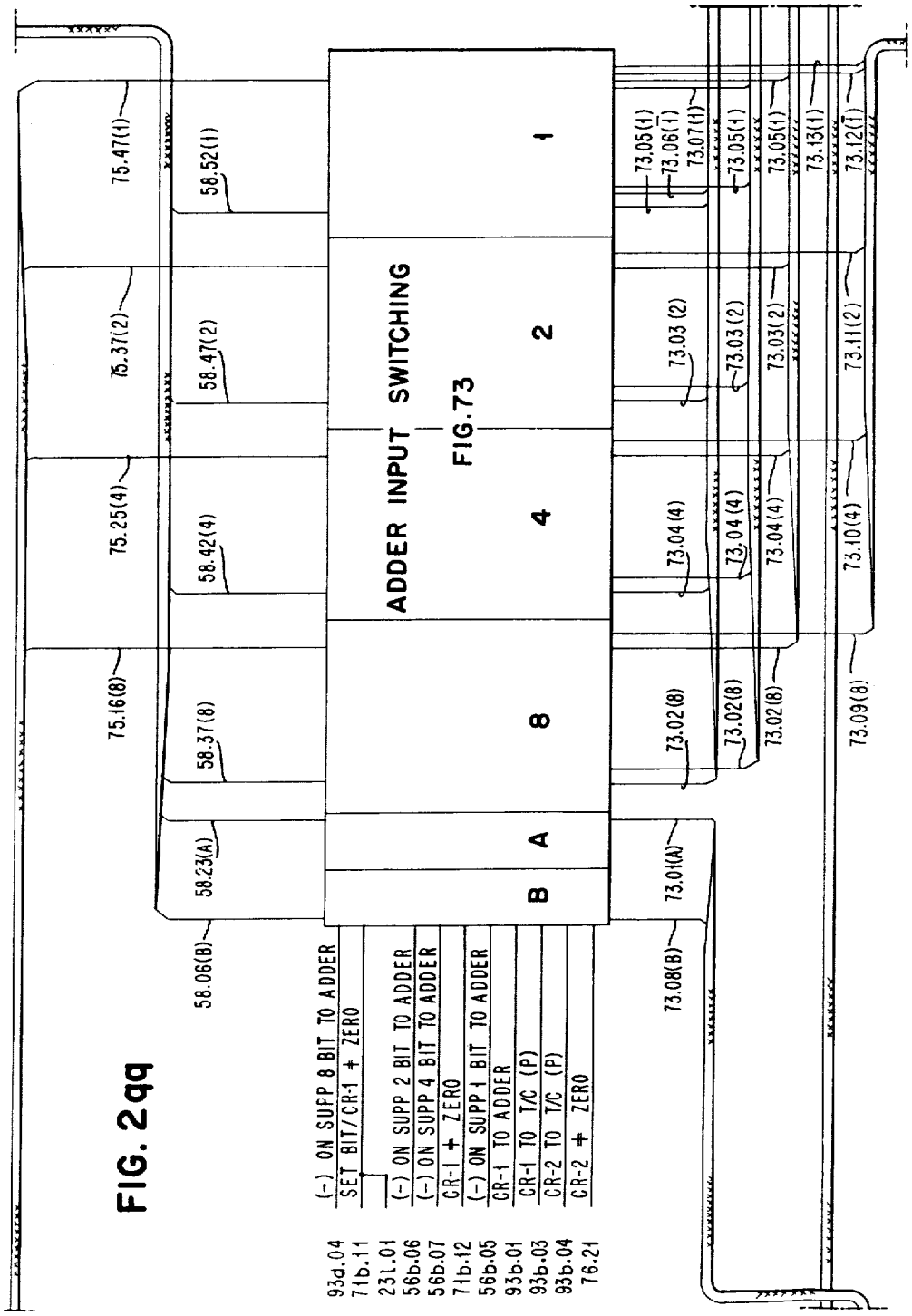

ADDER INPUT SWITCHING
FIG. 73
1
2
4
8
A
B
75.47(1)
75.37(2)
75.25(4)
75.16(8)
58.52(1)
58.47(2)
58.42(4)
58.37(8)
58.23(A)
58.06(B)
73.05(1)
73.06(1)
73.07(1)
73.03(2)
73.04(4)
73.02(8)
73.01(A)
73.08(B)
73.13(1)
73.11(2)
73.10(4)
73.09(8)
(-) ON SUPP 8 BIT TO ADDER
SET BIT/CR-1 + ZERO
(-) ON SUPP 2 BIT TO ADDER
(-) ON SUPP 4 BIT TO ADDER
CR-1 + ZERO
(-) ON SUPP 1 BIT TO ADDER
CR-1 TO ADDER
CR-1 TO T/C (P)
CR-2 TO T/C (P)
CR-2 + ZERO
93d.04
71b.11
231.01
56b.06
56b.07
71b.12
56b.05
93b.01
93b.03
93b.04
76.21

FIG. 2qq

FIG. 2rr

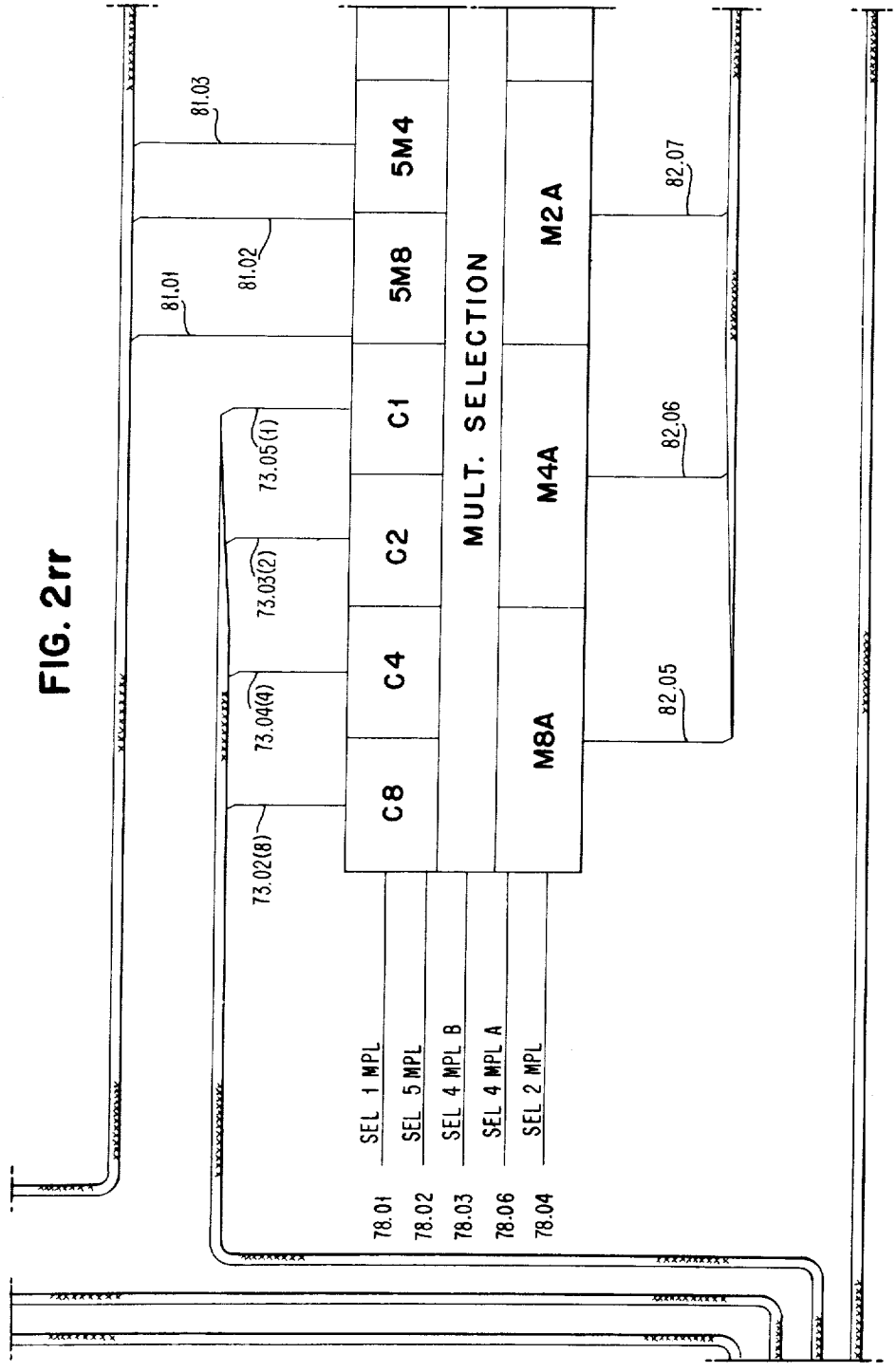
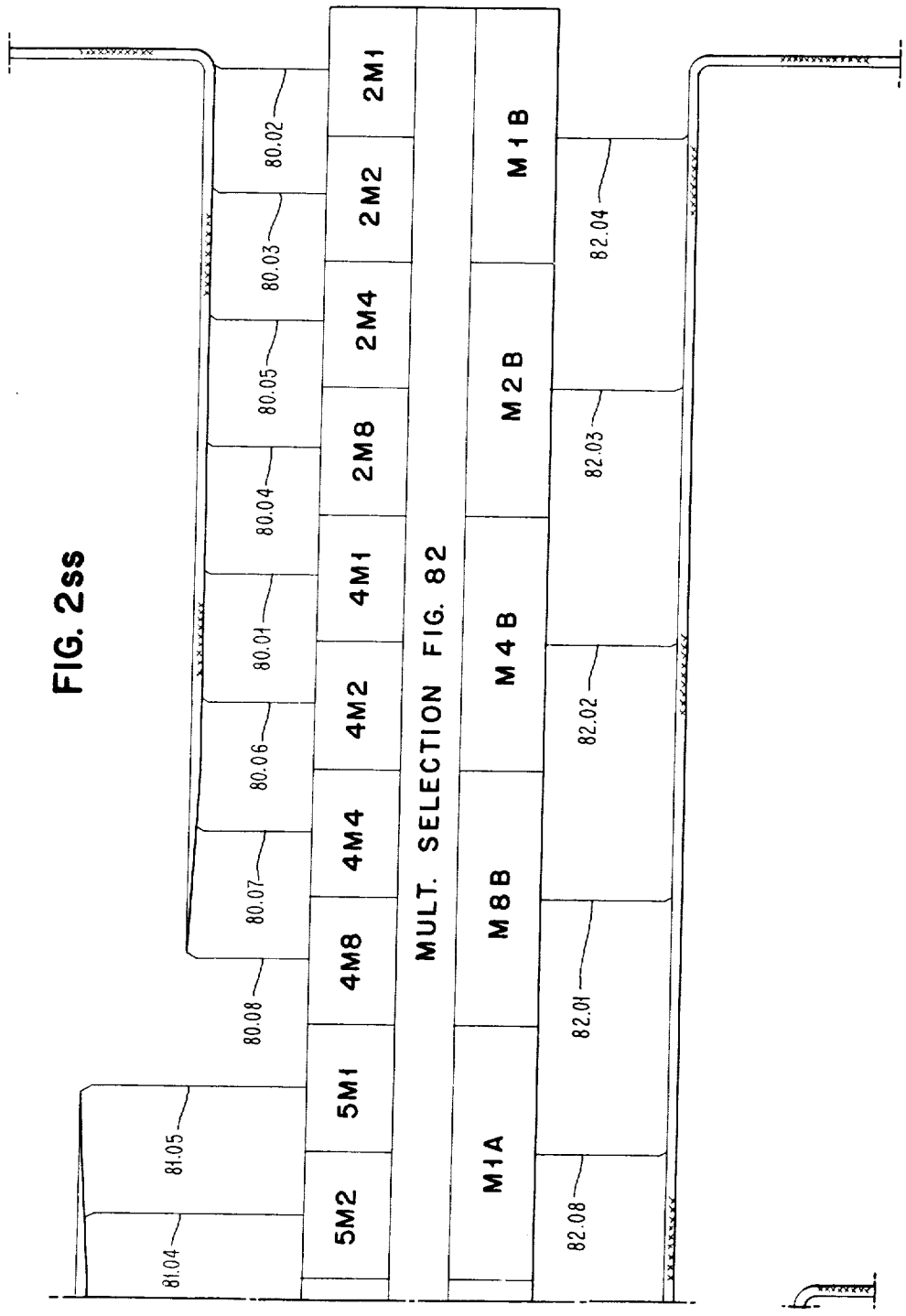

81.03
81.02
81.01
73.05(1)
73.03(2)
73.04(4)
73.02(8)
5M4
5M8
C1
C2
C4
C8
MULT. SELECTION
M2A
M4A
M8A
82.07
82.06
82.05
SEL 1 MPL
SEL 5 MPL
SEL 4 MPL B
SEL 4 MPL A
SEL 2 MPL
78.01
78.02
78.03
78.06
78.04

FIG. 2ss


2M1
2M2
2M4
2M8
4M1
4M2
4M4
4M8
5M1
5M2
MULT. SELECTION FIG. 82
M1B
M2B
M4B
M8B
M1A
80.02
80.03
80.05
80.04
80.01
80.06
80.07
80.08
81.05
81.04
82.04
82.03
82.02
82.01
82.08

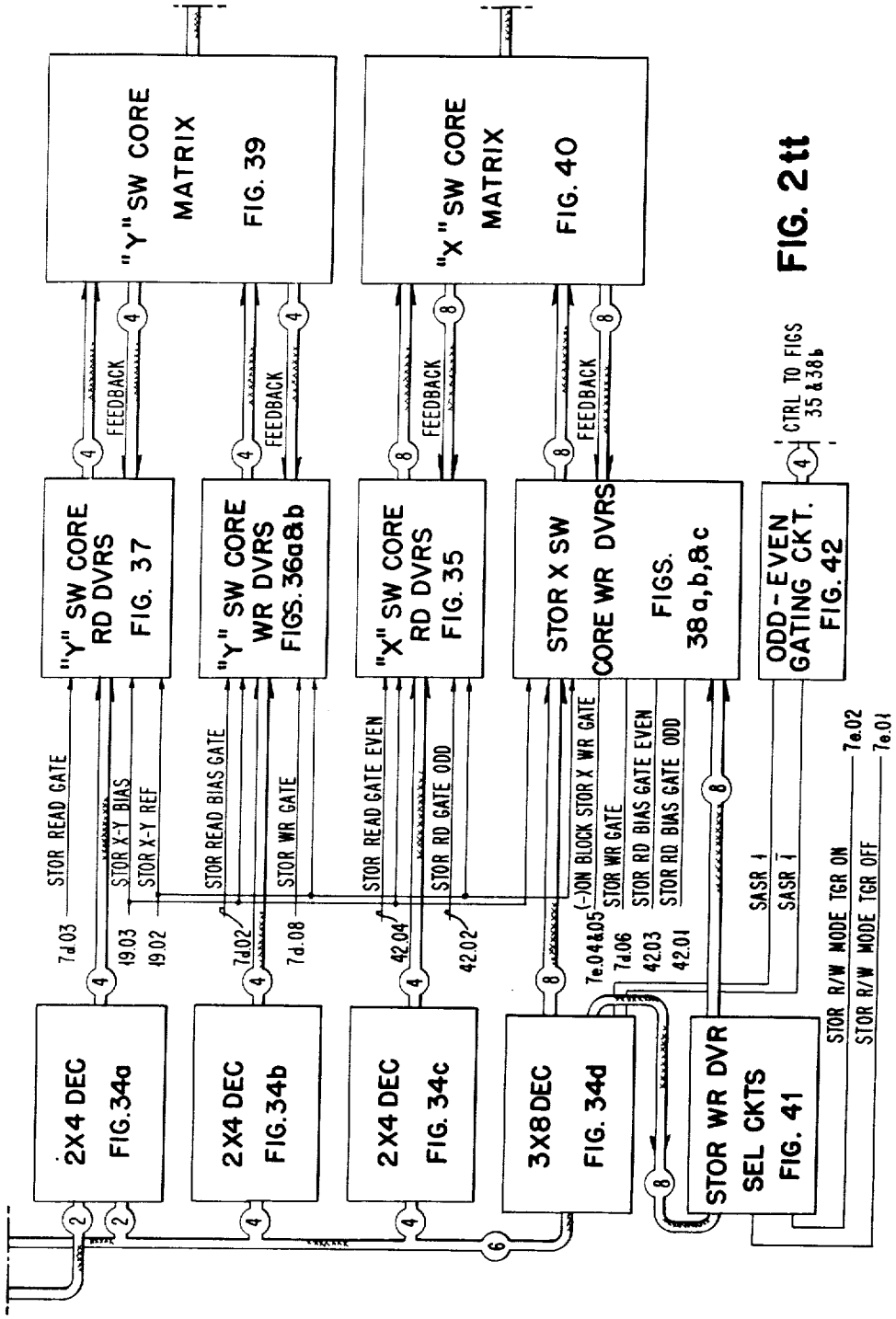

"Y" SW CORE MATRIX FIG. 39
"X" SW CORE MATRIX FIG. 40
"Y" SW CORE RD DVRS FIG. 37
"Y" SW CORE WR DVRS FIGS. 36a&b
"X" SW CORE RD DVRS FIG. 35
STOR X SW CORE WR DVRS FIGS. 38a,b,&c
ODD-EVEN GATING CKT. FIG. 42
2X4 DEC FIG. 34a
2X4 DEC FIG. 34b
2X4 DEC FIG. 34c
3X8 DEC FIG. 34d
STOR WR DVR SEL CKTS FIG. 41
FEEDBACK
CTRL TO FIGS 35 & 38b
STOR READ GATE
STOR X-Y BIAS
STOR X-Y REF
STOR READ BIAS GATE
STOR WR GATE
STOR READ GATE EVEN
STOR RD GATE ODD
(-)ON BLOCK STOR X WR GATE
STOR WR GATE
STOR RD BIAS GATE EVEN
STOR RD BIAS GATE ODD
SASR 1
SASR 1
STOR R/W MODE TGR ON
STOR R/W MODE TGR OFF

FIG. 2tt

FIG. 2uu

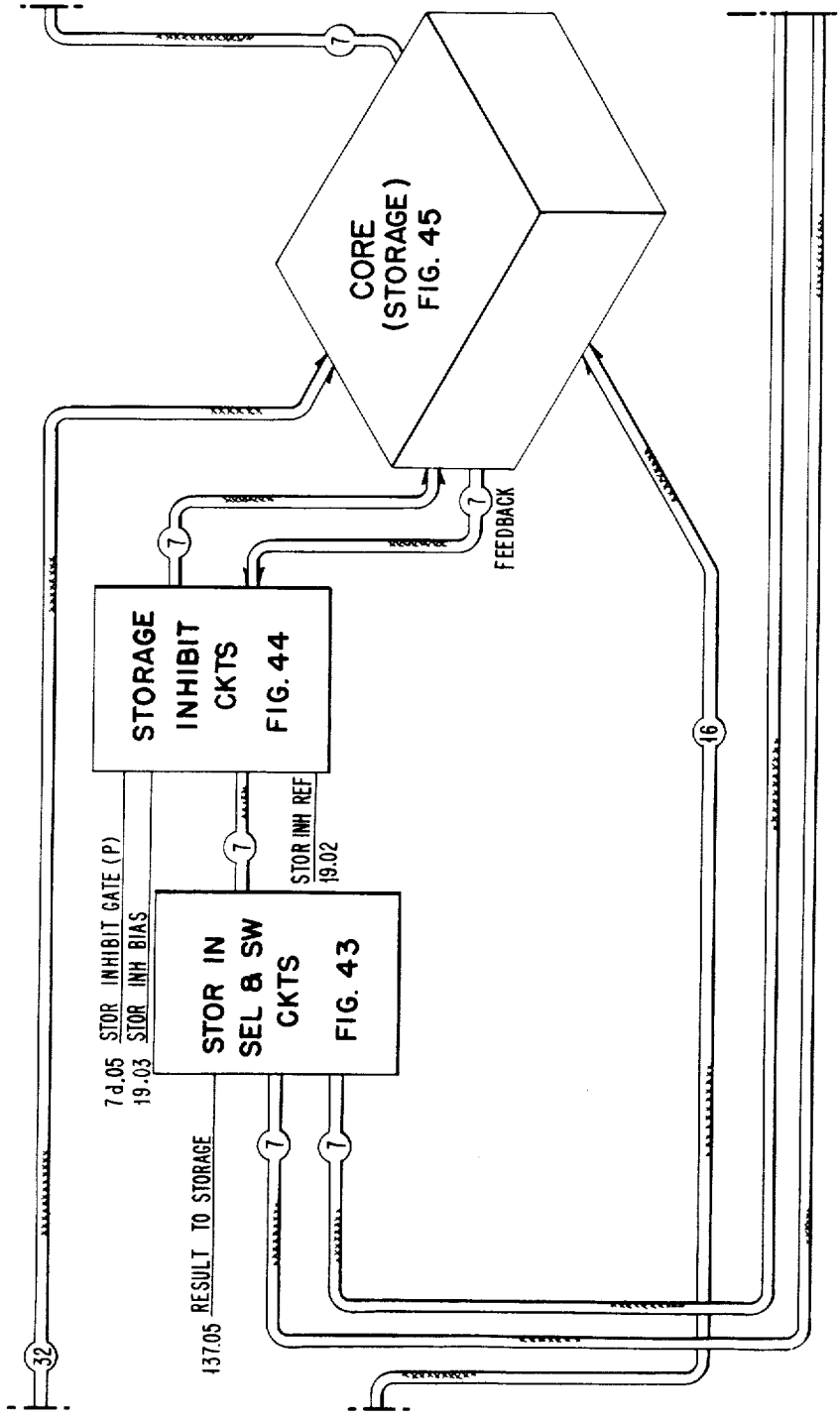
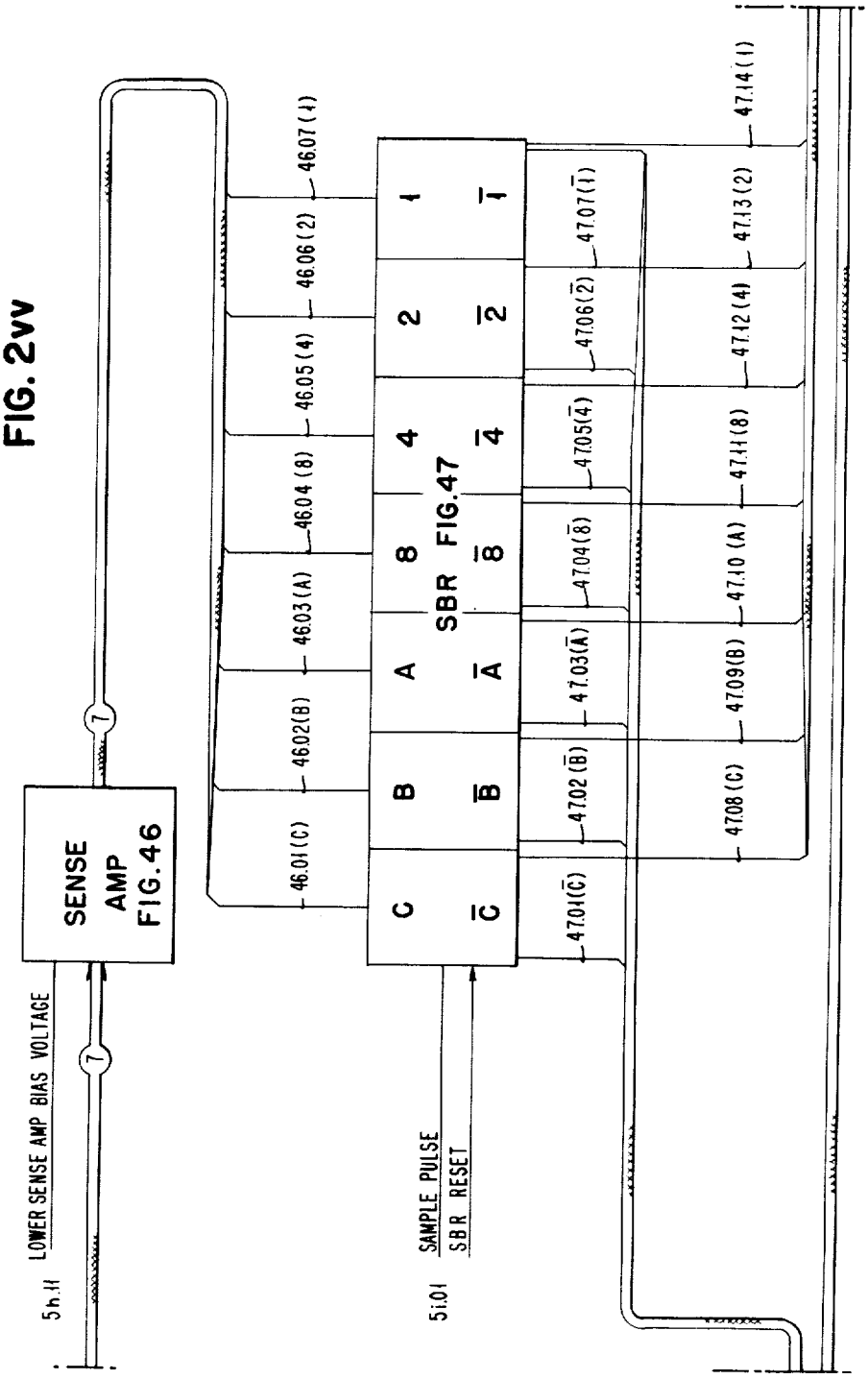
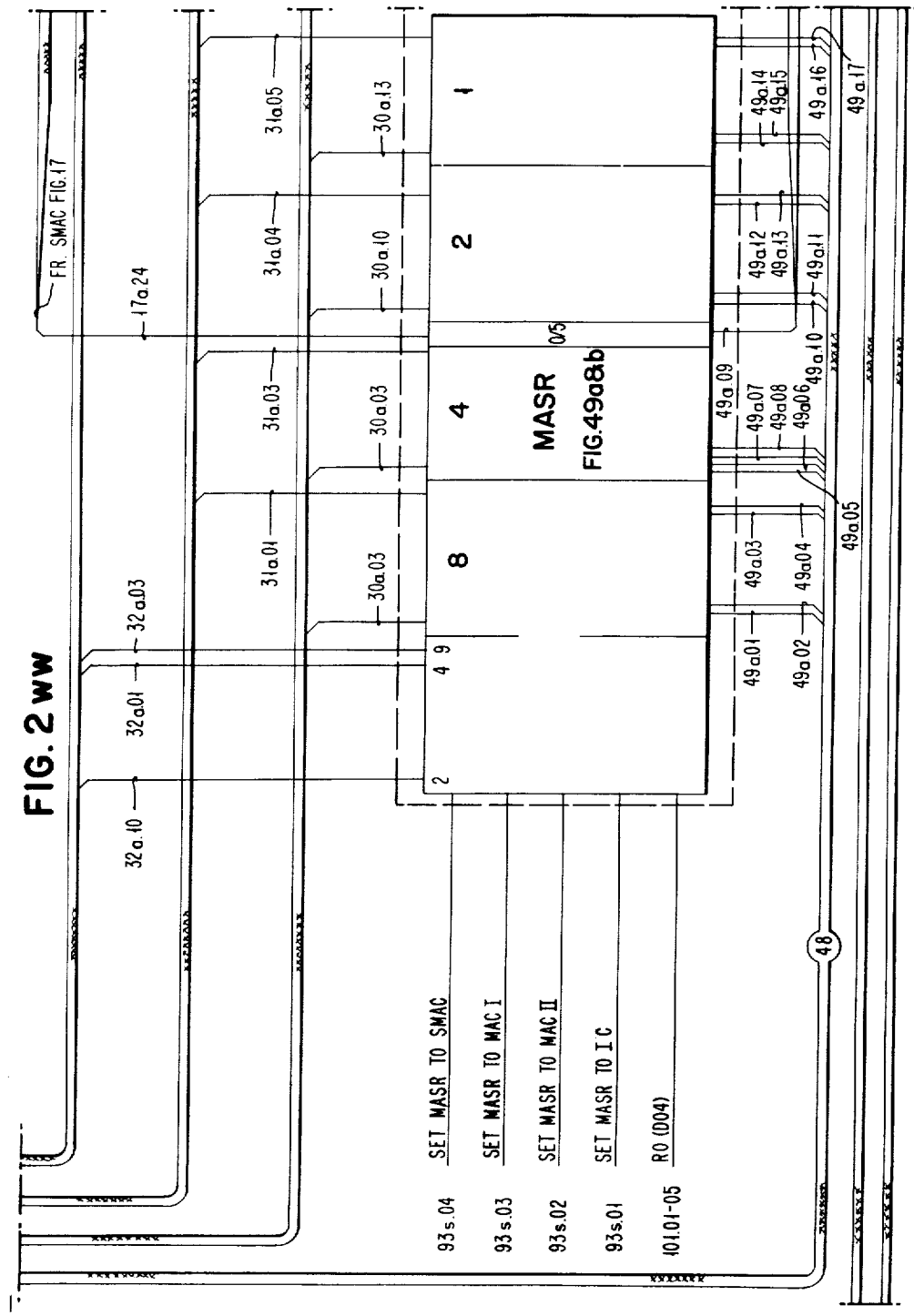
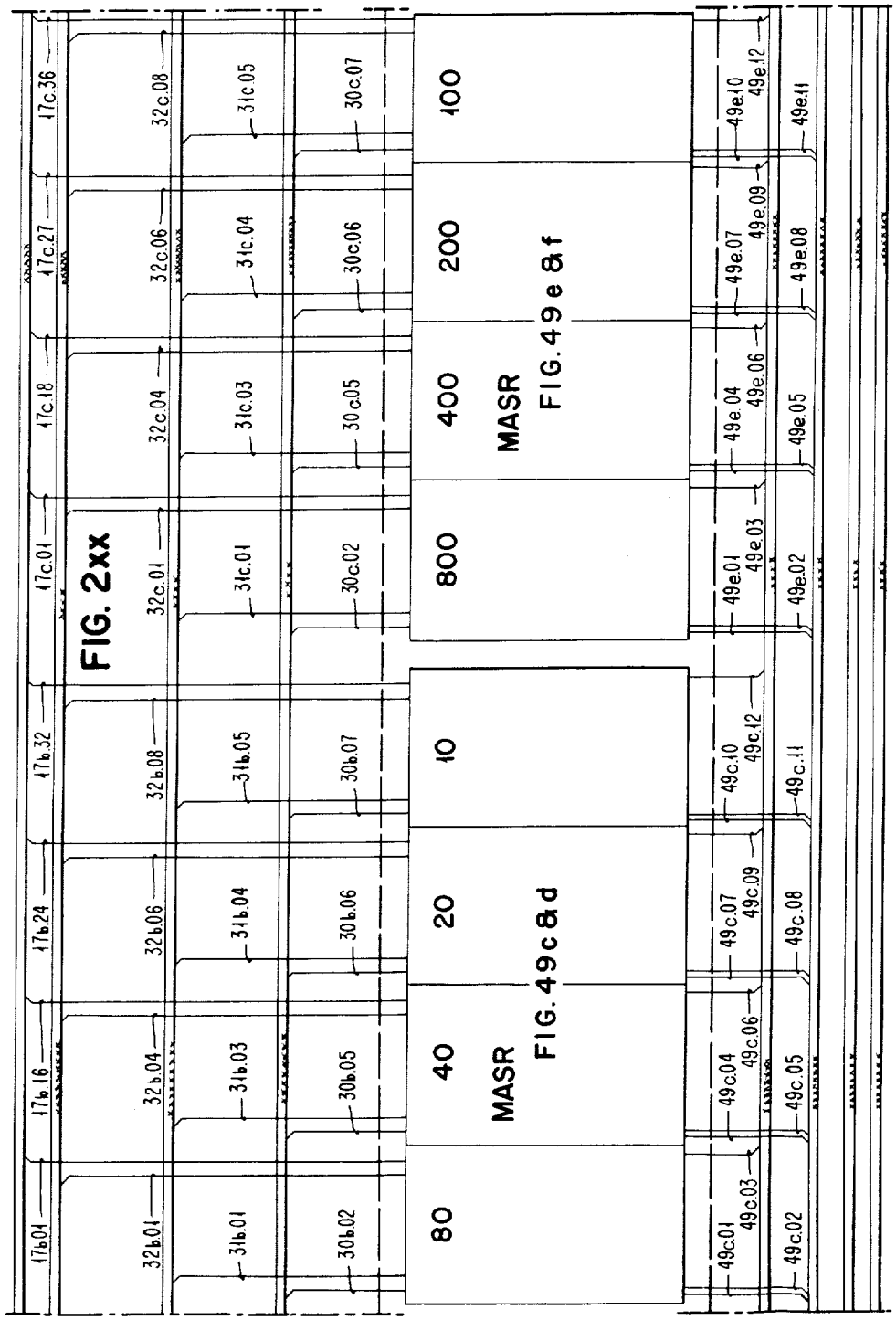
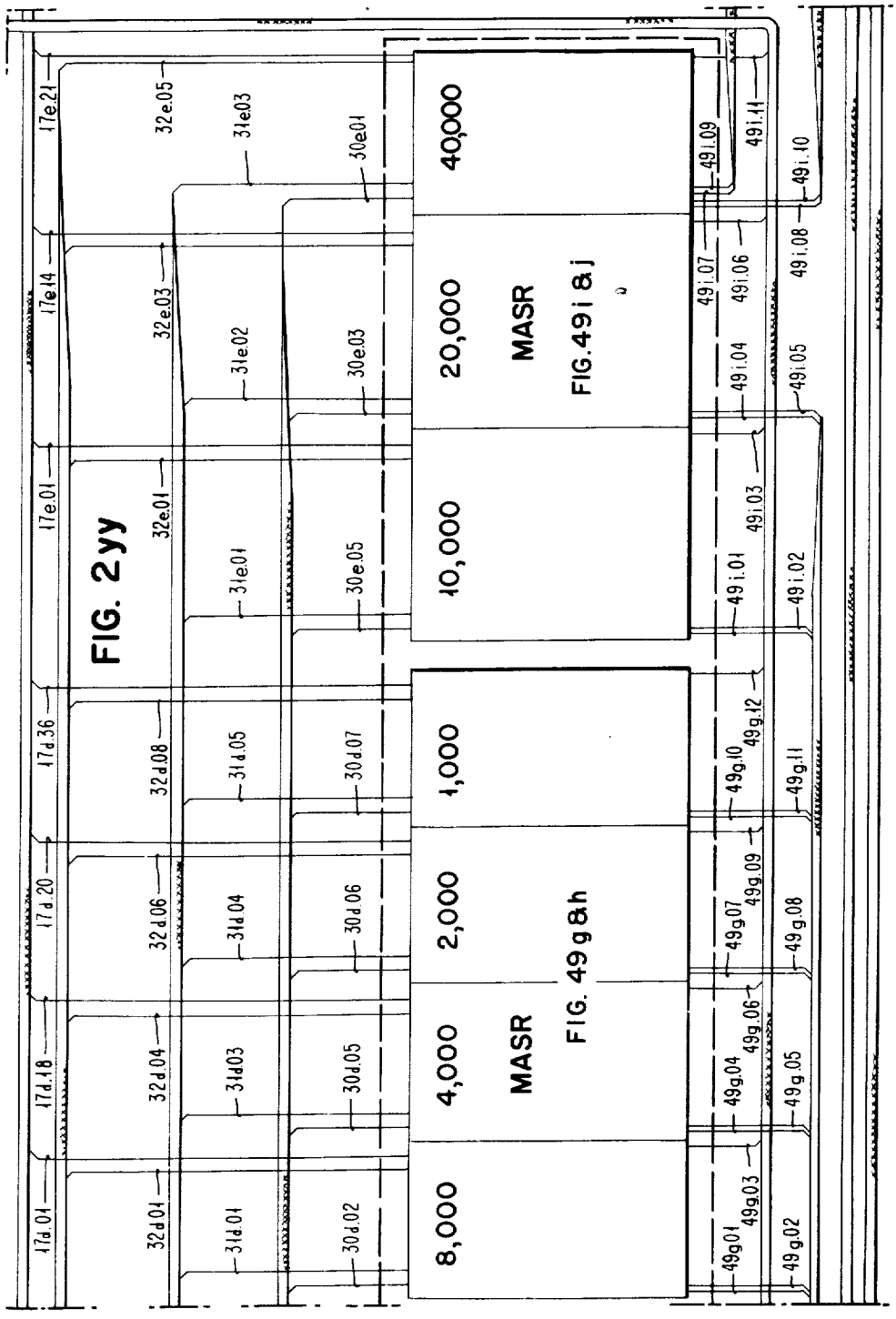

CORE (STORAGE) FIG. 45
STORAGE INHIBIT CKTS FIG. 44
STOR IN SEL & SW CKTS FIG. 43
FEEDBACK
STOR INH REF 19.02
7d.05 STOR INHIBIT GATE (P)
19.03 STOR INH BIAS
137.05 RESULT TO STORAGE
7
16
32

FIG. 2vv


SENSE AMP FIG.46
LOWER SENSE AMP BIAS VOLTAGE
5h.11
SAMPLE PULSE
SBR RESET
5i.01
SBR FIG.47
C
B
A
8
4
2
1
$\bar{C}$
$\bar{B}$
$\bar{A}$
$\bar{8}$
$\bar{4}$
$\bar{2}$
$\bar{1}$
46.01(C)
46.02(B)
46.03(A)
46.04(8)
46.05(4)
46.06(2)
46.07(1)
47.01($\bar{C}$)
47.02($\bar{B}$)
47.03($\bar{A}$)
47.04($\bar{8}$)
47.05($\bar{4}$)
47.06($\bar{2}$)
47.07($\bar{1}$)
47.08(C)
47.09(B)
47.10(A)
47.11(8)
47.12(4)
47.13(2)
47.14(1)


FIG. 2 ww
FR. SMAC FIG. 17
17a.24
31a.05
31a.04
31a.03
31a.01
30a.13
30a.10
30a.03
30a.03
32a.03
32a.01
32a.10
MASR
FIG. 49a8b
1
2
4
8
4 9
2
0/5
49a.09
49a.07
49a08
49a06
49a.10
49a.14
49a15
49a.16
49a.17
49a.12
49a.13
49a.11
49a03
49a04
49a05
49a01
49a02
48
SET MASR TO SMAC
SET MASR TO MAC I
SET MASR TO MAC II
SET MASR TO I C
RO (004)
93s.04
93s.03
93s.02
93s.01
101.01-05


FIG. 2xx
MASR
FIG. 49c & d
MASR
FIG. 49e & f
80
40
20
10
800
400
200
100
17b.01
17b.16
17b.24
17b.32
17c.01
17c.18
17c.27
17c.36
32b.01
32b.04
32b.06
32b.08
32c.01
32c.04
32c.06
32c.08
31b.01
31b.03
31b.04
31b.05
31c.01
31c.03
31c.04
31c.05
30b.02
30b.05
30b.06
30b.07
30c.02
30c.05
30c.06
30c.07
49c.01
49c.03
49c.04
49c.06
49c.07
49c.09
49c.10
49c.12
49c.02
49c.05
49c.08
49c.11
49e.01
49e.03
49e.04
49e.06
49e.07
49e.09
49e.10
49e.12
49e.02
49e.05
49e.08
49e.11


FIG. 2yy
40,000
20,000
10,000
MASR
FIG. 49i & j
1,000
2,000
4,000
8,000
MASR
FIG. 49g & h
17d.01
17d.04
17d.18
17d.20
17d.36
17e.01
17e.14
17e.21
32d.01
32d.04
32d.06
32d.08
32e.01
32e.03
32e.05
31d.01
31d.03
31d.04
31d.05
31e.01
31e.02
31e.03
30d.02
30d.05
30d.06
30d.07
30e.05
30e.03
30e.01
49g.01
49g.03
49g.04
49g.06
49g.07
49g.09
49g.10
49g.12
49g.02
49g.05
49g.08
49g.11
49i.01
49i.03
49i.04
49i.05
49i.07
49i.06
49i.08
49i.09
49i.11
49i.10
49i.02

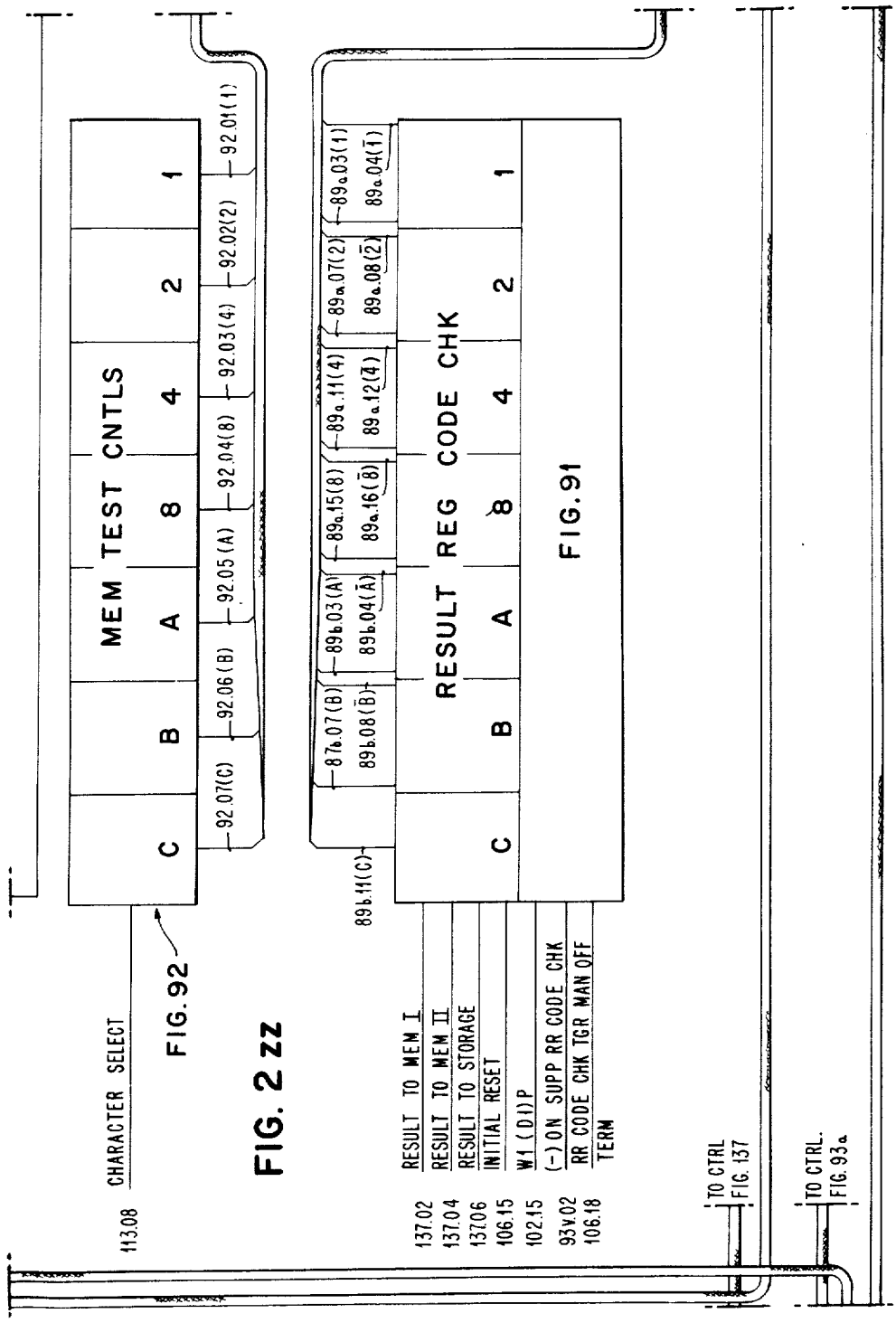
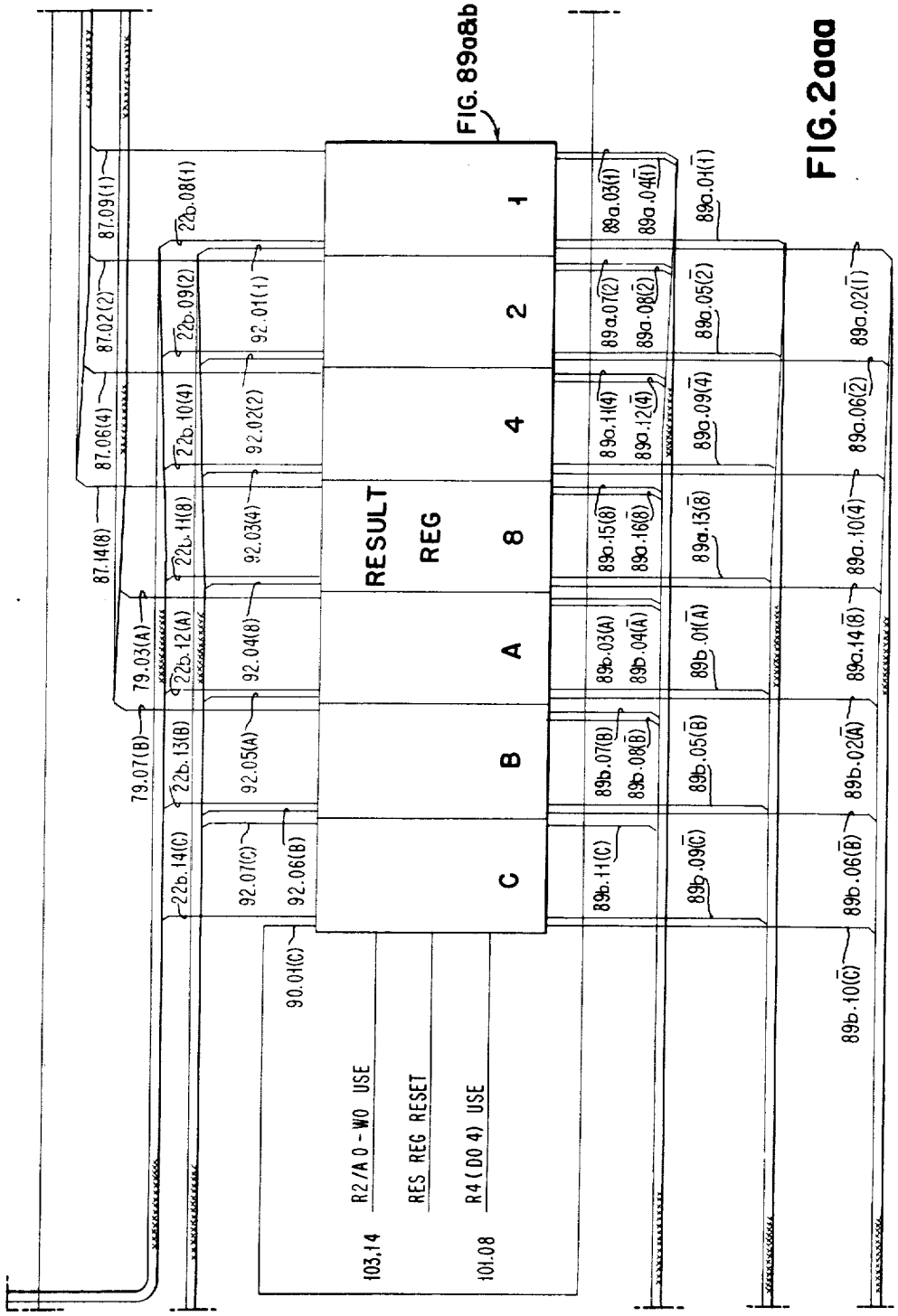

MEM TEST CNTLS
C
B
A
8
4
2
1
92.07(C)
92.06(B)
92.05(A)
92.04(8)
92.03(4)
92.02(2)
92.01(1)
RESULT REG CODE CHK
87b.07(B)
89b.08(B̄)
89b.03(A)
89b.04(Ā)
89a.15(8)
89a.16(8̄)
89a.11(4)
89a.12(4̄)
89a.07(2)
89a.08(2̄)
89a.03(1)
89a.04(1̄)
89b.11(C)
FIG. 91
FIG. 92
CHARACTER SELECT
113.08
RESULT TO MEM I
RESULT TO MEM II
RESULT TO STORAGE
INITIAL RESET
W1 (01)P
(-) ON SUPP RR CODE CHK
RR CODE CHK TGR MAN OFF
TERM
137.02
137.04
137.06
106.15
102.15
93v.02
106.18
TO CTRL FIG. 137
TO CTRL. FIG. 93a

FIG. 2zz

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FIG. 2aa



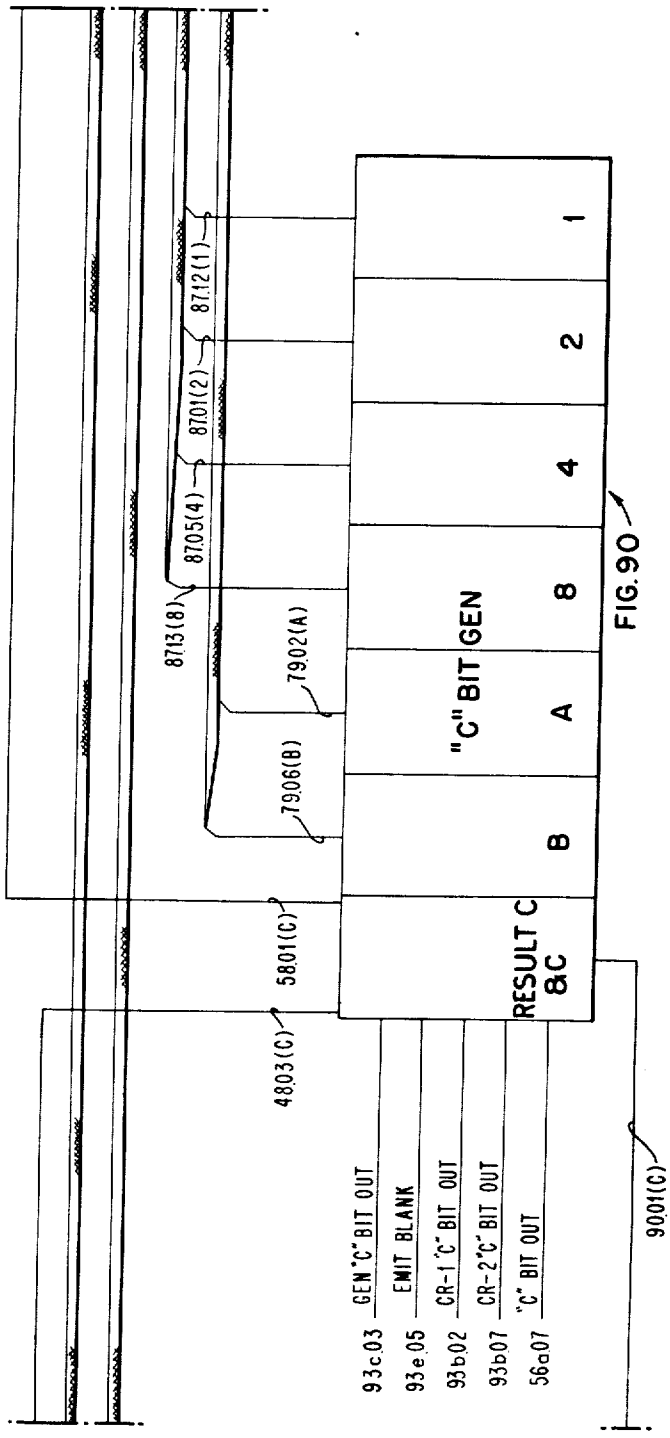

87.13(8)
87.05(4)
87.01(2)
87.12(1)
79.02(A)
79.06(B)
58.01(C)
48.03(C)
"C" BIT GEN
RESULT C &C
1
2
4
8
A
B
FIG. 90
90.01(C)
93c.03 GEN "C" BIT OUT
93e.05 EMIT BLANK
93b.02 CR-1 "C" BIT OUT
93b.07 CR-2 "C" BIT OUT
56a.07 "C" BIT OUT

FIG. 2bbb

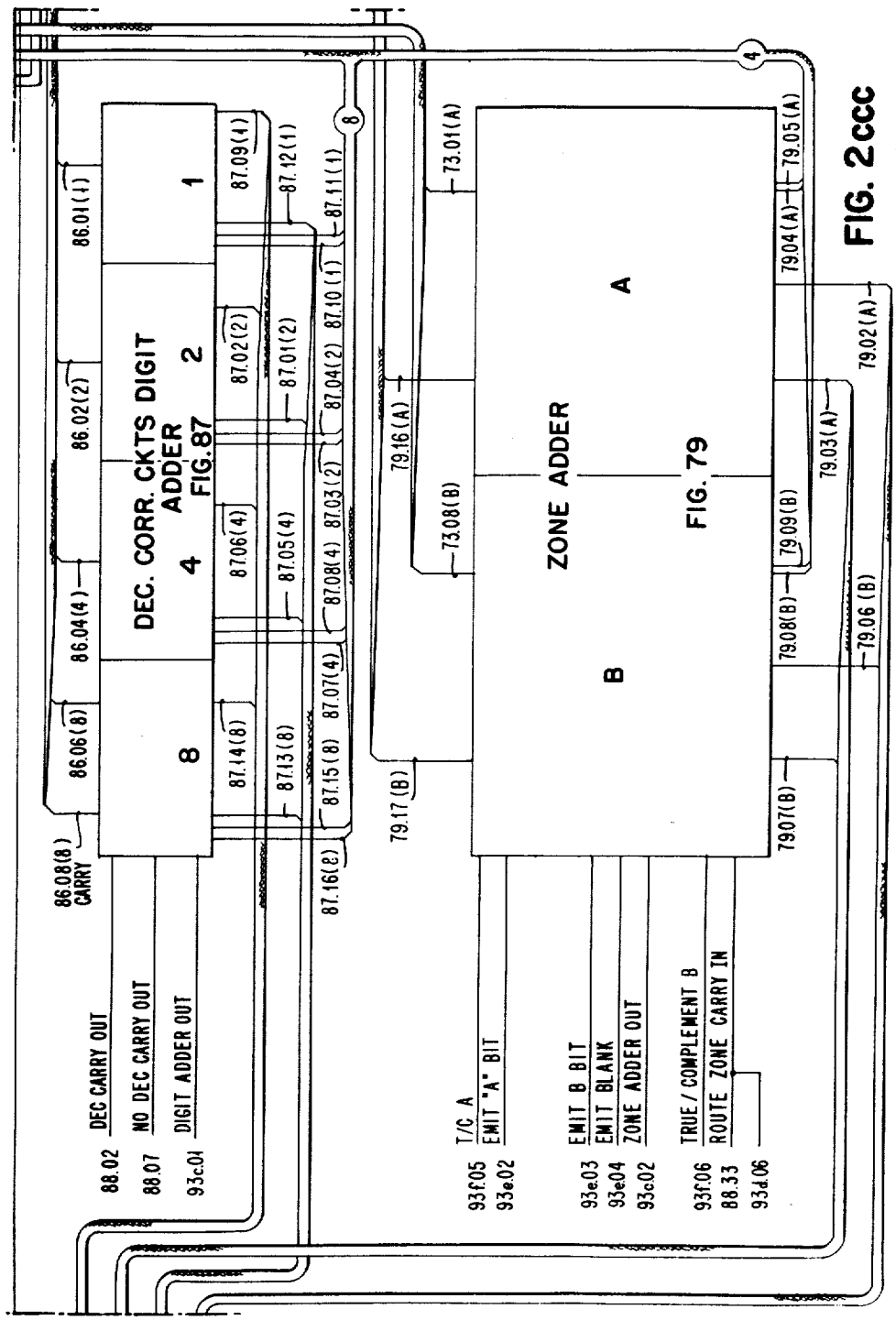

DEC. CORR. CKTS DIGIT ADDER FIG. 87
8
4
2
1
ZONE ADDER FIG. 79
A
B
86.08(8) CARRY
86.06(8)
86.04(4)
86.02(2)
86.01(1)
87.14(8)
87.13(8)
87.15(8)
87.07(4)
87.16(E)
87.06(4)
87.05(4)
87.08(4)
87.03(2)
87.02(2)
87.01(2)
87.04(2)
87.09(1)
87.12(1)
87.10(1)
87.11(1)
79.17(B)
79.16(A)
73.08(B)
73.01(A)
79.07(B)
79.08(B)
79.09(B)
79.04(A)
79.05(A)
79.02(A)
79.03(A)
79.06(B)
88.02 DEC CARRY OUT
88.07 NO DEC CARRY OUT
93c01 DIGIT ADDER OUT
93f05 T/C A
93e02 EMIT "A" BIT
93e03 EMIT B BIT
93e04 EMIT BLANK
93c02 ZONE ADDER OUT
93f06 TRUE / COMPLEMENT B
88.33 ROUTE ZONE CARRY IN
93d06

FIG. 2ccc

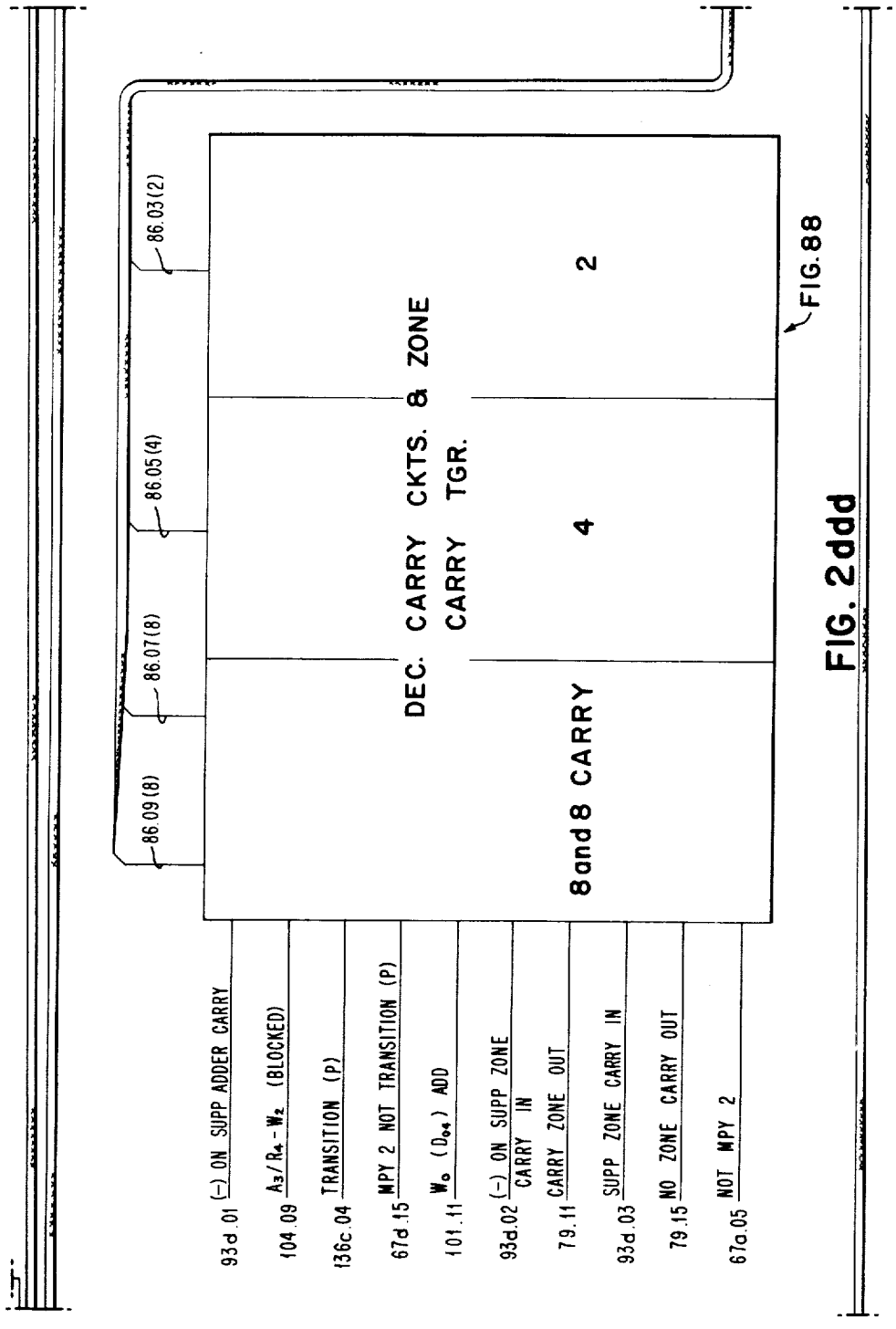


FIG. 88

FIG. 2dd

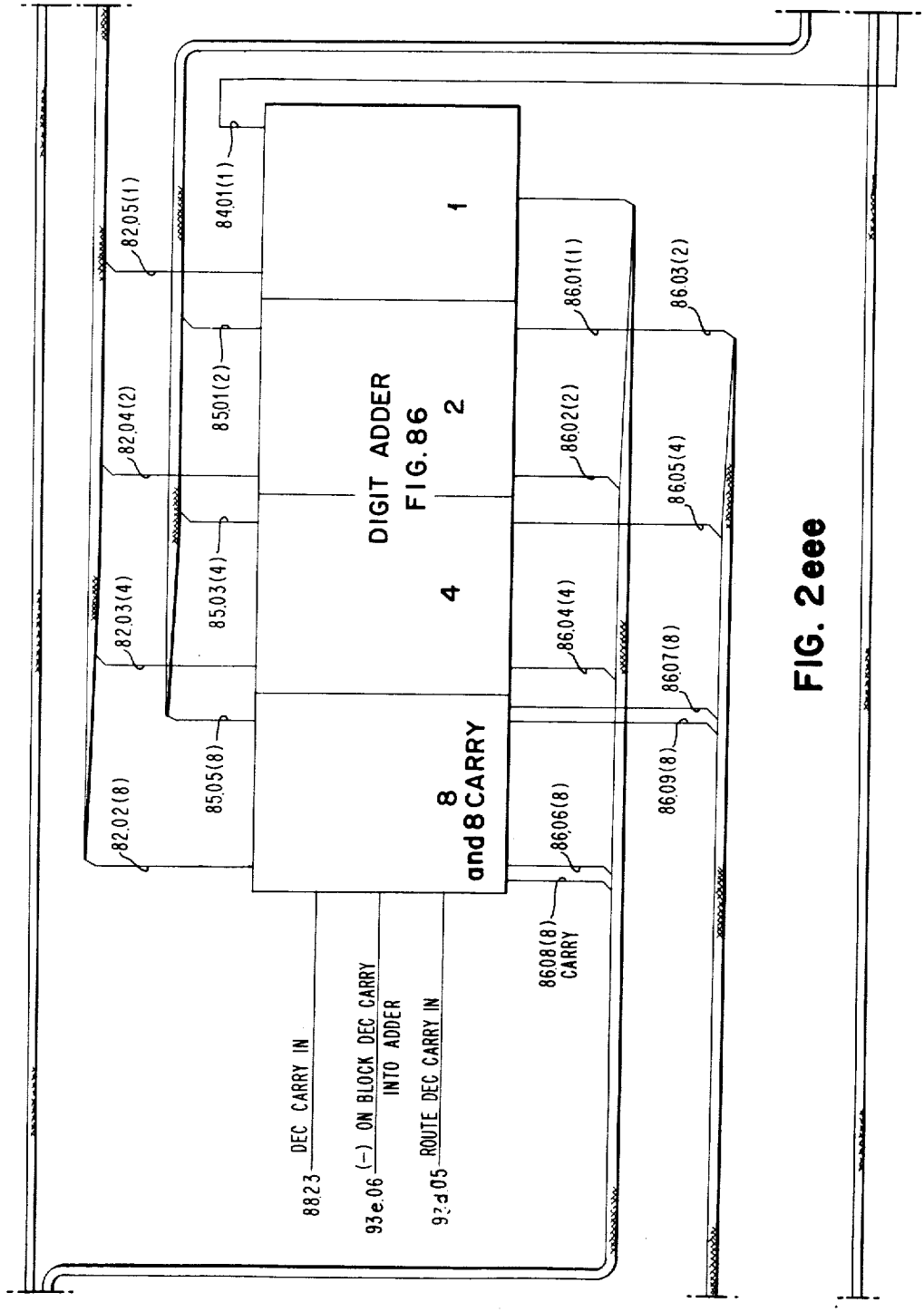
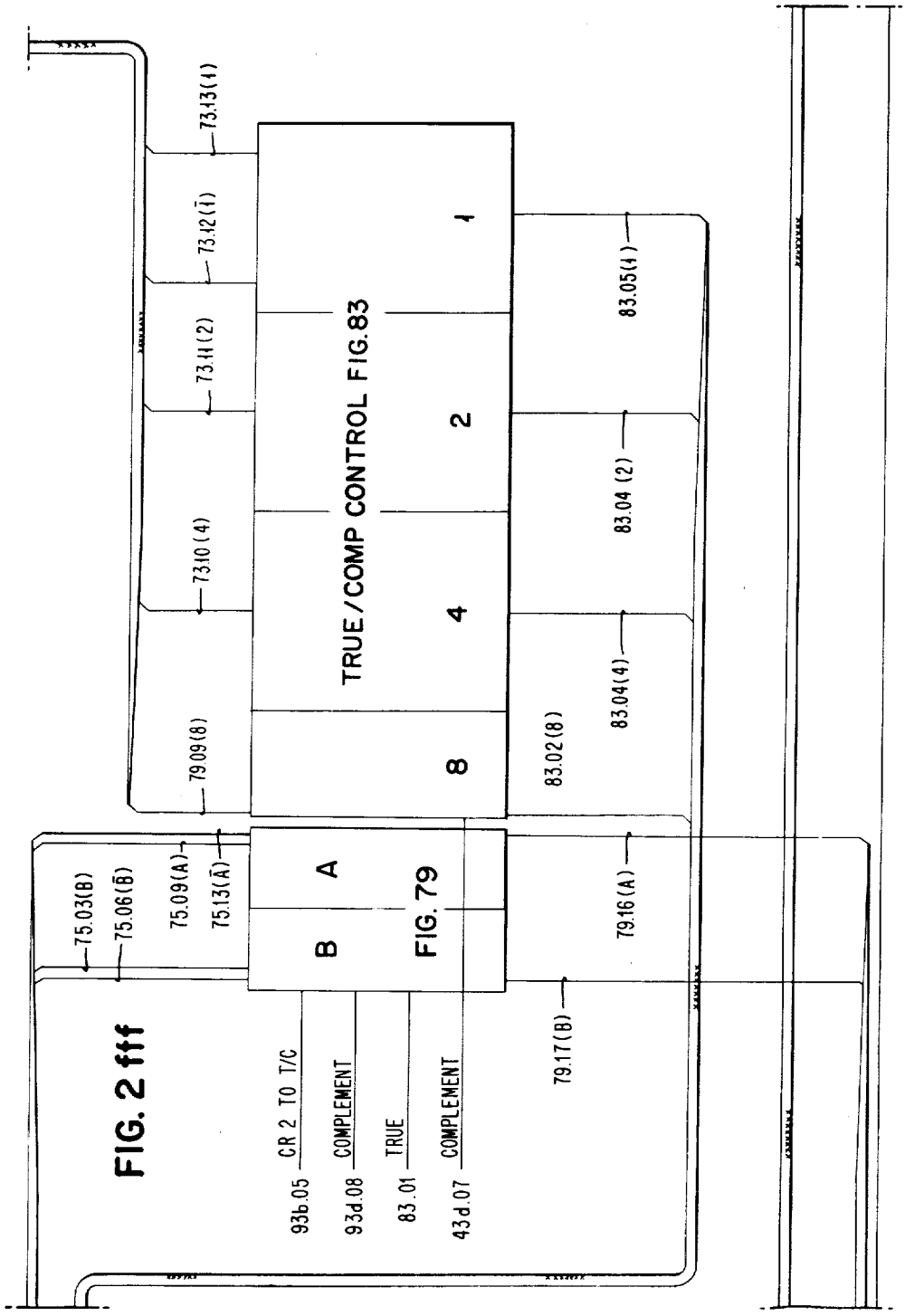

DIGIT ADDER
FIG. 86
1
2
4
8 and 8 CARRY
8401(1)
8205(1)
8501(2)
8204(2)
8503(4)
8203(4)
8505(8)
8202(8)
8601(1)
8603(2)
8602(2)
8605(4)
8604(4)
8607(8)
8609(8)
8606(8)
8608(8) CARRY
8823 DEC CARRY IN
93e.06 (-) ON BLOCK DEC CARRY INTO ADDER
93d.05 ROUTE DEC CARRY IN

FIG. 2eee


73.13(1)
73.12(1)
73.11(2)
73.10(4)
79.09(8)
TRUE/COMP CONTROL FIG.83
1
2
4
8
83.05(1)
83.04(2)
83.04(4)
83.02(8)
75.03(B)
75.06(B)
75.09(A)
75.13(A)
A
B
FIG. 79
79.16(A)
79.17(B)
FIG. 2 fff
93b.05 CR 2 TO T/C
93d.08 COMPLEMENT
83.01 TRUE
43d.07 COMPLEMENT

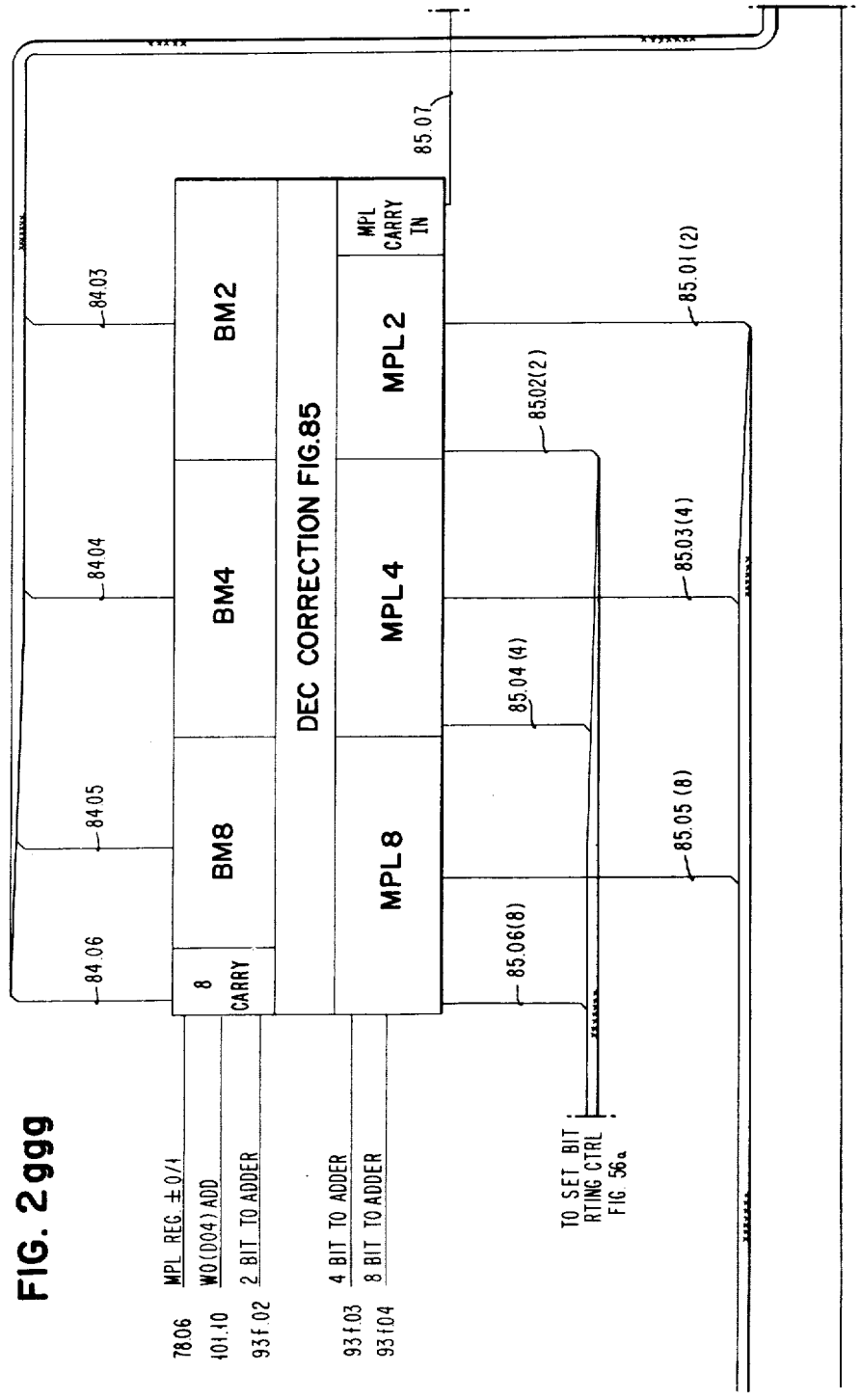

DEC CORRECTION FIG.85
BM2
BM4
BM8
8 CARRY
MPL 2
MPL 4
MPL 8
MPL CARRY IN
85.07
84.03
84.04
84.05
84.06
85.01(2)
85.02(2)
85.03(4)
85.04(4)
85.05(8)
85.06(8)
TO SET BIT RTING CTRL FIG 56a
7806 MPL REG ±0/1
101.10 W0(004) ADD
93f02 2 BIT TO ADDER
93f03 4 BIT TO ADDER
93f04 8 BIT TO ADDER

FIG. 2ggg

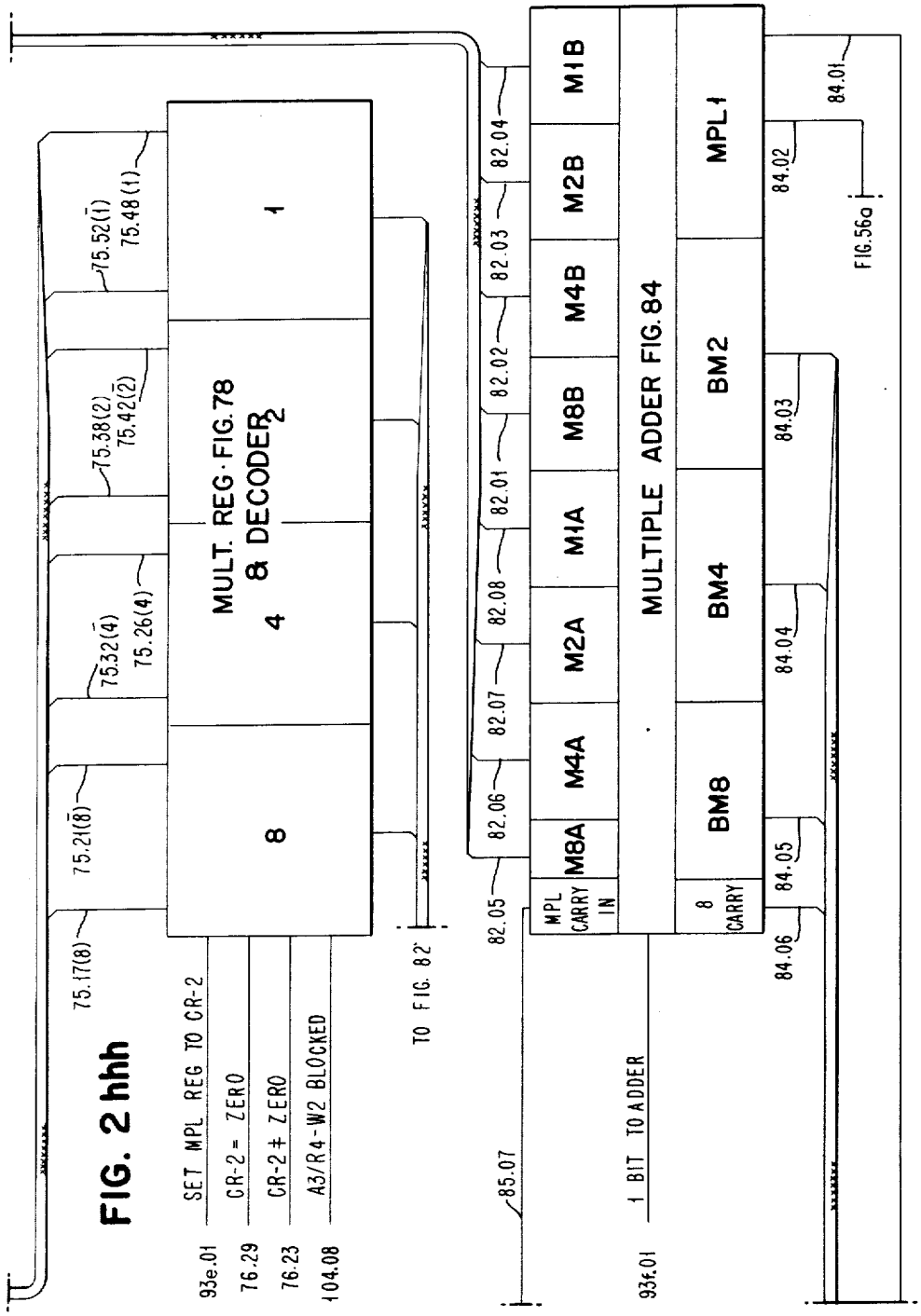

MULT. REG. FIG. 78
& DECODER
4
2
1
8
75.17(8)
75.21(8̄)
75.32(4̄)
75.26(4)
75.38(2)
75.42(2̄)
75.52(1̄)
75.48(1)
SET MPL REG TO CR-2
CR-2 = ZERO
CR-2 ≠ ZERO
A3/R4-W2 BLOCKED
93e.01
76.29
76.23
104.08
TO FIG. 82
82.05
82.06
82.07
82.08
82.01
82.02
82.03
82.04
MPL CARRY IN
M8A
M4A
M2A
M1A
M8B
M4B
M2B
M1B
MULTIPLE ADDER FIG. 84
8 CARRY
BM8
BM4
BM2
MPL 1
84.01
84.02
84.03
84.04
84.05
84.06
FIG. 56a
85.07
1 BIT TO ADDER
93f.01

FIG. 2 hhh

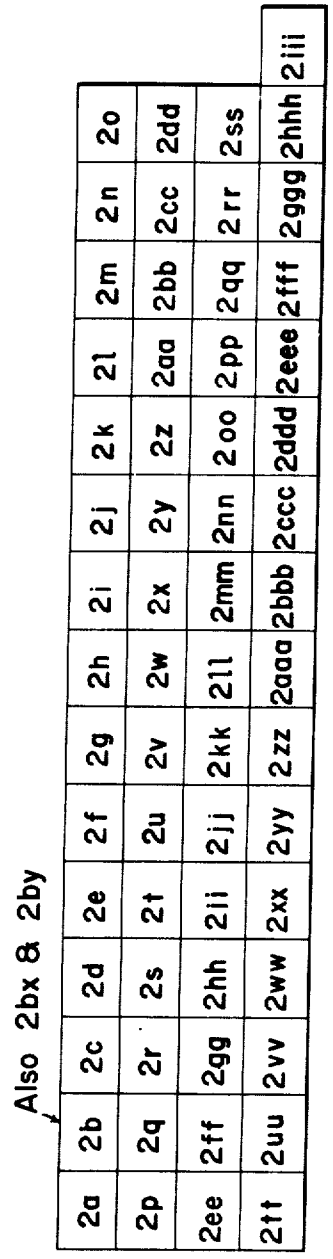

Also 2bx & 2by
2a 2b 2c 2d 2e 2f 2g 2h 2i 2j 2k 2l 2m 2n 2o
2p 2q 2r 2s 2t 2u 2v 2w 2x 2y 2z 2aa 2bb 2cc 2dd
2ee 2ff 2gg 2hh 2ii 2jj 2kk 2ll 2mm 2nn 2oo 2pp 2qq 2rr 2ss
2tt 2uu 2vv 2ww 2xx 2yy 2zz 2aaa 2bbb 2ccc 2ddd 2eee 2fff 2ggg 2hhh 2iii

FIG. 2iii

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FIG. 3a MEM. 4 X 10 DECODER 1000 ORDER

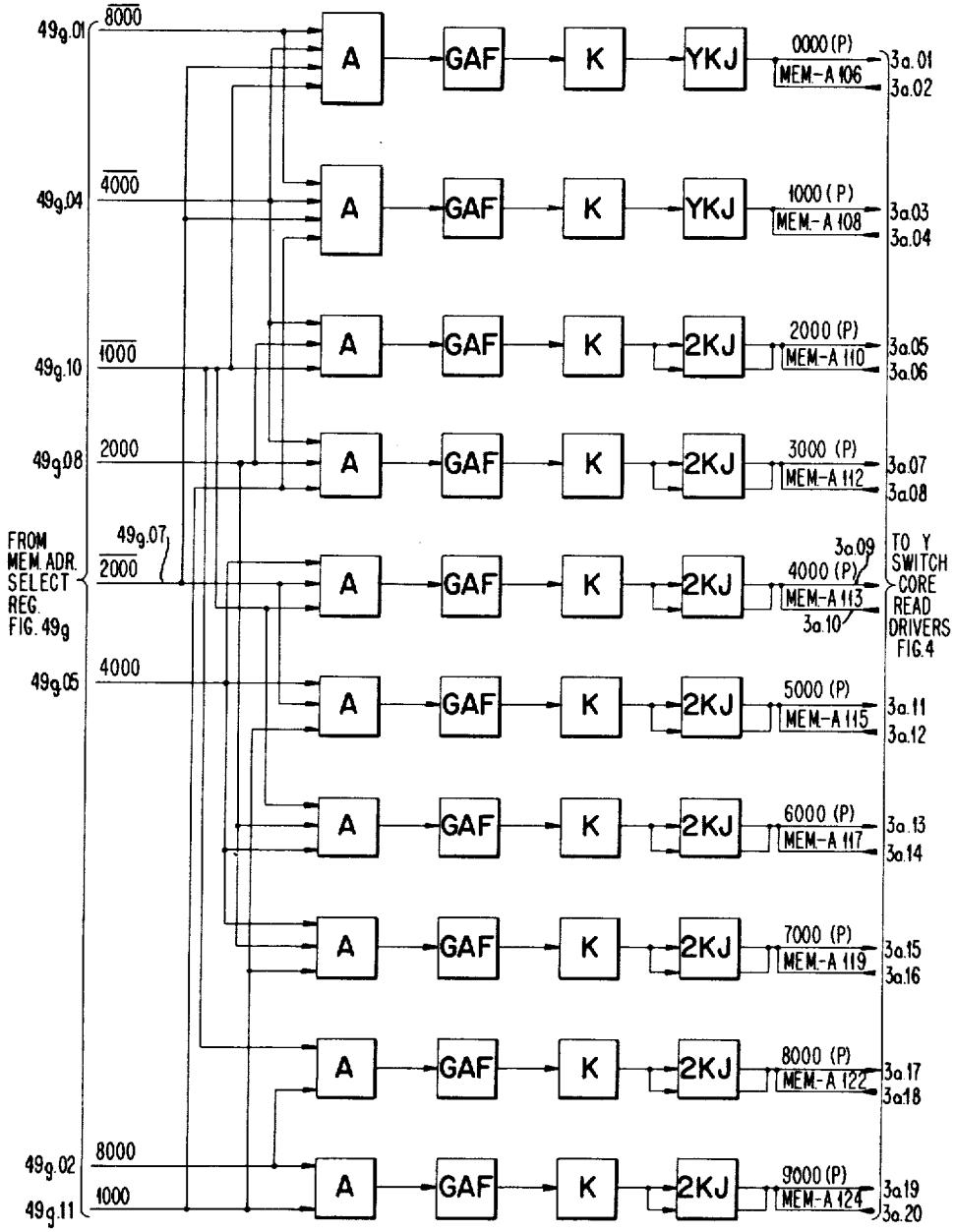


FIG. 3b

MEM. 4X10 DECODER

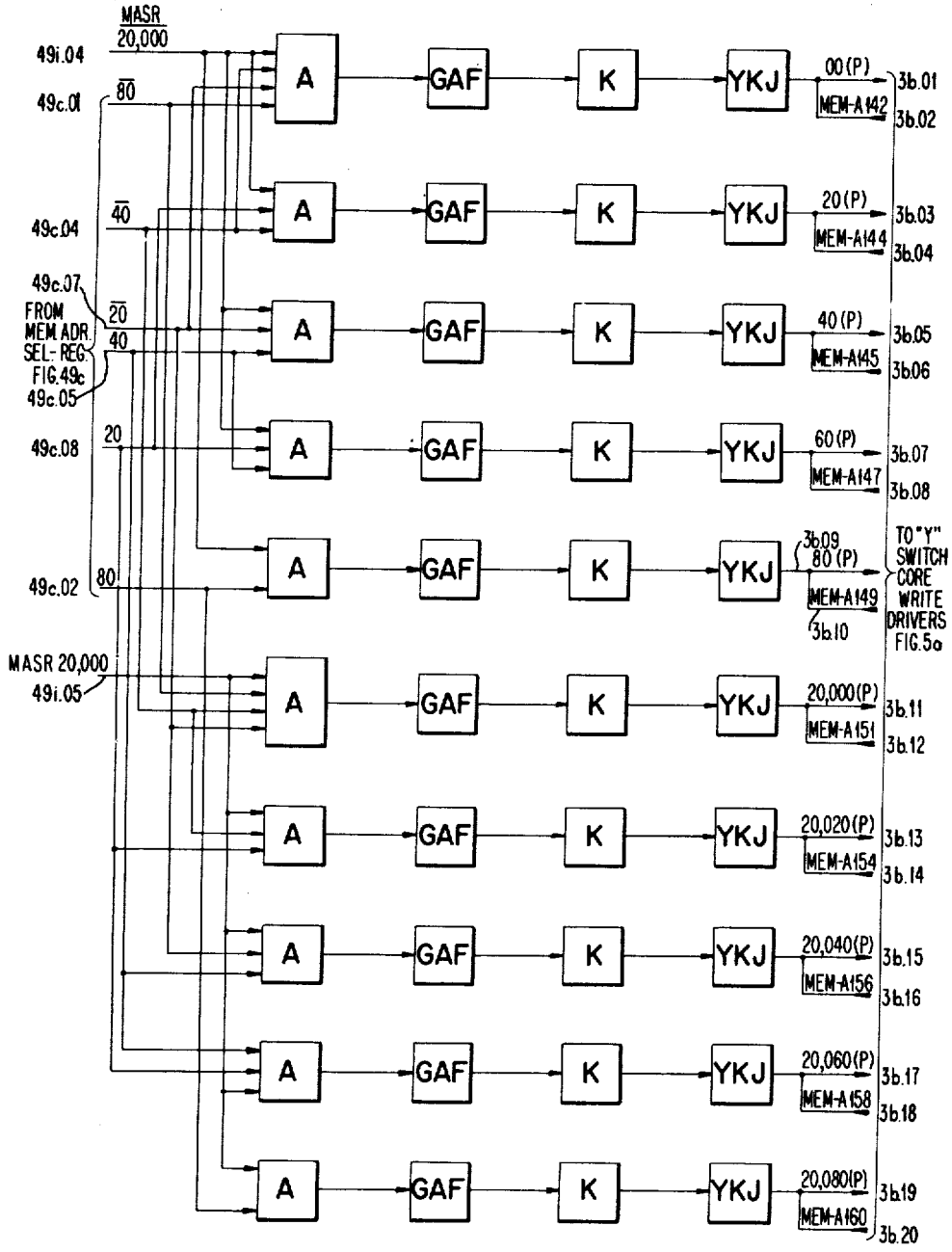
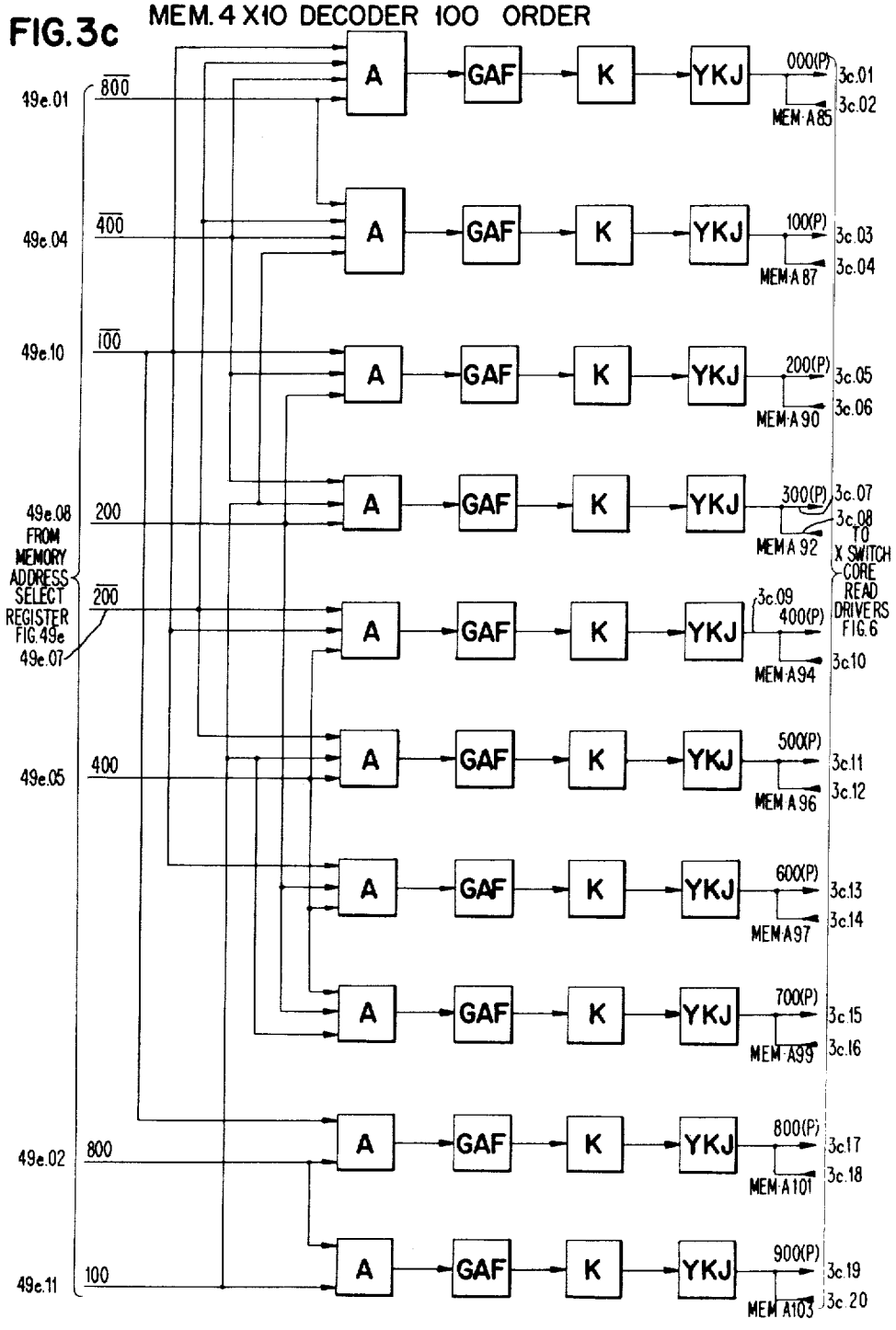
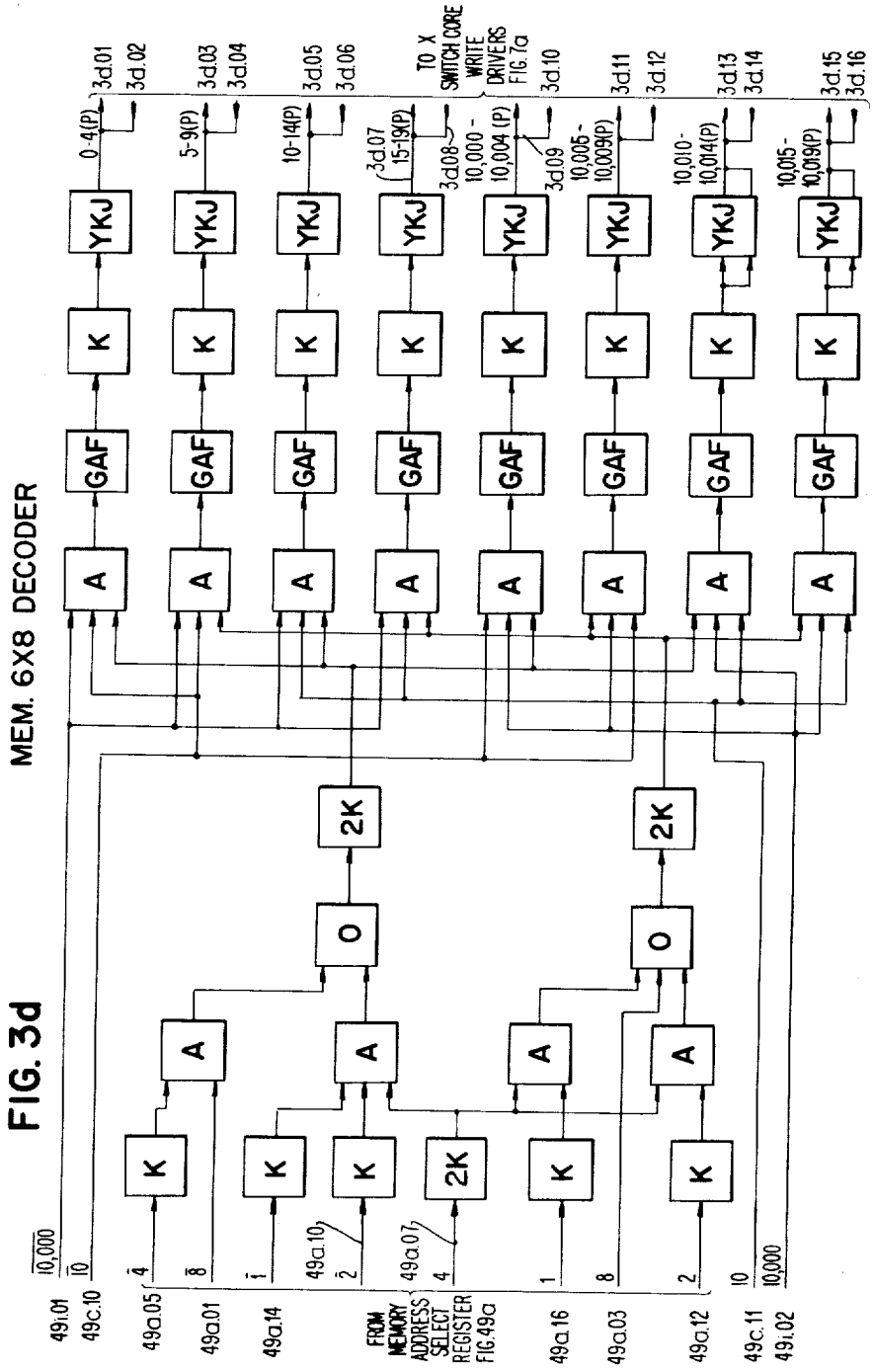


FIG. 3c


MEM. 4 X 10 DECODER 100 ORDER
49e.01
800
49e.04
400
49e.10
100
49e.08
200
FROM MEMORY ADDRESS SELECT REGISTER FIG. 49e
49e.07
200
49e.05
400
49e.02
800
49e.11
100
A
GAF
K
YKJ
000(P)
MEM A85
3c.01
3c.02
100(P)
MEM A87
3c.03
3c.04
200(P)
MEM A90
3c.05
3c.06
300(P)
MEM A92
3c.07
3c.08
TO X SWITCH CORE READ DRIVERS FIG. 6
3c.09
400(P)
MEM A94
3c.10
500(P)
MEM A96
3c.11
3c.12
600(P)
MEM A97
3c.13
3c.14
700(P)
MEM A99
3c.15
3c.16
800(P)
MEM A101
3c.17
3c.18
900(P)
MEM A103
3c.19
3c.20

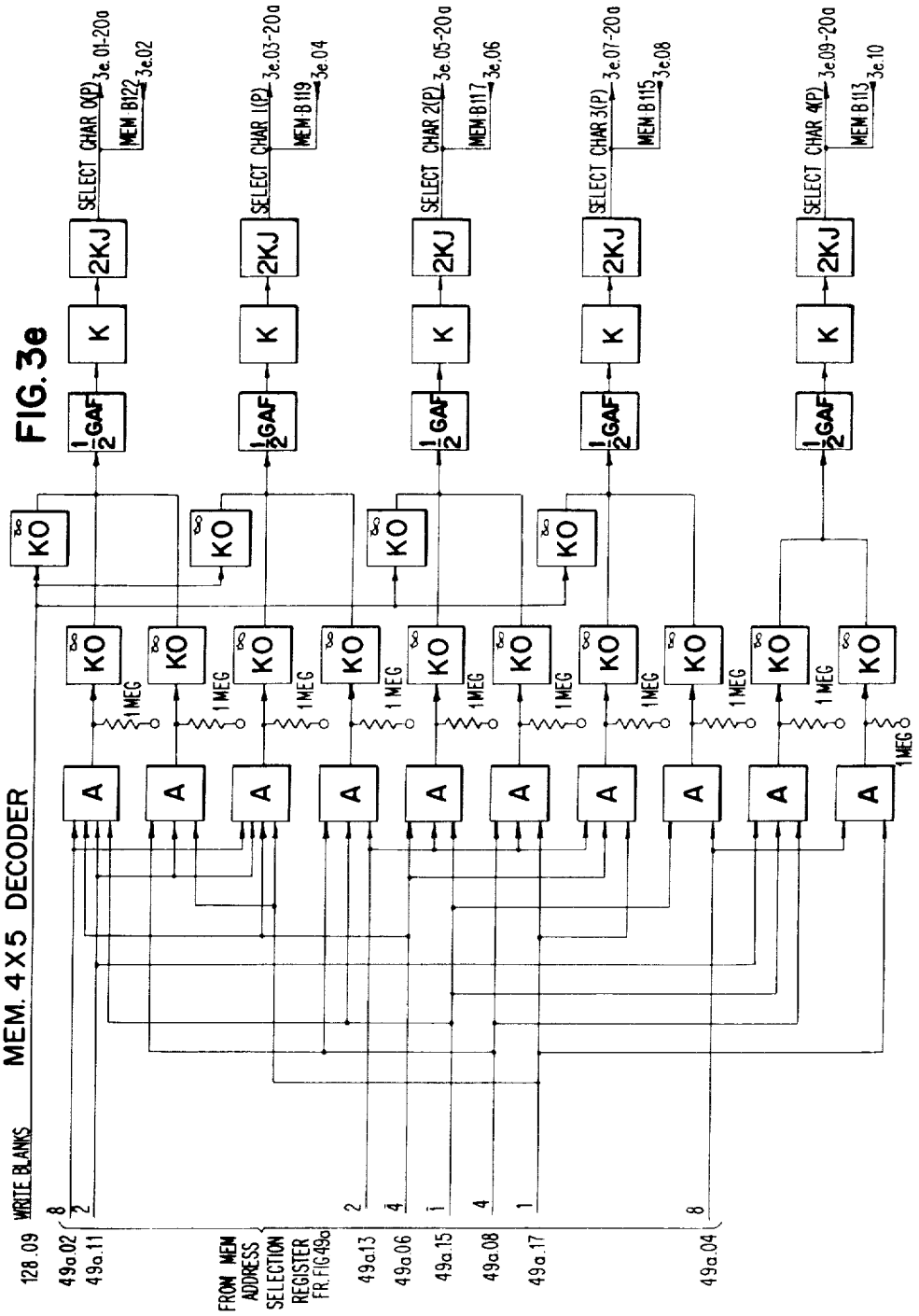

MEM. 6X8 DECODER
FIG. 3d
TO X SWITCH CORE WRITE DRIVERS FIG. 7a
FROM MEMORY ADDRESS SELECT REGISTER FIG. 49a
YKJ
K
GAF
A
2K
O
0-4(P)
5-9(P)
10-14(P)
15-19(P)
10,000 - 10,004 (P)
10,005 - 10,009(P)
10,010 - 10,014(P)
10,015 - 10,019(P)
3d.01
3d.02
3d.03
3d.04
3d.05
3d.06
3d.07
3d.08
3d.09
3d.10
3d.11
3d.12
3d.13
3d.14
3d.15
3d.16
49.01
49c.10
49a.05
49a.01
49a.14
49a.10
49a.07
49a.16
49a.03
49a.12
49c.11
49.02

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FIG. 3e



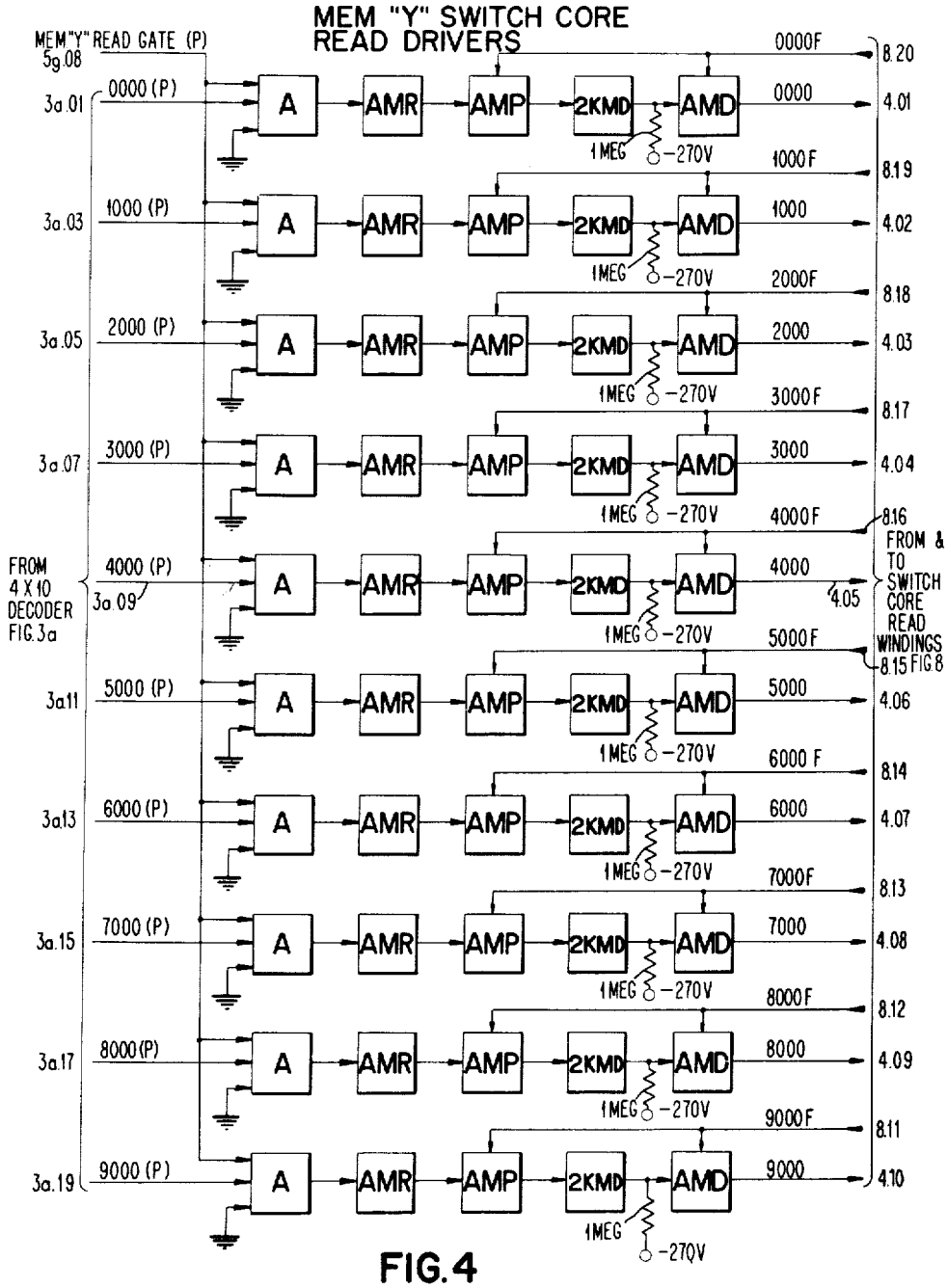
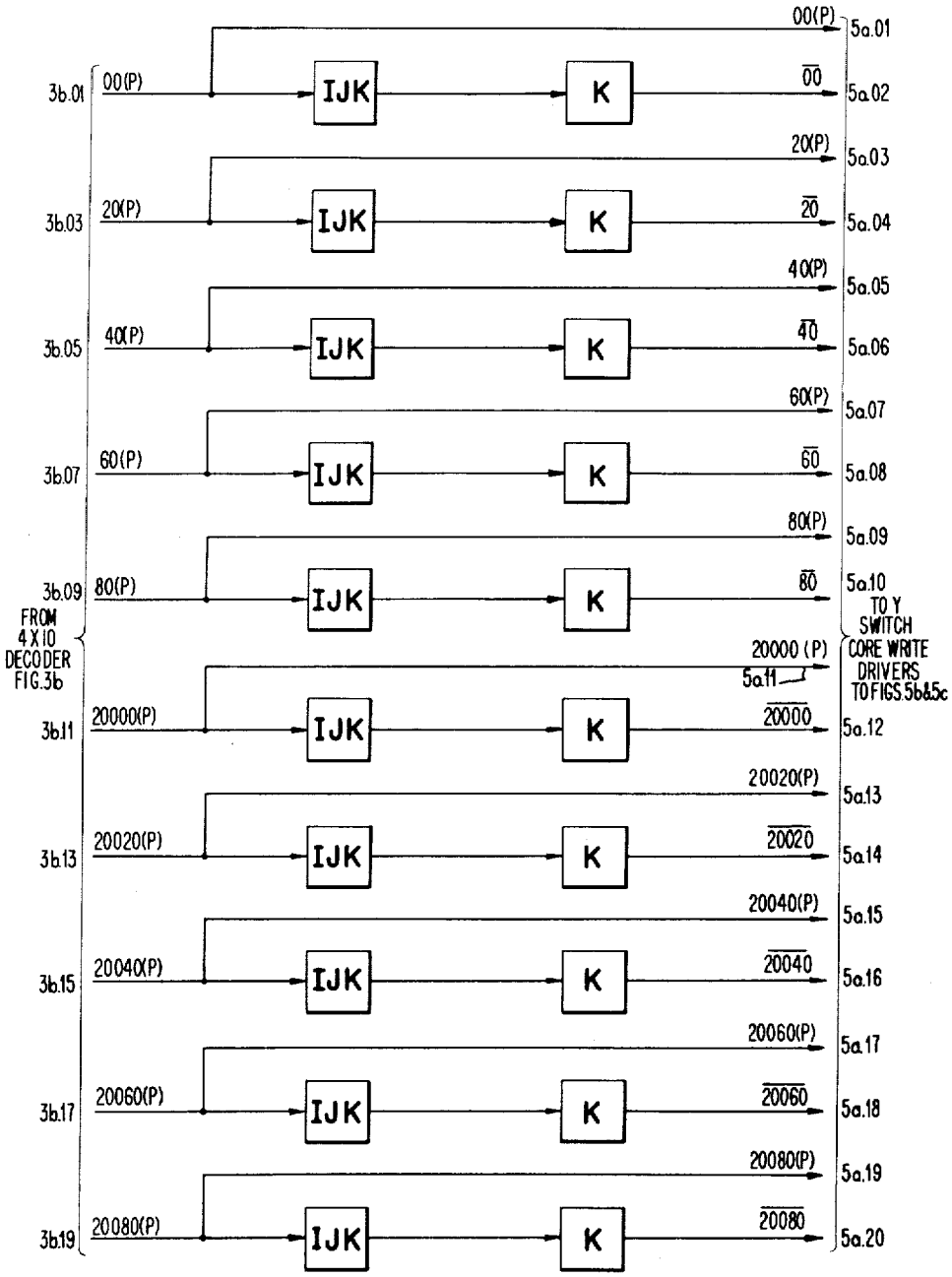

MEM "Y" SWITCH CORE READ DRIVERS
MEM "Y" READ GATE (P) 5g.08
0000 (P)
3a.01
1000 (P)
3a.03
2000 (P)
3a.05
3000 (P)
3a.07
4000 (P)
3a.09
5000 (P)
3a11
6000 (P)
3a13
7000 (P)
3a.15
8000 (P)
3a17
9000 (P)
3a.19
FROM 4 X 10 DECODER FIG. 3a
A
AMR
AMP
2KMD
AMD
1MEG
-270V
0000F
8.20
0000
4.01
1000F
8.19
1000
4.02
2000F
8.18
2000
4.03
3000F
8.17
3000
4.04
4000F
8.16
4000
4.05
5000F
5000
4.06
6000F
8.14
6000
4.07
7000F
8.13
7000
4.08
8000F
8.12
8000
4.09
9000F
8.11
9000
4.10
FROM & TO SWITCH CORE READ WINDINGS 8.15 FIG.8

FIG. 4

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FIG.5a

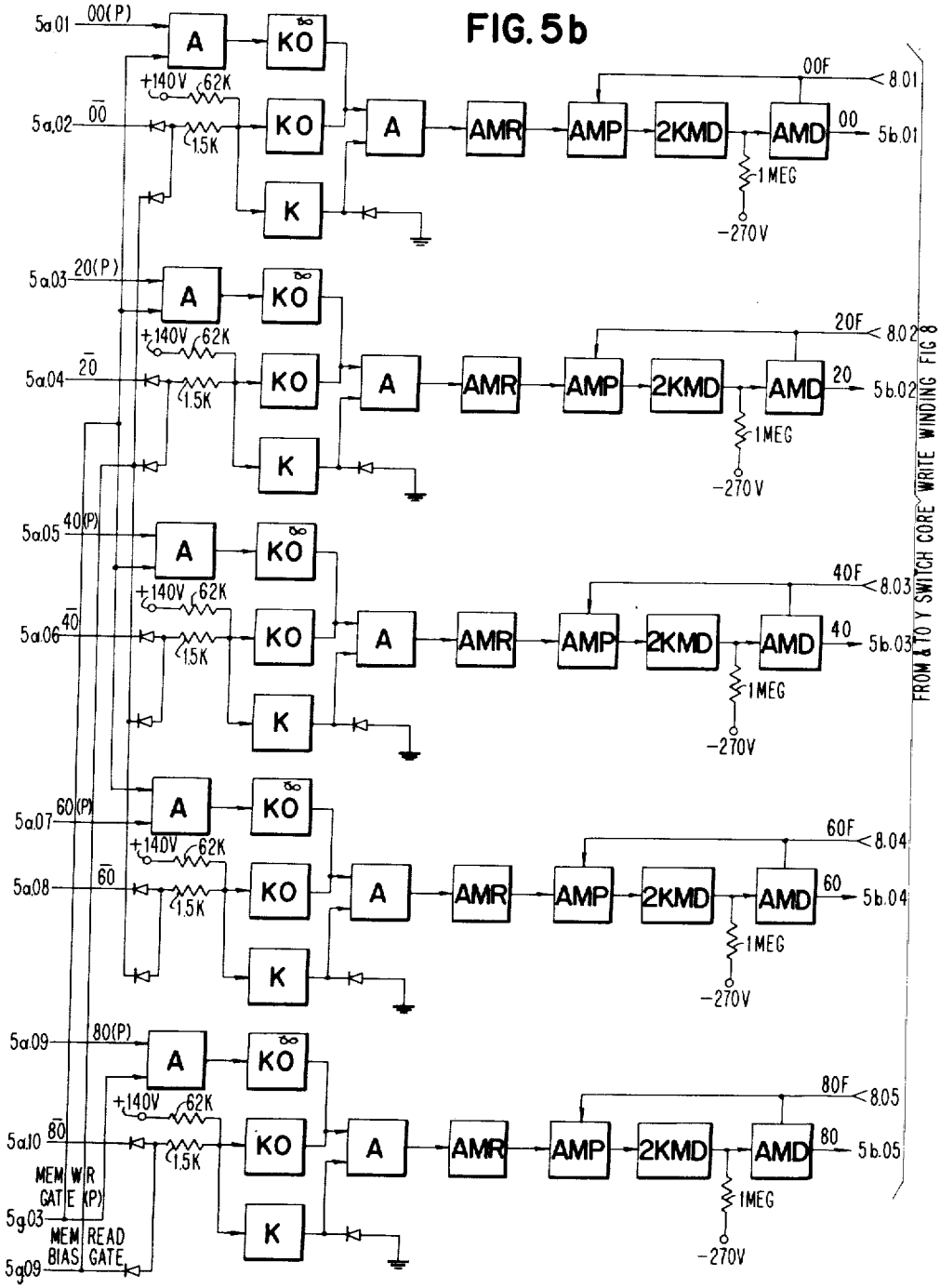
4 X 10 DECODER OUTPUT INVERTERS



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MEM Y SWITCH CORE WRITE DRIVERS

FIG. 5b



MEM Y SWITCH CORE WRITE DRIVERS

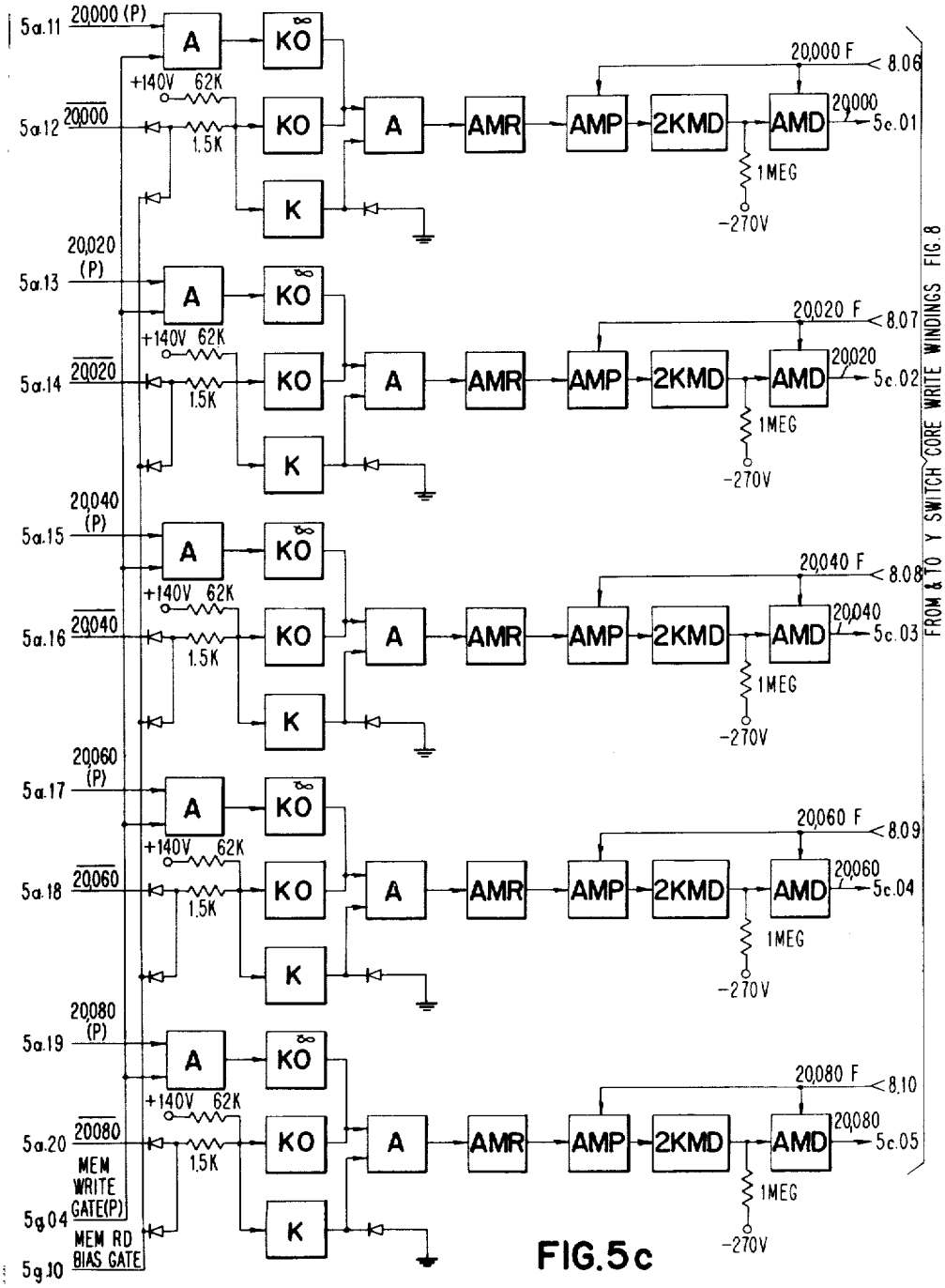
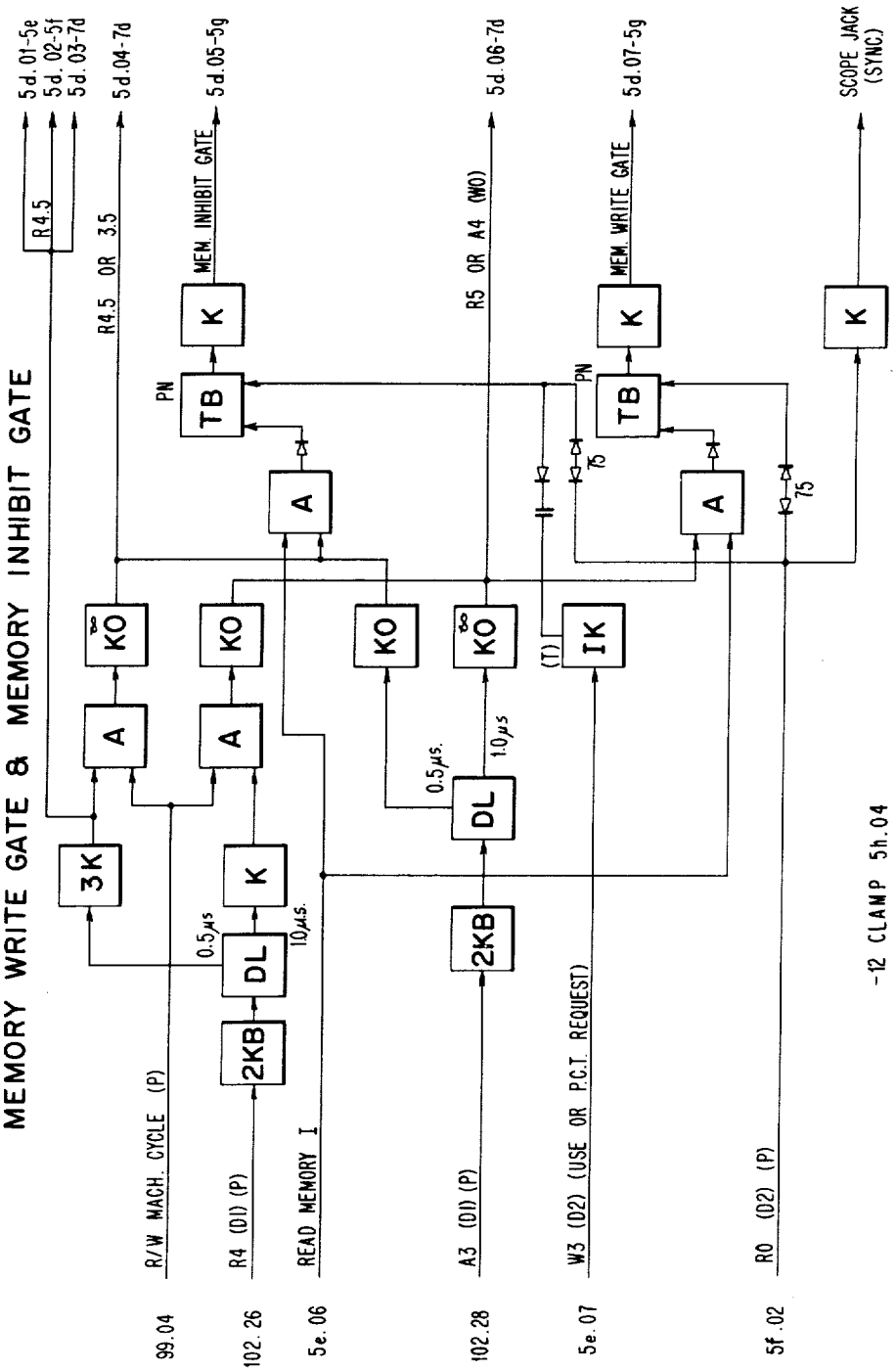
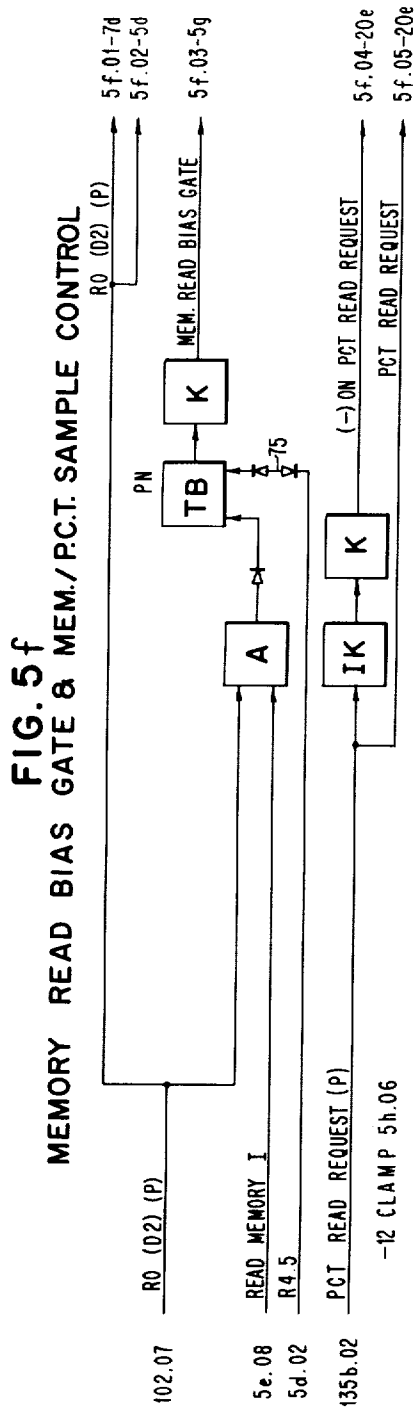


FIG. 5c

FIG. 5d
MEMORY WRITE GATE & MEMORY INHIBIT GATE




MEMORY READ BIAS GATE & MEM./P.C.T. SAMPLE CONTROL
RO (D2) (P)
5f.01-7d
5f.02-5d
5f.03-5g
MEM. READ BIAS GATE
PN
TB
K
75
A
(-) ON PCT READ REQUEST
5f.04-20e
PCT READ REQUEST
5f.05-20e
IK
K
RO (D2) (P)
READ MEMORY I
R4.5
PCT READ REQUEST (P)
-12 CLAMP 5h.06
102.07
5e.08
5d.02
135b.02

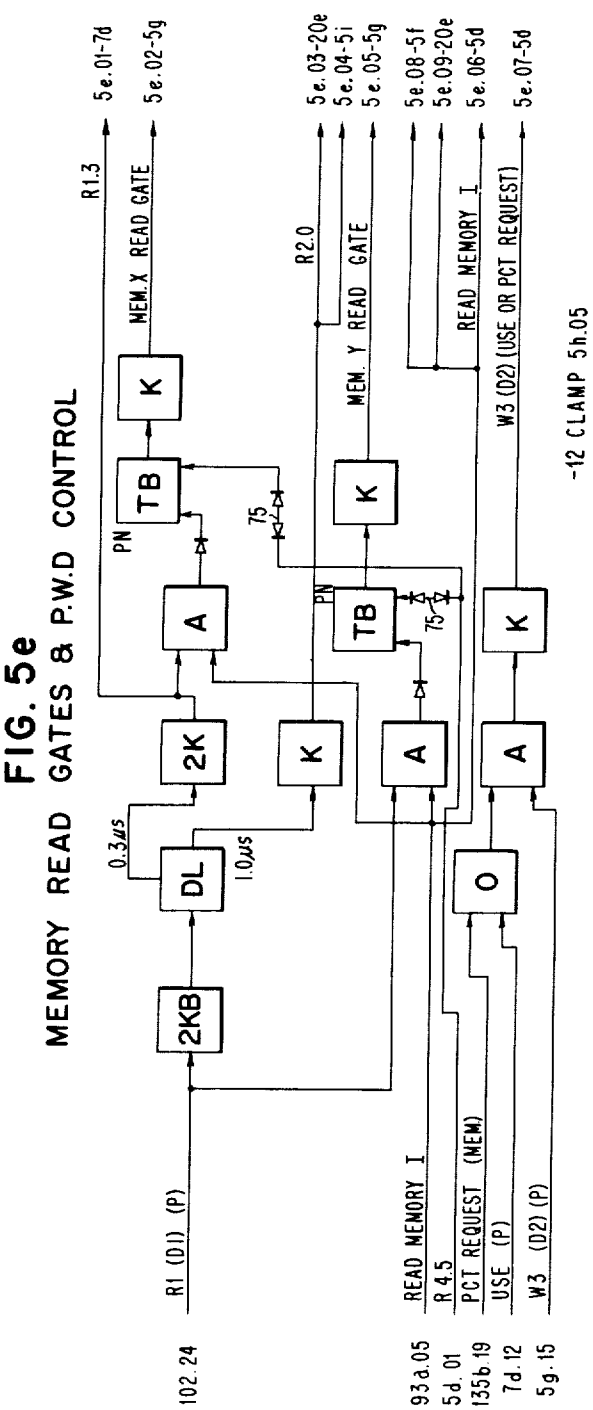
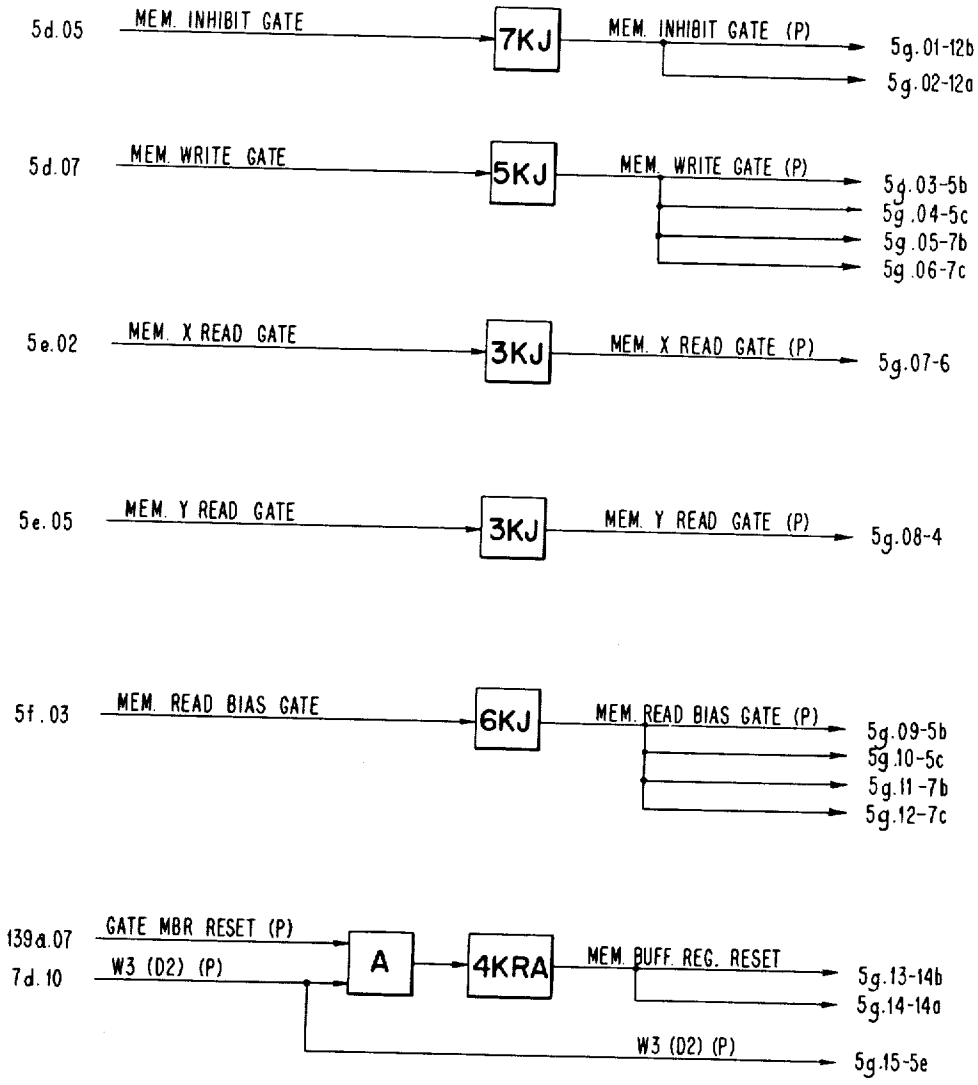

MEMORY READ GATES & P.W.D CONTROL
R1.3
5e.01-7d
5e.02-5g
MEM.X READ GATE
PN
TB
K
75
A
2K
0.3μs
DL
1.0μs
2KB
R1 (D1) (P)
R2.0
5e.03-20e
5e.04-5i
5e.05-5g
MEM. Y READ GATE
5e.08-5f
5e.09-20e
5e.06-5d
READ MEMORY I
5e.07-5d
W3 (D2) (USE OR PCT REQUEST)
O
READ MEMORY I
R4.5
PCT REQUEST (MEM)
USE (P)
W3 (D2) (P)
-12 CLAMP 5h.05
102.24
93a.05
5d.01
135b.19
7d.12
5g.15

FIG. 5g

MEMORY GATE POWERING & M.B.R. RESET



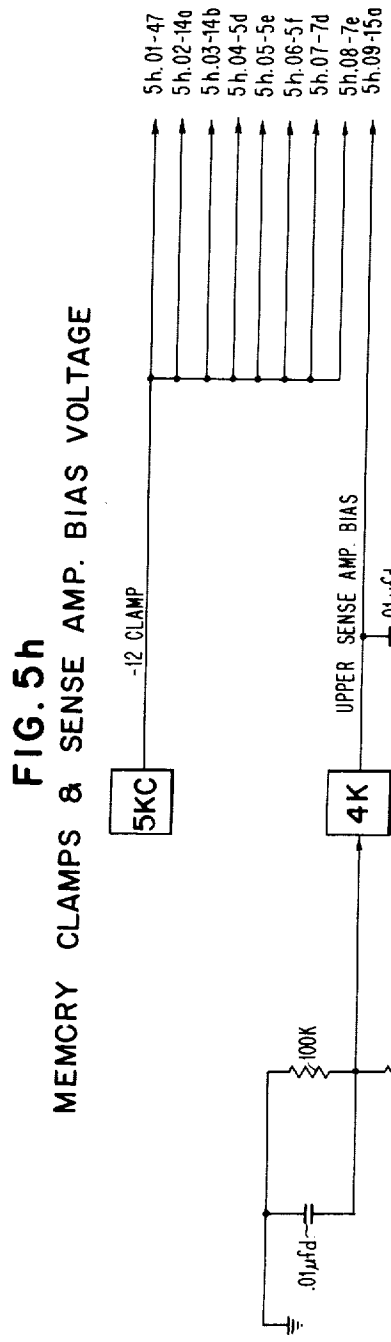


FIG. 5h
MEMCRY CLAMPS & SENSE AMP. BIAS VOLTAGE

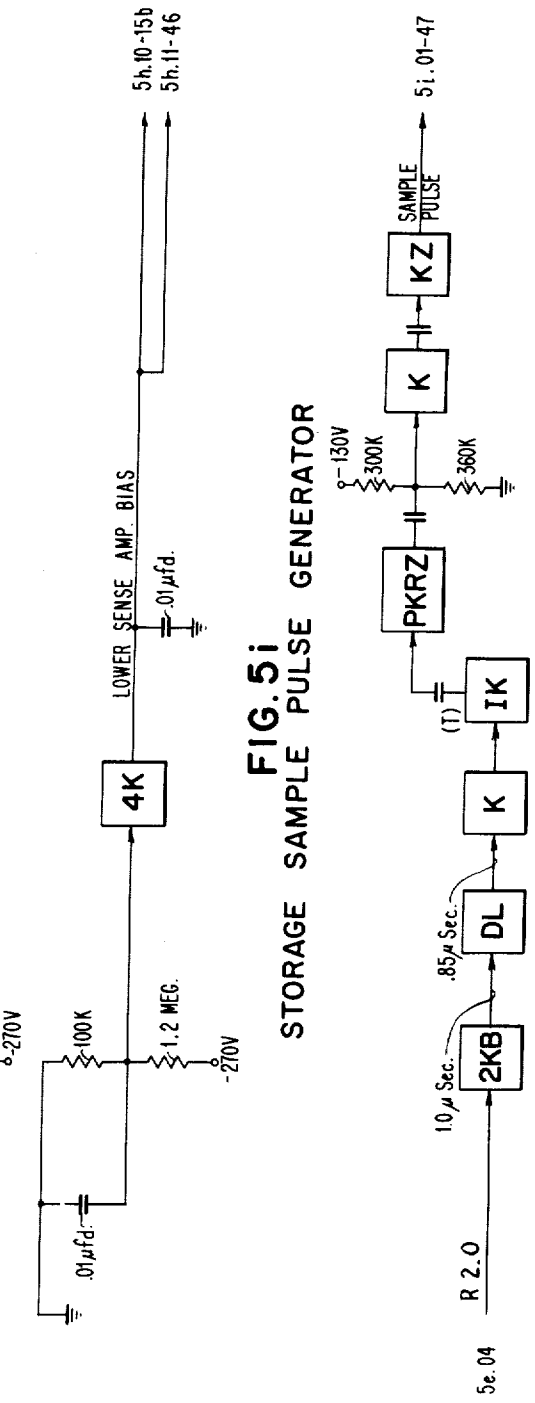


FIG. 5i
STORAGE SAMPLE PULSE GENERATOR

FIG. 6

MEM. X SWITCH CORE READ DRIVERS

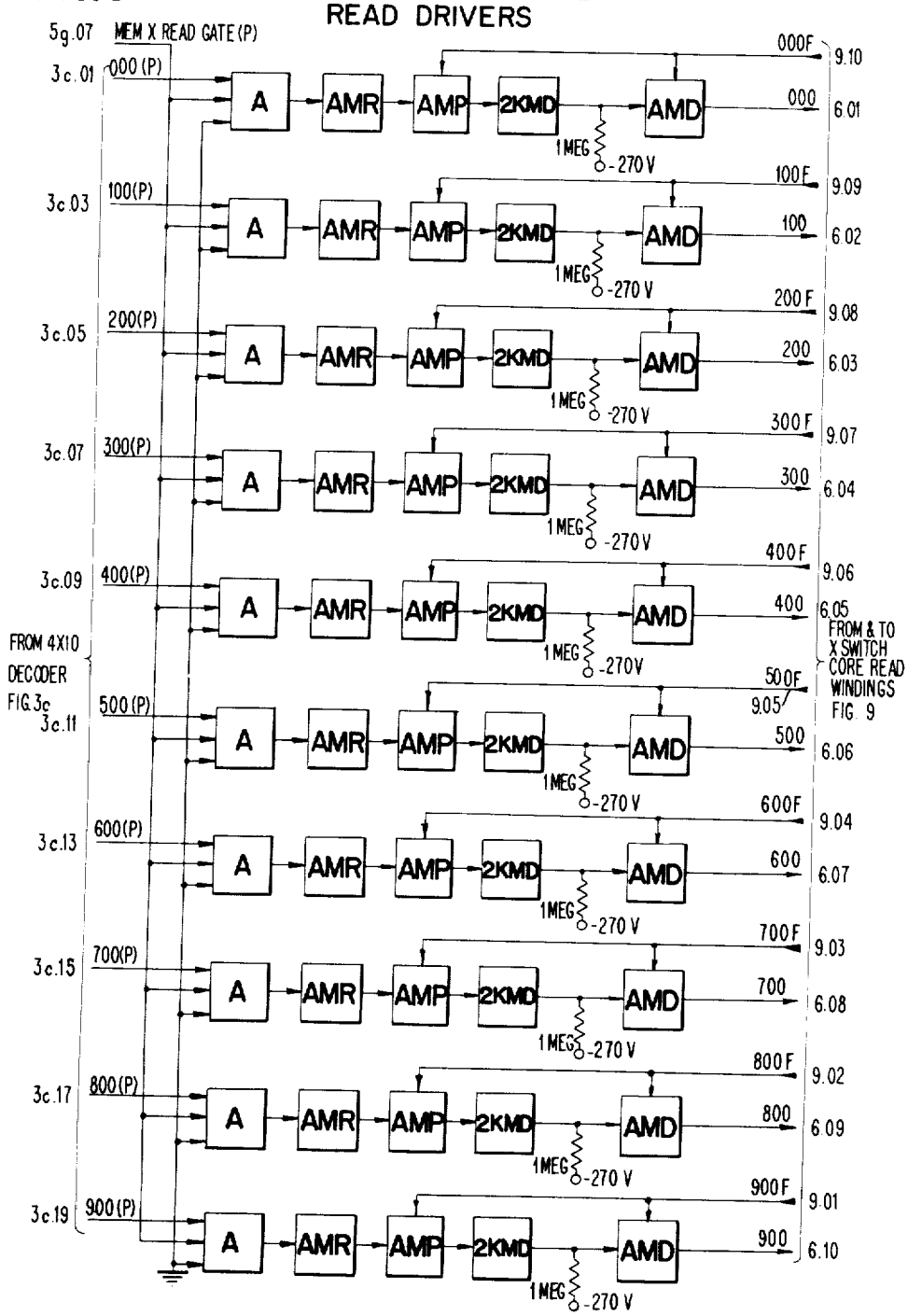
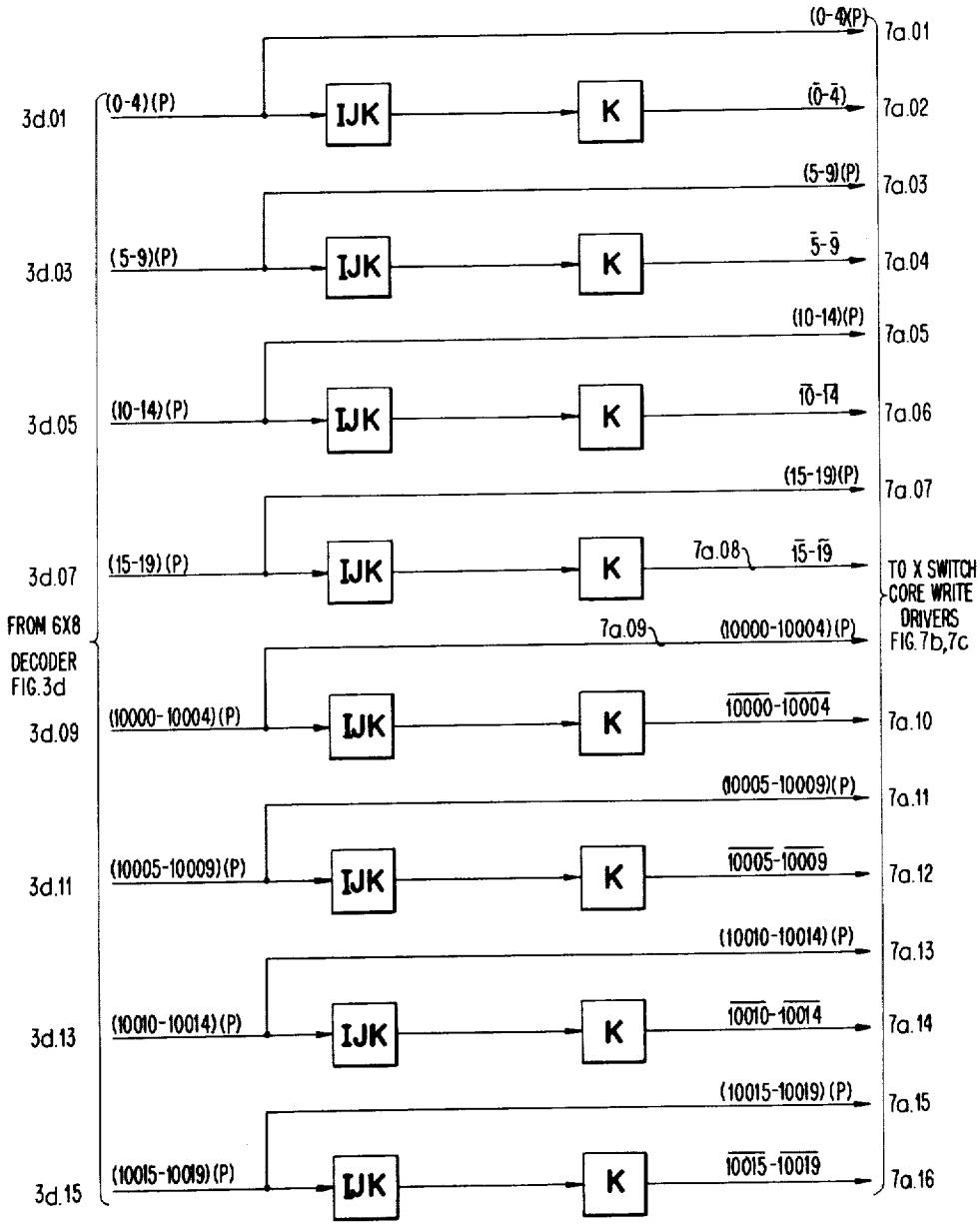


FIG. 7a

6 X 8 DECODER OUTPUT INVERTERS



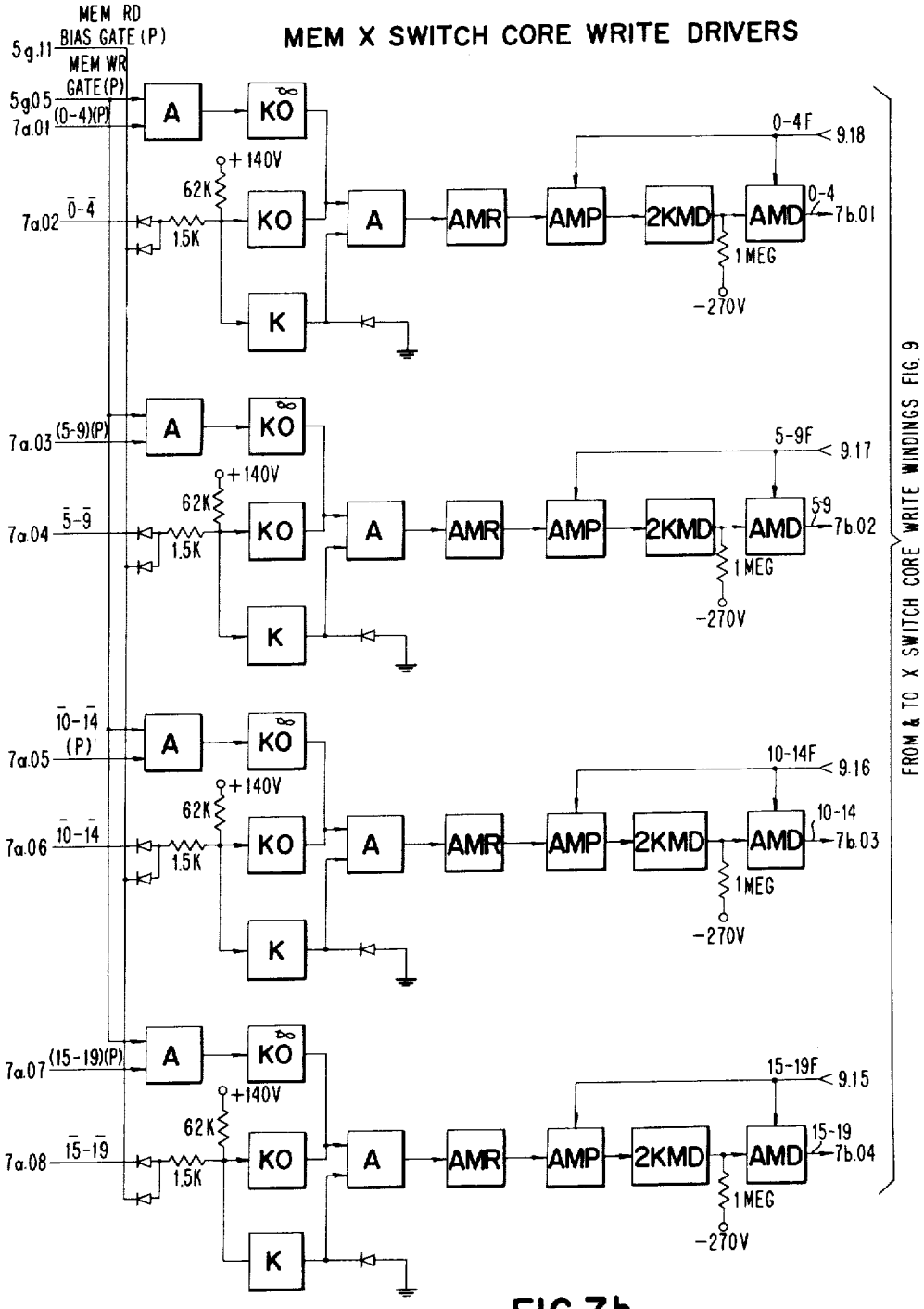

MEM X SWITCH CORE WRITE DRIVERS
MEM RD BIAS GATE (P)
5g.11
MEM WR GATE (P)
5g.05
7a.01
(0-4)(P)
A
KO
+140V
62K
1.5K
7a.02
0-4
K
AMR
AMP
2KMD
AMD
1 MEG
-270V
0-4F
9.18
0-4
7b.01
7a.03
(5-9)(P)
5-9F
9.17
7a.04
5-9
5-9
7b.02
10-14
(P)
7a.05
10-14F
9.16
7a.06
10-14
10-14
7b.03
7a.07
(15-19)(P)
15-19F
9.15
7a.08
15-19
15-19
7b.04
FROM & TO X SWITCH CORE WRITE WINDINGS FIG. 9

FIG. 7b

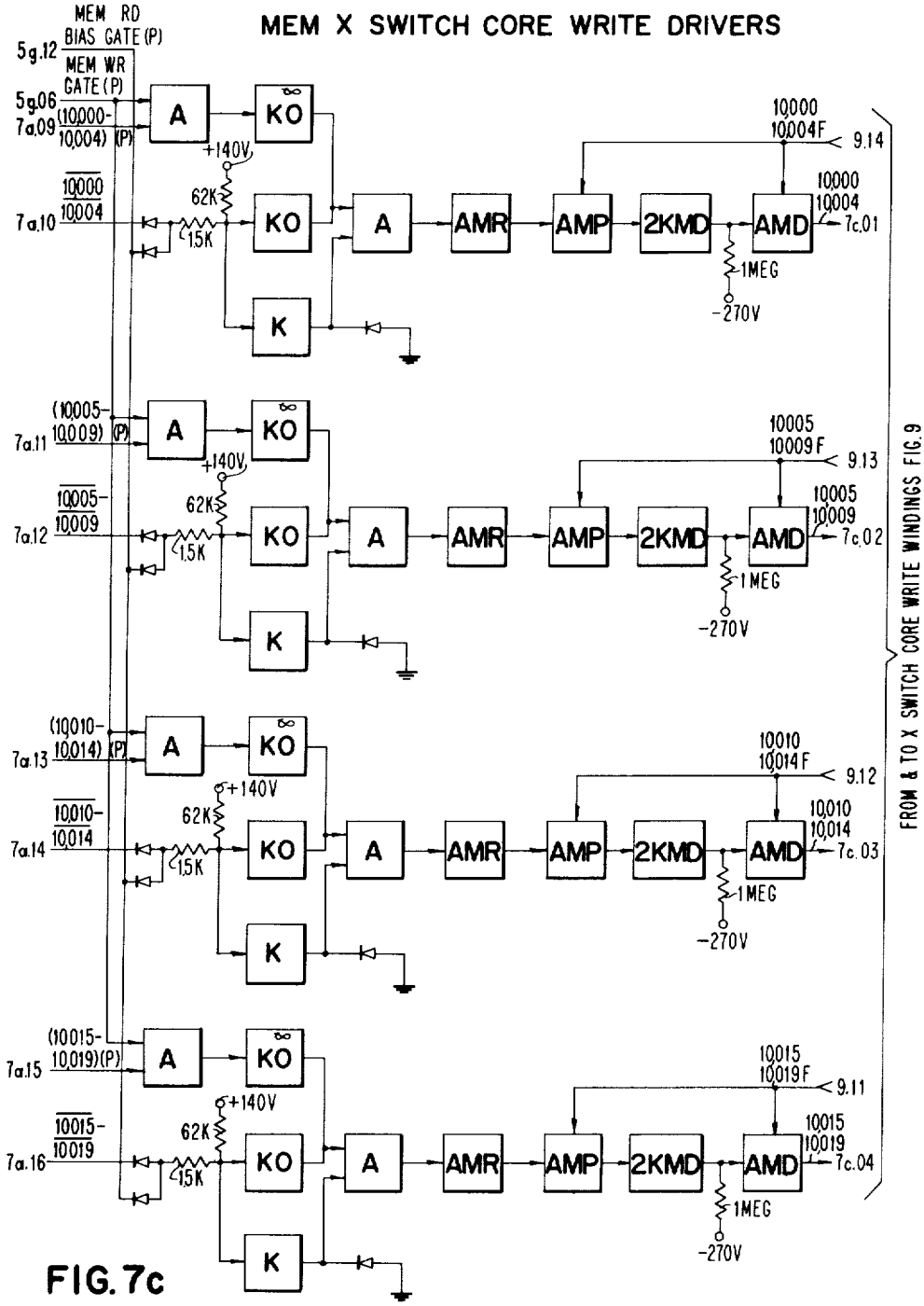

MEM X SWITCH CORE WRITE DRIVERS
MEM RD BIAS GATE (P)
MEM WR GATE (P)
5g.12
5g.06
7a.09
(10000-10004) (P)
10000 10004
7a.10
+140V
62K
1.5K
A
KO
K
AMR
AMP
2KMD
AMD
1MEG
-270V
10000 10004F
9.14
10000 10004
7c.01
(10005-10009) (P)
7a.11
10005-10009
7a.12
10005 10009F
9.13
10005 10009
7c.02
(10010-10014) (P)
7a.13
10010-10014
7a.14
10010 10014F
9.12
10010 10014
7c.03
(10015-10019) (P)
7a.15
10015-10019
7a.16
10015 10019F
9.11
10015 10019
7c.04
FROM & TO X SWITCH CORE WRITE WINDINGS FIG. 9

FIG. 7c

FIG. 7d

STOR. READ BIAS GT, READ GT., INHIBIT GT., WRITE GT. & BUFF REG. RESET

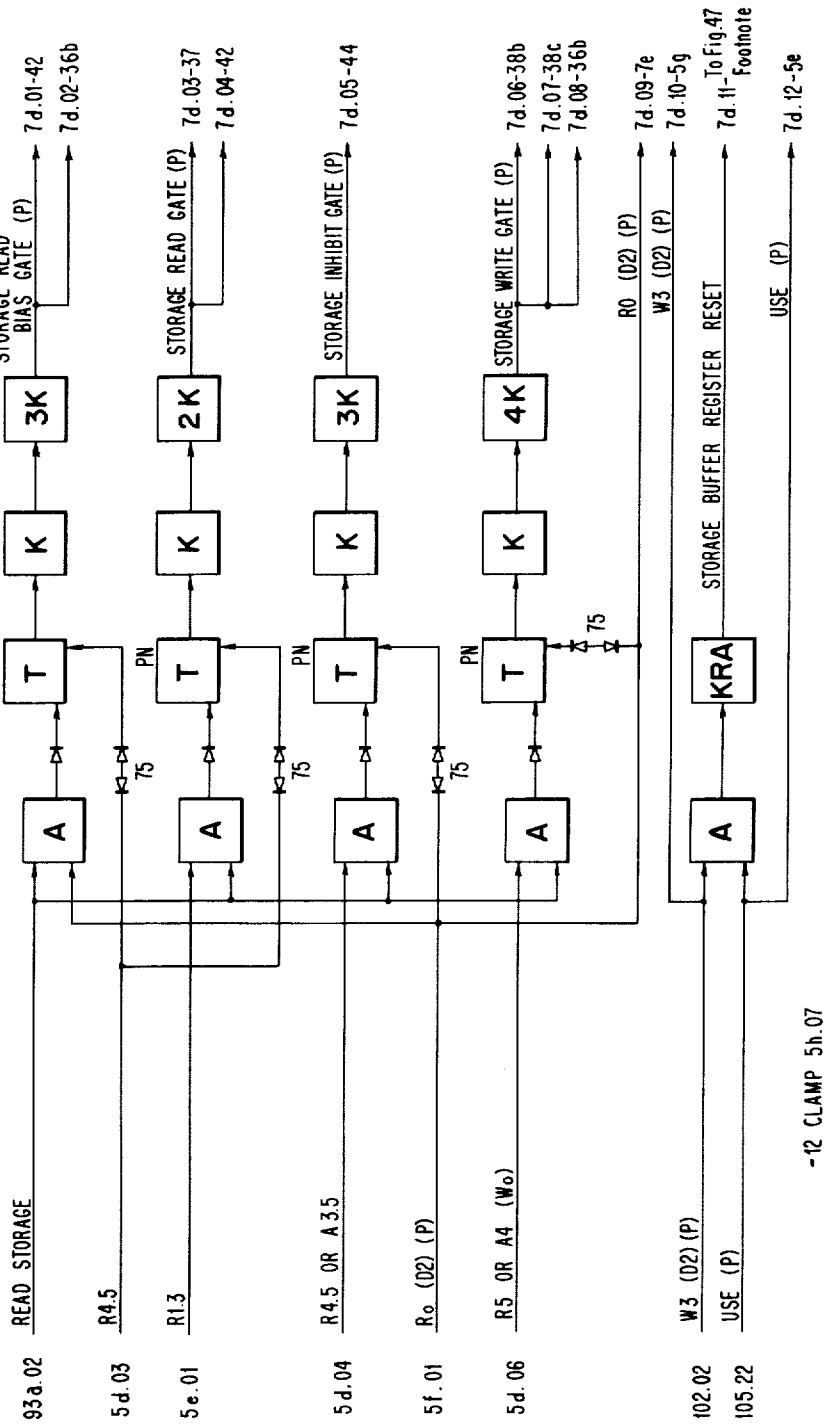
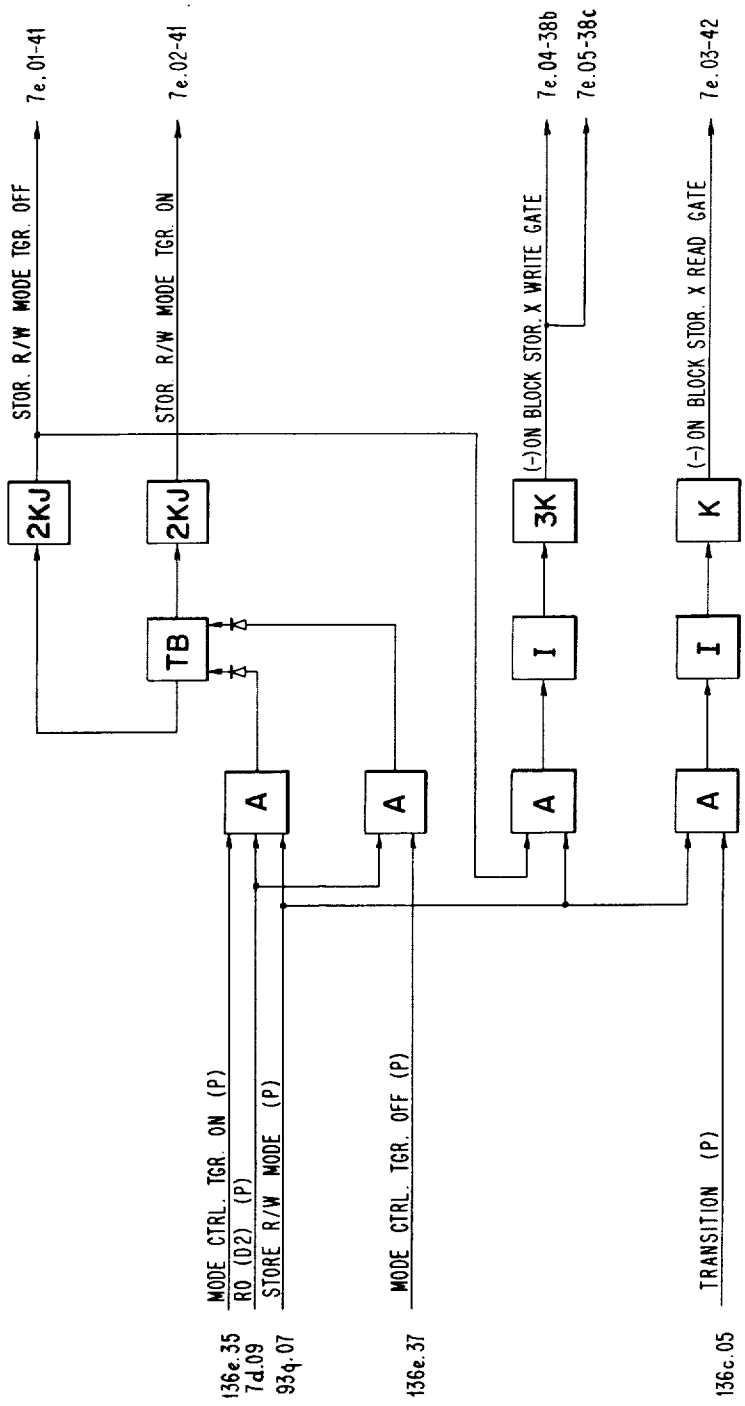


FIG. 7e
STORAGE R/W MODE CTRL.



-12 CLAMP 5h.08

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FIG. 8 Y SWITCH CORE MATRIX

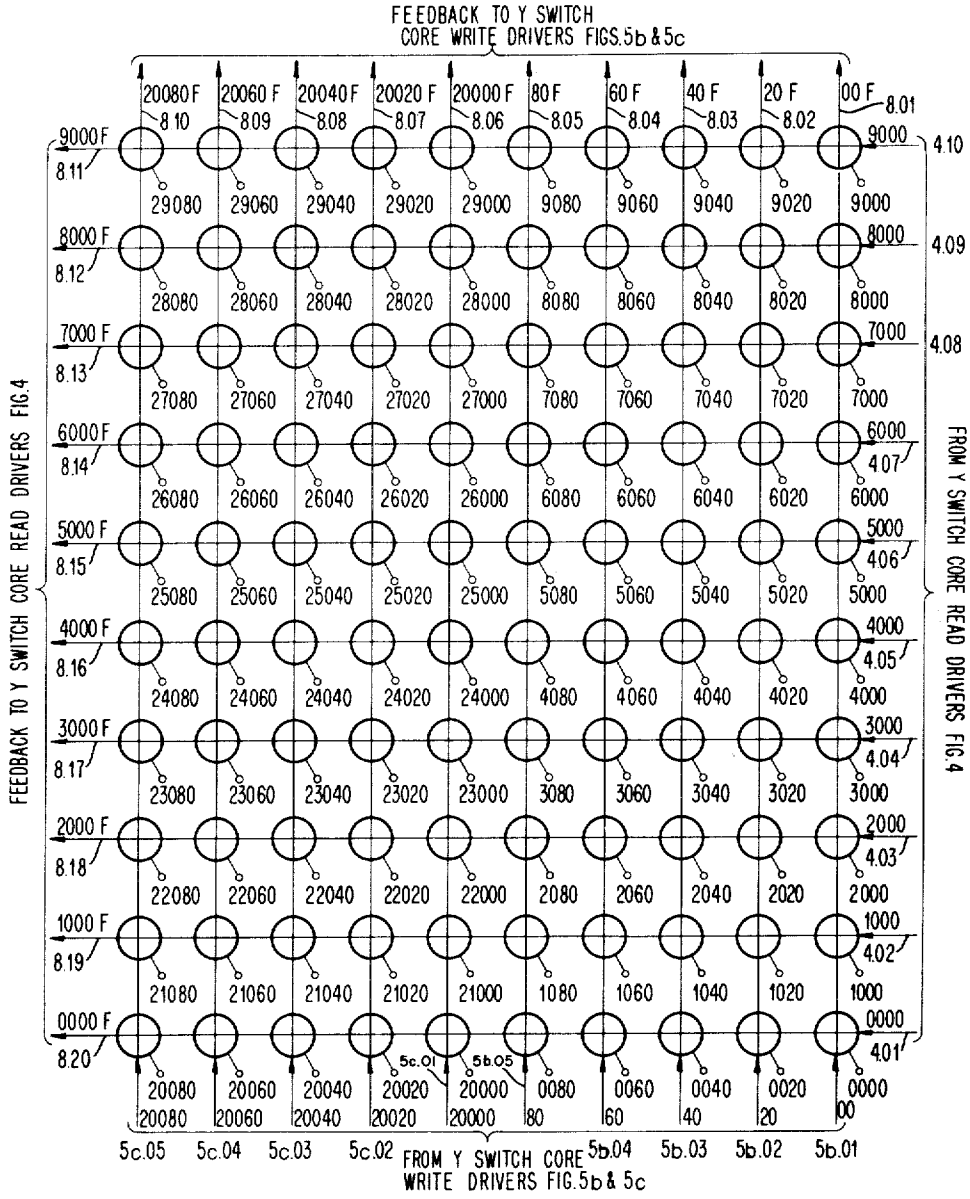


FIG.9 "X" SWITCH CORE MATRIX

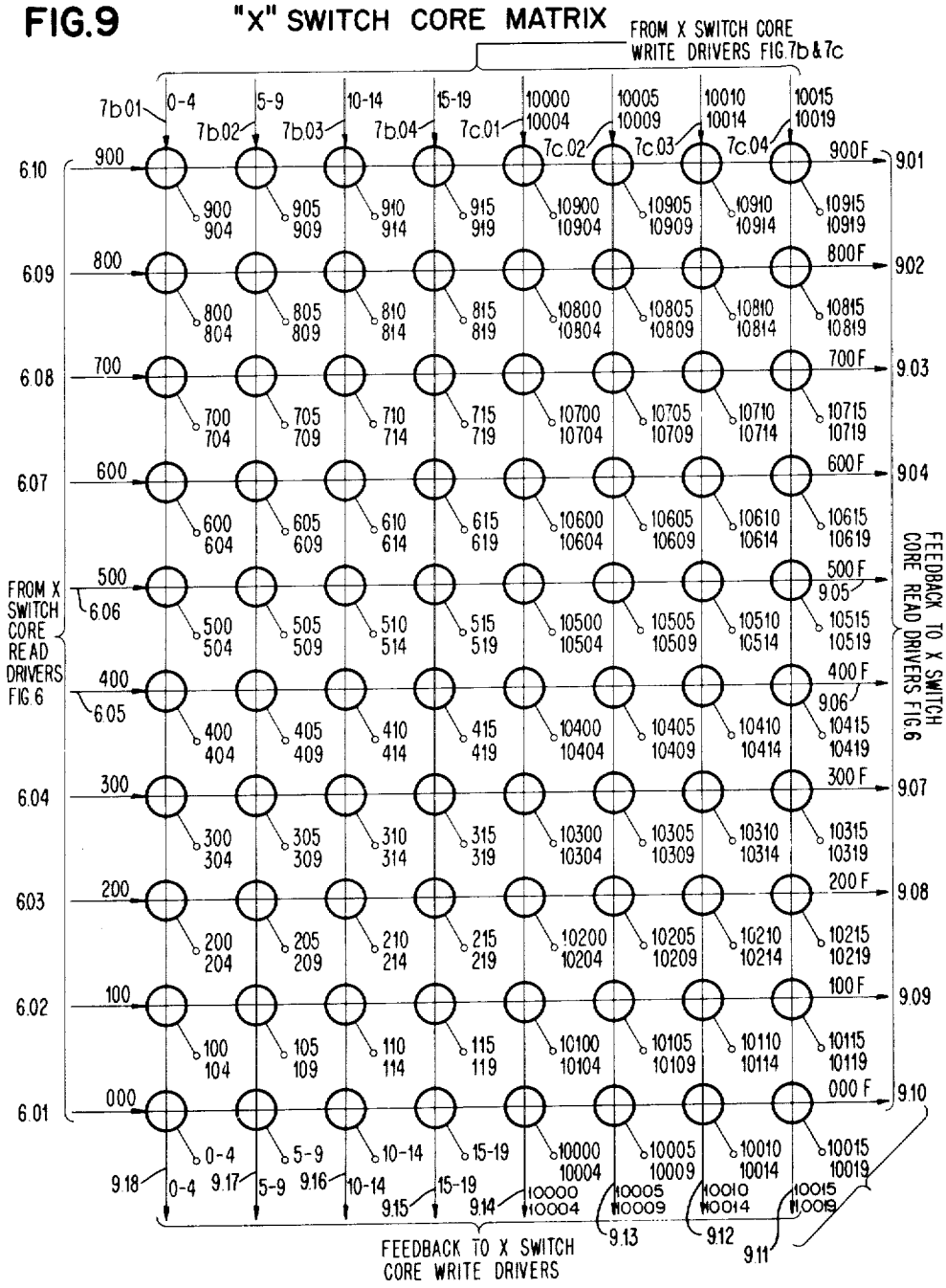
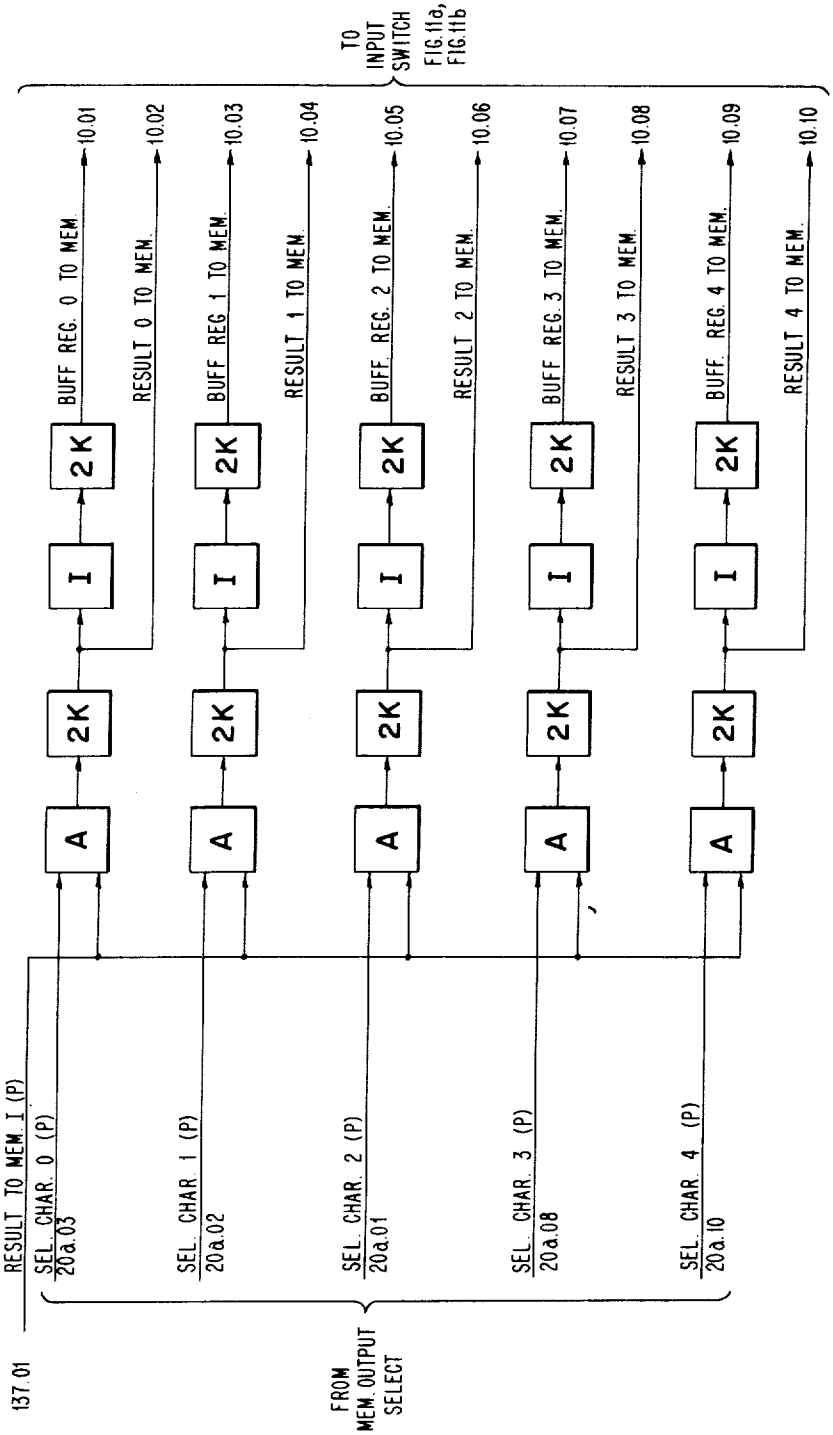


FIG. 10
MEM INPUT SELECT



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FIG. 11a MEM. INPUT SWITCH CHAR. 4,3,2

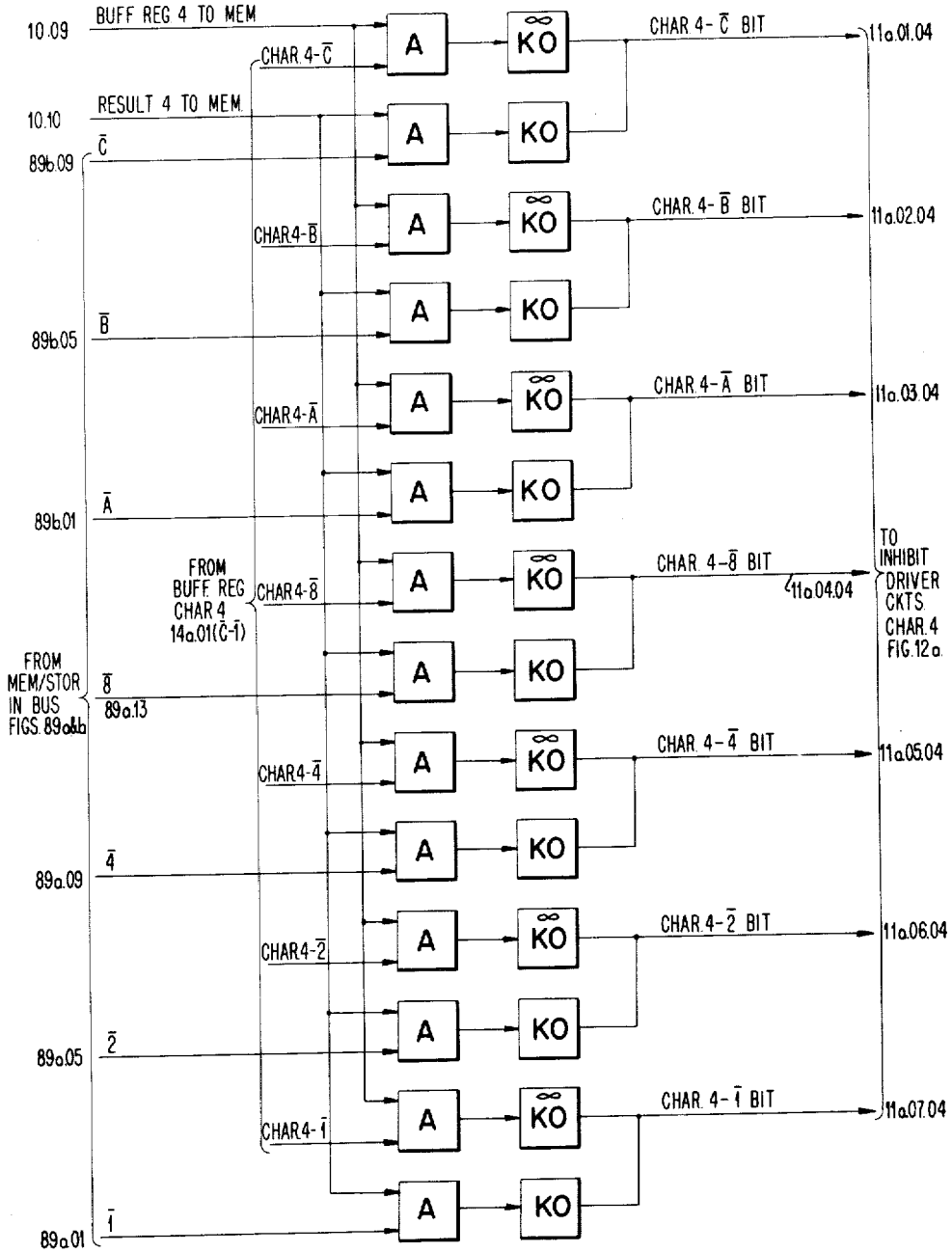


FIG.11b MEM. INPUT SWITCH CHAR. 0 & 1

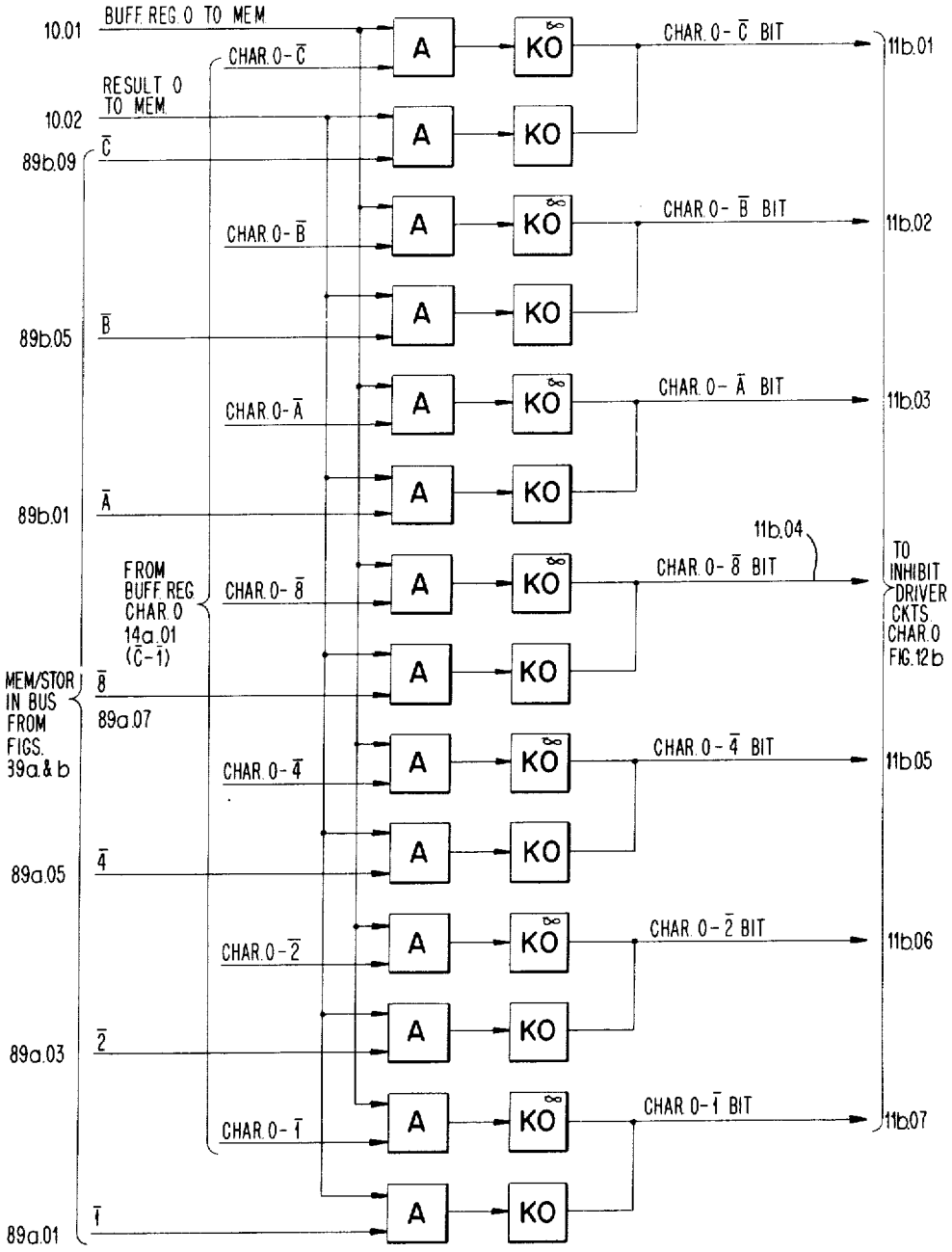


FIG.12a MEM. INHIBIT DRIVER CIRCUITS CHAR. 4,3 & 2

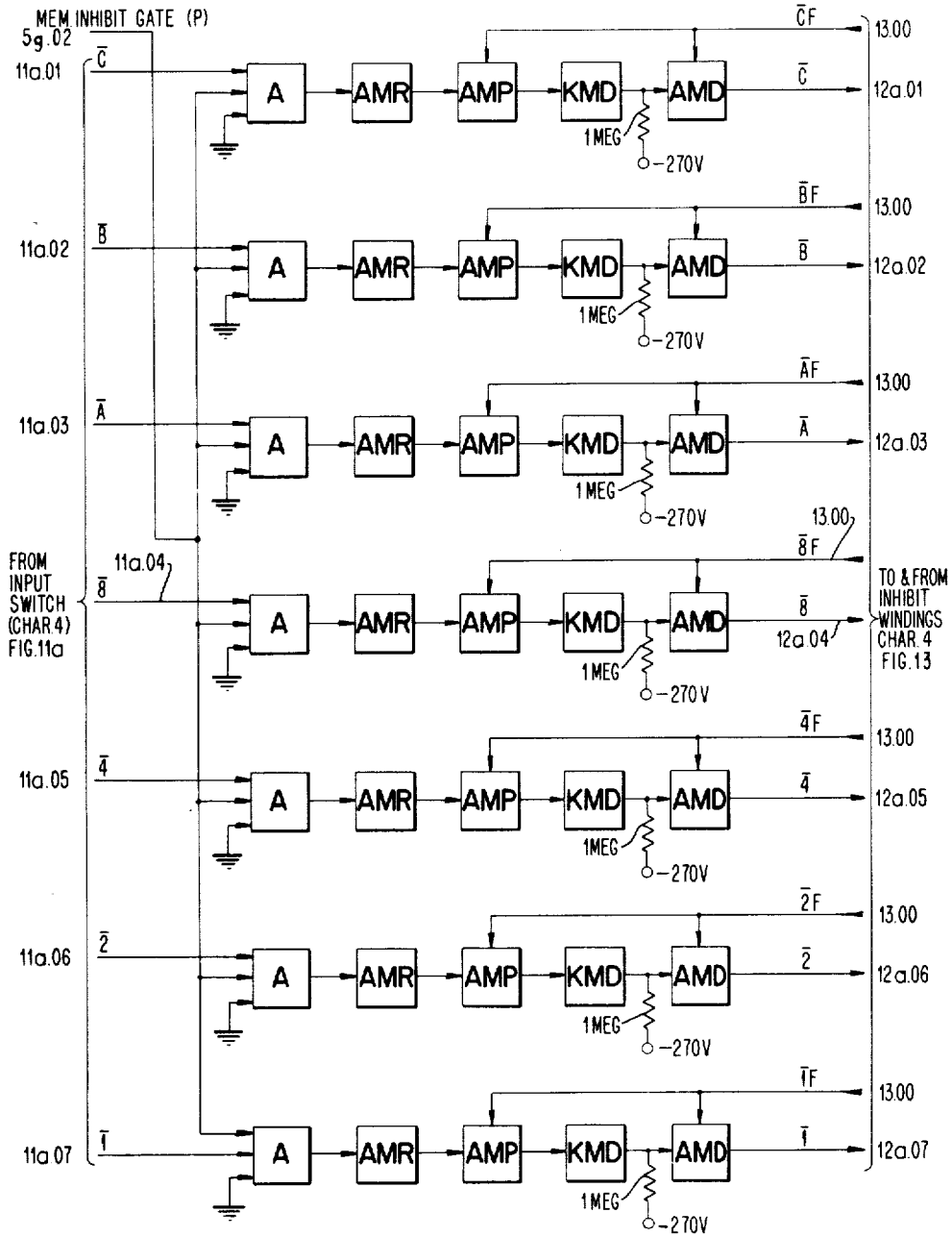


FIG.12b

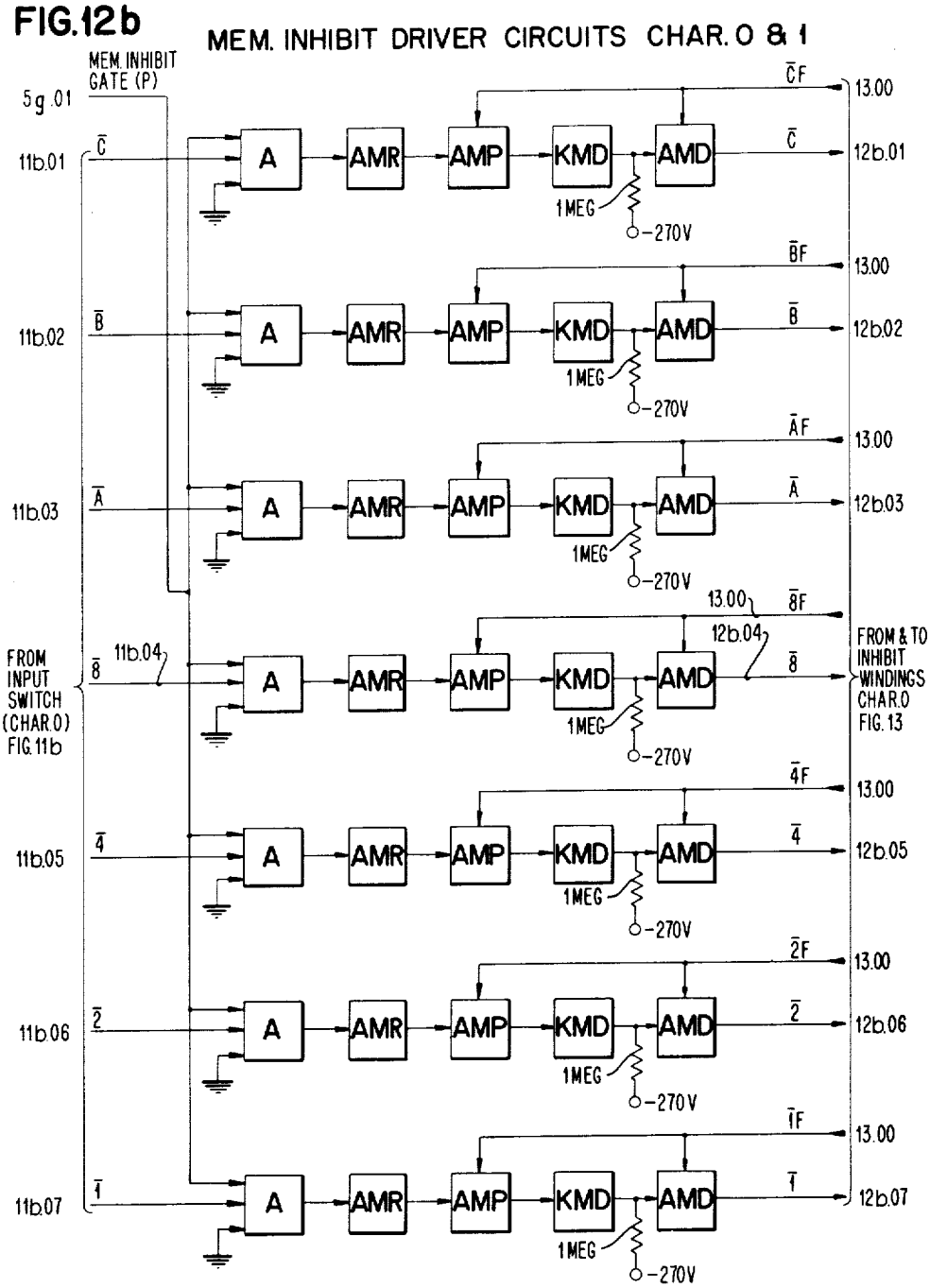
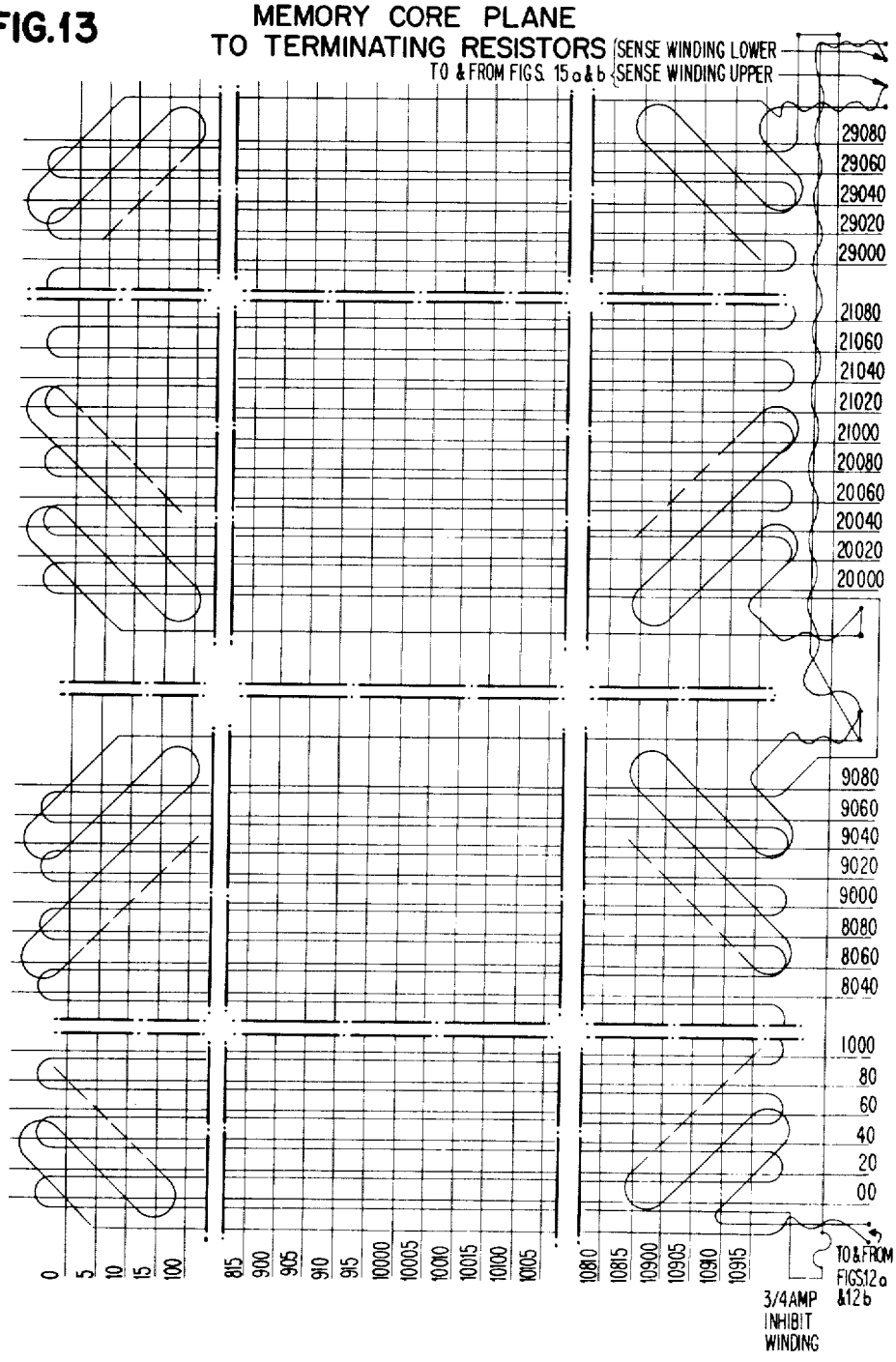

MEM. INHIBIT DRIVER CIRCUITS CHAR. 0 & 1
MEM. INHIBIT GATE (P)
5g.01
11b.01
11b.02
11b.03
11b.04
11b.05
11b.06
11b.07
FROM INPUT SWITCH (CHAR.0) FIG.11b
A
AMR
AMP
KMD
AMD
1MEG
-270V
13.00
12b.01
12b.02
12b.03
12b.04
12b.05
12b.06
12b.07
FROM & TO INHIBIT WINDINGS CHAR.0 FIG.13

FIG. 13


MEMORY CORE PLANE
TO TERMINATING RESISTORS
TO & FROM FIGS. 15a & b
SENSE WINDING LOWER
SENSE WINDING UPPER
29080
29060
29040
29020
29000
21080
21060
21040
21020
21000
20080
20060
20040
20020
20000
9080
9060
9040
9020
9000
8080
8060
8040
1000
80
60
40
20
00
0
5
10
15
100
815
900
905
910
915
10000
10005
10010
10015
10100
10105
10810
10815
10900
10905
10910
10915
TO & FROM FIGS 12a & 12b
3/4 AMP INHIBIT WINDING

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FIG. 14a

MEMORY BUFFER REGISTER CHAR. 4,3 & 2

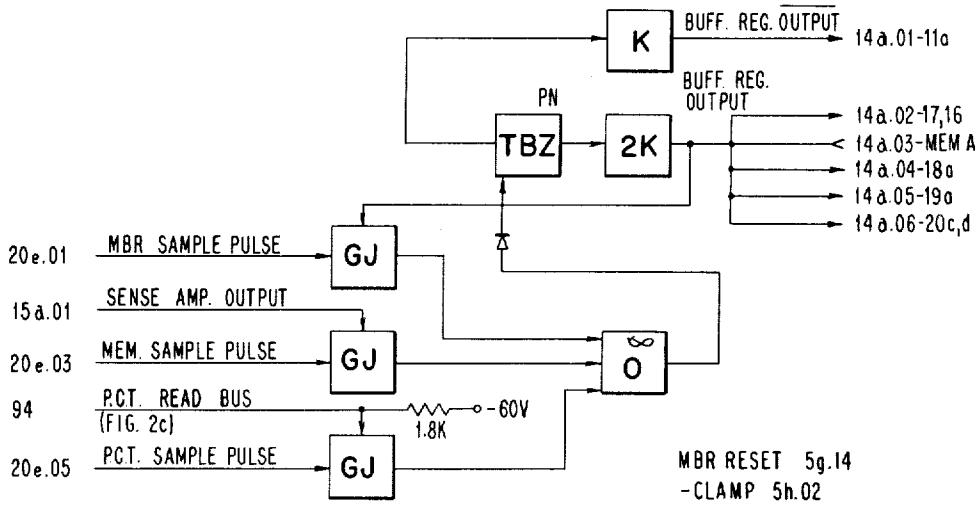


FIG. 14b

MEMORY BUFFER REGISTER CHAR. 0 & 1

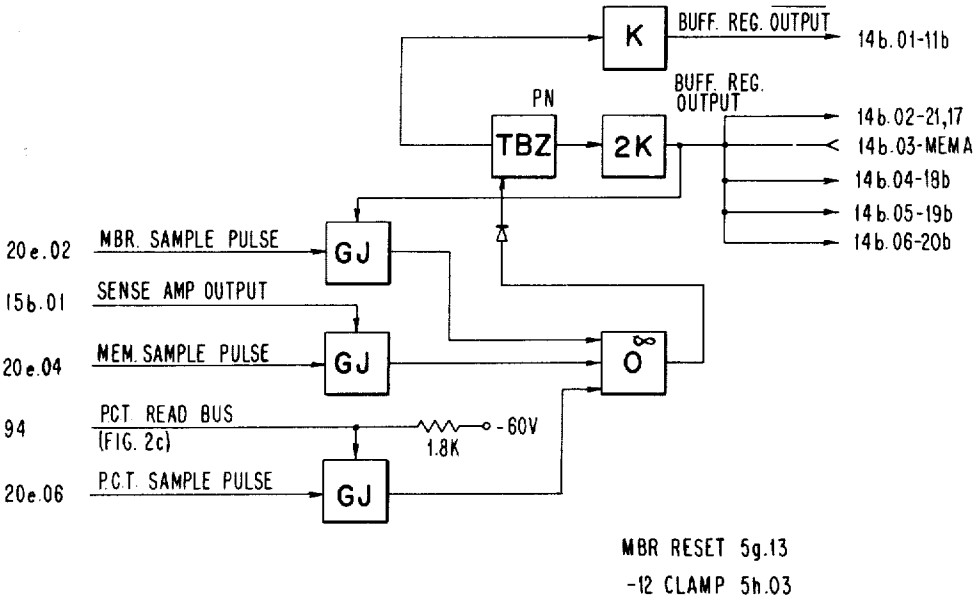


FIG. 15a
UPPER SENSE AMPLIFIER CIRCUITS
(TYPICAL OF ALL CHAR. 4,3&2 SENSE AMP.)

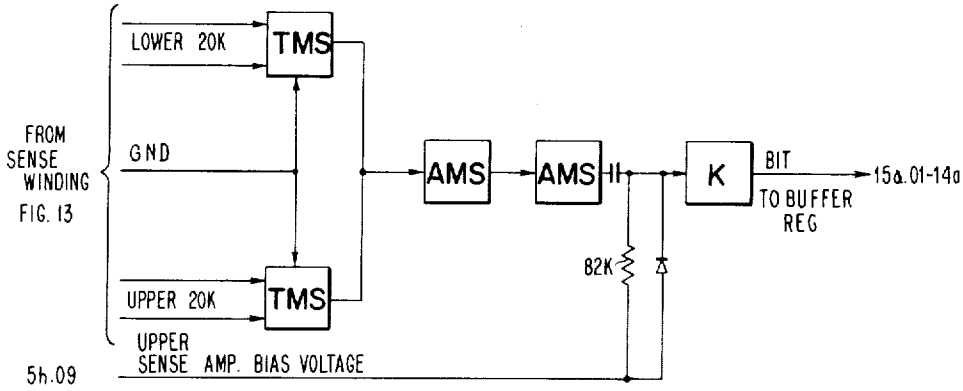
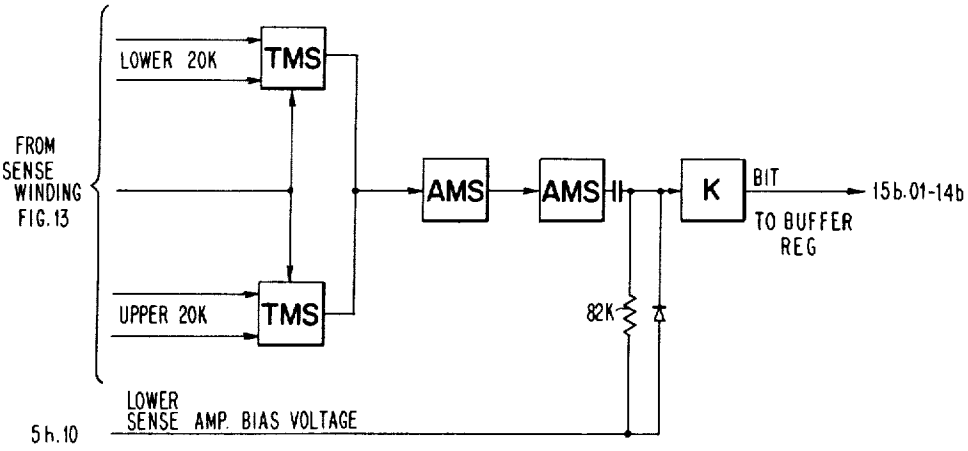
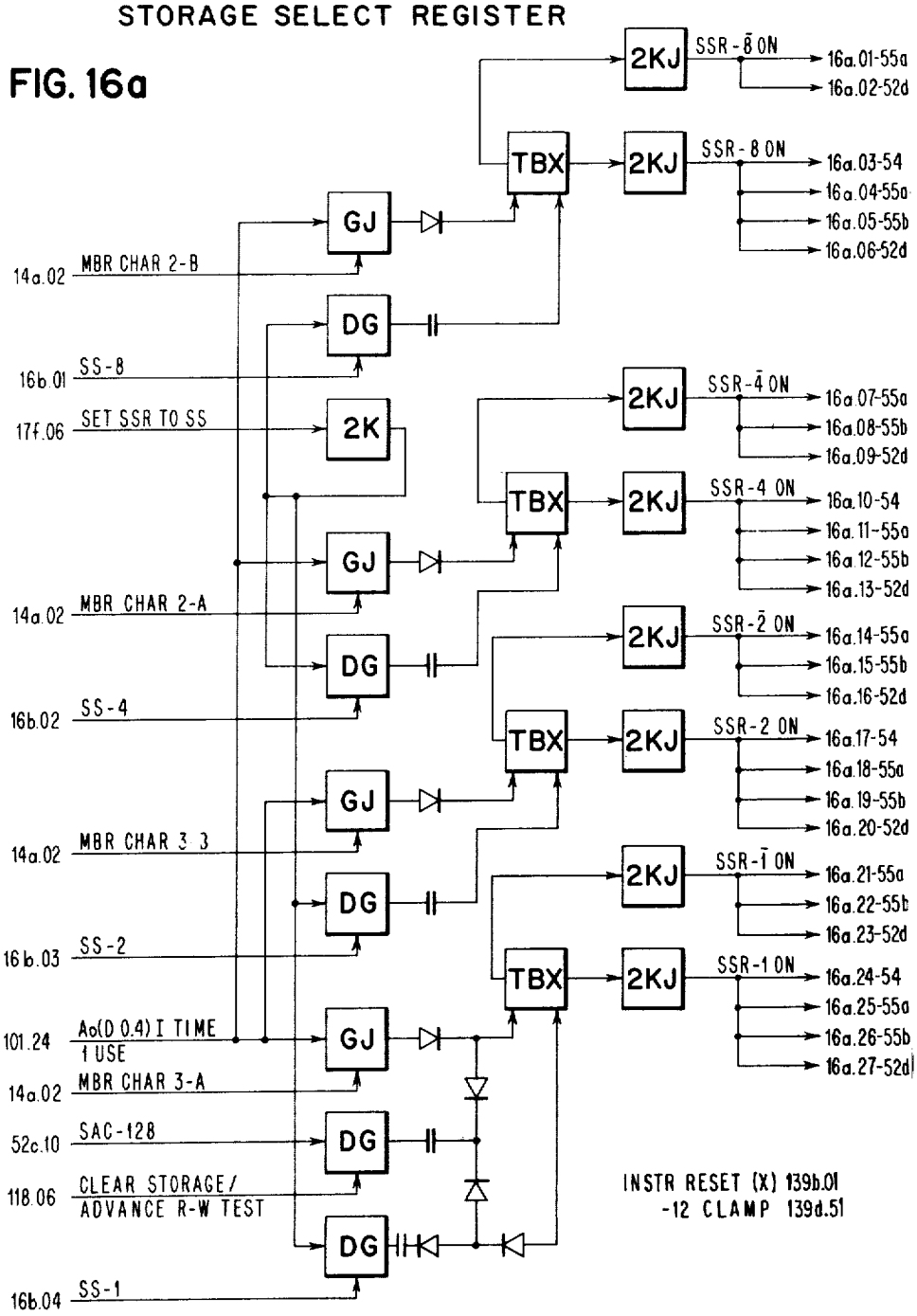


FIG. 15b
LOWER SENSE AMPLIFIER CIRCUITS
(TYPICAL OF ALL CHAR. 0&1 SENSE AMP.)



STORAGE SELECT REGISTER

FIG. 16a



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FIG.23k OPERATION DECODER LDA, BLM, TZB

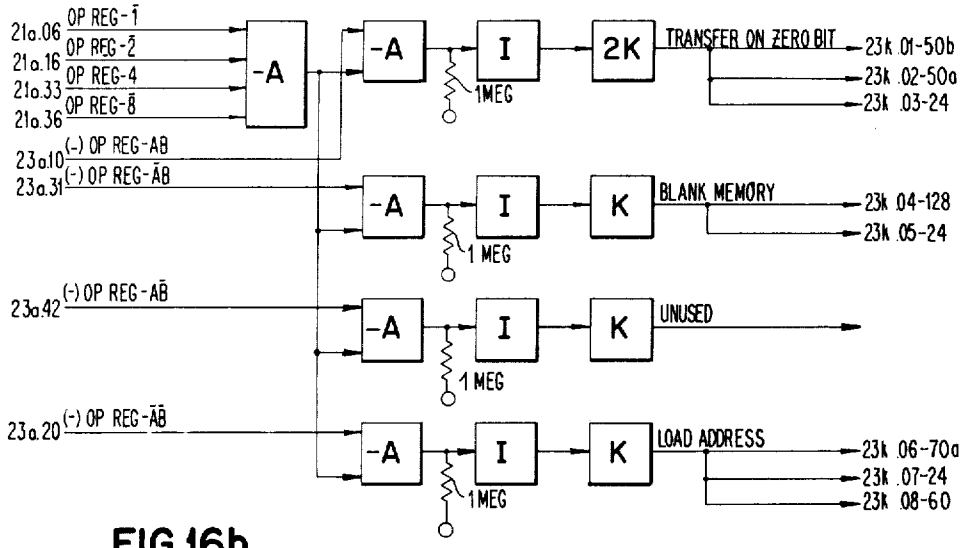
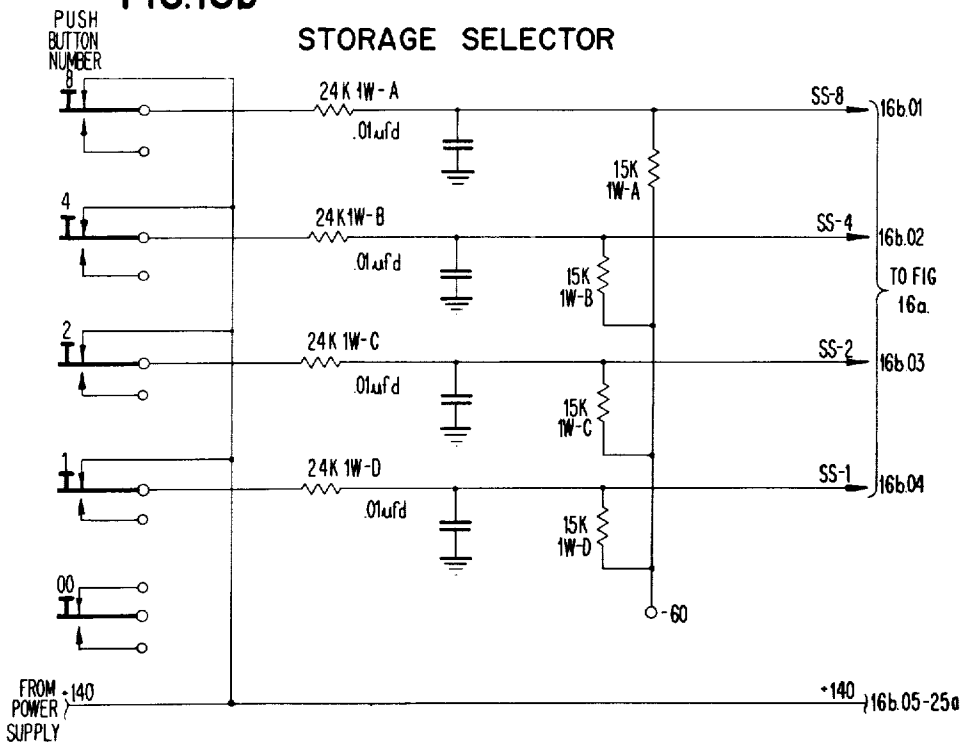


FIG.16b

STORAGE SELECTOR

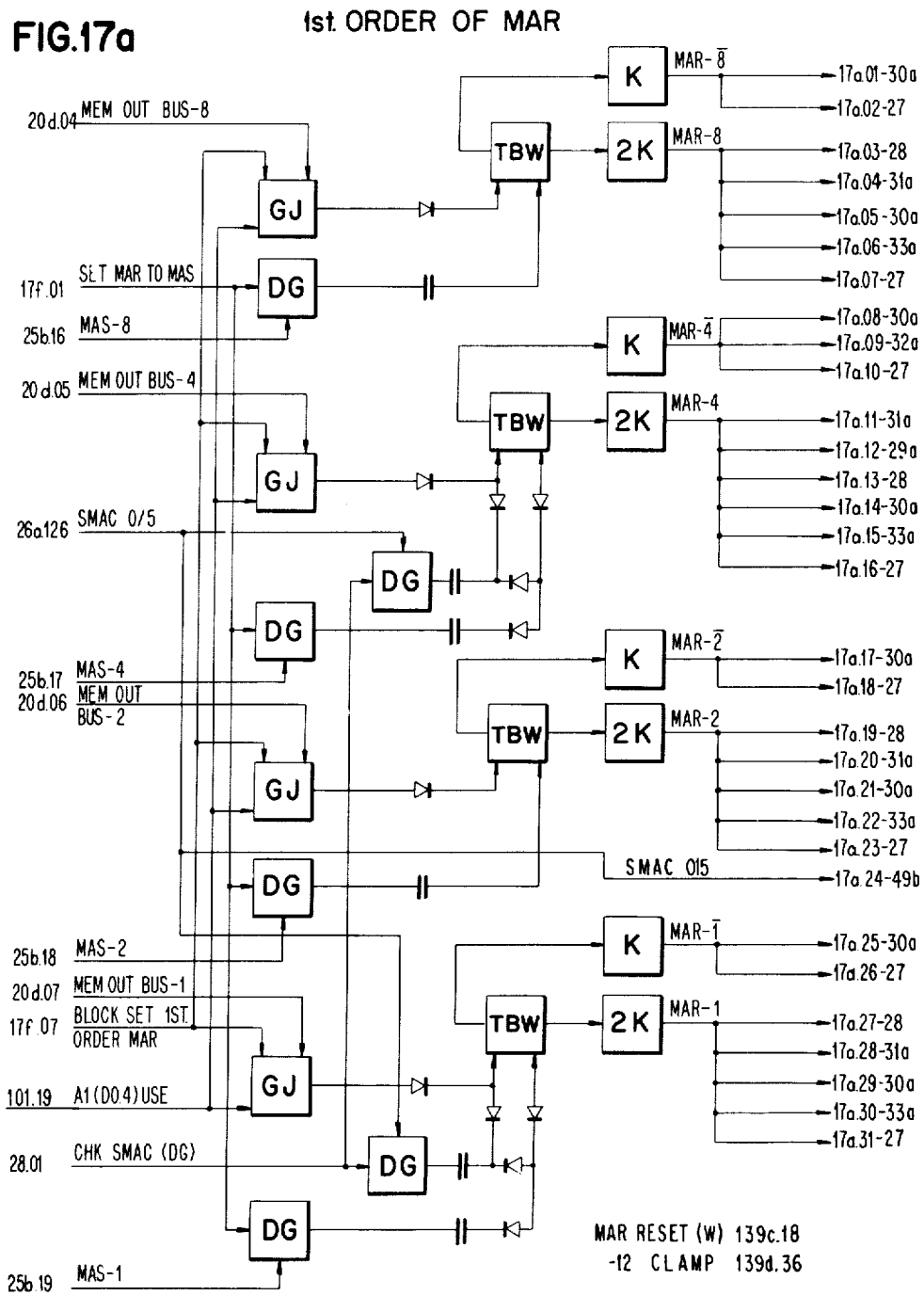


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FIG.17a



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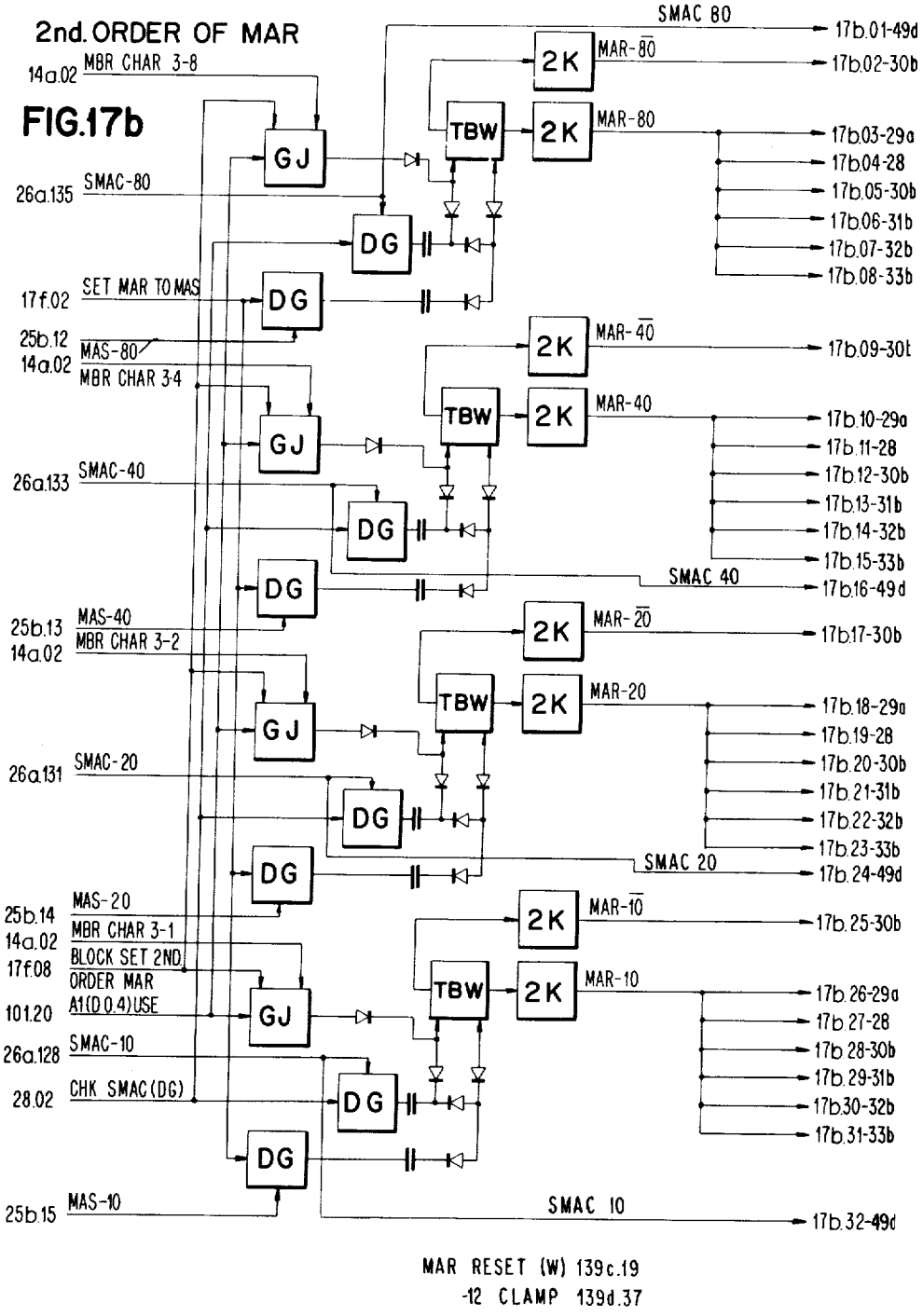


FIG.17c

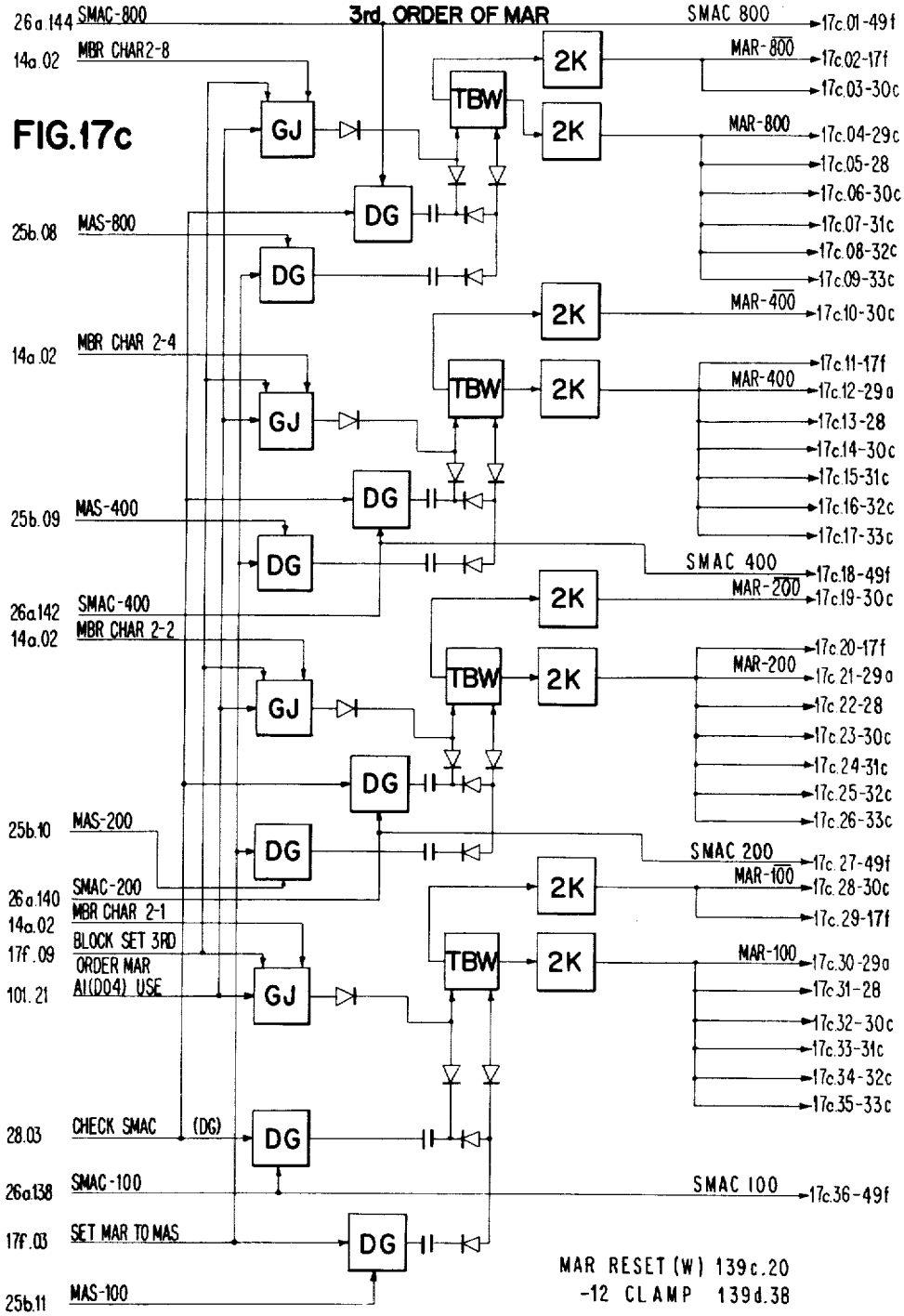
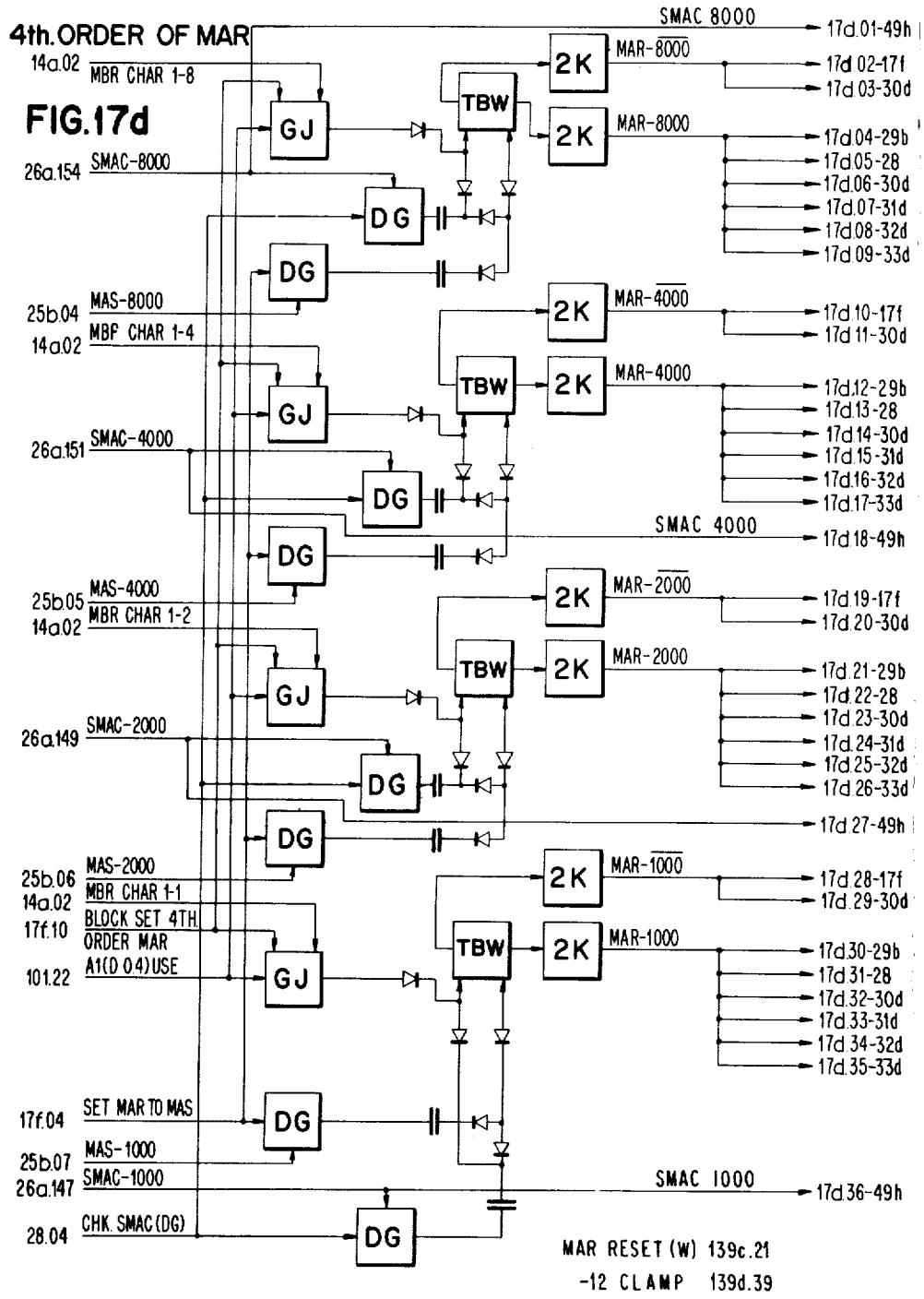
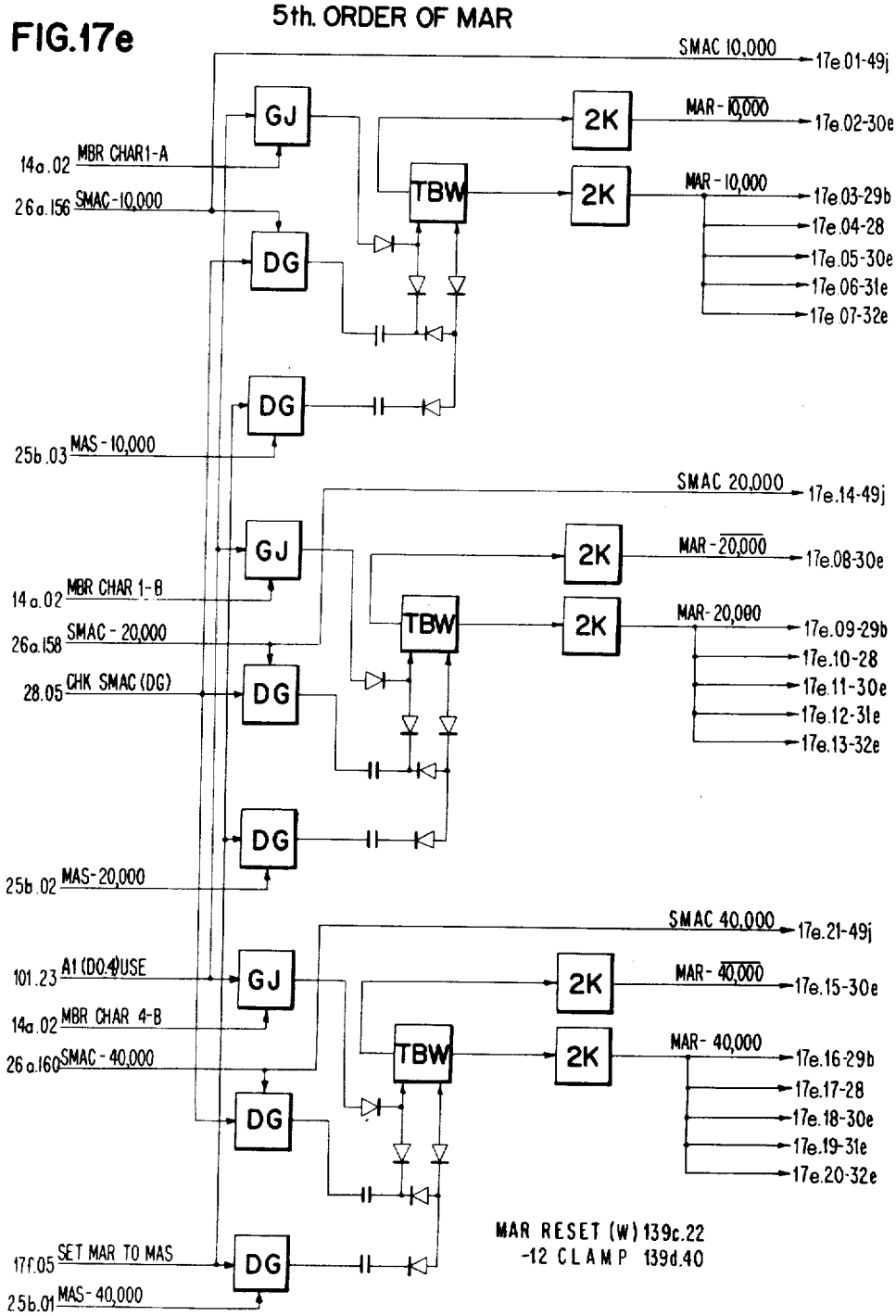

3rd. ORDER OF MAR
26a.144 SMAC-800
14a.02 MBR CHAR2-8
25b.08 MAS-800
14a.02 MBR CHAR 2-4
25b.09 MAS-400
26a.142 SMAC-400
14a.02 MBR CHAR 2-2
25b.10 MAS-200
26a.140 SMAC-200
14a.02 MBR CHAR 2-1
17f.09 BLOCK SET 3RD ORDER MAR
101.21 AI(D04) USE
28.03 CHECK SMAC (DG)
26a.138 SMAC-100
17f.03 SET MAR TO MAS
25b.11 MAS-100
GJ
DG
TBW
2K
SMAC 800
MAR-800
MAR-400
SMAC 400
MAR-200
SMAC 200
MAR-100
SMAC 100
17c.01-49f
17c.02-17f
17c.03-30c
17c.04-29c
17c.05-28
17c.06-30c
17c.07-31c
17c.08-32c
17c.09-33c
17c.10-30c
17c.11-17f
17c.12-29a
17c.13-28
17c.14-30c
17c.15-31c
17c.16-32c
17c.17-33c
17c.18-49f
17c.19-30c
17c.20-17f
17c.21-29a
17c.22-28
17c.23-30c
17c.24-31c
17c.25-32c
17c.26-33c
17c.27-49f
17c.28-30c
17c.29-17f
17c.30-29a
17c.31-28
17c.32-30c
17c.33-31c
17c.34-32c
17c.35-33c
17c.36-49f
MAR RESET (W) 139c.20
-12 CLAMP 139d.38

FIG.17d


4th.ORDER OF MAR
14a.02 MBR CHAR 1-8
26a.154 SMAC-8000
25b.04 MAS-8000
14a.02 MBF CHAR 1-4
26a.151 SMAC-4000
25b.05 MAS-4000
14a.02 MBR CHAR 1-2
26a.149 SMAC-2000
25b.06 MAS-2000
14a.02 MBR CHAR 1-1
17f.10 BLOCK SET 4TH ORDER MAR
101.22 A1(D 0-4) USE
17f.04 SET MAR TO MAS
25b.07 MAS-1000
26a.147 SMAC-1000
28.04 CHK. SMAC (DG)
GJ
DG
TBW
2K
SMAC 8000
MAR-8000
MAR-8000
MAR-4000
MAR-4000
SMAC 4000
MAR-2000
MAR-2000
MAR-1000
MAR-1000
SMAC 1000
17d.01-49h
17d.02-17f
17d.03-30d
17d.04-29b
17d.05-28
17d.06-30d
17d.07-31d
17d.08-32d
17d.09-33d
17d.10-17f
17d.11-30d
17d.12-29b
17d.13-28
17d.14-30d
17d.15-31d
17d.16-32d
17d.17-33d
17d.18-49h
17d.19-17f
17d.20-30d
17d.21-29b
17d.22-28
17d.23-30d
17d.24-31d
17d.25-32d
17d.26-33d
17d.27-49h
17d.28-17f
17d.29-30d
17d.30-29b
17d.31-28
17d.32-30d
17d.33-31d
17d.34-32d
17d.35-33d
17d.36-49h
MAR RESET (W) 139c.21
-12 CLAMP 139d.39

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FIG.17e



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FIG.17f

MEMORY ADDRESS REGISTER CONTROLS

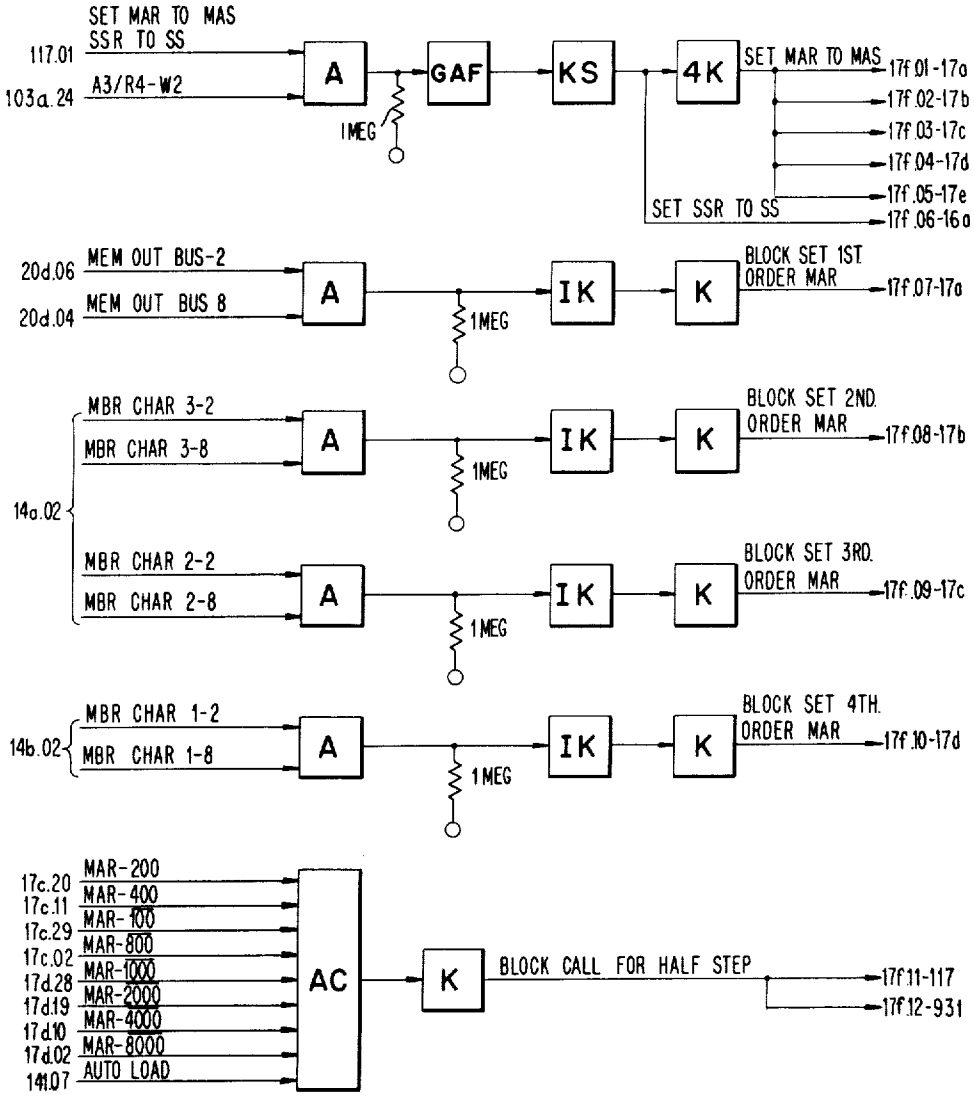


FIG. 18a

P.C.T. WRITE BUSSES CHAR. 4,3 & 2

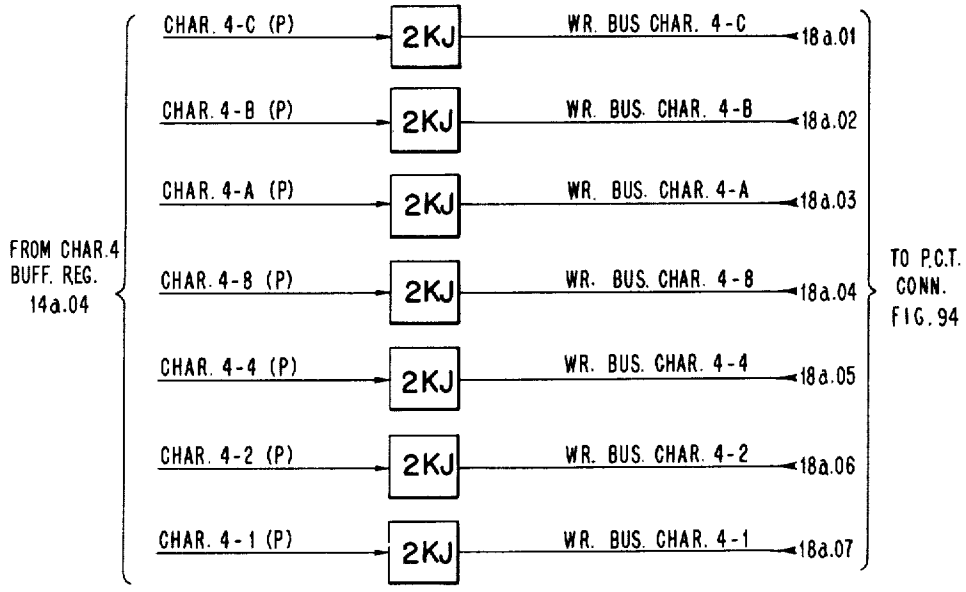


FIG. 18b

P.C.T. WRITE BUSSES CHAR. 1 & 0

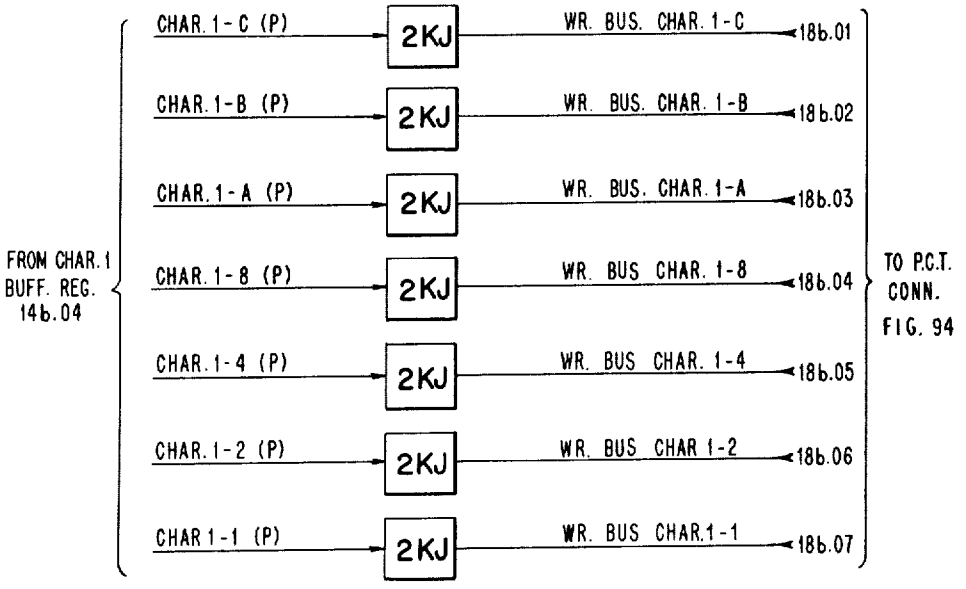


FIG. 19a

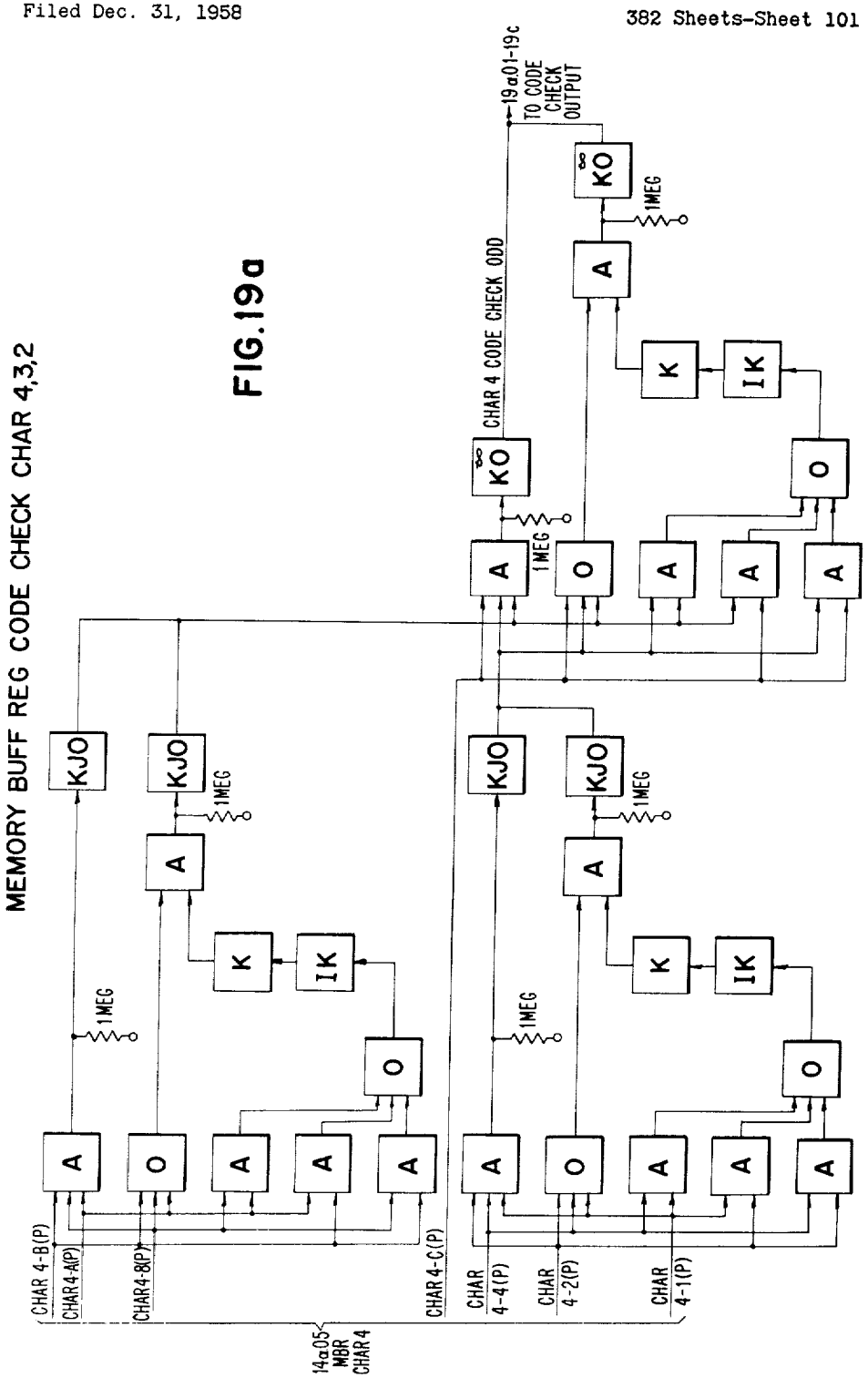

MEMORY BUFF REG CODE CHECK CHAR 4,3,2
19a01-19c TO CODE CHECK OUTPUT
CHAR 4 CODE CHECK ODD
KO
1MEG
A
K
IK
O
KJO
CHAR 4-B(P)
CHAR 4-A(P)
CHAR 4-8(P)
CHAR 4-C(P)
CHAR 4-4(P)
CHAR 4-2(P)
CHAR 4-1(P)
14a05 MBR CHAR 4

FIG.19b

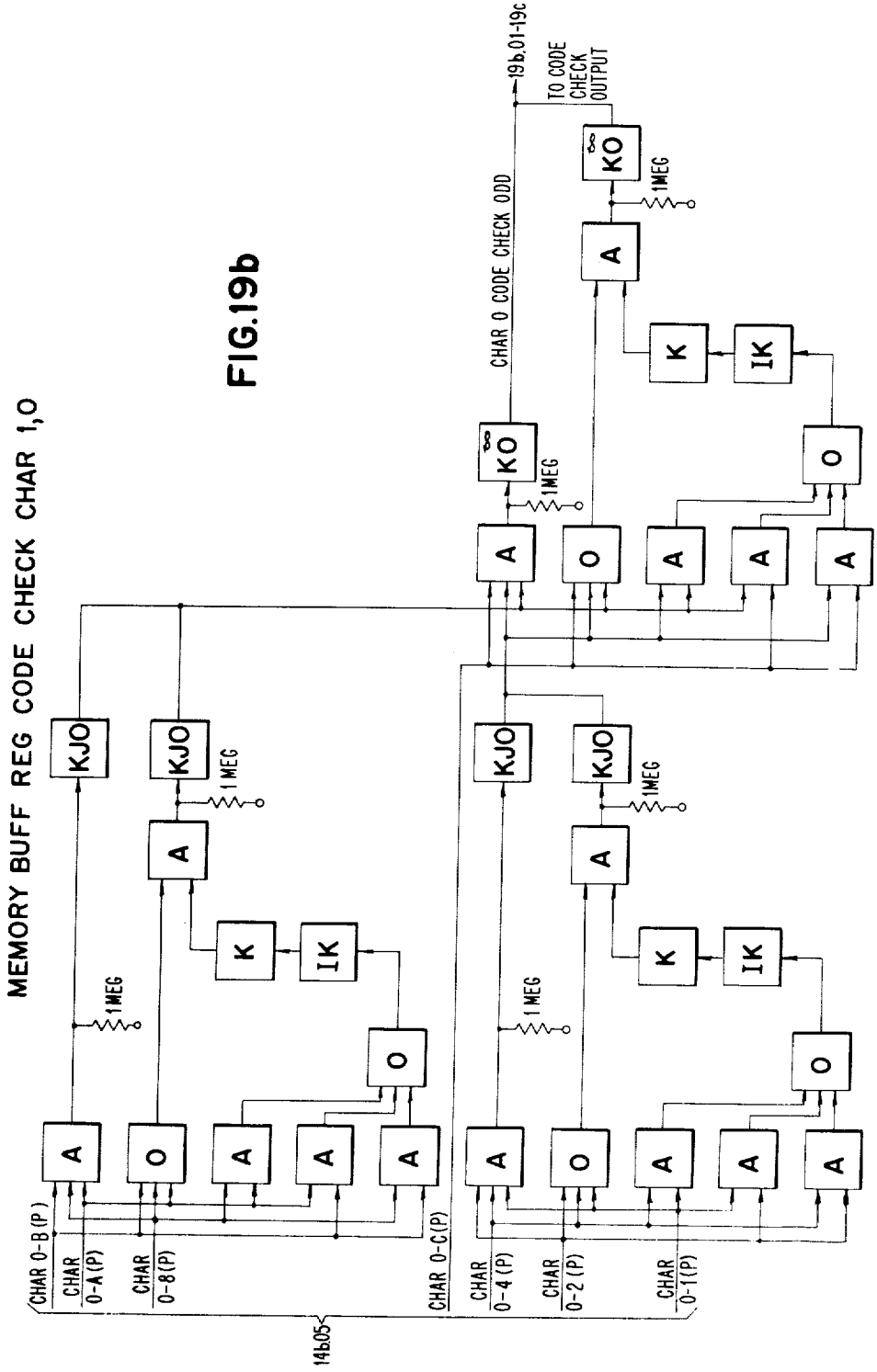

MEMORY BUFF REG CODE CHECK CHAR 1,0
19b.01-19c
TO CODE CHECK OUTPUT
CHAR 0 CODE CHECK ODD
KO
KJO
A
O
K
IK
1MEG
CHAR 0-B (P)
CHAR 0-A (P)
CHAR 0-8 (P)
CHAR 0-C (P)
CHAR 0-4 (P)
CHAR 0-2 (P)
CHAR 0-1 (P)
14b05

FIG. 19c

MEMORY BUFF. REG. CODE CHECK OUTPUT

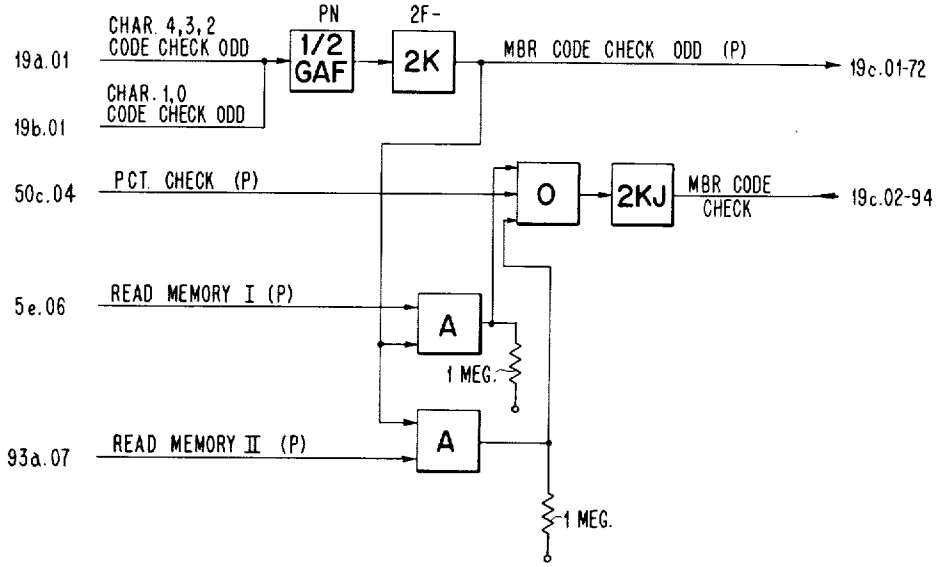


FIG. 142b DRIVER BIAS VOLTAGE REGULATOR

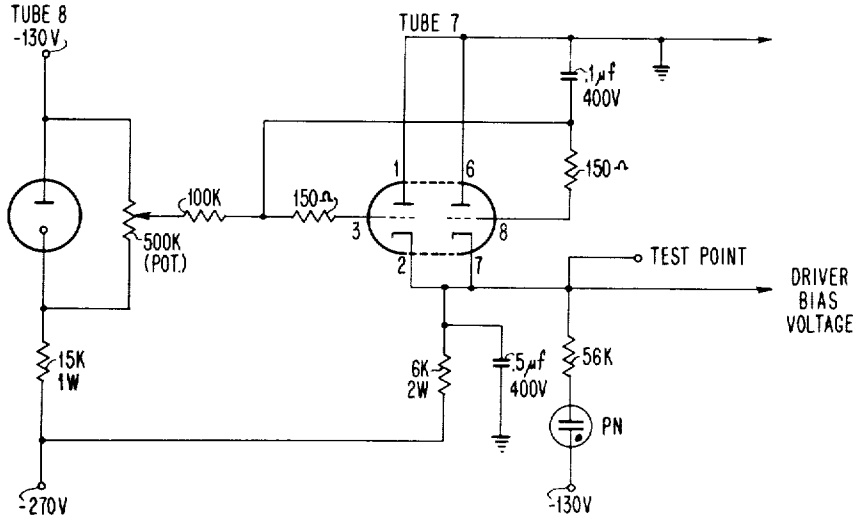
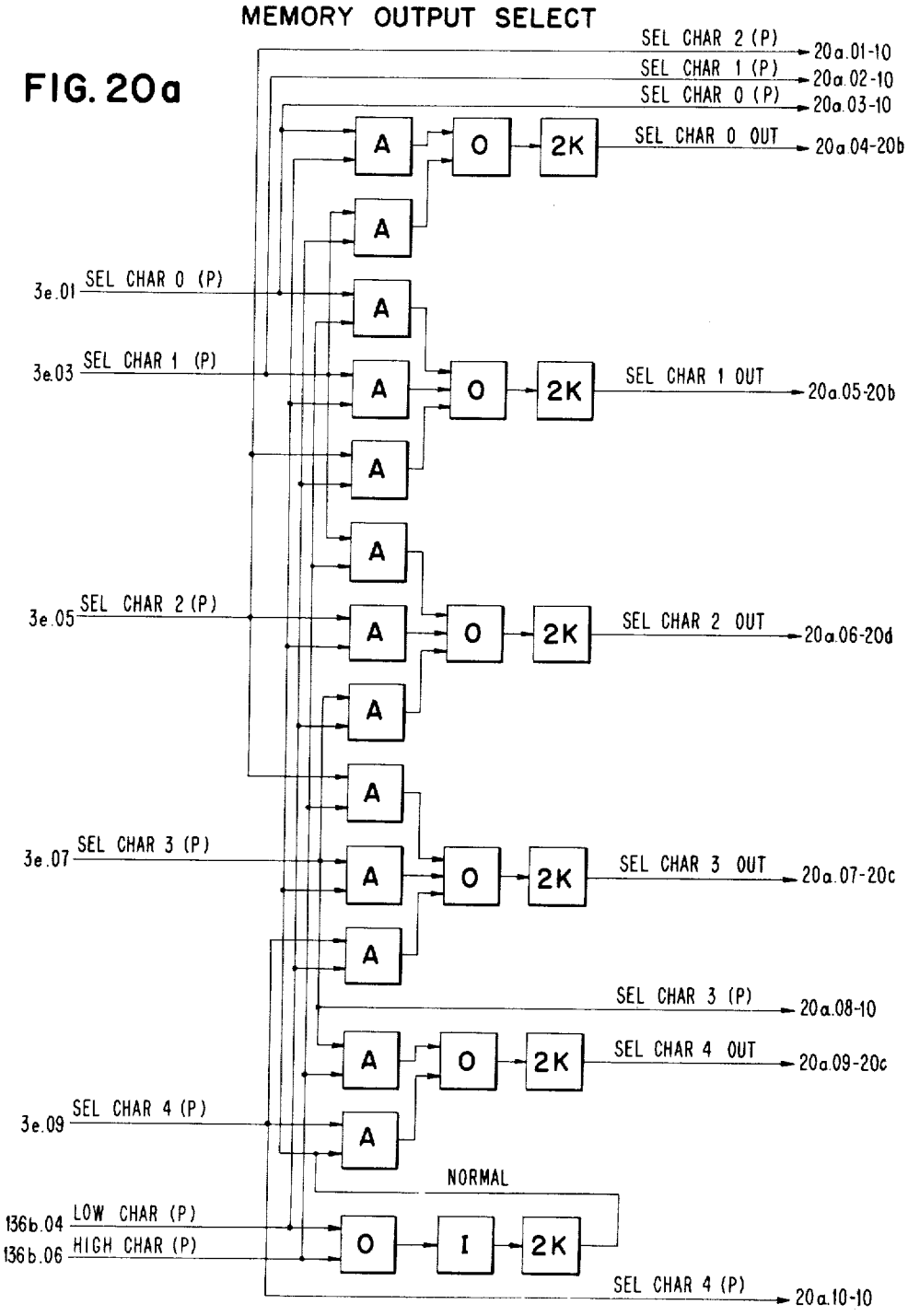


FIG. 20a


MEMORY OUTPUT SELECT
SEL CHAR 2 (P)
20a.01-10
SEL CHAR 1 (P)
20a.02-10
SEL CHAR 0 (P)
20a.03-10
A
O
2K
SEL CHAR 0 OUT
20a.04-20b
3e.01 SEL CHAR 0 (P)
3e.03 SEL CHAR 1 (P)
SEL CHAR 1 OUT
20a.05-20b
3e.05 SEL CHAR 2 (P)
SEL CHAR 2 OUT
20a.06-20d
3e.07 SEL CHAR 3 (P)
SEL CHAR 3 OUT
20a.07-20c
SEL CHAR 3 (P)
20a.08-10
SEL CHAR 4 OUT
20a.09-20c
3e.09 SEL CHAR 4 (P)
NORMAL
136b.04 LOW CHAR (P)
136b.06 HIGH CHAR (P)
I
SEL CHAR 4 (P)
20a.10-10

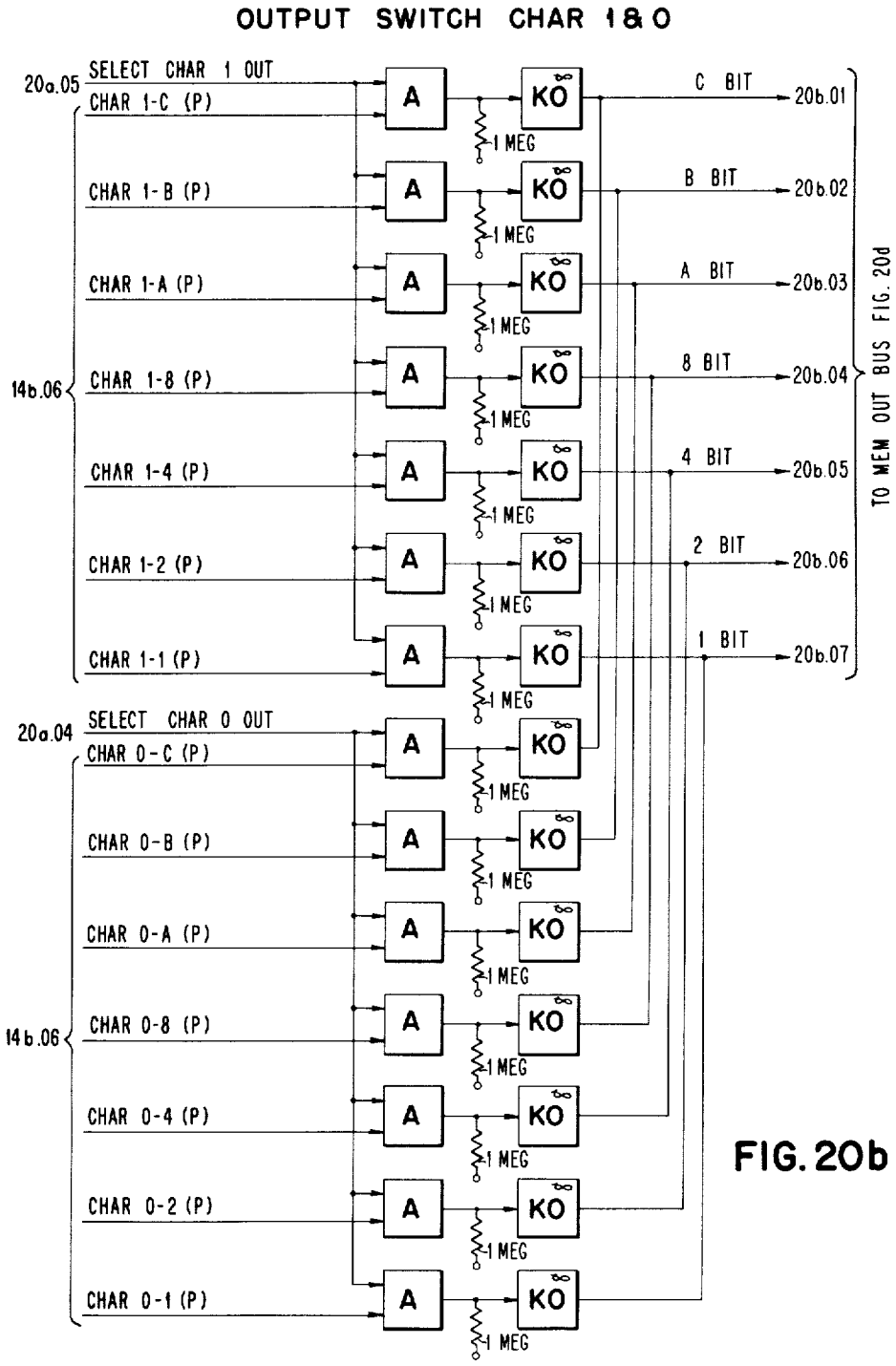

OUTPUT SWITCH CHAR 1 & 0
20a.05
SELECT CHAR 1 OUT
CHAR 1-C (P)
CHAR 1-B (P)
CHAR 1-A (P)
14b.06
CHAR 1-8 (P)
CHAR 1-4 (P)
CHAR 1-2 (P)
CHAR 1-1 (P)
20a.04
SELECT CHAR 0 OUT
CHAR 0-C (P)
CHAR 0-B (P)
CHAR 0-A (P)
14b.06
CHAR 0-8 (P)
CHAR 0-4 (P)
CHAR 0-2 (P)
CHAR 0-1 (P)
A
KO
1 MEG
C BIT
B BIT
A BIT
8 BIT
4 BIT
2 BIT
1 BIT
20b.01
20b.02
20b.03
20b.04
20b.05
20b.06
20b.07
TO MEM OUT BUS FIG. 20d

FIG. 20b

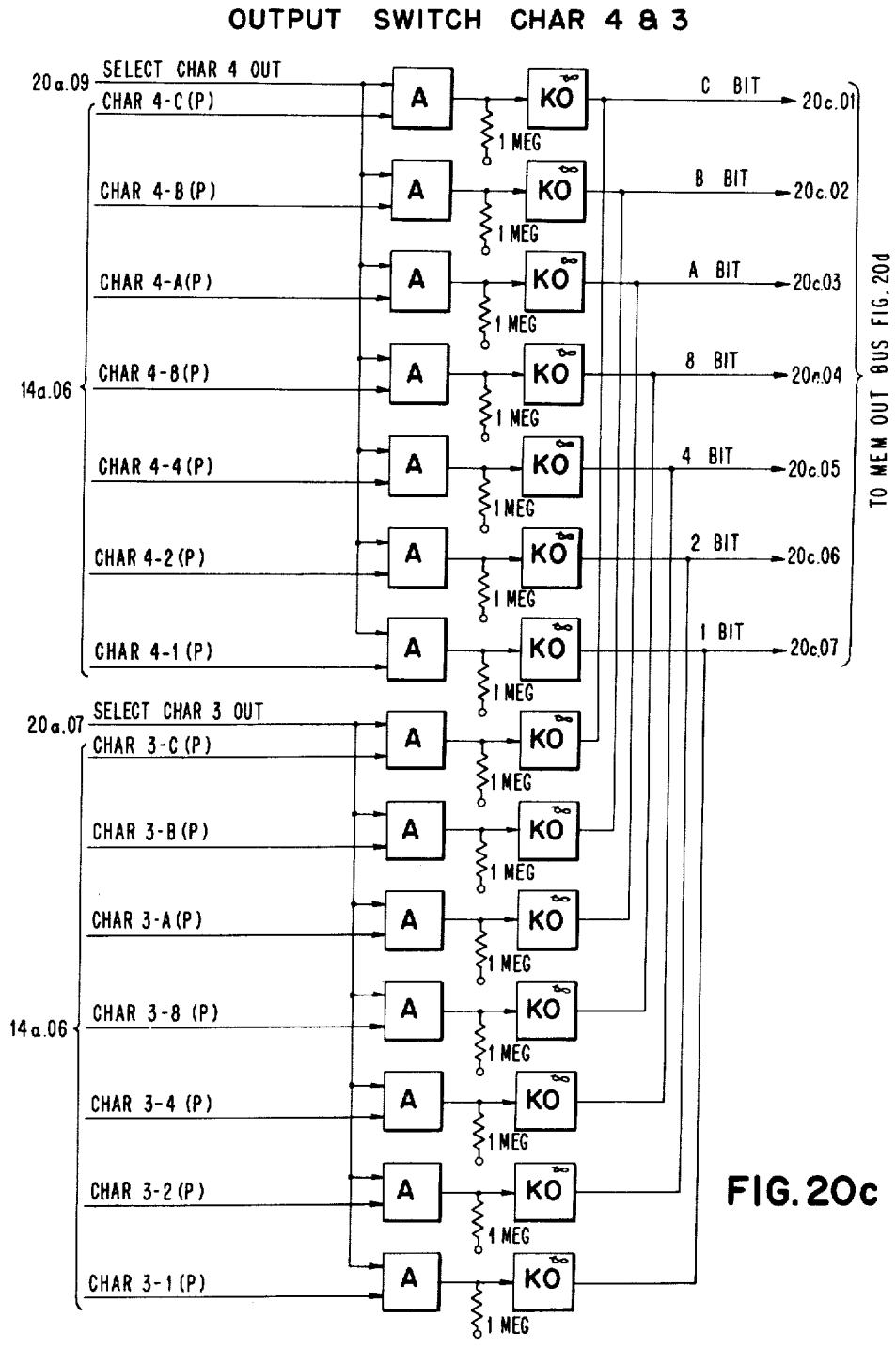

OUTPUT SWITCH CHAR 4 & 3
20a.09
SELECT CHAR 4 OUT
CHAR 4-C(P)
CHAR 4-B(P)
CHAR 4-A(P)
CHAR 4-8(P)
CHAR 4-4(P)
CHAR 4-2(P)
CHAR 4-1(P)
14a.06
20a.07
SELECT CHAR 3 OUT
CHAR 3-C(P)
CHAR 3-B(P)
CHAR 3-A(P)
CHAR 3-8(P)
CHAR 3-4(P)
CHAR 3-2(P)
CHAR 3-1(P)
14a.06
A
KO
1 MEG
C BIT
B BIT
A BIT
8 BIT
4 BIT
2 BIT
1 BIT
20c.01
20c.02
20c.03
20c.04
20c.05
20c.06
20c.07
TO MEM OUT BUS FIG. 20d

FIG. 20c

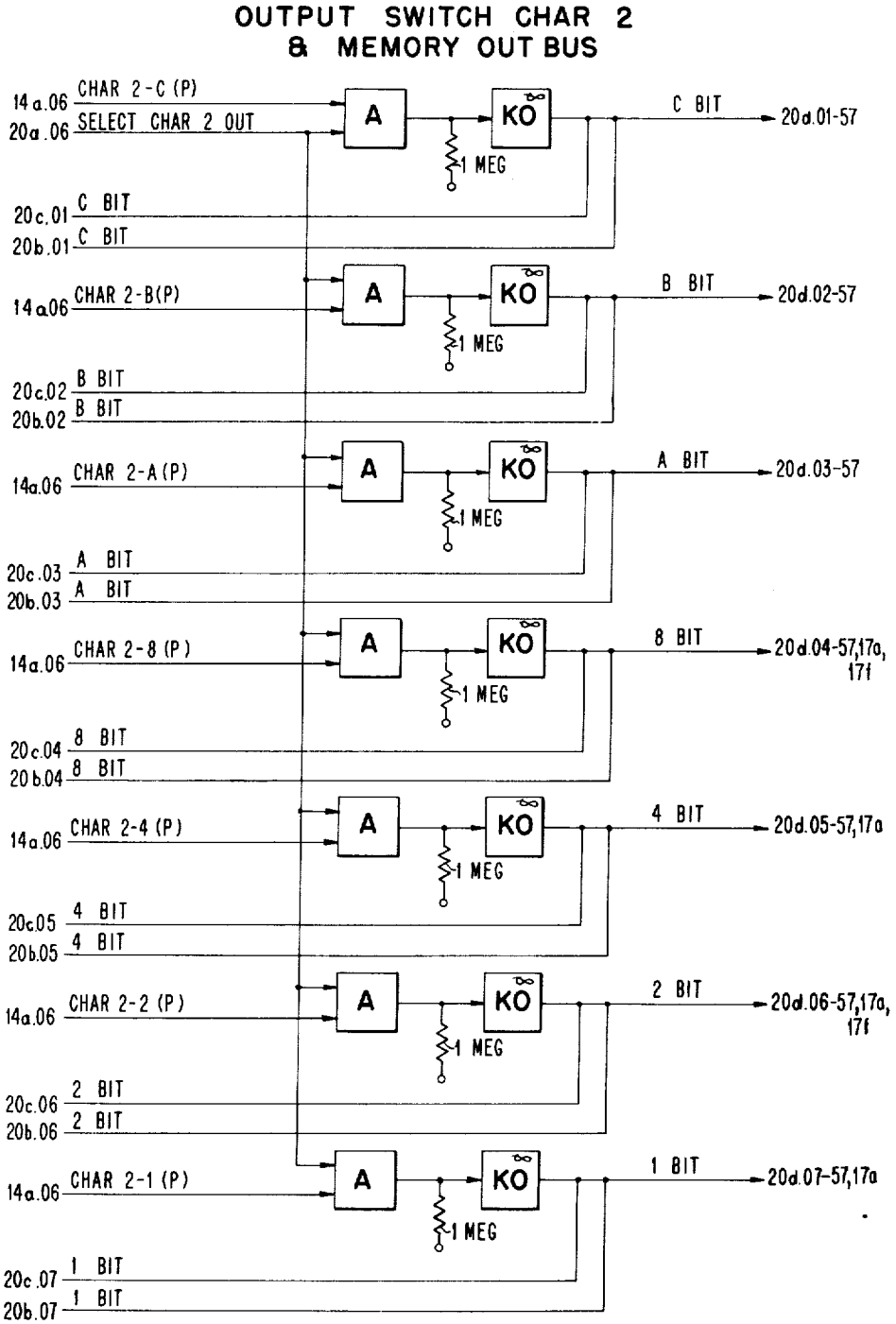
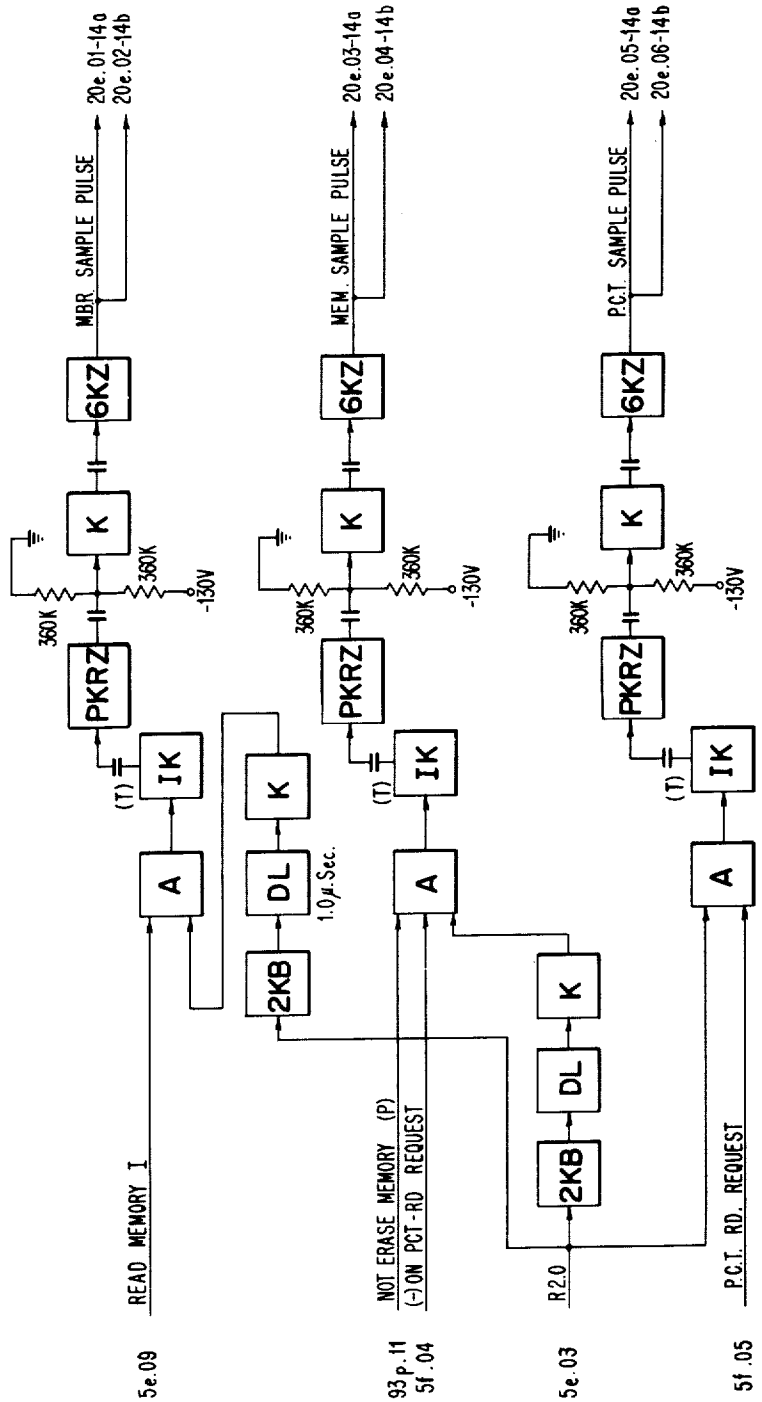

OUTPUT SWITCH CHAR 2
& MEMORY OUT BUS
14a.06 CHAR 2-C (P)
20a.06 SELECT CHAR 2 OUT
A
KO
1 MEG
C BIT
20d.01-57
20c.01 C BIT
20b.01 C BIT
14a.06 CHAR 2-B(P)
B BIT
20d.02-57
20c.02 B BIT
20b.02 B BIT
14a.06 CHAR 2-A(P)
A BIT
20d.03-57
20c.03 A BIT
20b.03 A BIT
14a.06 CHAR 2-8 (P)
8 BIT
20d.04-57,17a, 17f
20c.04 8 BIT
20b.04 8 BIT
14a.06 CHAR 2-4 (P)
4 BIT
20d.05-57,17a
20c.05 4 BIT
20b.05 4 BIT
14a.06 CHAR 2-2 (P)
2 BIT
20d.06-57,17a, 17f
20c.06 2 BIT
20b.06 2 BIT
14a.06 CHAR 2-1 (P)
1 BIT
20d.07-57,17a
20c.07 1 BIT
20b.07 1 BIT

FIG. 20d

FIG. 20e

MEMORY SAMPLE PULSE GENERATOR & P.C.T. SAMPLE PULSE GEN. &
M.B.R SAMPLE PULSE GENERATOR



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FIG. 21a

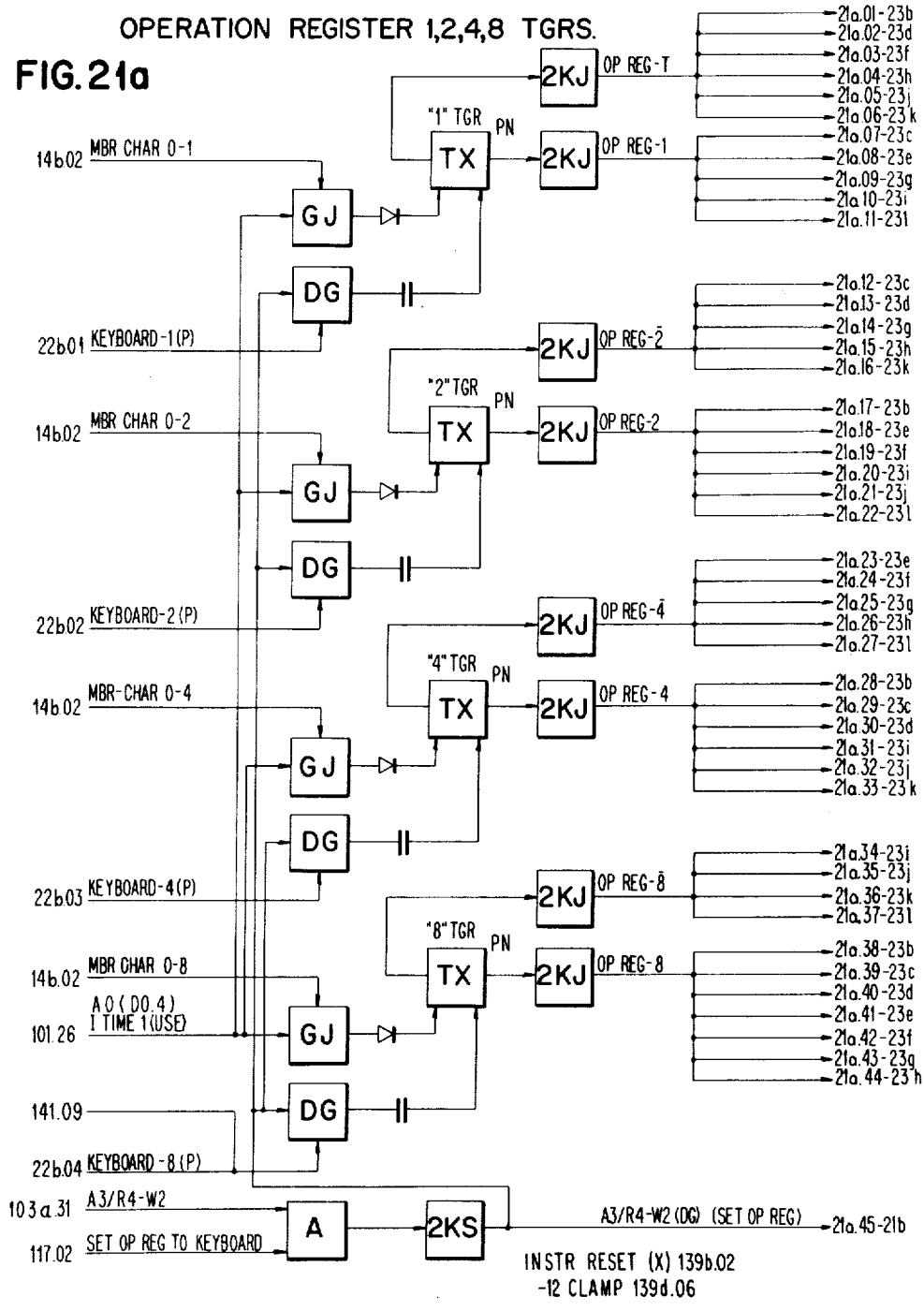
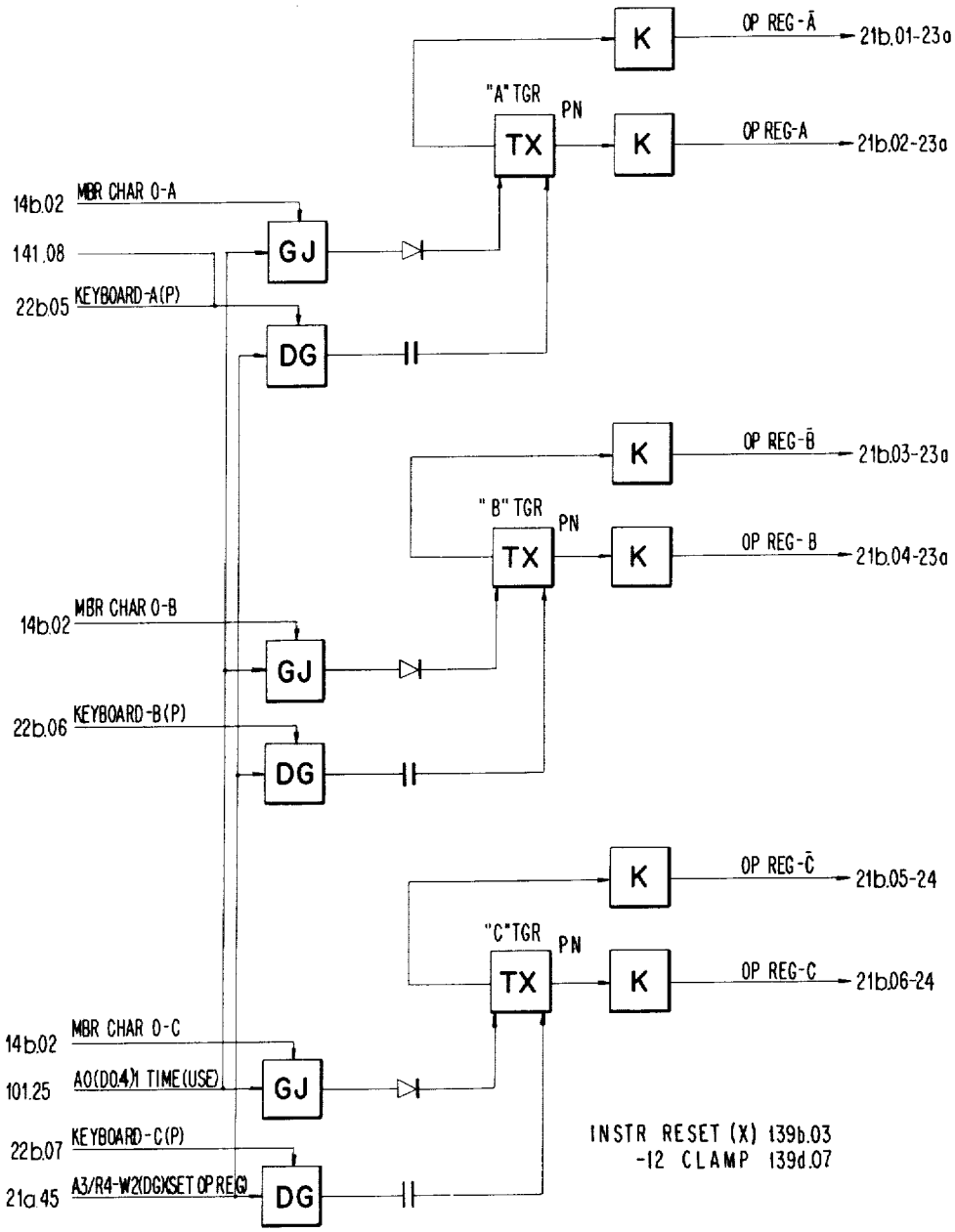


FIG.21b

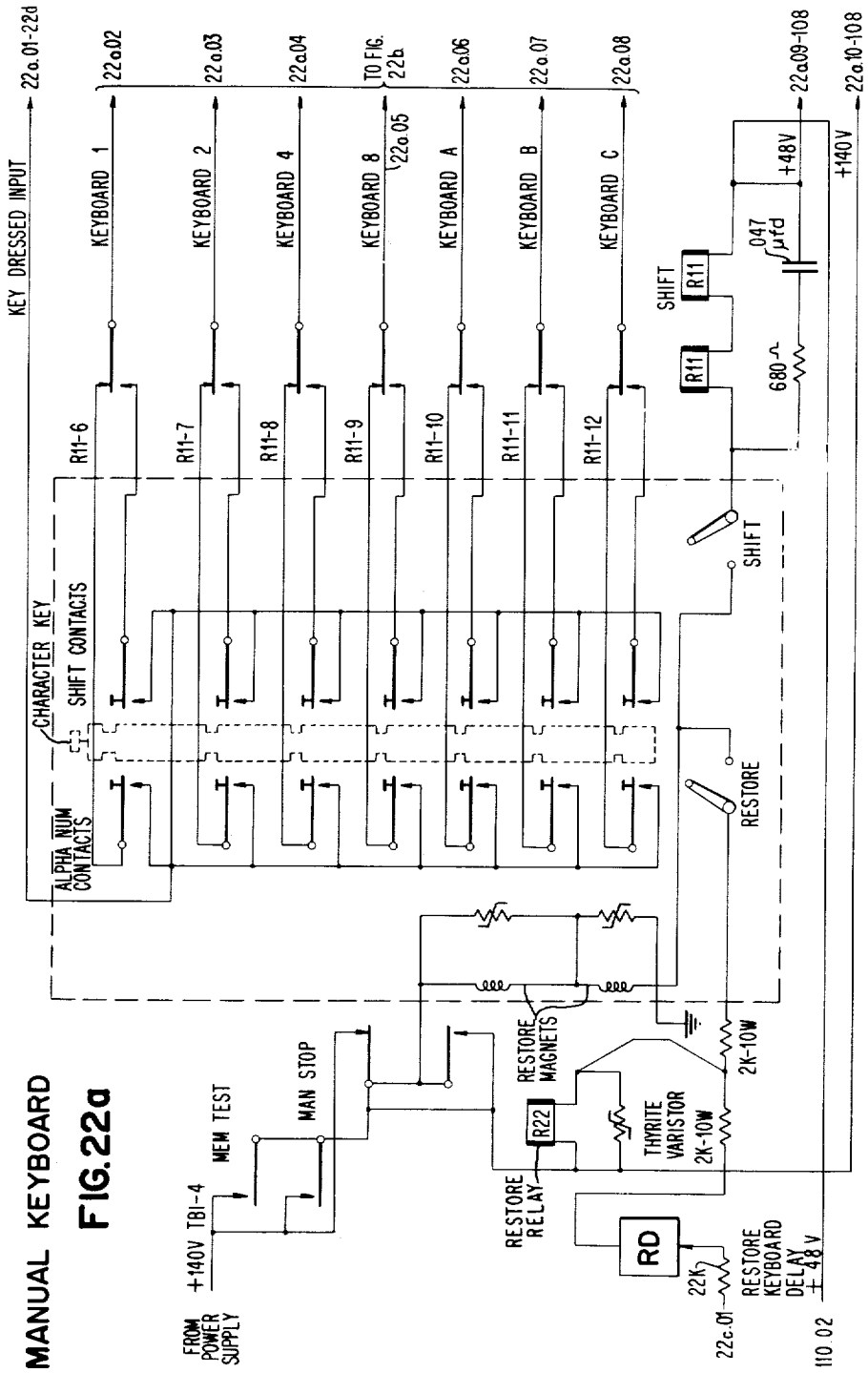
OPERATION REGISTER A,B,C TRIGGERS



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MANUAL KEYBOARD

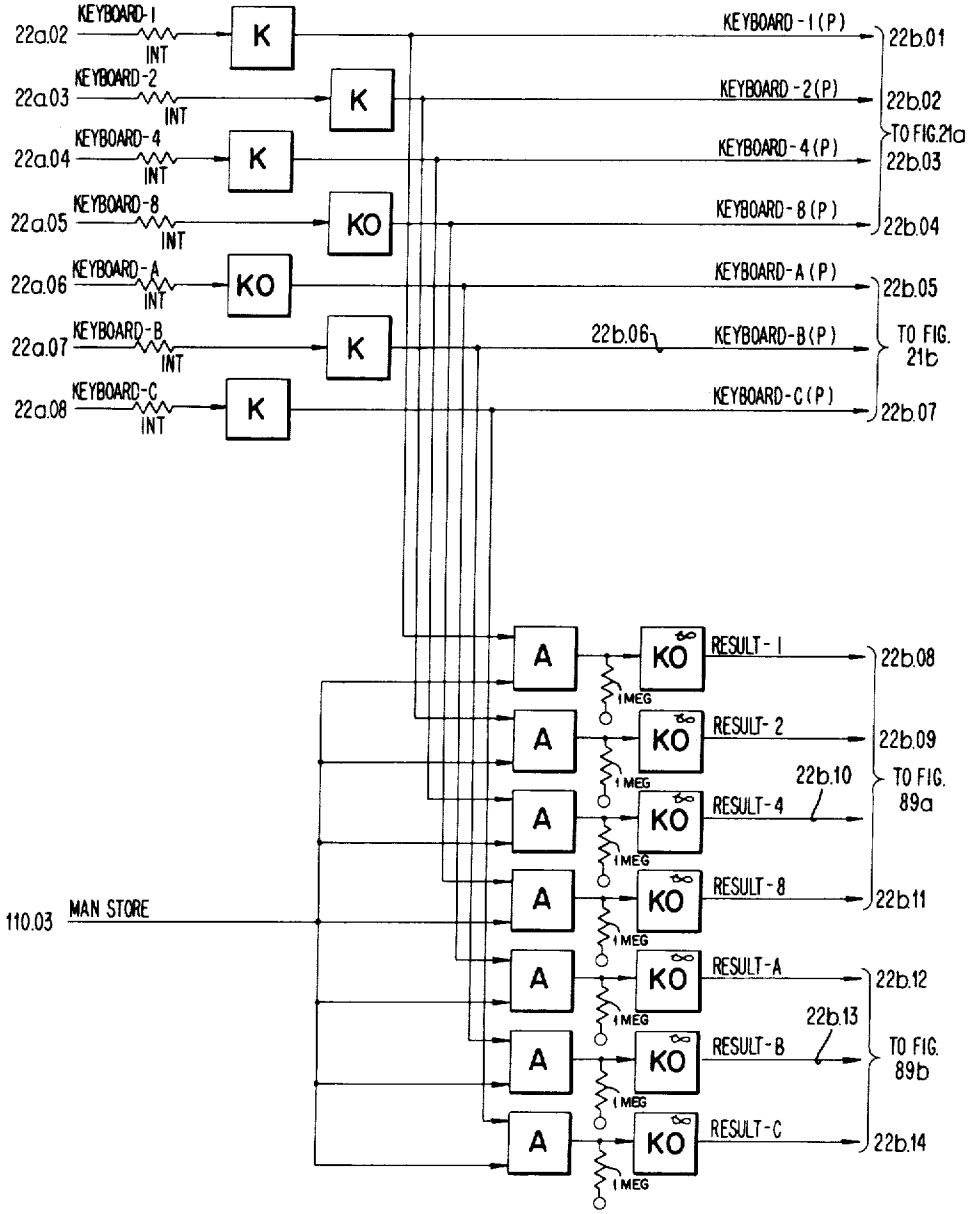
FIG. 22a

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FIG.22b KEYBOARD OUTPUTS



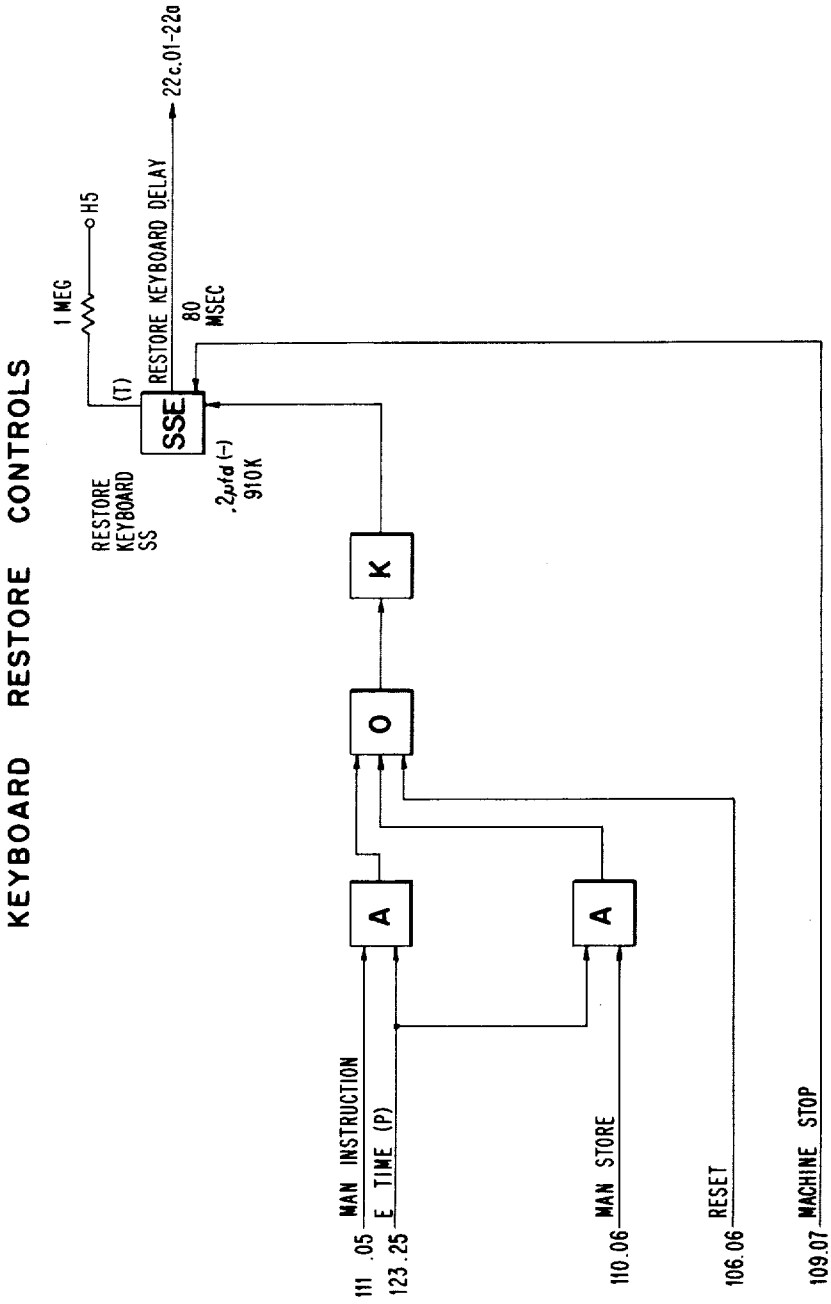


FIG. 22c

-12 CLAMP 139e.08

FIG. 22d

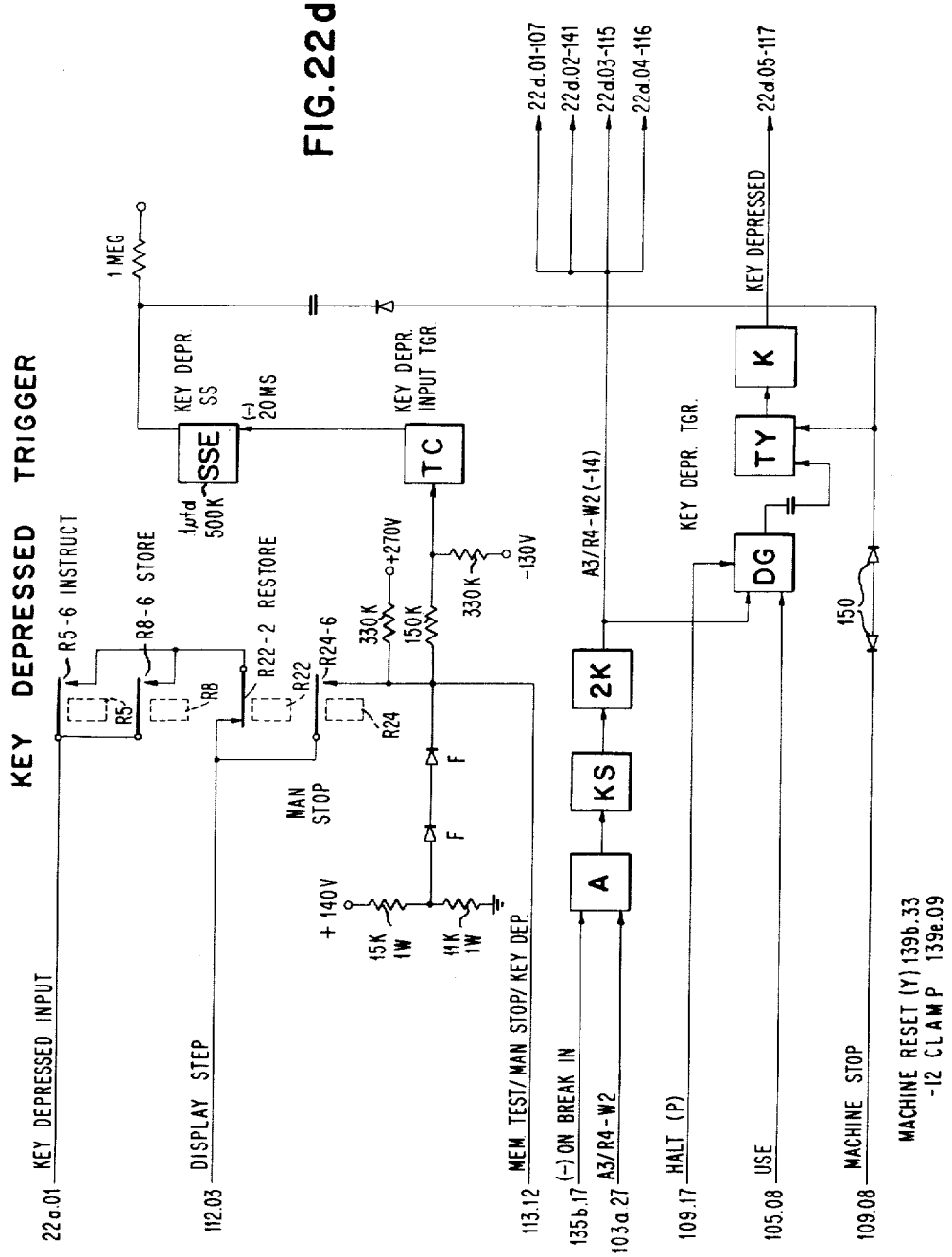

KEY DEPRESSED TRIGGER
22a.01 KEY DEPRESSED INPUT
R5-6 INSTRUCT
R8-6 STORE
R22-2 RESTORE
R24-6
R5
R8
R22
R24
1 MEG
KEY DEPR SS
(-) 20MS
SSE
1μfd 500K
KEY DEPR. INPUT TGR.
TC
+270V
330K
150K
330K
-130V
MAN STOP
+ 140V
15K 1W
11K 1W
F
F
112.03 DISPLAY STEP
113.12 MEM TEST/MAN STOP/KEY DEP
135b.17 (-) ON BREAK IN
103a.27 A3/R4-W2
A
KS
2K
A3/R4-W2(-14)
22d.01-107
22d.02-141
22d.03-115
22d.04-116
KEY DEPR. TGR.
DG
TY
K
KEY DEPRESSED
22d.05-117
150
109.17 HALT (P)
105.08 USE
109.08 MACHINE STOP
MACHINE RESET (Y) 139b.33
-12 CLAMP 139e.09

FIG. 23a

OPERATION ZONE DECODER

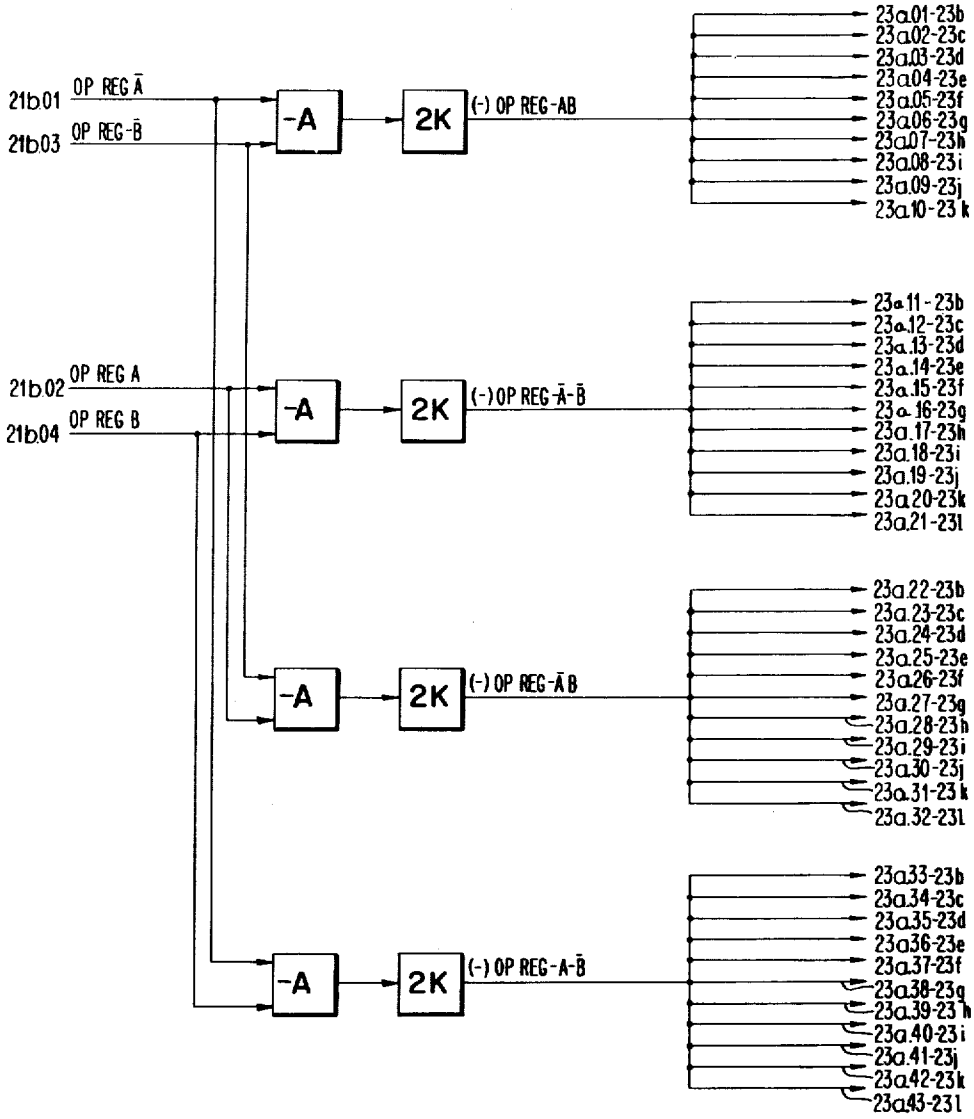


FIG.23b

OPERATION DECODER NO OP, STOP, TR, SEND

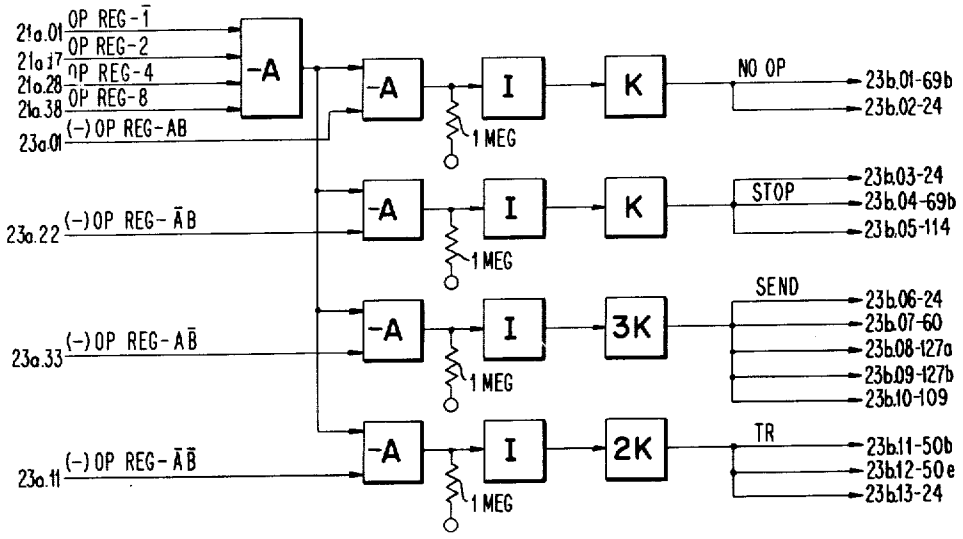


FIG.23c

OPERATION DECODER SET L, TR HI, RWW SEL

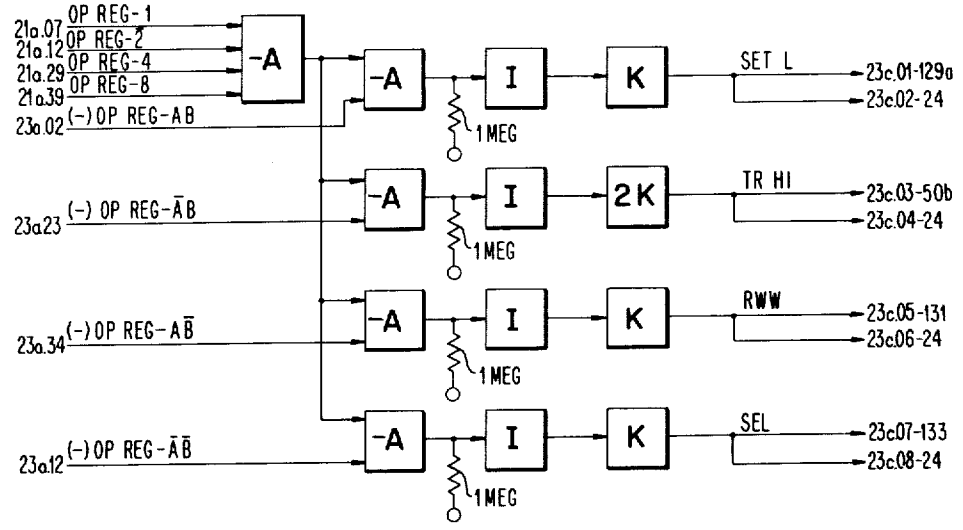


FIG.23d
OPERATION DECODER SHOR, TR EQ, SIGN CTRL.

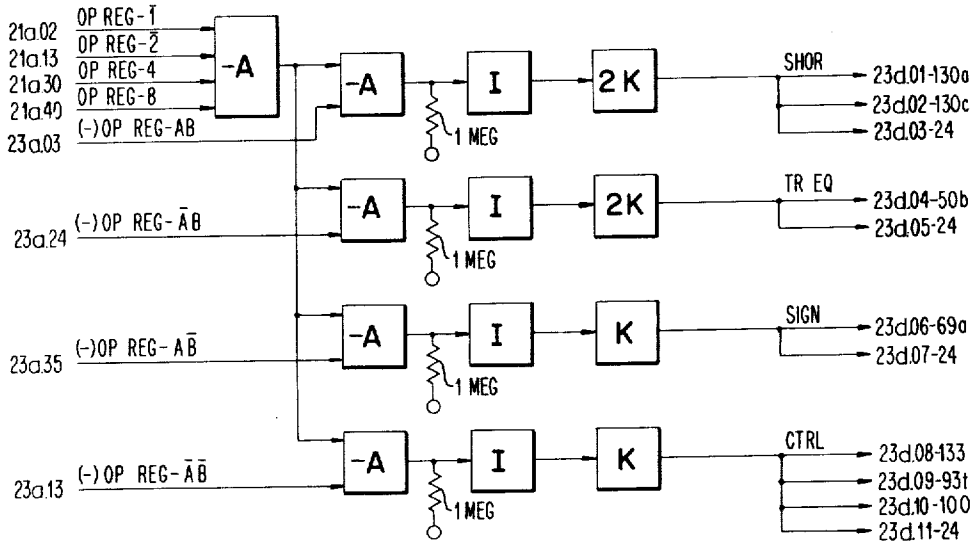
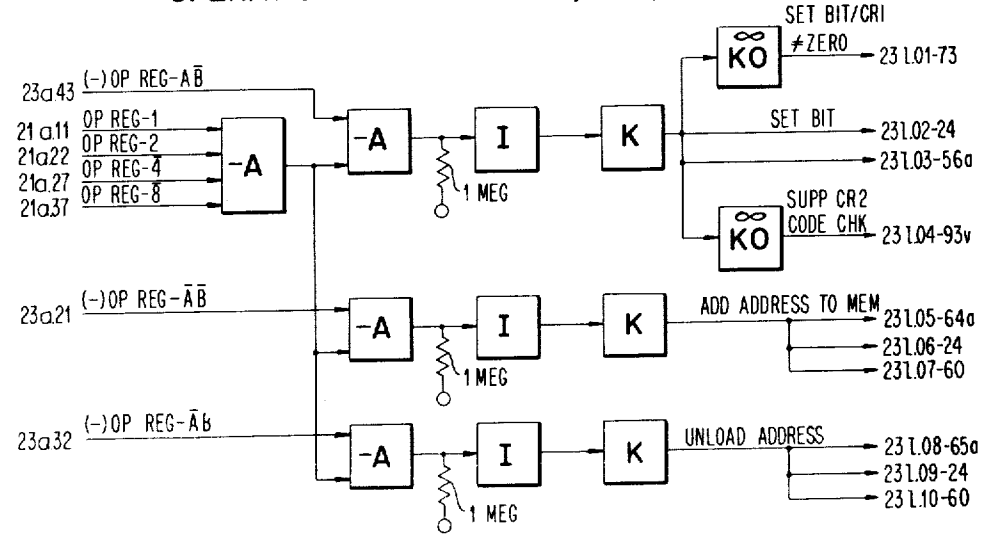


FIG.231
OPERATION DECODER ULA, AAM, SB



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FIG.23e OPERATION DECODER LENG, TR PLS, RCV, COMP

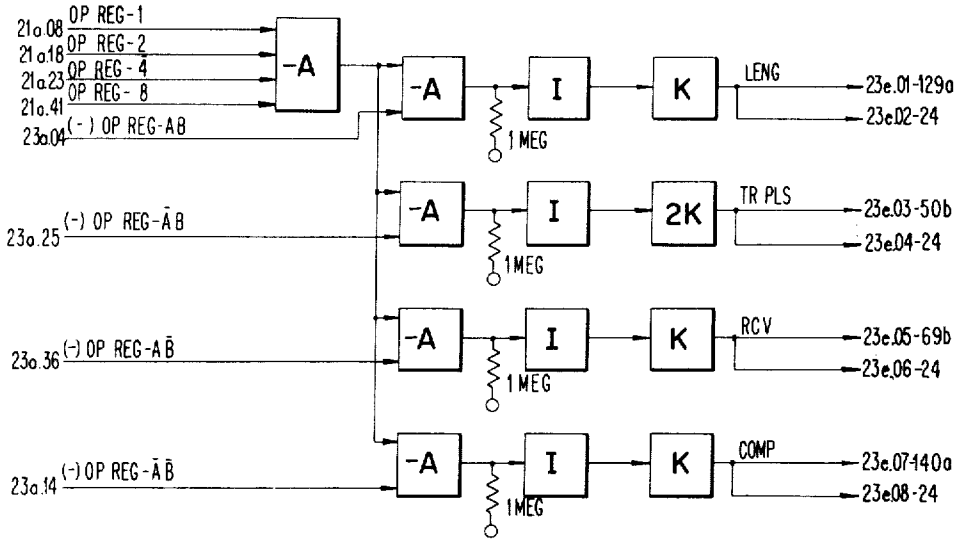
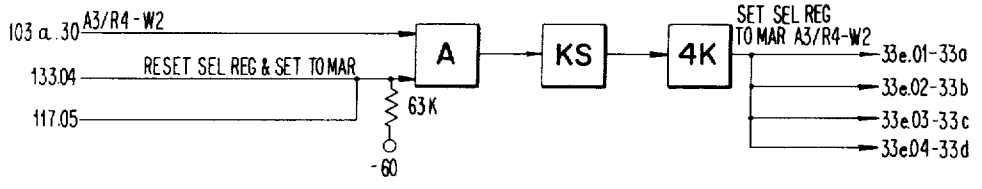


FIG.33e SELECT REGISTER CONTROLS



OPERATION DECODER-ROUND, TR ZRO, MPY, ST PR

FIG. 23f

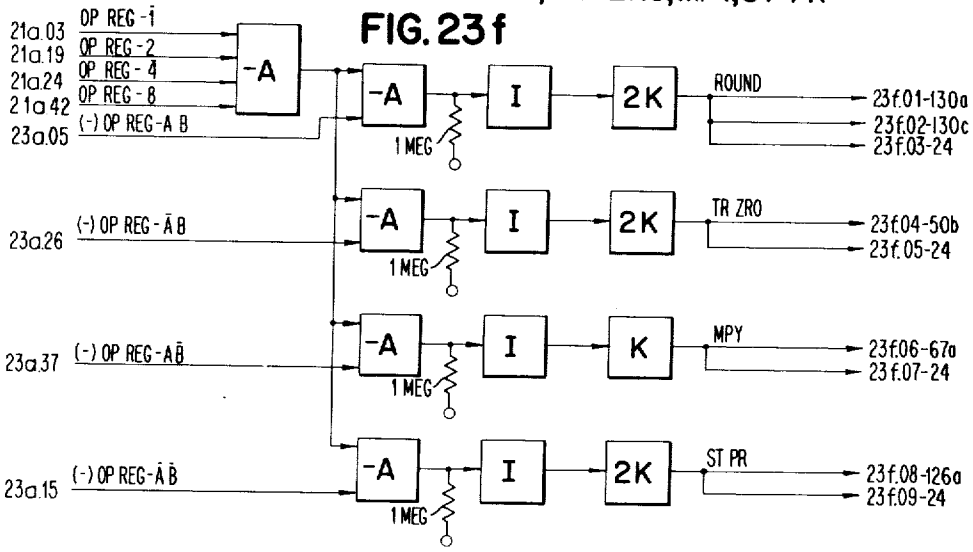
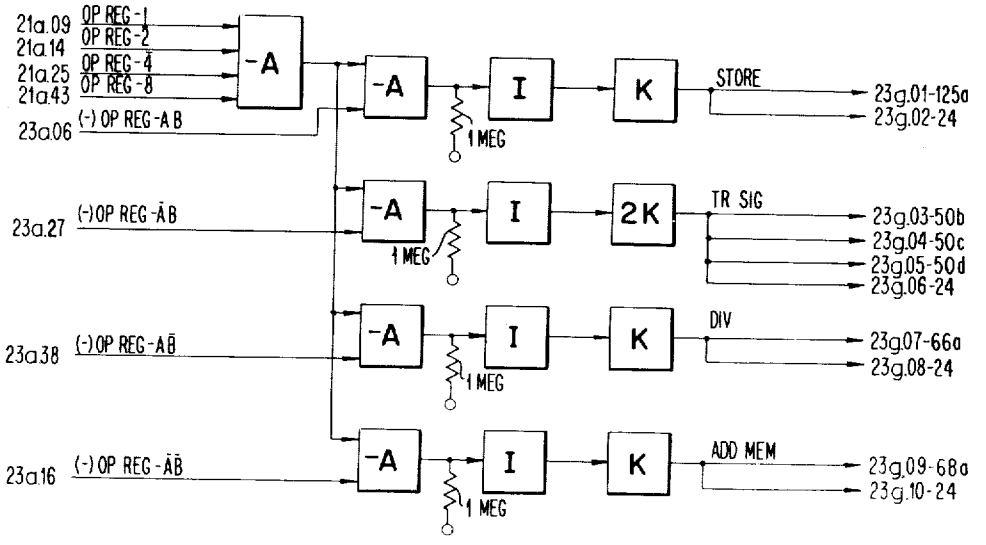


FIG. 23g

OPERATION DECODER STORE, TR SIG, DIV, ADD MEM



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FIG.23h

OPERATION DECODER ADD, SUB, NORM TR, LOAD

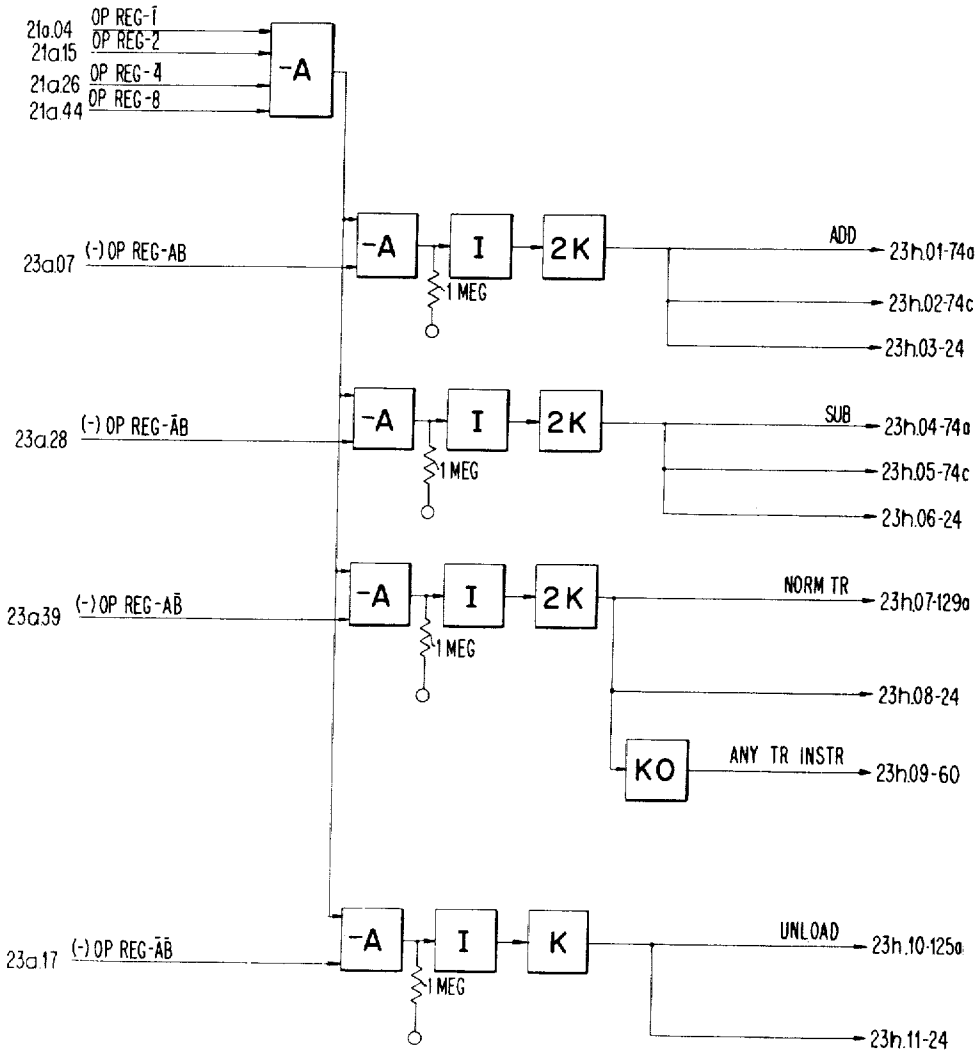


FIG.23i

OPERATION DECODER-R ADD, R SUB, READ, LOAD

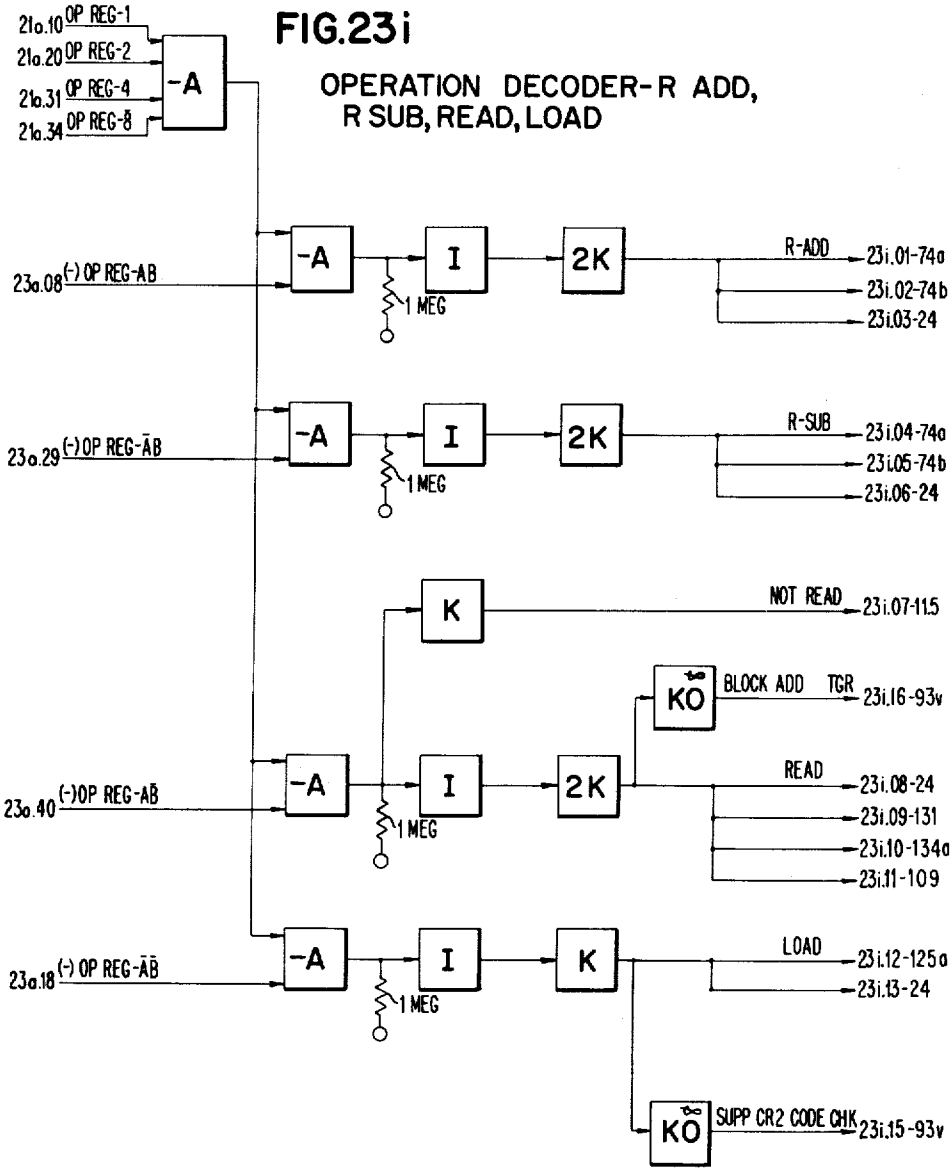
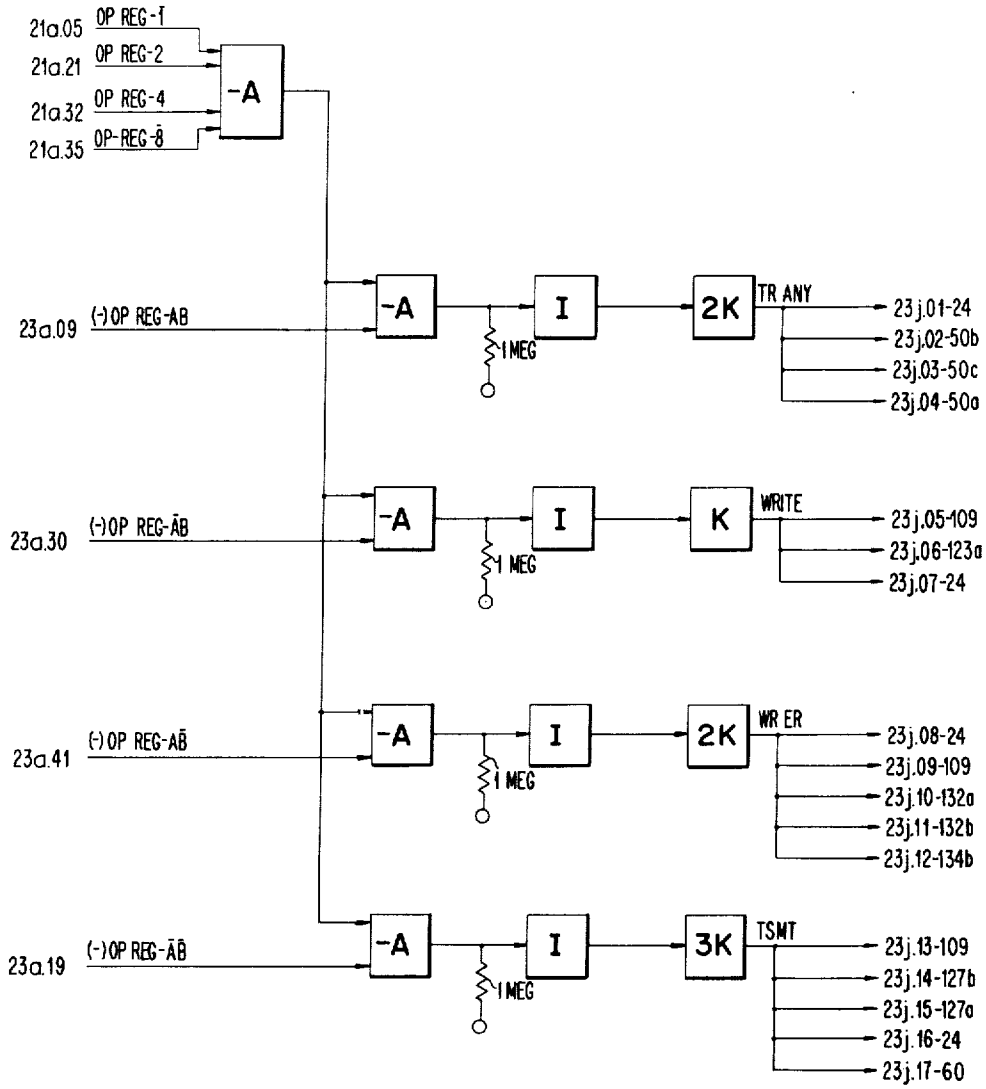


FIG. 23j

OPERATION DECODER-TR ANY, WR ER, TSMT



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FIG. 24 OPERATION CHECK CIRCUITS

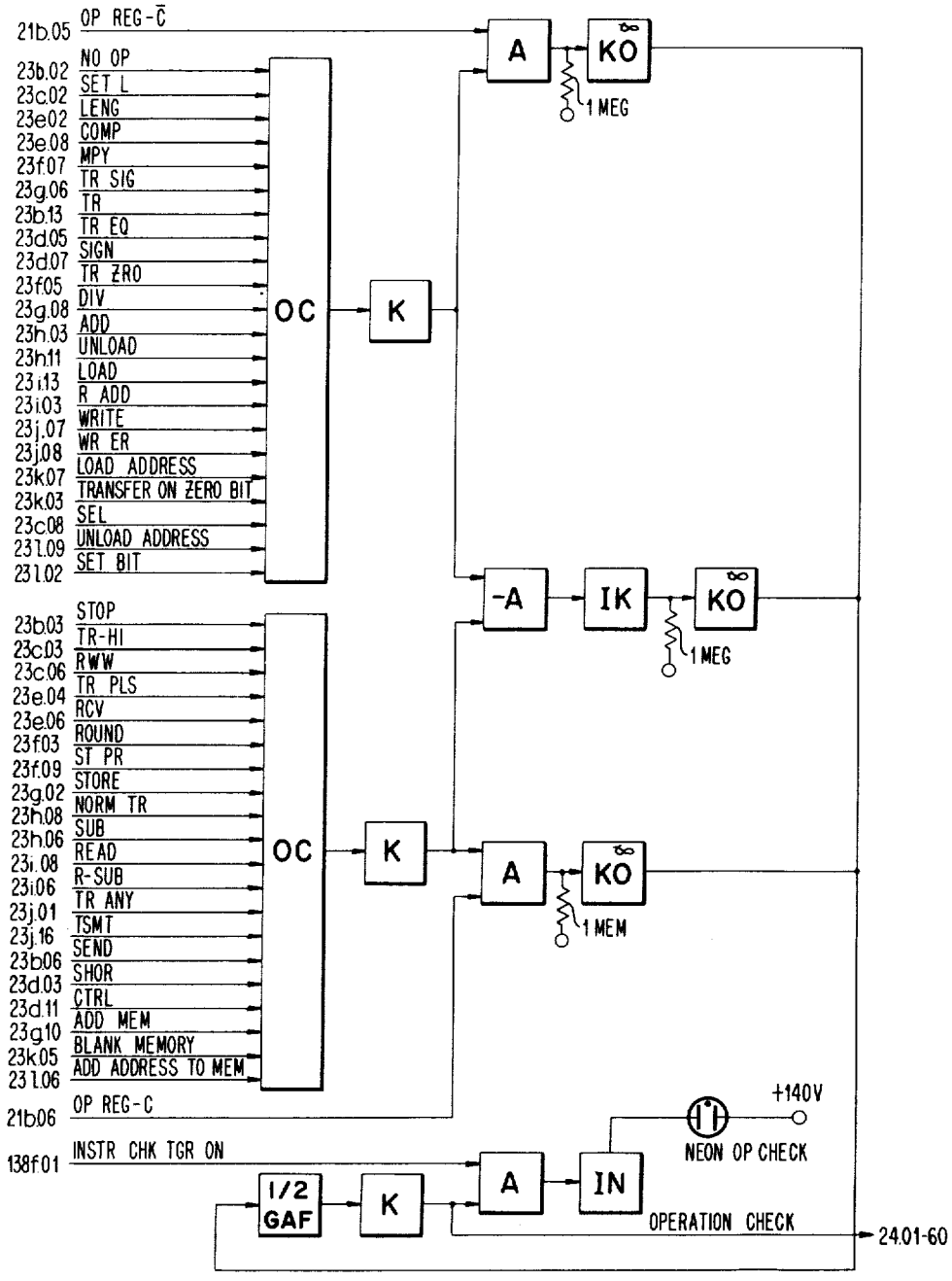


FIG.25a MEMORY ADDRESS SELECTOR KEYS

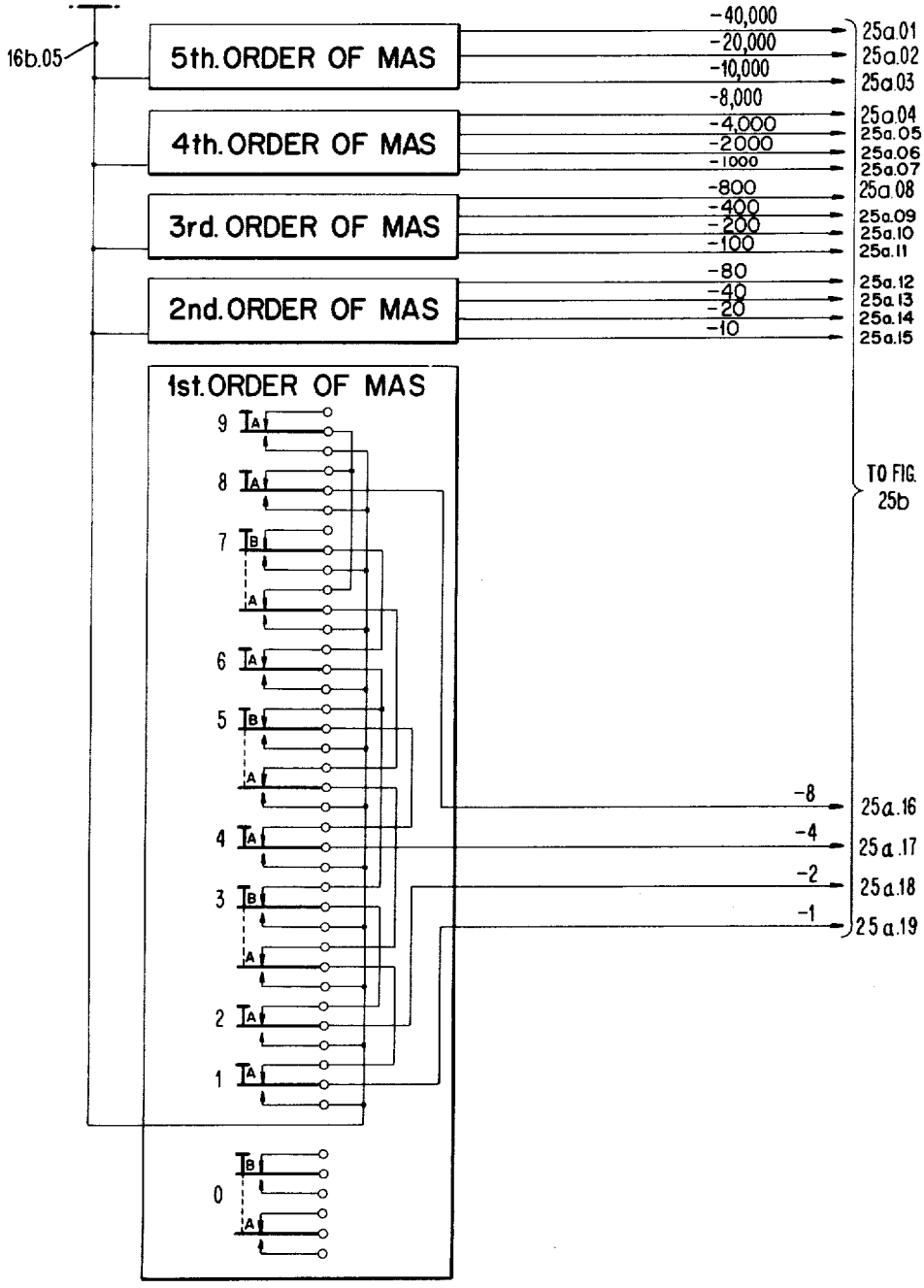


FIG.25b MEMORY ADDRESS SELECTOR KEY OUTPUTS

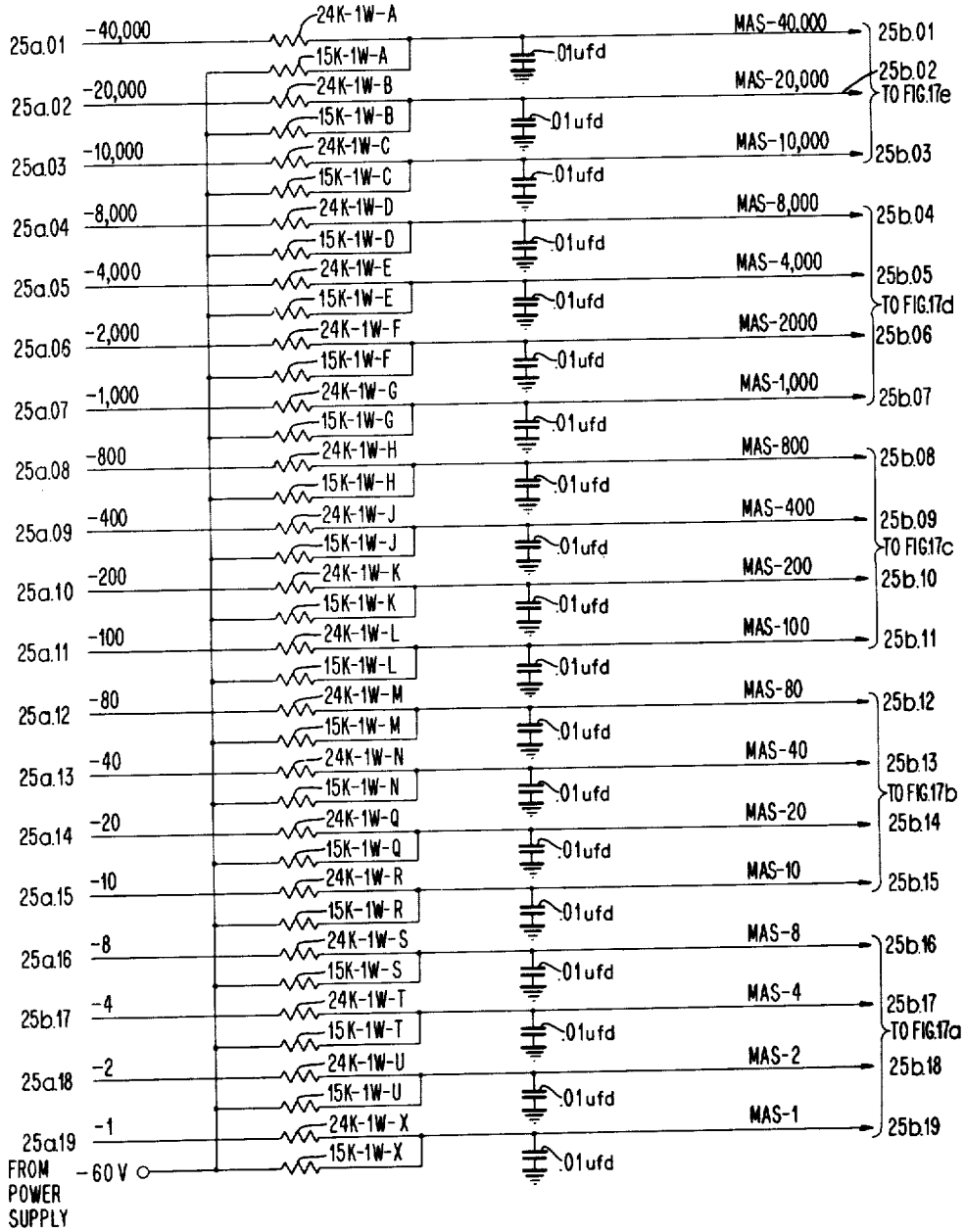


FIG. 26a PARALLEL CHARACTER TRANSMISSION CABLE A CONNECTOR LAYOUT

8 PCT ADDR CHECK 109	7 SMAC-MAR CHECK 28.06	6 SPARE	5 PCT CHECK 50c	4 PCT IND ON 134c	3 SR = 02XX 33f.14	2 SPARE	1 NEON PCT OPEN FIL
16 PCT REQUEST(P) 135b.21	15 PCT READ 135b	14 PCT READY 50c	13 GND	12 MACH STOP 109.03	11 GND	10 READ CALL(P) 138b.10	9 GND
24 GND	23 A1/R2-W1 (P) 104.06	22 GND	21 PCT DISC 134f	20 GND	19 PCT SVC CALL 135a	18 GND	17 SPARE
32 W3-R2 (P) 104.05	31 GND	30 W1-R0 (P) 104.01	29 GND	28 PCT ADDR CHK RESET 109.01	27 GND	26 WRITE CALL(P) 138e.06	25 GND
40 GND	39 WRITE TM 27.05	38 GND	37 CTRL 0000 27.02	36 GND	35 W0-W3 (P) 104.04	34 GND	33 SPARE
48 CTRL 0005 27.13	47 GND	46 CTRL 0004 27.11	45 GND	44 CTRL 0003 27.09	43 GND	42 CTRL 0002 27.07	41 GND
56 GND	55 CTRL 0008 27.19	54 GND	53 CTRL 0007 27.17	52 GND	51 CTRL 0006 27.15	50 GND	49 PCT CHK SMAC
64 SEL REG 2 33a.08	63 GND	62 SEL REG 1 33a.04	61 GND	60 SEL REG 1000's ORD=0 33f.12	59 GND	58 CTRL 0009 27.21	57 GND
72 GND	71 SEL REG 10 33b.04	70 GND	69 SEL REG 8 33a.15	68 GND	67 SEL REG 4 33a.12	66 GND	65 SPARE
80 SEL REG 100 33c.05	79 GND	78 SEL REG 80 33b.13	77 GND	76 SEL REG 40 33b.10	75 GND	74 SEL REG 20 33b.07	73 GND
88 GND	87 SEL REG 800 33c.15	86 GND	85 SEL REG 400 33c.12	84 GND	83 SEL REG 200 33c.08	82 GND	81 SSR-1(P) 55a.01
96 MAR/MASR 40(P) 29a.04	95 GND	94 MAR/MASR 20(P) 29a.03	93 GND	92 MAR/MASR 10(P) 29a.02	91 GND	90 MAR/MASR 0/5 29a.01	89 GND
104 GND	103 MAR/MASR 200(P) 29a.07	102 GND	101 MAR/MASR 100(P) 29a.06	100 GND	99 MAR/MASR 80 (P) 29a.05	98 GND	97 SSR-2(P) 55a.07
112 MAR/MASR 2000(P) 29b.03	111 GND	110 MAR/MASR 1,000(P) 29b.02	109 GND	108 MAR/MASR 800(P) 29b.01	107 GND	106 MAR/MASR 400(P) 29a.08	105 GND
120 GND	119 MAR/MASR 10,000(P) 29b.06	118 GND	117 MAR/MASR 8,000(P) 29b.05	116 GND	115 MAR/MASR 4,000(P) 29b.04	114 GND	113 SPARE
128 SMAC 10 17b	127 GND	126 SMAC 0/5 17a	125 GND	124 MAR/MASR 40,000(P) 29b.08	123 GND	122 MAR/MASR 20,000(P) 29b.07	121 GND
136 GND	135 SMAC 80 17b	134	133 SMAC 40 17b	132	131 SMAC 20 17b	130	129 DSU SELECTED 132b
144 SMAC 800 17c	143 GND	142 SMAC 400 17c	141 GND	140 SMAC 200 17c	139 GND	138 SMAC 100 17c	137 GND
152 GND	151 SMAC 4000 17d	150 GND	149 SMAC 2000 17d	148 GND	147 SMAC 1000 17d	146 GND	145 SPARE
160 SMAC 40,000 17e	159 GND	158 SMAC 20,000 17e	157 GND	156 SMAC 10,000 17e	155 GND	154 SMAC 8,000 17d	153 GND

FIG. 26b

I/O SIGNAL CABLE CONNECTOR LAYOUT SP CONNECTOR RECEPTACLE - WIRING SIDE

8 GND	7 READY 50c	6 GND	5 I/O SYNC PULSE 134f.01	4 GND	3 SPARE	2 GND	1 SPARE
16 READ BUS 8 48	15 GND	14 READ BUS 4 48	13 GND	12 READ BUS 2 48	11 GND	10 READ BUS 1 48	9 GND
24 GND	23 END R/W(P) 93t.01	22 GND	21 READ BUS C 48	20 GND	19 READ BUS B 48	18 GND	17 READ BUS A 48
32 WR BUS 8 58.41	31 GND	30 WR BUS 4 58.46	29 GND	28 WR BUS 2 58.51	27 GND	26 WR BUS 1 58.56	25 GND
40 GND	39 PREPARE TO READ (P) 93t.10	38 GND	37 WR BUS C 58.04	36 GND	35 WR BUS B 58.21	34 GND	33 WR BUS A 58.36
48 WR TM 27.04	47 GND	46 CTRL 0000 27.01	45 GND	44 WR CALL (P) 138e.05	43 GND	42 RD CALL (P) 138b.07	41 GND
56 GND	55 CTRL 0005 27.12	54 GND	53 CTRL 0004 27.10	52 GND	51 CTRL 0003 27.08	50 GND	49 CTRL 0002 27.06
64 CTRL 0009 27.20	63 GND	62 CTRL 0008 27.18	61 GND	60 CTRL 0007 27.16	59 GND	58 CTRL 0006 27.14	57 GND
72 GND	71 I/O OPEN FIL	70 GND	69 I/O IND ON 134c	68 GND	67 R/W ERROR 134c	66 GND	65 RECORD ERROR 134c
80 READ DISC 93t	79 GND	78 READ RESPONSE 93t	77 GND	76 WRITE DISC 93t	75 GND	74 WRITE RESPONSE 93t	73 GND
88 DC RETURN	87 GND	86 GND	85 GND	84 GND	83 GND	82 GND	81 DC RETURN
96 SEL REG 80 33b.12	95 SEL REG 40 33b.09	94 SEL REG 20 33b.06	93 SEL REG 10 33b.03	92 SEL REG 8 33a.14	91 SEL REG 4 33a.11	90 SEL REG 2 33a.07	89 SEL REG 1 33a.03
104 SEL REG 8000 33d.08	103 SEL REG 4000 33d.06	102 SEL REG 2000 33d.04	101 SEL REG 1000 33d.02	100 SEL REG 800 33c.14	99 SEL REG 400 33c.11	98 SEL REG 200 33c.07	97 SEL REG 100 33c.04
112 SPARE	111 SPARE	110 SPARE	109 SPARE	108 SPARE	107 SPARE	106 SPARE	105 SR 1000 ORDER = 0 33f.11
120 SPARE	119 SPARE	118 SPARE	117 SPARE	116 SPARE	115 SPARE	114 SPARE	113 SPARE
128 SPARE	127 SPARE	126 SPARE	125 SPARE	124 SPARE	123 SPARE	122 SPARE	121 SPARE
136 SPARE	135 SPARE	134 SPARE	133 SPARE	132 SPARE	131 SPARE	130 SPARE	129 SPARE
144	143	142	141 SPARE	140 SPARE	139	138	137
152	151	150	149	148	147	146	145
160	159	158	157	156	155	154	153

FIG. 27 CONTROL ADDRESS DECODER

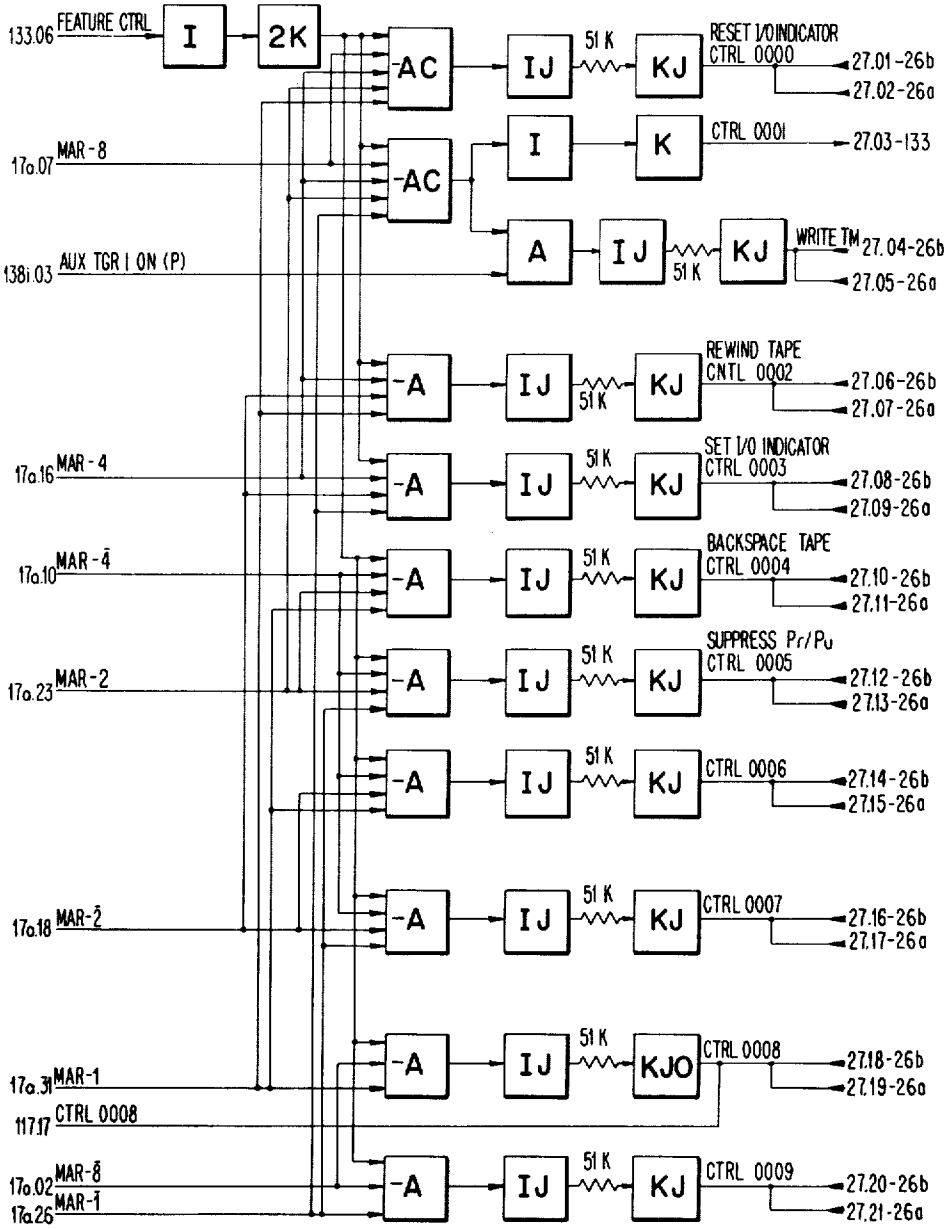


FIG. 28

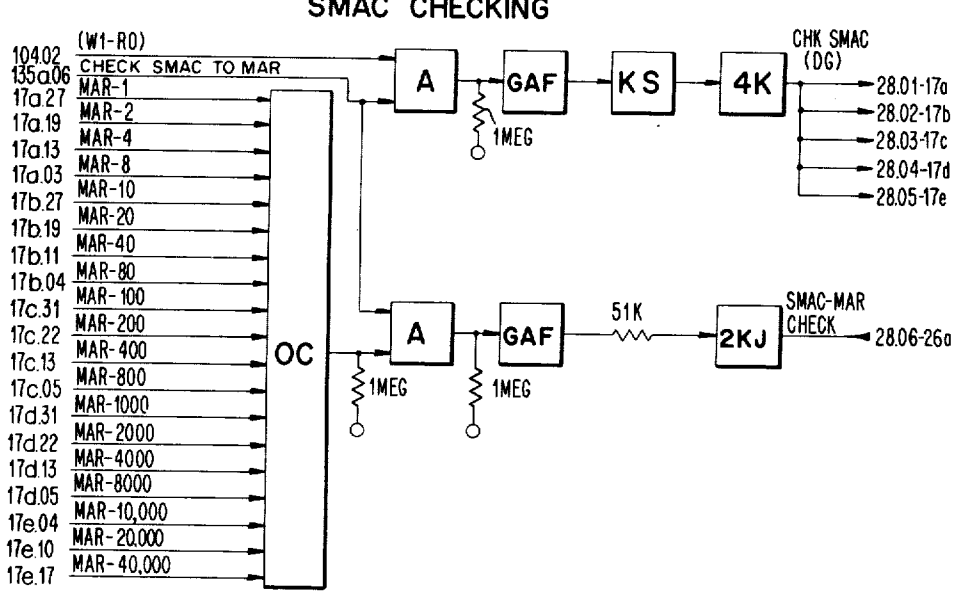


FIG. 31e

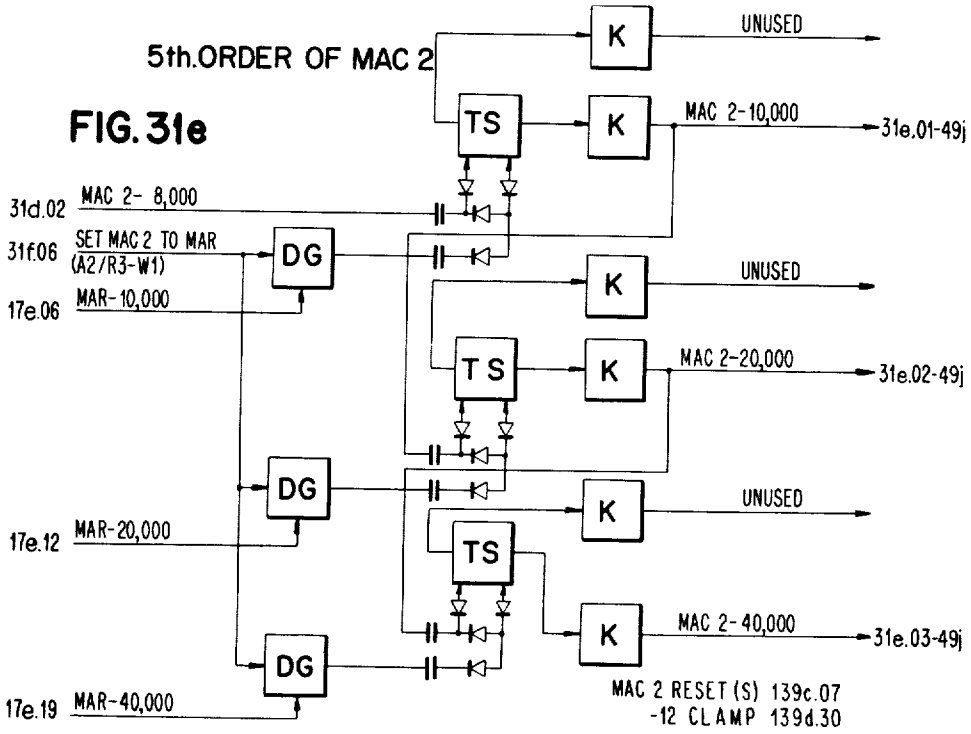
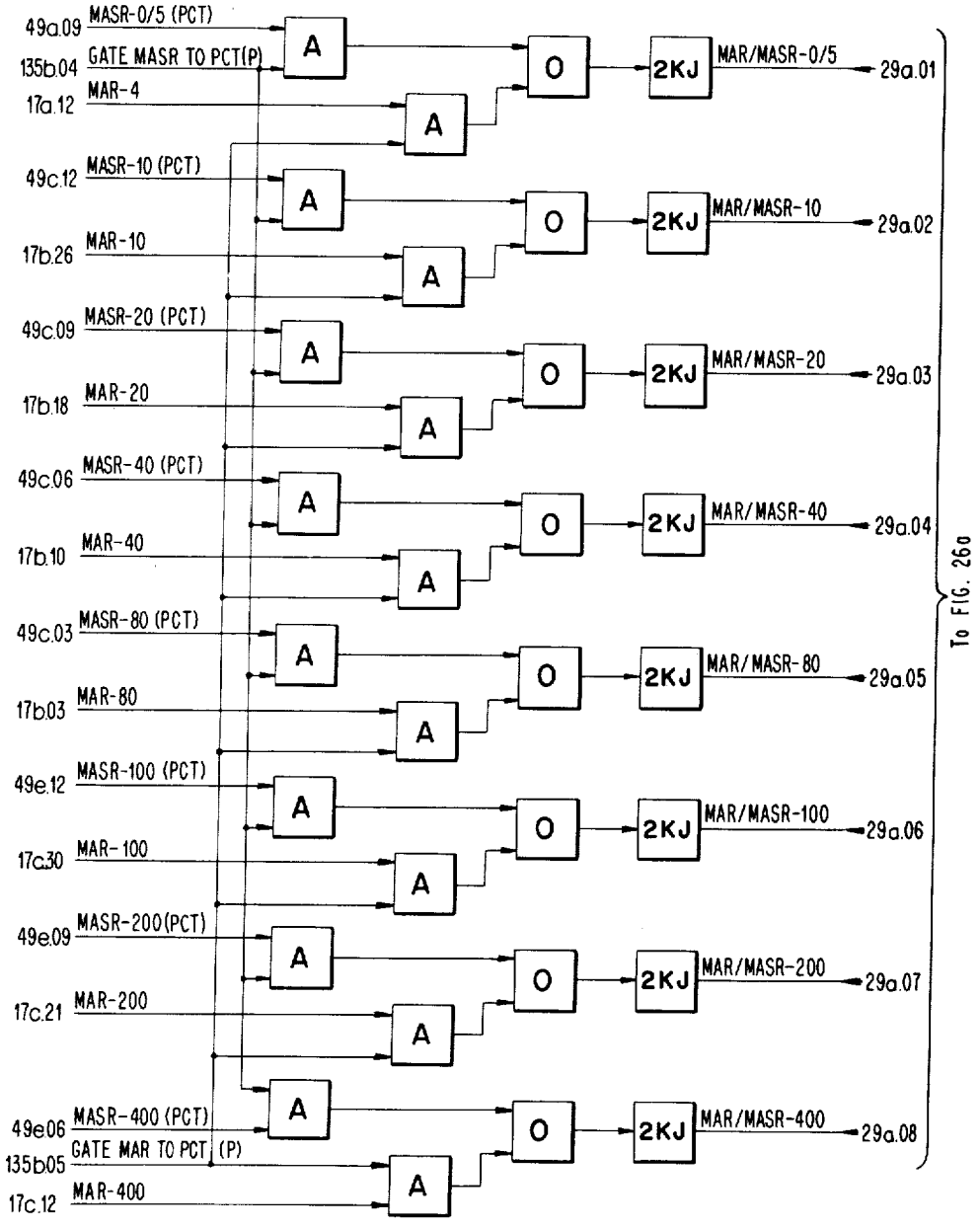


FIG.29a MASR/MAR TO DSU POWERING



MASR/MAR TO DSU POWERING

FIG.29b

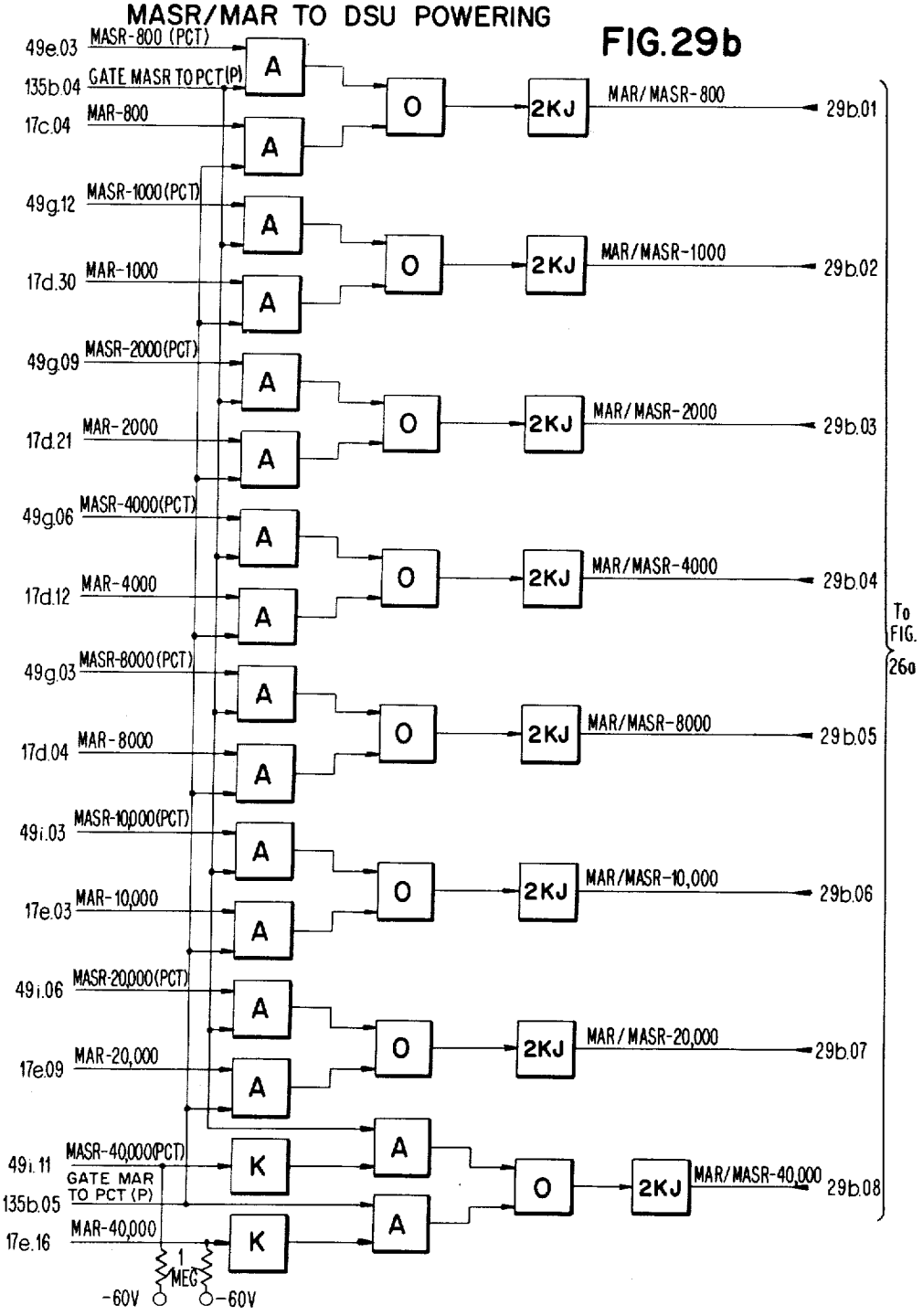
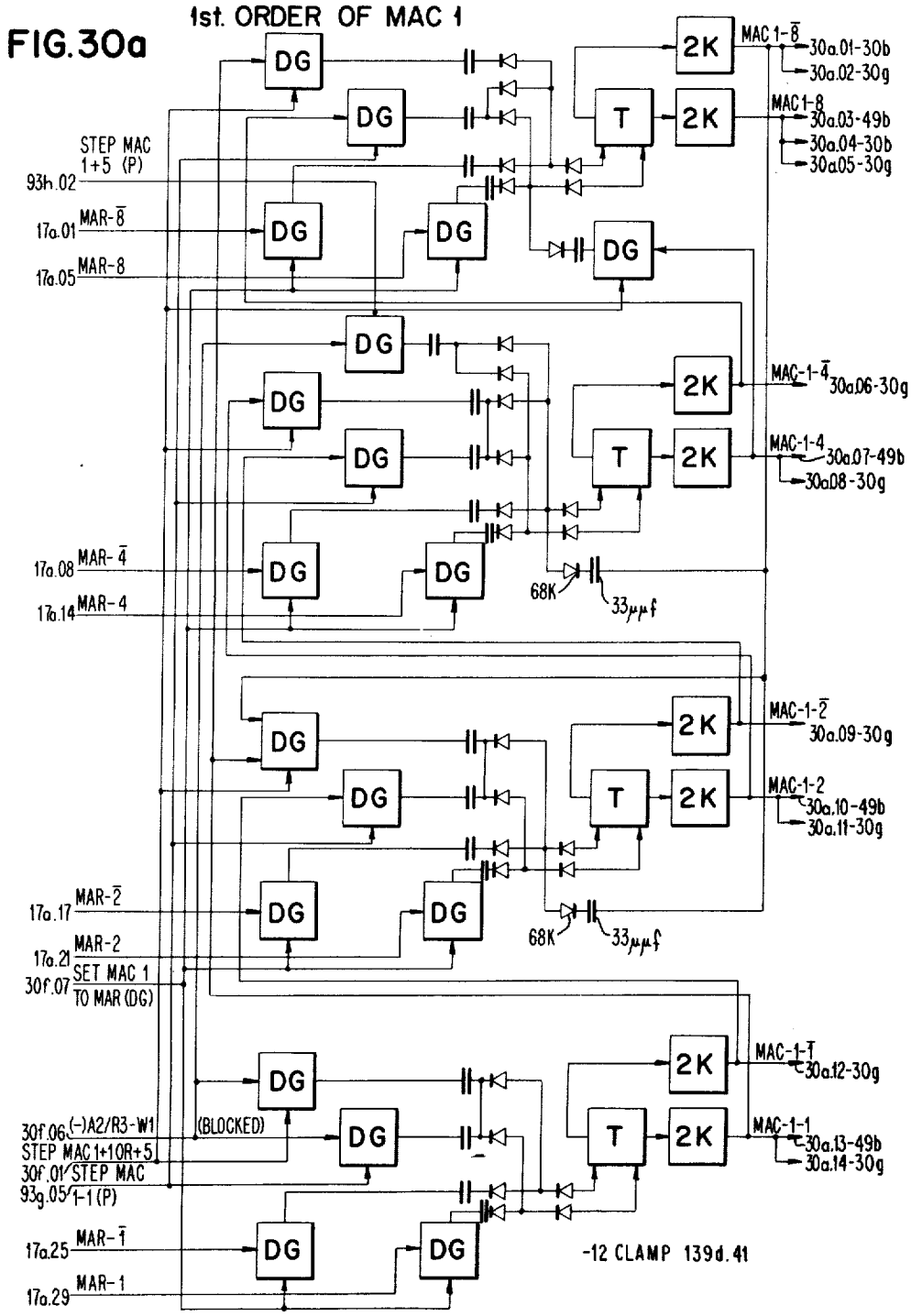


FIG.30a


1st. ORDER OF MAC 1
DG
2K
T
MAC 1-8̄
30a.01-30b
30a.02-30g
MAC 1-8
30a.03-49b
30a.04-30b
30a.05-30g
STEP MAC 1+5 (P)
93h.02
17a.01 MAR-8̄
17a.05 MAR-8
MAC-1-4̄
30a.06-30g
MAC-1-4
30a.07-49b
30a.08-30g
17a.08 MAR-4̄
17a.14 MAR-4
68K
33μμf
MAC-1-2̄
30a.09-30g
MAC-1-2
30a.10-49b
30a.11-30g
17a.17 MAR-2̄
17a.21 MAR-2
30f.07 SET MAC 1 TO MAR (DG)
MAC-1-1̄
30a.12-30g
MAC-1-1
30a.13-49b
30a.14-30g
30f.06 (-)A2/R3-W1
STEP MAC 1+10R+5
30f.01 STEP MAC
93g.05 1-1 (P)
(BLOCKED)
17a.25 MAR-1̄
17a.29 MAR-1
-12 CLAMP 139d.41

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FIG. 30b

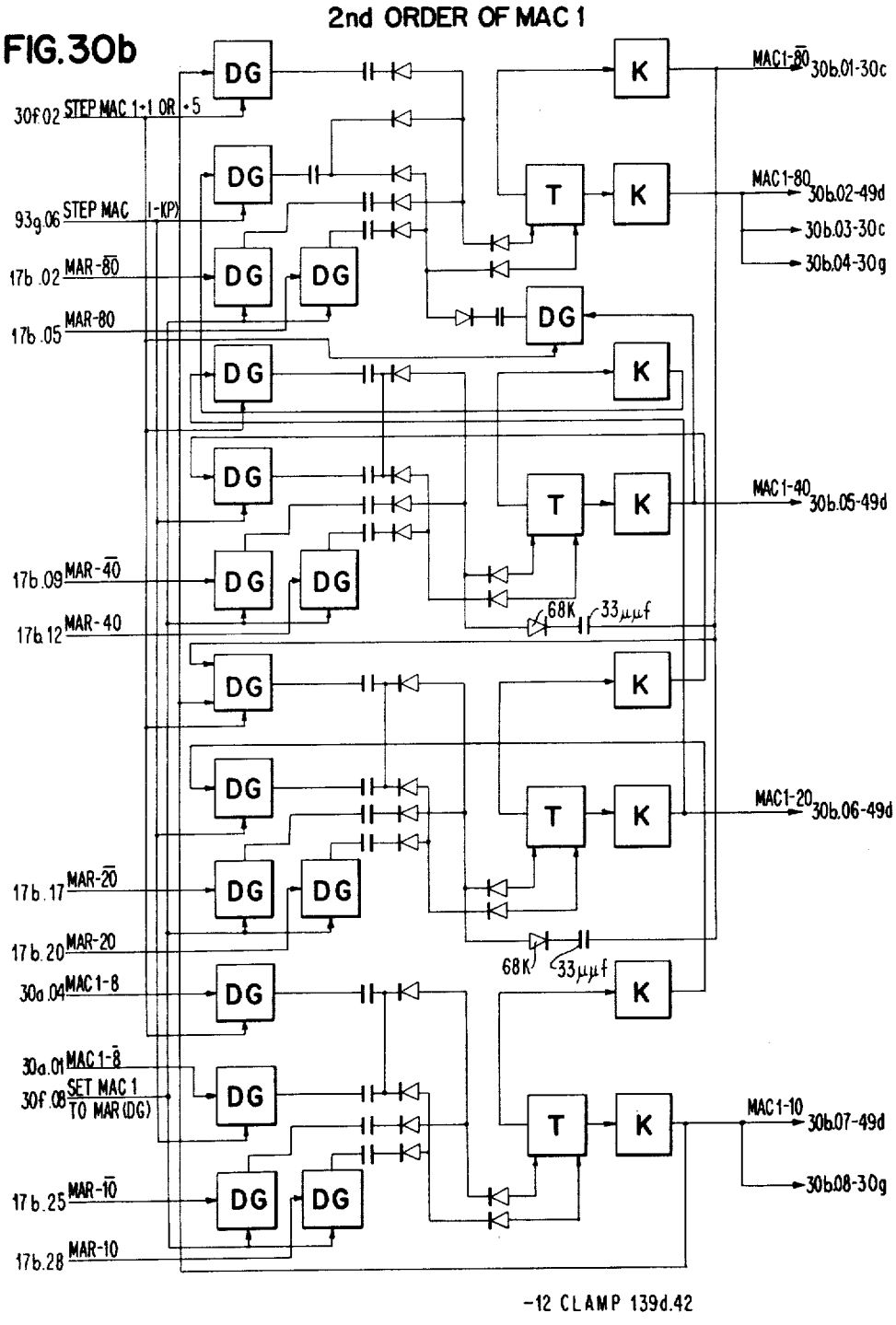
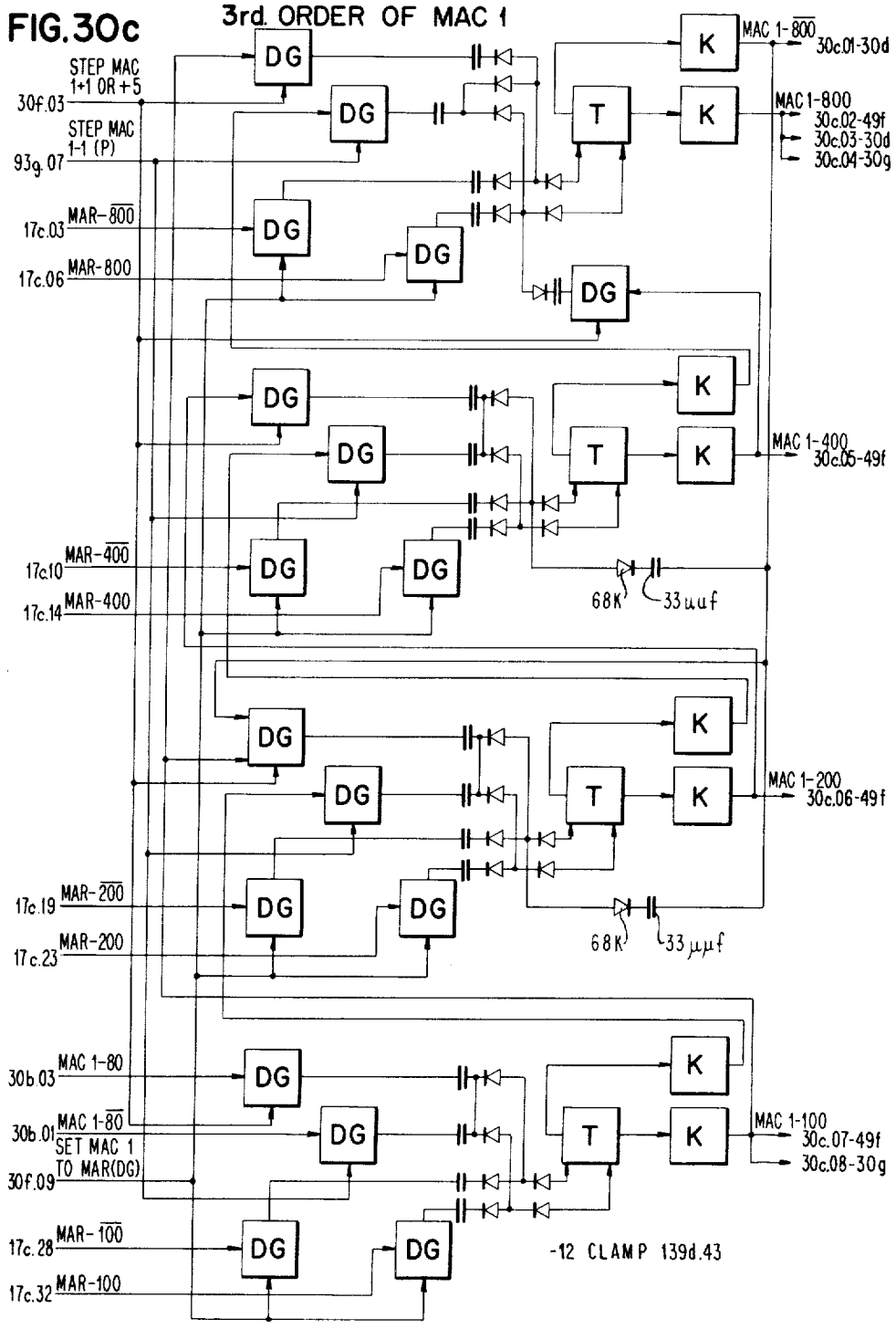


FIG. 30c


3rd. ORDER OF MAC 1
STEP MAC 1+1 OR +5
30f.03
STEP MAC 1-1 (P)
93g.07
17c.03 MAR-800
17c.06 MAR-800
17c.10 MAR-400
17c.14 MAR-400
17c.19 MAR-200
17c.23 MAR-200
30b.03 MAC 1-80
30b.01 MAC 1-80
SET MAC 1 TO MAR(DG)
30f.09
17c.28 MAR-100
17c.32 MAR-100
DG
K
T
MAC 1-800
30c.01-30d
MAC 1-800
30c.02-49f
30c.03-30d
30c.04-30g
MAC 1-400
30c.05-49f
MAC 1-200
30c.06-49f
MAC 1-100
30c.07-49f
30c.08-30g
68K
33 μμf
-12 CLAMP 139d.43

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FIG. 30d

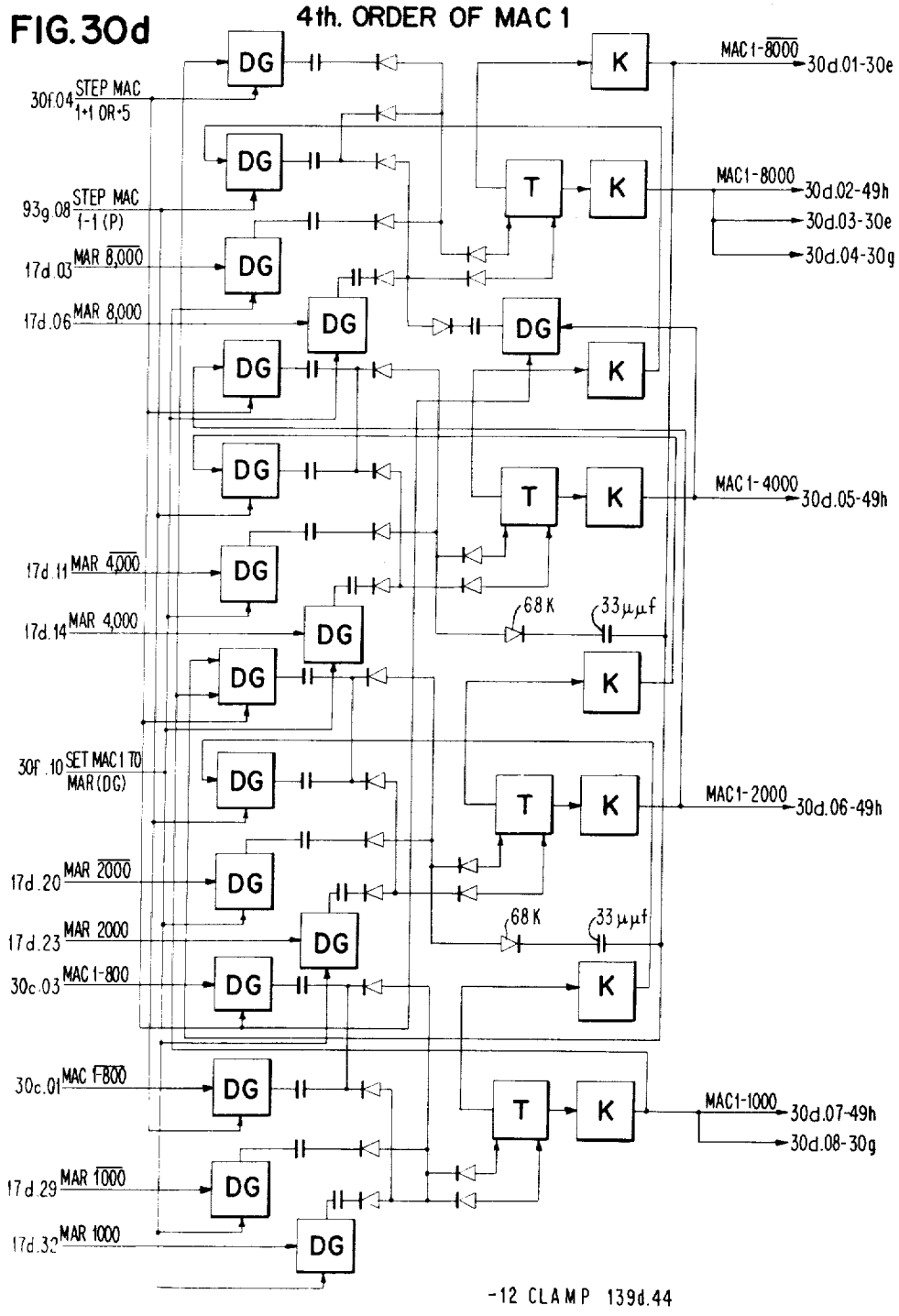
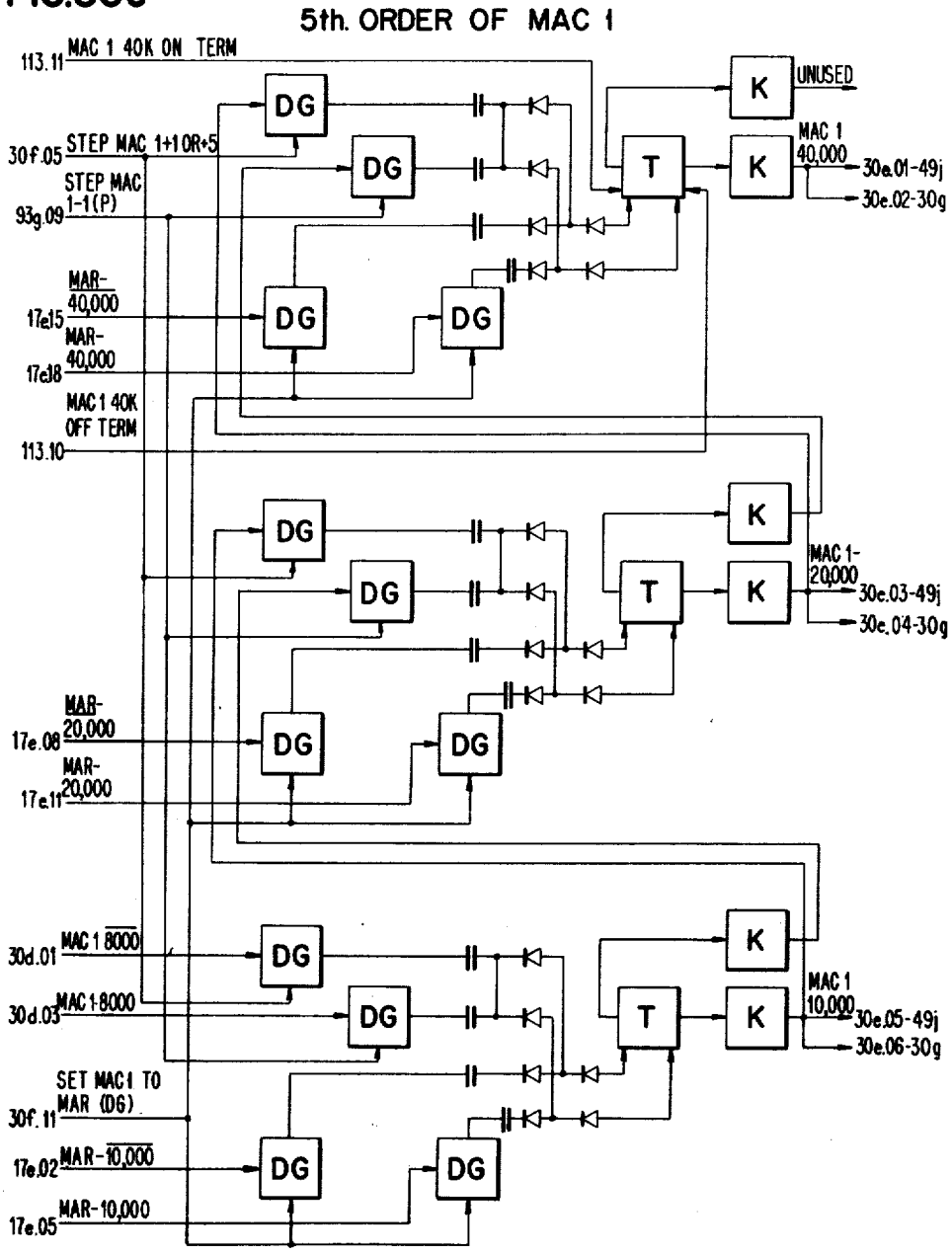


FIG.30e



-12 CLAMP 139d.45

FIG. 30f

MAC 1 CONTROLS

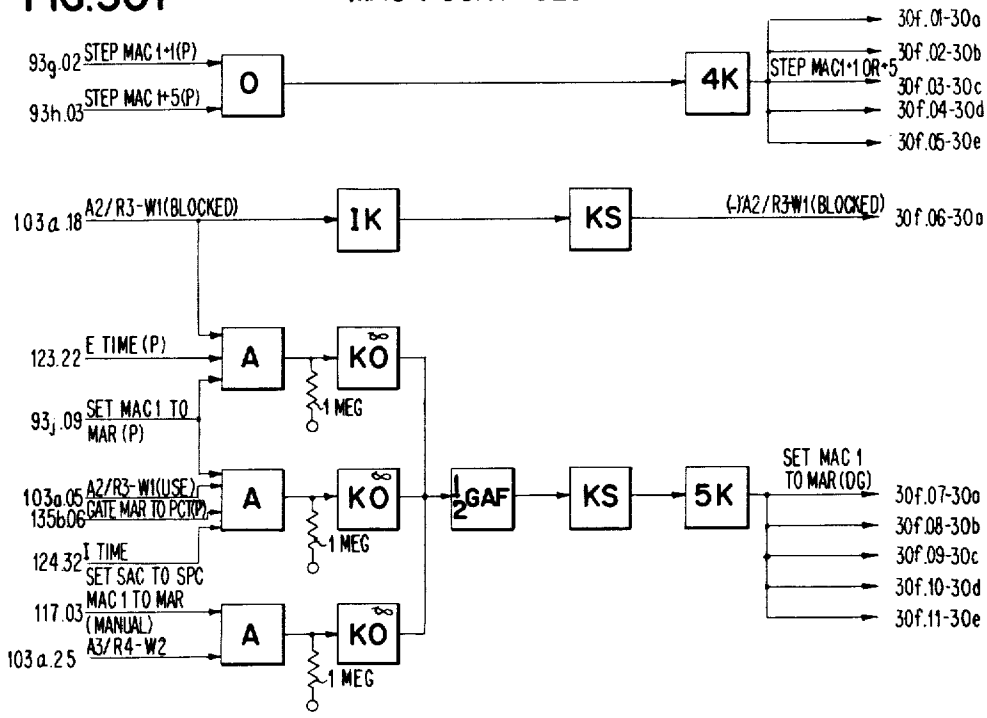


FIG. 31f

MAC 2 CONTROLS

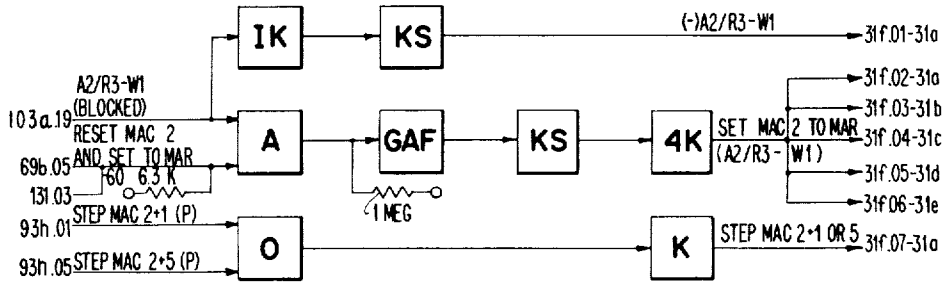
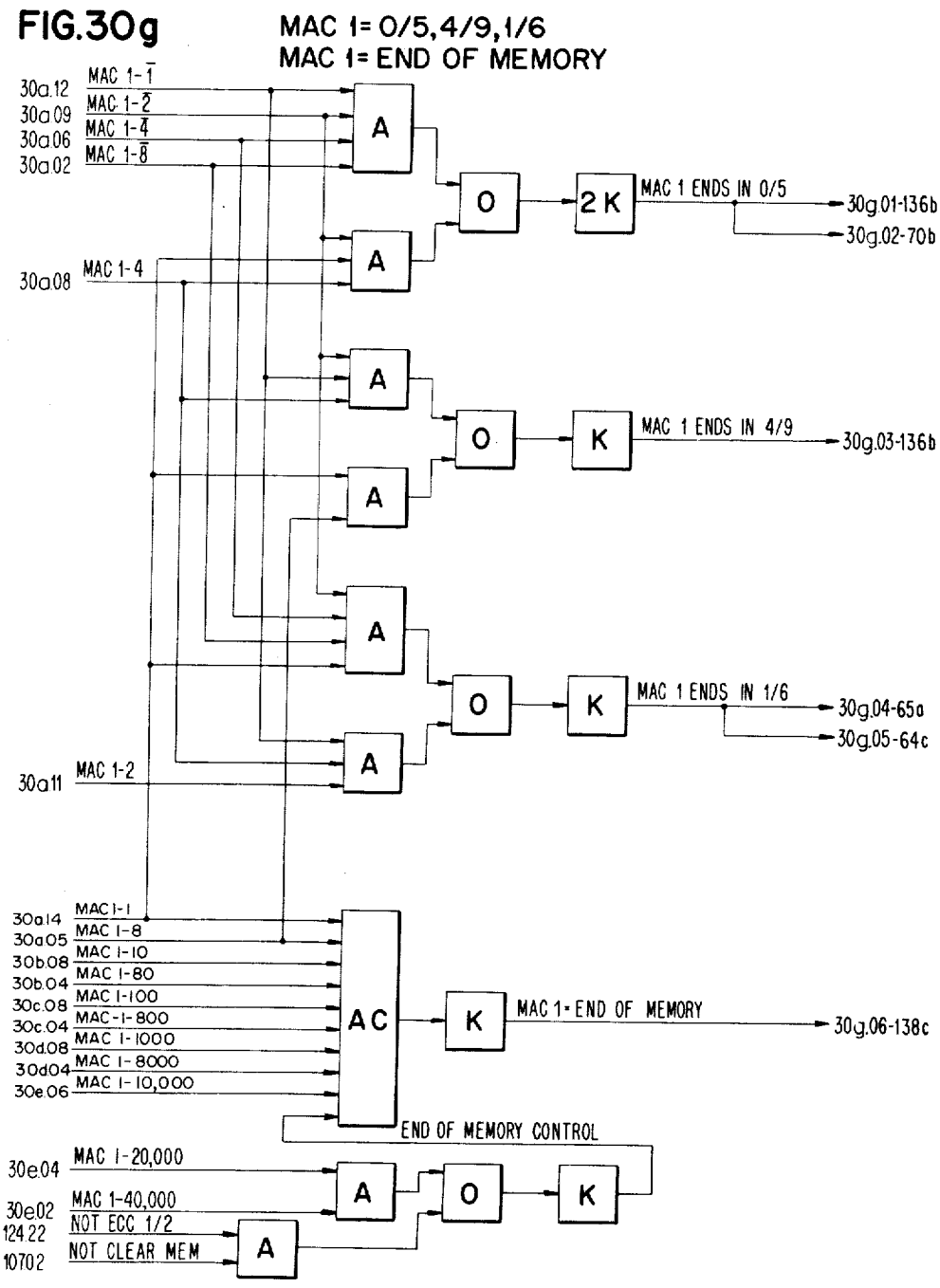


FIG.30g


MAC 1= 0/5,4/9,1/6
MAC 1= END OF MEMORY
30a.12 MAC 1-1
30a.09 MAC 1-2
30a.06 MAC 1-4
30a.02 MAC 1-8
A
O
2K
MAC 1 ENDS IN 0/5
30g.01-136b
30g.02-70b
30a.08 MAC 1-4
A
A
O
K
MAC 1 ENDS IN 4/9
30g.03-136b
A
A
O
K
MAC 1 ENDS IN 1/6
30g.04-65a
30g.05-64c
A
30a.11 MAC 1-2
30a.14 MAC 1-1
30a.05 MAC 1-8
30b.08 MAC 1-10
30b.04 MAC 1-80
30c.08 MAC 1-100
30c.04 MAC 1-800
30d.08 MAC 1-1000
30d.04 MAC 1-8000
30e.06 MAC 1-10,000
AC
K
MAC 1-END OF MEMORY
30g.06-138c
END OF MEMORY CONTROL
30e.04 MAC 1-20,000
30e.02 MAC 1-40,000
124.22 NOT ECC 1/2
1070.2 NOT CLEAR MEM
A
A
O
K

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FIG. 31a

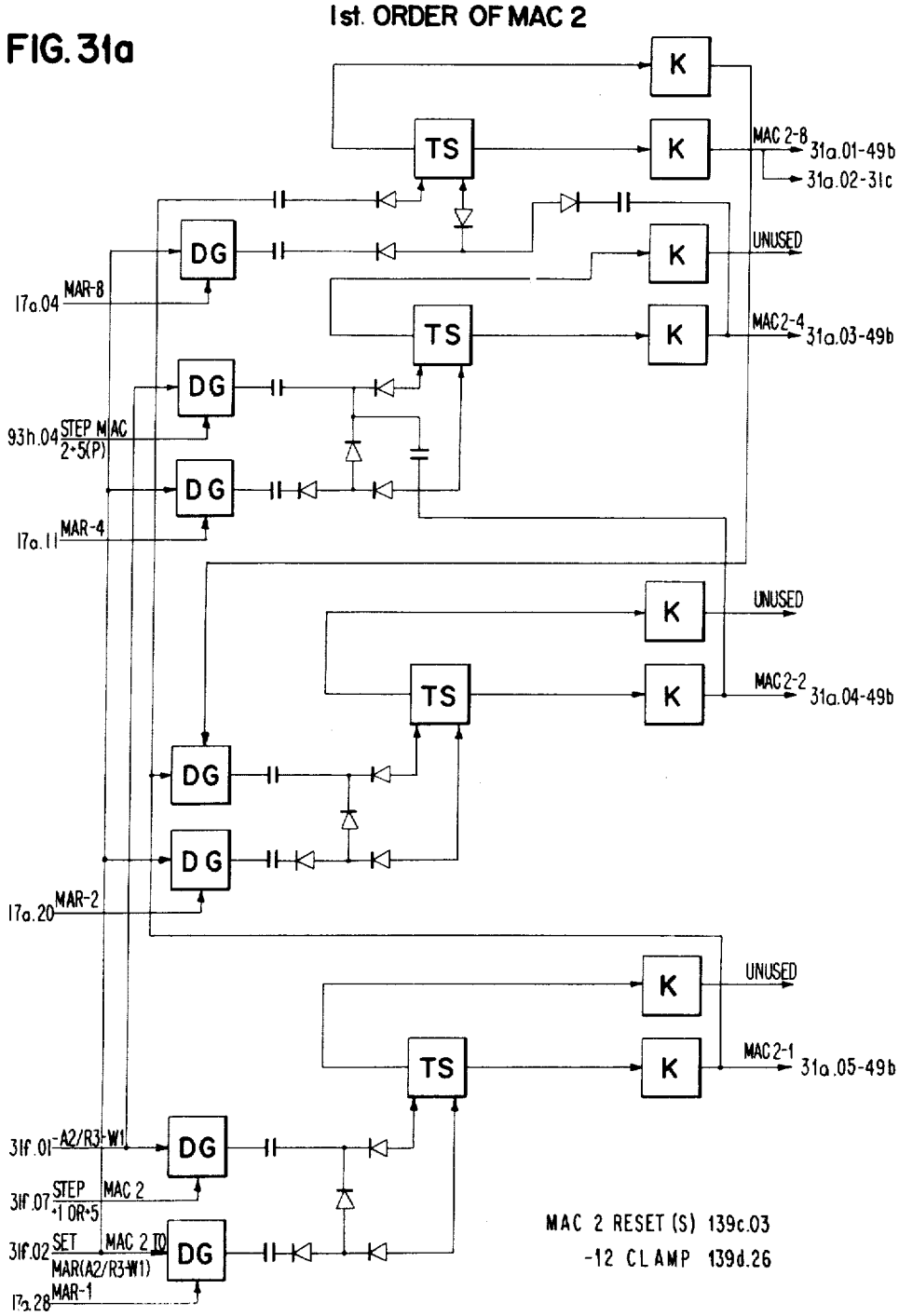
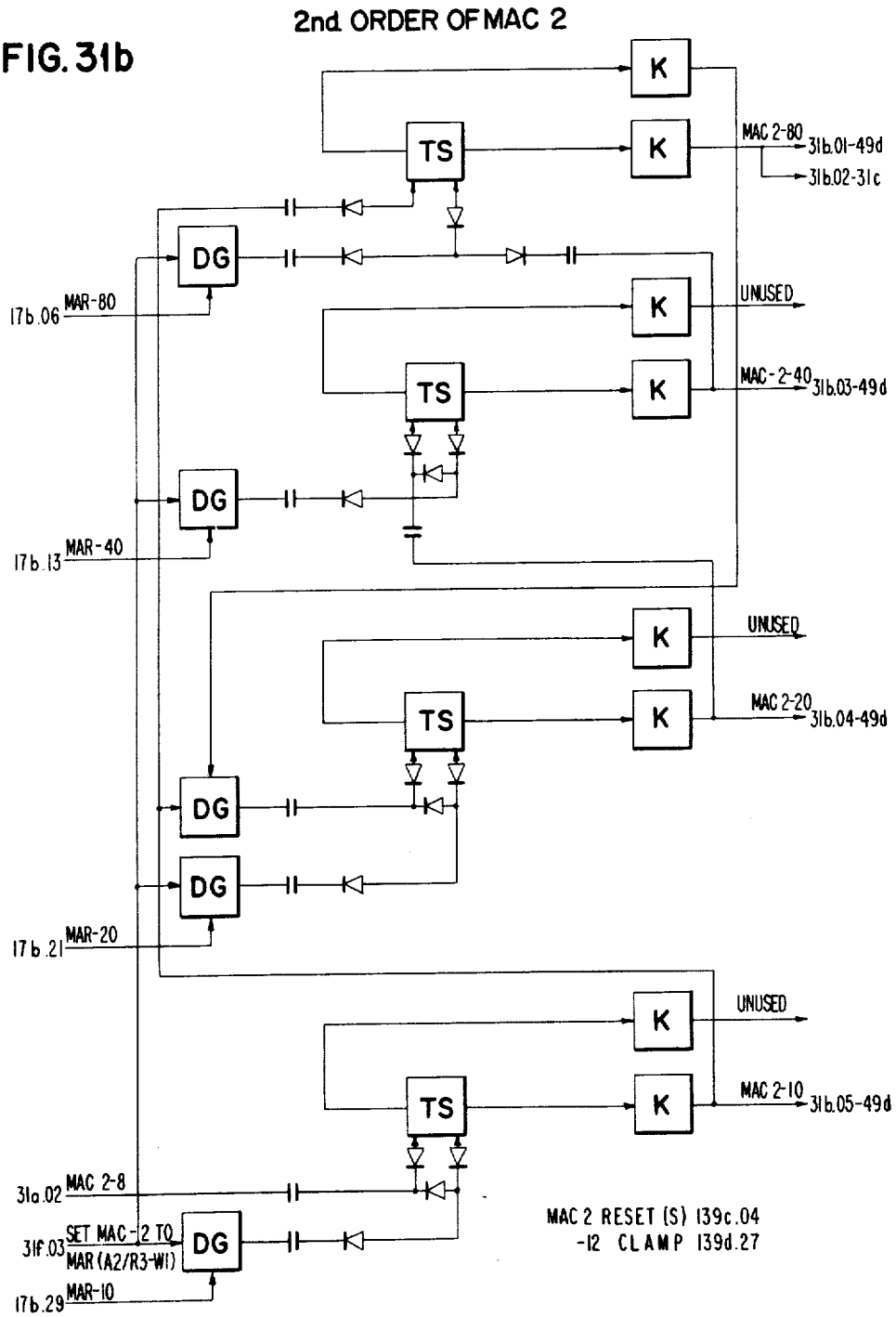


FIG. 31b


2nd ORDER OF MAC 2
K
TS
DG
MAC 2-80
31b.01-49d
31b.02-31c
UNUSED
MAC-2-40
31b.03-49d
MAC 2-20
31b.04-49d
MAC 2-10
31b.05-49d
17b.06 MAR-80
17b.13 MAR-40
17b.21 MAR-20
17b.29 MAR-10
31a.02 MAC 2-8
31f.03 SET MAC-2 TO MAR (A2/R3-W1)
MAC 2 RESET (S) 139c.04
-12 CLAMP 139d.27

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FIG.31c

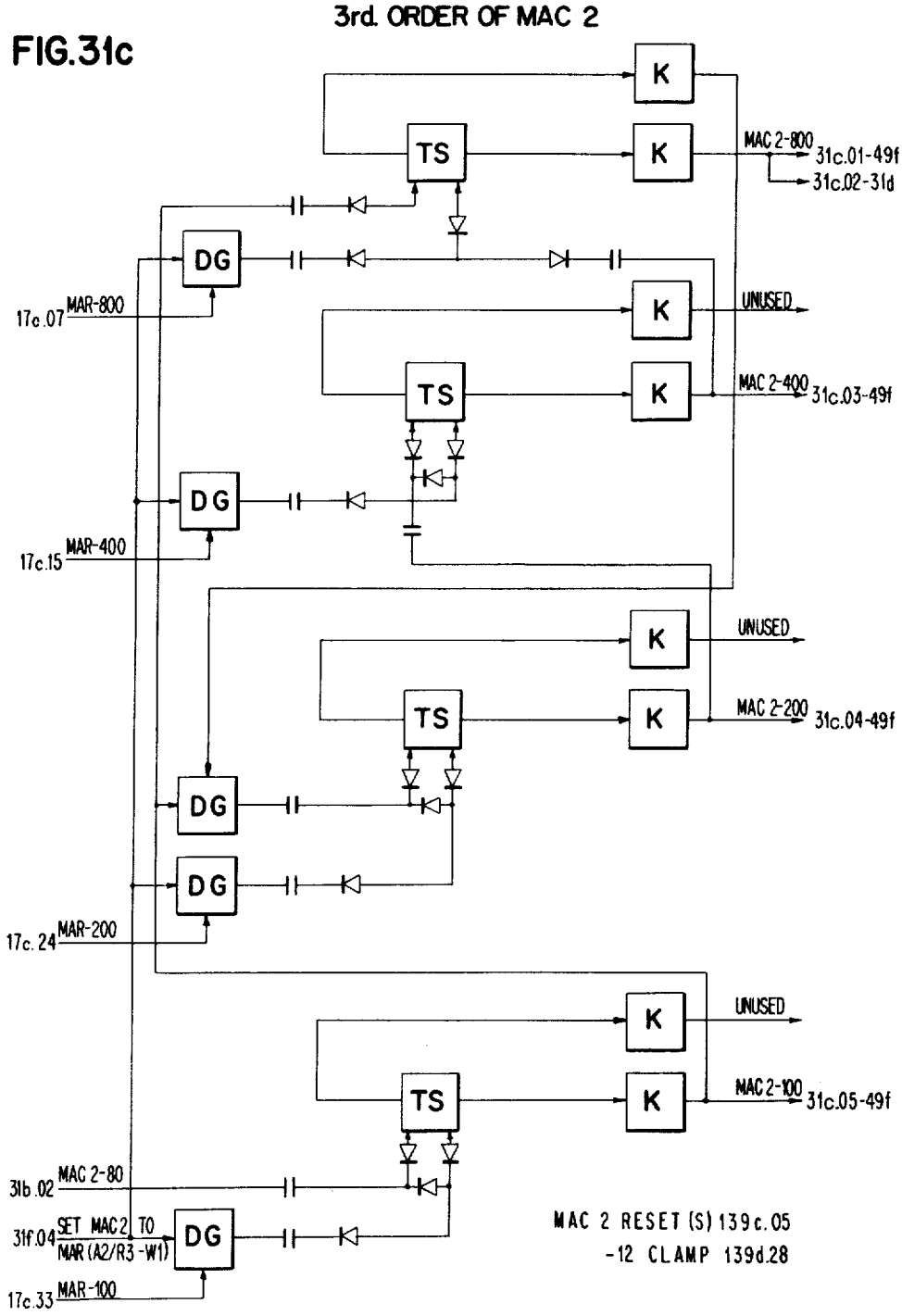
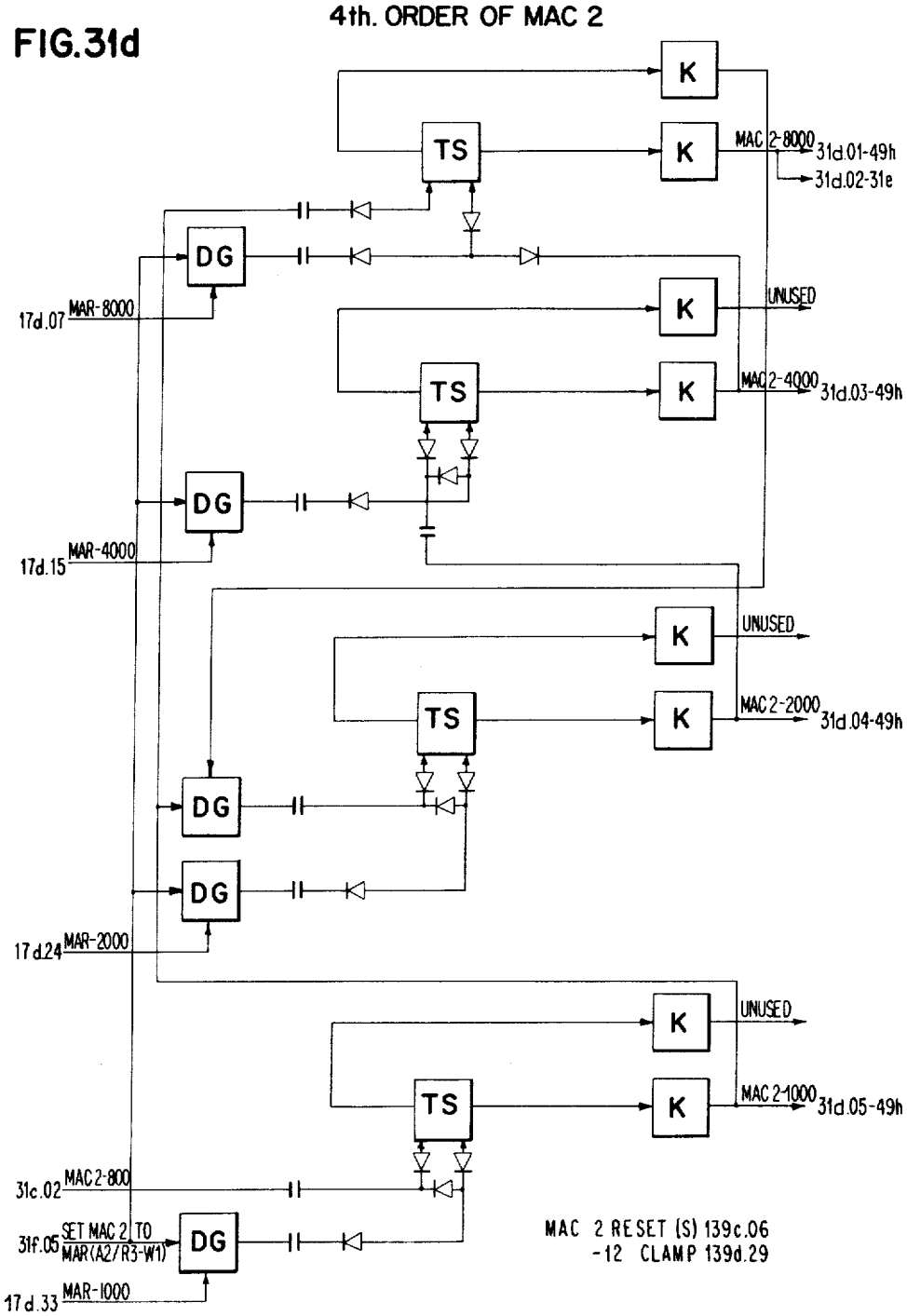


FIG.31d


4th. ORDER OF MAC 2
K
TS
K
MAC 2-8000
31d.01-49h
31d.02-31e
DG
17d.07 MAR-8000
K
UNUSED
TS
K
MAC 2-4000
31d.03-49h
DG
17d.15 MAR-4000
K
UNUSED
TS
K
MAC 2-2000
31d.04-49h
DG
DG
17d.24 MAR-2000
K
UNUSED
TS
K
MAC 2-1000
31d.05-49h
31c.02 MAC 2-800
31f.05 SET MAC 2 TO MAR (A2/R3-W1)
DG
17d.33 MAR-1000
MAC 2 RESET (S) 139c.06
-12 CLAMP 139d.29

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FIG. 32a INSTRUCTION COUNTER CONTROLS 8 4,9, OF IC

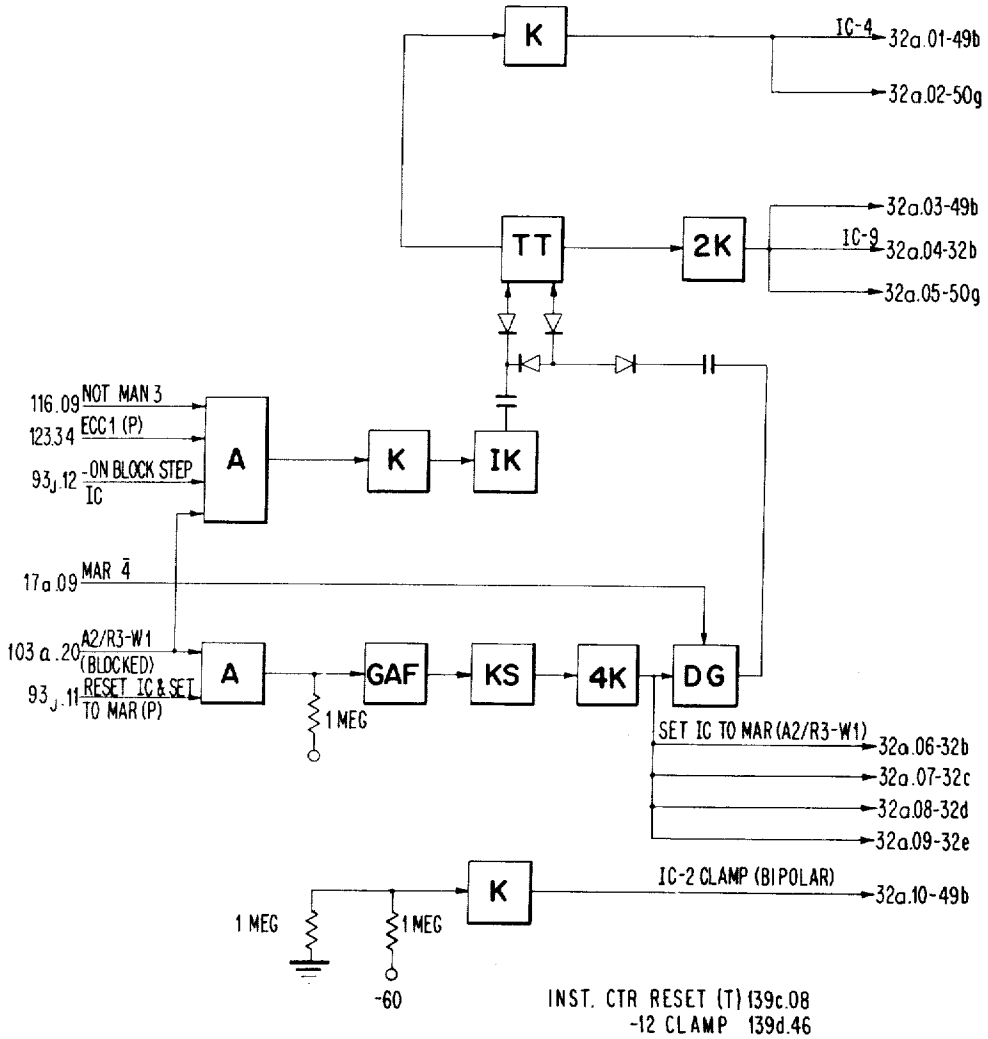


FIG. 32b

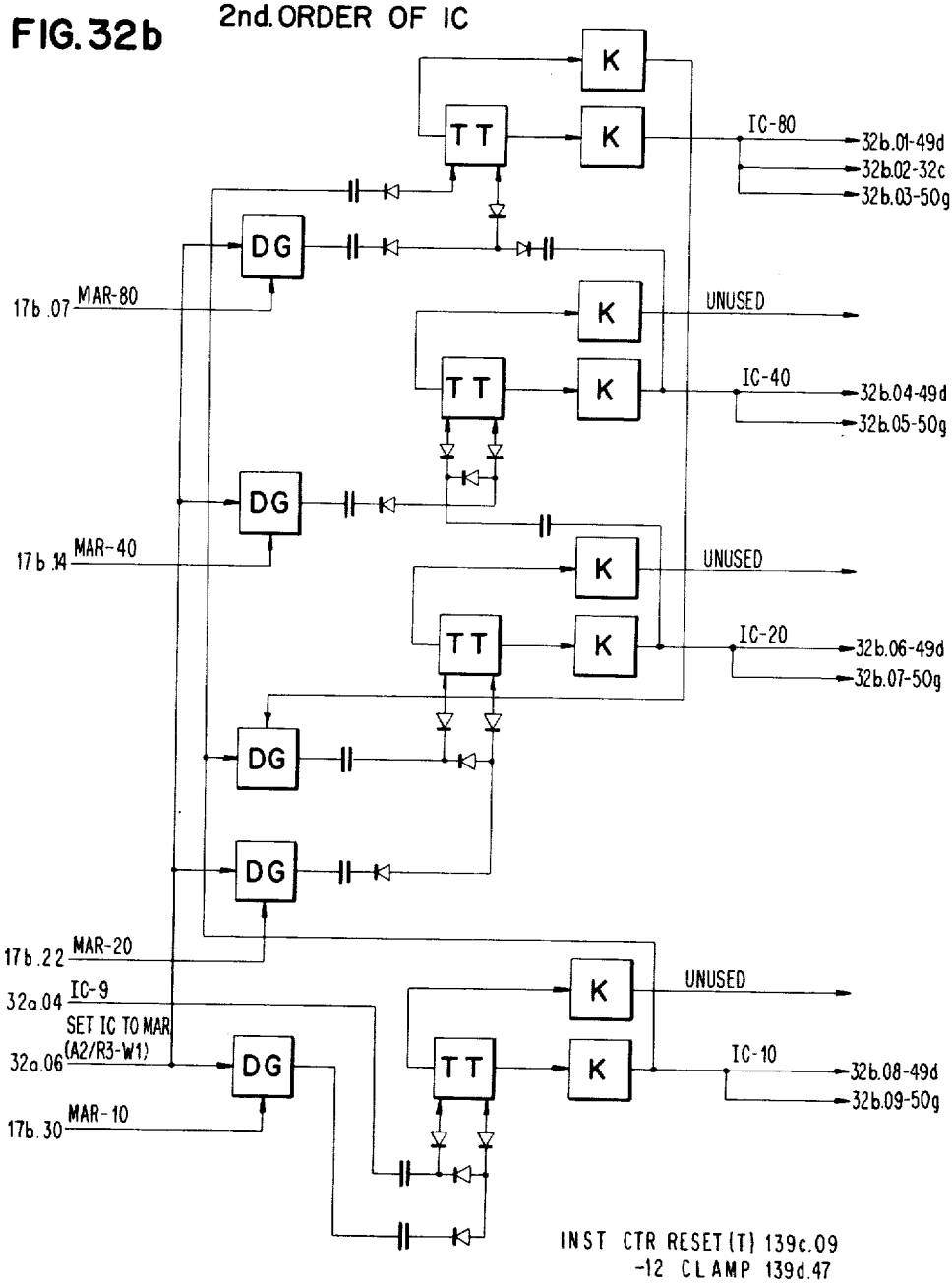
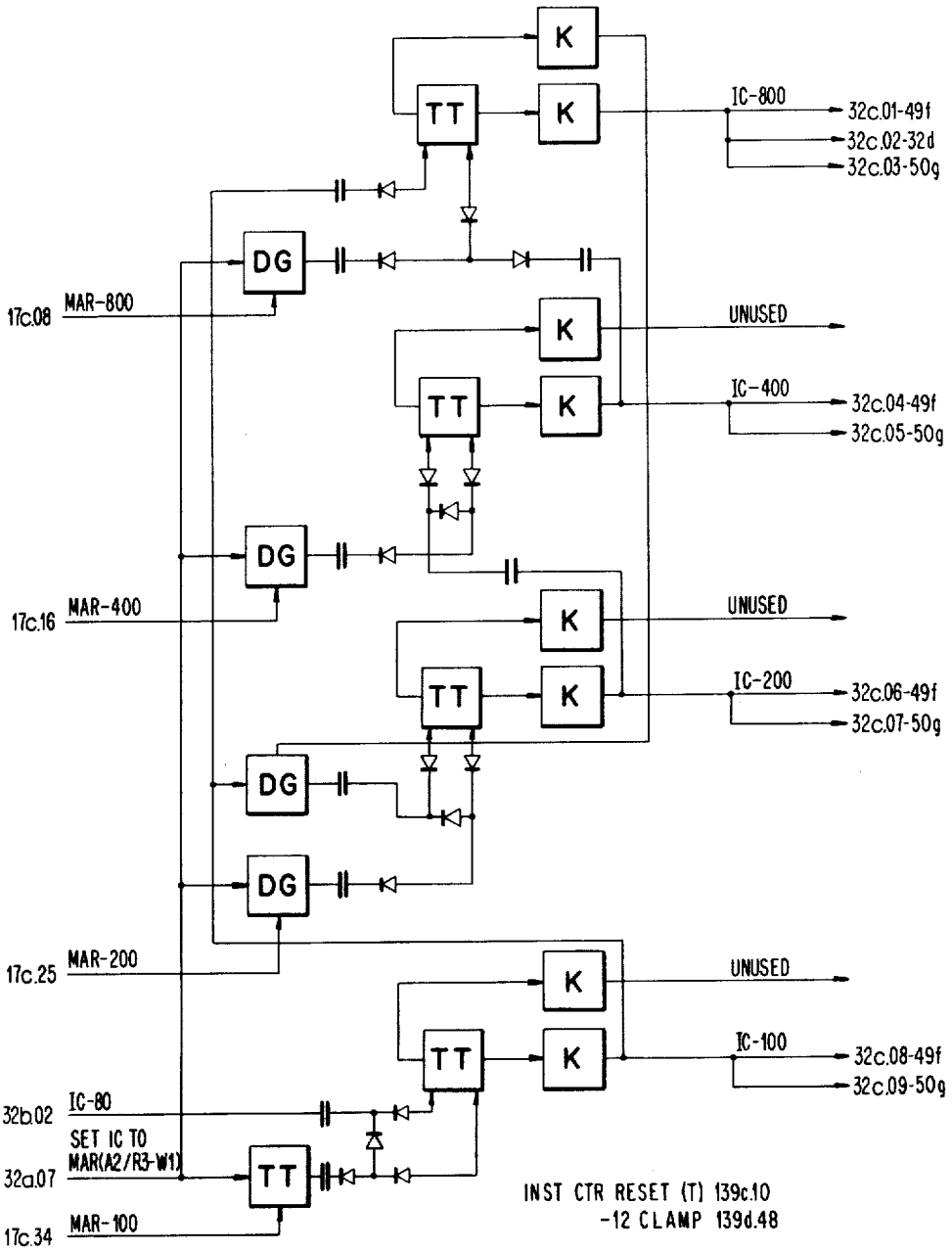

2nd. ORDER OF IC
K
TT
K
IC-80
32b.01-49d
32b.02-32c
32b.03-50g
DG
17b.07 MAR-80
K
UNUSED
TT
K
IC-40
32b.04-49d
32b.05-50g
DG
17b.14 MAR-40
K
UNUSED
TT
K
IC-20
32b.06-49d
32b.07-50g
DG
DG
17b.22 MAR-20
32a.04 IC-9
SET IC TO MAR (A2/R3-W1)
32a.06
K
UNUSED
DG
TT
K
IC-10
32b.08-49d
32b.09-50g
17b.30 MAR-10
INST CTR RESET (T) 139c.09
-12 CLAMP 139d.47

FIG.32c 3rd. ORDER OF IC



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FIG. 32d

4th. ORDER OF IC

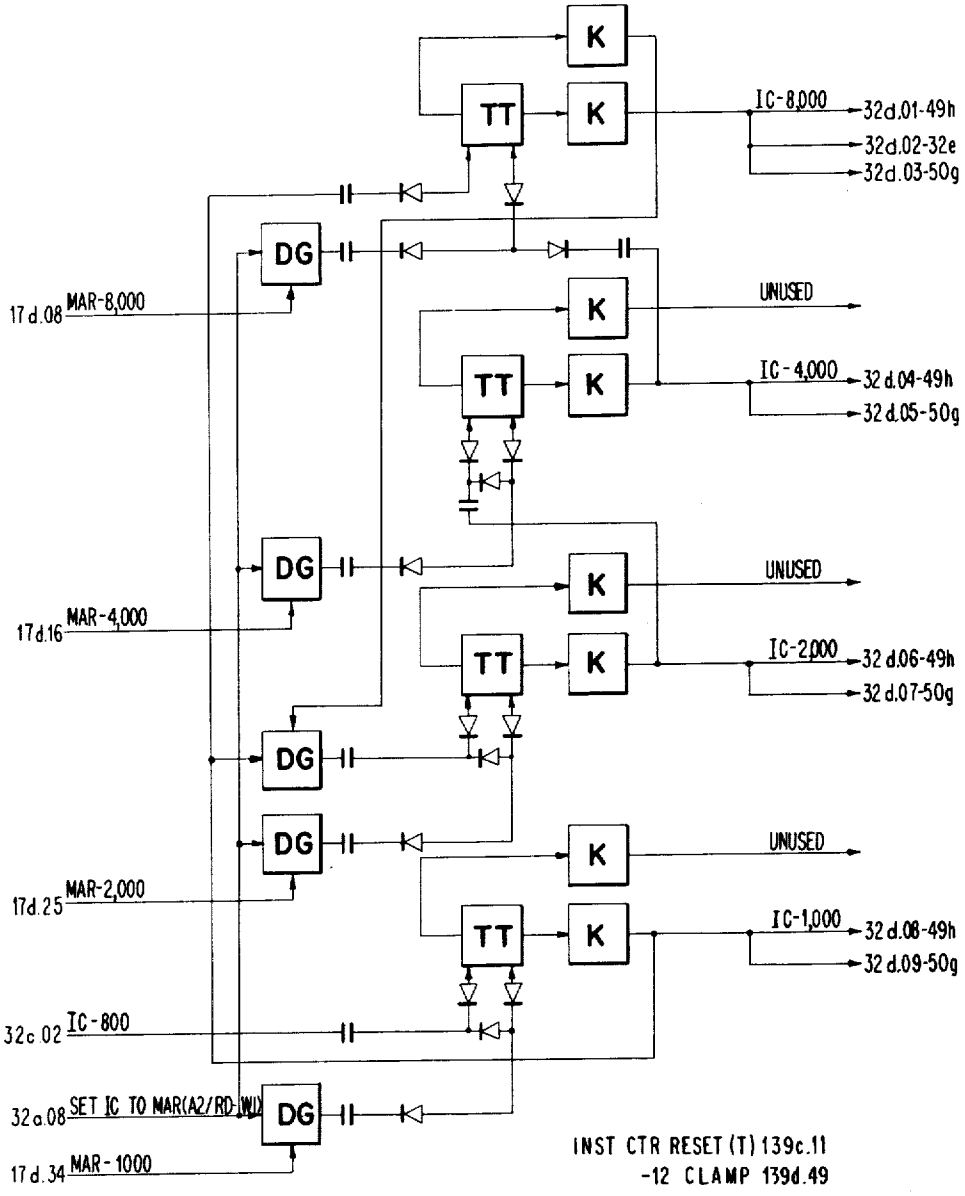


FIG. 32e

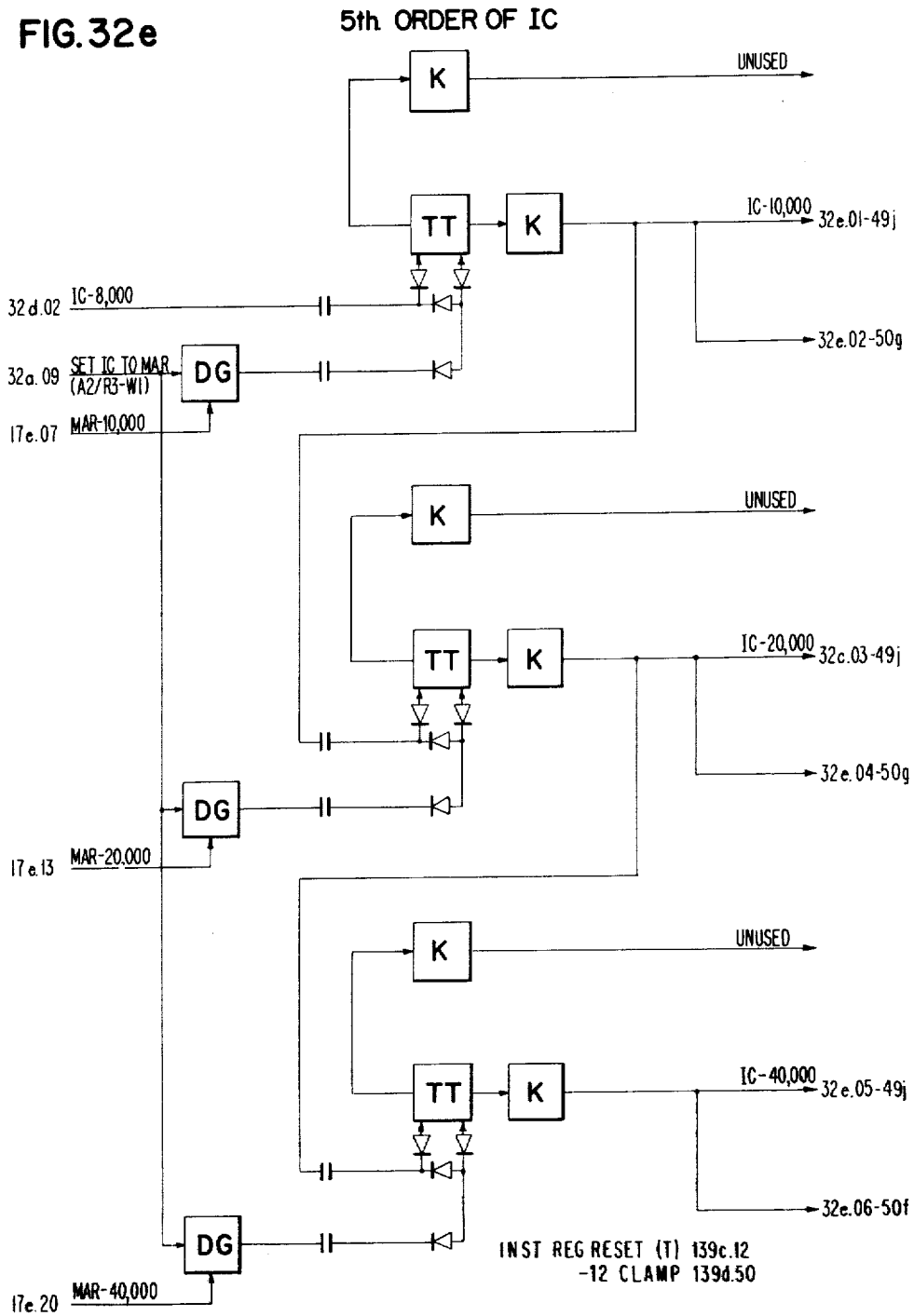

5th ORDER OF IC
K
UNUSED
TT
K
IC-10,000
32e.01-49j
32e.02-50g
32d.02 IC-8,000
32a.09 SET IC TO MAR (A2/R3-W1)
DG
17e.07 MAR-10,000
K
UNUSED
TT
K
IC-20,000
32c.03-49j
32e.04-50g
DG
17e.13 MAR-20,000
K
UNUSED
TT
K
IC-40,000
32e.05-49j
32e.06-50f
DG
17e.20 MAR-40,000
INST REG RESET (T) 139c.12
-12 CLAMP 139d.50

FIG.33a

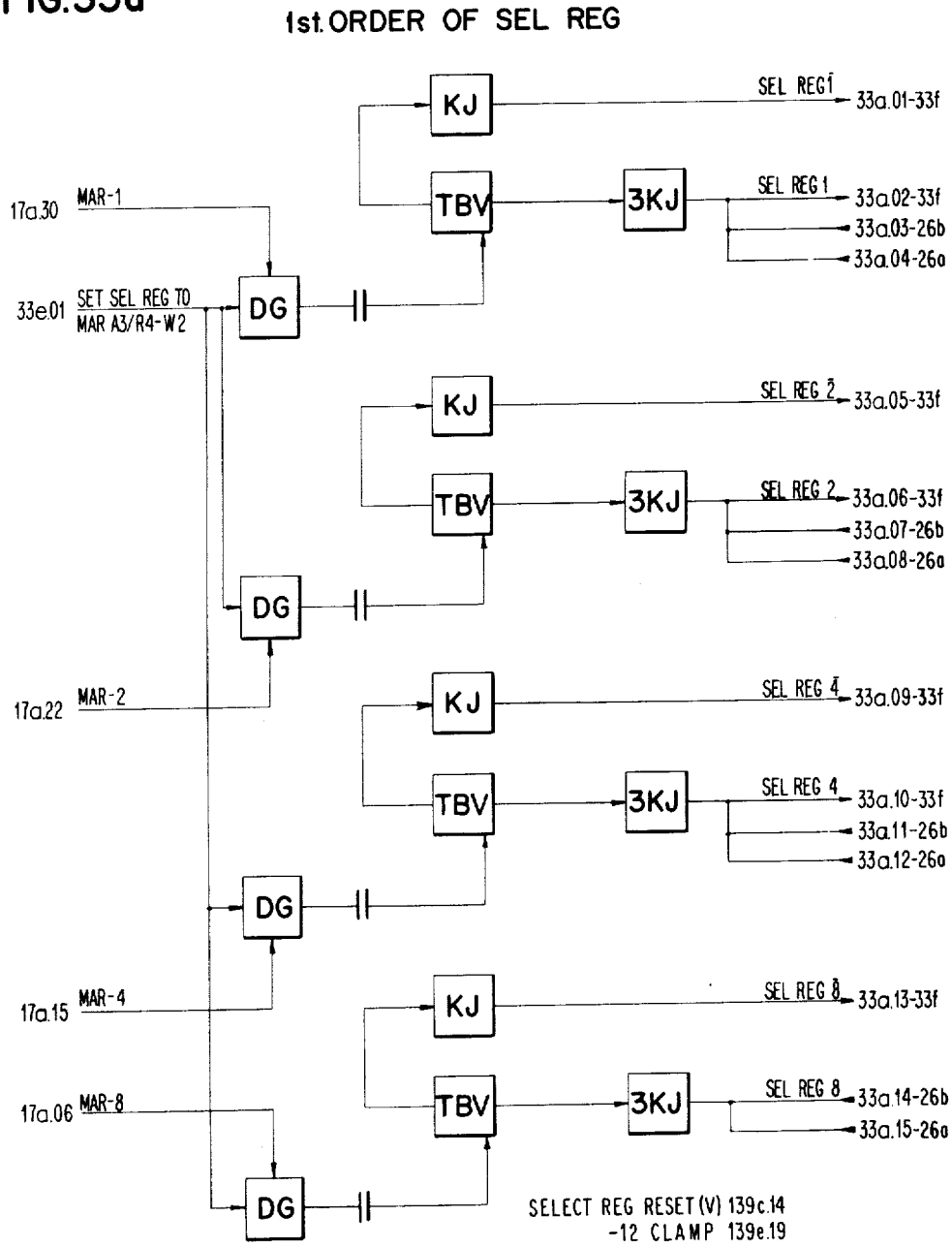
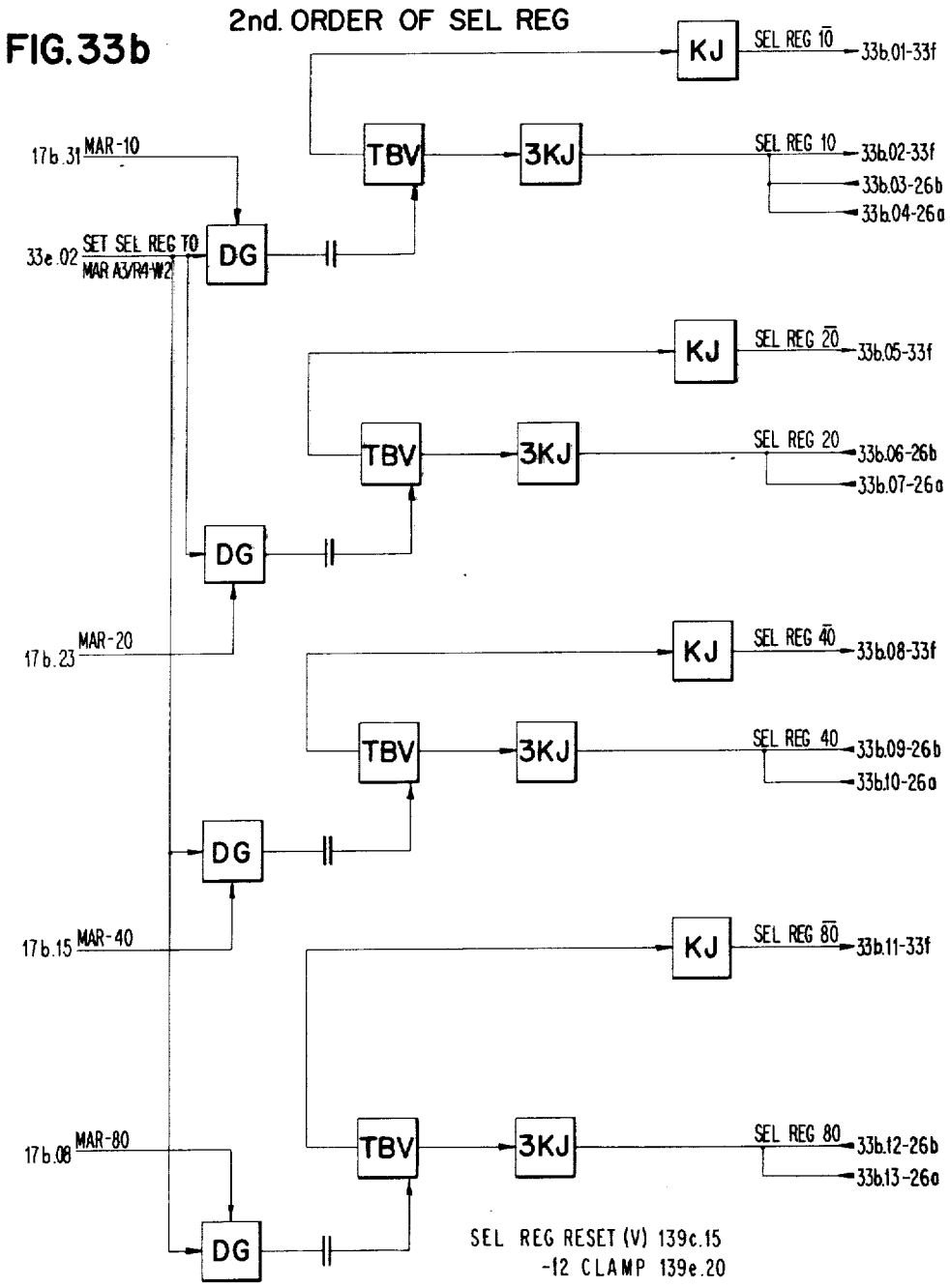
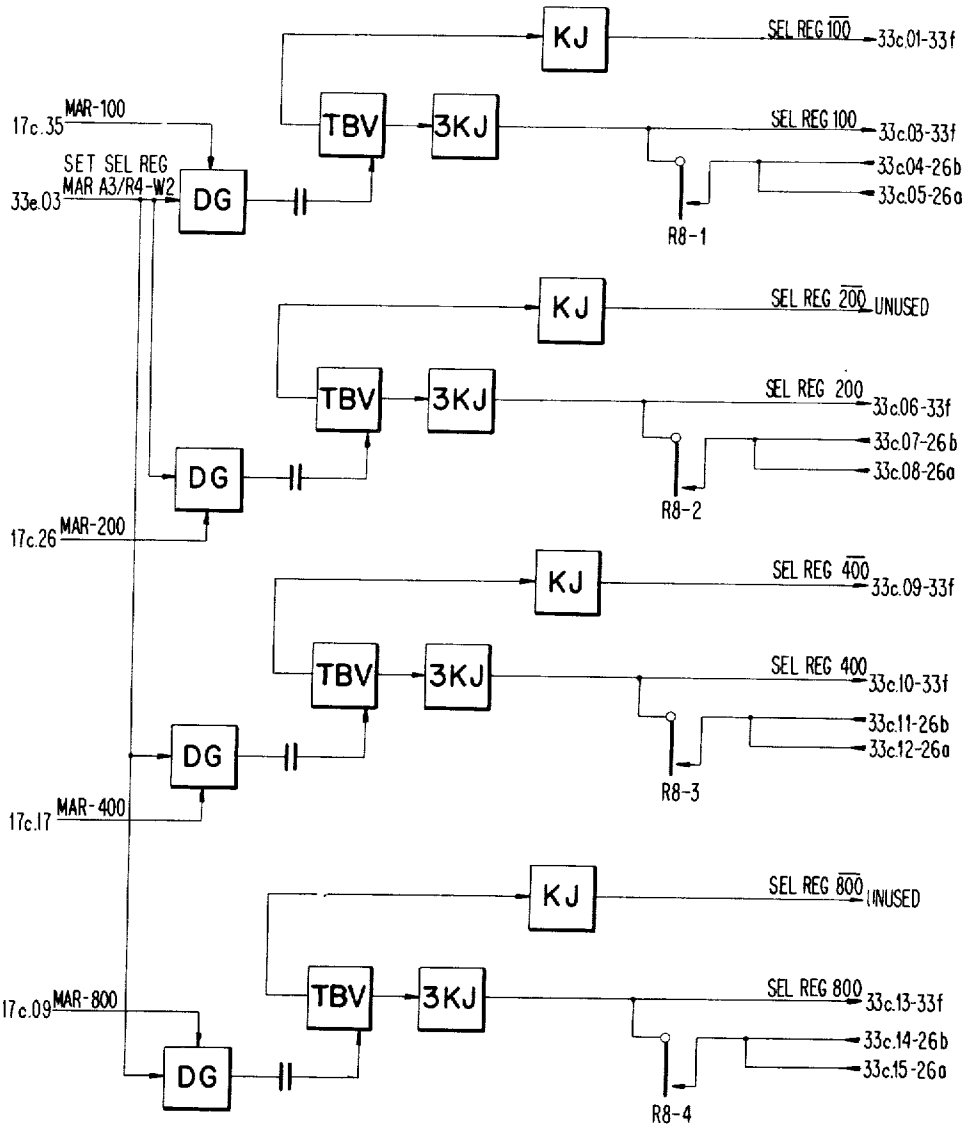

1st. ORDER OF SEL REG
KJ
SEL REG 1
33a.01-33f
TBV
3KJ
SEL REG 1
33a.02-33f
33a.03-26b
33a.04-26a
17a.30 MAR-1
33e.01 SET SEL REG TO MAR A3/R4-W2
DG
KJ
SEL REG 2
33a.05-33f
TBV
3KJ
SEL REG 2
33a.06-33f
33a.07-26b
33a.08-26a
DG
17a.22 MAR-2
KJ
SEL REG 4
33a.09-33f
TBV
3KJ
SEL REG 4
33a.10-33f
33a.11-26b
33a.12-26a
DG
17a.15 MAR-4
KJ
SEL REG 8
33a.13-33f
17a.06 MAR-8
TBV
3KJ
SEL REG 8
33a.14-26b
33a.15-26a
DG
SELECT REG RESET (V) 139c.14
-12 CLAMP 139e.19

FIG. 33b


2nd. ORDER OF SEL REG
KJ
SEL REG 10
33b.01-33f
17b.31 MAR-10
TBV
3KJ
SEL REG 10
33b.02-33f
33b.03-26b
33b.04-26a
33e.02 SET SEL REG TO
MAR A3/R4-W2
DG
KJ
SEL REG 20
33b.05-33f
TBV
3KJ
SEL REG 20
33b.06-26b
33b.07-26a
DG
17b.23 MAR-20
KJ
SEL REG 40
33b.08-33f
TBV
3KJ
SEL REG 40
33b.09-26b
33b.10-26a
DG
17b.15 MAR-40
KJ
SEL REG 80
33b.11-33f
17b.08 MAR-80
TBV
3KJ
SEL REG 80
33b.12-26b
33b.13-26a
DG
SEL REG RESET (V) 139c.15
-12 CLAMP 139e.20

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FIG. 33c 3rd. ORDER OF SEL. REG.



SEL REG RESET (V) 139c.16
-12 CLAMP 139e.21

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FIG.33d 4th. ORDER OF SEL REG

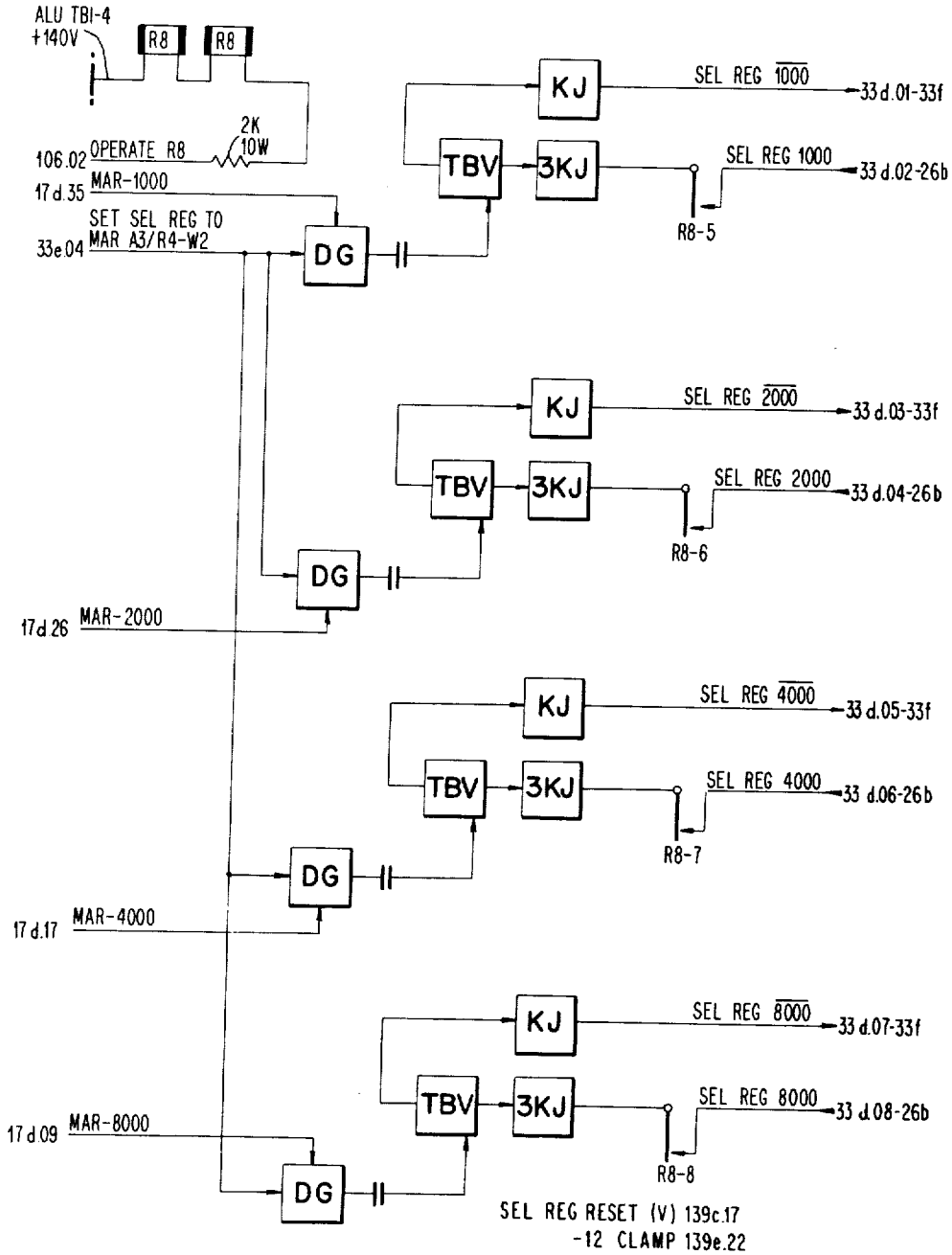


FIG. 33f

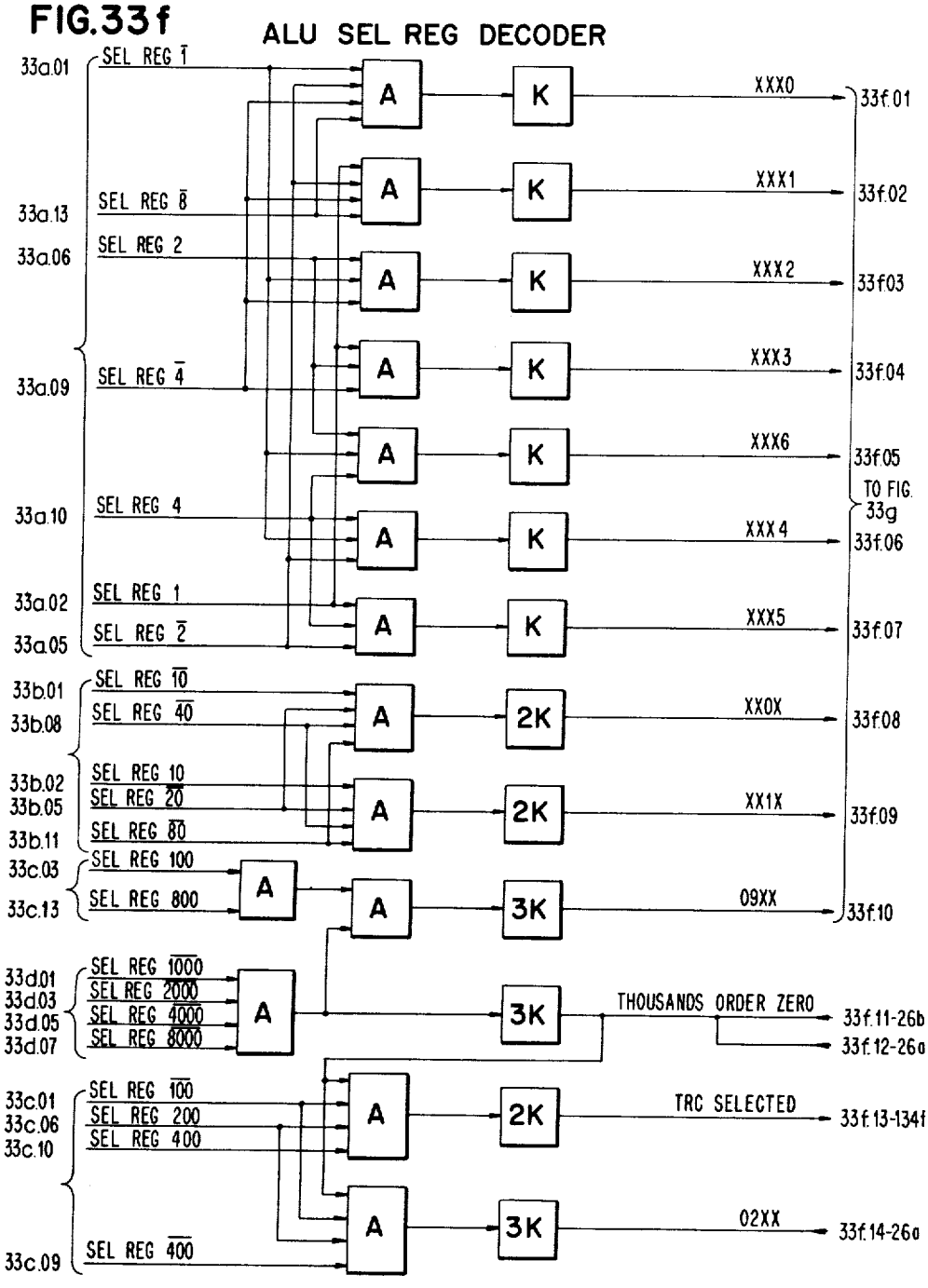

ALU SEL REG DECODER
33a.01
SEL REG 1
33a.13
SEL REG 8
33a.06
SEL REG 2
33a.09
SEL REG 4
33a.10
SEL REG 4
33a.02
SEL REG 1
33a.05
SEL REG 2
33b.01
SEL REG 10
33b.08
SEL REG 40
33b.02
SEL REG 10
33b.05
SEL REG 20
33b.11
SEL REG 80
33c.03
SEL REG 100
33c.13
SEL REG 800
33d.01
SEL REG 1000
33d.03
SEL REG 2000
33d.05
SEL REG 4000
33d.07
SEL REG 8000
33c.01
SEL REG 100
33c.06
SEL REG 200
33c.10
SEL REG 400
33c.09
SEL REG 400
A
K
2K
3K
XXX0
XXX1
XXX2
XXX3
XXX6
XXX4
XXX5
XXOX
XX1X
09XX
THOUSANDS ORDER ZERO
TRC SELECTED
02XX
33f.01
33f.02
33f.03
33f.04
33f.05
TO FIG. 33g
33f.06
33f.07
33f.08
33f.09
33f.10
33f.11-26b
33f.12-26a
33f.13-134f
33f.14-26a

FIG. 33g

ALU SEL. REG. DECODER

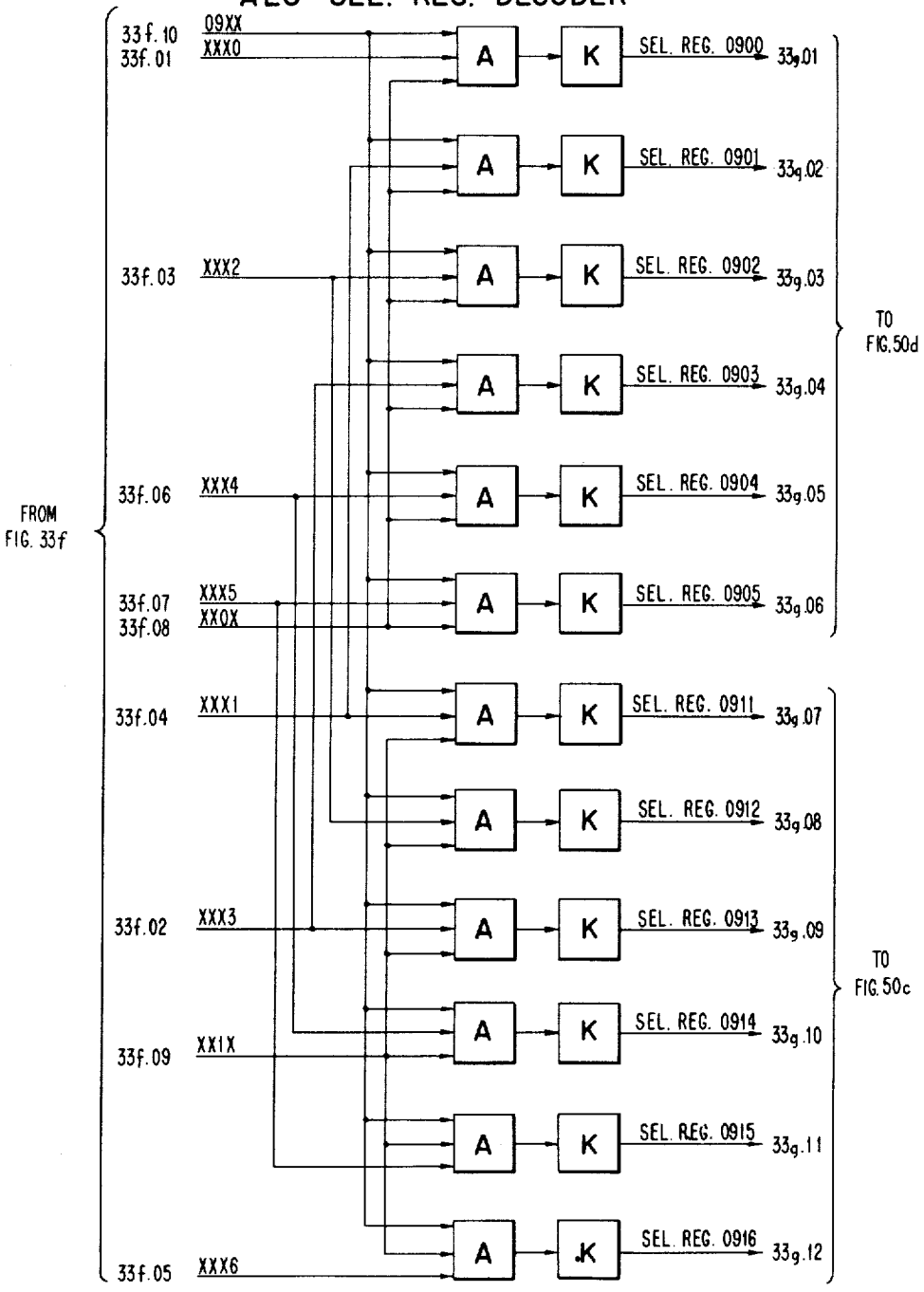


FIG.34a STORAGE 2X4 DECODER 128,256

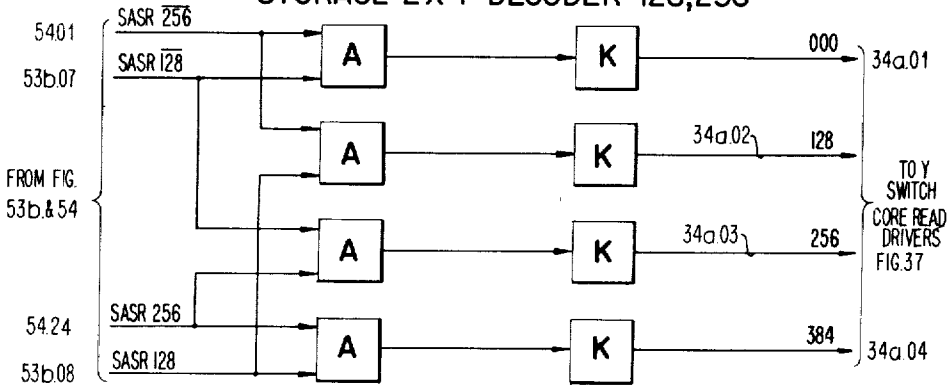


FIG. 34b STORAGE 2X4 DECODER 32,64

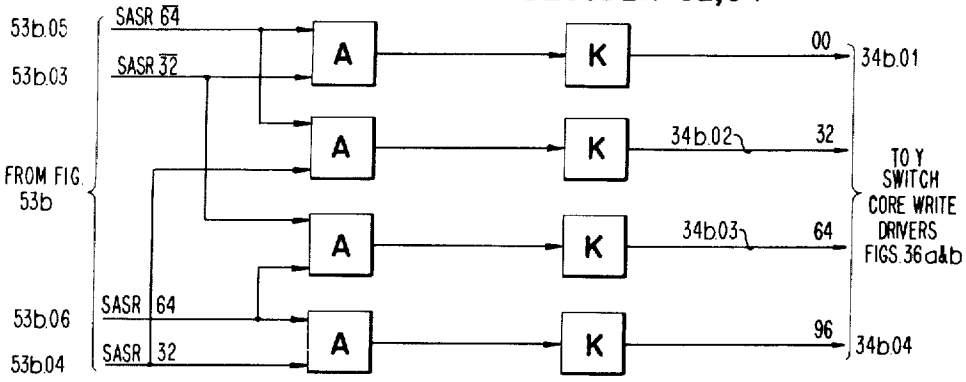


FIG. 34c STORAGE 2X4 DECODER 8,16

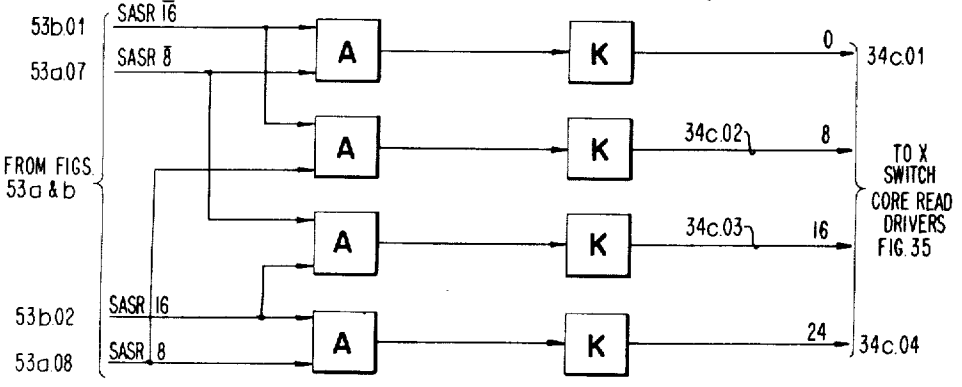


FIG. 34d

STORAGE 3 X 8 DECODER

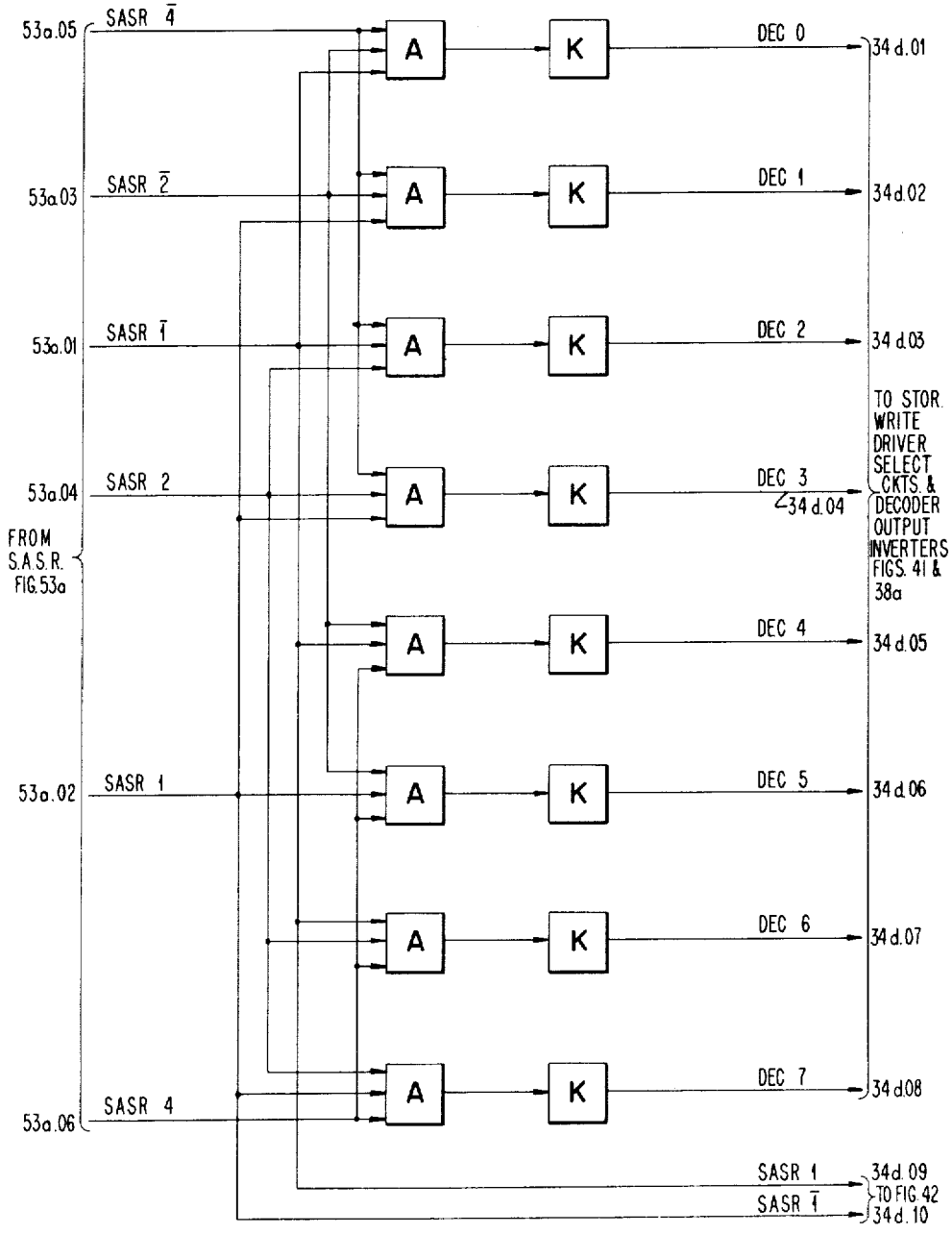


FIG. 35

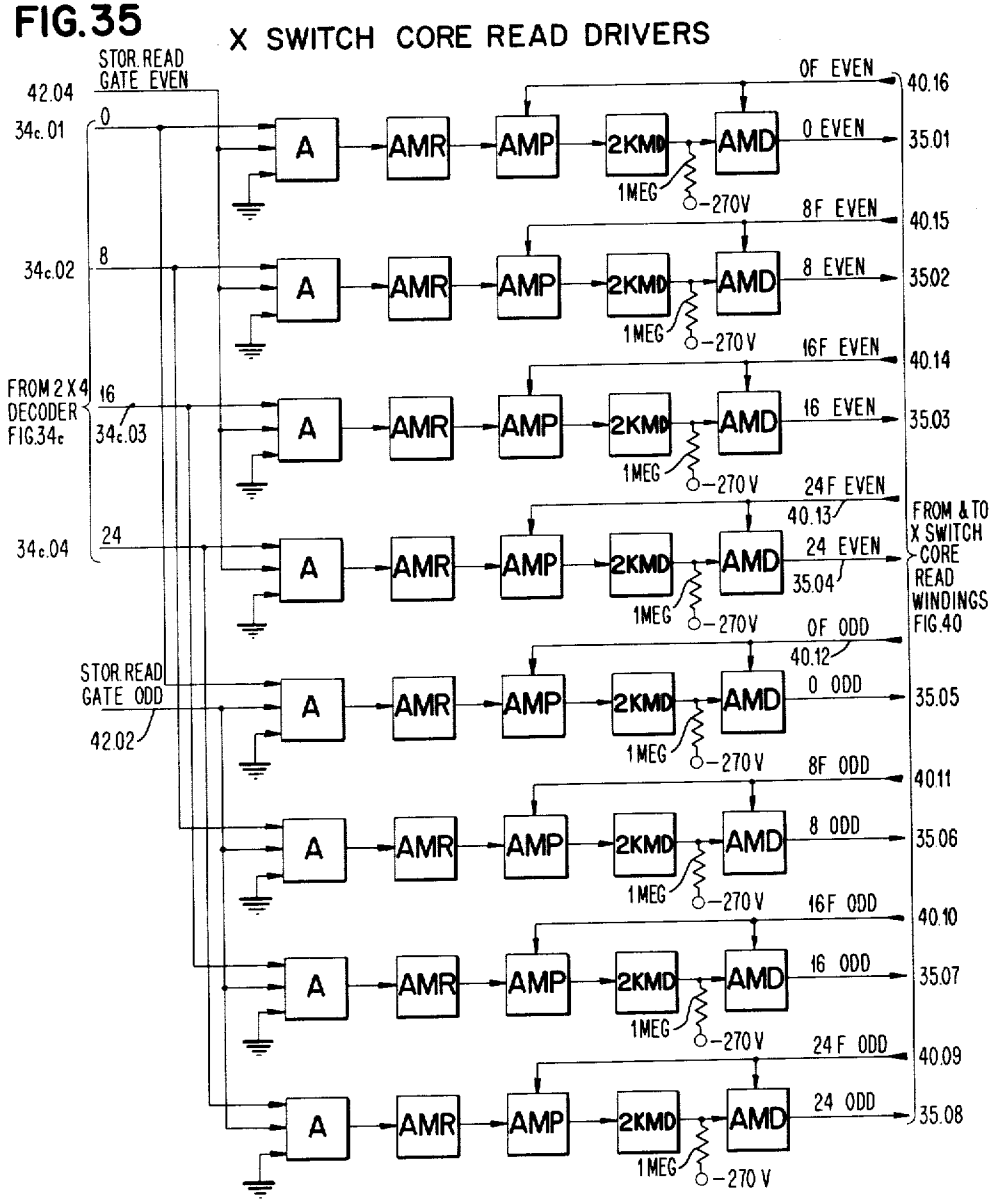

X SWITCH CORE READ DRIVERS
STOR. READ GATE EVEN
42.04
34c.01
0
34c.02
8
FROM 2 X 4 DECODER FIG. 34c
16
34c.03
34c.04
24
STOR. READ GATE ODD
42.02
A
AMR
AMP
2KMD
AMD
1MEG
-270V
0F EVEN
40.16
0 EVEN
35.01
8F EVEN
40.15
8 EVEN
35.02
16F EVEN
40.14
16 EVEN
35.03
24F EVEN
40.13
24 EVEN
35.04
0F ODD
40.12
0 ODD
35.05
8F ODD
40.11
8 ODD
35.06
16F ODD
40.10
16 ODD
35.07
24F ODD
40.09
24 ODD
35.08
FROM & TO X SWITCH CORE READ WINDINGS FIG. 40

FIG. 36a

2 X 4 DECODER OUTPUT INVERTERS

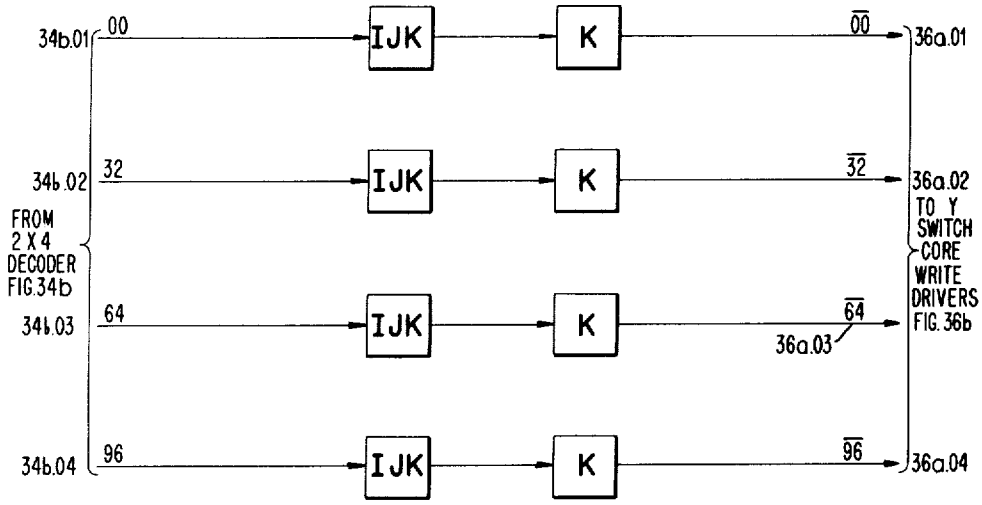
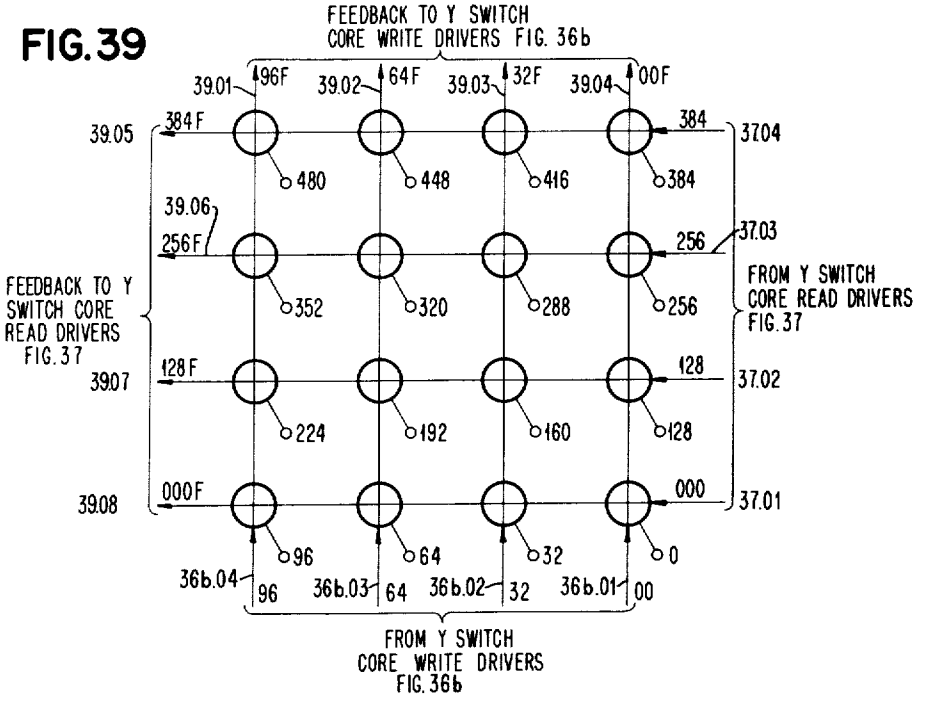


FIG. 39

"Y" SWITCH CORE MATRIX



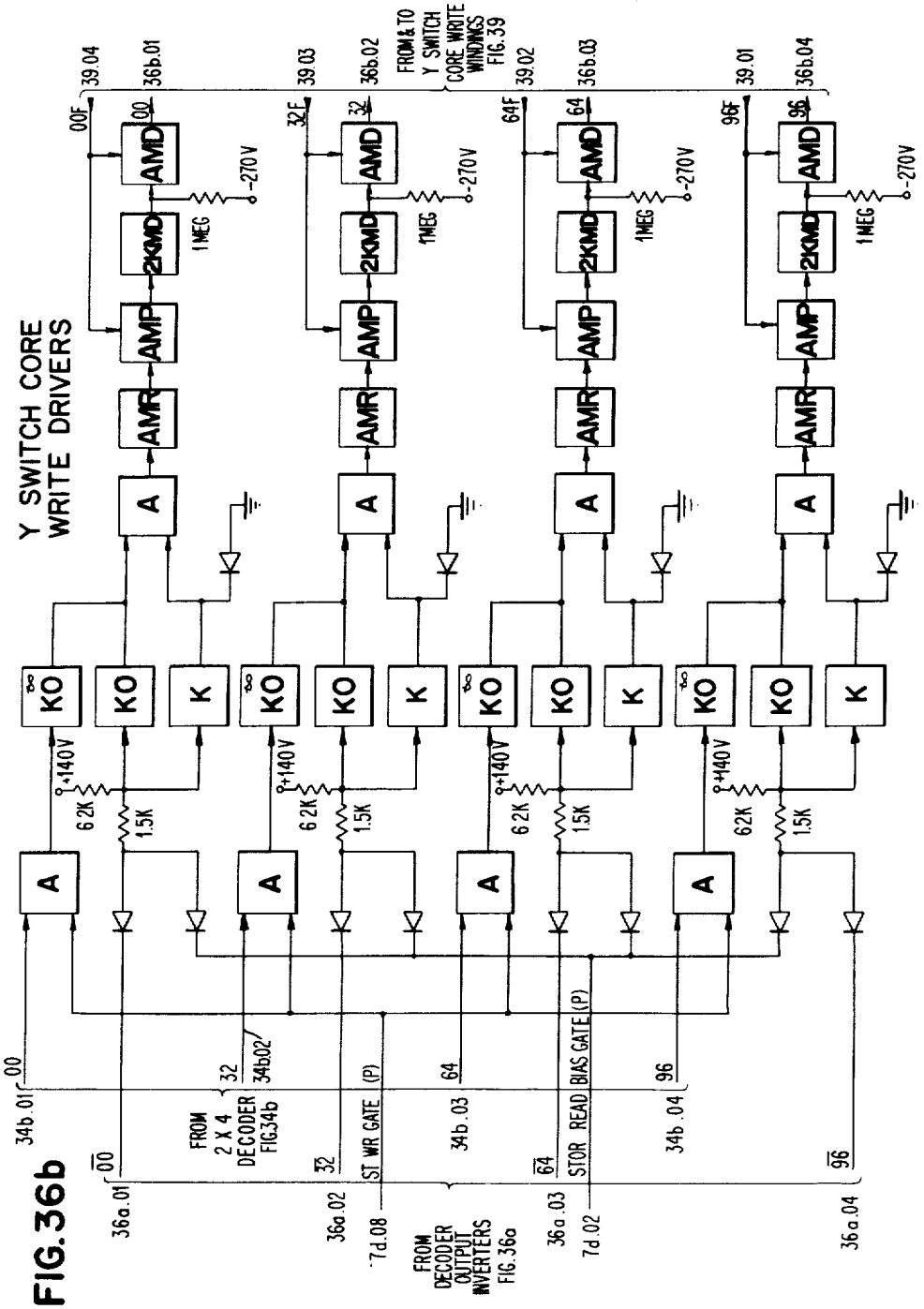

Y SWITCH CORE WRITE DRIVERS
FROM & TO Y SWITCH CORE WRITE WINDINGS FIG. 39
39.04
39.03
39.02
39.01
36b.01
36b.02
36b.03
36b.04
00F
32F
64F
96F
AMD
2KMD
AMP
AMR
A
KO
K
1MEG
-270V
+140V
6.2K
1.5K
34b.01
34b.02
34b.03
34b.04
FROM 2 X 4 DECODER FIG. 34b
ST WR GATE (P)
STOR READ BIAS GATE (P)
36a.01
36a.02
36a.03
36a.04
7d.08
7d.02
FROM DECODER OUTPUT INVERTERS FIG. 36a

FIG. 36b

FIG. 37

Y SWITCH CORE READ DRIVERS

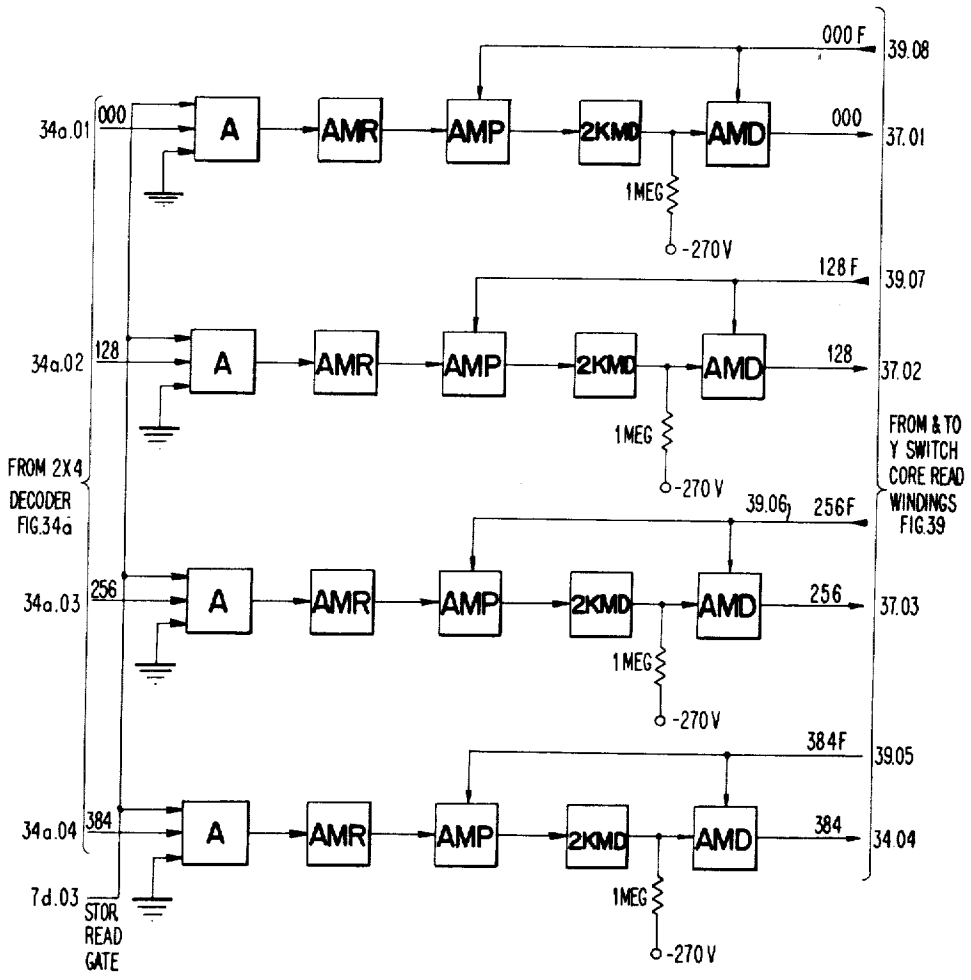
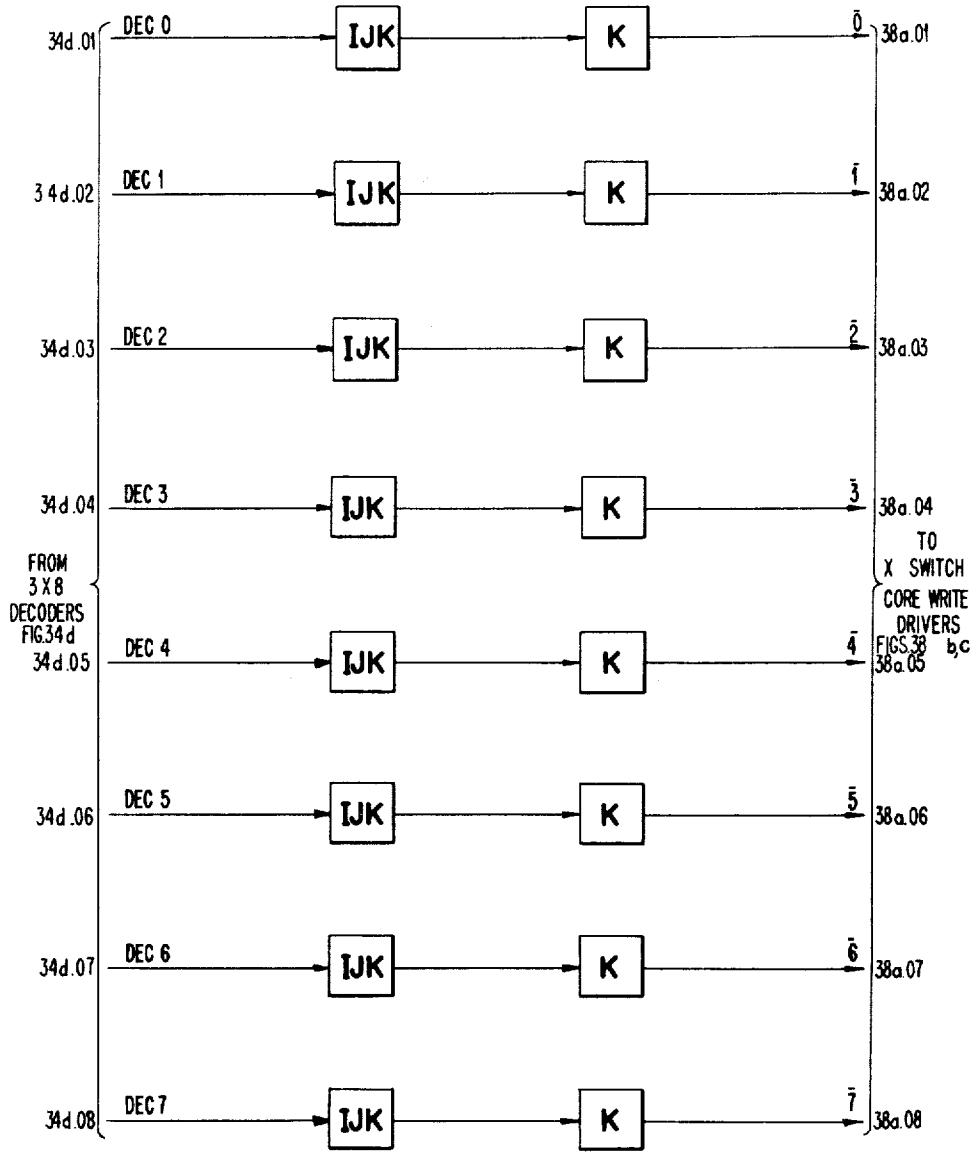
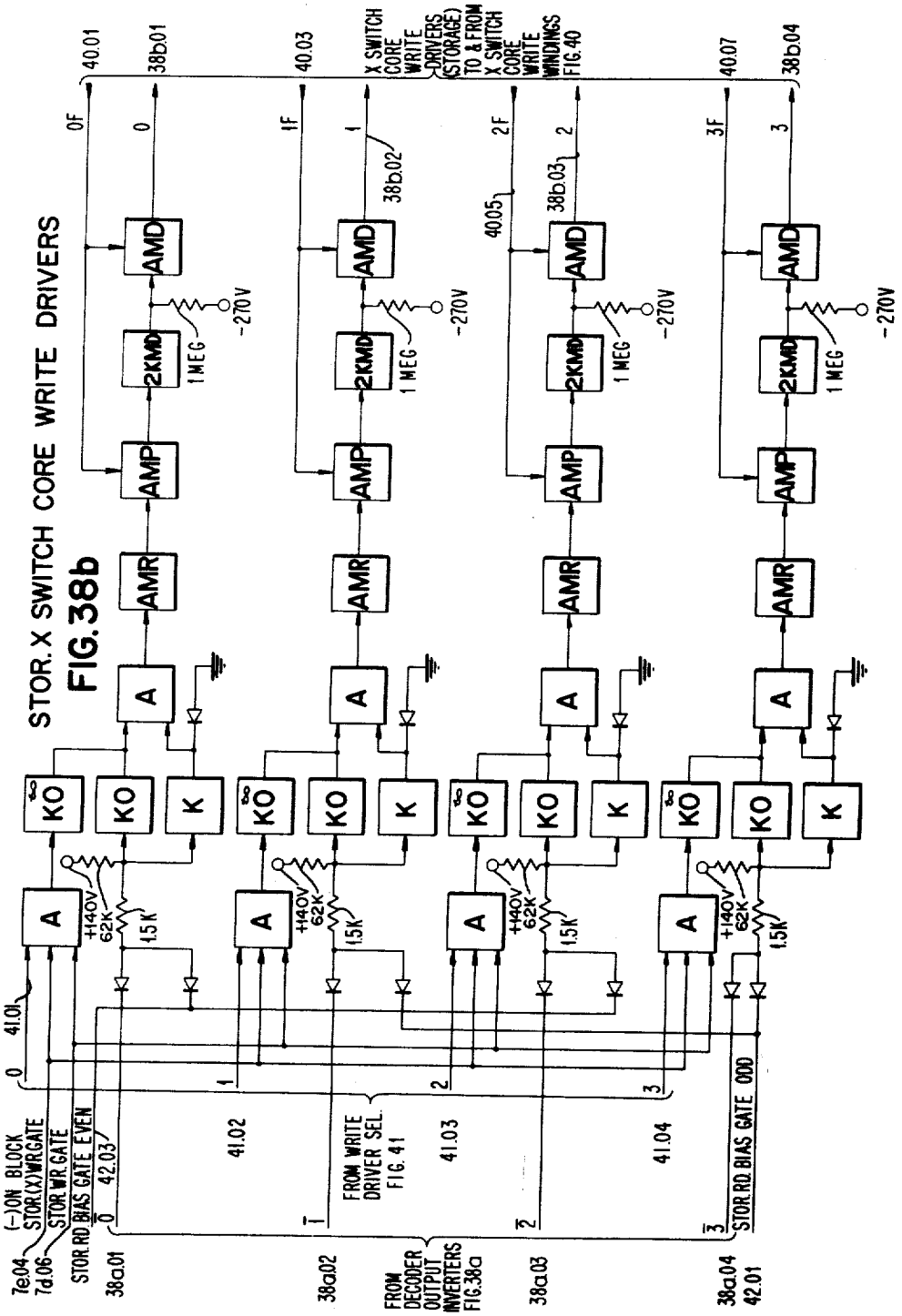


FIG. 38a

3 X 8 DECODER OUTPUT INVERTERS




STOR. X SWITCH CORE WRITE DRIVERS
FIG. 38b
X SWITCH CORE WRITE DRIVERS (STORAGE) TO & FROM X SWITCH CORE WRITE WINDINGS FIG. 40
40.01
40.03
40.05
40.07
38b.01
38b.02
38b.03
38b.04
0F
1F
2F
3F
AMD
2KMD
AMP
AMR
A
KO
K
1 MEG
-270V
+140V
62K
1.5K
41.01
41.02
41.03
41.04
42.03
FROM WRITE DRIVER SEL. FIG. 41
(-)ON BLOCK STOR(X)WR GATE
STOR WR GATE
STOR RD BIAS GATE EVEN
STOR RD BIAS GATE ODD
7e.04
7d.06
38a.01
38a.02
38a.03
38a.04
42.01
FROM DECODER OUTPUT INVERTERS FIG. 38a

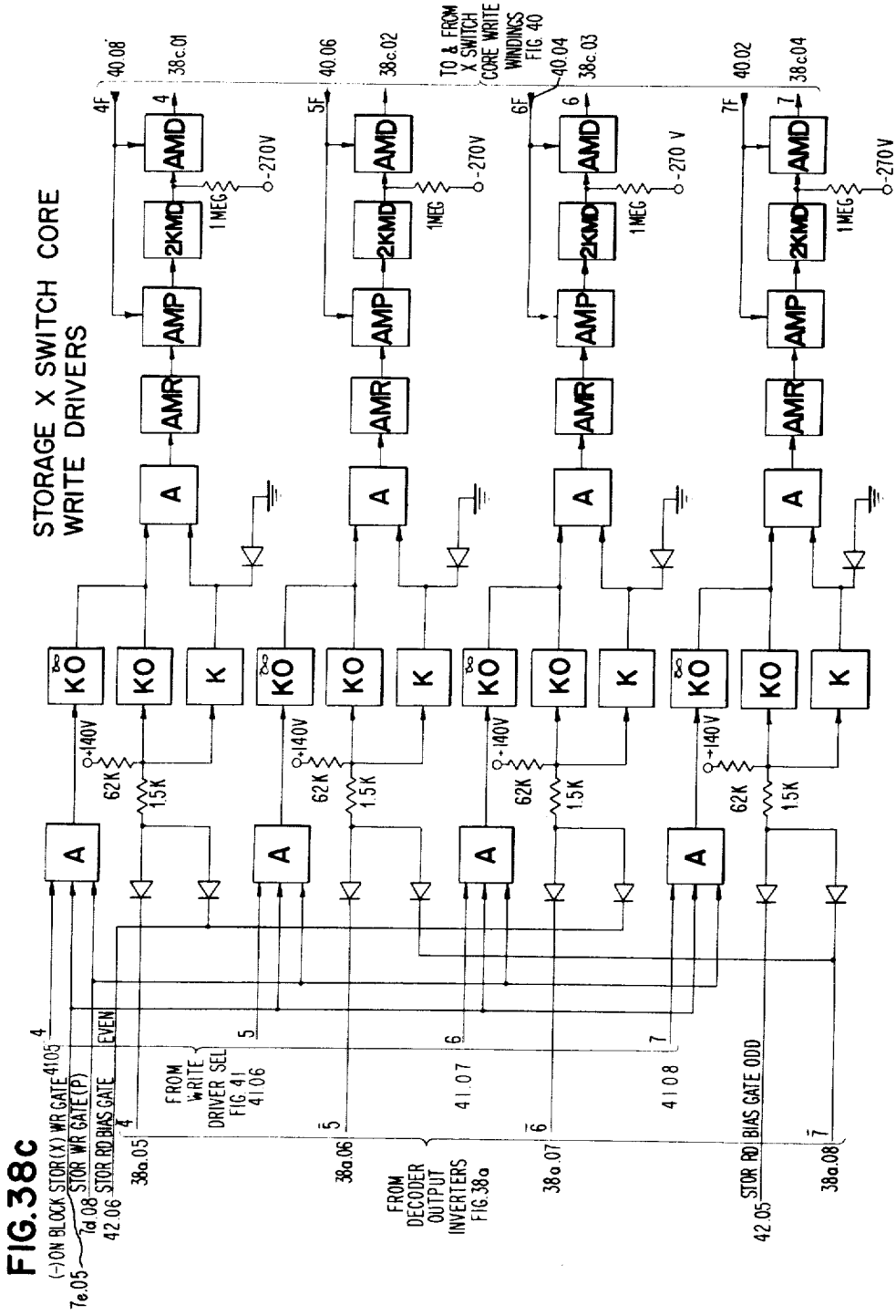

STORAGE X SWITCH CORE WRITE DRIVERS
TO & FROM X SWITCH CORE WRITE WINDINGS FIG 40
AMD
2KMD
AMP
AMR
A
KO
K
-270V
1MEG
+140V
62K
1.5K
FROM WRITE DRIVER SEL FIG 41 41.06
FROM DECODER OUTPUT INVERTERS FIG 38a
(-) ON BLOCK STOR (X) WR GATE 41.05
STOR WR GATE (P)
STOR RD BIAS GATE EVEN
STOR RD BIAS GATE ODD
EVEN
ODD

FIG. 38c

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FIG.40 "X" SWITCH CORE MATRIX 4 X 8 DIAGRAM

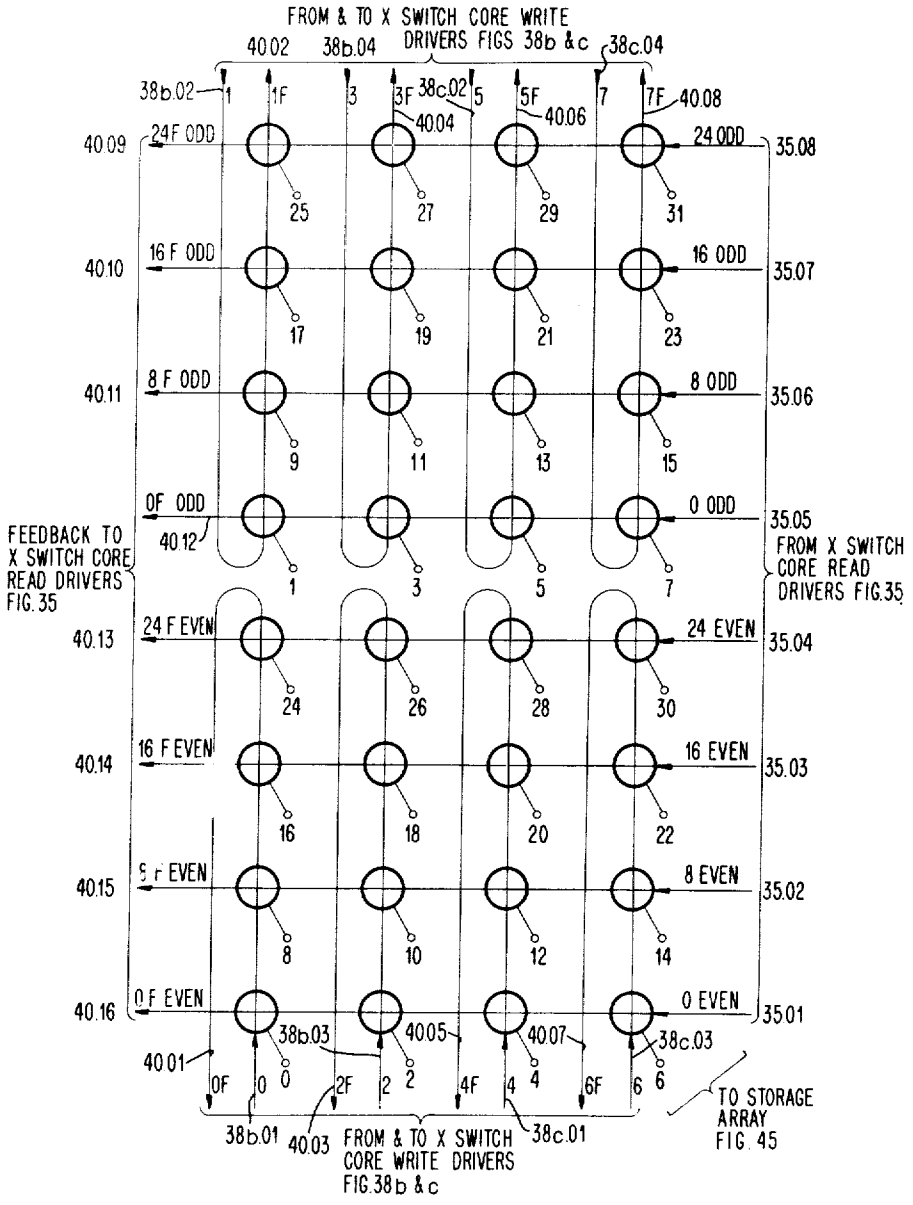


FIG. 41 STORAGE WRITE DRIVER SELECT CIRCUIT

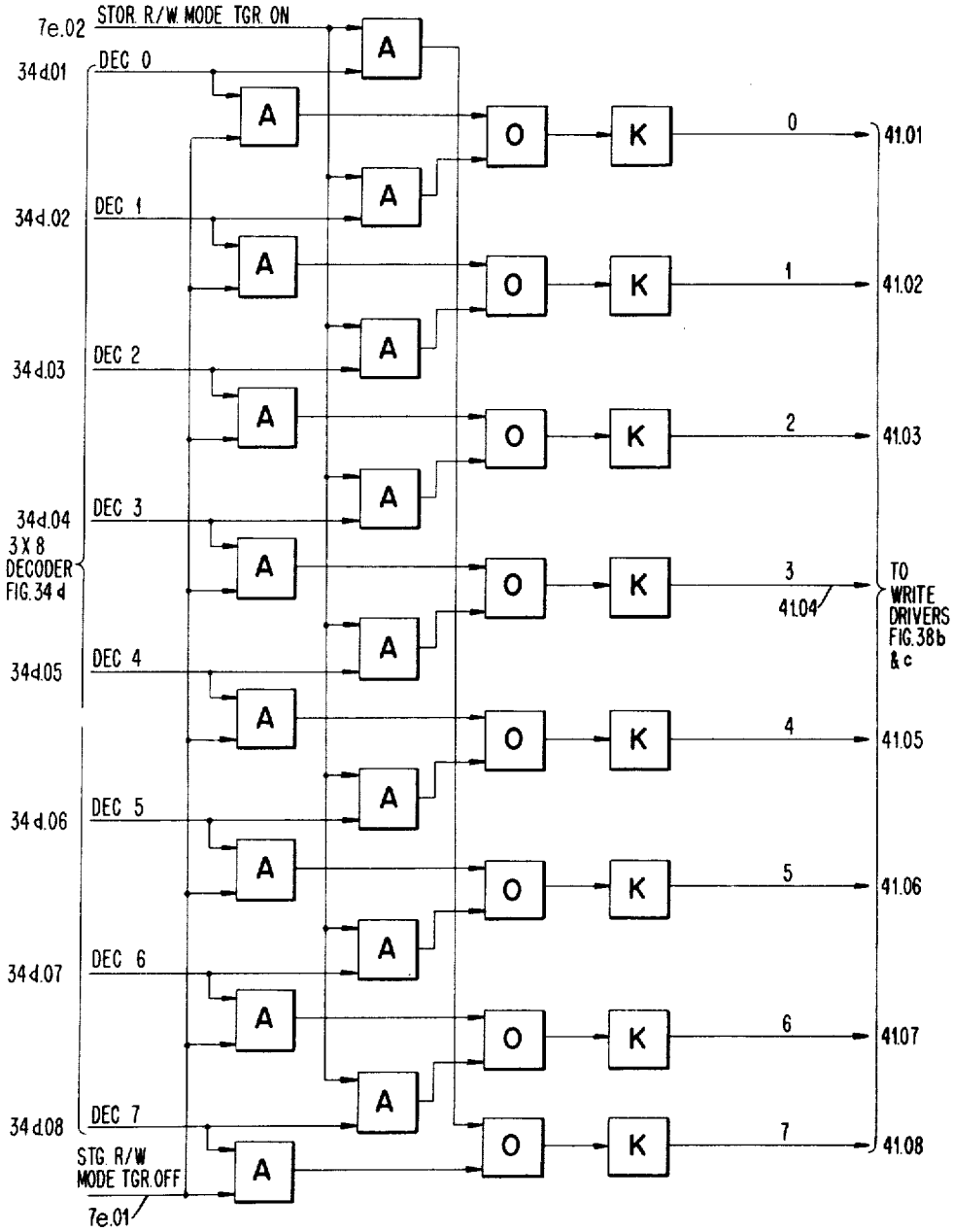


FIG. 42
ODD-EVEN GATING CIRCUIT

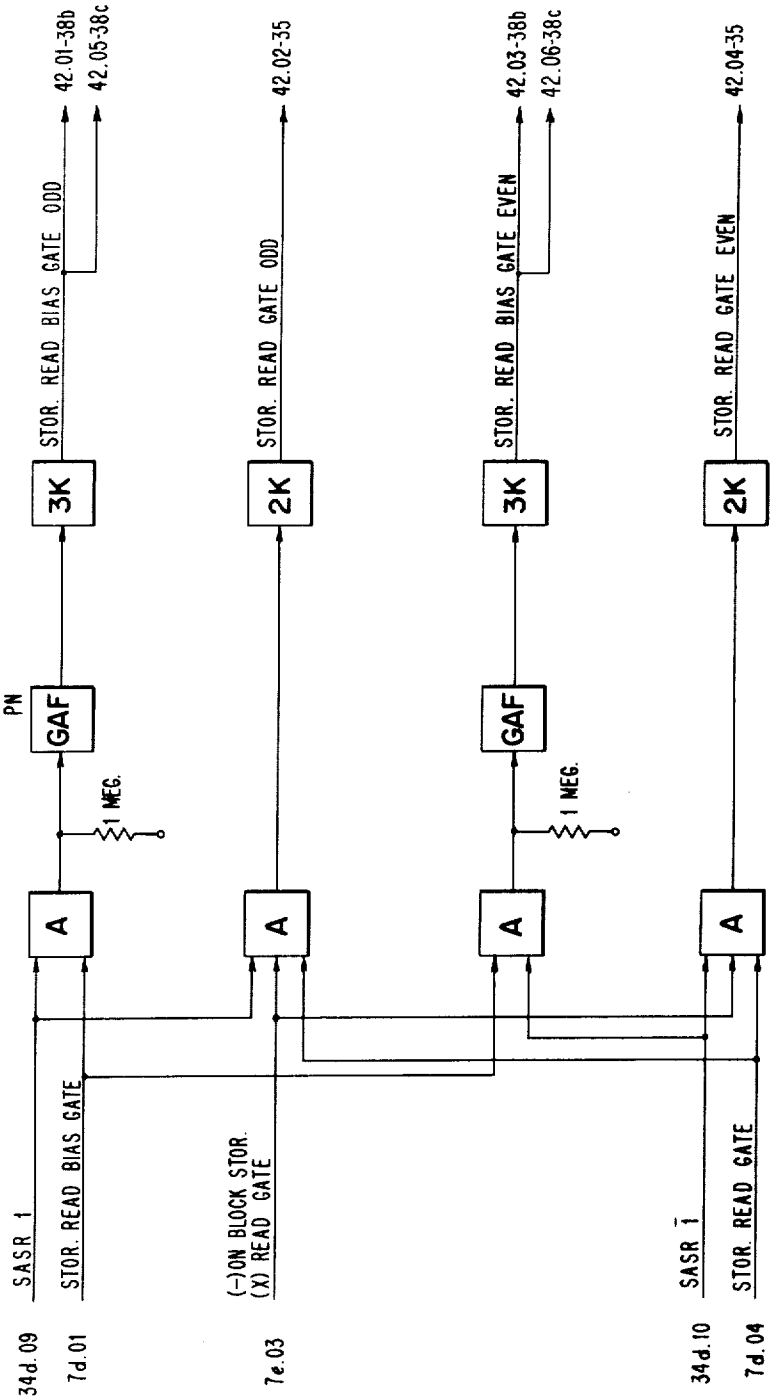
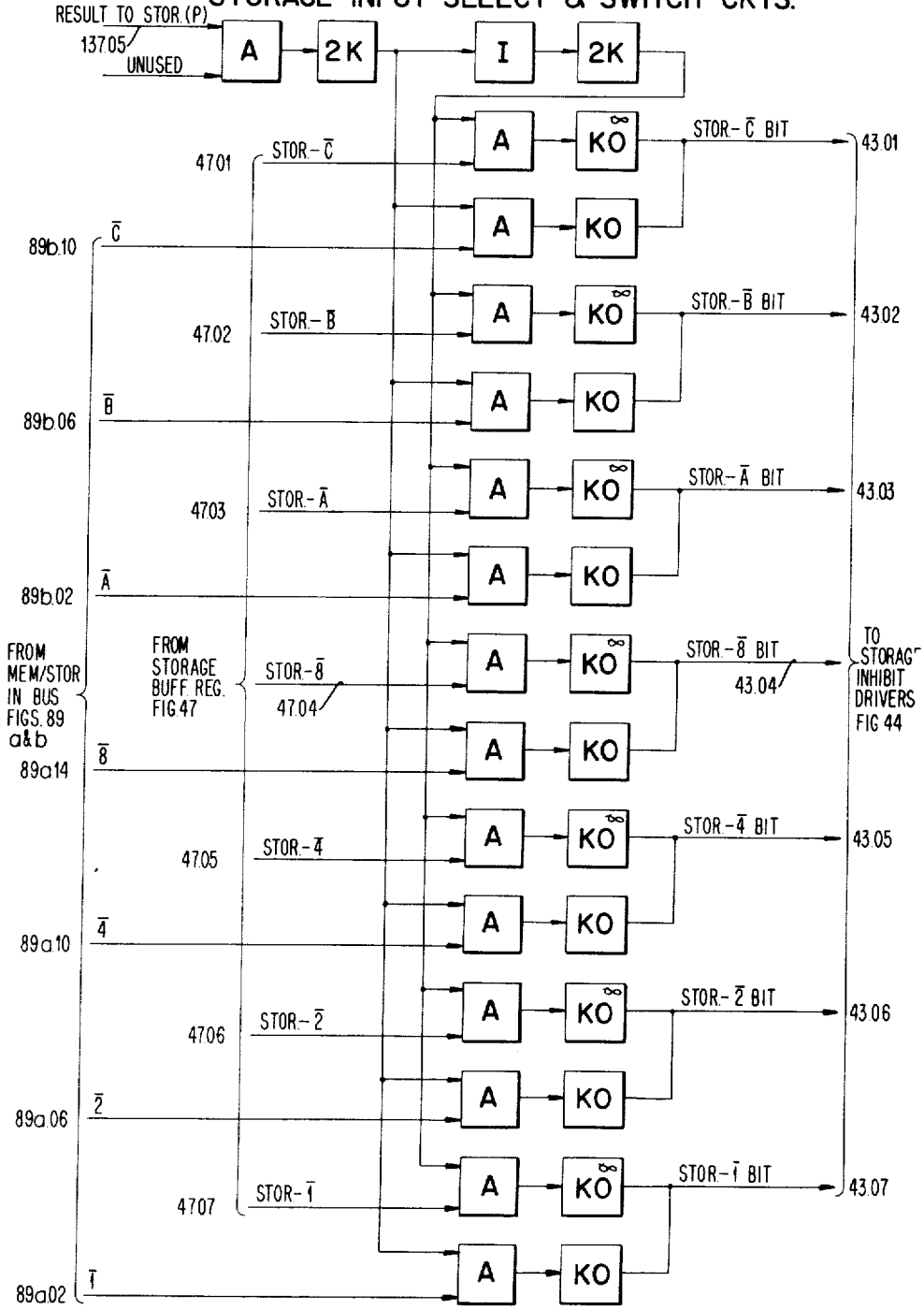


FIG. 43 STORAGE INPUT SELECT & SWITCH CKTS.



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FIG. 44 STORAGE INHIBIT DRIVERS

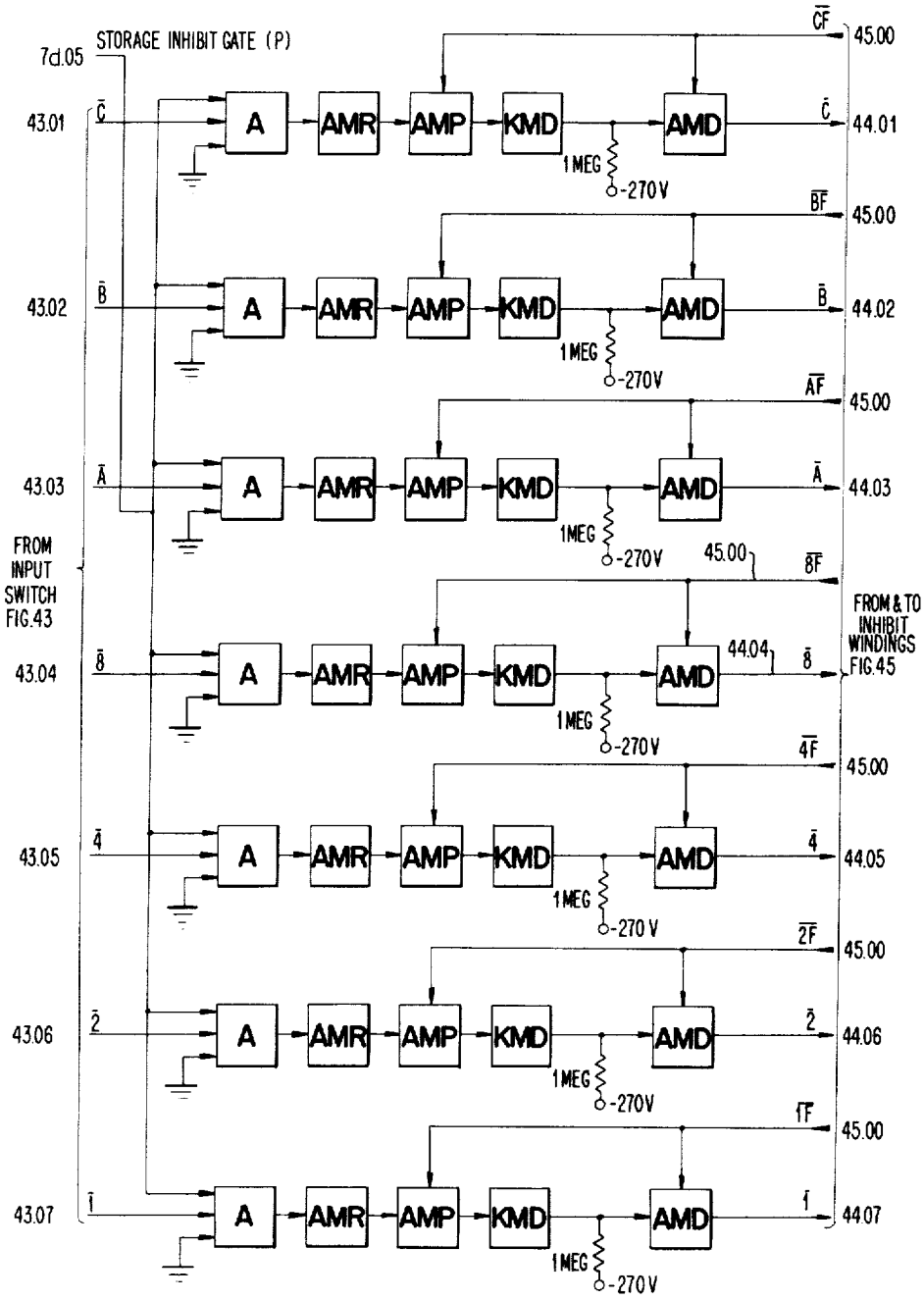


FIG.45

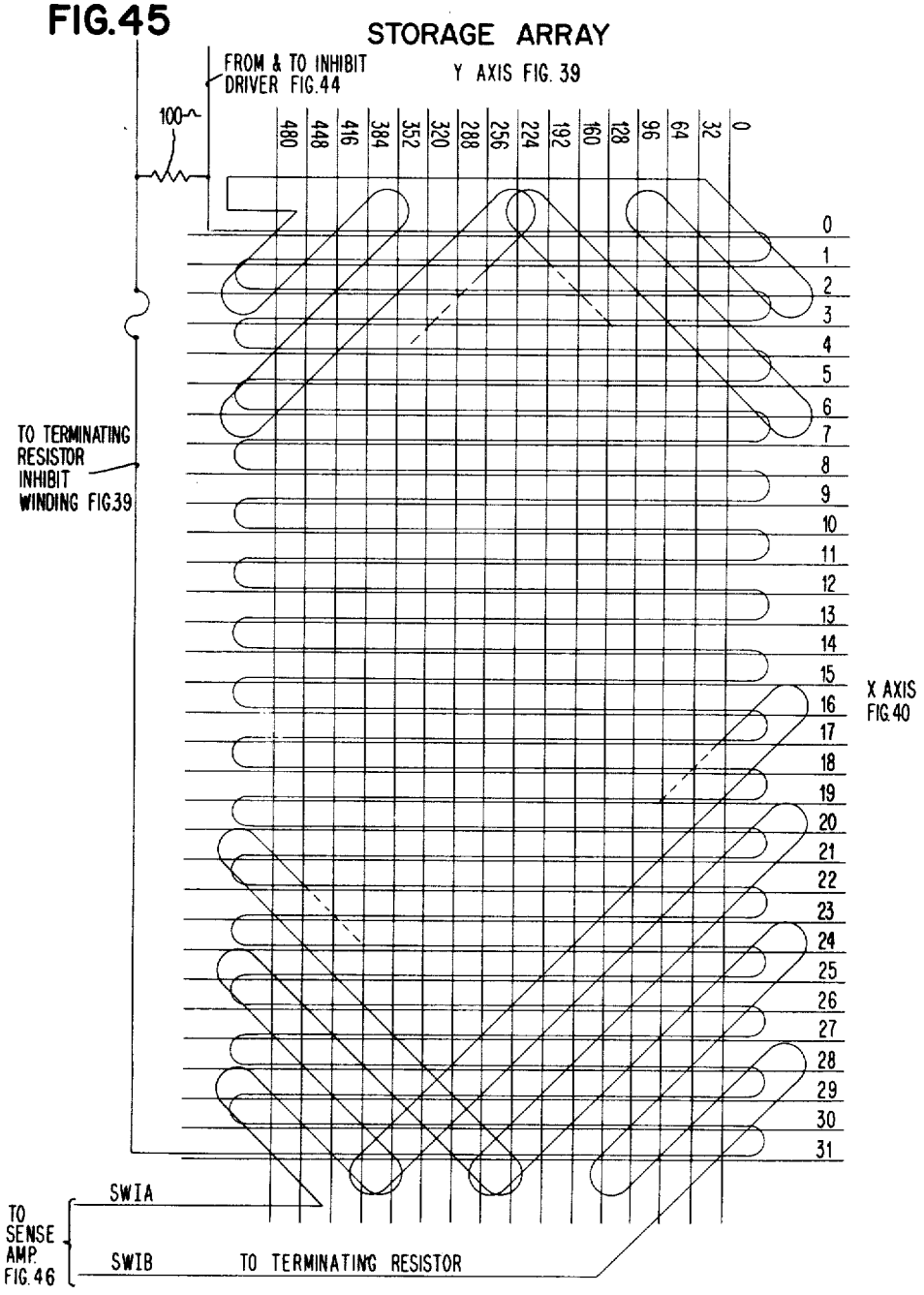
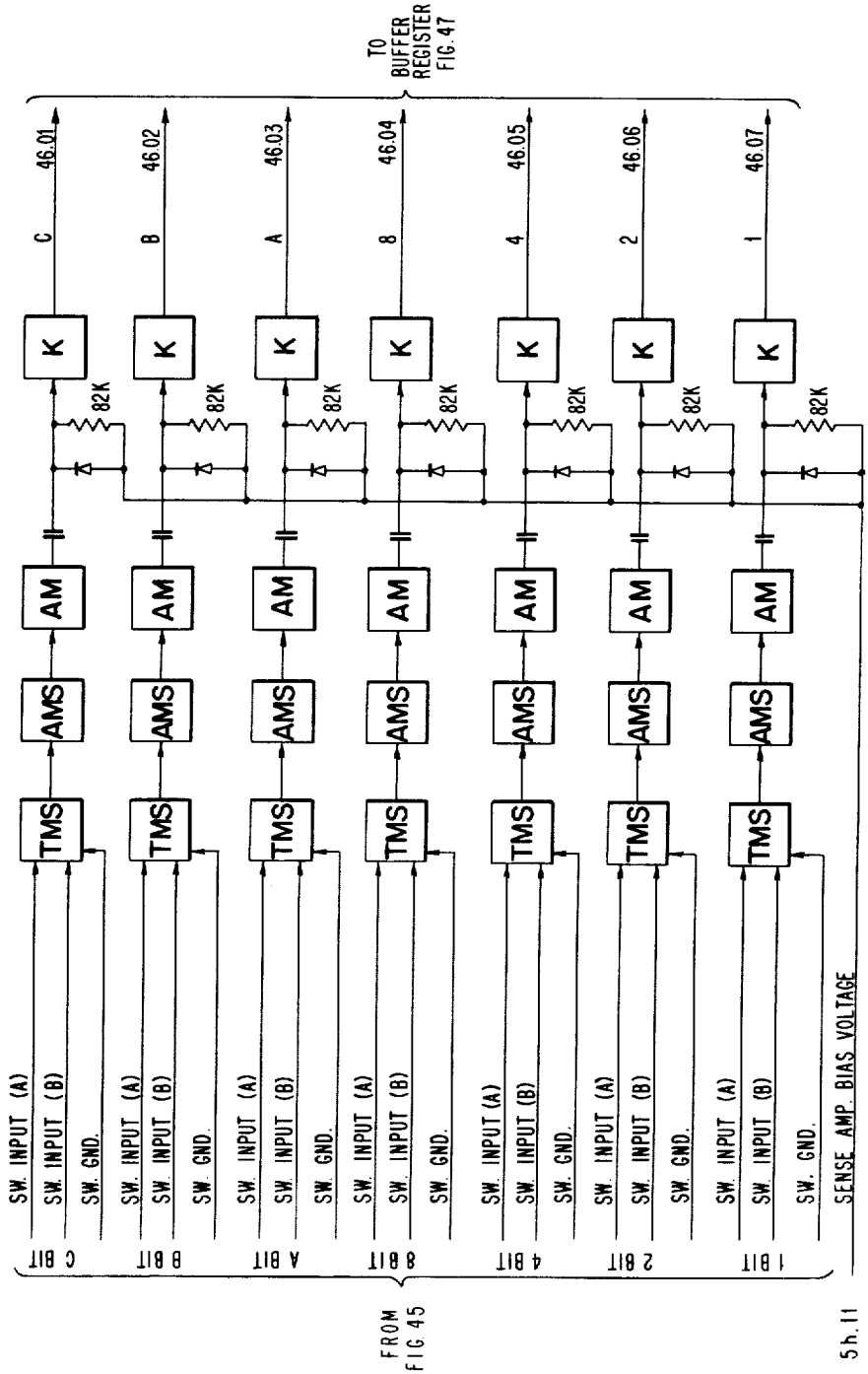
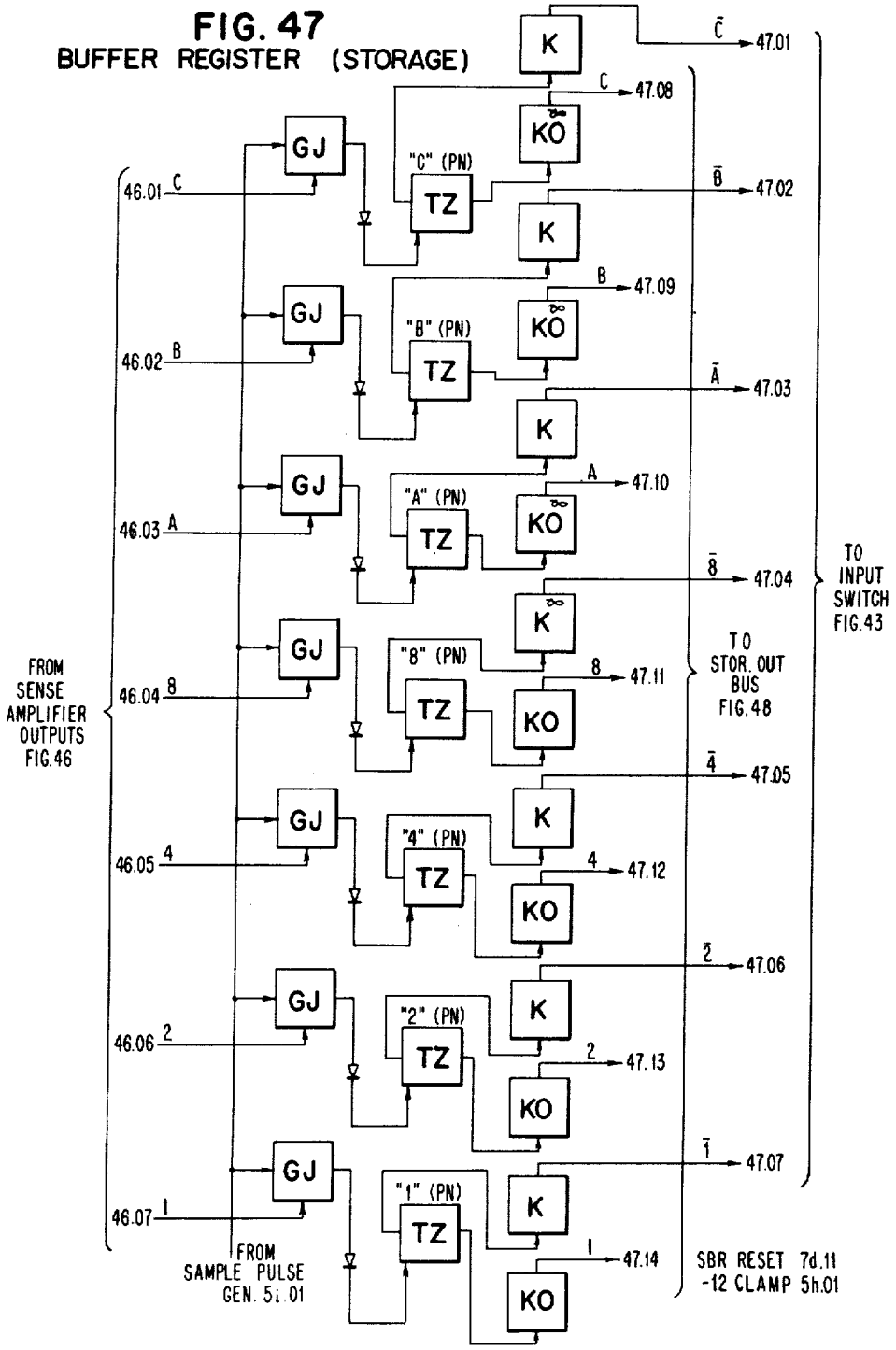

STORAGE ARRAY
FROM & TO INHIBIT DRIVER FIG.44
Y AXIS FIG. 39
100
480
448
416
384
352
320
288
256
224
192
160
128
96
64
32
0
0
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25
26
27
28
29
30
31
X AXIS FIG.40
TO TERMINATING RESISTOR INHIBIT WINDING FIG39
SWIA
TO SENSE AMP. FIG.46
SWIB
TO TERMINATING RESISTOR

FIG. 46
SENSE AMPLIFIER (STORAGE)



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FIG. 47
BUFFER REGISTER (STORAGE)



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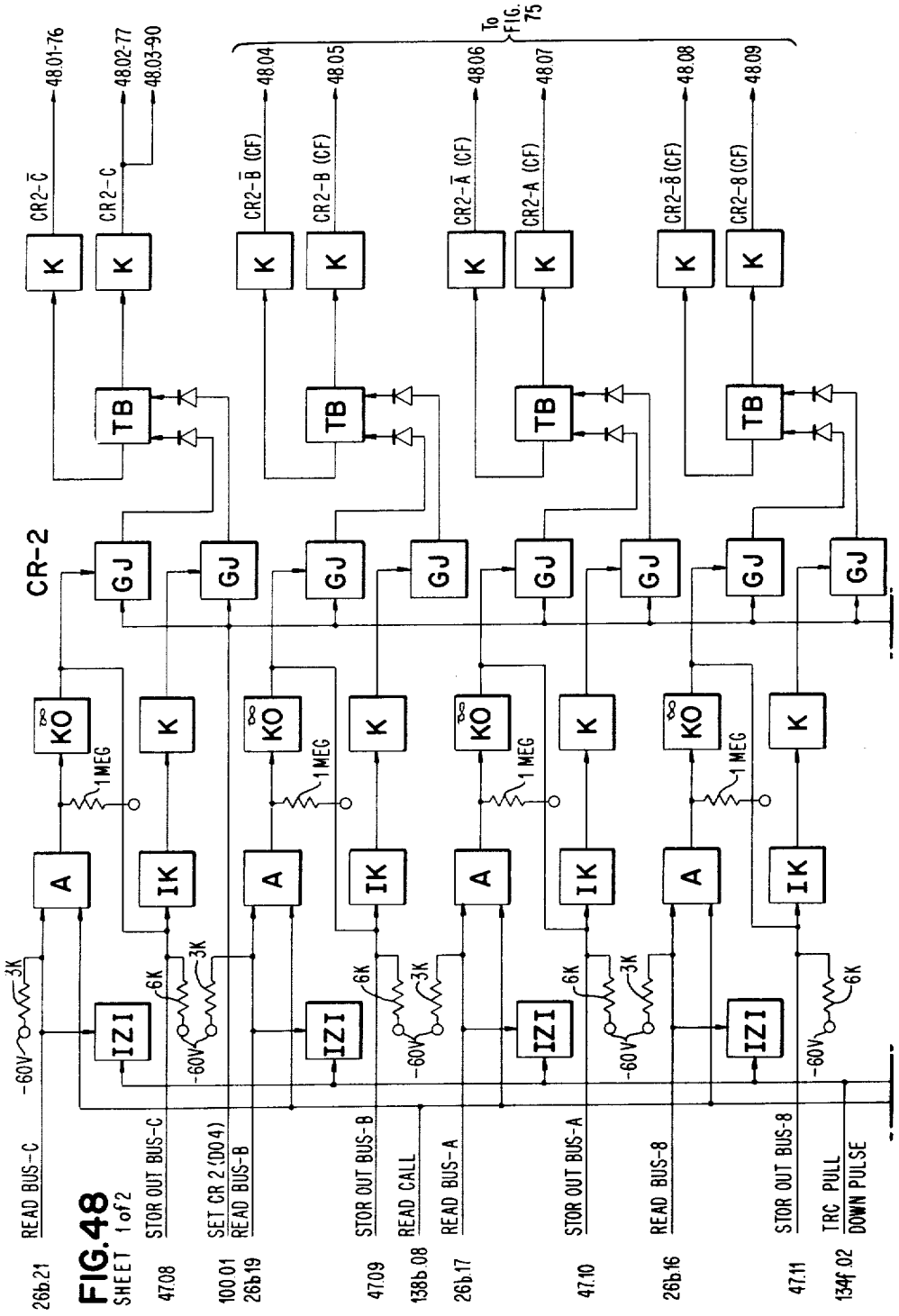


FIG. 48 SHEET 1 of 2

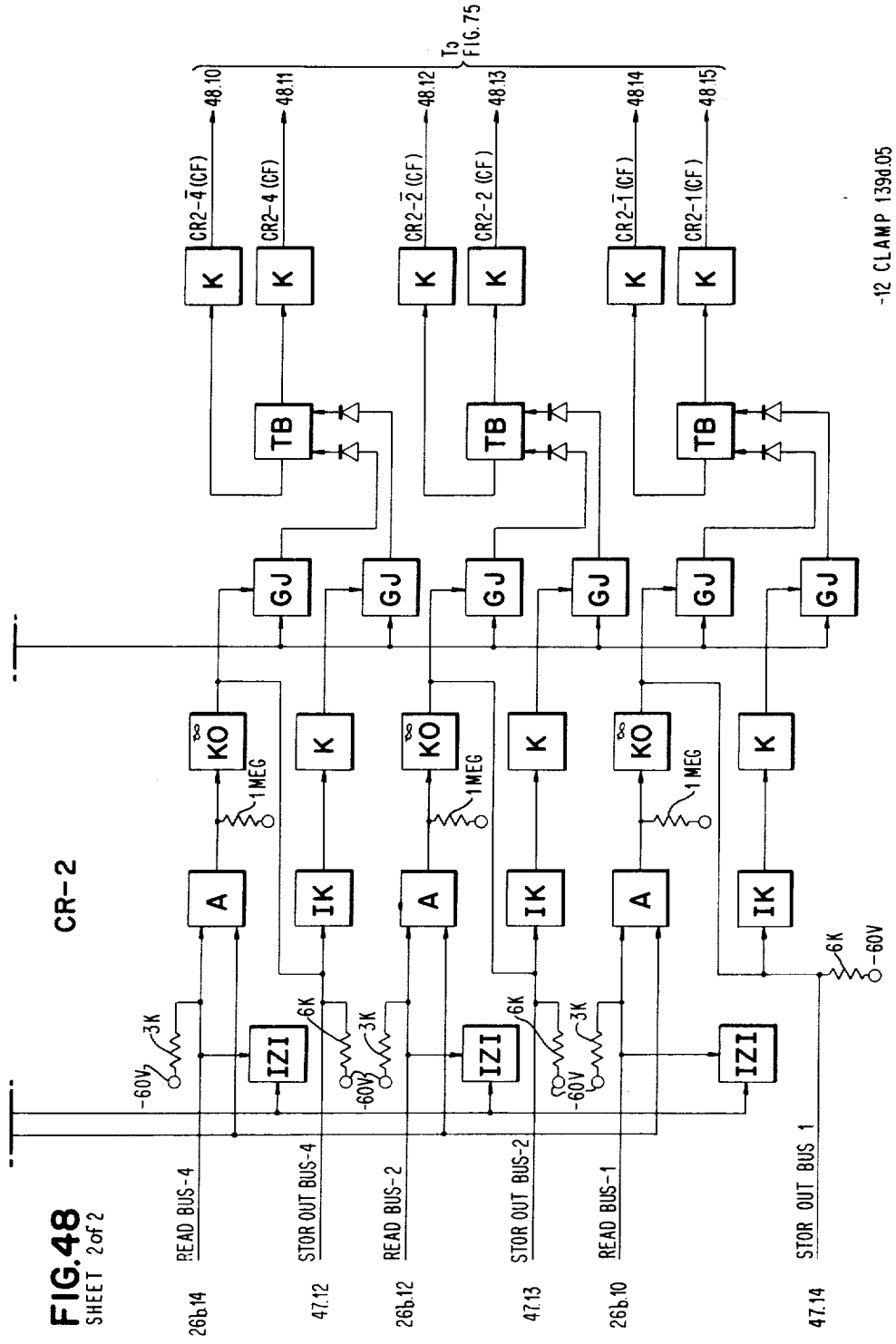
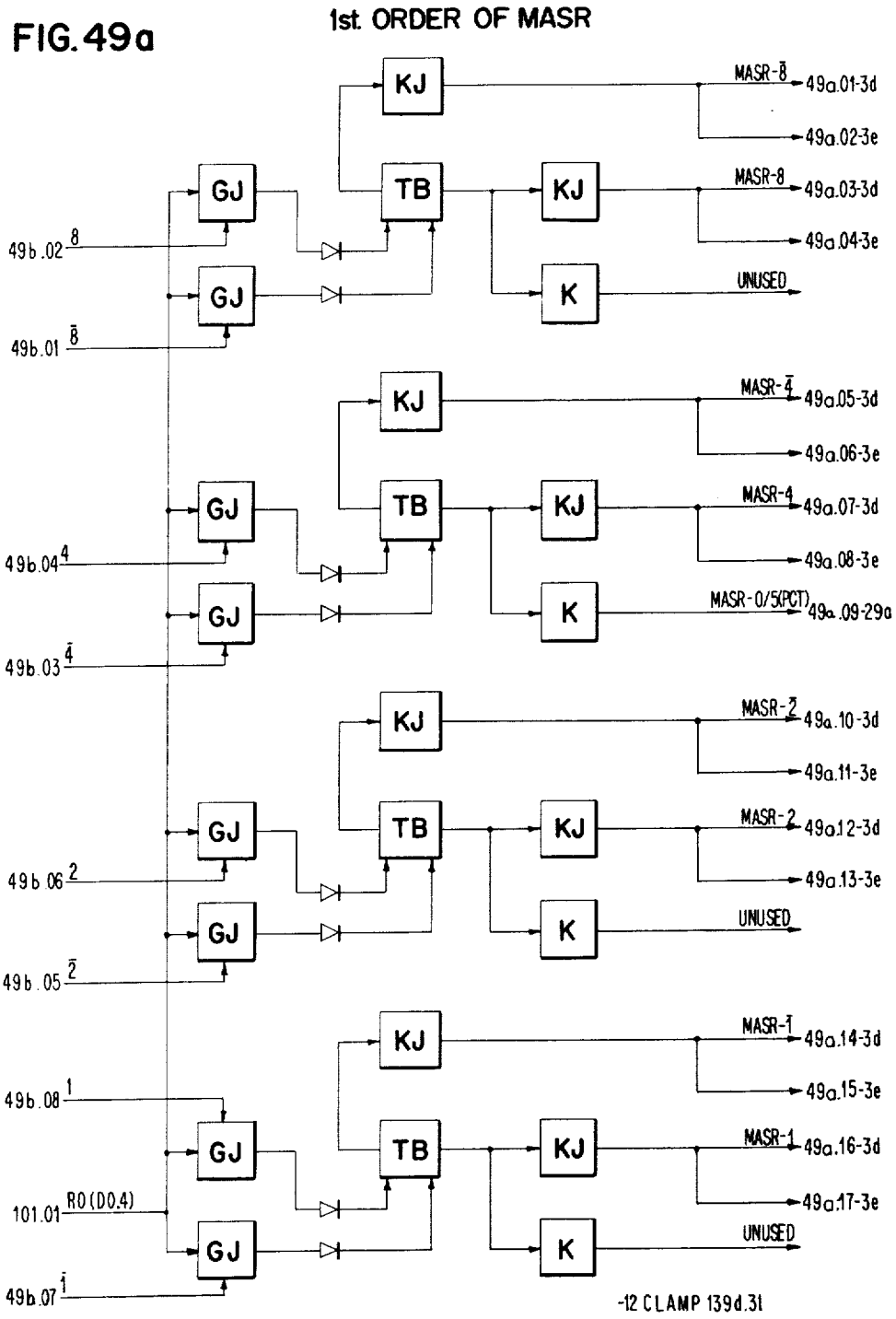
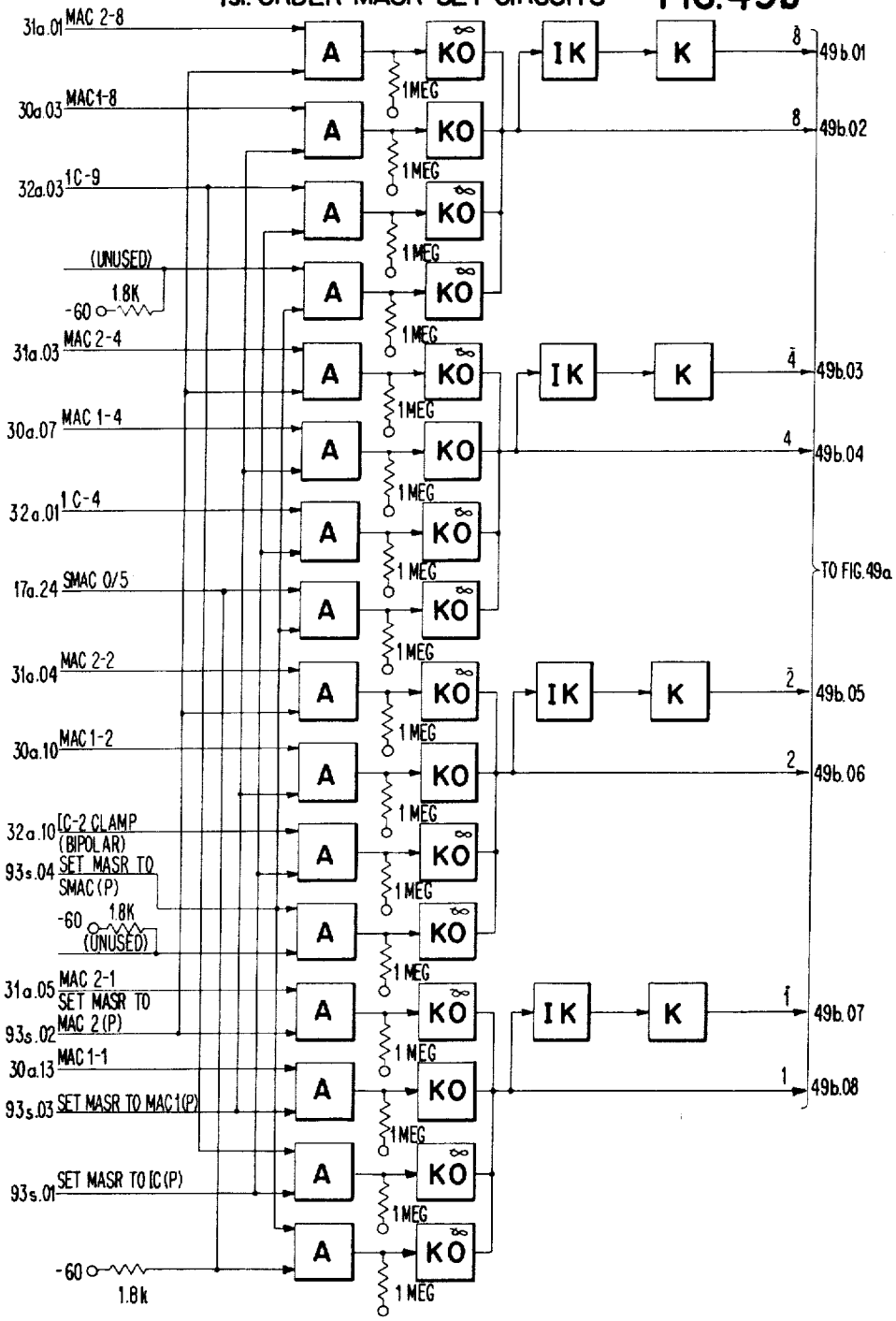


FIG. 48
SHEET 2 of 2

FIG. 49a


1st ORDER OF MASR
KJ
GJ
TB
K
MASR-8̄
49a.01-3d
49a.02-3e
MASR-8
49a.03-3d
49a.04-3e
UNUSED
49b.02 8
49b.01 8̄
MASR-4̄
49a.05-3d
49a.06-3e
MASR-4
49a.07-3d
49a.08-3e
MASR-0/5(PCT)
49a.09-29a
49b.04 4
49b.03 4̄
MASR-2̄
49a.10-3d
49a.11-3e
MASR-2
49a.12-3d
49a.13-3e
UNUSED
49b.06 2
49b.05 2̄
MASR-1̄
49a.14-3d
49a.15-3e
MASR-1
49a.16-3d
49a.17-3e
UNUSED
49b.08 1
101.01 R0 (D0.4)
49b.07 1̄
-12 CLAMP 139d.31

1st. ORDER MASR SET CIRCUITS FIG. 49b



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FIG. 49c

2nd. ORDER OF MASR

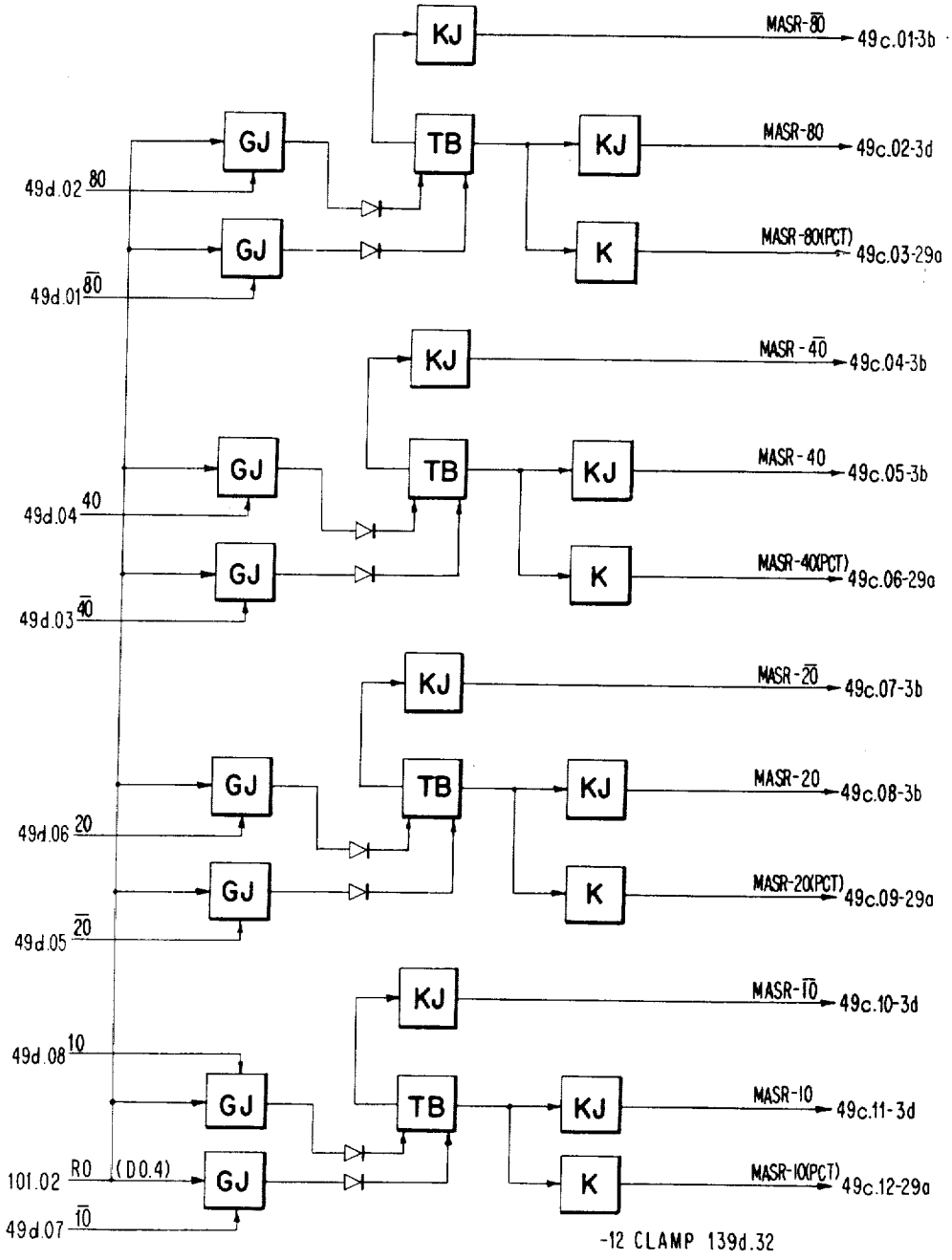
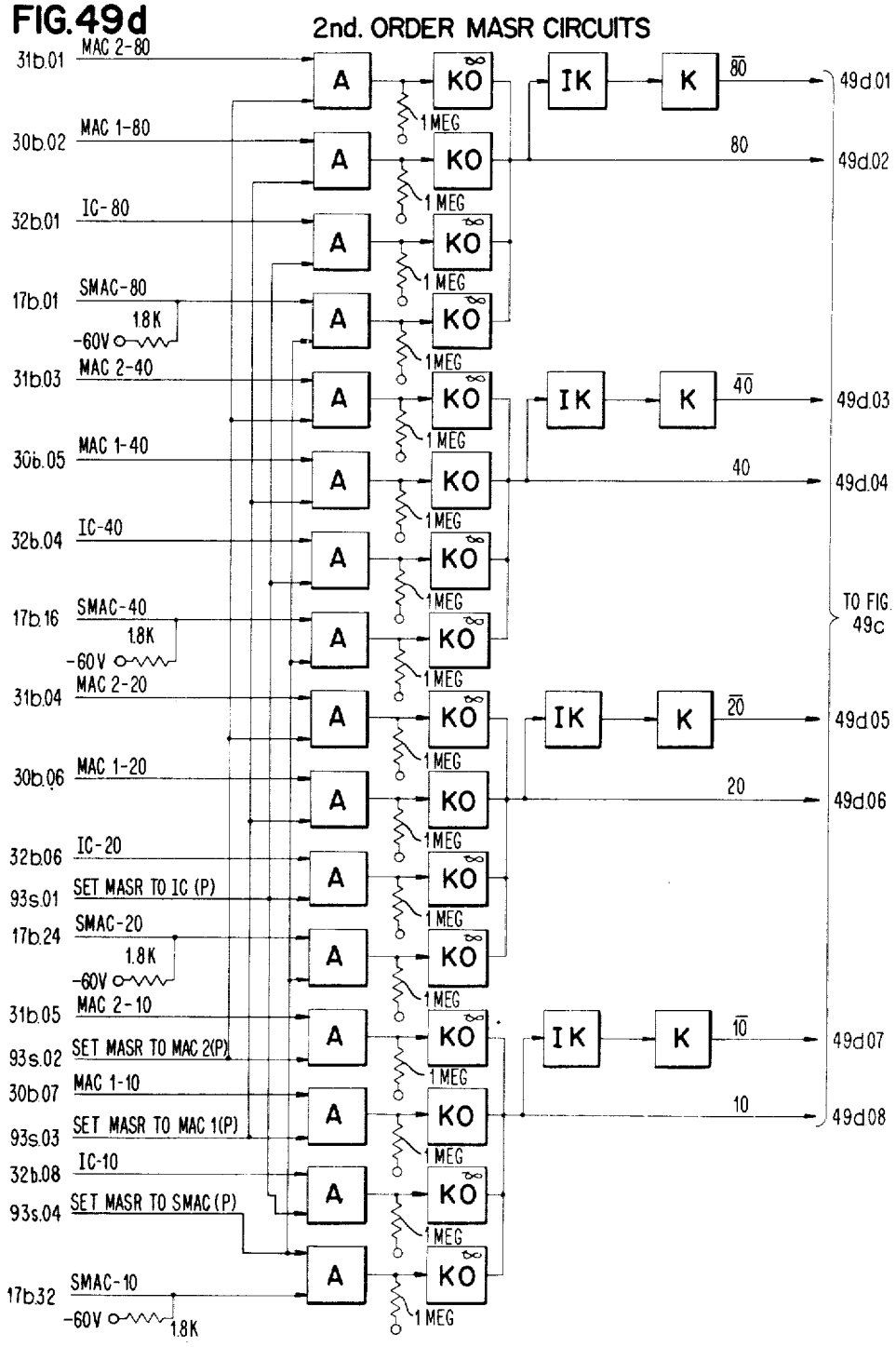


FIG. 49d


2nd. ORDER MASR CIRCUITS
31b.01 MAC 2-80
30b.02 MAC 1-80
32b.01 IC-80
17b.01 SMAC-80
1.8K
-60V
31b.03 MAC 2-40
30b.05 MAC 1-40
32b.04 IC-40
17b.16 SMAC-40
1.8K
-60V
31b.04 MAC 2-20
30b.06 MAC 1-20
32b.06 IC-20
93s.01 SET MASR TO IC (P)
17b.24 SMAC-20
1.8K
-60V
31b.05 MAC 2-10
93s.02 SET MASR TO MAC 2(P)
30b.07 MAC 1-10
93s.03 SET MASR TO MAC 1(P)
32b.08 IC-10
93s.04 SET MASR TO SMAC (P)
17b.32 SMAC-10
-60V
1.8K
A
KO
1 MEG
IK
K
80
80
40
40
20
20
10
10
49d.01
49d.02
49d.03
49d.04
TO FIG. 49c
49d.05
49d.06
49d.07
49d.08

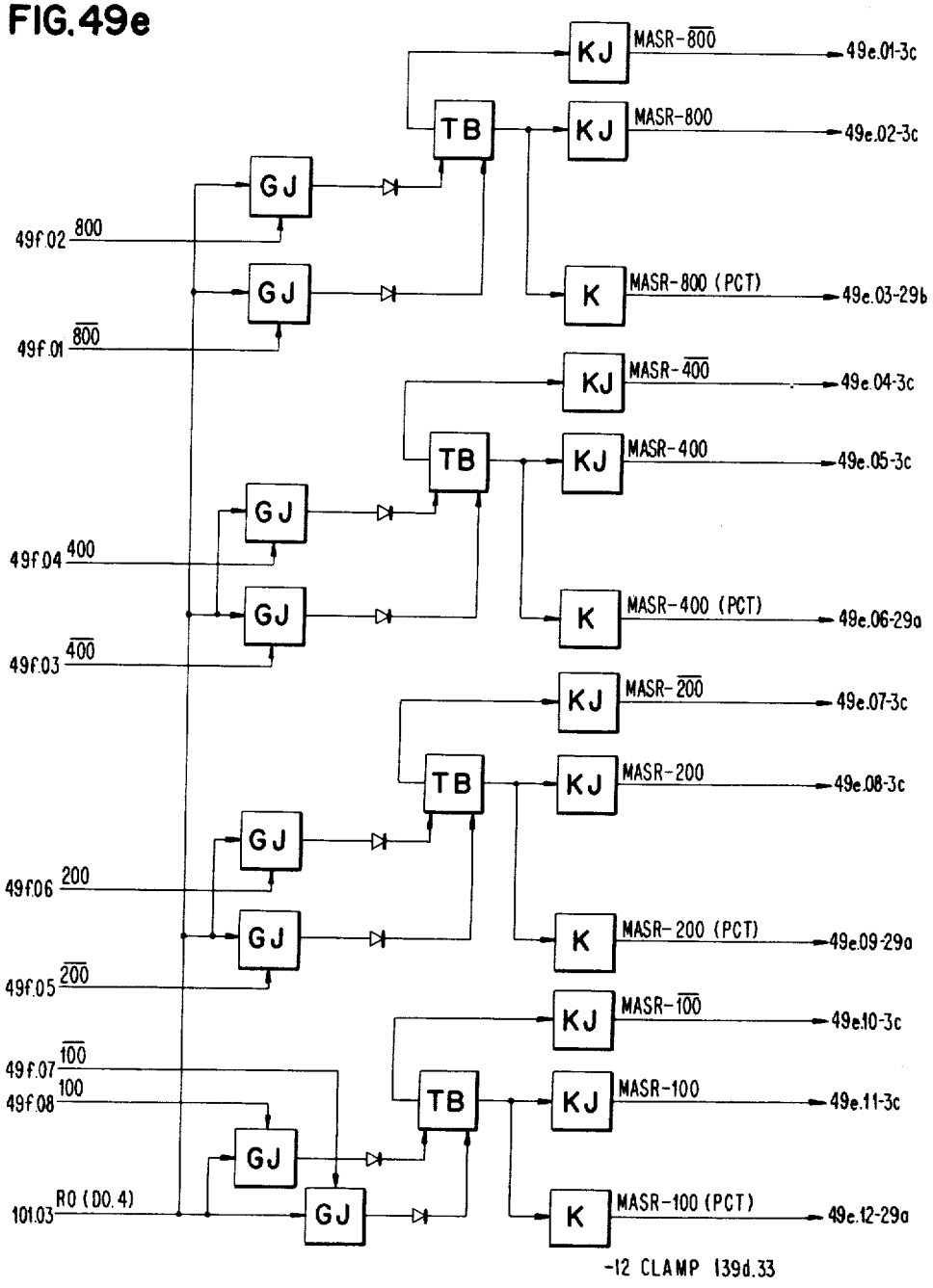
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3rd. ORDER OF MASR

FIG. 49e



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FIG. 49f 3rd. ORDER MASR SET CIRCUIT

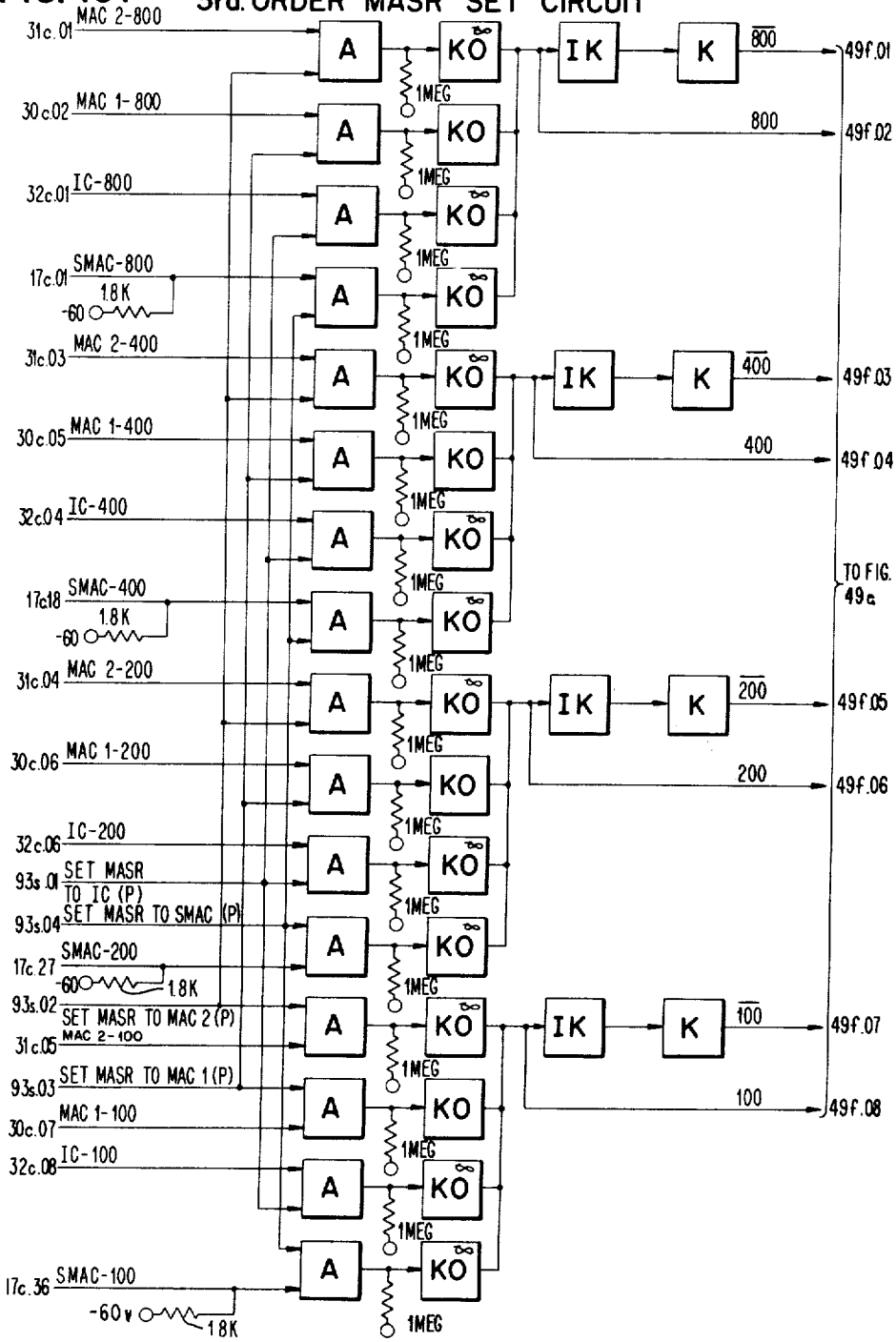
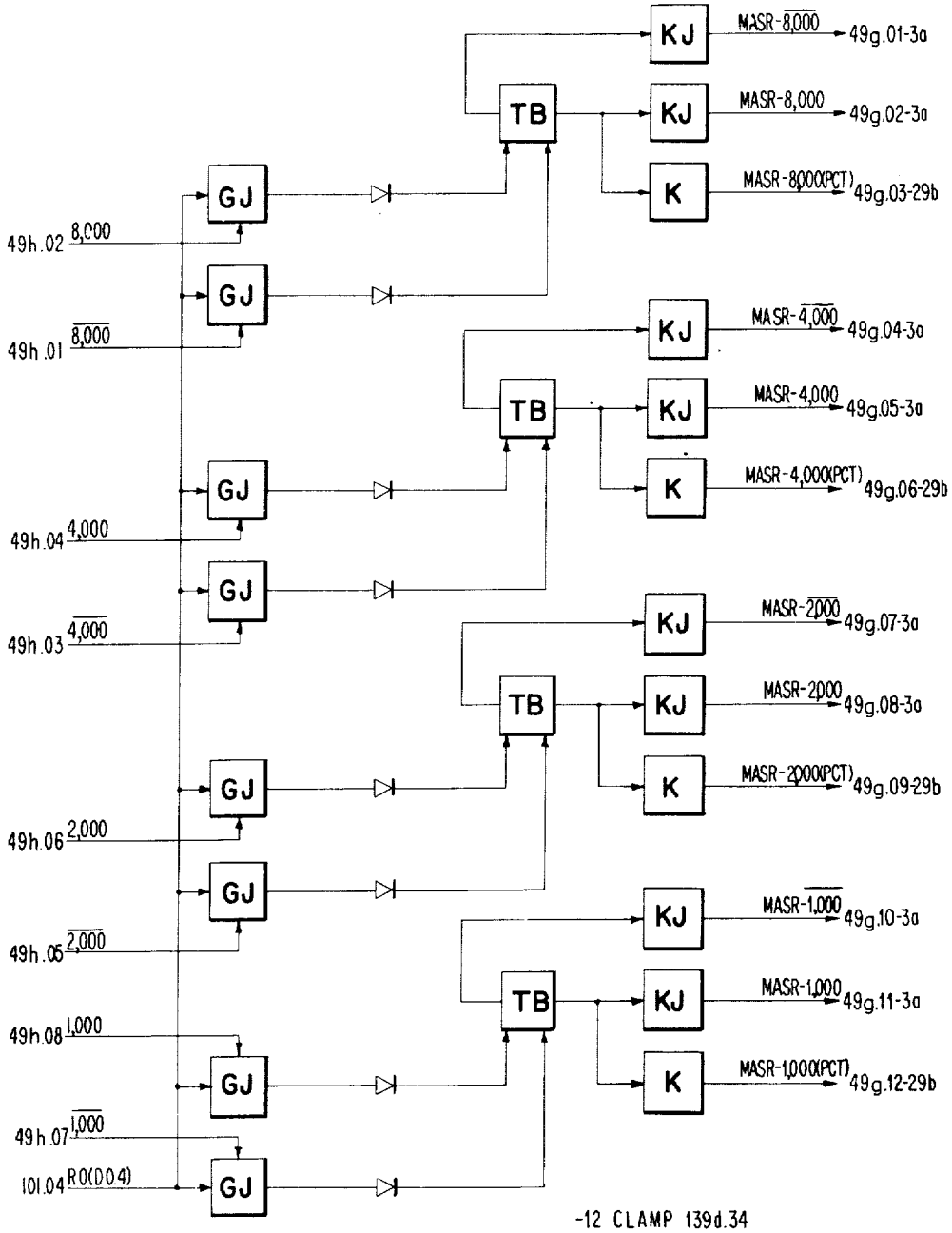


FIG.49g 4th. ORDER OF MASR



-12 CLAMP 139d.34

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FIG. 49h 4th. ORDER MASR SET CIRCUITS

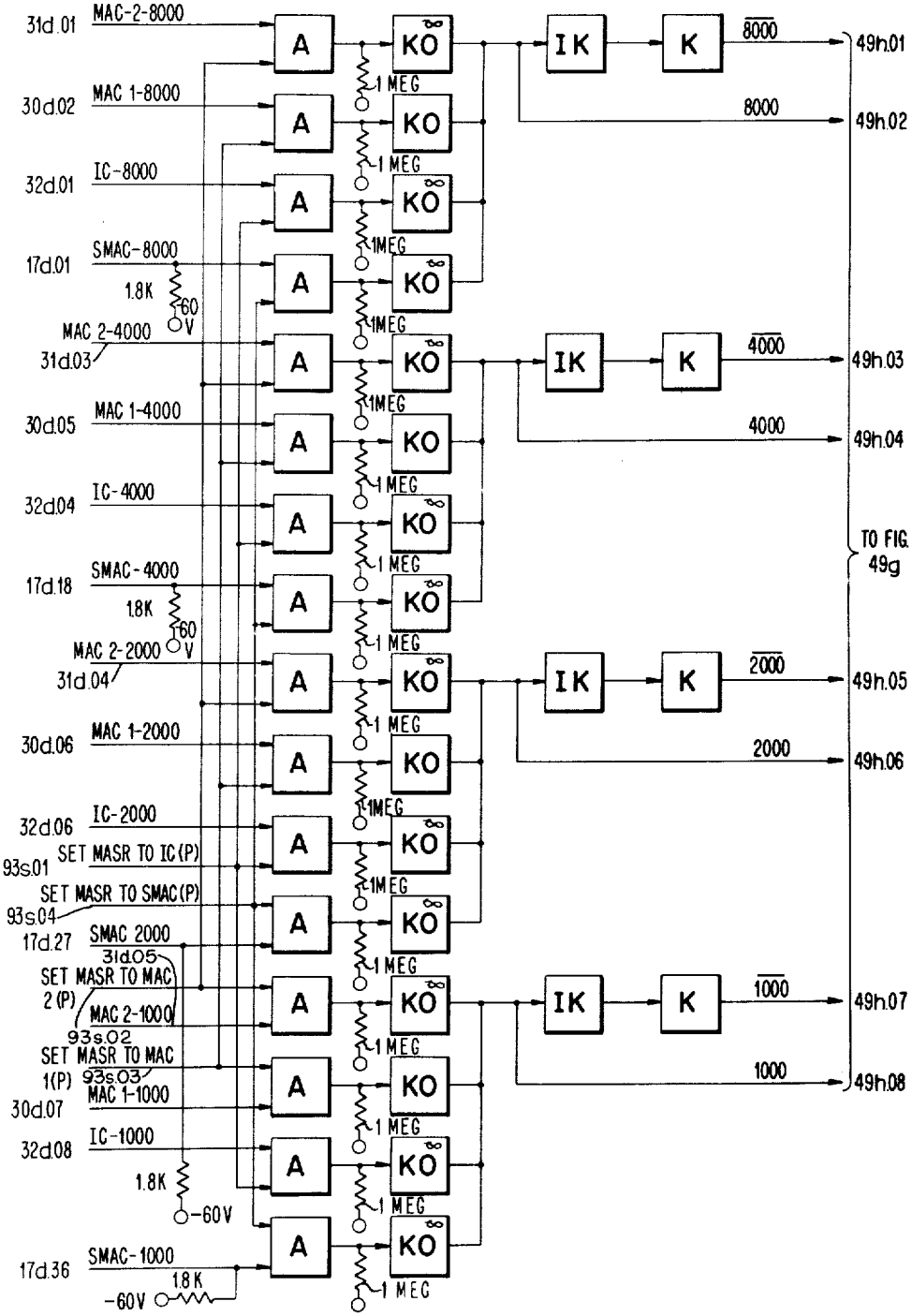
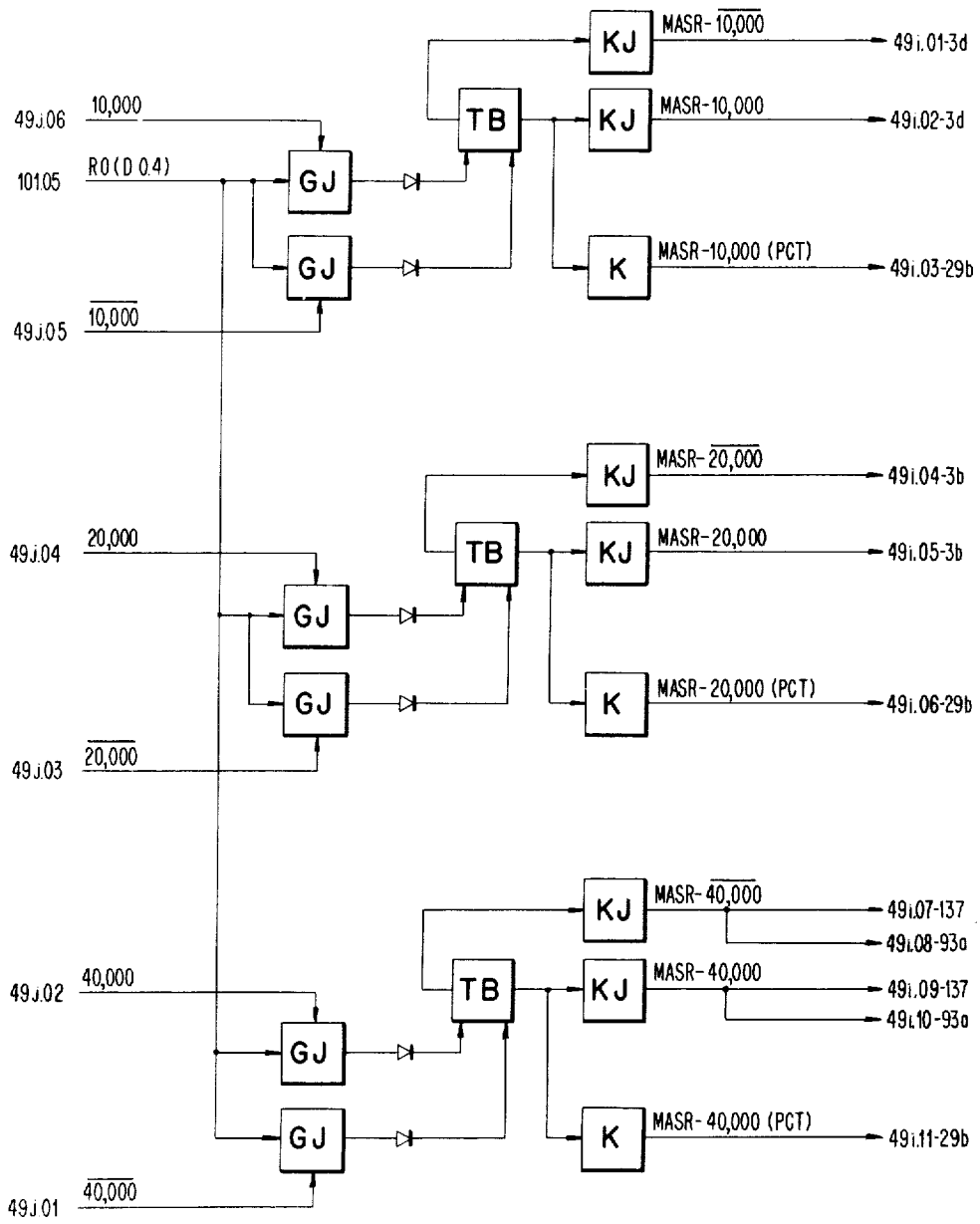


FIG.49i

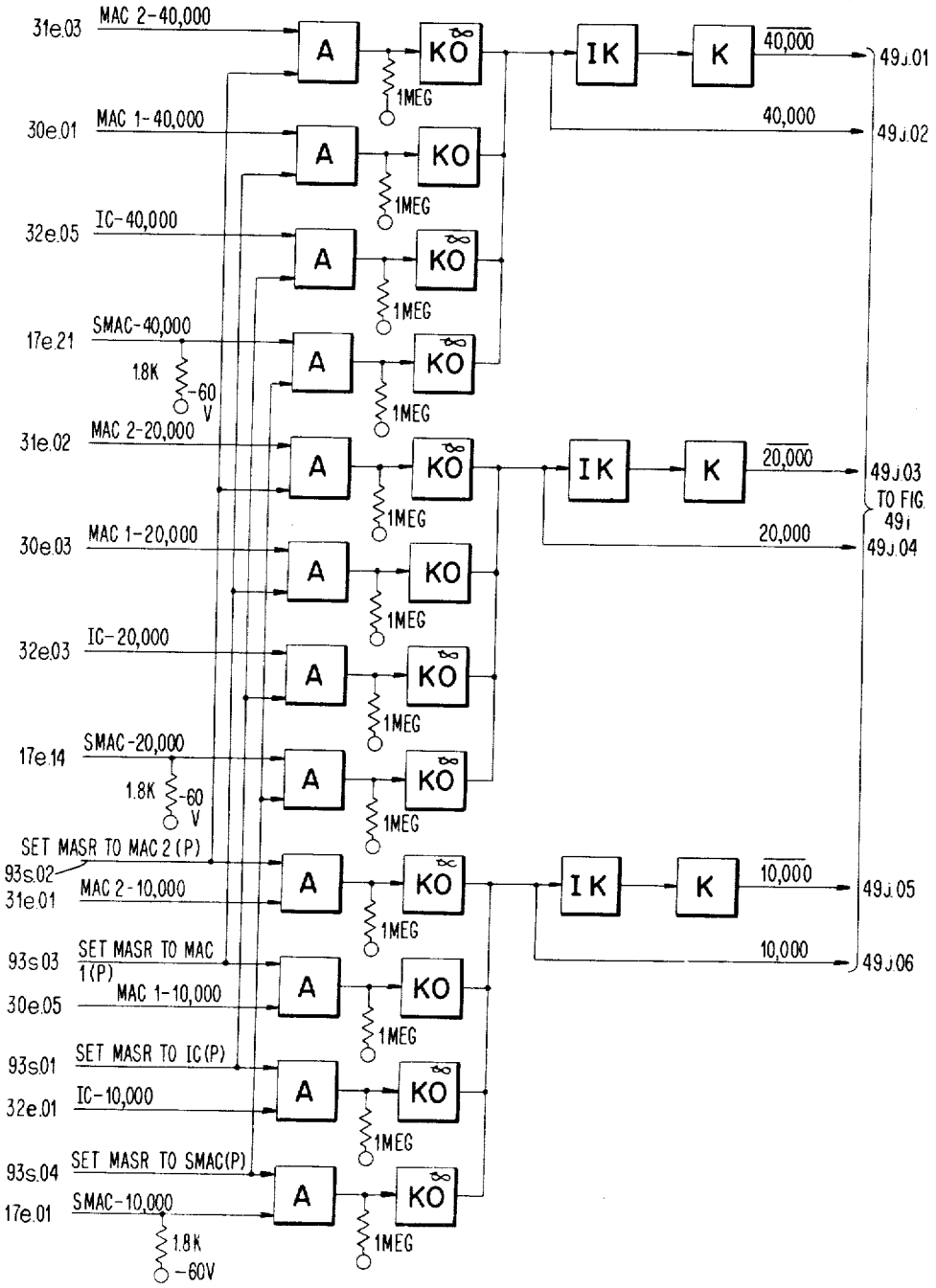


-12 CLAMP 139d.35

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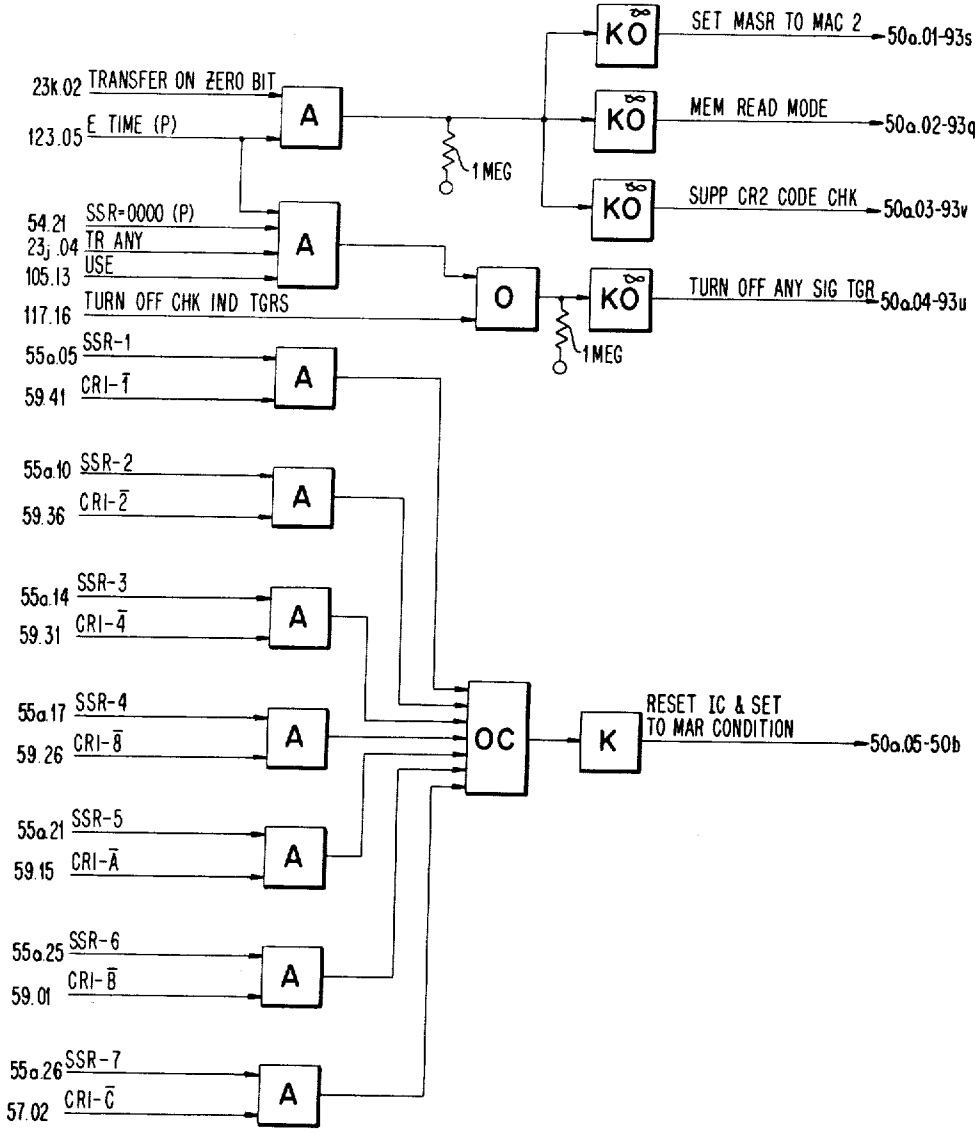
FIG. 49j

5th. ORDER MASR SET CIRCUITS



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FIG. 50a TRANSFER ROUTING CONTROLS



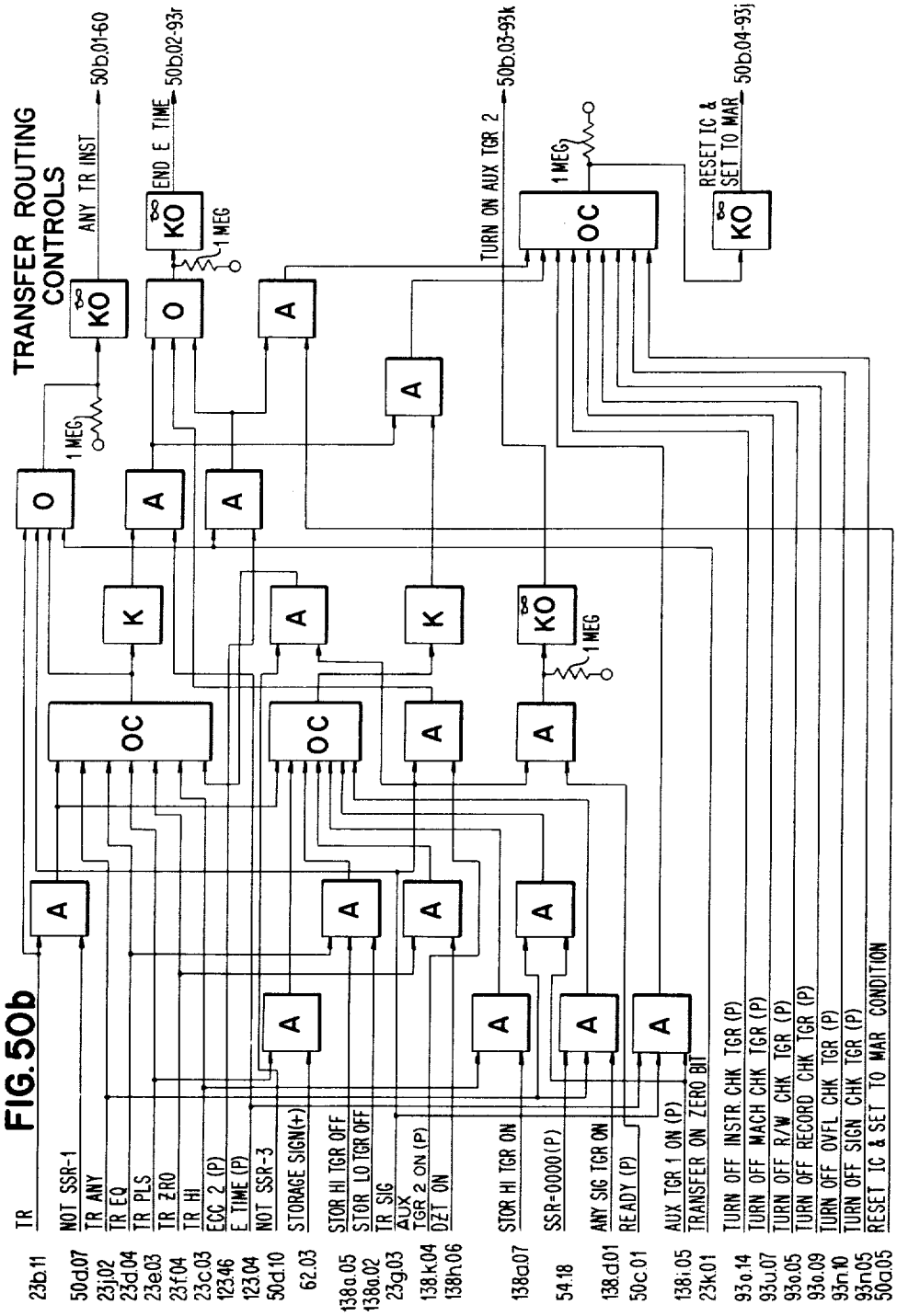

TRANSFER ROUTING CONTROLS
ANY TR INST
50b.01-60
END E TIME
50b.02-93r
TURN ON AUX TGR 2
50b.03-93k
RESET IC & SET TO MAR
50b.04-93j
1 MEG
O
A
K
KO
OC
TR
NOT SSR-1
TR ANY
TR EQ
TR PLS
TR ZRO
TR HI
ECC 2 (P)
E TIME (P)
NOT SSR-3
STORAGE SIGN(+)
STOR HI TGR OFF
STOR LO TGR OFF
TR SIG
AUX TGR 2 ON (P)
DZT ON
STOR HI TGR ON
SSR=0000 (P)
ANY SIG TGR ON
READY (P)
AUX TGR 1 ON (P)
TRANSFER ON ZERO BIT
TURN OFF INSTR CHK TGR (P)
TURN OFF MACH CHK TGR (P)
TURN OFF R/W CHK TGR (P)
TURN OFF RECORD CHK TGR (P)
TURN OFF OVFL CHK TGR (P)
TURN OFF SIGN CHK TGR (P)
RESET IC & SET TO MAR CONDITION
23b.11
50d.07
23j.02
23d.04
23e.03
23f.04
23c.03
123.46
123.04
50d.10
62.03
138a.05
138a.02
23g.03
138k.04
138h.06
138a.07
54.18
138d.01
50c.01
138i.05
23k.01
93a.14
93u.07
93a.05
93a.09
93n.10
93n.05
50a.05

FIG. 50b

FIG.50c TRANSFER ROUTING CONTROLS

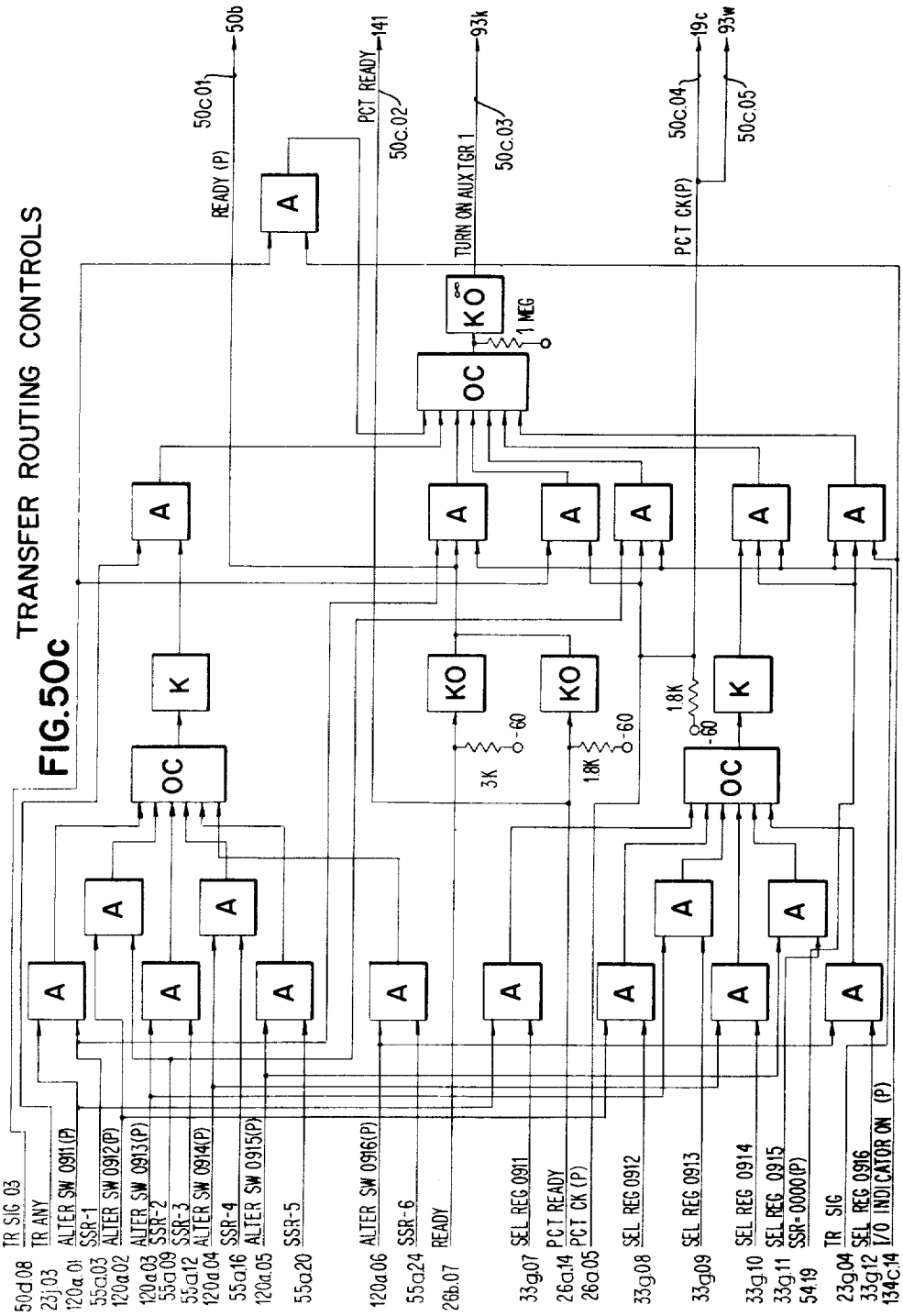


FIG.50d TRANSFER ROUTING CONTROLS

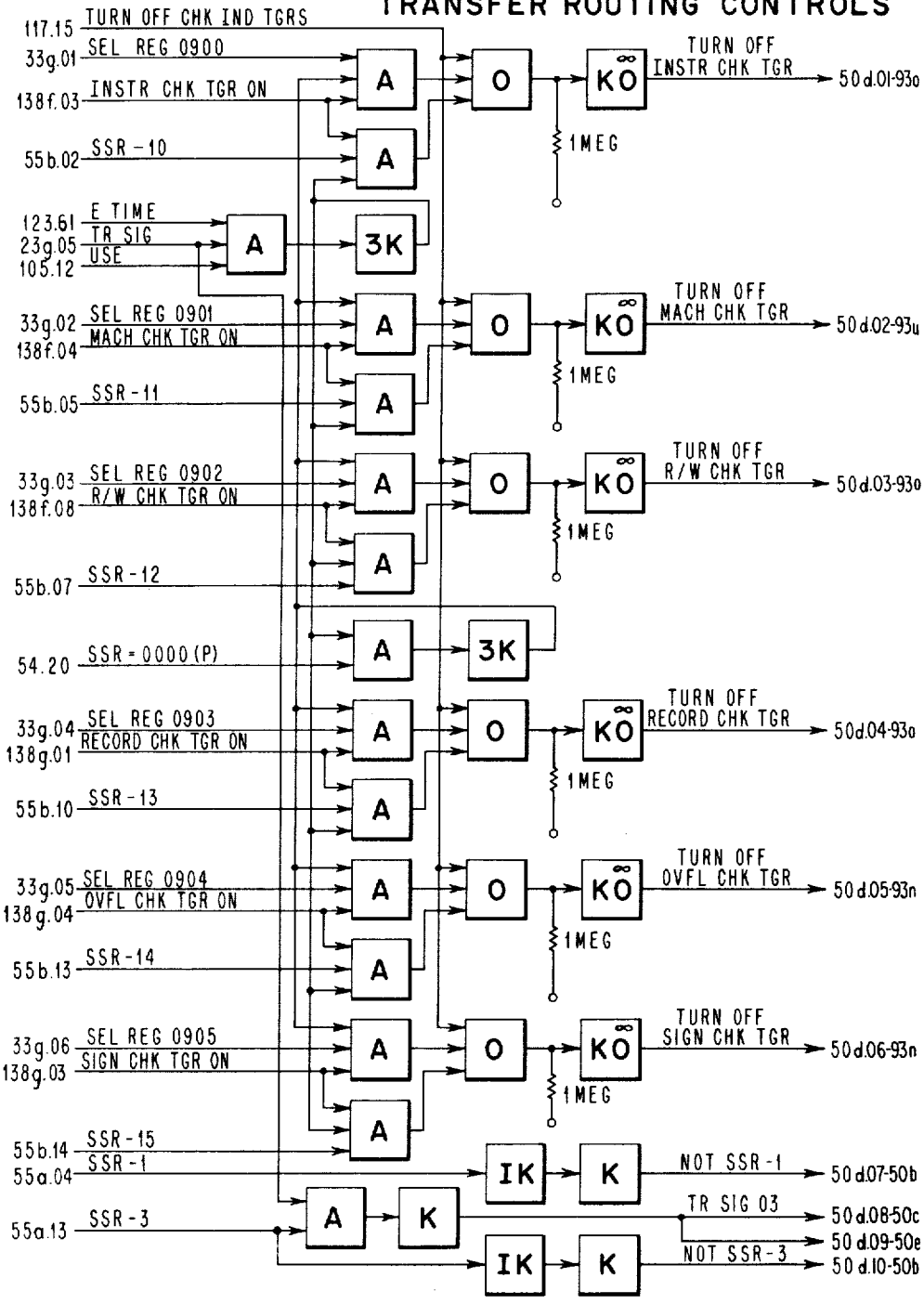


FIG. 50e TRANSFER 01

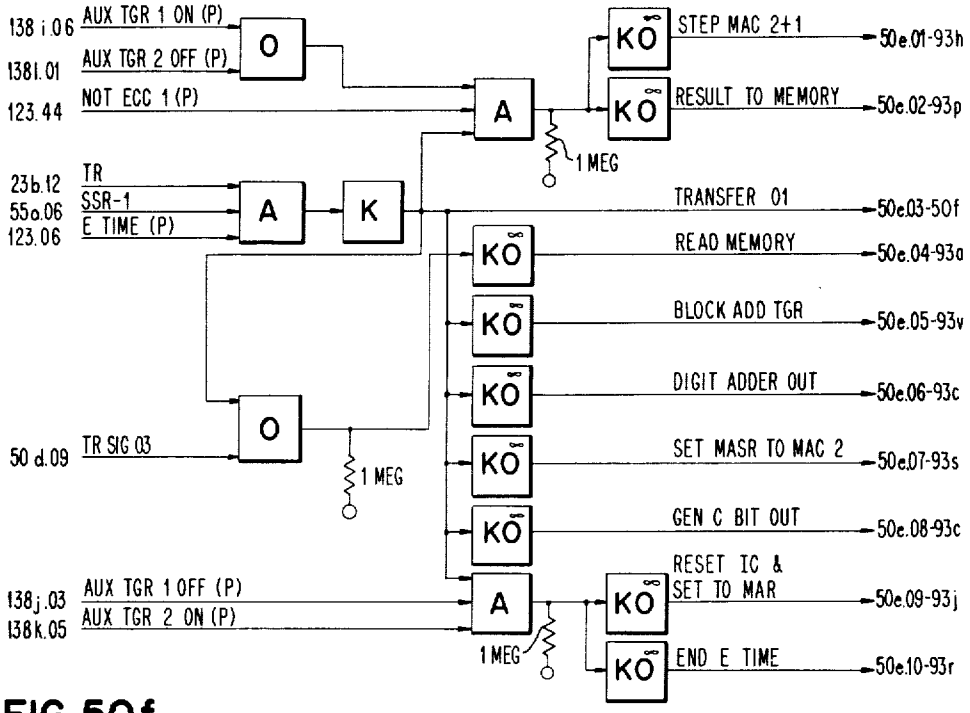
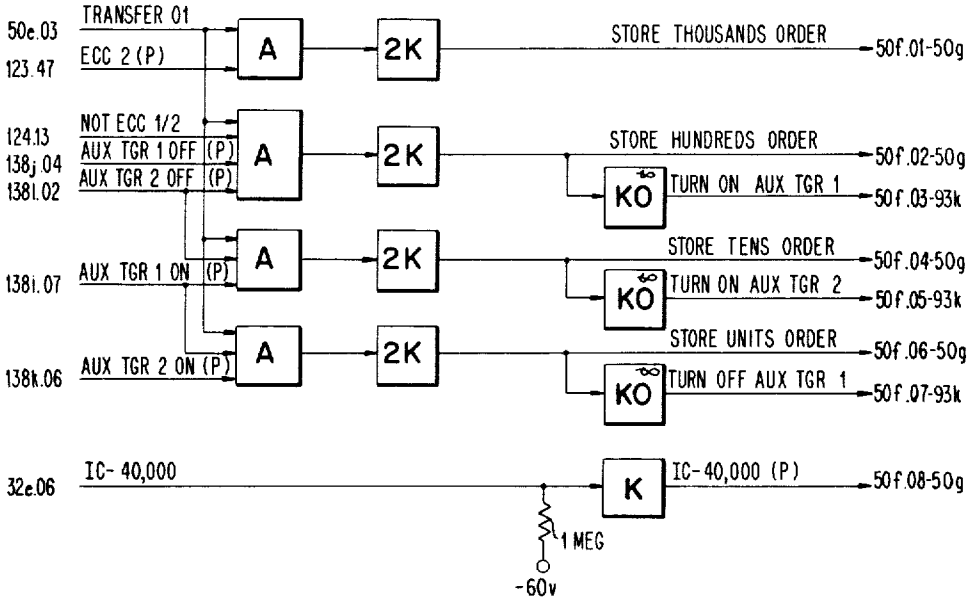
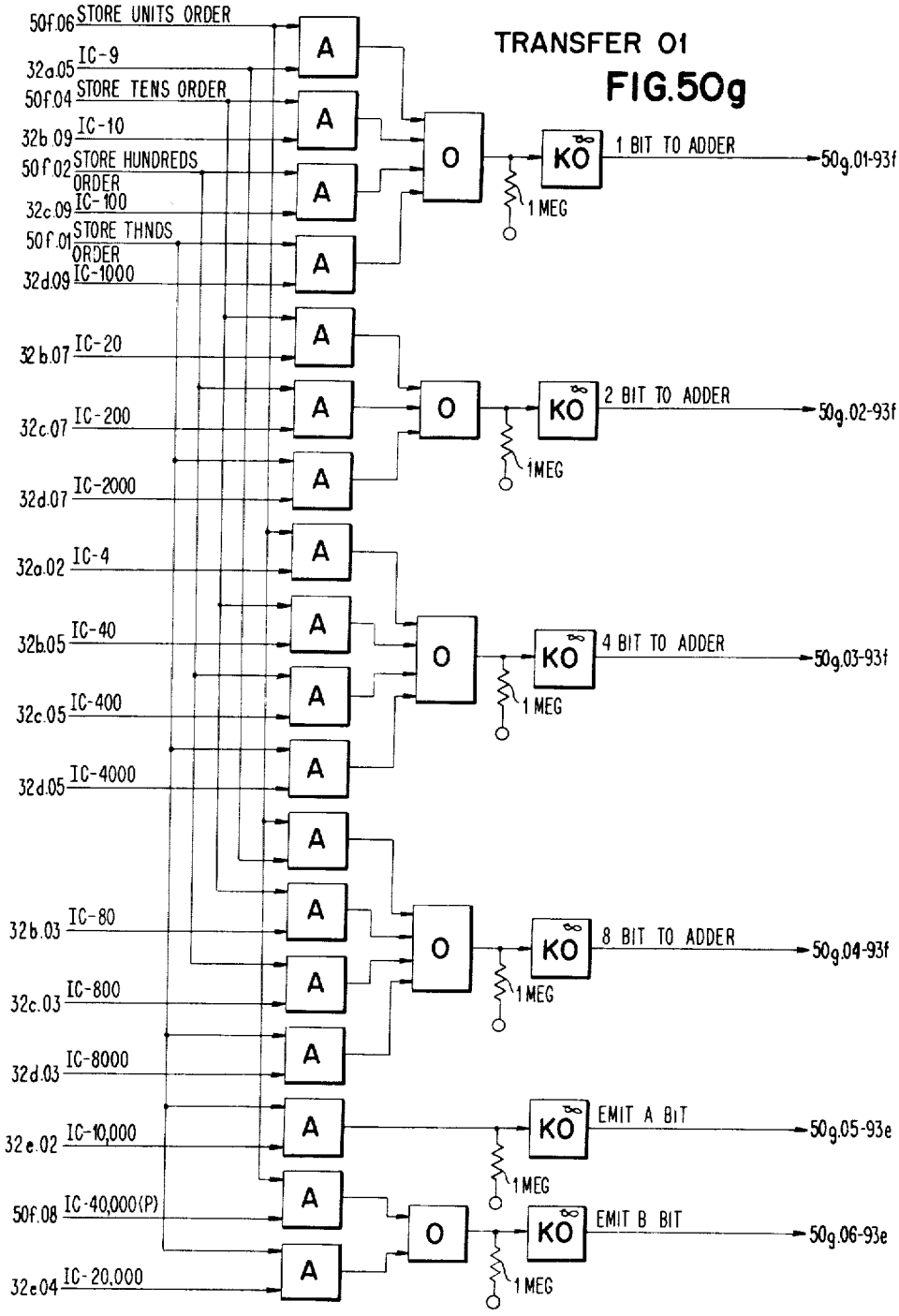


FIG. 50f TRANSFER 01




TRANSFER 01
FIG.50g
50f.06 STORE UNITS ORDER
32a.05 IC-9
50f.04 STORE TENS ORDER
32b.09 IC-10
50f.02 STORE HUNDREDS ORDER
32c.09 IC-100
50f.01 STORE THNDS ORDER
32d.09 IC-1000
32b.07 IC-20
32c.07 IC-200
32d.07 IC-2000
32a.02 IC-4
32b.05 IC-40
32c.05 IC-400
32d.05 IC-4000
32b.03 IC-80
32c.03 IC-800
32d.03 IC-8000
32e.02 IC-10,000
50f.08 IC-40,000(P)
32e.04 IC-20,000
A
O
KO
1 MEG
1 BIT TO ADDER
50g.01-93f
2 BIT TO ADDER
50g.02-93f
4 BIT TO ADDER
50g.03-93f
8 BIT TO ADDER
50g.04-93f
EMIT A BIT
50g.05-93e
EMIT B BIT
50g.06-93e

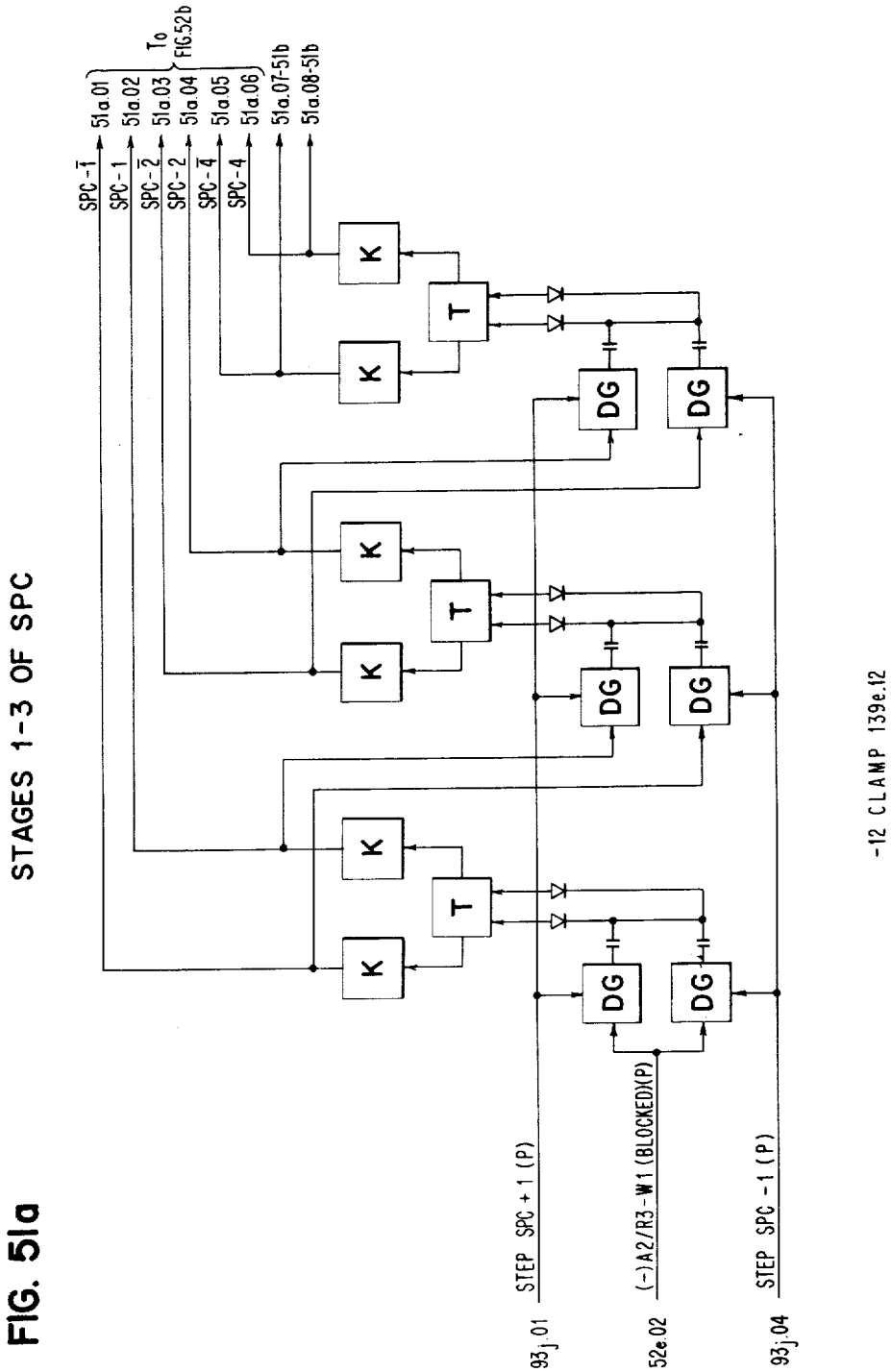

STAGES 1-3 OF SPC
SPC-1
SPC-1
SPC-2
SPC-2
SPC-4
SPC-4
51a.01
51a.02
51a.03
51a.04
51a.05
51a.06
To FIG.52b
51a.07-51b
51a.08-51b
K
T
DG
STEP SPC+1 (P)
(-)A2/R3-W1 (BLOCKED)(P)
STEP SPC-1 (P)
93j.01
52e.02
93j.04
-12 CLAMP 139e.12

FIG. 51a

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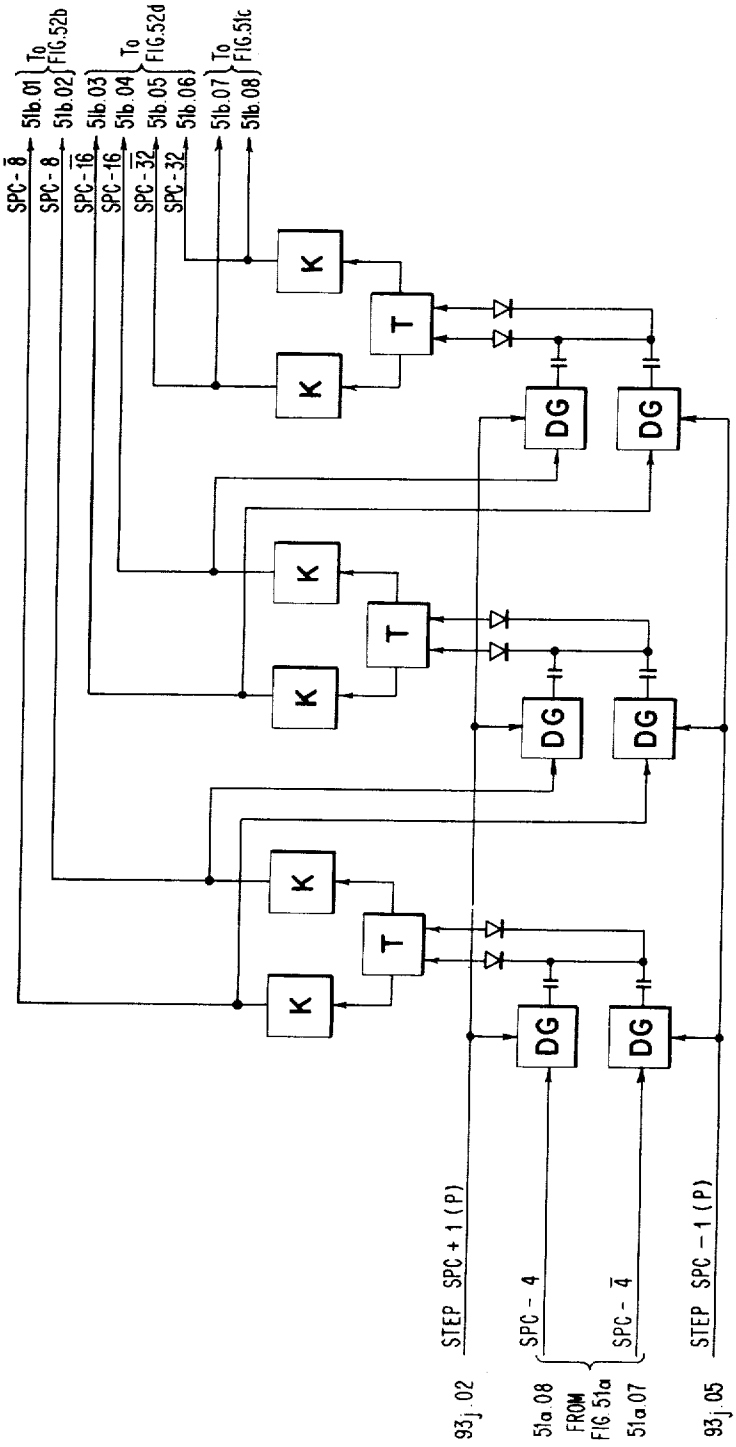
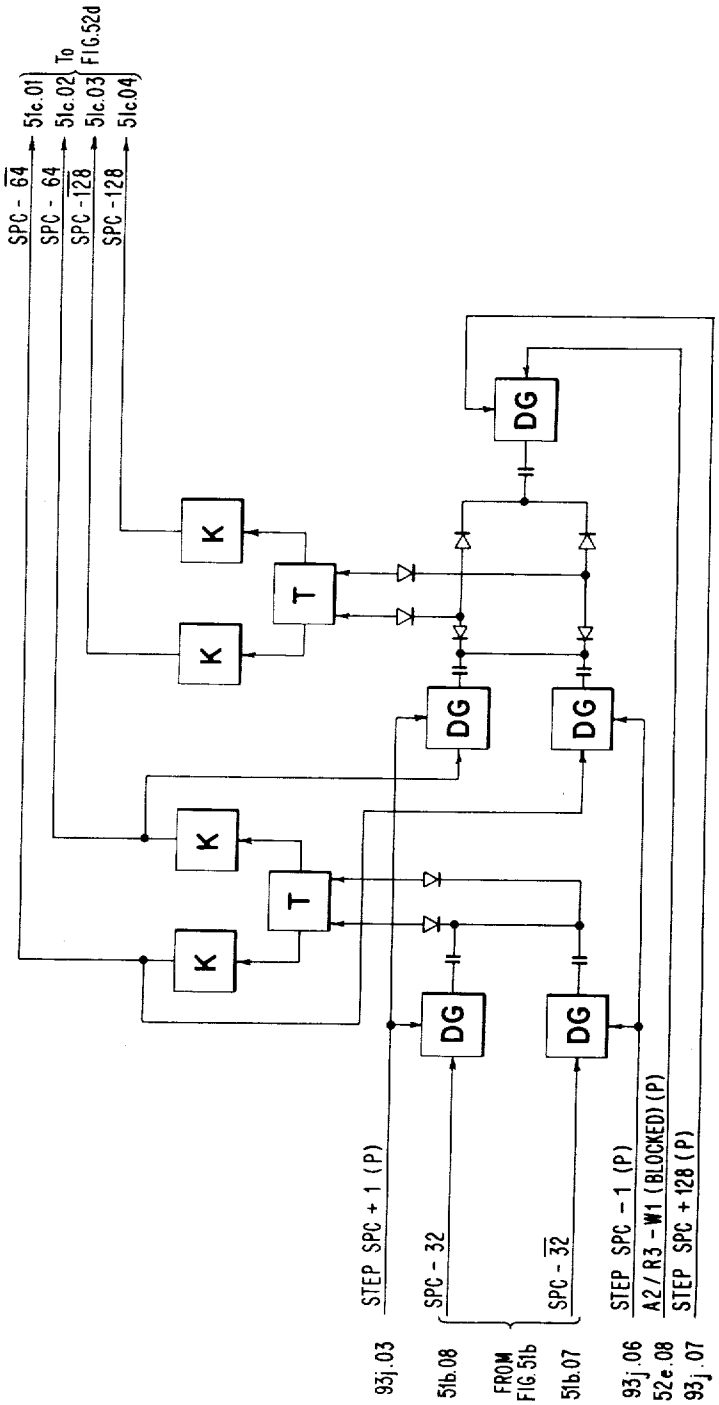


FIG. 51b

FIG. 51c

STAGES 7-8 OF SPC

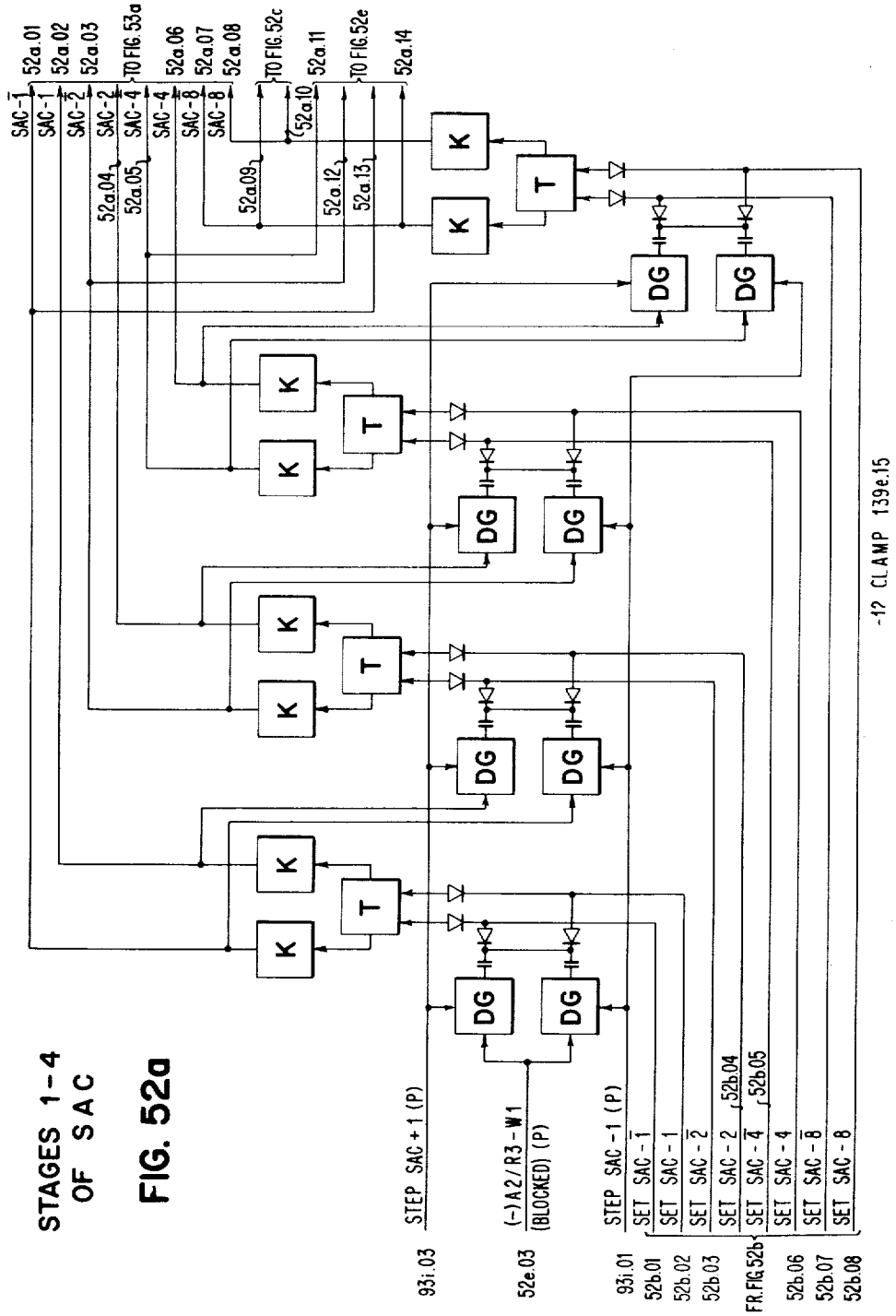


-12 CLAMP 139e.14

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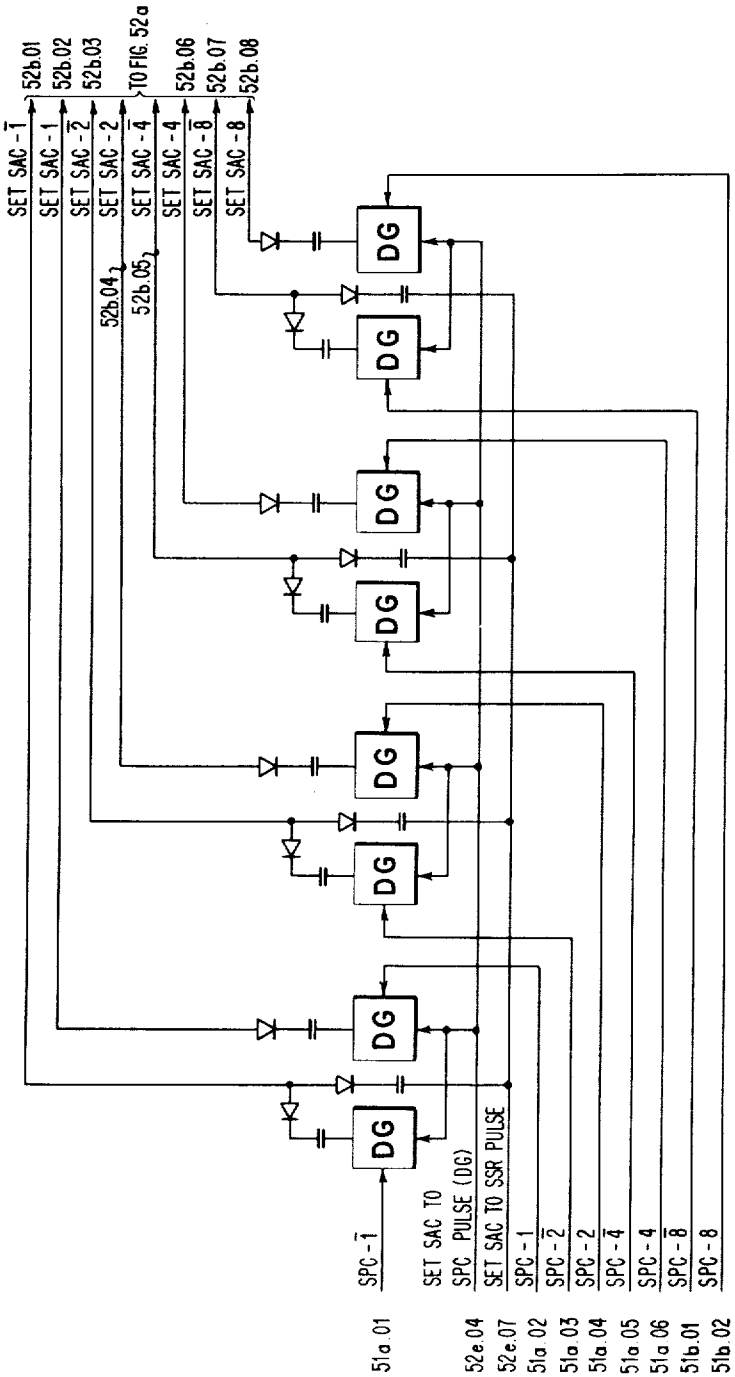


STAGES 1-4 OF SAC

FIG. 52a

FIG. 52b

STAGES 1-4 OF SAC



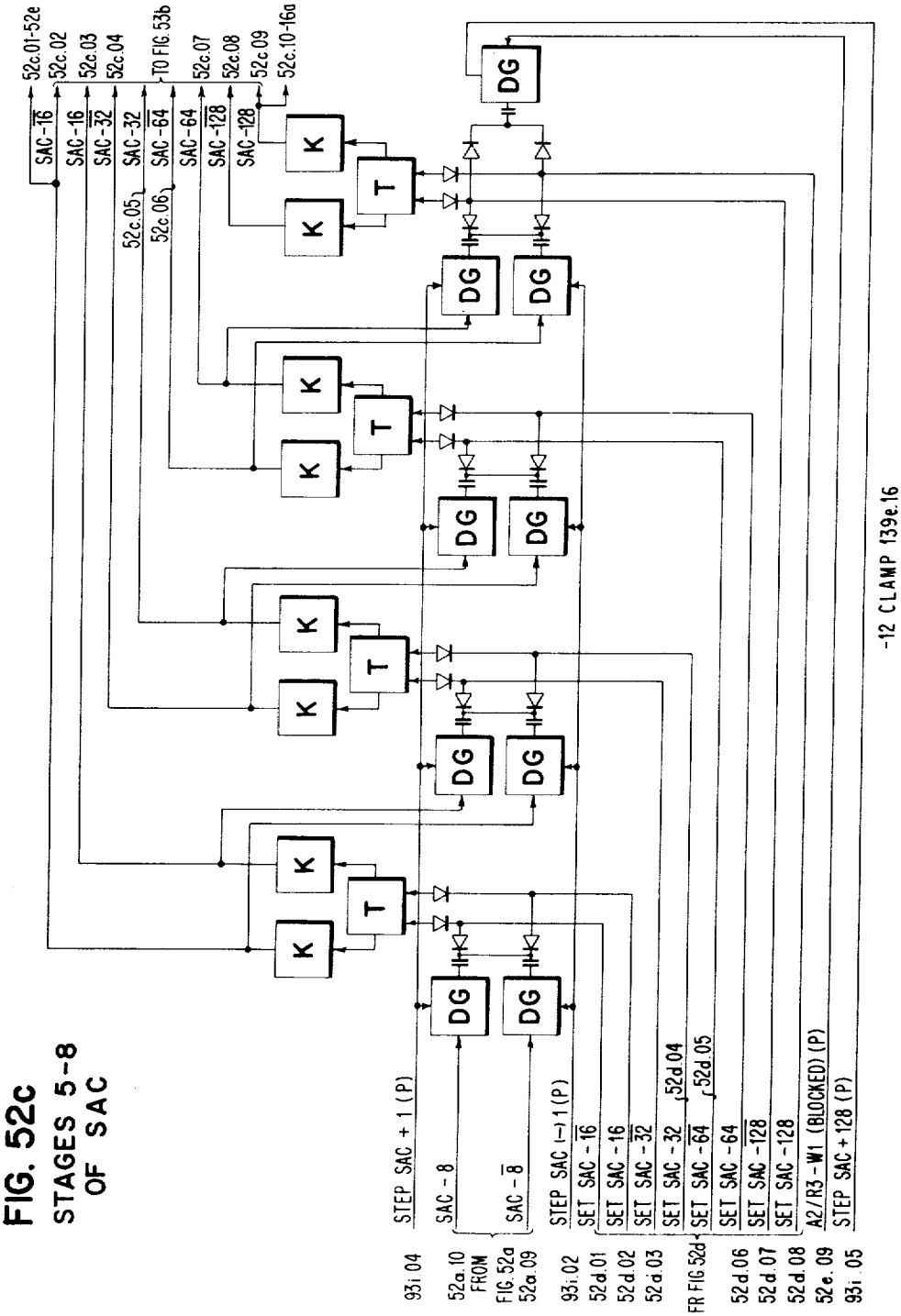
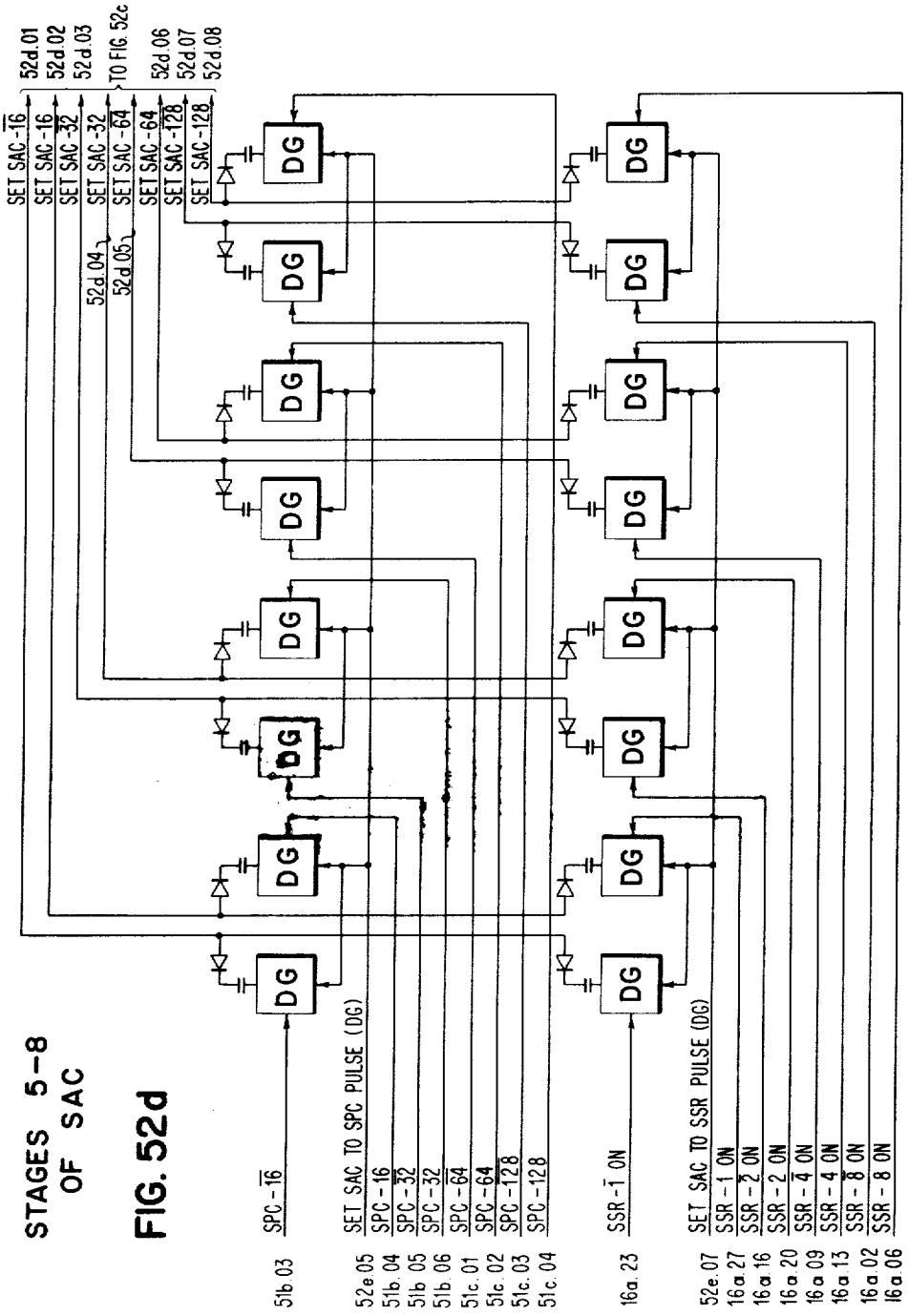


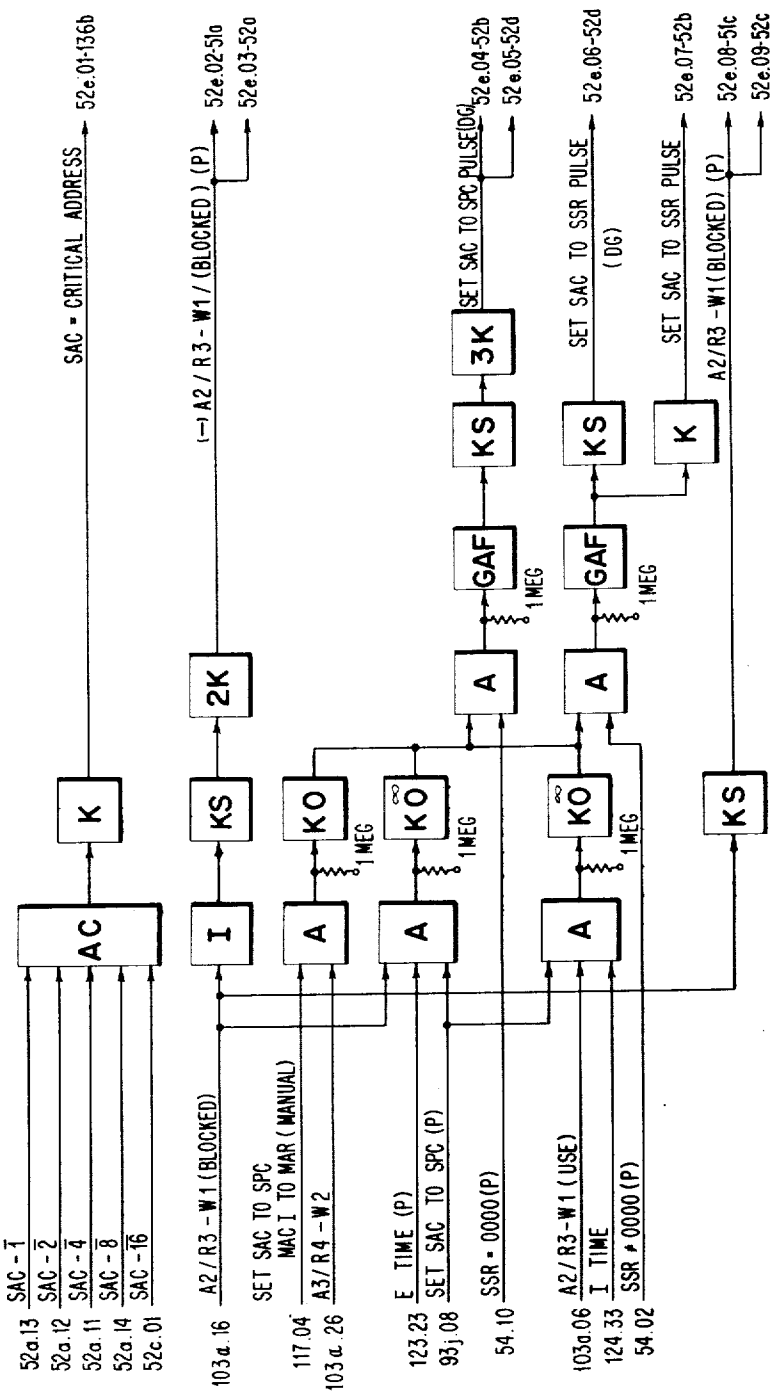
FIG. 52c
STAGES 5-8 OF SAC



STAGES 5-8 OF SAC

FIG. 52d

FIG. 52e


SAC CONTROLS
SAC - CRITICAL ADDRESS
52e.01-136b
(→) A2/R3-W1/(BLOCKED) (P)
52e.02-51a
52e.03-52a
SET SAC TO SPC PULSE(DG)
52e.04-52b
52e.05-52d
SET SAC TO SSR PULSE (DG)
52e.06-52d
SET SAC TO SSR PULSE
52e.07-52b
A2/R3-W1(BLOCKED) (P)
52e.08-51c
52e.09-52c
SAC-1
SAC-2
SAC-4
SAC-8
SAC-16
52a.13
52a.12
52a.11
52a.14
52c.01
AC
K
103a.16
A2/R3-W1(BLOCKED)
I
KS
2K
SET SAC TO SPC
MAC I TO MAR (MANUAL)
117.04
A3/R4-W2
103a.26
A
KO
1MEG
E TIME (P)
123.23
SET SAC TO SPC (P)
93j.08
SSR=0000(P)
54.10
GAF
3K
KS
A2/R3-W1(USE)
103a.06
I TIME
124.33
SSR≠0000(P)
54.02
K

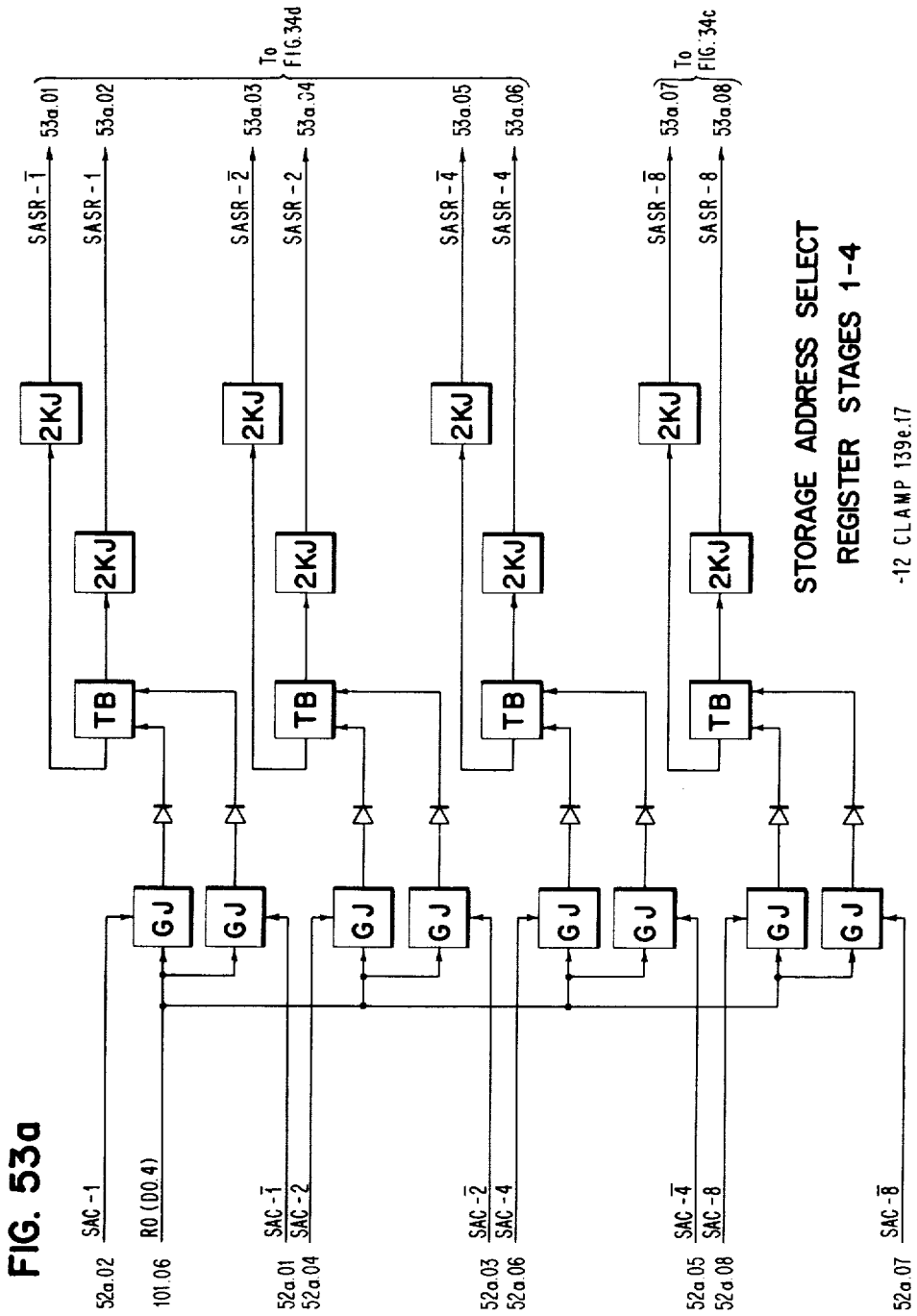

To FIG. 34d
To FIG. 34c
53a.01
53a.02
53a.03
53a.04
53a.05
53a.06
53a.07
53a.08
SASR - $\overline{1}$
SASR - 1
SASR - $\overline{2}$
SASR - 2
SASR - $\overline{4}$
SASR - 4
SASR - $\overline{8}$
SASR - 8
2KJ
TB
GJ
STORAGE ADDRESS SELECT
REGISTER STAGES 1-4
-12 CLAMP 139e.17
SAC - 1
RO (00.4)
SAC - $\overline{1}$
SAC - 2
SAC - $\overline{2}$
SAC - 4
SAC - $\overline{4}$
SAC - 8
SAC - $\overline{8}$
52a.02
101.06
52a.01
52a.04
52a.03
52a.06
52a.05
52a.08
52a.07

FIG. 53a

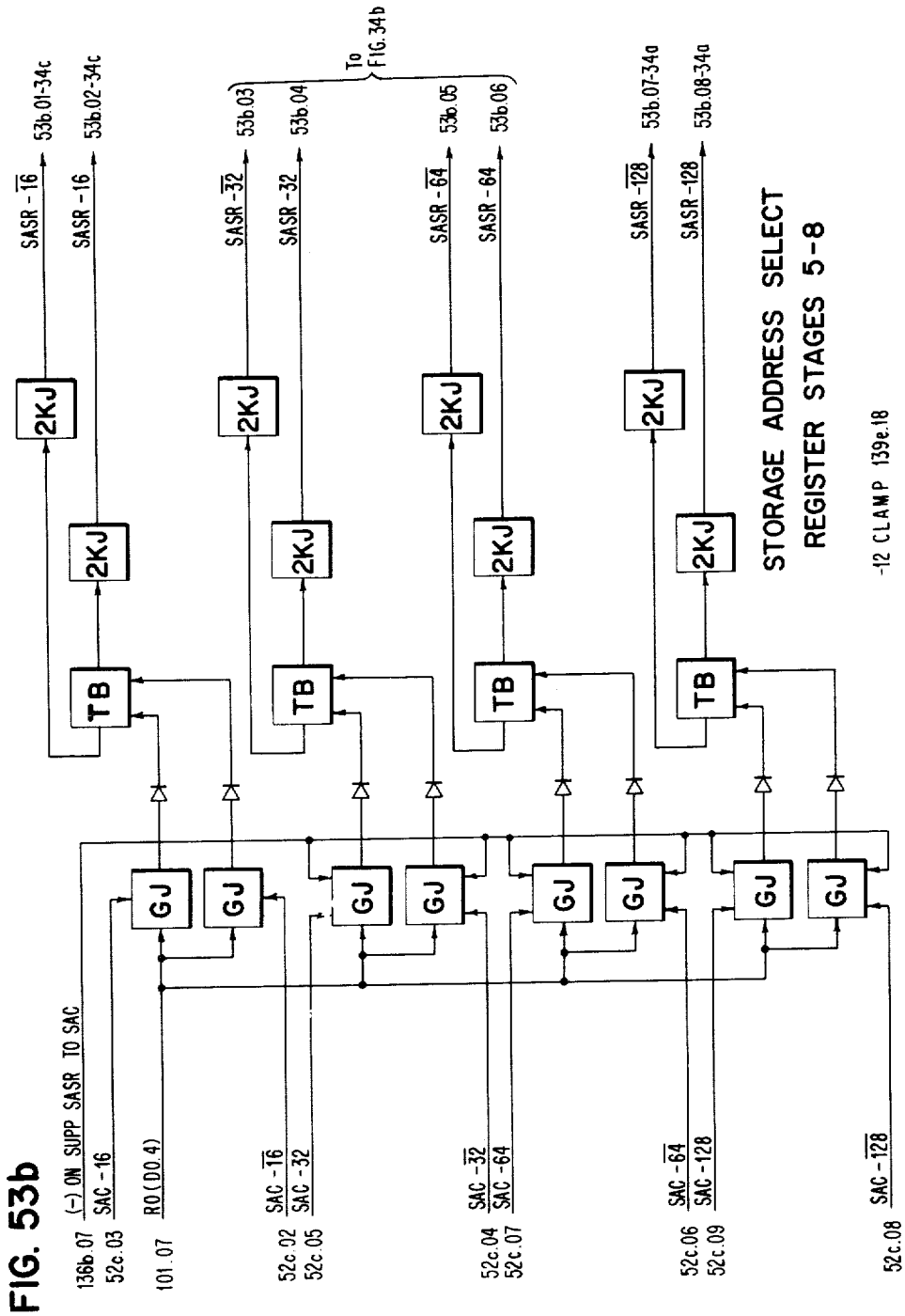
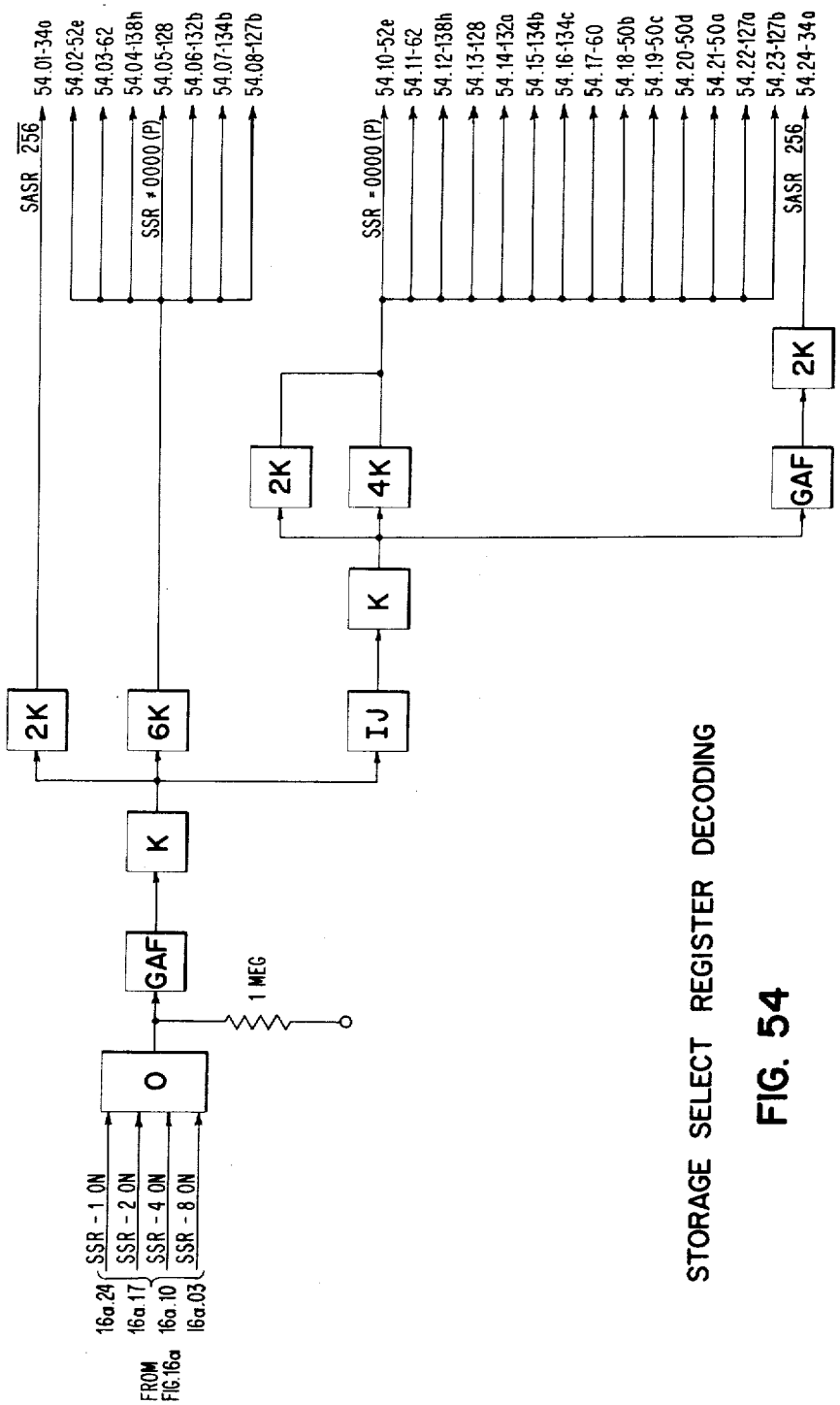

To FIG. 34b
53b.01-34c
53b.02-34c
53b.03
53b.04
53b.05
53b.06
53b.07-34a
53b.08-34a
SASR -16
SASR -16
SASR -32
SASR -32
SASR -64
SASR -64
SASR -128
SASR -128
2KJ
TB
GJ
STORAGE ADDRESS SELECT
REGISTER STAGES 5-8
-12 CLAMP 139e.18
(-) ON SUPP SASR TO SAC
136b.07
52c.03
SAC -16
SAC -16
SAC -32
SAC -32
SAC -64
SAC -64
SAC -128
SAC -128
101.07
RO(00.4)
52c.02
52c.05
52c.04
52c.07
52c.06
52c.09
52c.08

FIG. 53b



STORAGE SELECT REGISTER DECODING

FIG. 54

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FIG. 55a SSR DECODER 1-8

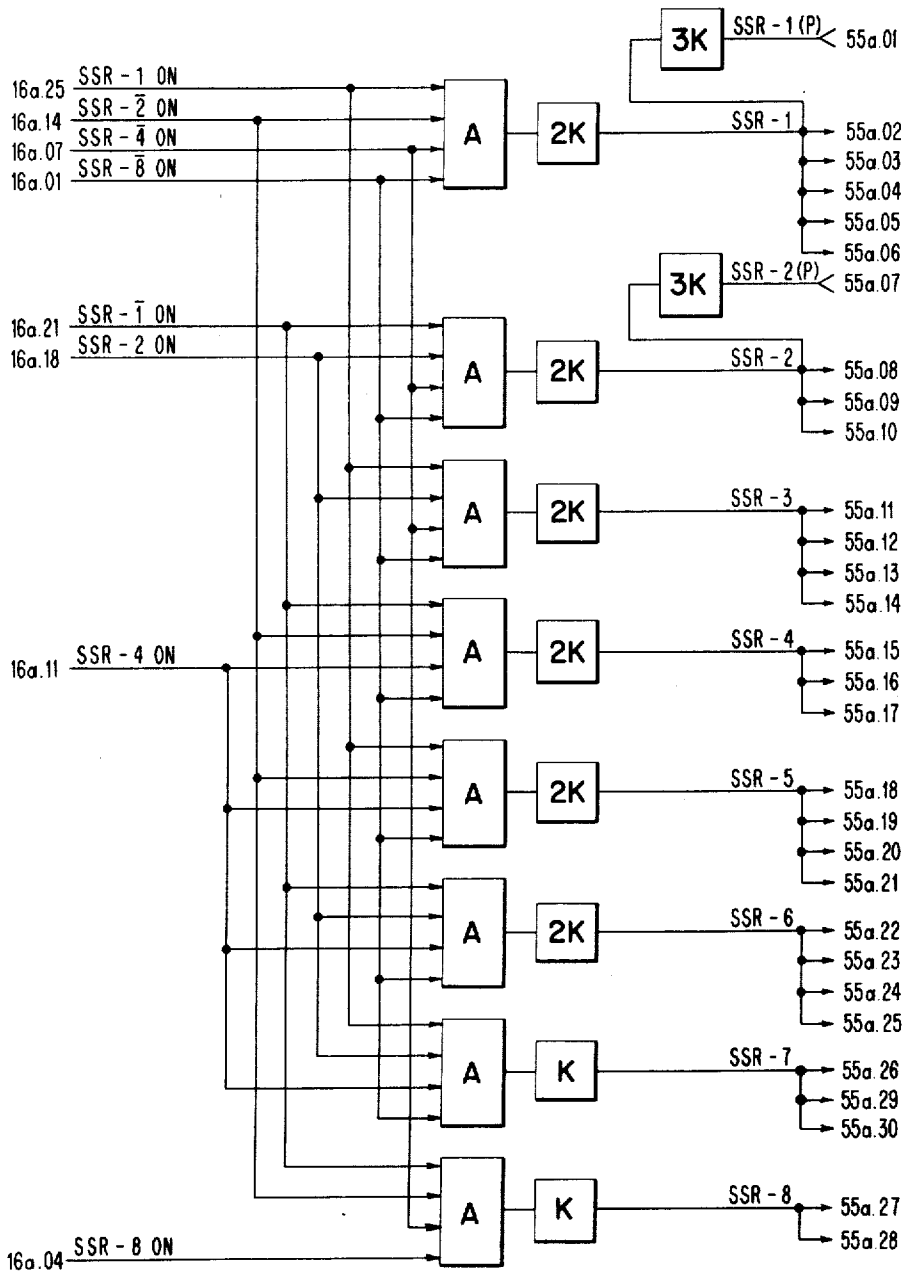


FIG. 55b

SSR DECODER 9-15

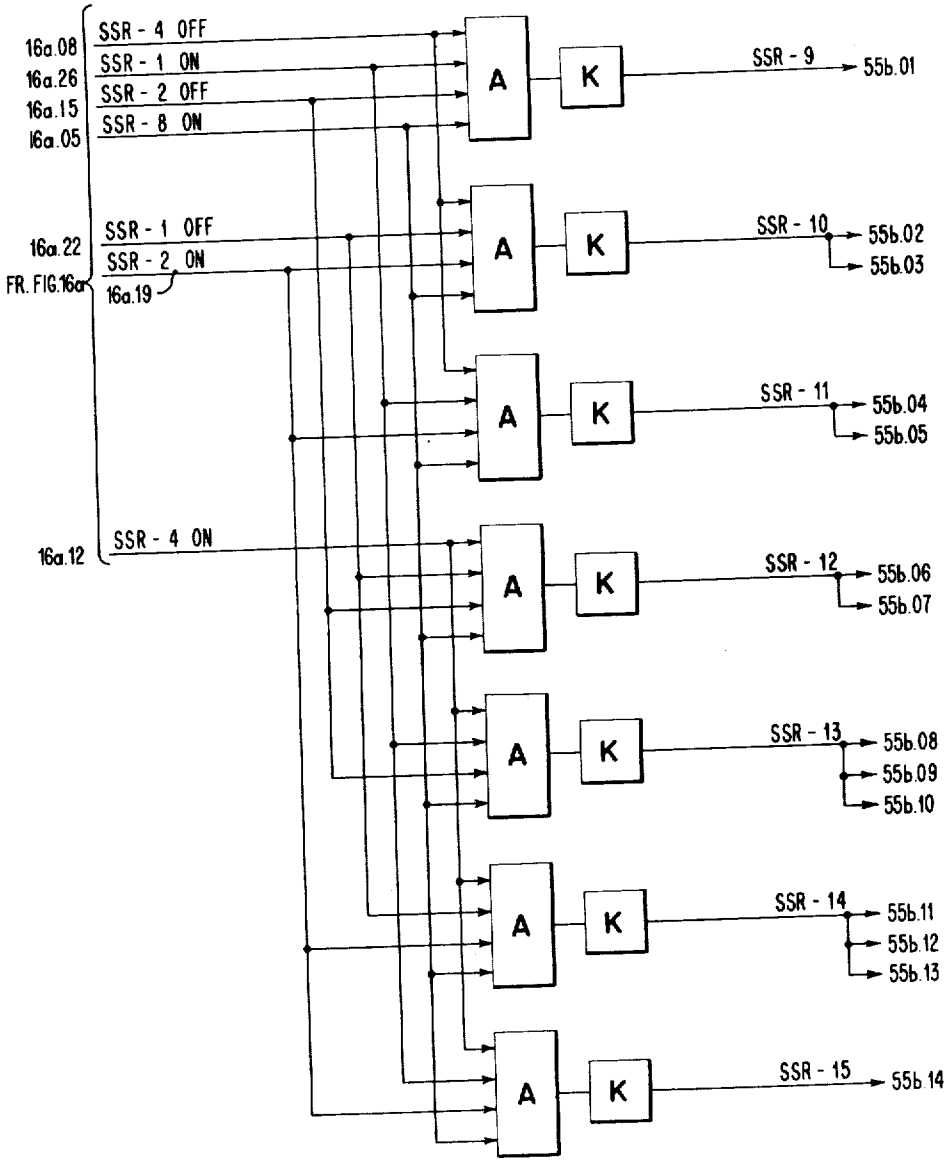


FIG.56a

SET BIT ROUTING CONTROLS

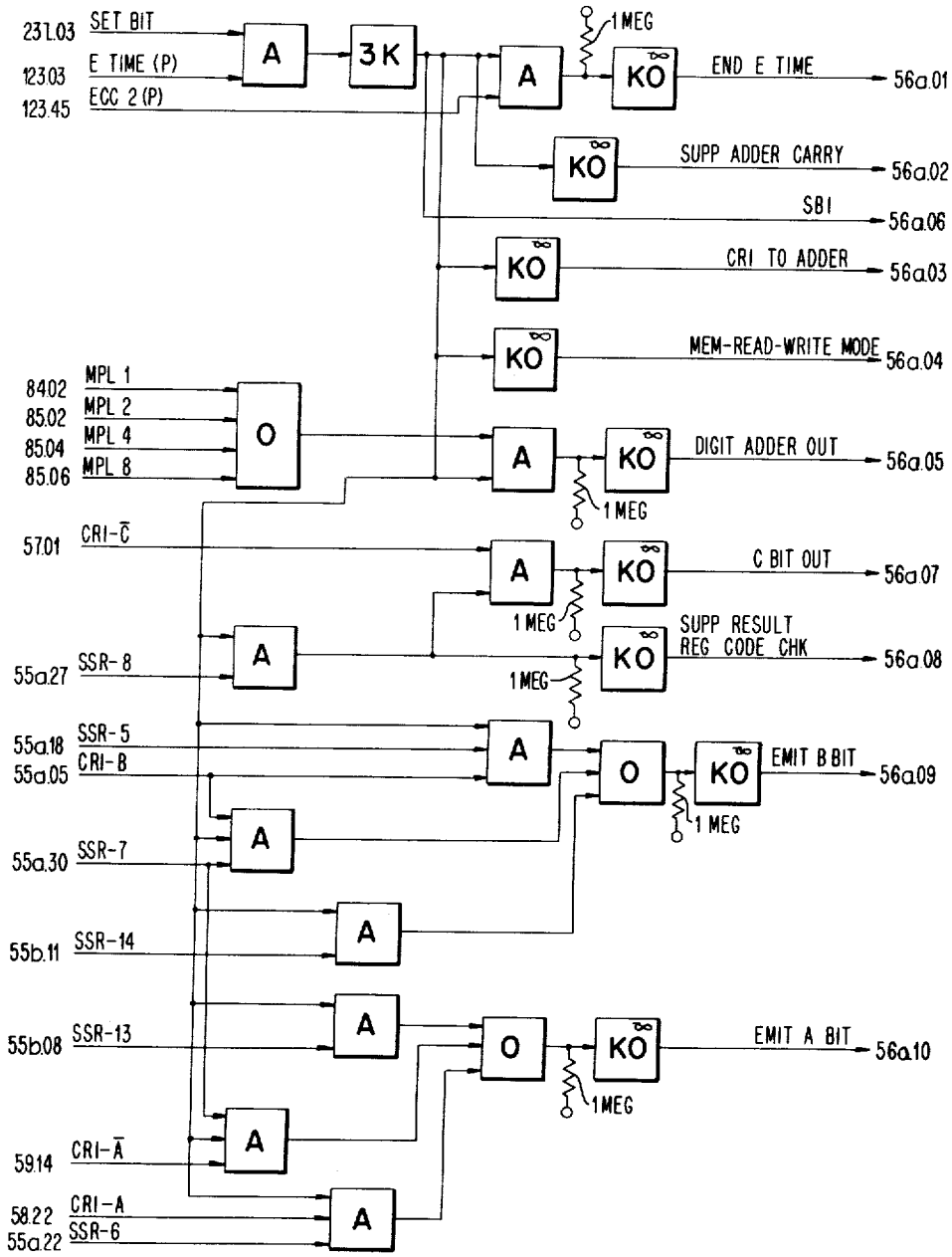


FIG. 56b

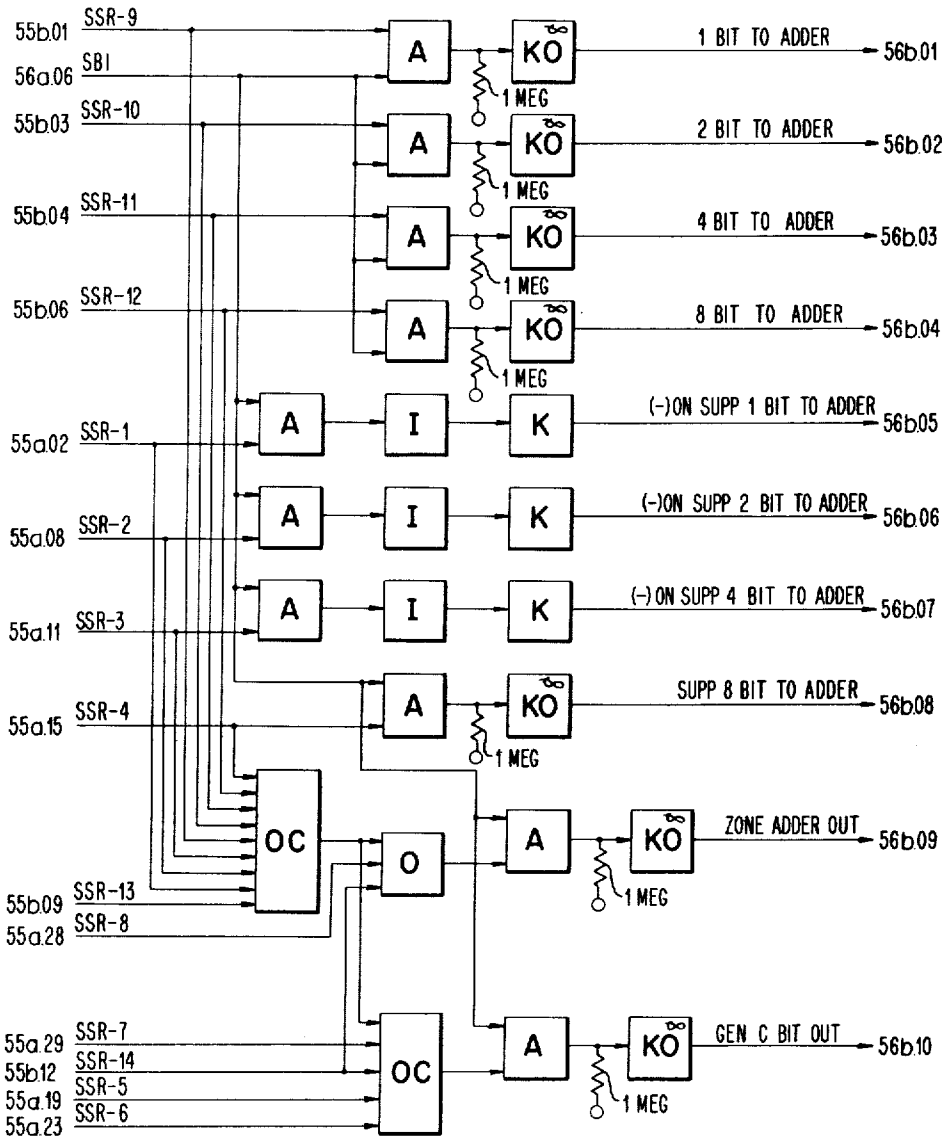

SET BIT ROUTING CONTROLS
55b.01 SSR-9
56a.06 SBI
55b.03 SSR-10
55b.04 SSR-11
55b.06 SSR-12
55a.02 SSR-1
55a.08 SSR-2
55a.11 SSR-3
55a.15 SSR-4
55b.09 SSR-13
55a.28 SSR-8
55a.29 SSR-7
55b.12 SSR-14
55a.19 SSR-5
55a.23 SSR-6
A
I
K
KO
OC
O
1 MEG
1 BIT TO ADDER
56b.01
2 BIT TO ADDER
56b.02
4 BIT TO ADDER
56b.03
8 BIT TO ADDER
56b.04
(-)ON SUPP 1 BIT TO ADDER
56b.05
(-)ON SUPP 2 BIT TO ADDER
56b.06
(-)ON SUPP 4 BIT TO ADDER
56b.07
SUPP 8 BIT TO ADDER
56b.08
ZONE ADDER OUT
56b.09
GEN C BIT OUT
56b.10

FIG.57

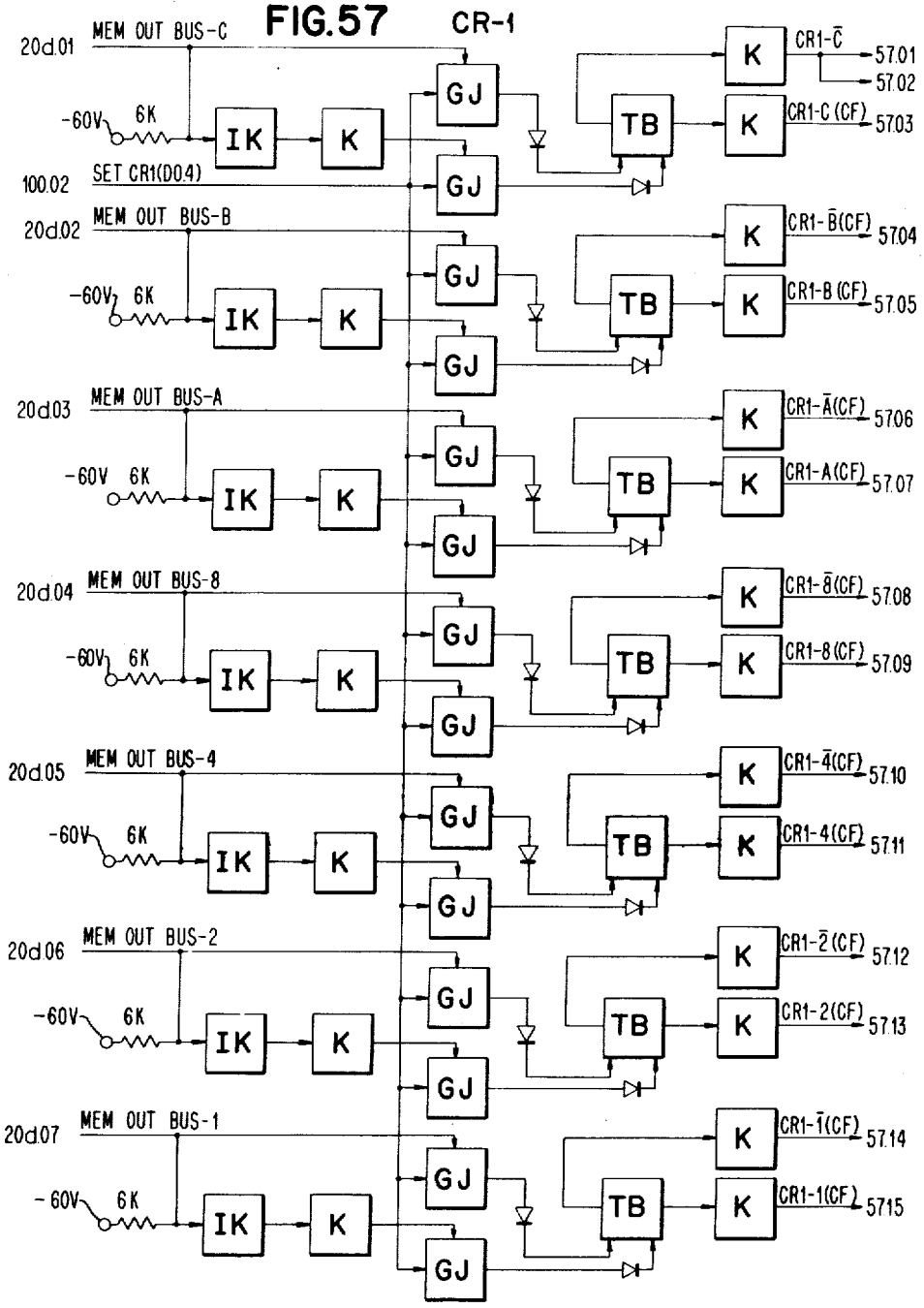

CR-1
20d.01
MEM OUT BUS-C
-60V
6K
IK
K
GJ
100.02
SET CR1(D0.4)
TB
CR1-C̄
57.01
57.02
CR1-C (CF)
57.03
20d.02
MEM OUT BUS-B
CR1-B̄(CF)
57.04
CR1-B (CF)
57.05
20d.03
MEM OUT BUS-A
CR1-Ā(CF)
57.06
CR1-A(CF)
57.07
20d.04
MEM OUT BUS-8
CR1-8̄(CF)
57.08
CR1-8(CF)
57.09
20d.05
MEM OUT BUS-4
CR1-4̄(CF)
57.10
CR1-4(CF)
57.11
20d.06
MEM OUT BUS-2
CR1-2̄(CF)
57.12
CR1-2(CF)
57.13
20d.07
MEM OUT BUS-1
CR1-1̄(CF)
57.14
CR1-1(CF)
57.15

FIG.58
SHEET 1 of 2

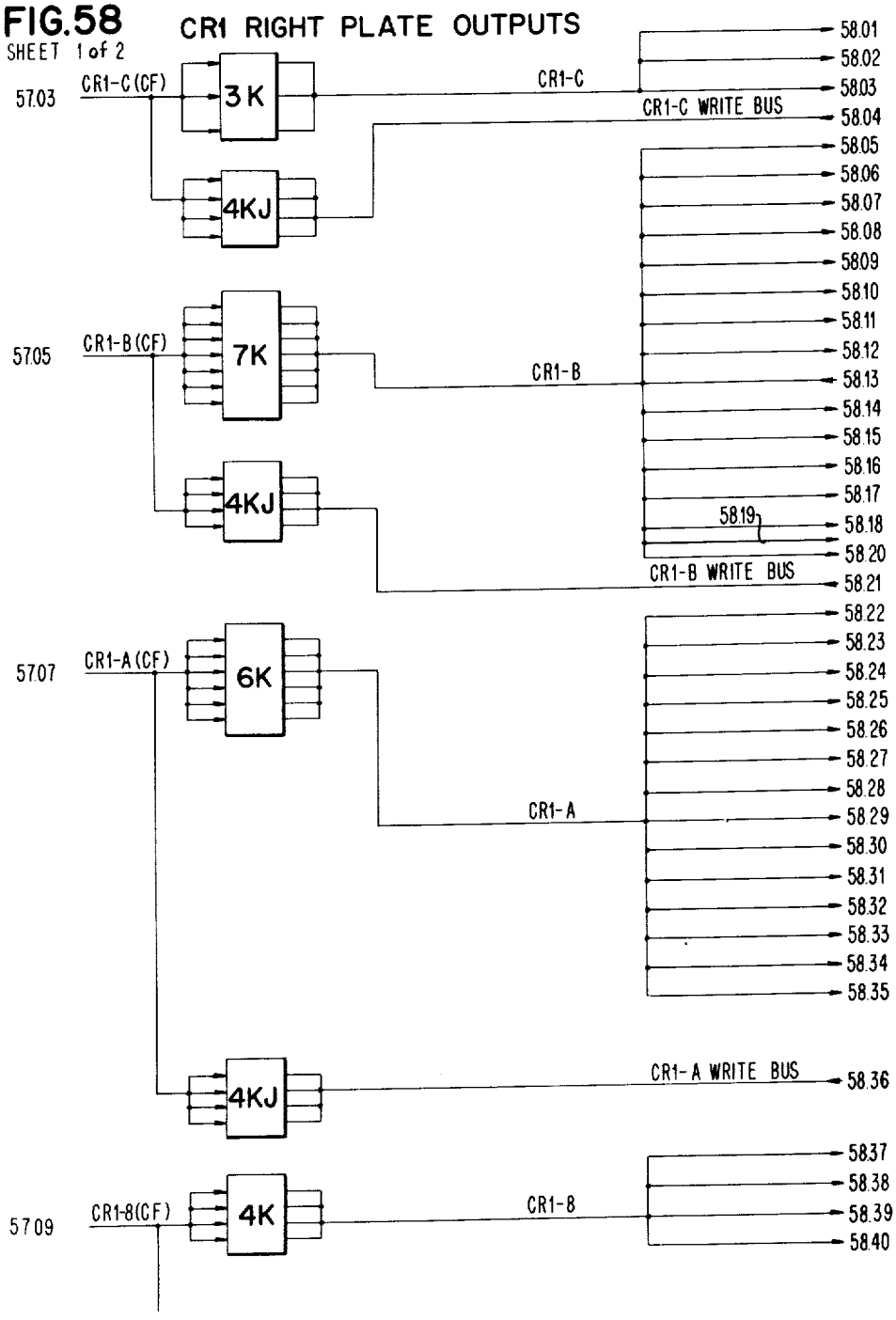


FIG.58
SHEET 2 of 2

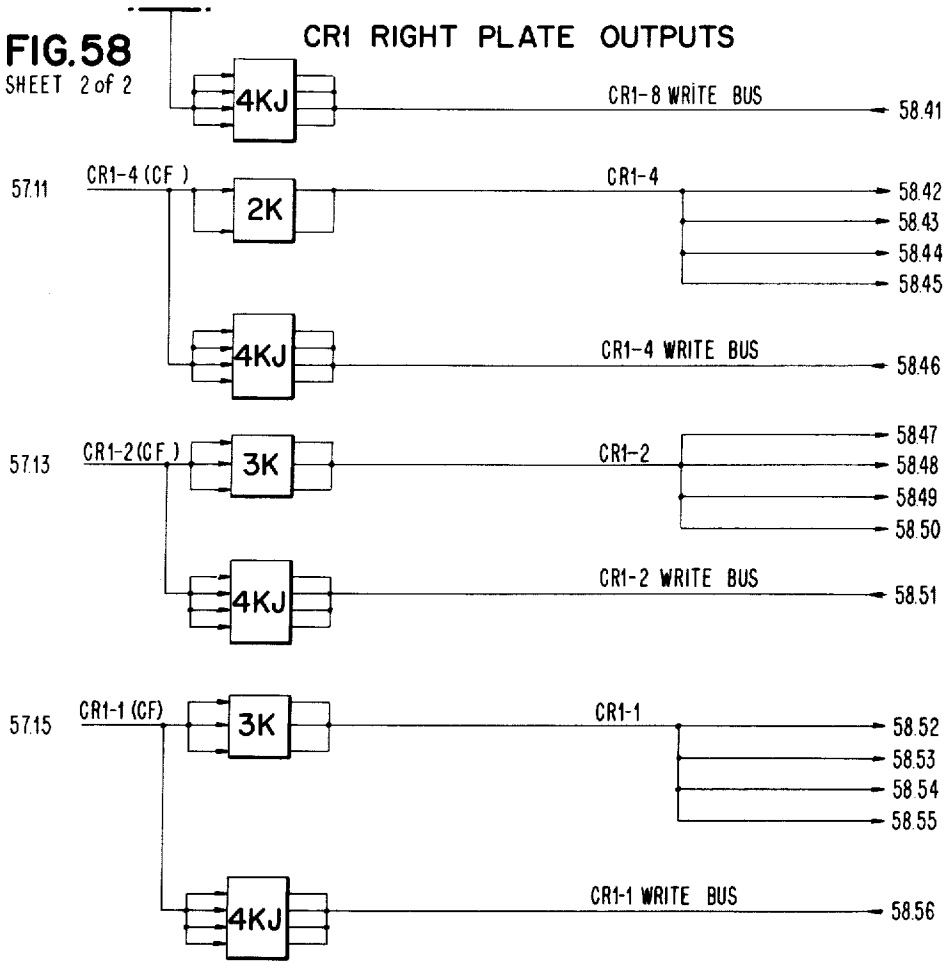


FIG. 59 CR1 LEFT PLATE OUTPUTS

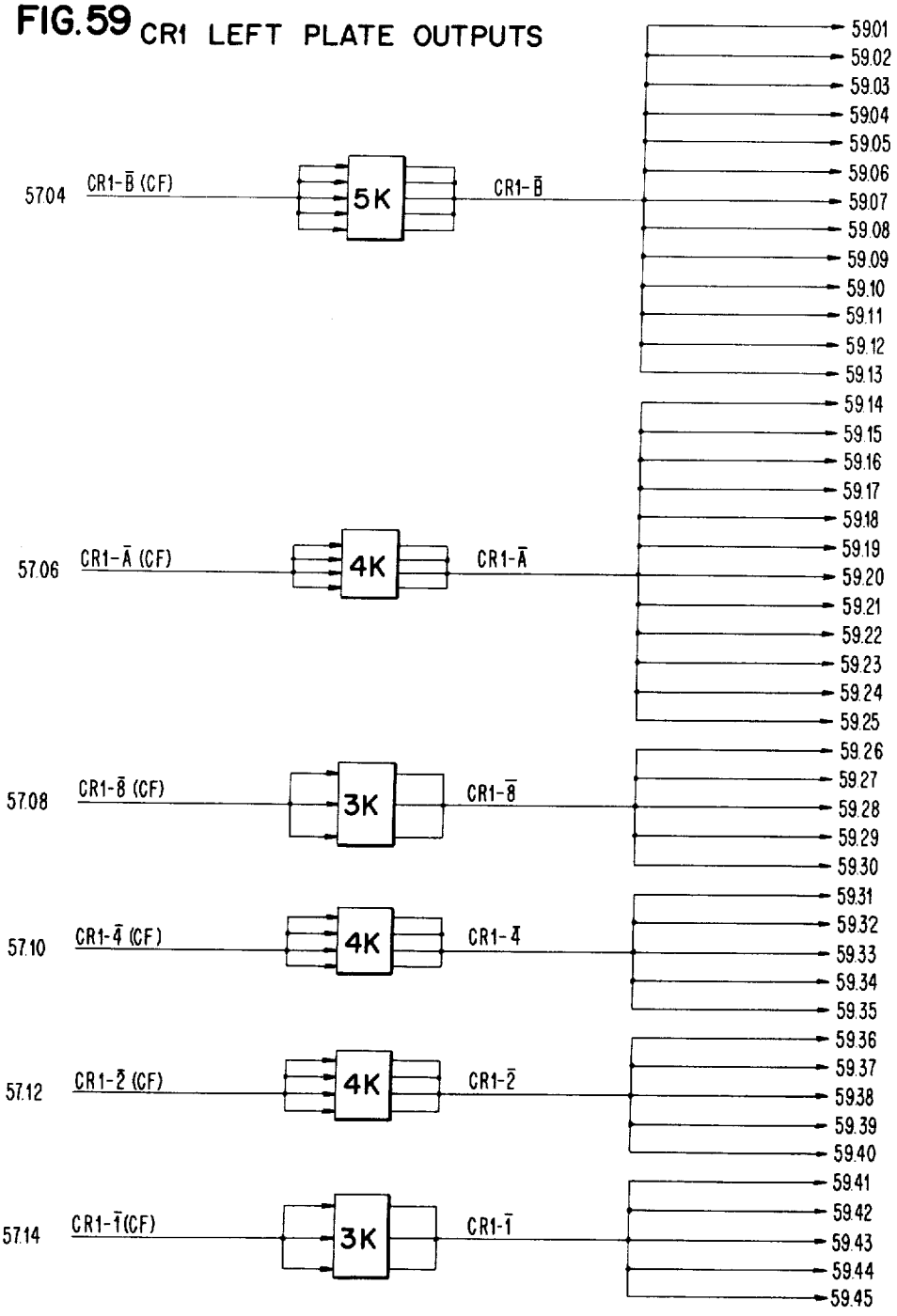
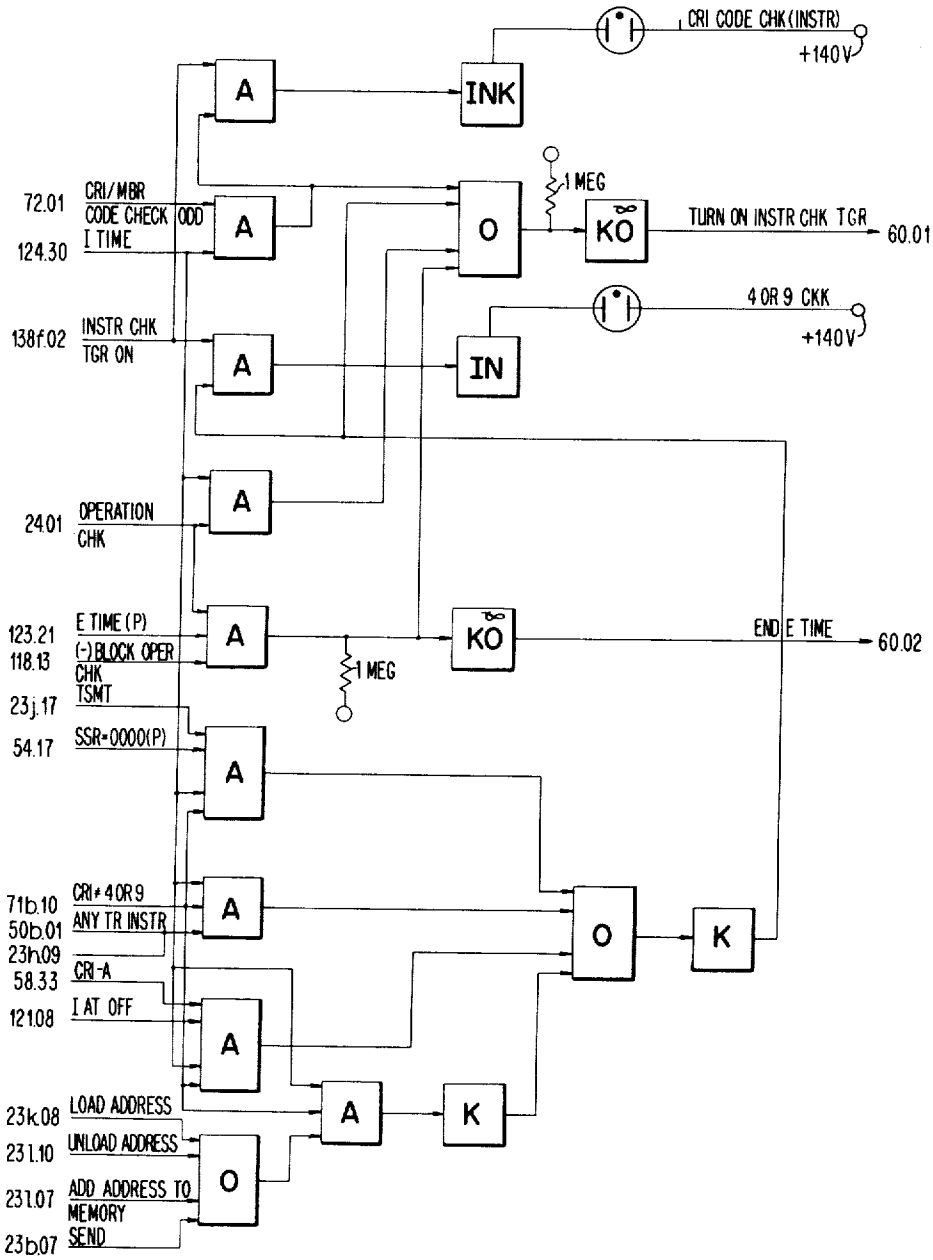


FIG. 60 INSTRUCTION CHECK CIRCUITS



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FIG. 61

I TIME ROUTING CONTROLS

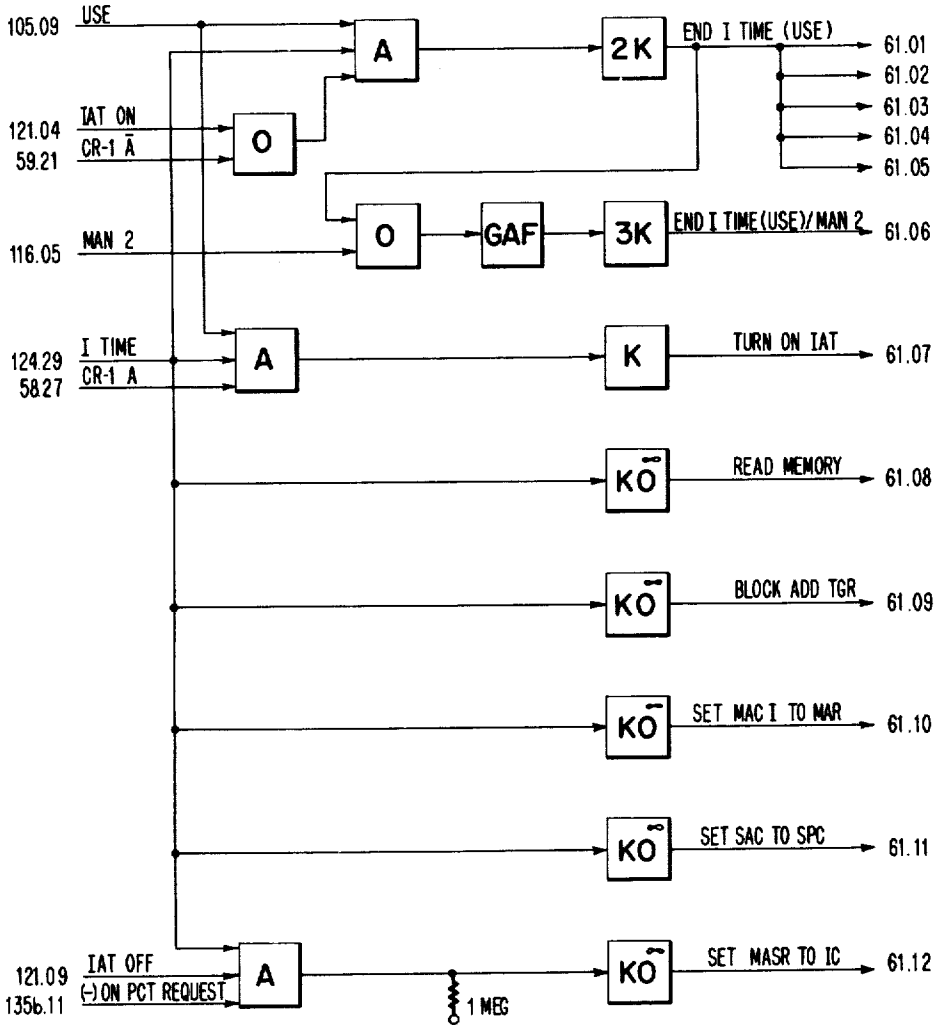


FIG. 62 STORAGE SIGN TGRS. & CONTROLS

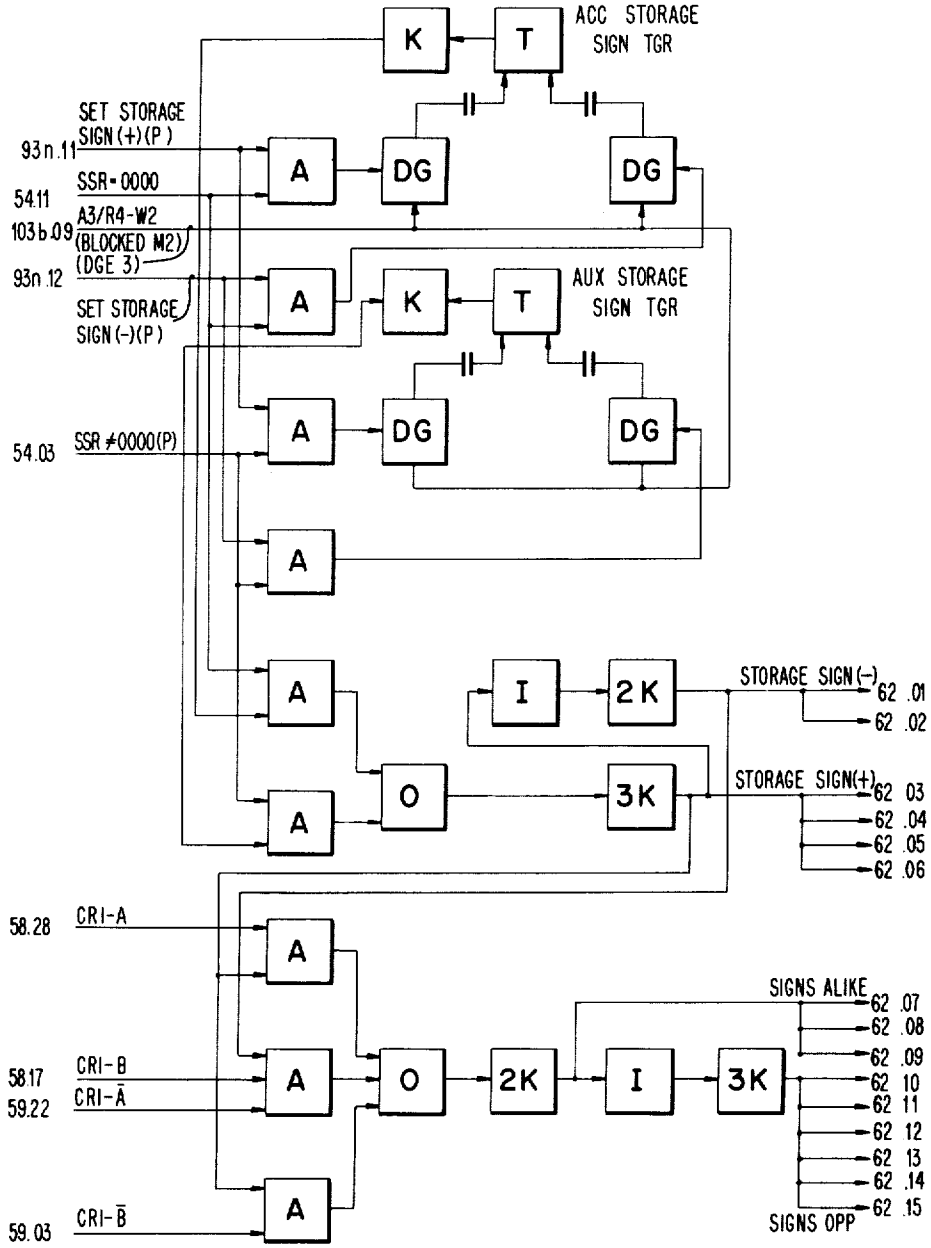


FIG. 63a

INTER REG CHECK ROUTING 1

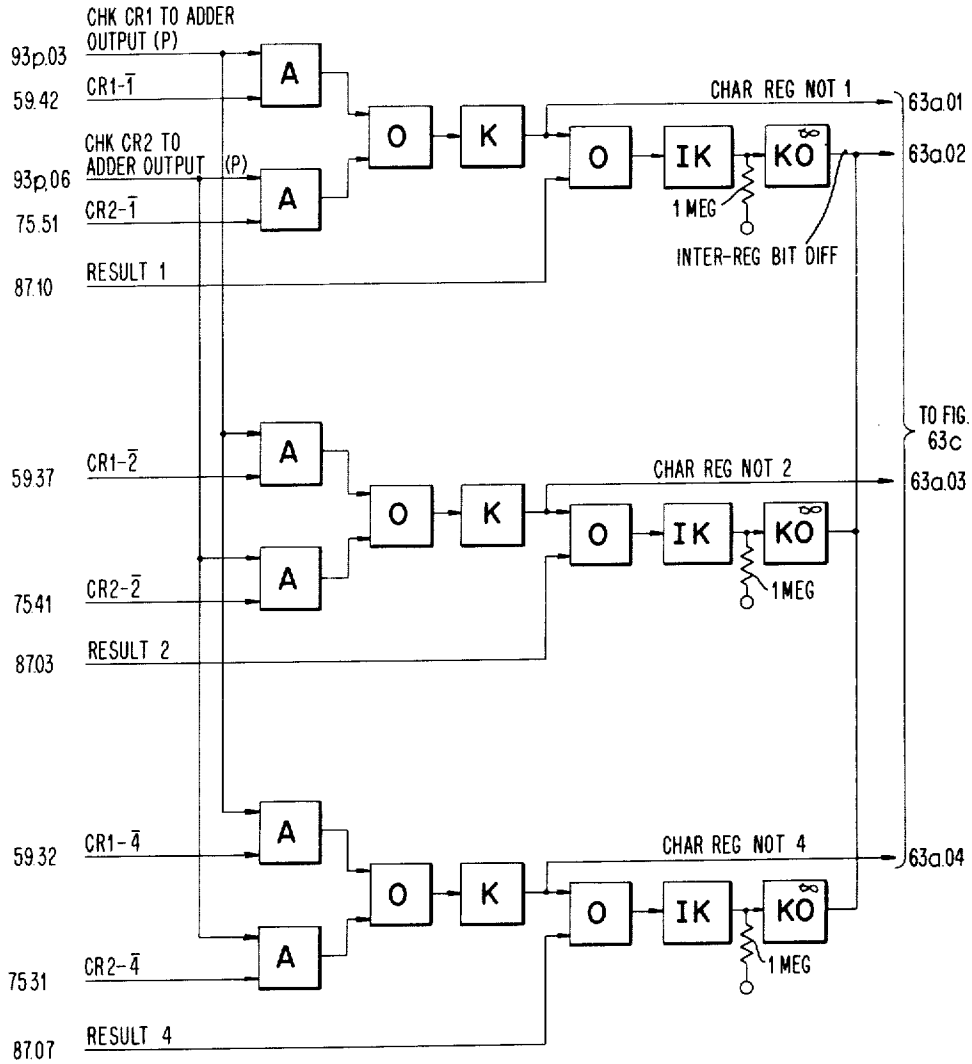


FIG. 63b

INTER-REG CHECK ROUTING 2

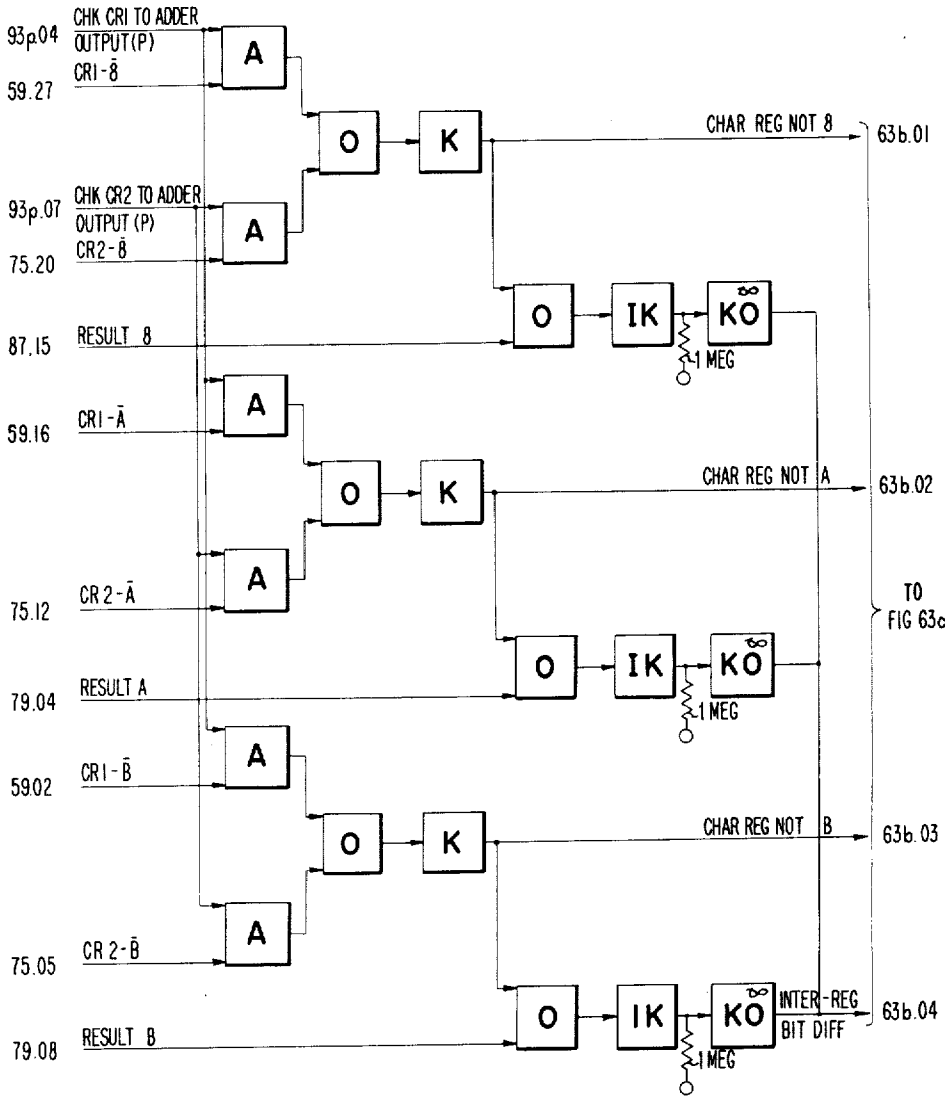


FIG. 63c INTER-REG CHECK TGR

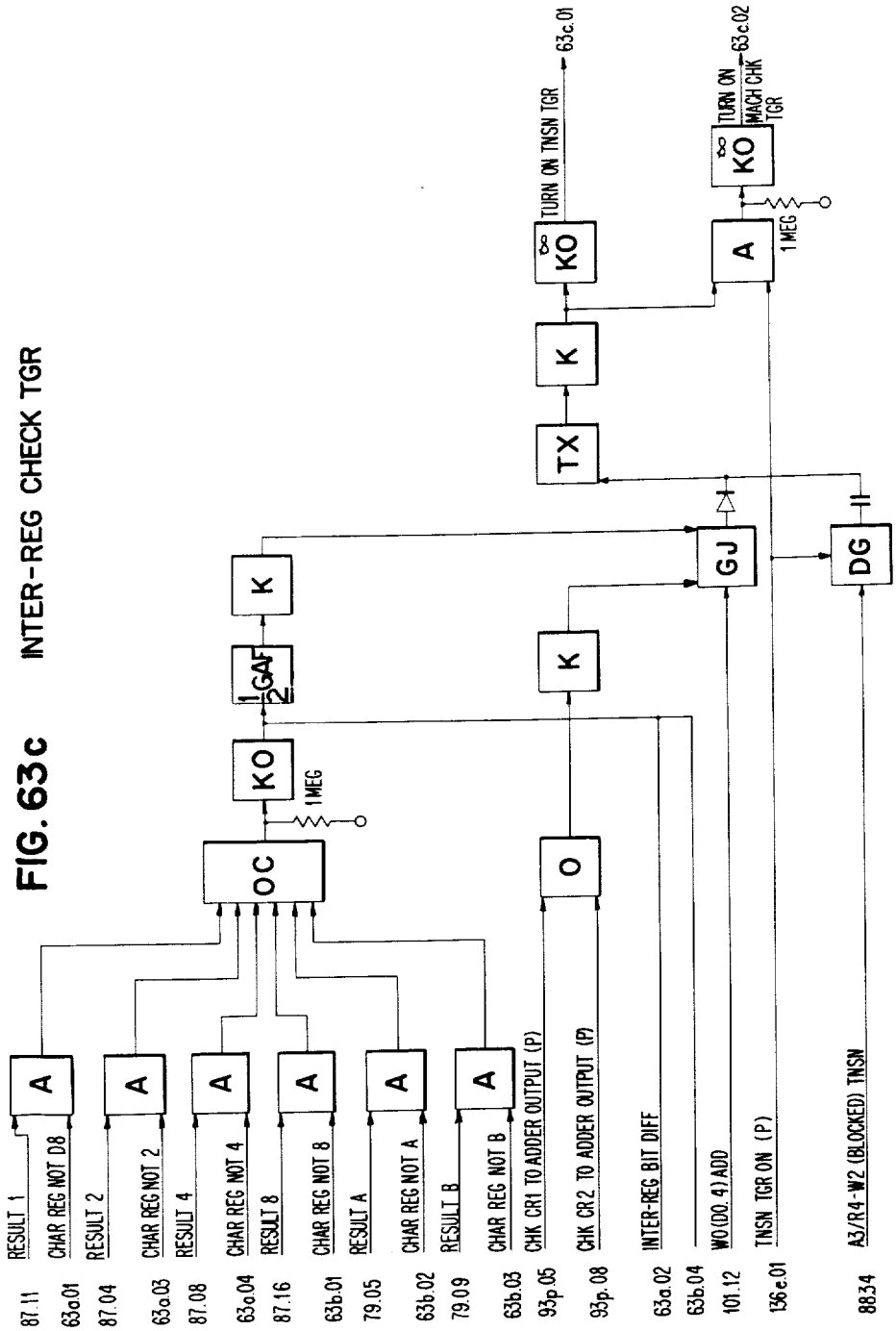


FIG.64a

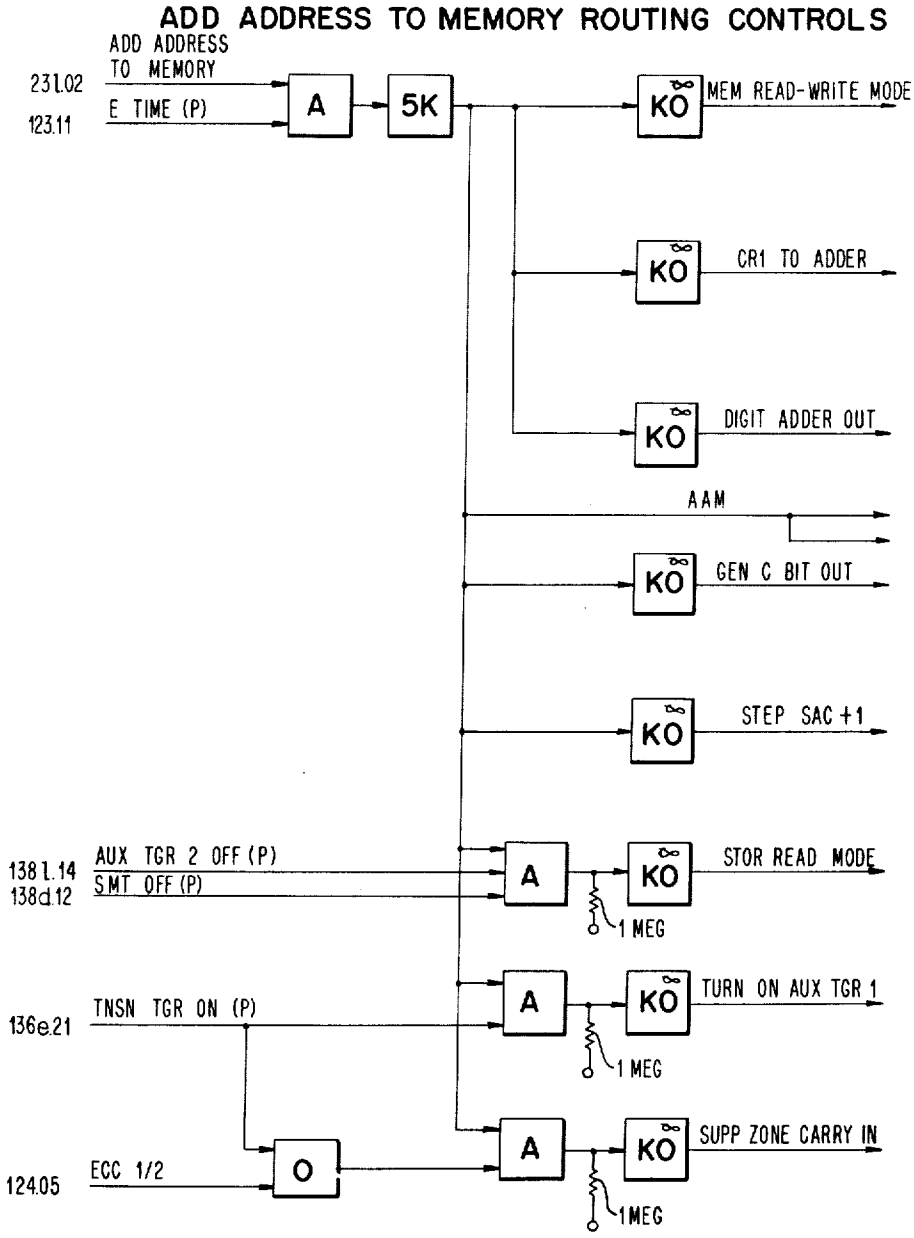
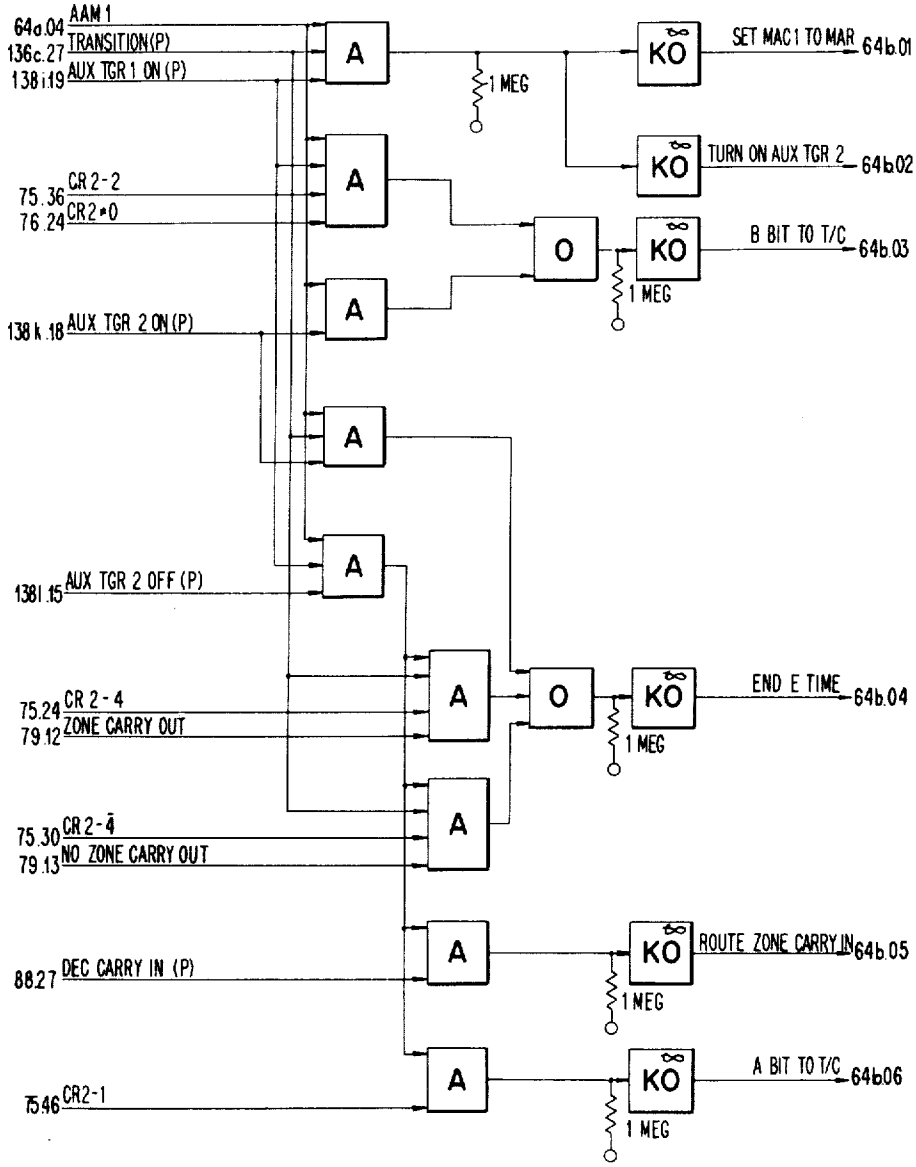

ADD ADDRESS TO MEMORY ROUTING CONTROLS
ADD ADDRESS TO MEMORY
231.02
E TIME (P)
123.11
A
5K
KO
MEM READ-WRITE MODE
CR1 TO ADDER
DIGIT ADDER OUT
AAM
GEN C BIT OUT
STEP SAC +1
138 l.14
AUX TGR 2 OFF (P)
138 d.12
SMT OFF (P)
STOR READ MODE
1 MEG
136e.21
TNSN TGR ON (P)
TURN ON AUX TGR 1
124.05
ECC 1/2
O
SUPP ZONE CARRY IN

FIG.64b

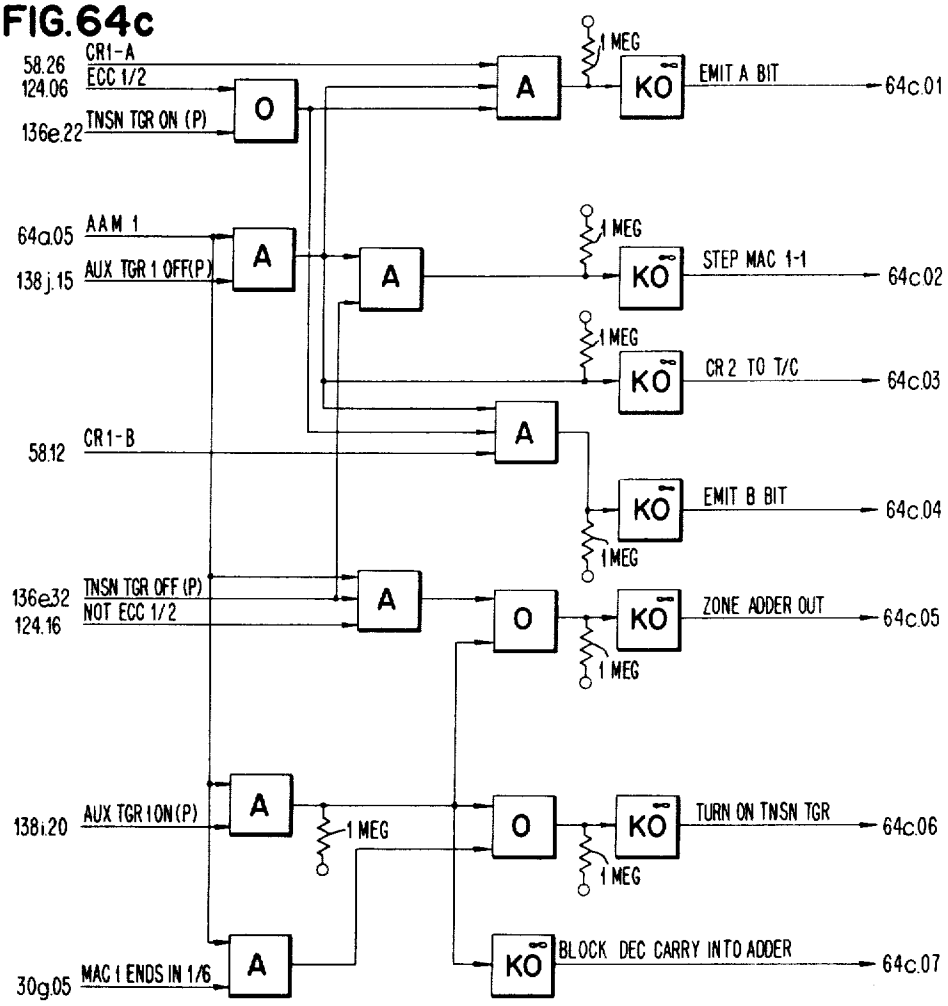
ADD ADDRESS TO MEMORY ROUTING CONTROLS



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ADD ADDRESS TO MEMORY ROUTING CONTROLS

FIG.64c



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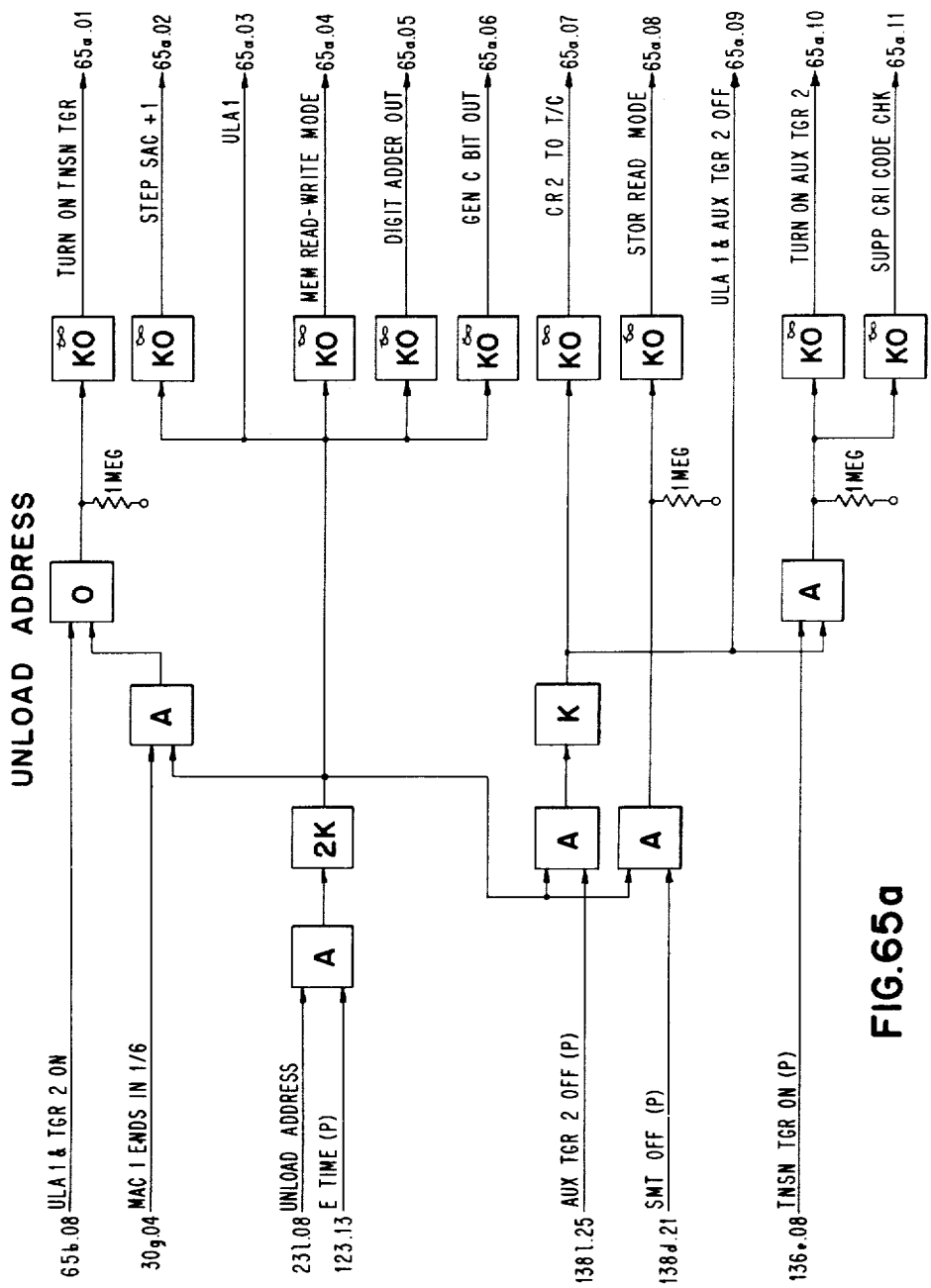
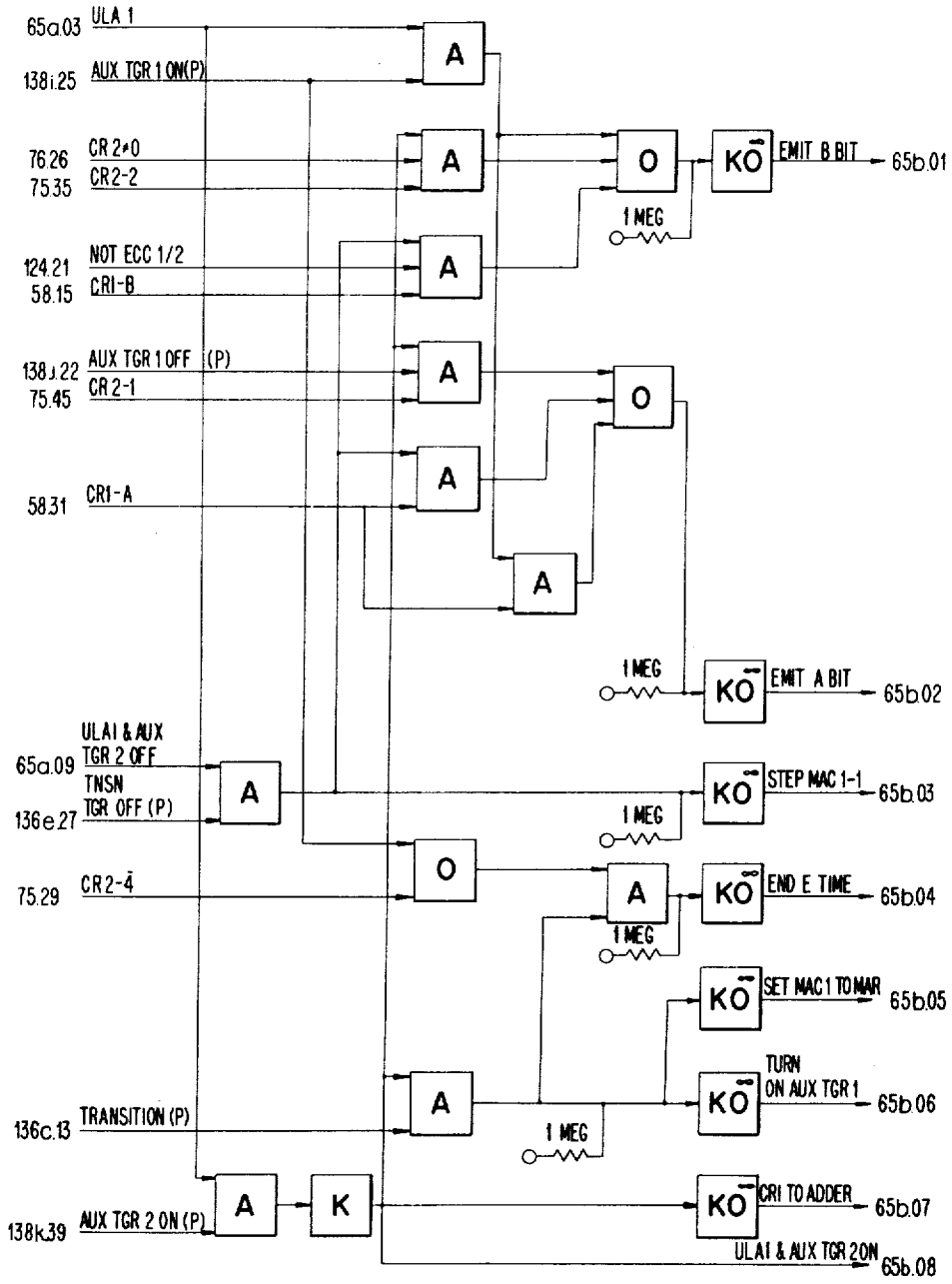


FIG.65a

FIG.65b


UNLOAD ADDRESS
65a.03 ULA 1
138i.25 AUX TGR 1 ON(P)
76.26 CR 2≠0
75.35 CR2-2
124.21 NOT ECC 1/2
58.15 CR1-B
138j.22 AUX TGR 1 OFF (P)
75.45 CR 2-1
58.31 CR1-A
65a.09 ULA1 & AUX TGR 2 OFF TNSN TGR OFF (P)
136e.27
75.29 CR2-4
136c.13 TRANSITION (P)
138k.39 AUX TGR 2 ON (P)
A
O
K
KO
1 MEG
EMIT B BIT 65b.01
EMIT A BIT 65b.02
STEP MAC 1-1 65b.03
END E TIME 65b.04
SET MAC1 TO MAR 65b.05
TURN ON AUX TGR 1 65b.06
CR1 TO ADDER 65b.07
ULA1 & AUX TGR 2 ON 65b.08

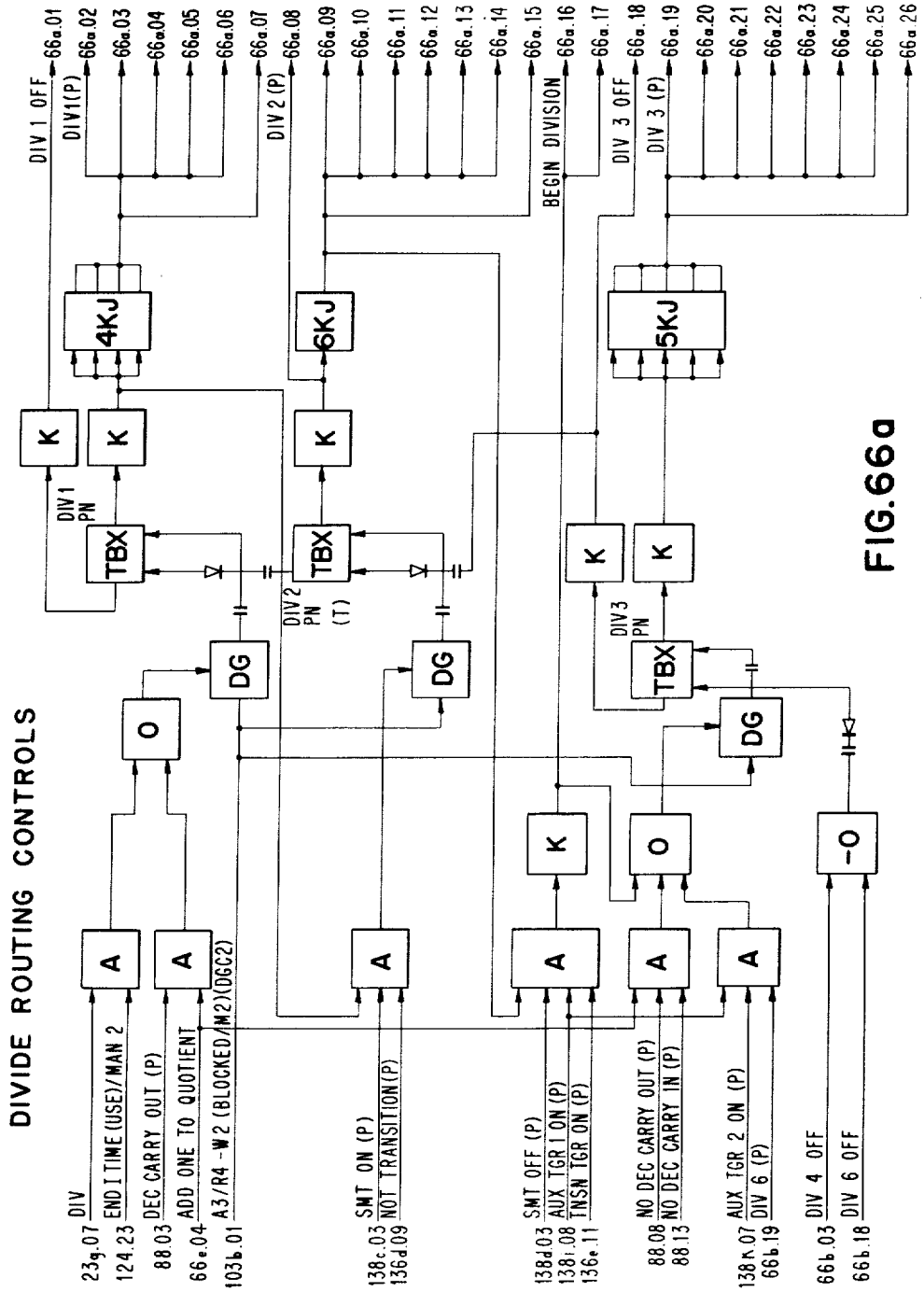

DIVIDE ROUTING CONTROLS
DIV 1 OFF 66a.01
DIV1(P) 66a.02
66a.03
66a.04
66a.05
66a.06
66a.07
DIV 2 (P) 66a.08
66a.09
66a.10
66a.11
66a.12
66a.13
66a.14
66a.15
BEGIN DIVISION 66a.16
66a.17
DIV 3 OFF 66a.18
DIV 3 (P) 66a.19
66a.20
66a.21
66a.22
66a.23
66a.24
66a.25
66a.26
4KJ
6KJ
5KJ
K
TBX
DIV1 PN
DIV2 PN (T)
DIV3 PN
DG
O
A
-O
DIV 23g.07
END ITIME (USE)/MAN 2 124.23
DEC CARRY OUT (P) 88.03
ADD ONE TO QUOTIENT 66e.04
A3/R4 - W2 (BLOCKED/M2)(DGC2) 103b.01
SMT ON (P) 138c.03
NOT TRANSITION(P) 136d.09
SMT OFF (P) 138d.03
AUX TGR 1 ON (P) 138i.08
TNSN TGR ON (P) 136e.11
NO DEC CARRY OUT (P) 88.08
NO DEC CARRY IN (P) 88.13
AUX TGR 2 ON (P) 138n.07
DIV 6 (P) 66b.19
DIV 4 OFF 66b.03
DIV 6 OFF 66b.18

FIG.66a

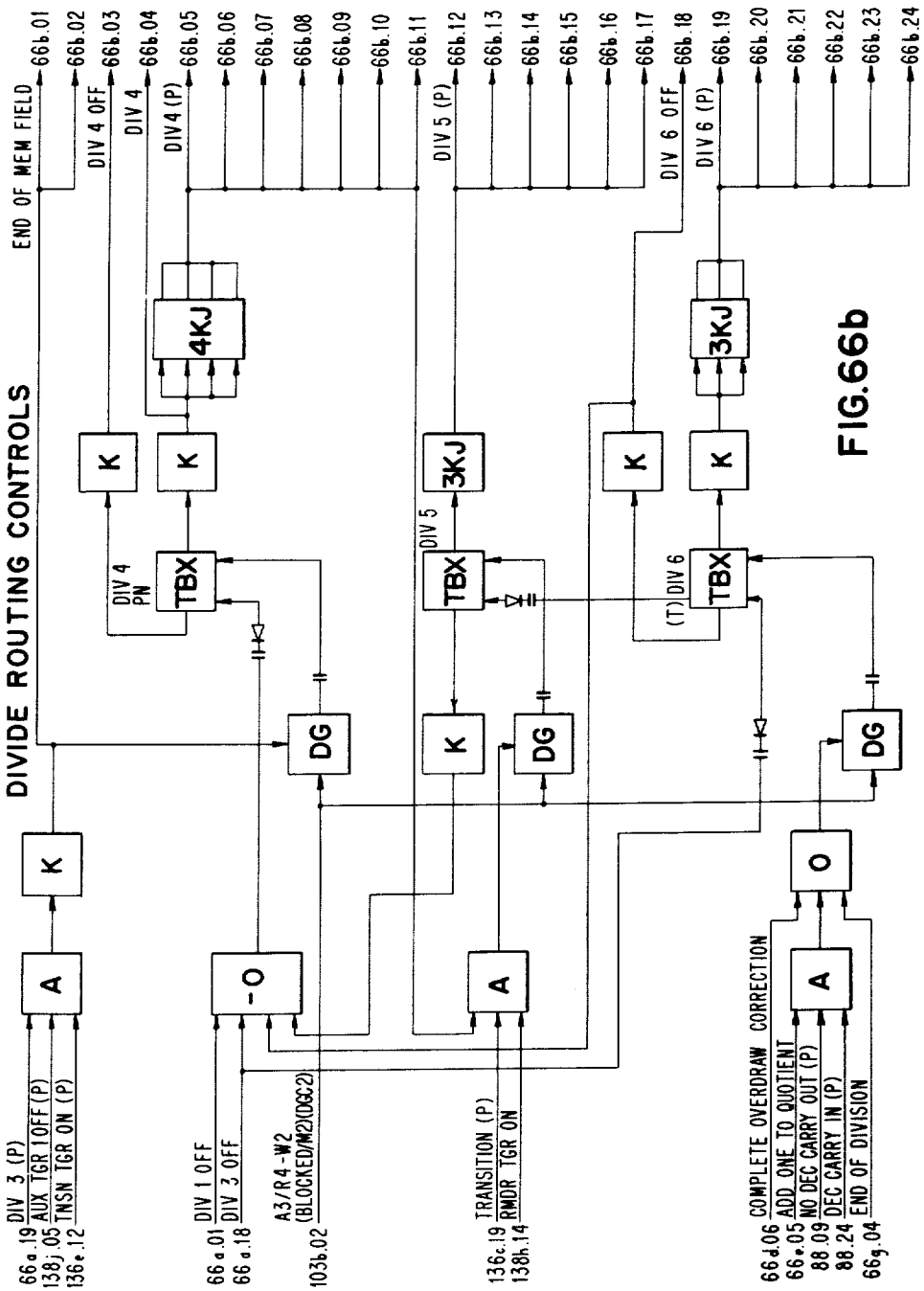

DIVIDE ROUTING CONTROLS
END OF MEM FIELD
66b.01
66b.02
DIV 4 OFF
66b.03
DIV 4
66b.04
DIV 4 (P)
66b.05
66b.06
66b.07
66b.08
66b.09
66b.10
66b.11
DIV 5 (P)
66b.12
66b.13
66b.14
66b.15
66b.16
66b.17
DIV 6 OFF
66b.18
DIV 6 (P)
66b.19
66b.20
66b.21
66b.22
66b.23
66b.24
4KJ
3KJ
3KJ
K
K
K
K
K
DIV 4 PN
TBX
TBX
DIV 5
TBX
(T) DIV 6
DG
DG
DG
A
-O
A
O
A
DIV 3 (P)
AUX TGR 1 OFF (P)
TNSN TGR ON (P)
66a.19
138j.05
136e.12
DIV 1 OFF
DIV 3 OFF
A3/R4-W2
(BLOCKED/M2)(DGC2)
66a.01
66a.18
103b.02
TRANSITION (P)
RMDR TGR ON
136c.19
138h.14
COMPLETE OVERDRAW CORRECTION
ADD ONE TO QUOTIENT
NO DEC CARRY OUT (P)
DEC CARRY IN (P)
END OF DIVISION
66d.06
66e.05
88.09
88.24
66g.04

FIG.66b

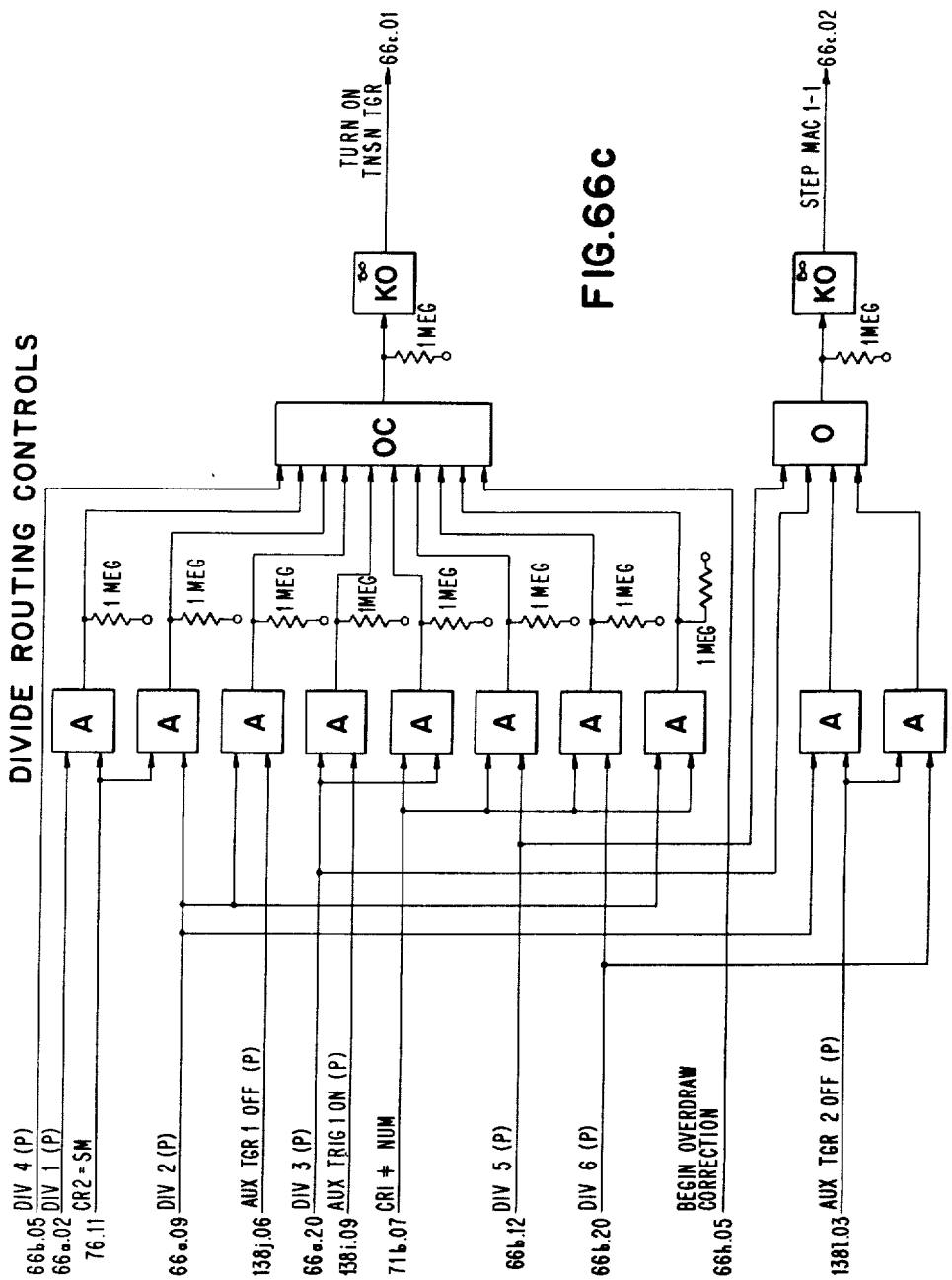

DIVIDE ROUTING CONTROLS
TURN ON TNS'N TGR
66c.01
STEP MAC 1-1
66c.02
KO
KO
1 MEG
OC
O
A
DIV 4 (P)
66b.05
DIV 1 (P)
66a.02
CR2 = SM
76.11
DIV 2 (P)
66a.09
AUX TGR 1 OFF (P)
138j.06
DIV 3 (P)
66a.20
AUX TRIG 1 ON (P)
138i.09
CR1 = NUM
71b.07
DIV 5 (P)
66b.12
DIV 6 (P)
66b.20
BEGIN OVERDRAW CORRECTION
66h.05
AUX TGR 2 OFF (P)
138l.03

FIG.66c

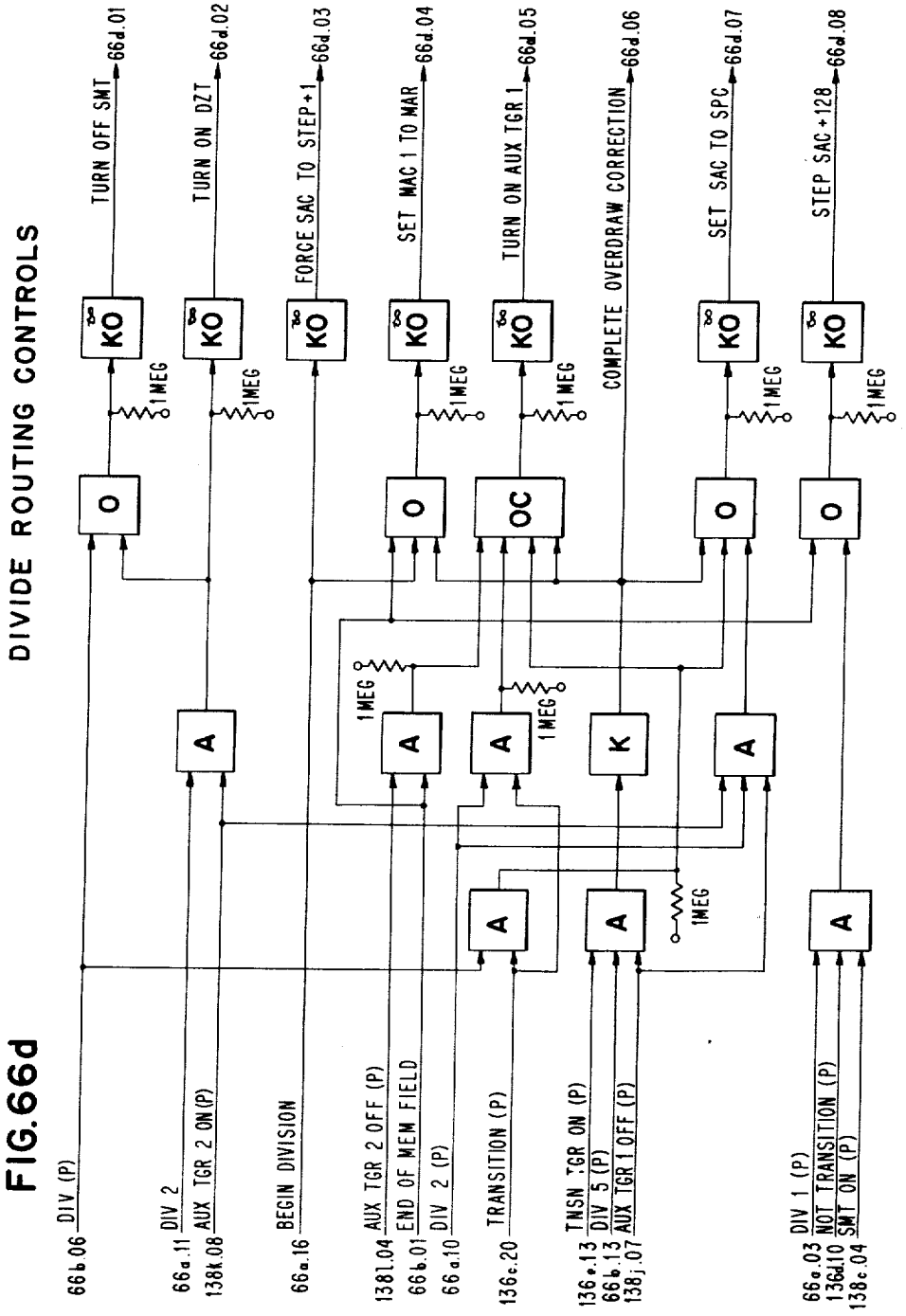

DIVIDE ROUTING CONTROLS
TURN OFF SMT 66d.01
TURN ON DZT 66d.02
FORCE SAC TO STEP+1 66d.03
SET MAC 1 TO MAR 66d.04
TURN ON AUX TGR 1 66d.05
COMPLETE OVERDRAW CORRECTION 66d.06
SET SAC TO SPC 66d.07
STEP SAC+128 66d.08
KO
O
OC
A
K
1MEG
66b.06 DIV (P)
66a.11 DIV 2
138k.08 AUX TGR 2 ON (P)
66a.16 BEGIN DIVISION
1381.04 AUX TGR 2 OFF (P)
66b.01 END OF MEM FIELD
66a.10 DIV 2 (P)
136c.20 TRANSITION (P)
136e.13 TNSN TGR ON (P)
66b.13 DIV 5 (P)
138j.07 AUX TGR 1 OFF (P)
66a.03 DIV 1 (P)
136d.10 NOT TRANSITION (P)
138c.04 SMT ON (P)

FIG.66d

FIG. 66e

DIVIDE ROUTING CONTROLS

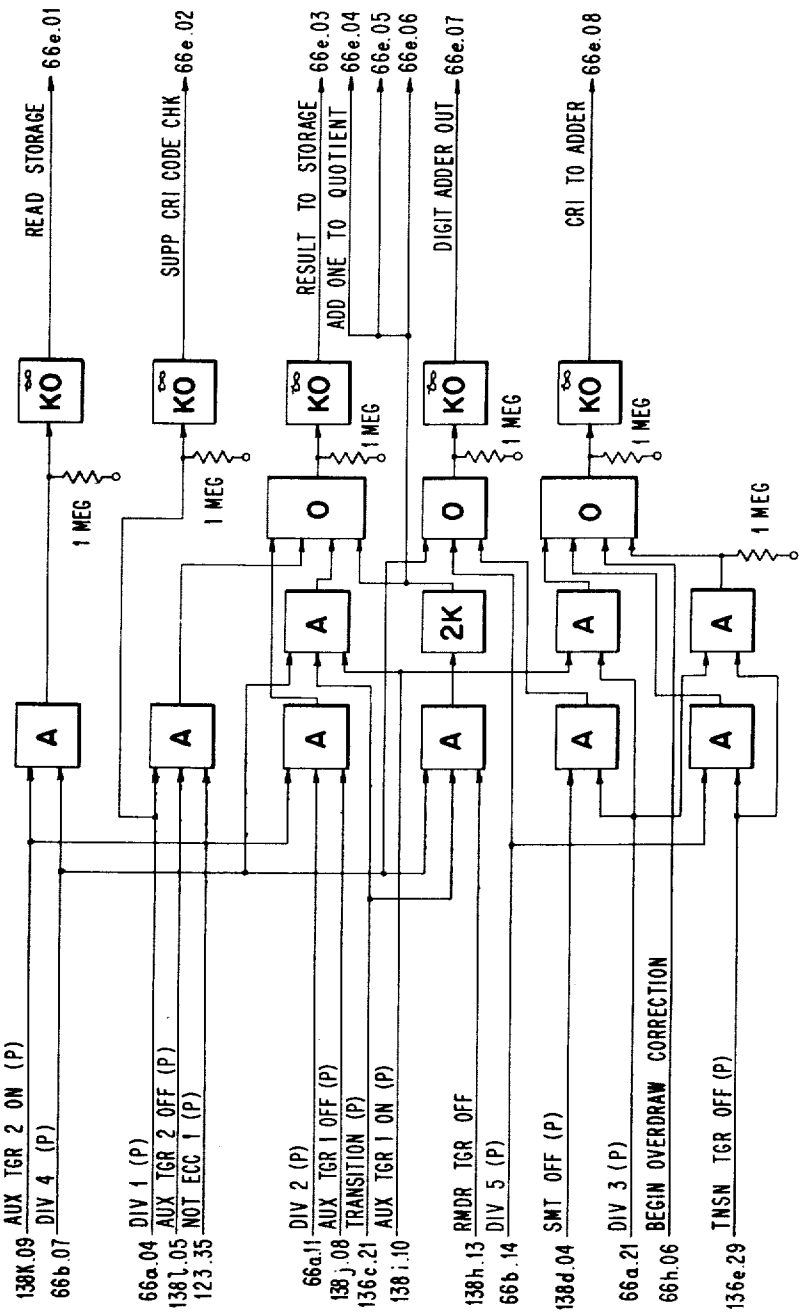
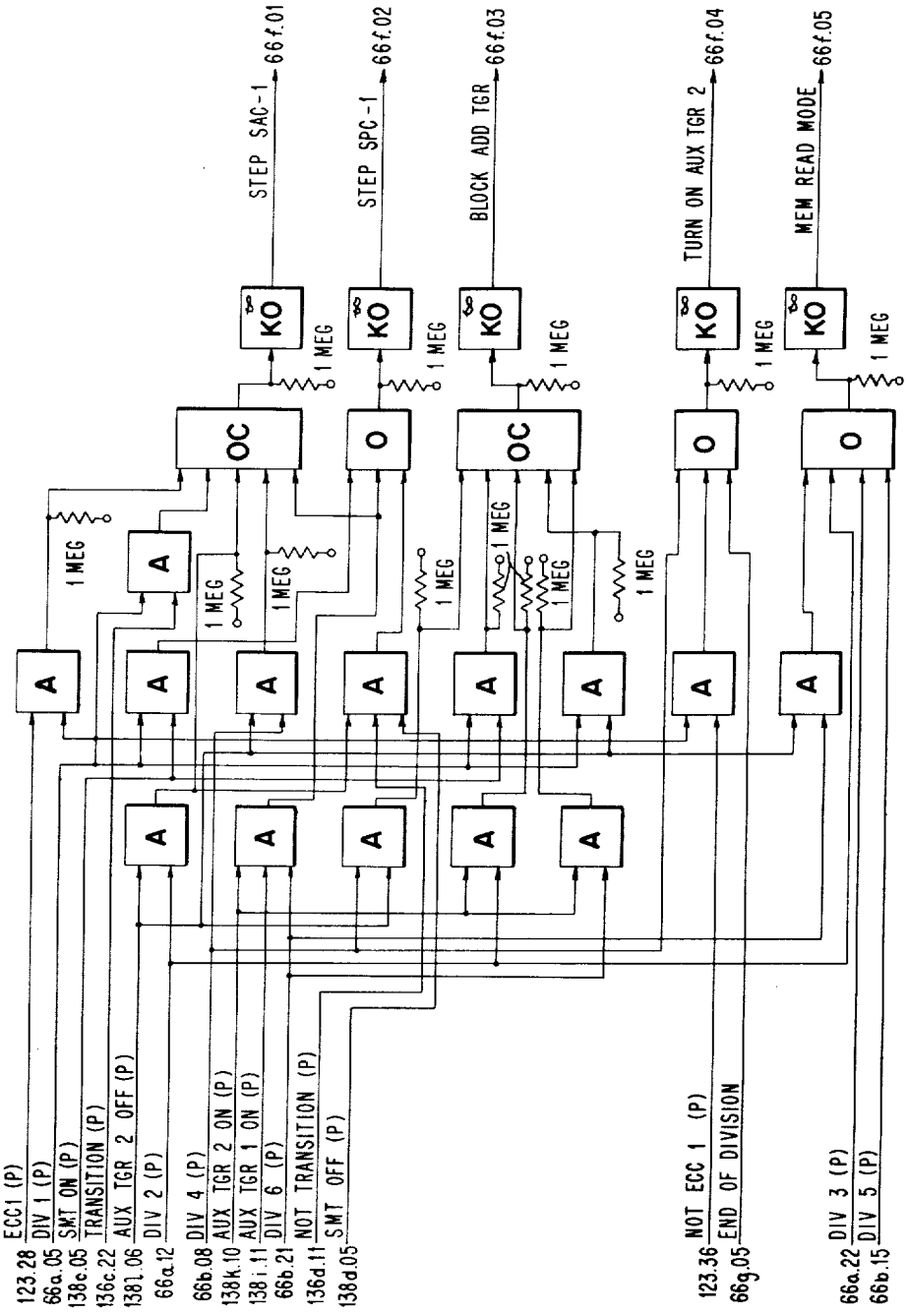


FIG. 66f

DIVIDE ROUTING CONTROLS



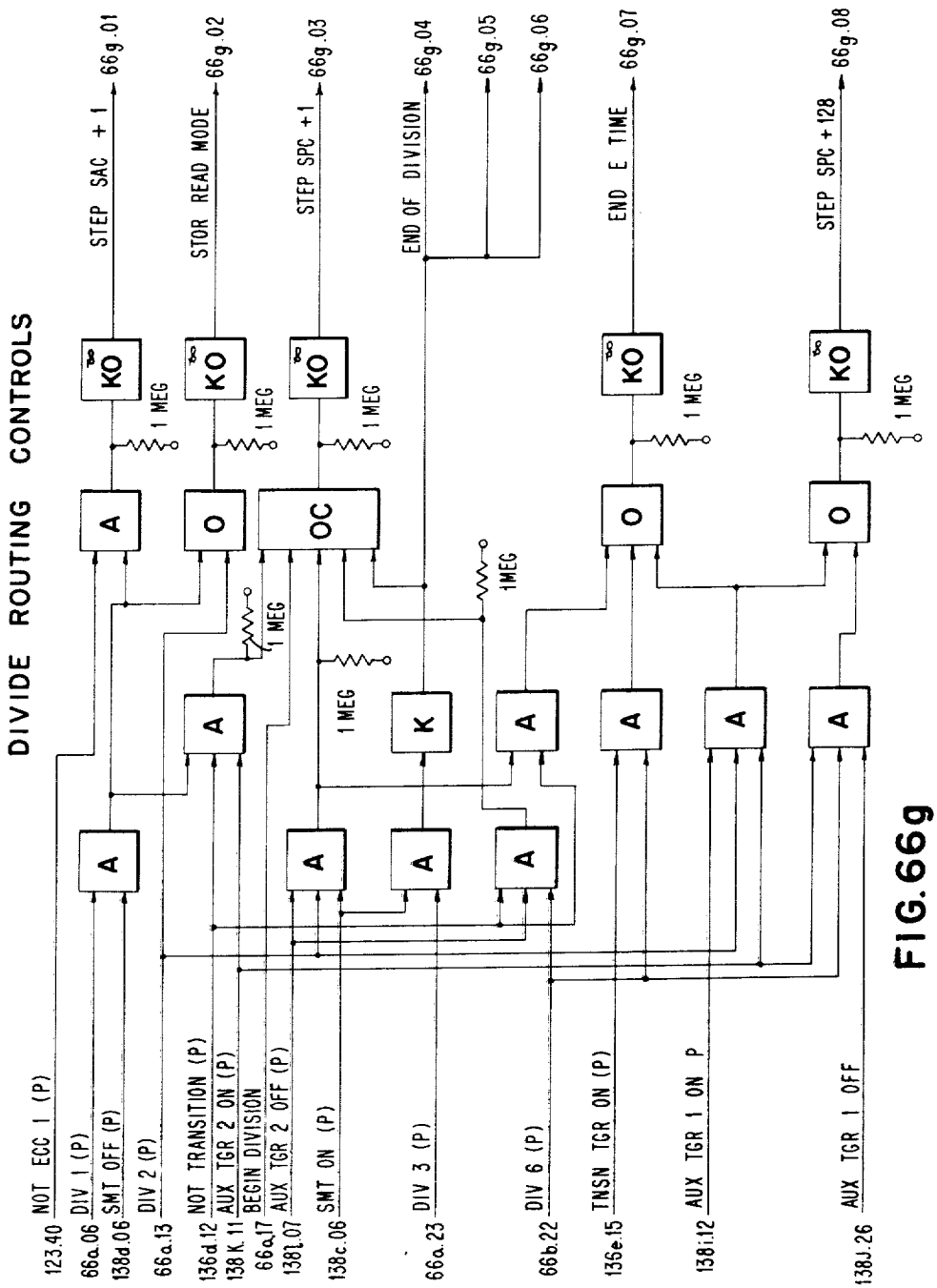

DIVIDE ROUTING CONTROLS
123.40 NOT ECC 1 (P)
66a.06 DIV 1 (P)
138d.06 SMT OFF (P)
66a.13 DIV 2 (P)
136d.12 NOT TRANSITION (P)
138K.11 AUX TGR 2 ON (P)
66a.17 BEGIN DIVISION
138l.07 AUX TGR 2 OFF (P)
138c.06 SMT ON (P)
66a.23 DIV 3 (P)
66b.22 DIV 6 (P)
136e.15 TNSN TGR ON (P)
138i.12 AUX TGR 1 ON P
138J.26 AUX TGR 1 OFF
STEP SAC + 1 66g.01
STOR READ MODE 66g.02
STEP SPC +1 66g.03
END OF DIVISION 66g.04
66g.05
66g.06
END E TIME 66g.07
STEP SPC +128 66g.08
KO
A
O
OC
K
1 MEG
1MEG

FIG.66g

FIG. 66h DIVIDE ROUTING CONTROLS

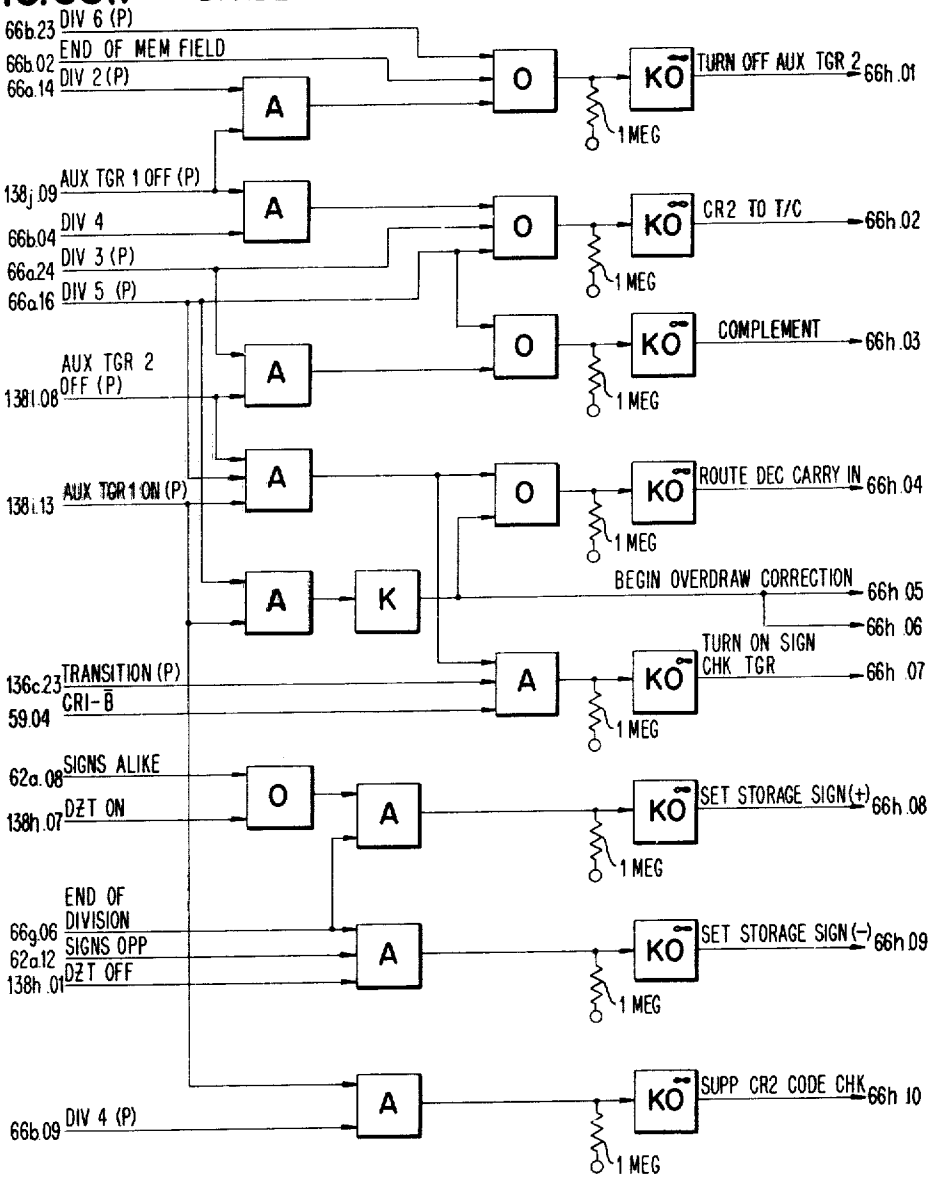


FIG. 66i

DIVIDE ROUTING CONTROLS

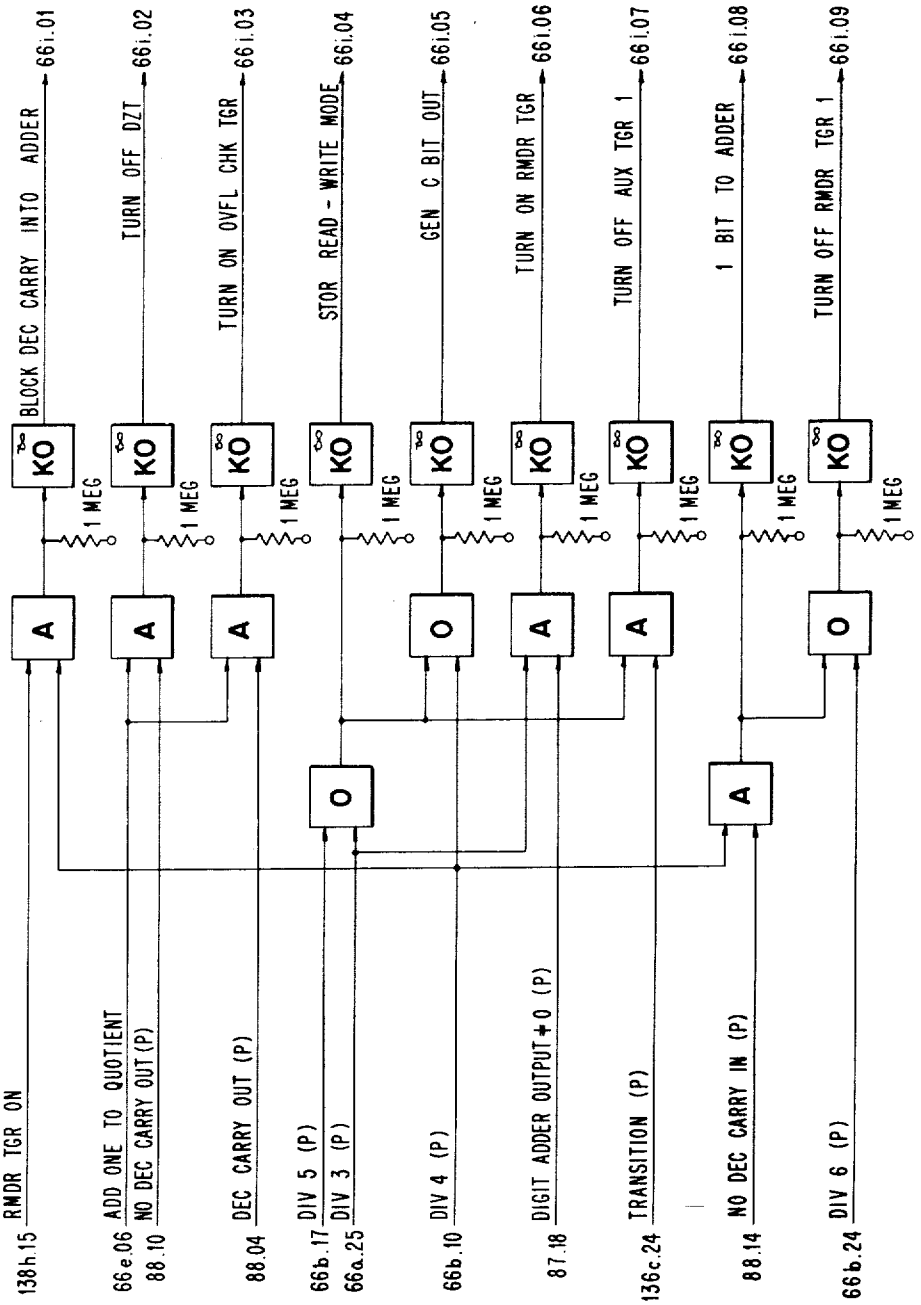


FIG. 67a

MULTIPLY ROUTING CONTROLS

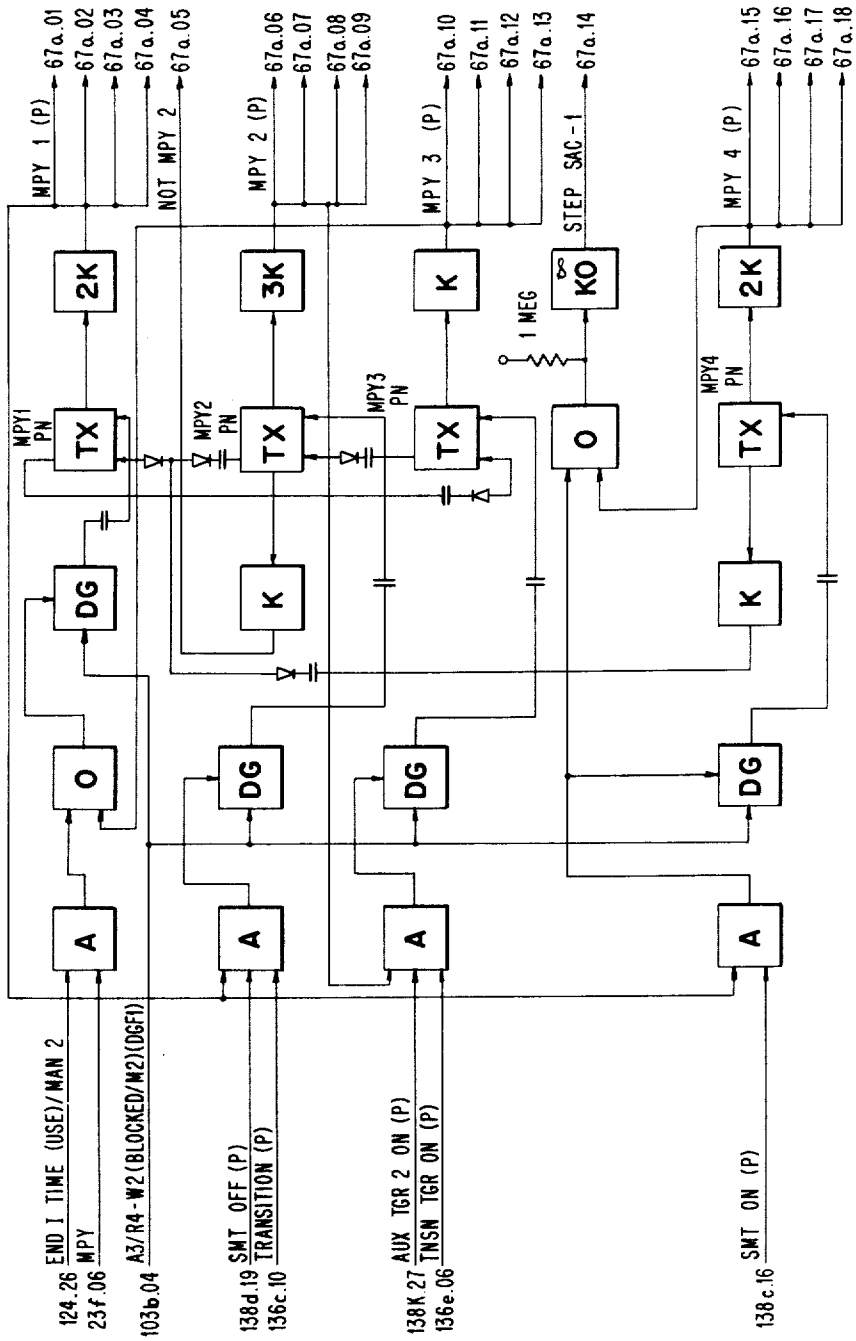


FIG. 67b
MULTIPLY ROUTING CONTROL

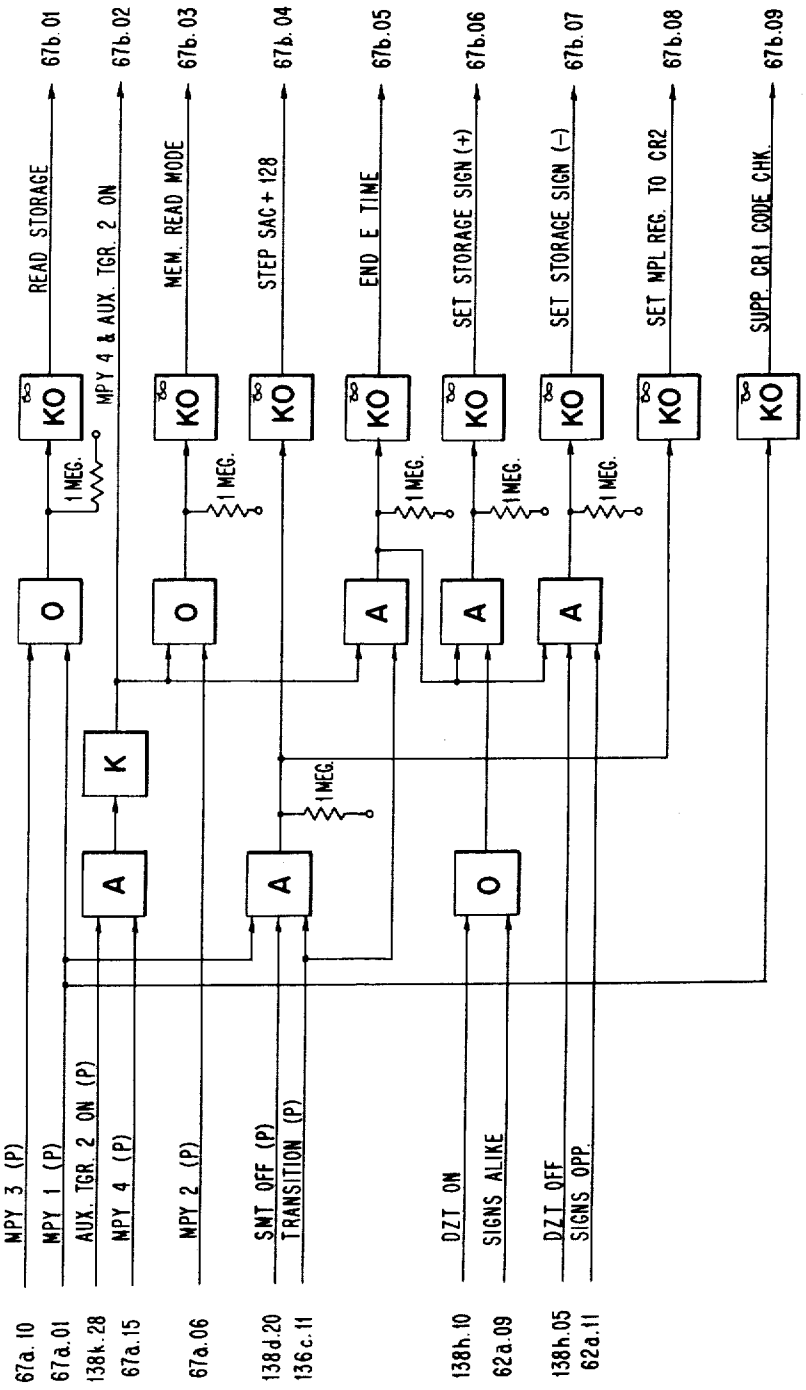
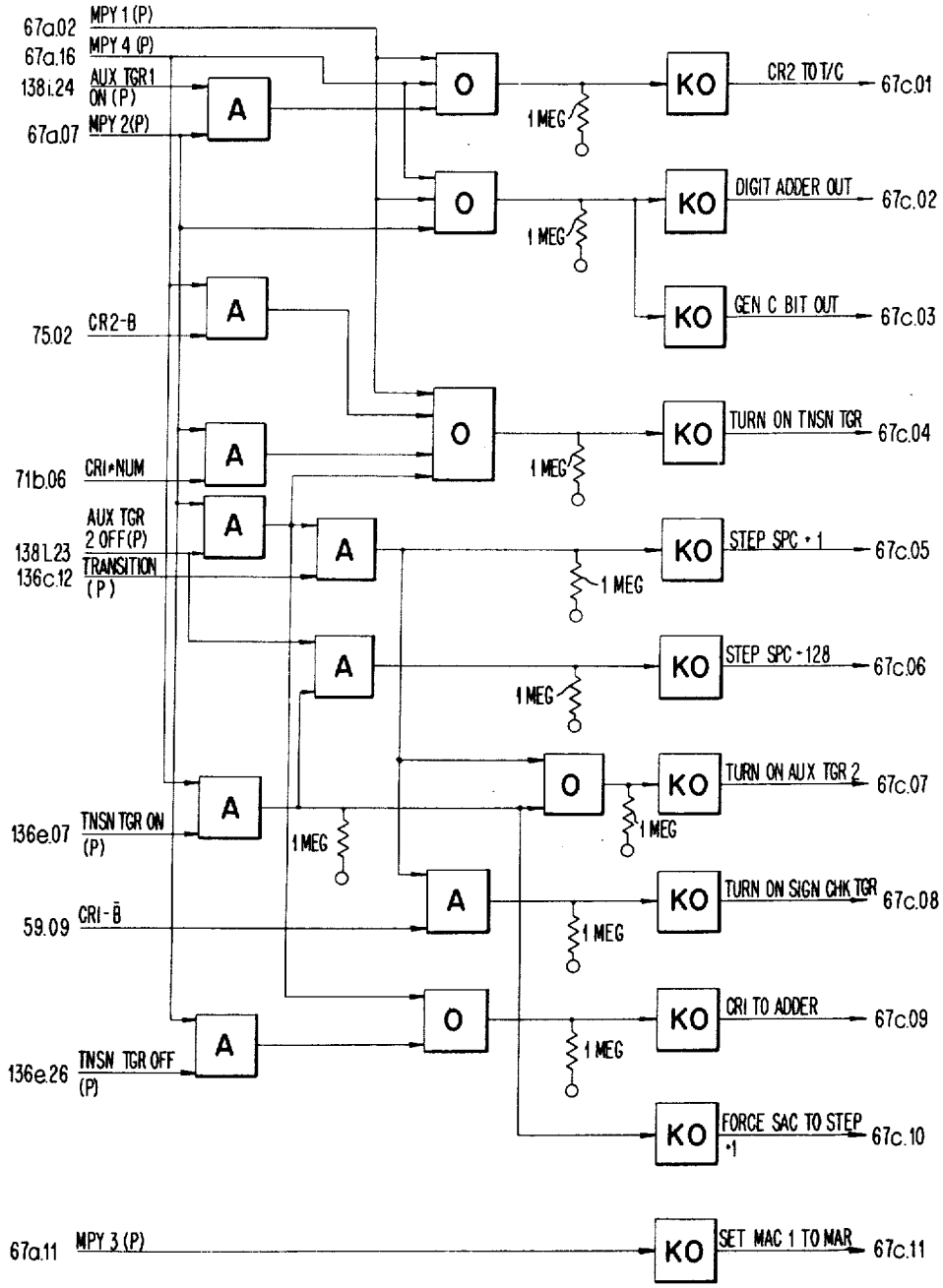


FIG.67c MULTIPLY ROUTING CONTROLS



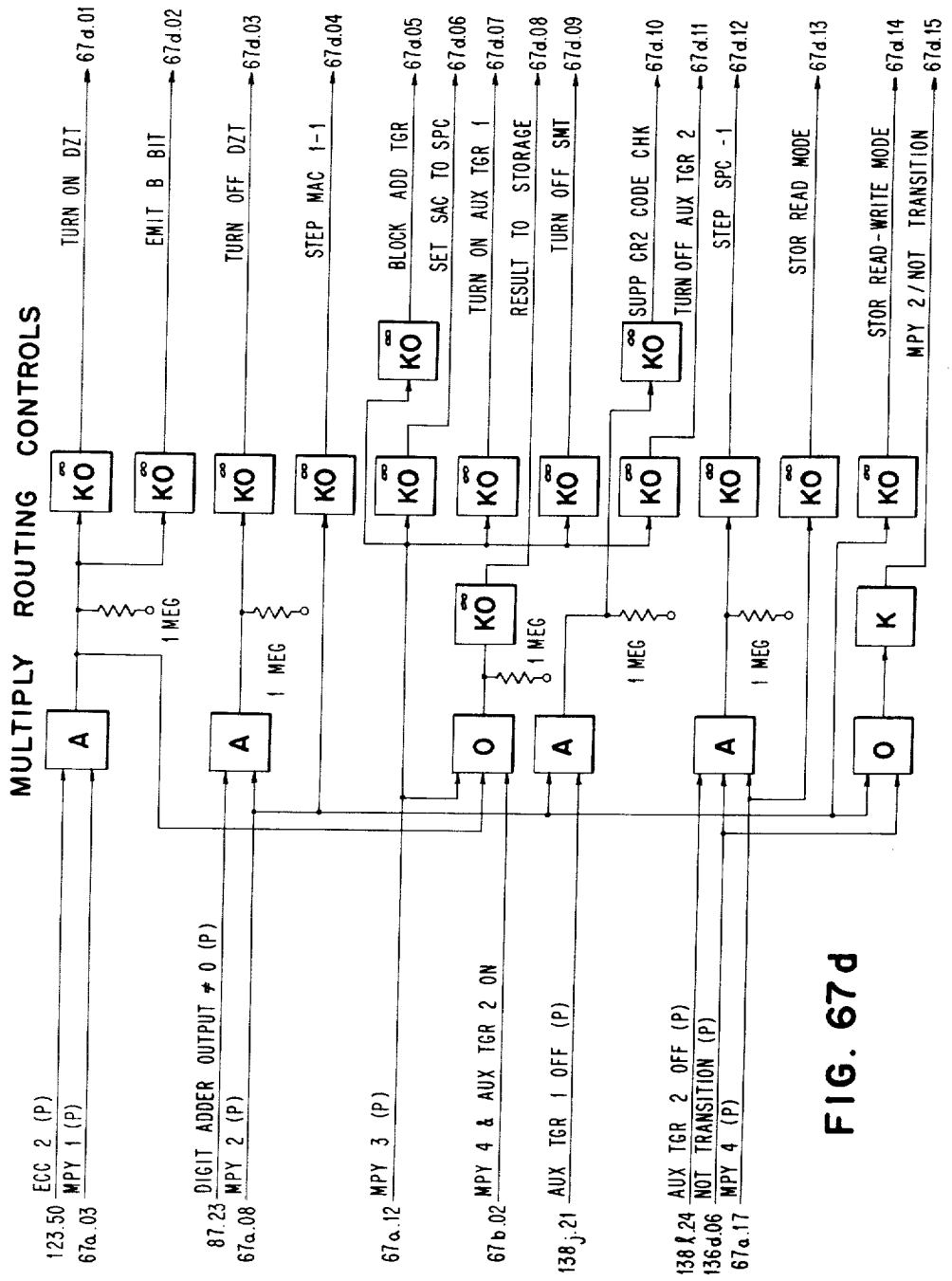

MULTIPLY ROUTING CONTROLS
TURN ON DZT
67d.01
EMIT B BIT
67d.02
TURN OFF DZT
67d.03
STEP MAC 1-1
67d.04
BLOCK ADD TGR
67d.05
SET SAC TO SPC
67d.06
TURN ON AUX TGR 1
67d.07
RESULT TO STORAGE
67d.08
TURN OFF SMT
67d.09
SUPP CR2 CODE CHK
67d.10
TURN OFF AUX TGR 2
67d.11
STEP SPC -1
67d.12
STOR READ MODE
67d.13
STOR READ-WRITE MODE
67d.14
MPY 2/NOT TRANSITION
67d.15
KO
A
O
K
1 MEG
123.50 ECC 2 (P)
67a.03 MPY 1 (P)
87.23 DIGIT ADDER OUTPUT ≠ 0 (P)
67a.08 MPY 2 (P)
67a.12 MPY 3 (P)
67b.02 MPY 4 & AUX TGR 2 ON
138 j.21 AUX TGR 1 OFF (P)
138 k.24 AUX TGR 2 OFF (P)
136d.06 NOT TRANSITION (P)
67a.17 MPY 4 (P)

FIG. 67d

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FIG. 68a

ADD TO MEMORY ROUTING CONTROLS

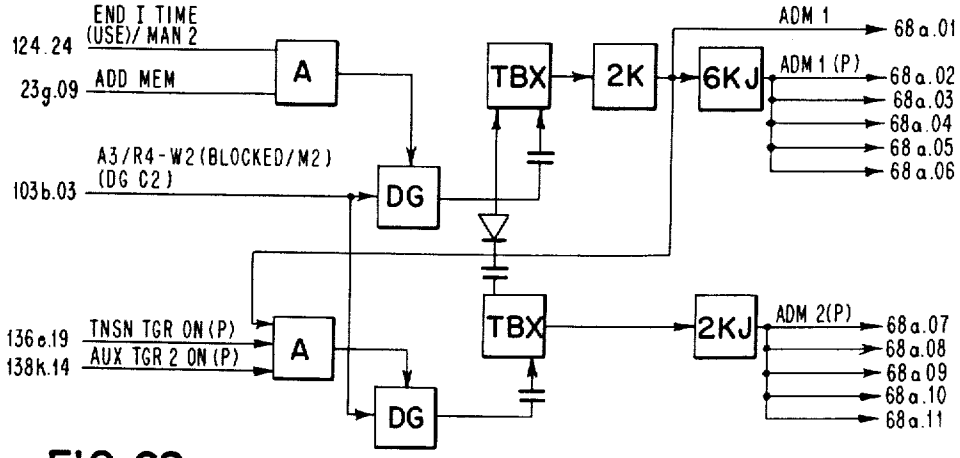


FIG. 68e

ADD TO MEMORY ROUTING CONTROLS

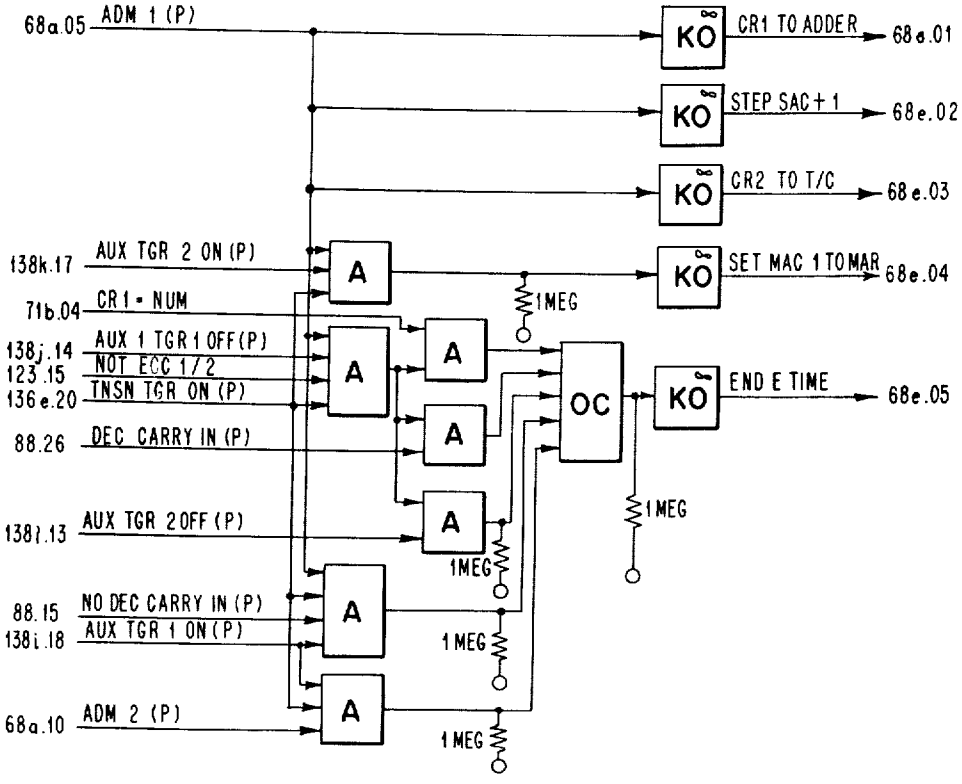


FIG.68b ADD TO MEMORY ROUTING CONTROLS

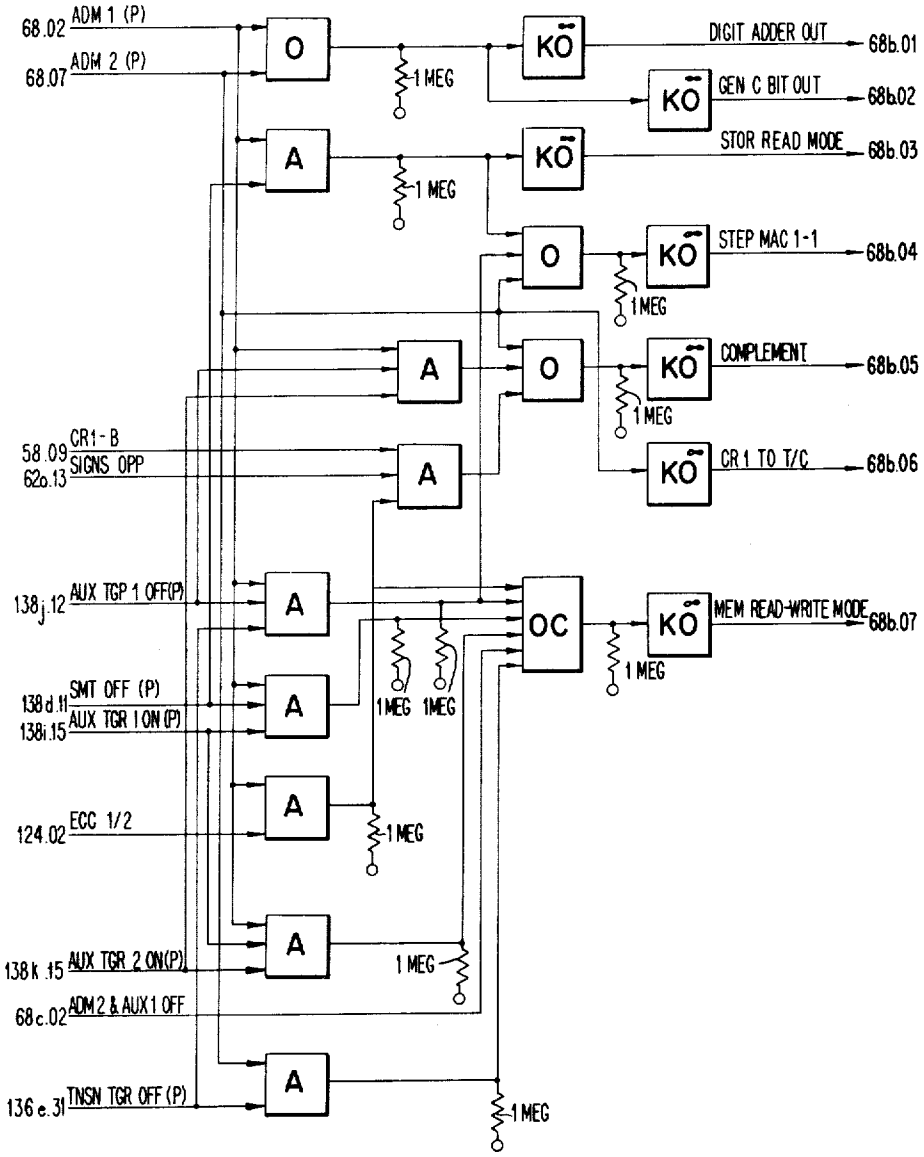


FIG.68c ADD TO MEMORY ROUTING CONTROLS

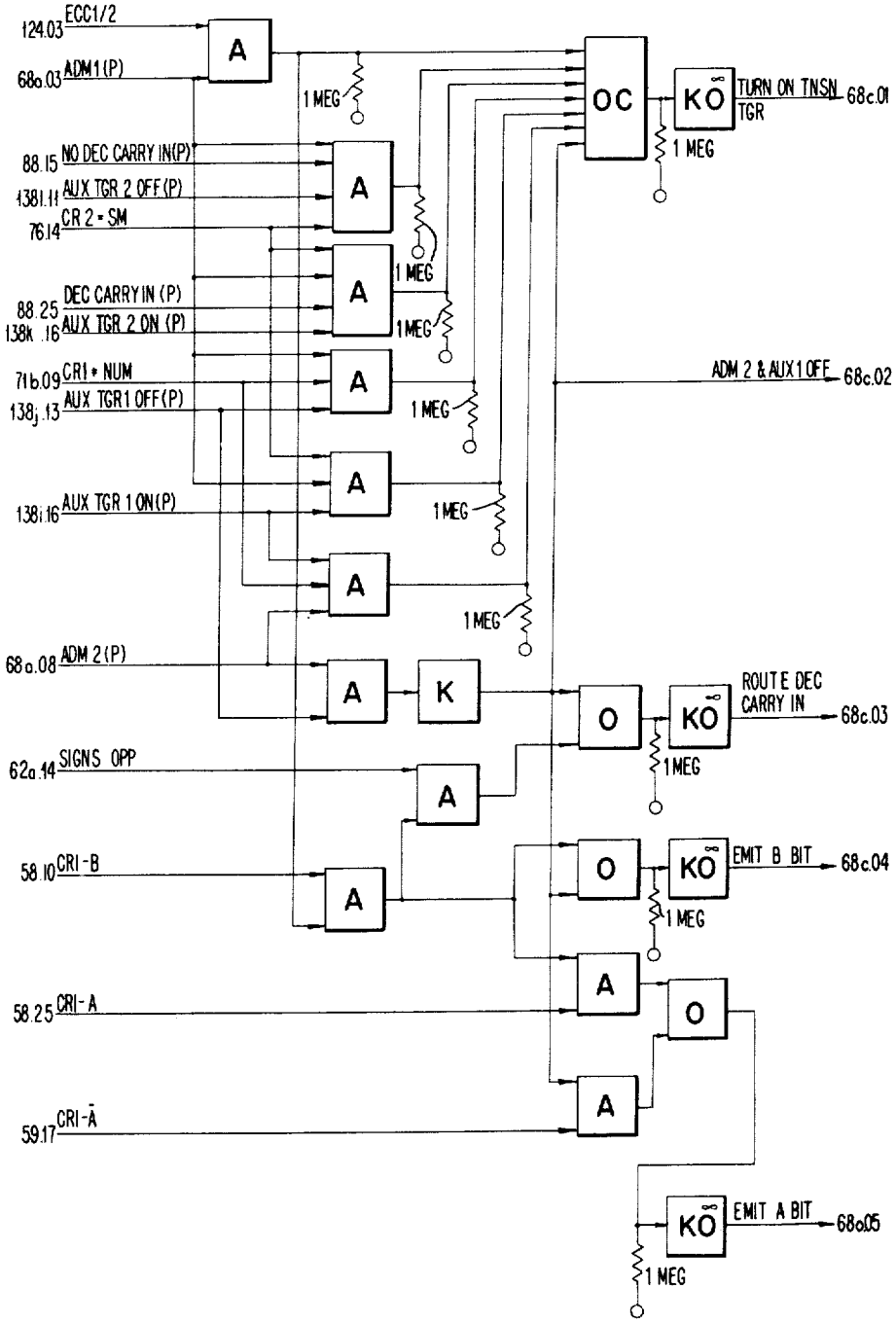
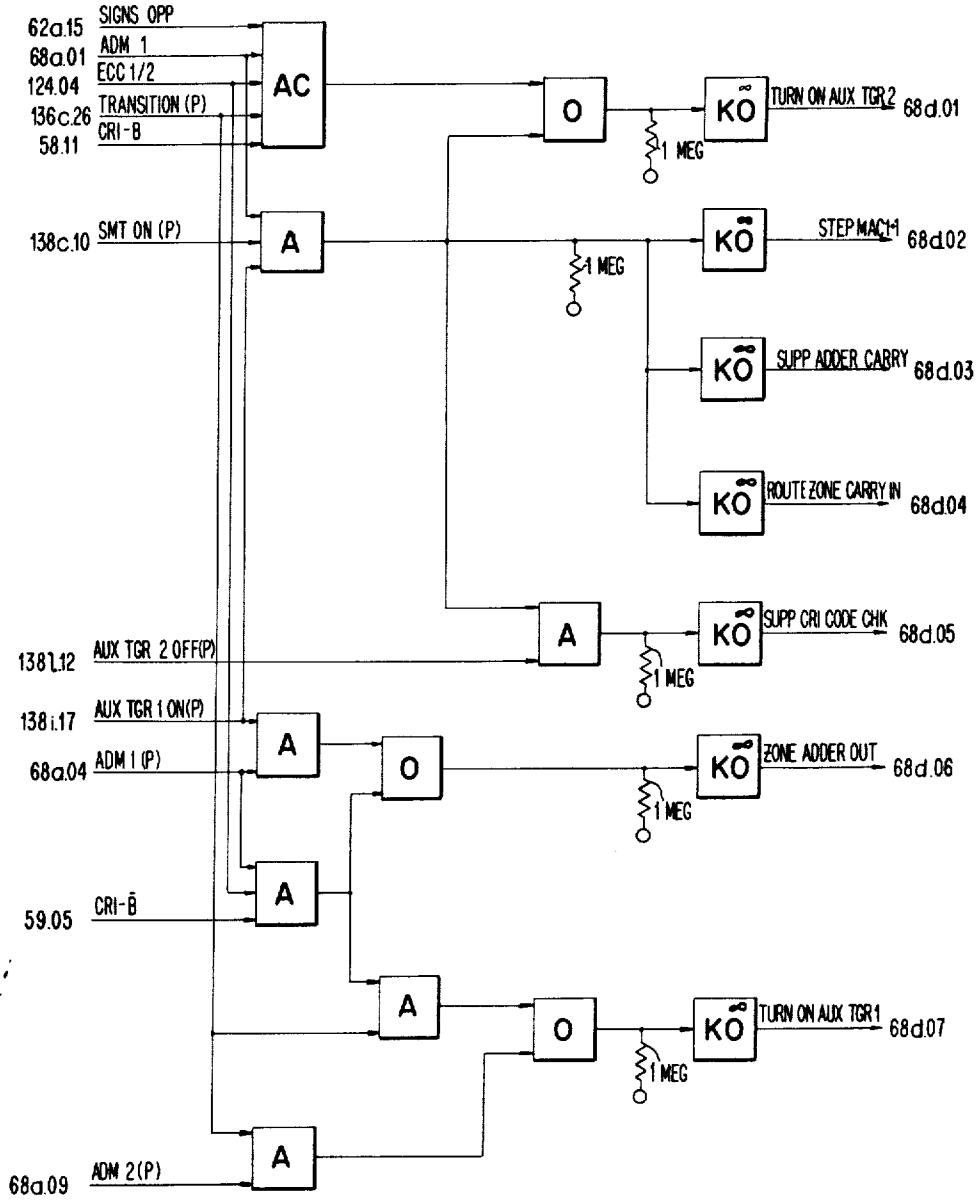


FIG. 68d ADD TO MEMORY ROUTING CONTROLS



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FIG.69a

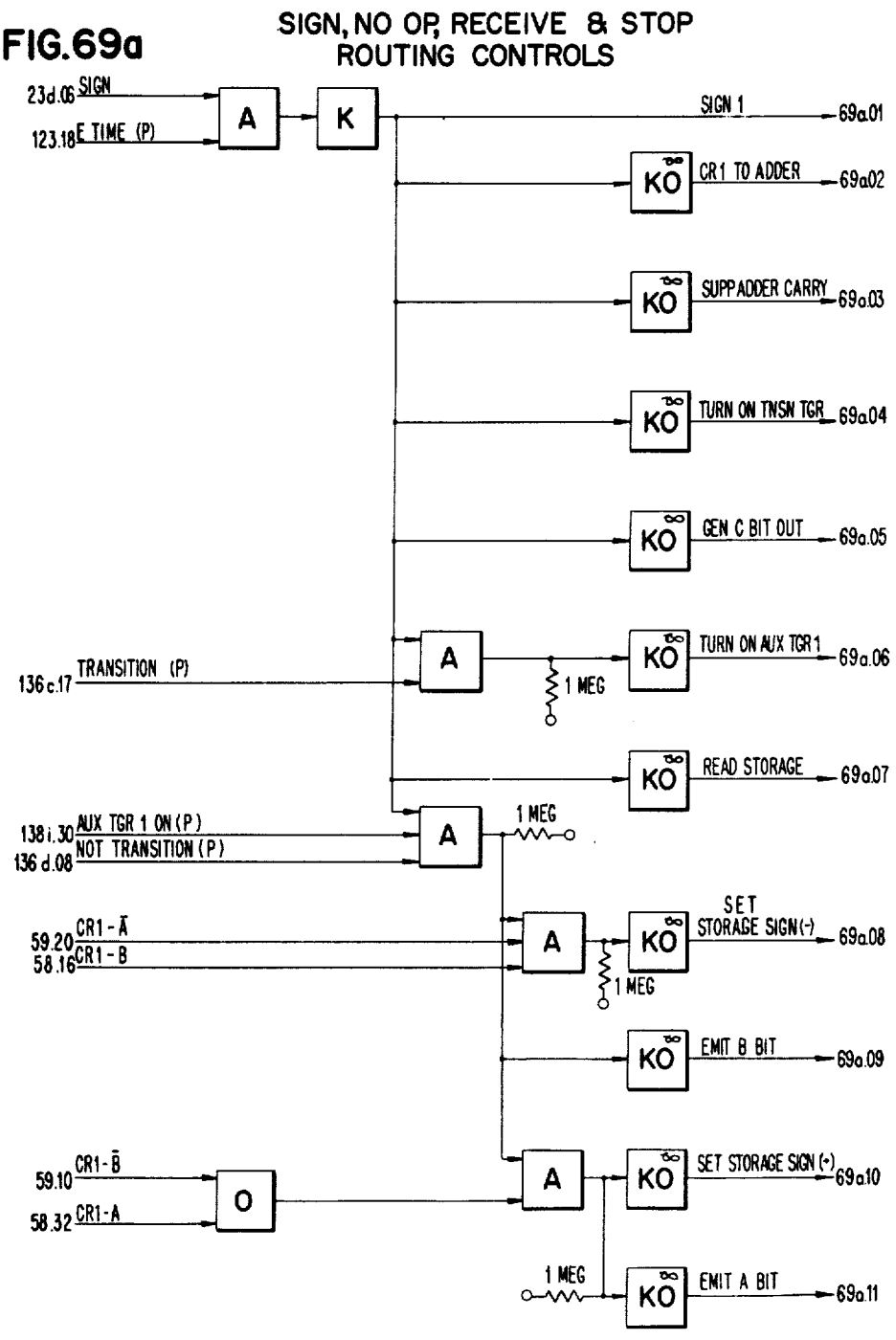
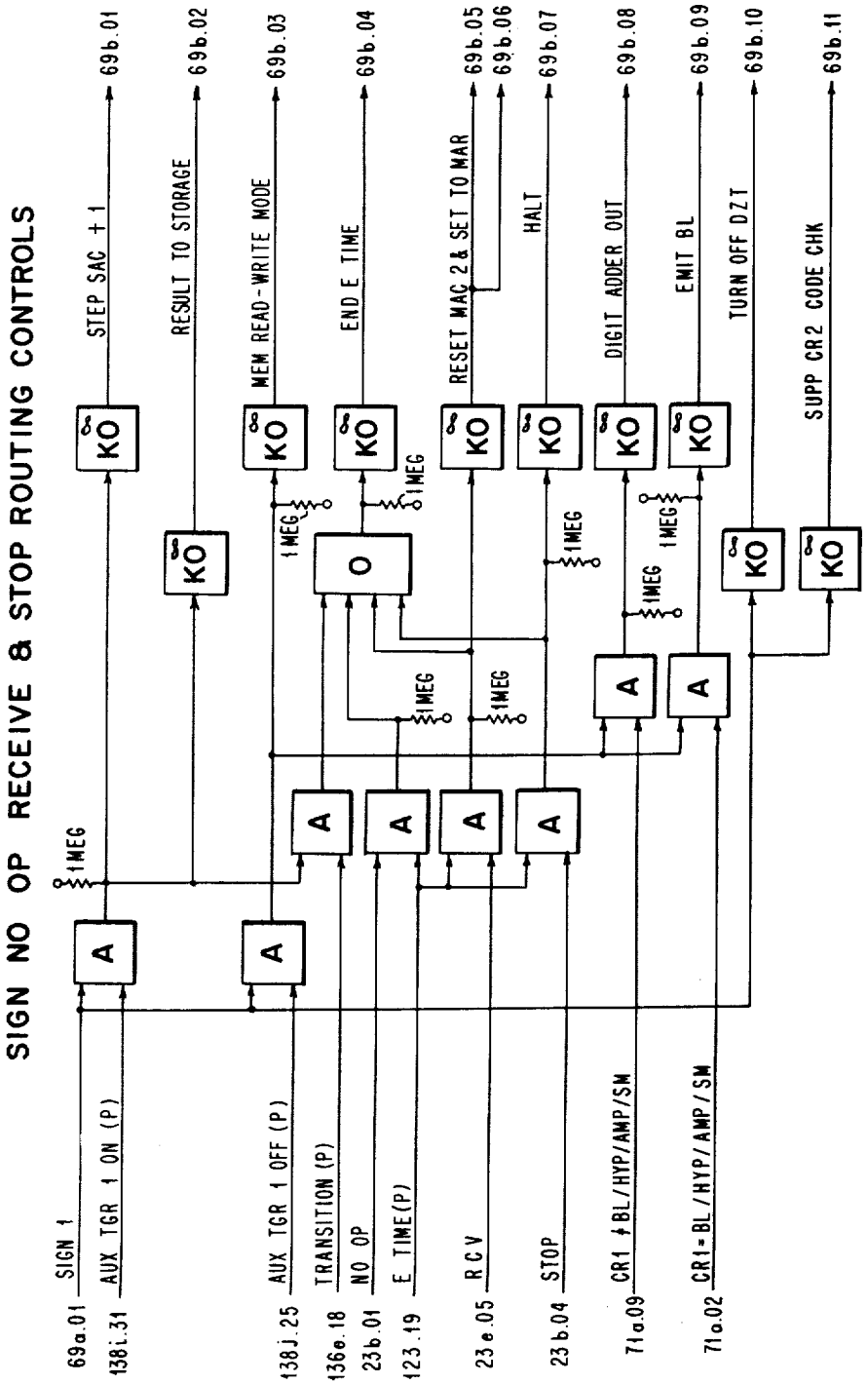


FIG. 69b


SIGN NO OP RECEIVE & STOP ROUTING CONTROLS
STEP SAC + 1
RESULT TO STORAGE
MEM READ-WRITE MODE
END E TIME
RESET MAC 2 & SET TO MAR
HALT
DIGIT ADDER OUT
EMIT BL
TURN OFF DZT
SUPP CR2 CODE CHK
69b.01
69b.02
69b.03
69b.04
69b.05
69b.06
69b.07
69b.08
69b.09
69b.10
69b.11
KO
A
O
1MEG
69a.01 SIGN 1
138i.31 AUX TGR 1 ON (P)
138j.25 AUX TGR 1 OFF (P)
136e.18 TRANSITION (P)
23b.01 NO OP
123.19 E TIME(P)
23e.05 R C V
23b.04 STOP
71a.09 CR1 ∤ BL/HYP/AMP/SW
71a.02 CR1-BL/HYP/AMP/SW

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FIG. 70a

LOAD ADDRESS ROUTING CONTROLS

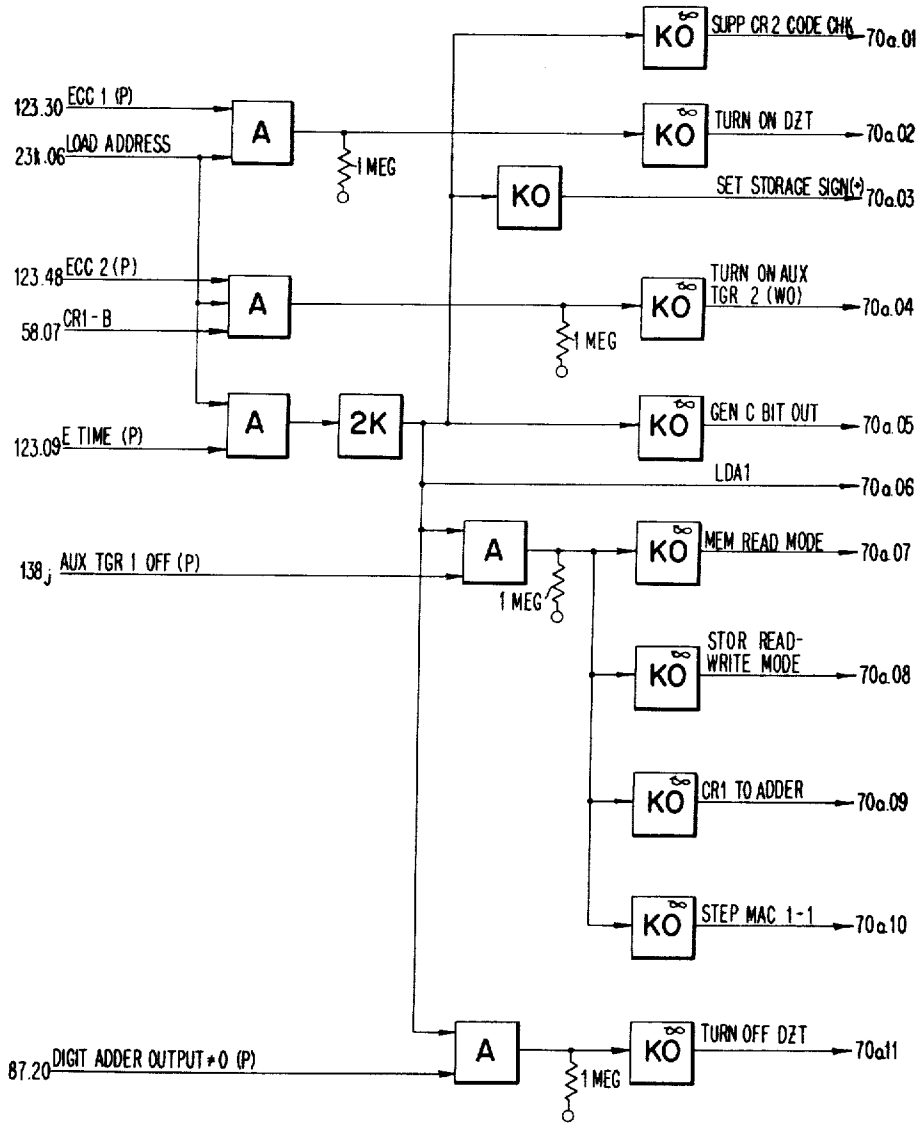
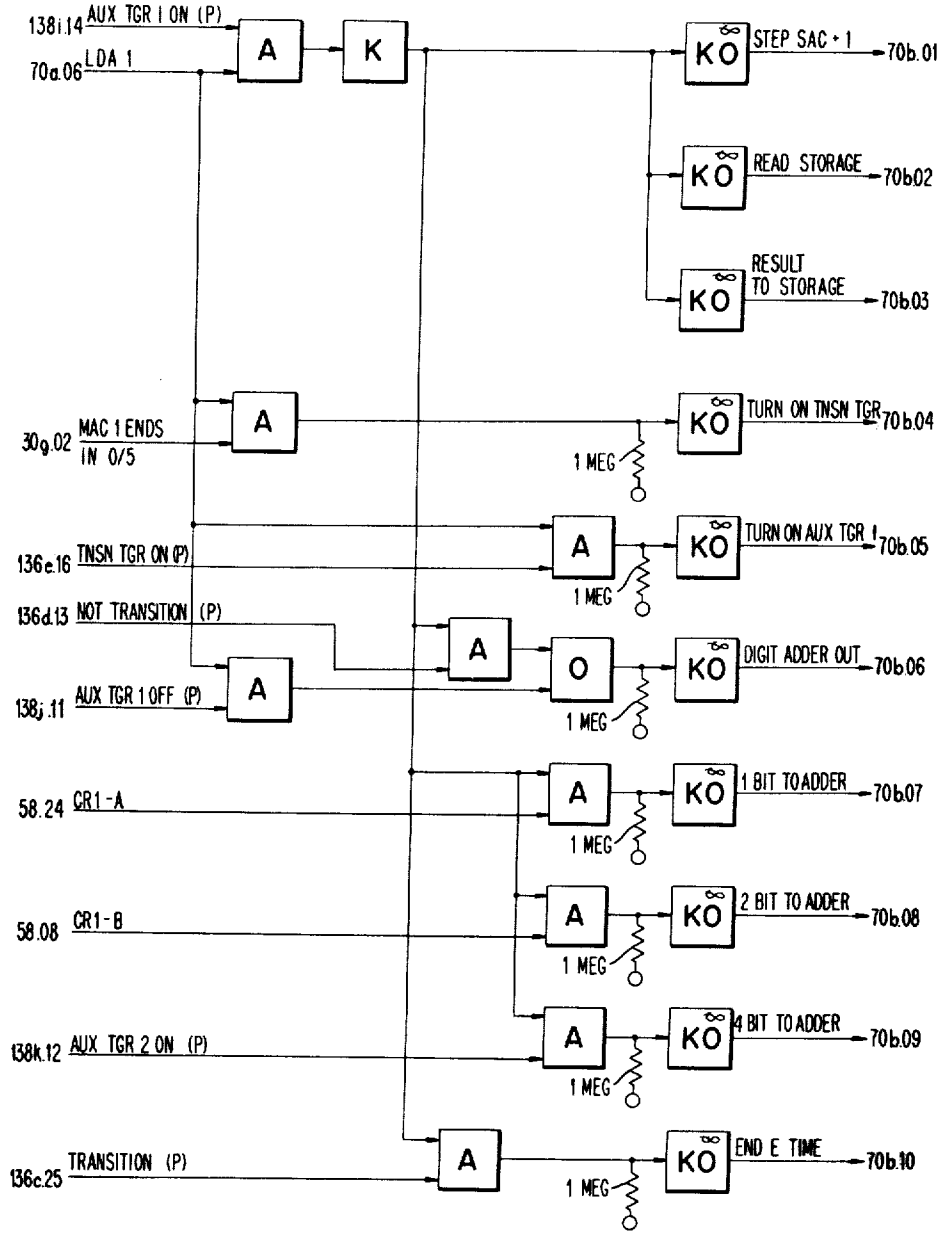


FIG. 70b LOAD ADDRESS ROUTING CONTROLS



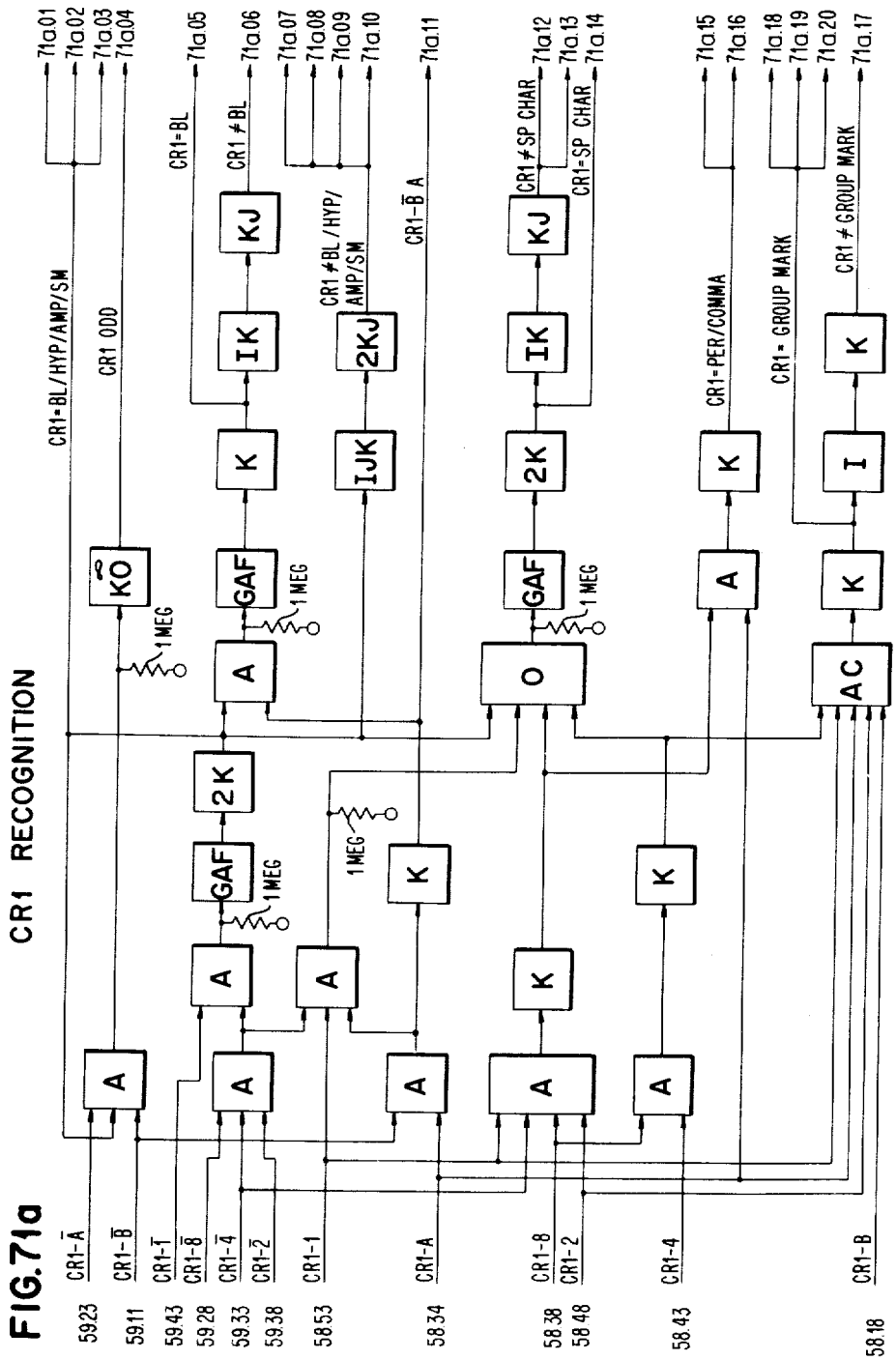

CR1 RECOGNITION
CR1-BL/HYP/AMP/SM
CR1 ODD
CR1=BL
CR1≠BL
CR1≠BL/HYP/AMP/SM
CR1-B̄ A
CR1≠SP CHAR
CR1=SP CHAR
CR1-PER/COMMA
CR1- GROUP MARK
CR1≠GROUP MARK
71a.01
71a.02
71a.03
71a.04
71a.05
71a.06
71a.07
71a.08
71a.09
71a.10
71a.11
71a.12
71a.13
71a.14
71a.15
71a.16
71a.18
71a.19
71a.20
71a.17
KO
GAF
IK
KJ
2KJ
IJK
2K
I
AC
A
K
O
1 MEG
CR1-Ā
CR1-B̄
CR1-1̄
CR1-8̄
CR1-4̄
CR1-2̄
CR1-1
CR1-A
CR1-8
CR1-2
CR1-4
CR1-B
5923
5911
5943
5928
5933
5938
5853
5834
5838
5848
5843
5818

FIG.71a

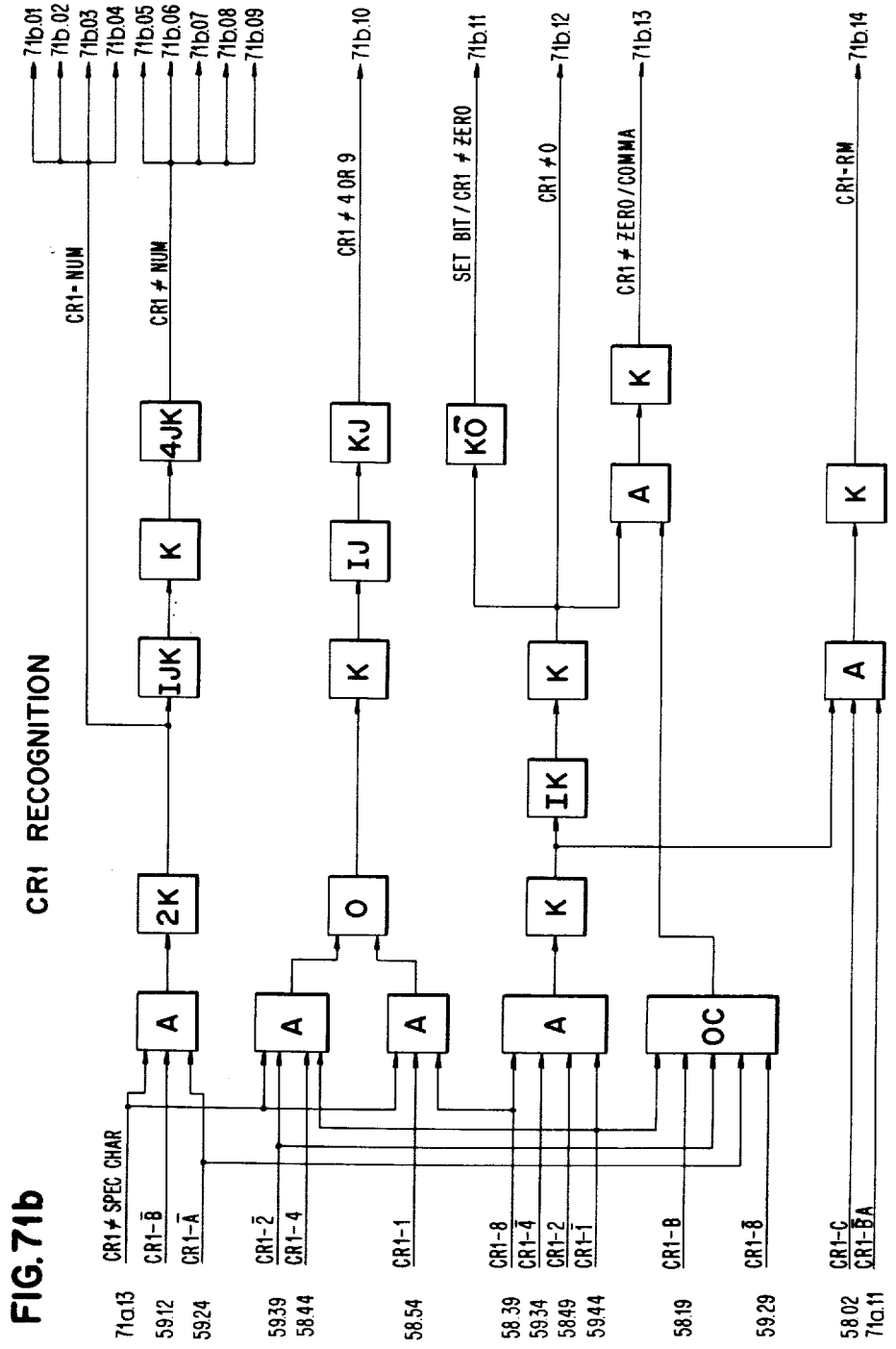

CR1 RECOGNITION
71b.01
71b.02
71b.03
71b.04
71b.05
71b.06
71b.07
71b.08
71b.09
71b.10
71b.11
71b.12
71b.13
71b.14
CR1-NUM
CR1 ≠ NUM
CR1 ≠ 4 OR 9
SET BIT / CR1 ≠ ZERO
CR1 ≠ 0
CR1 ≠ ZERO / COMMA
CR1-RM
4JK
K
IJK
2K
KJ
IJ
K
O
KŌ
K
IK
K
K
A
K
A
A
A
A
OC
A
CR1 ≠ SPEC CHAR
CR1-B̄
CR1-Ā
CR1-2̄
CR1-4
CR1-1
CR1-8
CR1-4̄
CR1-2
CR1-1̄
CR1-8
CR1-8̄
CR1-C
CR1-B̄A
71a.13
59.12
59.24
59.39
58.44
58.54
58.39
59.34
58.49
59.44
58.19
59.29
58.02
71a.11

FIG. 71b

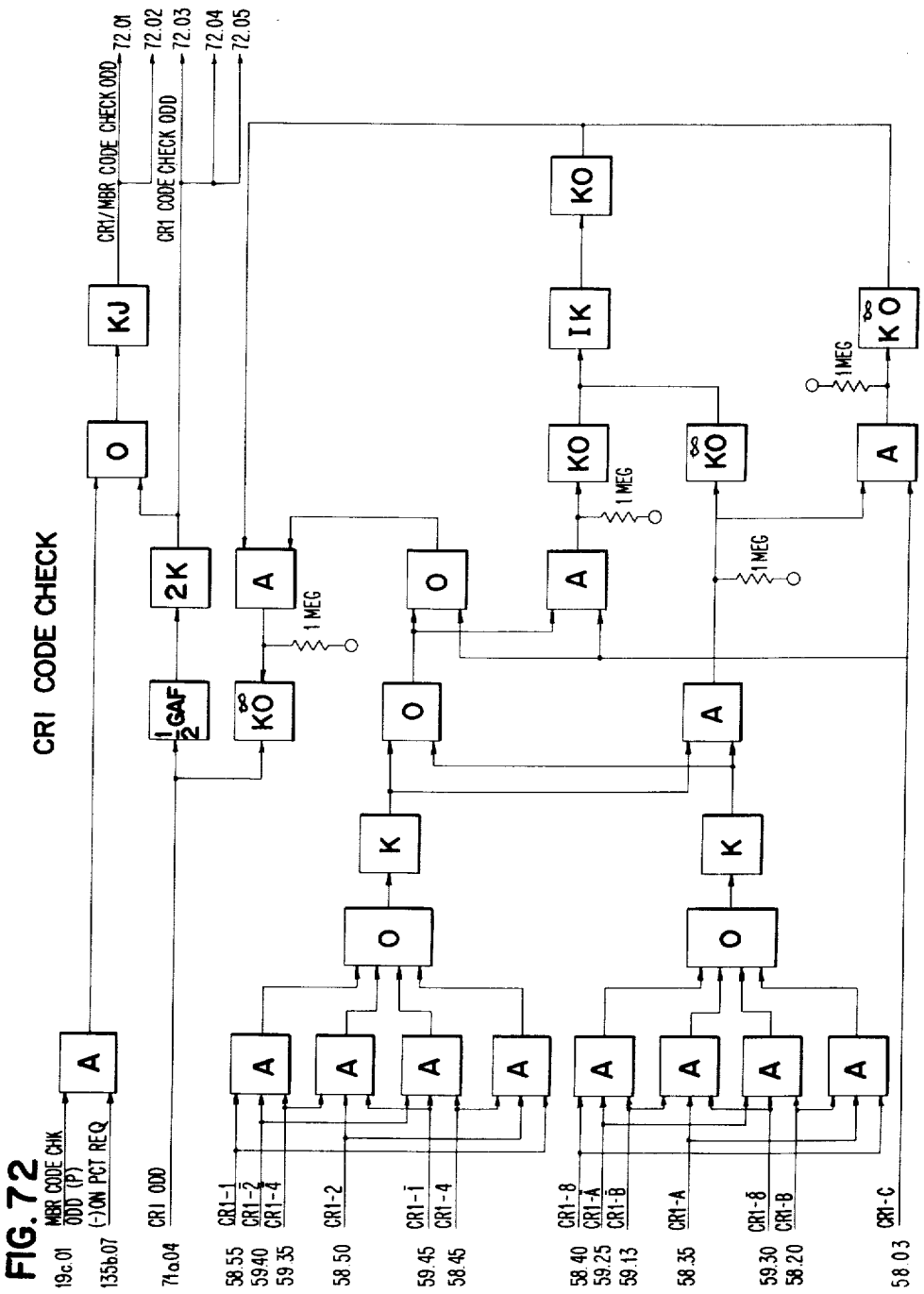

CR1 CODE CHECK
CR1/MBR CODE CHECK ODD
CR1 CODE CHECK ODD
72.01
72.02
72.03
72.04
72.05
KJ
O
2K
GAF
A
KO
1 MEG
K
IK
MBR CODE CHK ODD (P)
(-)ON PCT REQ
CR1 ODD
19c.01
135b.07
71a.04
CR1-1
CR1-2
CR1-4
CR1-8
CR1-A
CR1-B
CR1-C
58.55
59.40
59.35
58.50
59.45
58.45
58.40
59.25
59.13
58.35
59.30
58.20
58.03

FIG. 72

FIG. 73

ADDER INPUT SWITCHING

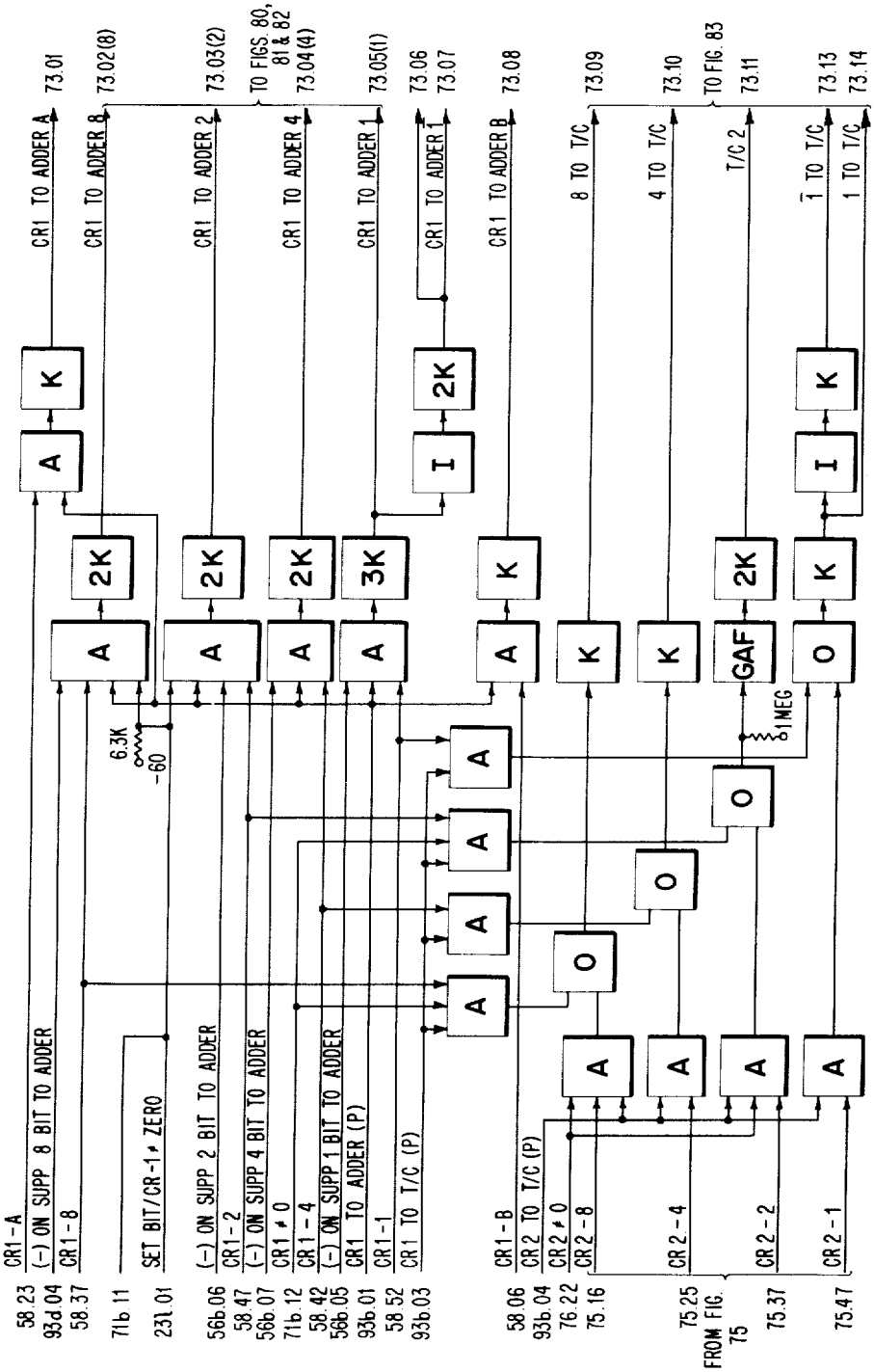


FIG. 74a

RESET ADD, RESET SUB, ADD-SUB ROUTING CONTROLS

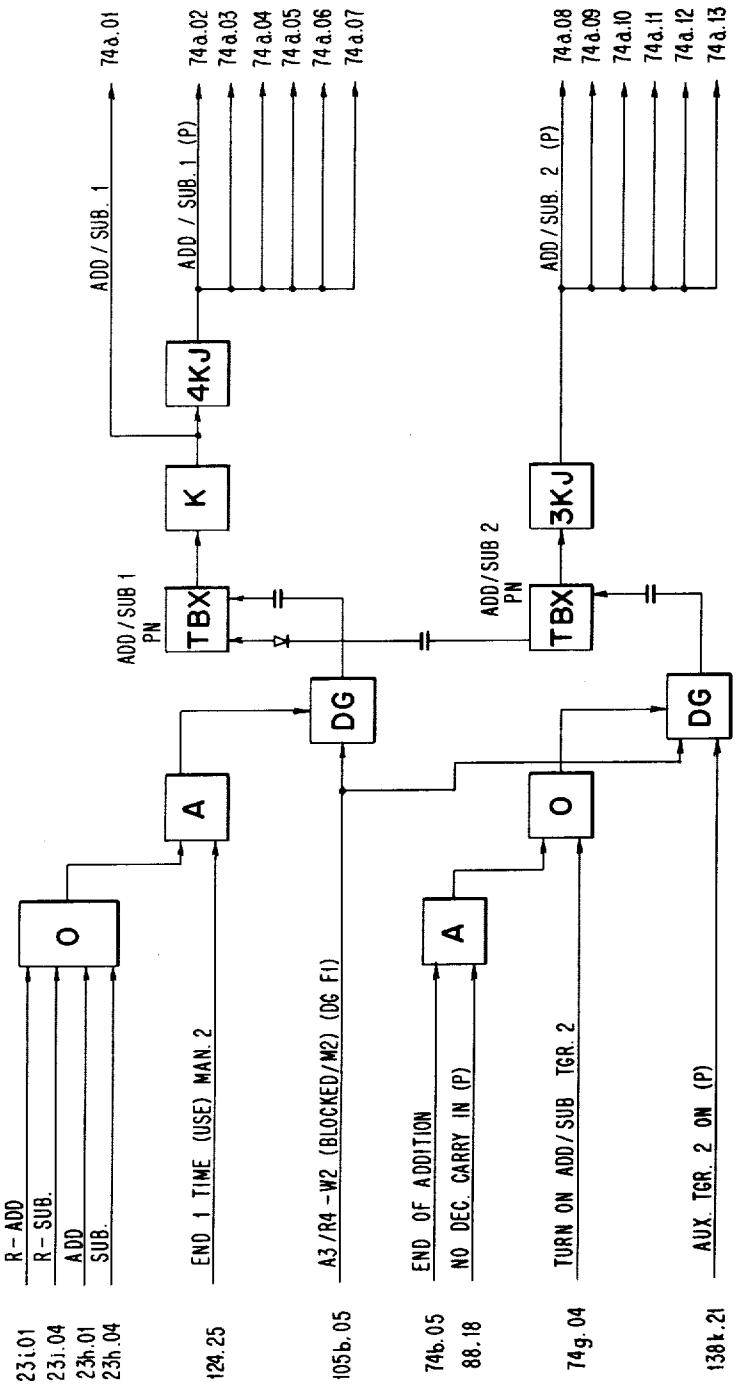


FIG. 74b

RESET ADD, RESET SUB, ADD-SUB ROUTING CONTROLS

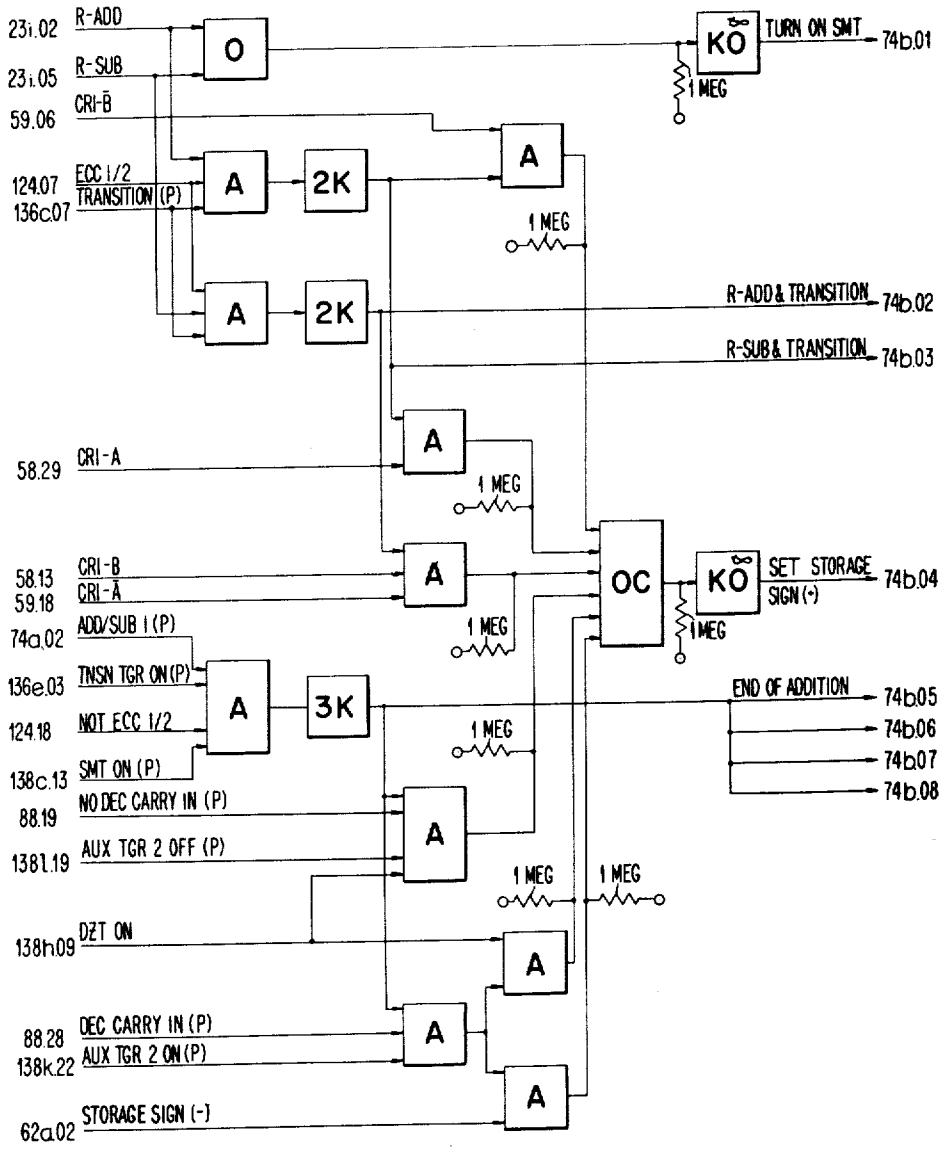
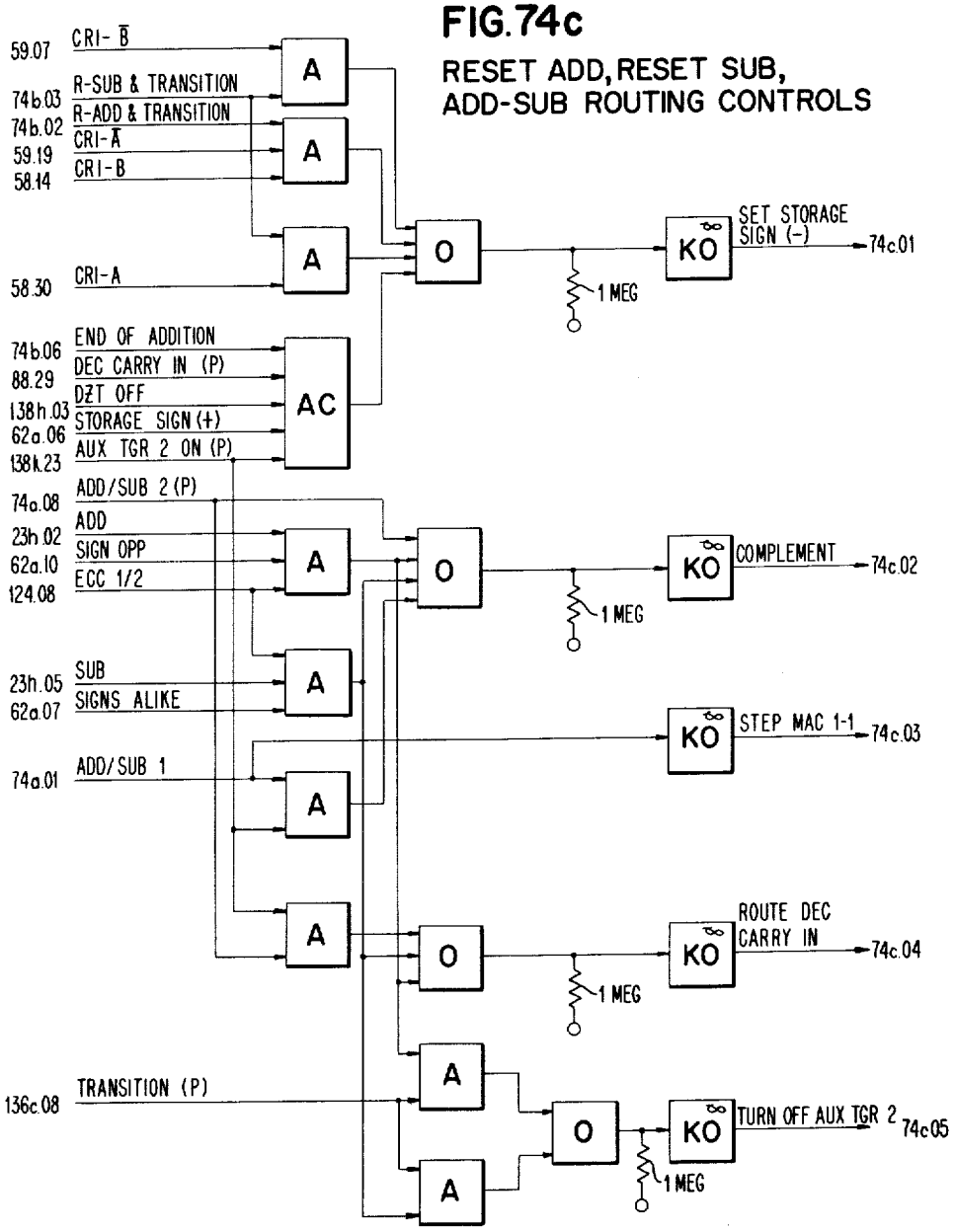


FIG. 74c

RESET ADD, RESET SUB, ADD-SUB ROUTING CONTROLS



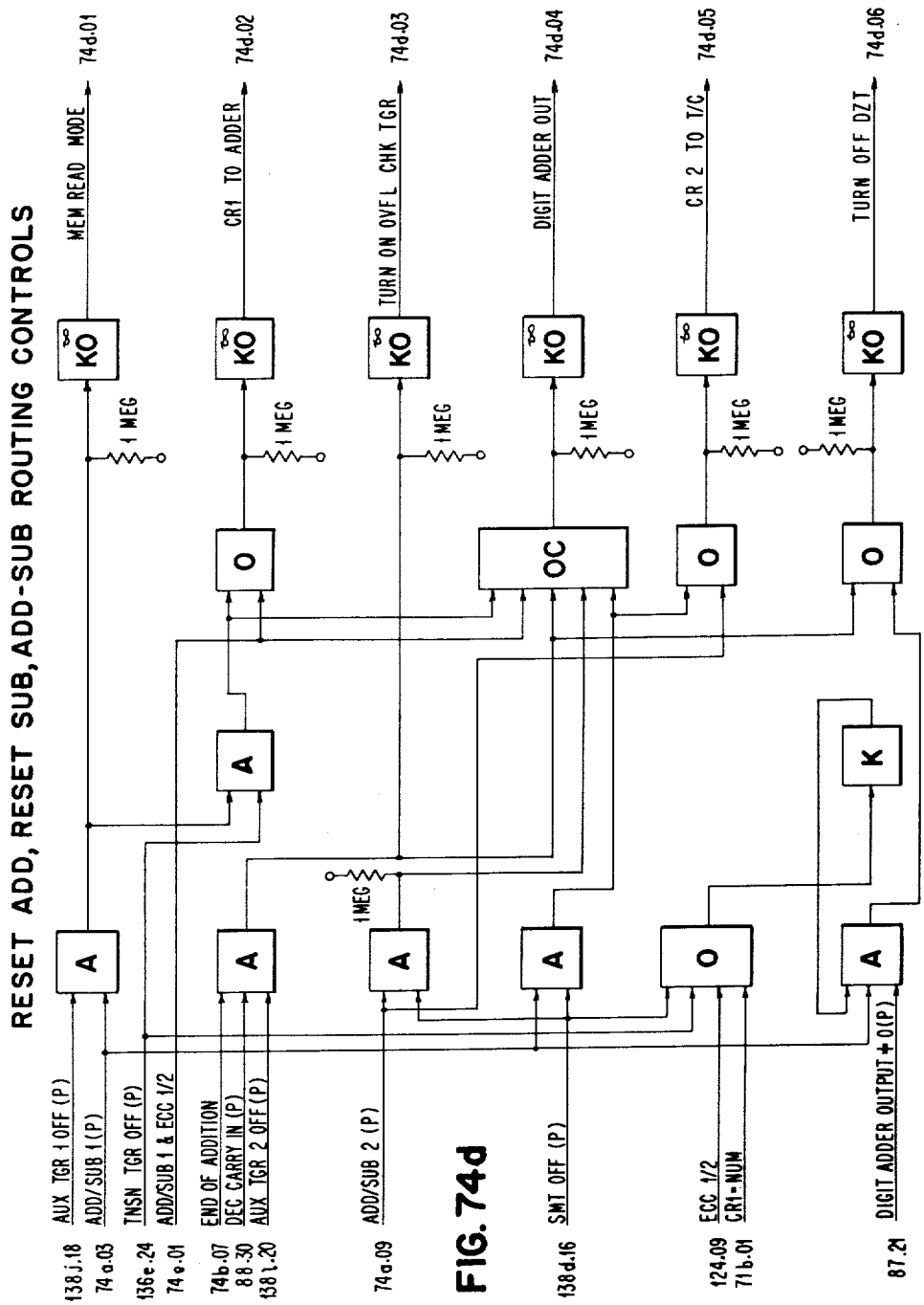
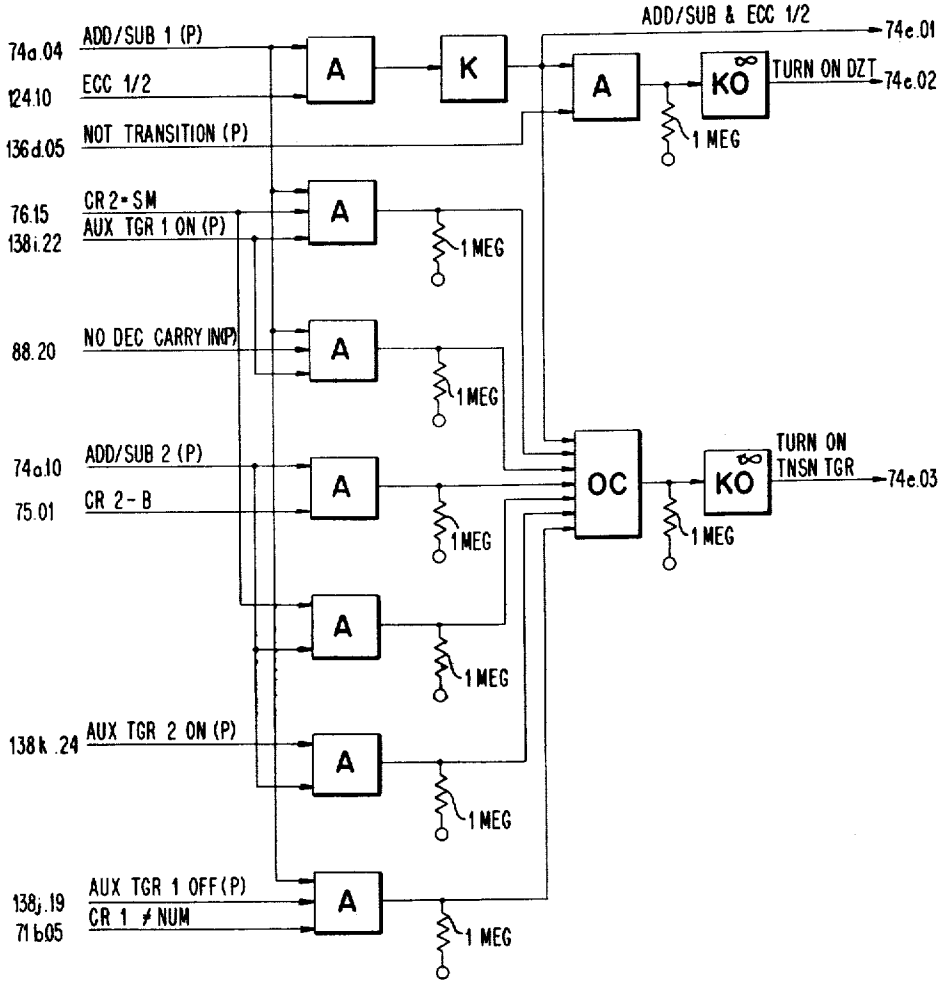

RESET ADD, RESET SUB, ADD-SUB ROUTING CONTROLS
MEM READ MODE
74d.01
CR1 TO ADDER
74d.02
TURN ON OVFL CHK TGR
74d.03
DIGIT ADDER OUT
74d.04
CR 2 TO T/C
74d.05
TURN OFF DZI
74d.06
KO
1 MEG
O
OC
A
K
AUX TGR 1 OFF (P)
138j.18
ADD/SUB 1 (P)
74a.03
TNSN TGR OFF (P)
136e.24
ADD/SUB 1 & ECC 1/2
74a.01
END OF ADDITION
74b.07
DEC CARRY IN (P)
88.30
AUX TGR 2 OFF (P)
138i.20
ADD/SUB 2 (P)
74a.09
SMT OFF (P)
138d.16
ECC 1/2
124.09
CR1-NUM
71b.01
DIGIT ADDER OUTPUT + O(P)
87.21

FIG. 74d

FIG. 74e

RESET ADD, RESET SUB, ADD-SUB ROUTING CONTROLS



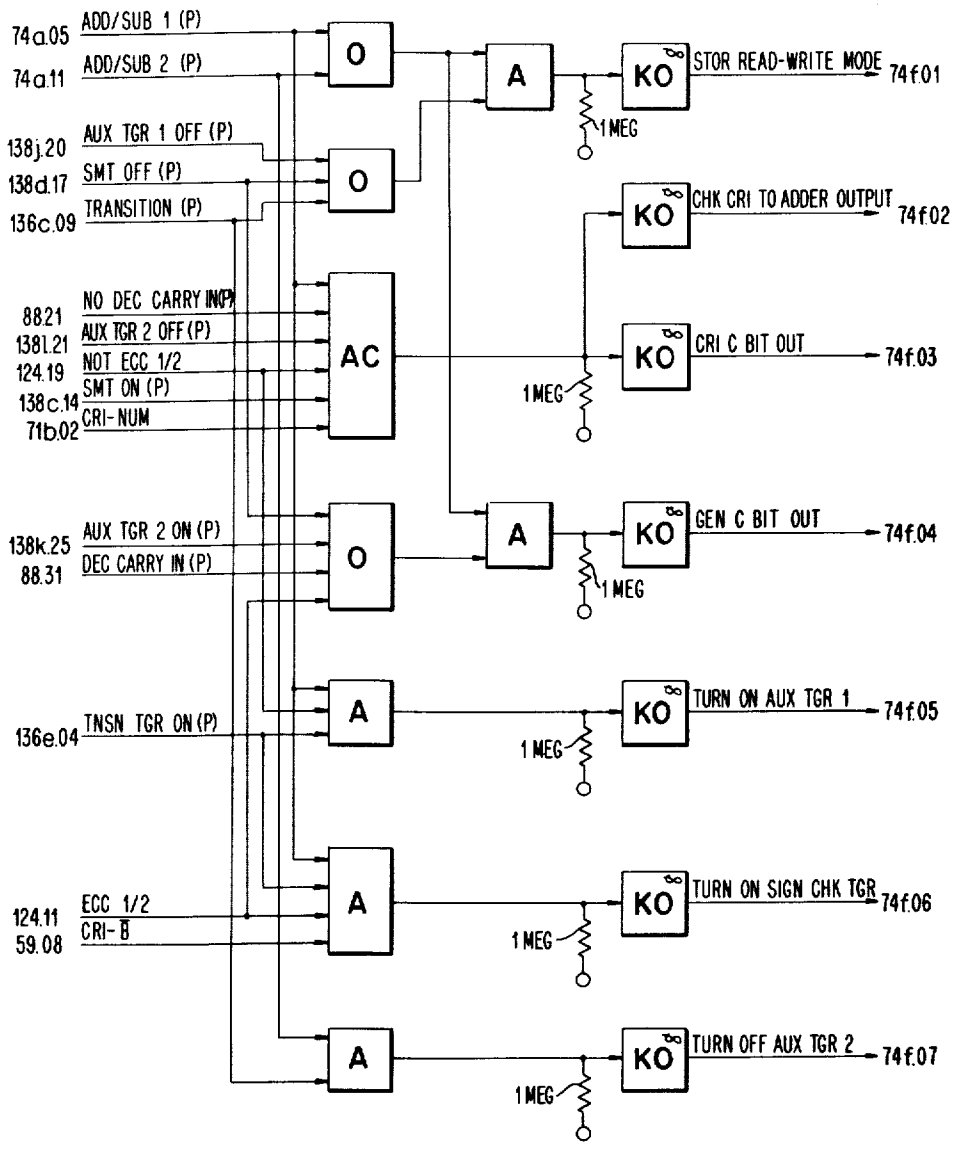
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FIG. 74f

RESET ADD, RESET SUB, ADD-SUB ROUTING CONTROLS



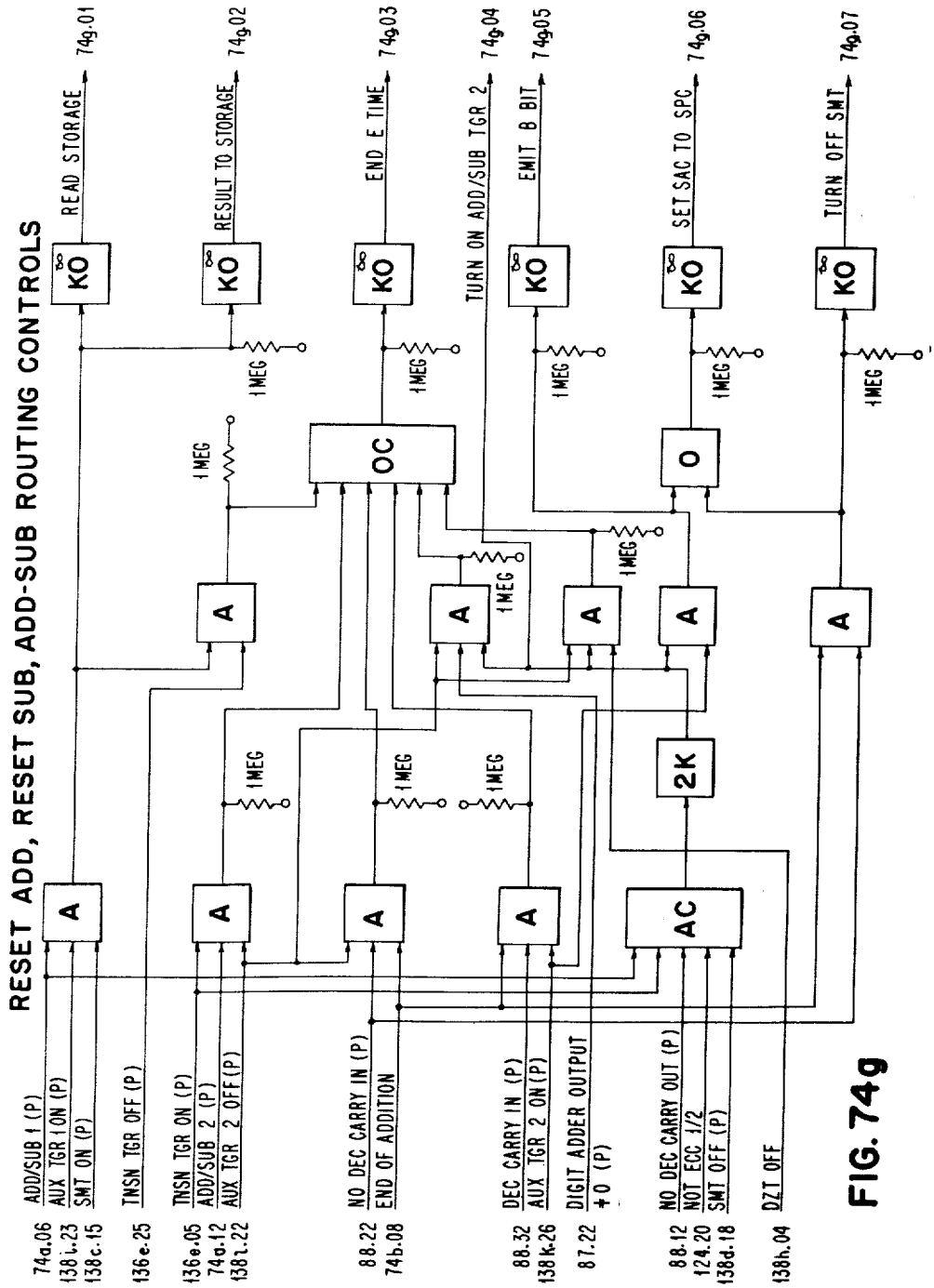
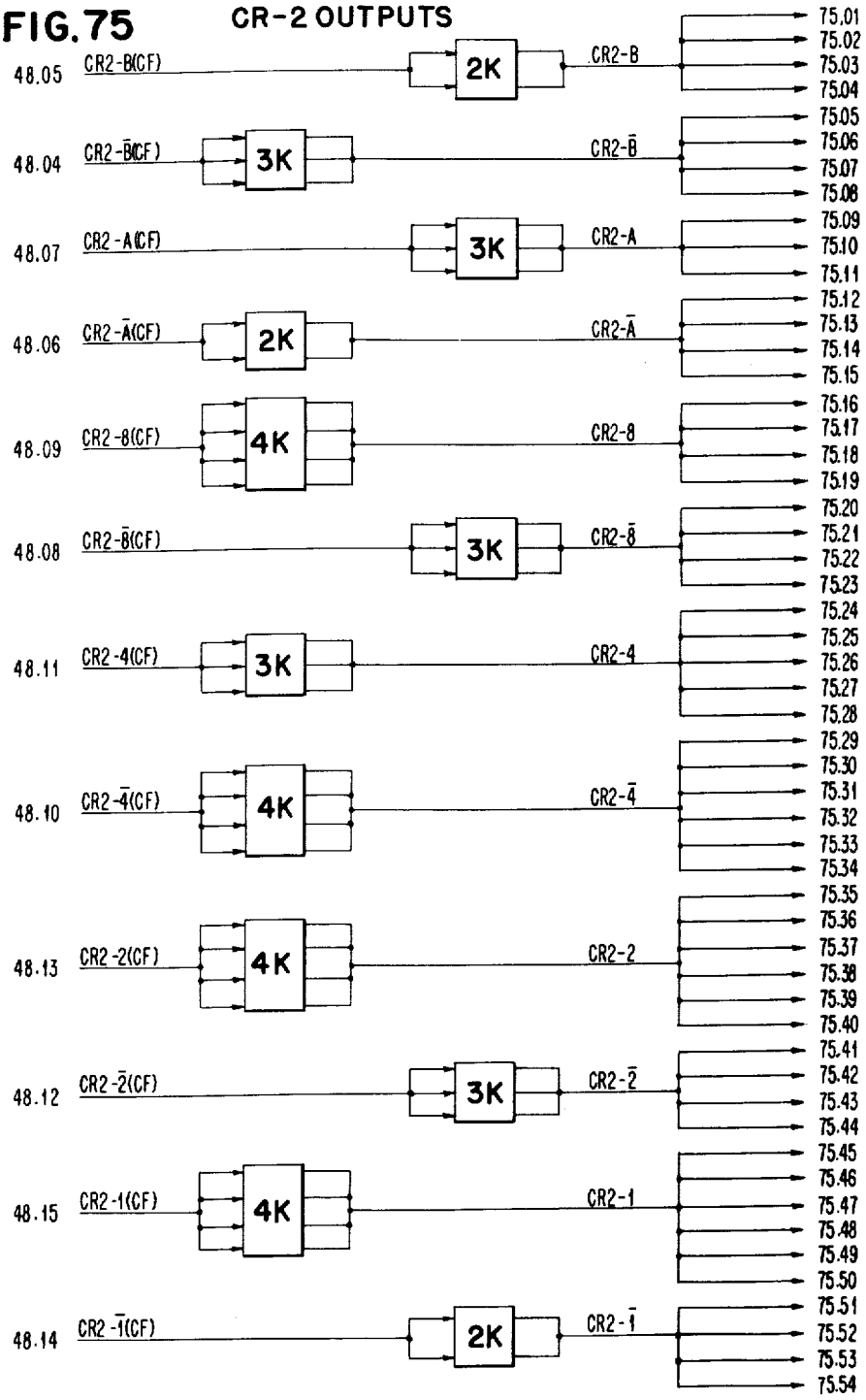

RESET ADD, RESET SUB, ADD-SUB ROUTING CONTROLS
READ STORAGE 74g.01
RESULT TO STORAGE 74g.02
END E TIME 74g.03
TURN ON ADD/SUB TGR 2 74g.04
EMIT B BIT 74g.05
SET SAC TO SPC 74g.06
TURN OFF SWT 74g.07
KO
1MEG
OC
O
A
AC
2K
ADD/SUB 1 (P) 74a.06
AUX TGR 1 ON (P) 138i.23
SWT ON (P) 138c.15
TNSN TGR OFF (P) 136e.25
TNSN TGR ON (P) 136e.05
ADD/SUB 2 (P) 74a.12
AUX TGR 2 OFF (P) 138i.22
NO DEC CARRY IN (P) 88.22
END OF ADDITION 74b.08
DEC CARRY IN (P) 88.32
AUX TGR 2 ON (P) 138k.26
DIGIT ADDER OUTPUT +0 (P) 87.22
NO DEC CARRY OUT (P) 88.12
NOT ECC 1/2 124.20
SWT OFF (P) 138d.18
DZT OFF 138h.04

FIG. 74g

FIG. 75


CR-2 OUTPUTS
48.05
CR2-B(CF)
2K
CR2-B
75.01
75.02
75.03
75.04
48.04
CR2-B̄(CF)
3K
CR2-B̄
75.05
75.06
75.07
75.08
48.07
CR2-A(CF)
3K
CR2-A
75.09
75.10
75.11
48.06
CR2-Ā(CF)
2K
CR2-Ā
75.12
75.13
75.14
75.15
48.09
CR2-8(CF)
4K
CR2-8
75.16
75.17
75.18
75.19
48.08
CR2-8̄(CF)
3K
CR2-8̄
75.20
75.21
75.22
75.23
48.11
CR2-4(CF)
3K
CR2-4
75.24
75.25
75.26
75.27
75.28
48.10
CR2-4̄(CF)
4K
CR2-4̄
75.29
75.30
75.31
75.32
75.33
75.34
48.13
CR2-2(CF)
4K
CR2-2
75.35
75.36
75.37
75.38
75.39
75.40
48.12
CR2-2̄(CF)
3K
CR2-2̄
75.41
75.42
75.43
75.44
48.15
CR2-1(CF)
4K
CR2-1
75.45
75.46
75.47
75.48
75.49
75.50
48.14
CR2-1̄(CF)
2K
CR2-1̄
75.51
75.52
75.53
75.54

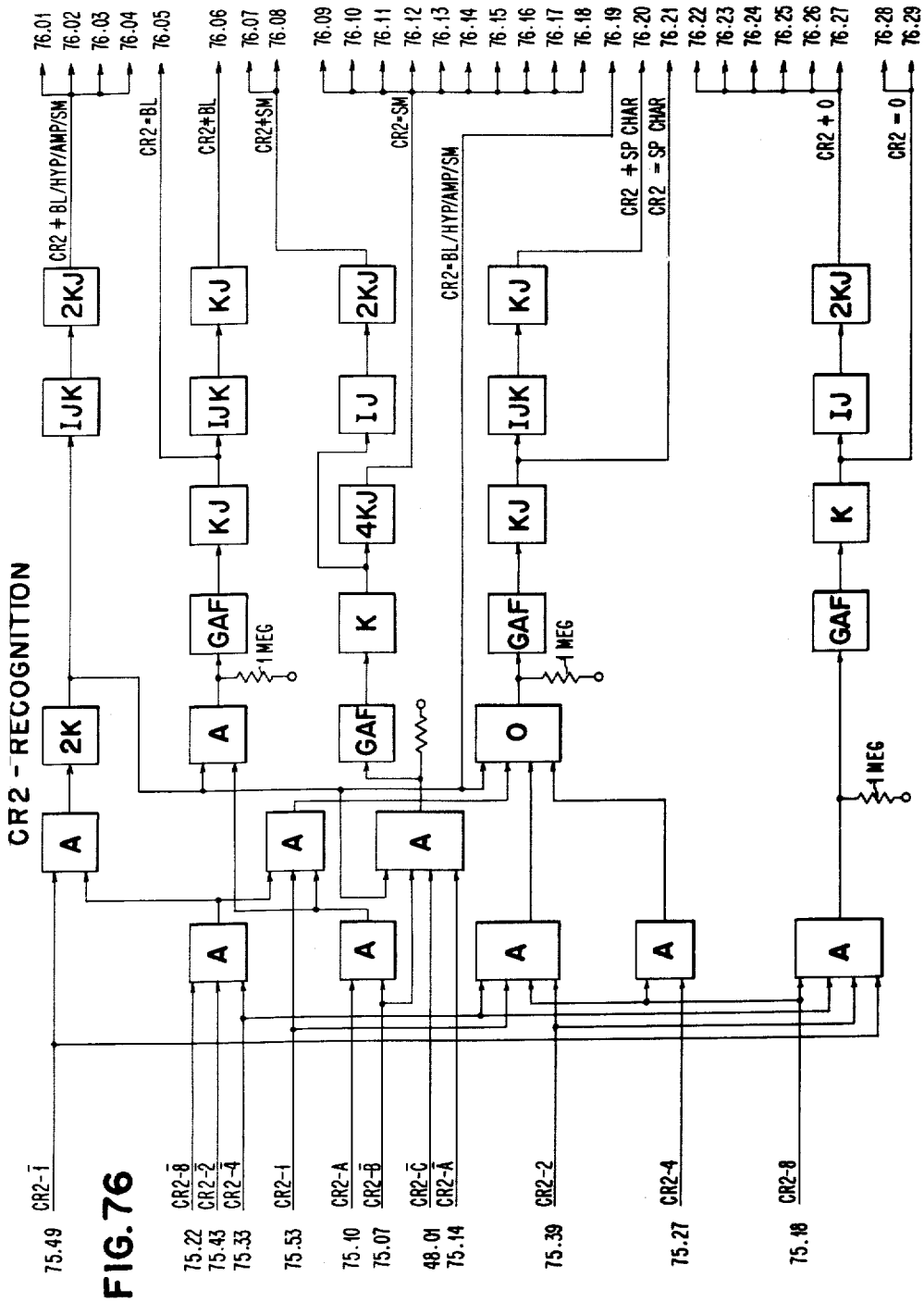

CR2 - RECOGNITION
76.01
76.02
76.03
76.04
76.05
76.06
76.07
76.08
76.09
76.10
76.11
76.12
76.13
76.14
76.15
76.16
76.17
76.18
76.19
76.20
76.21
76.22
76.23
76.24
76.25
76.26
76.27
76.28
76.29
CR2 + BL/HYP/AMP/SM
CR2 + BL
CR2 + BL
CR2 + SM
CR2 - SM
CR2 - BL/HYP/AMP/SM
CR2 + SP CHAR
CR2 - SP CHAR
CR2 + 0
CR2 - 0
2KJ
IJK
KJ
IJK
2KJ
IJ
KJ
IJK
2KJ
IJ
K
4KJ
KJ
GAF
K
GAF
2K
A
GAF
O
GAF
1 MEG
1 MEG
1 MEG
A
A
A
A
A
A
A
A
A
A
CR2-1
CR2-2
CR2-4
CR2-8
CR2-A
CR2-B
CR2-C
CR2-A
CR2-1
CR2-2
CR2-4
CR2-8
75.49
75.22
75.43
75.33
75.53
75.10
75.07
48.01
75.14
75.39
75.27
75.18

FIG. 76

FIG. 77

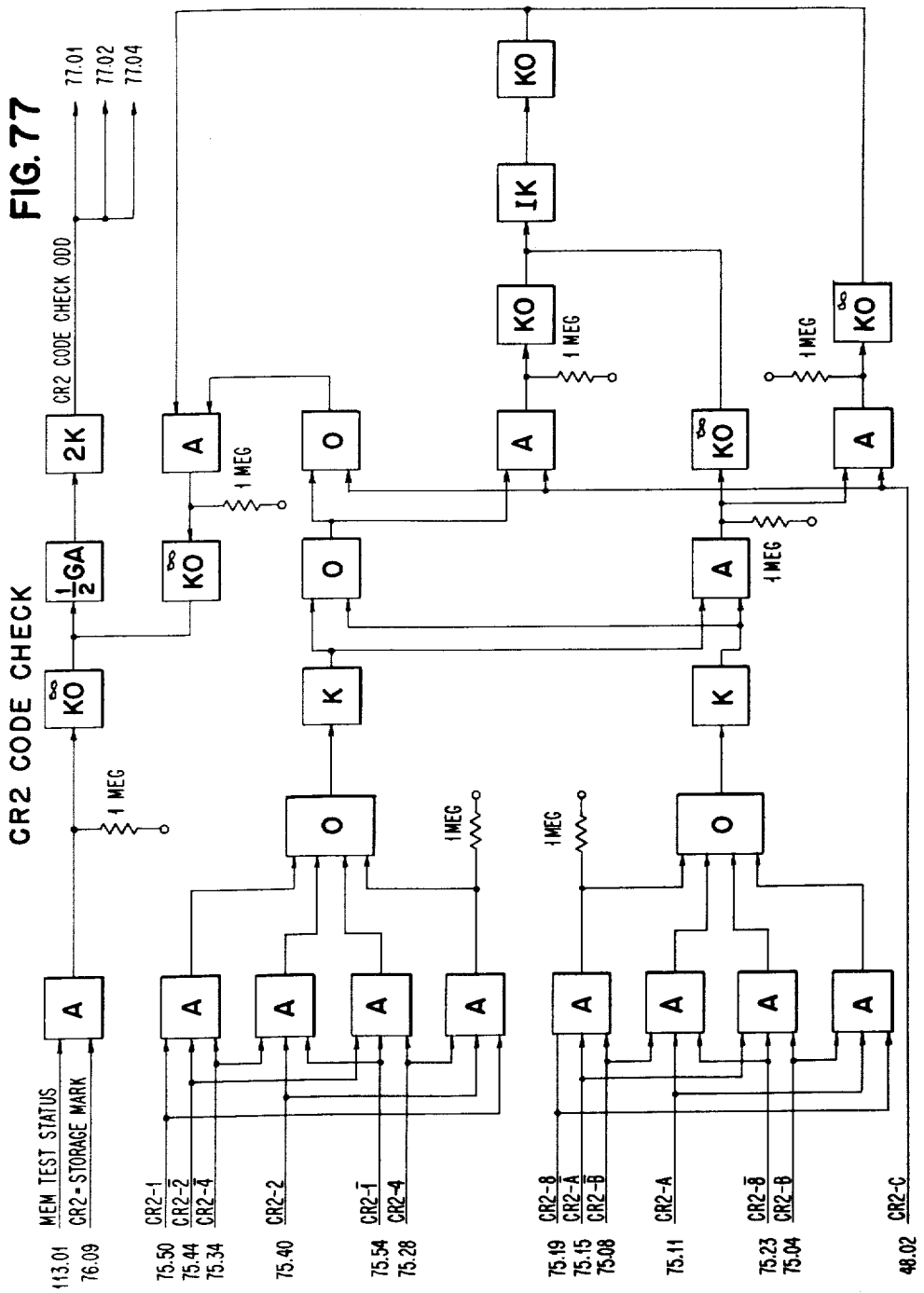

CR2 CODE CHECK
CR2 CODE CHECK ODD
77.01
77.02
77.04
2K
1/2GA
KO
A
O
K
IK
1 MEG
MEM TEST STATUS
CR2-STORAGE MARK
113.01
76.09
CR2-1
CR2-2̄
CR2-4̄
CR2-2
CR2-1̄
CR2-4
CR2-8
CR2-A
CR2-B̄
CR2-A
CR2-8̄
CR2-B
CR2-C
75.50
75.44
75.34
75.40
75.54
75.28
75.19
75.15
75.08
75.11
75.23
75.04
48.02

FIG. 78

MULTIPLE REGISTER & DECODER

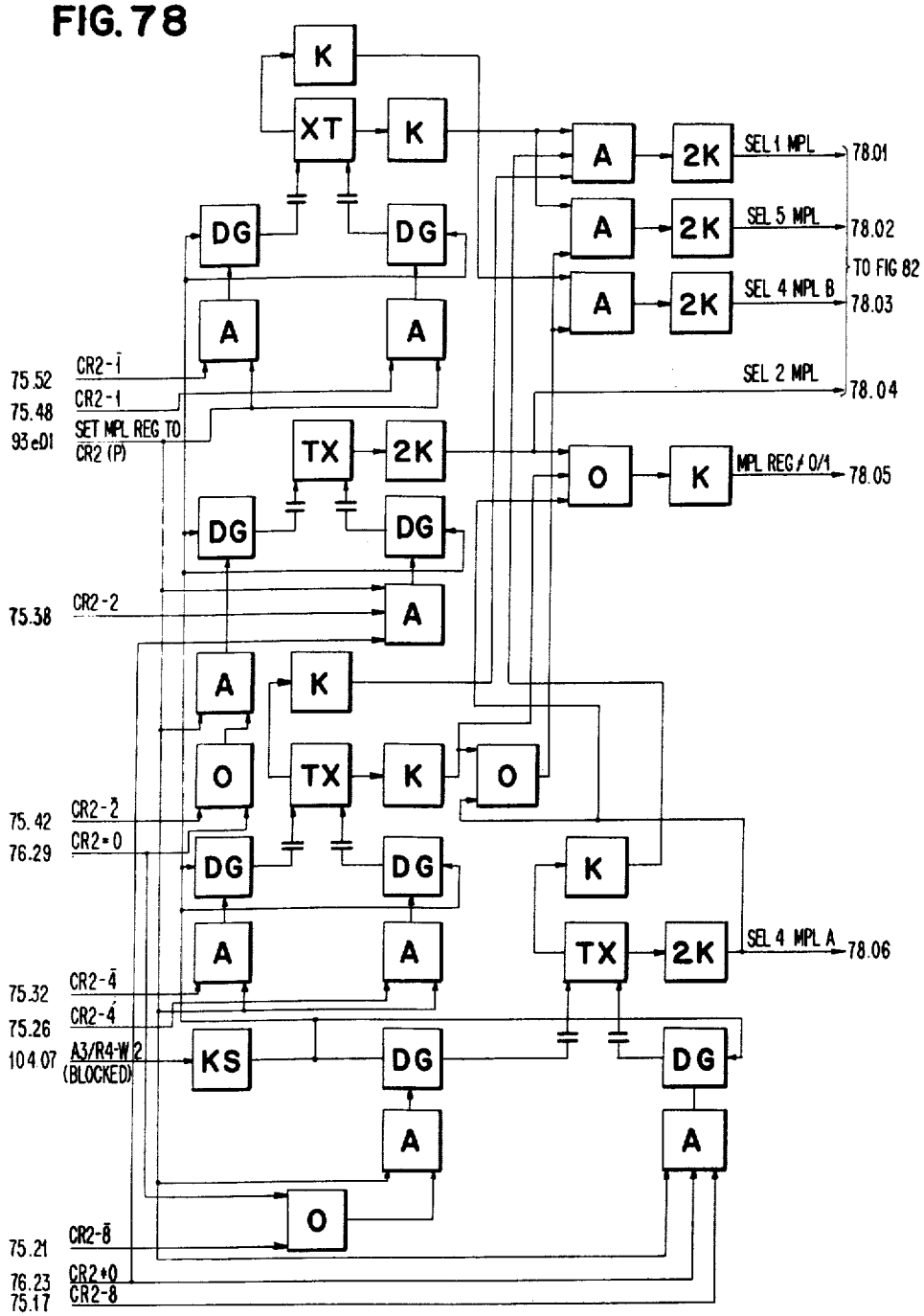
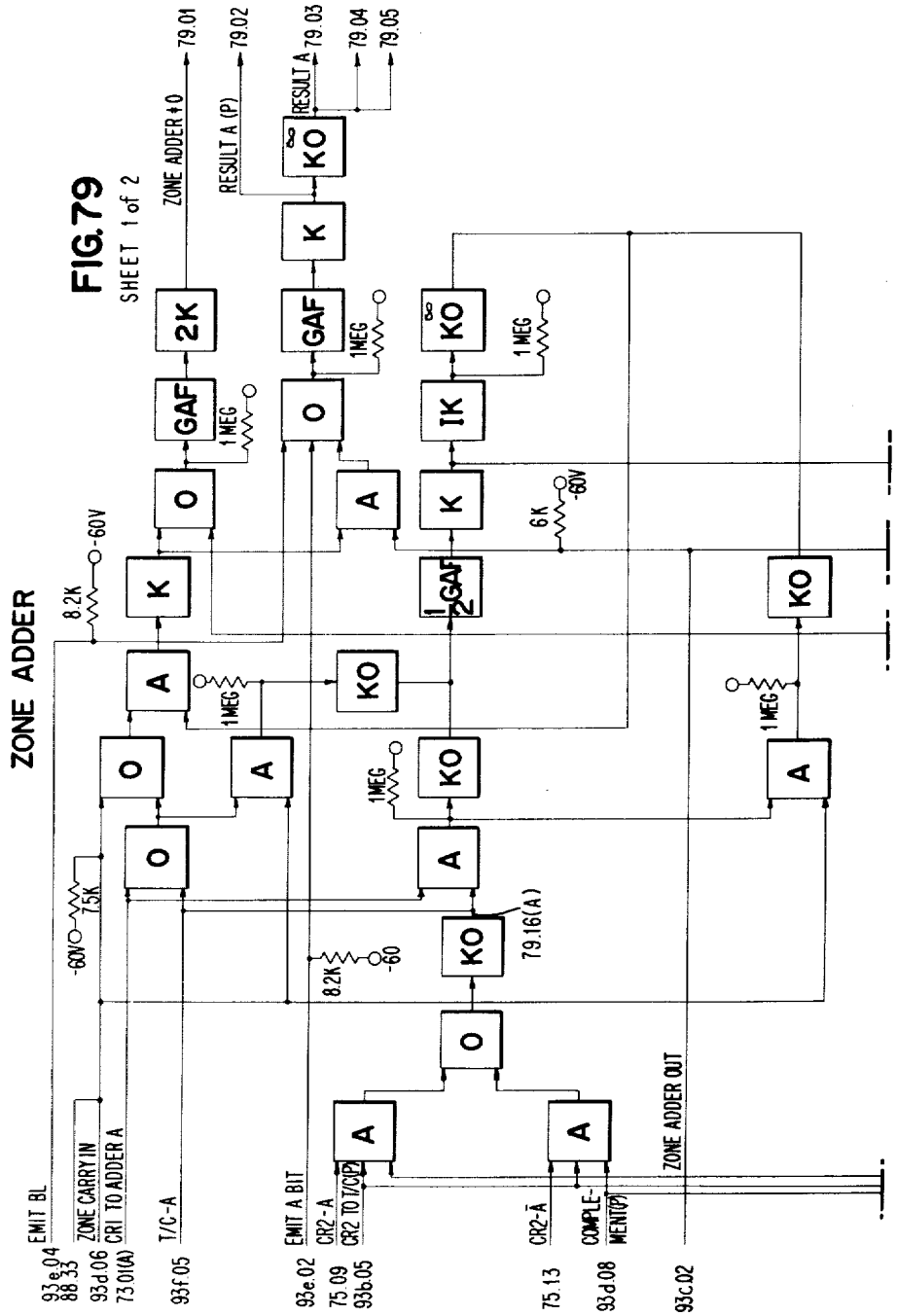


FIG. 79
SHEET 1 of 2



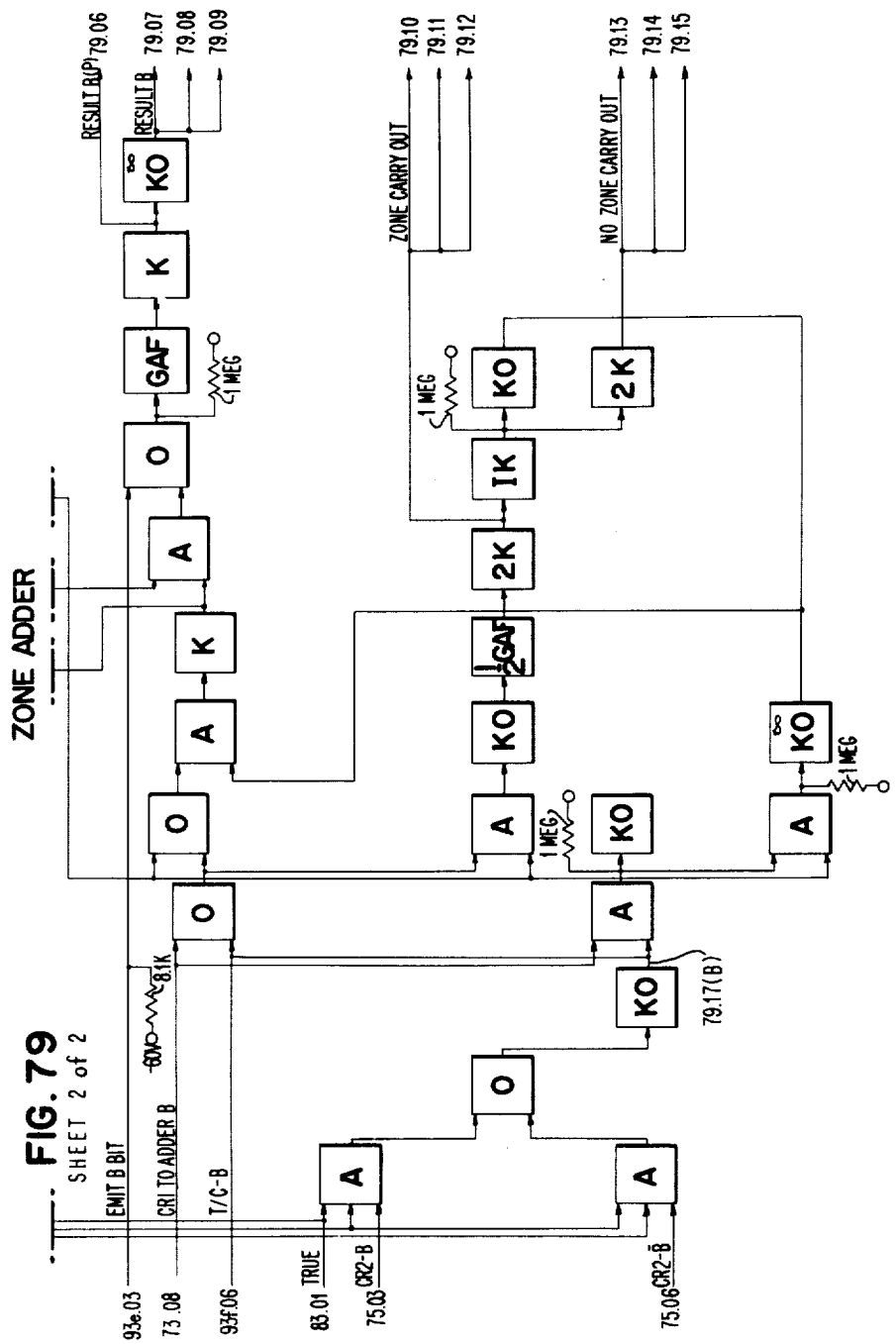


FIG. 79. SHEET 2 of 2

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FIG.80

SHEET 1 of 2

MULTIPLICAND DOUBLER & QUADRUPLER

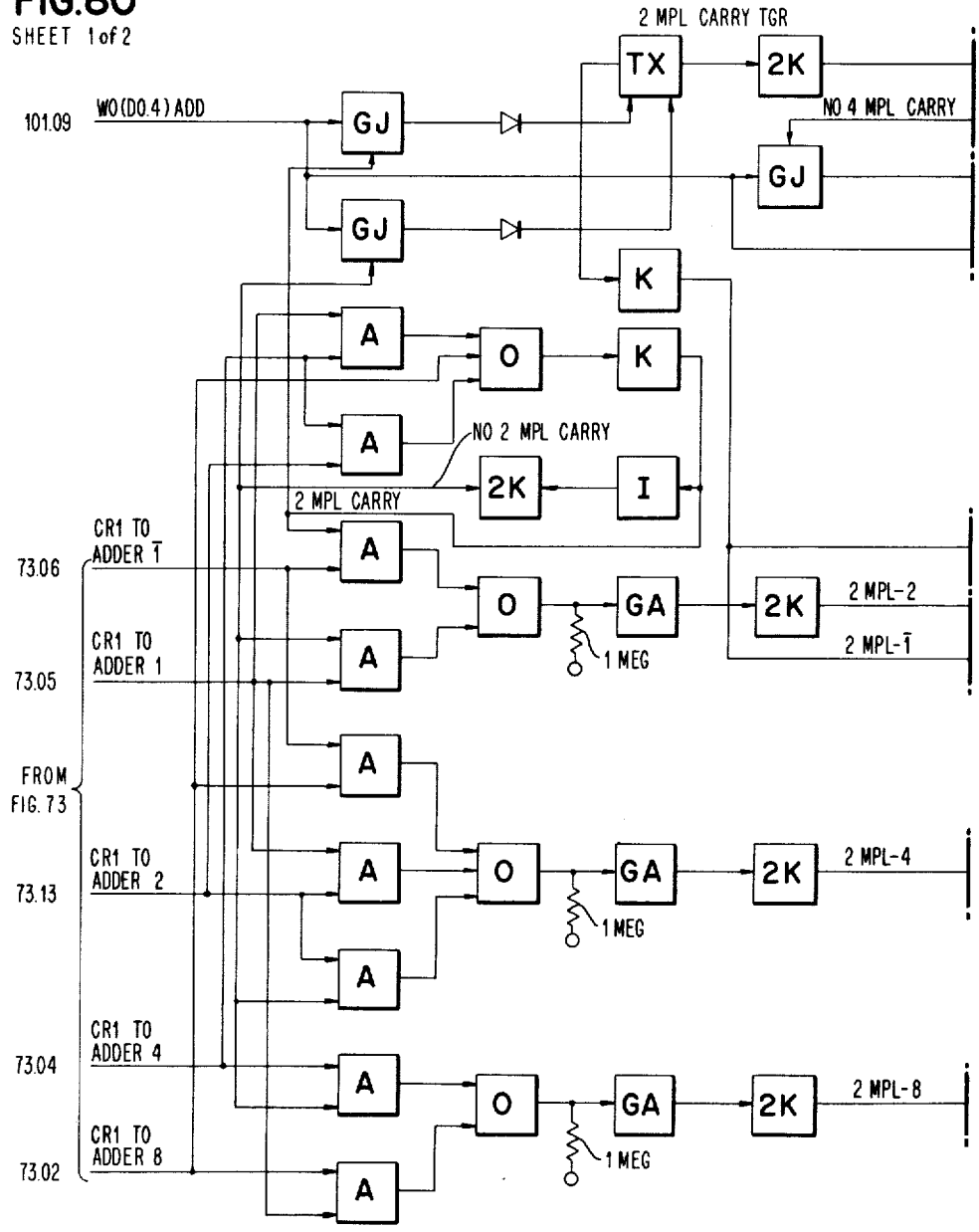
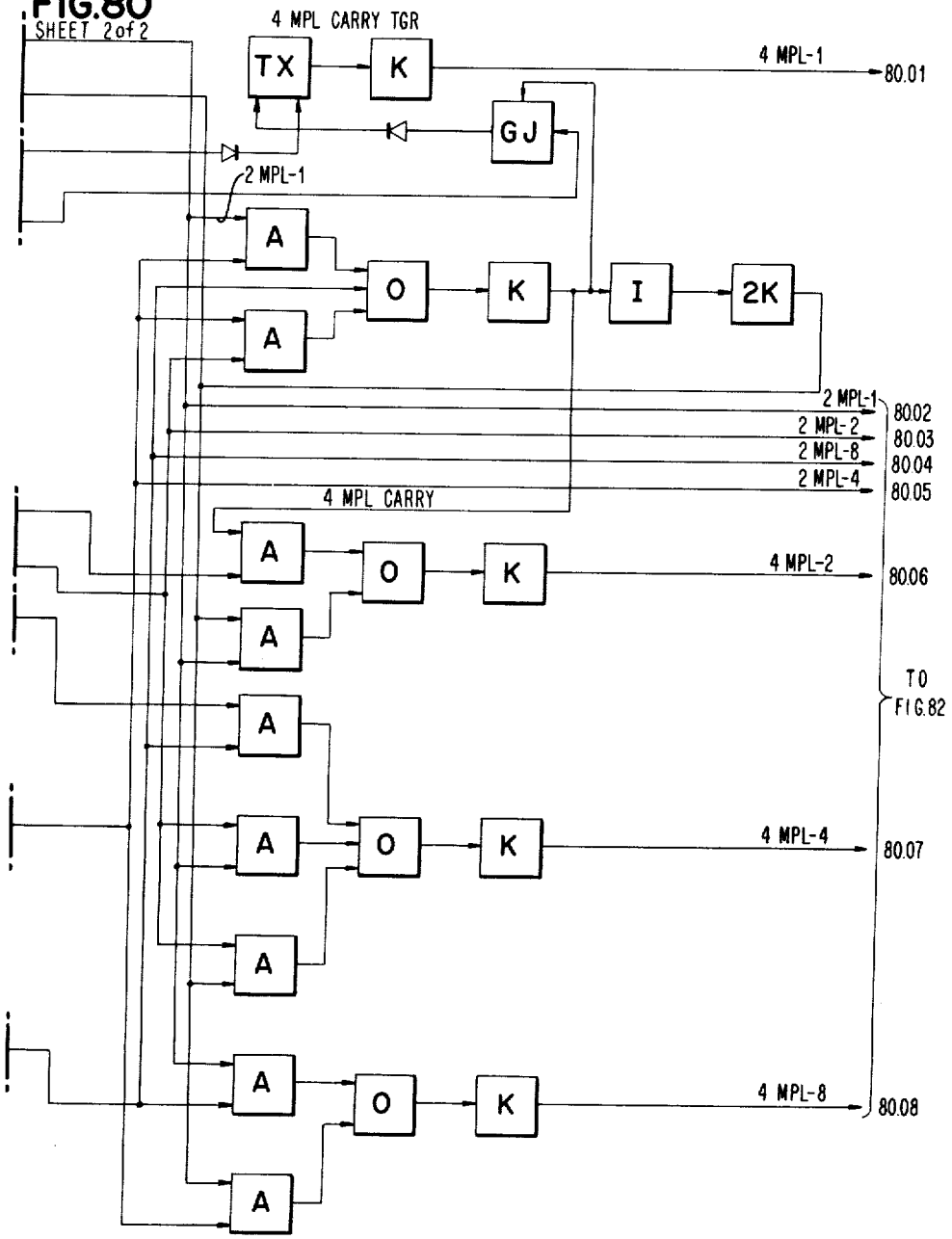


FIG.80 MULTIPLICAND DOUBLER & QUADRUPLER
SHEET 2 of 2



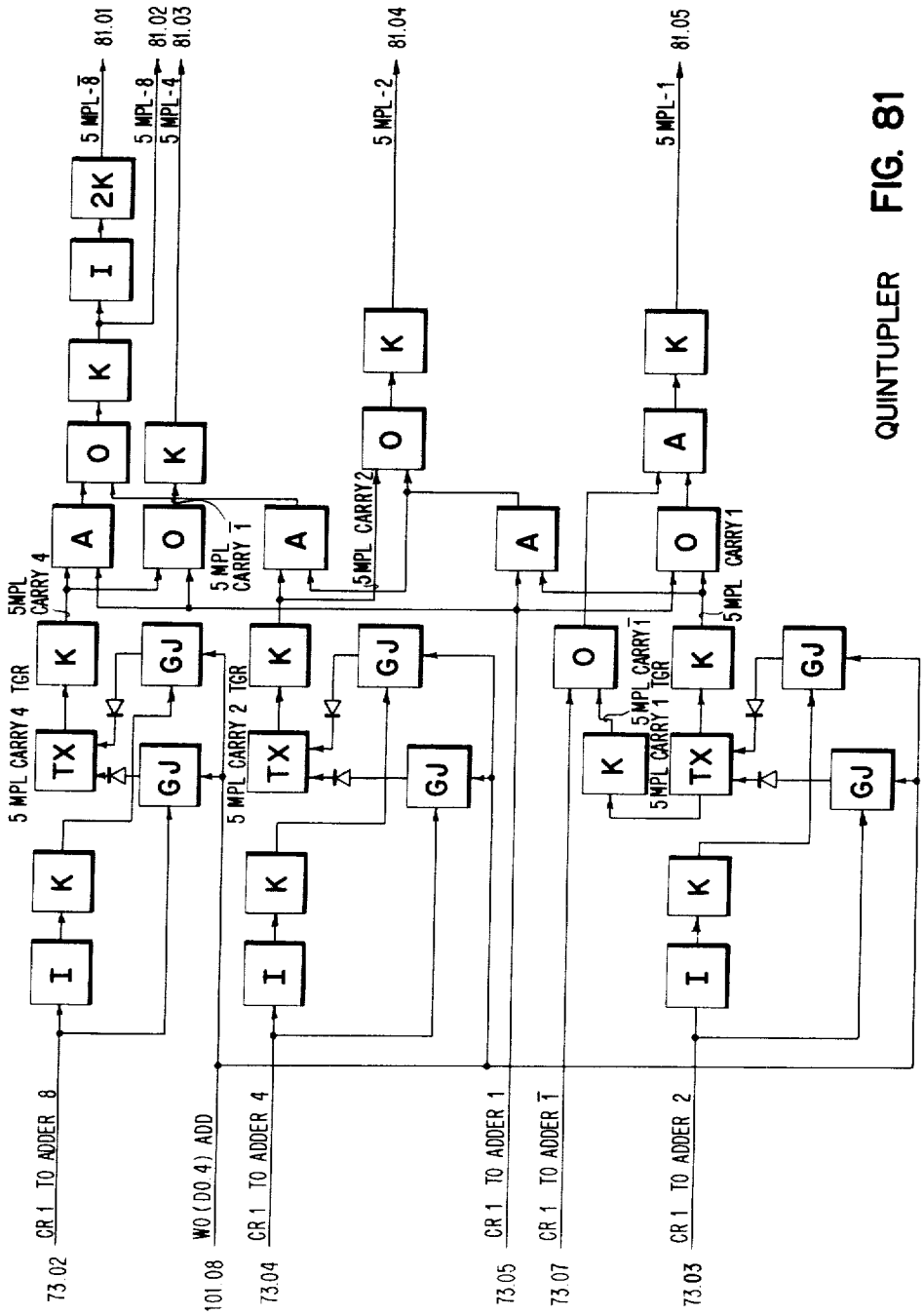


FIG. 81
QUINTUPLER

FIG. 82

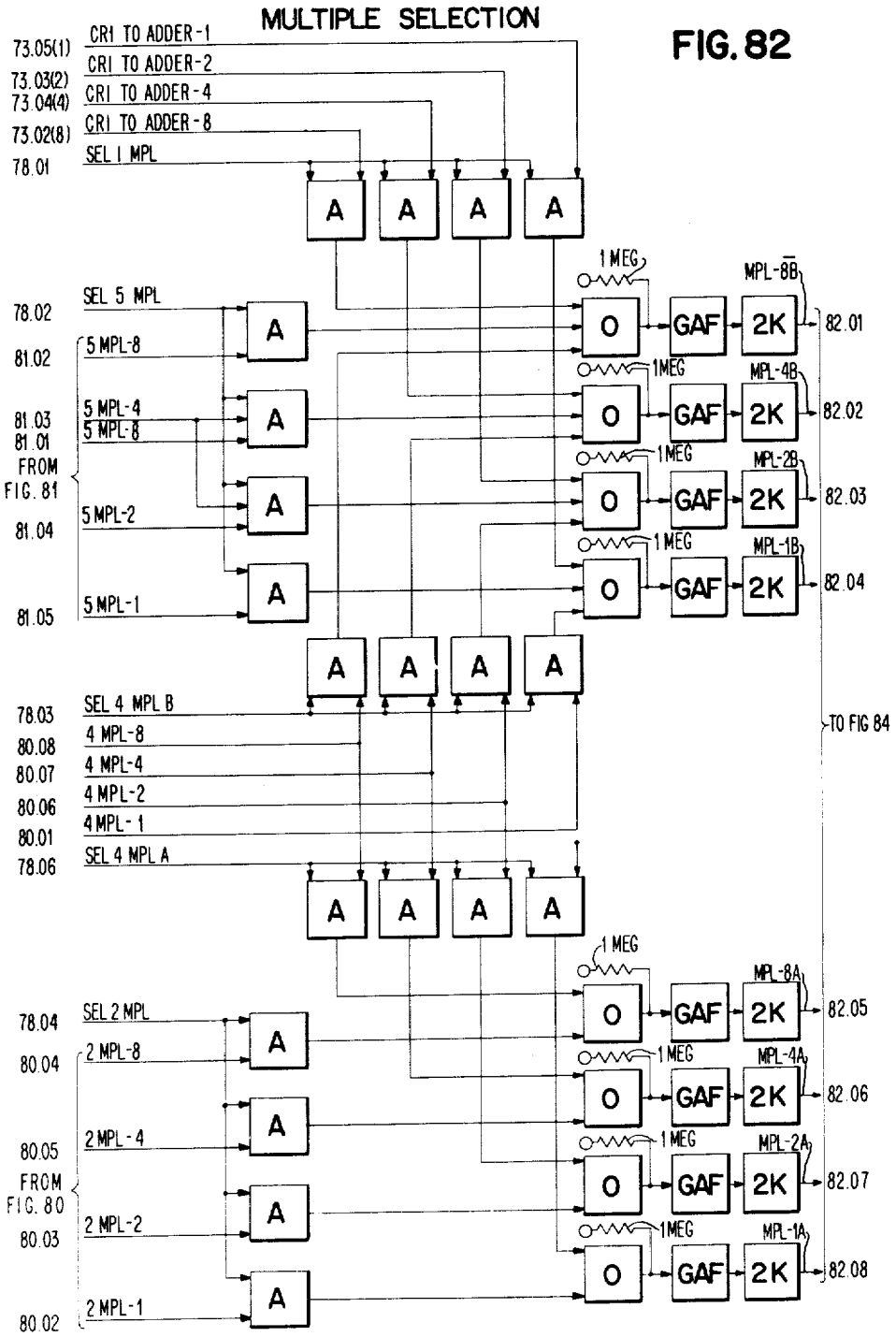
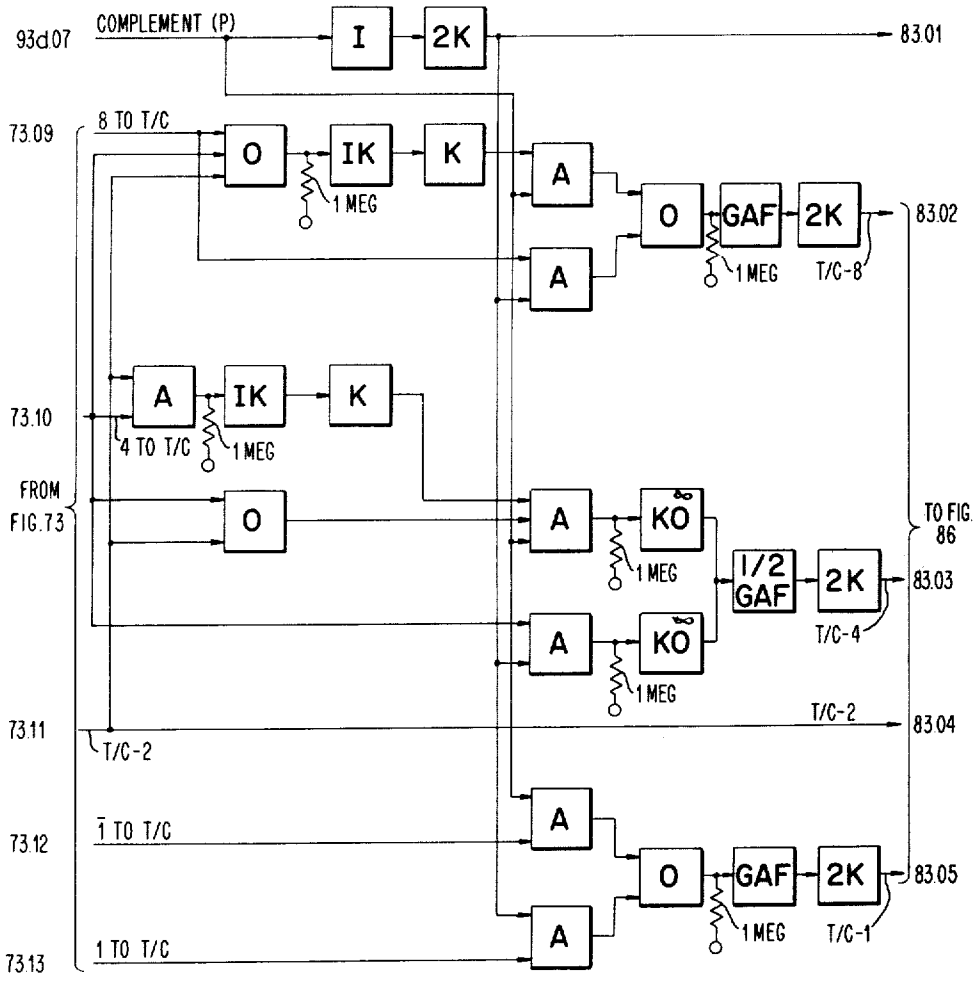

MULTIPLE SELECTION
73.05(1) CRI TO ADDER-1
73.03(2) CRI TO ADDER-2
73.04(4) CRI TO ADDER-4
73.02(8) CRI TO ADDER-8
78.01 SEL 1 MPL
A A A A
78.02 SEL 5 MPL
81.02 5 MPL-8
81.03 5 MPL-4
81.01 5 MPL-8
FROM FIG. 81
81.04 5 MPL-2
81.05 5 MPL-1
A A A A
78.03 SEL 4 MPL B
80.08 4 MPL-8
80.07 4 MPL-4
80.06 4 MPL-2
80.01 4 MPL-1
78.06 SEL 4 MPL A
A A A A
78.04 SEL 2 MPL
80.04 2 MPL-8
80.05 2 MPL-4
FROM FIG. 80
80.03 2 MPL-2
80.02 2 MPL-1
A
1 MEG
O
GAF
2K
MPL-8B
MPL-4B
MPL-2B
MPL-1B
MPL-8A
MPL-4A
MPL-2A
MPL-1A
82.01
82.02
82.03
82.04
82.05
82.06
82.07
82.08
TO FIG 84

FIG. 83

TRUE/COMP CONTROL



MULTIPLE ADDER FIG. 84

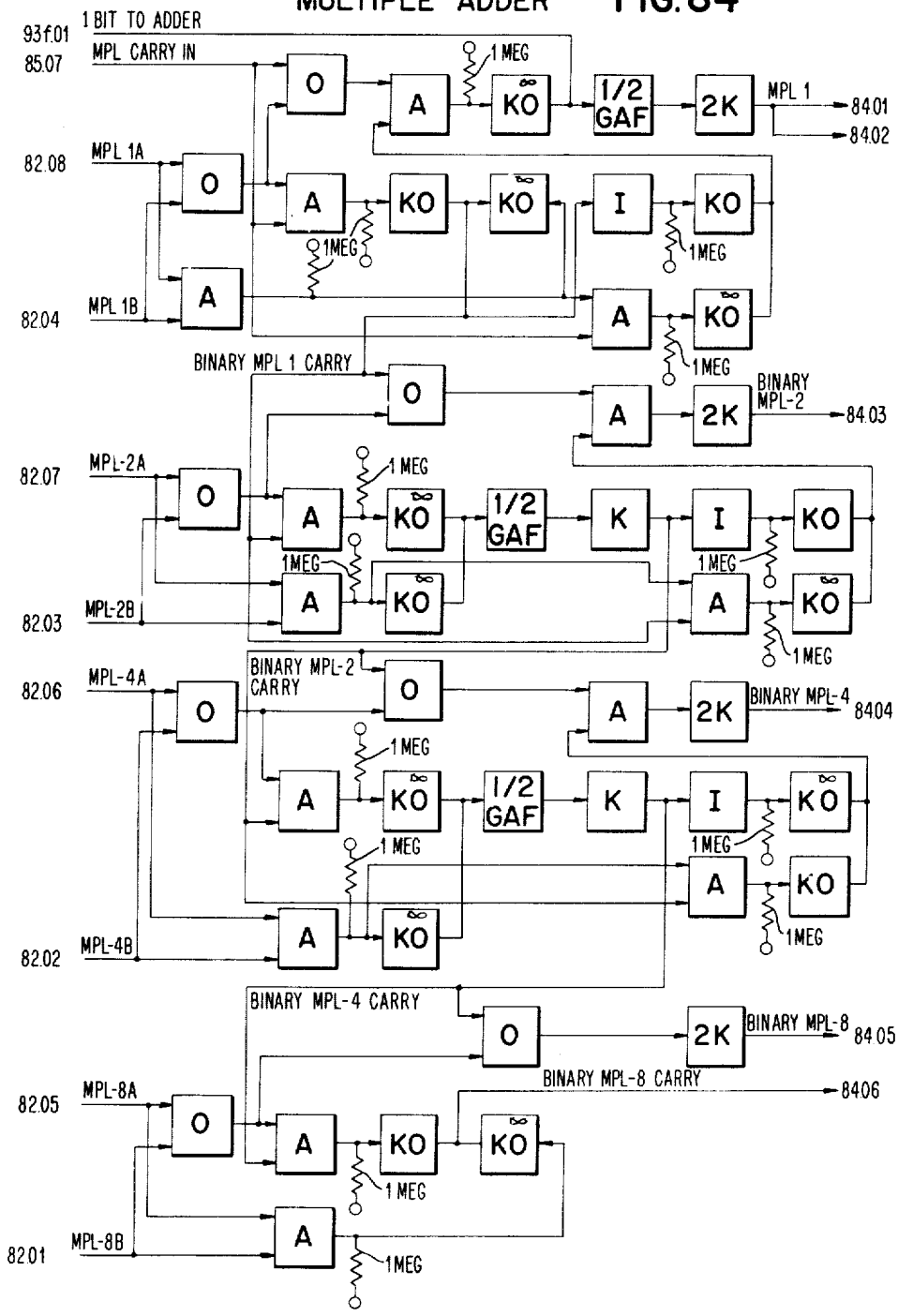


FIG. 85 DECIMAL CORRECTION CKTS

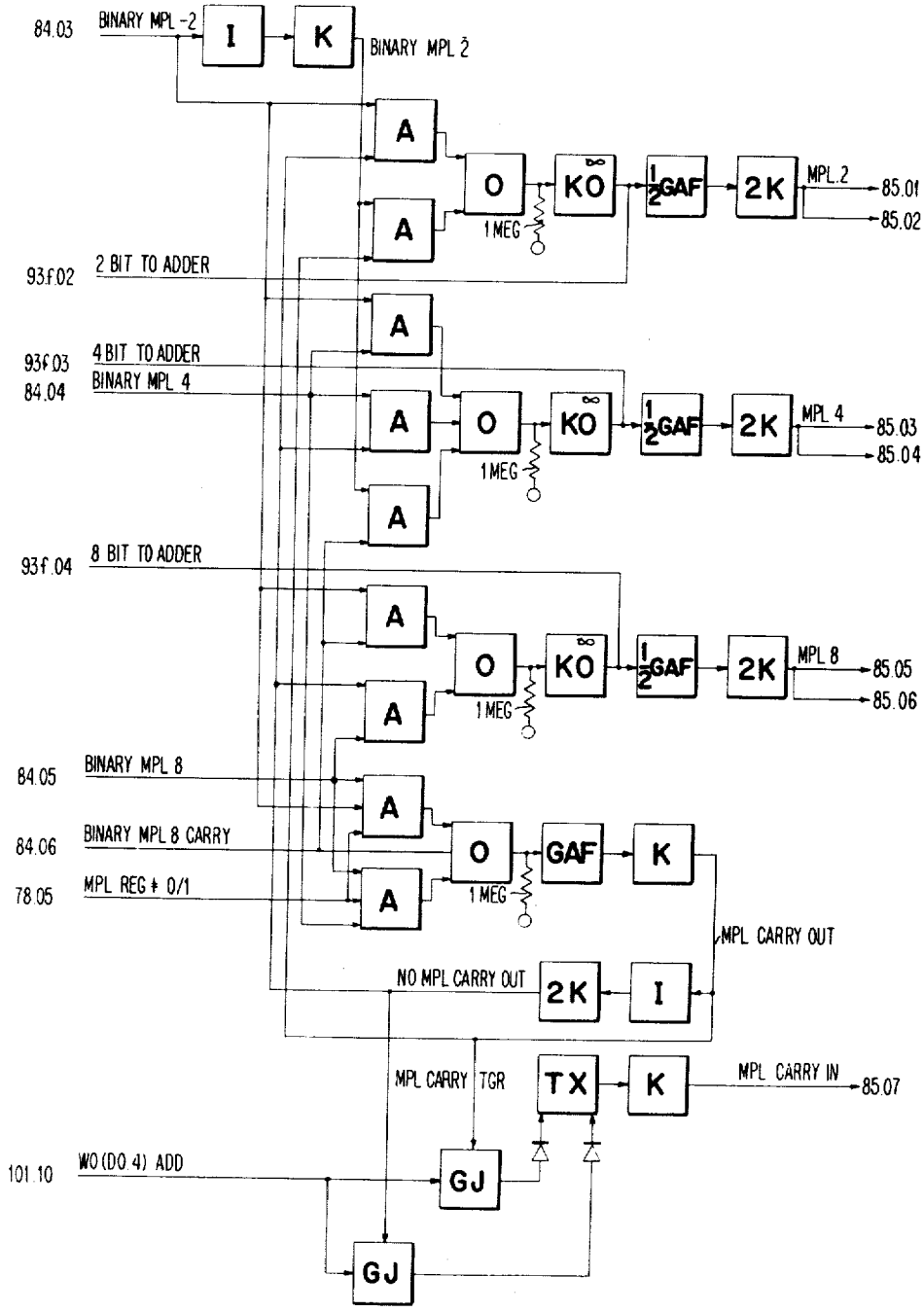
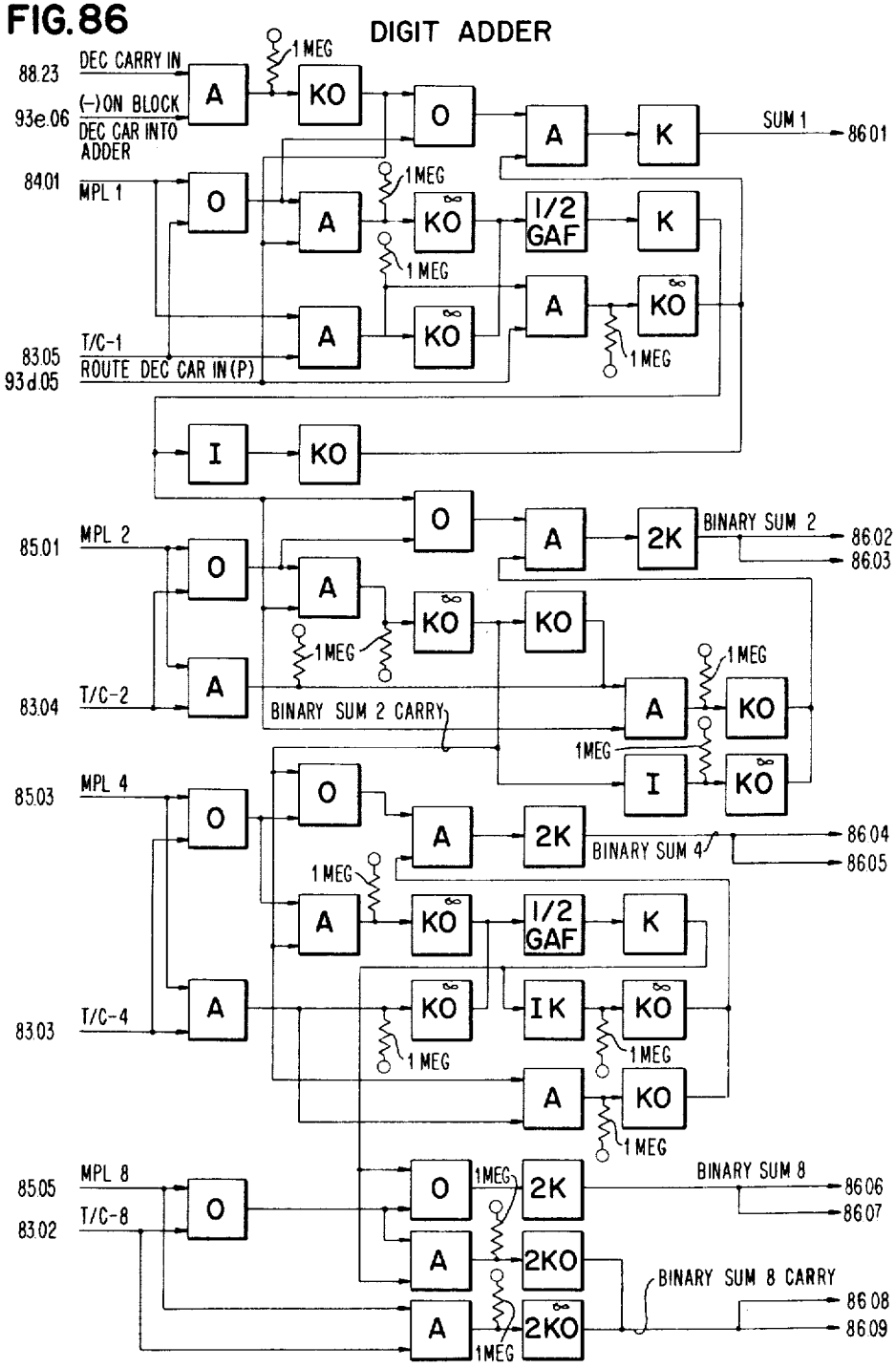


FIG. 86


DIGIT ADDER
88.23
DEC CARRY IN
93e.06
(-)ON BLOCK
DEC CAR INTO ADDER
1 MEG
A
KO
O
A
K
SUM 1
8601
8401
MPL 1
O
A
KO
1/2 GAF
K
A
KO
T/C-1
83.05
93d.05
ROUTE DEC CAR IN(P)
I
KO
85.01
MPL 2
BINARY SUM 2
2K
8602
8603
T/C-2
83.04
BINARY SUM 2 CARRY
85.03
MPL 4
BINARY SUM 4
8604
8605
T/C-4
83.03
IK
85.05
MPL 8
83.02
T/C-8
BINARY SUM 8
8606
8607
2KO
BINARY SUM 8 CARRY
8608
8609

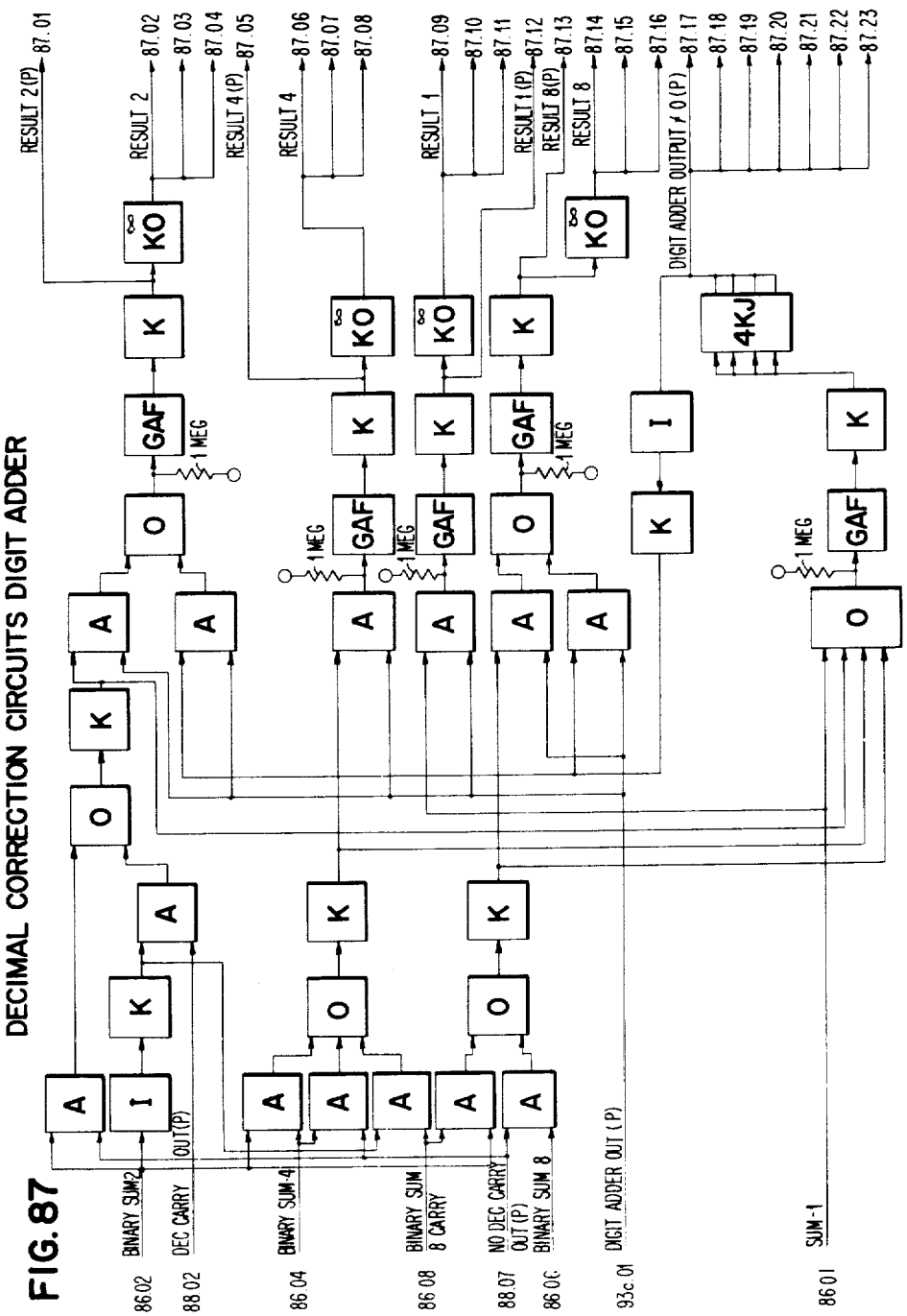
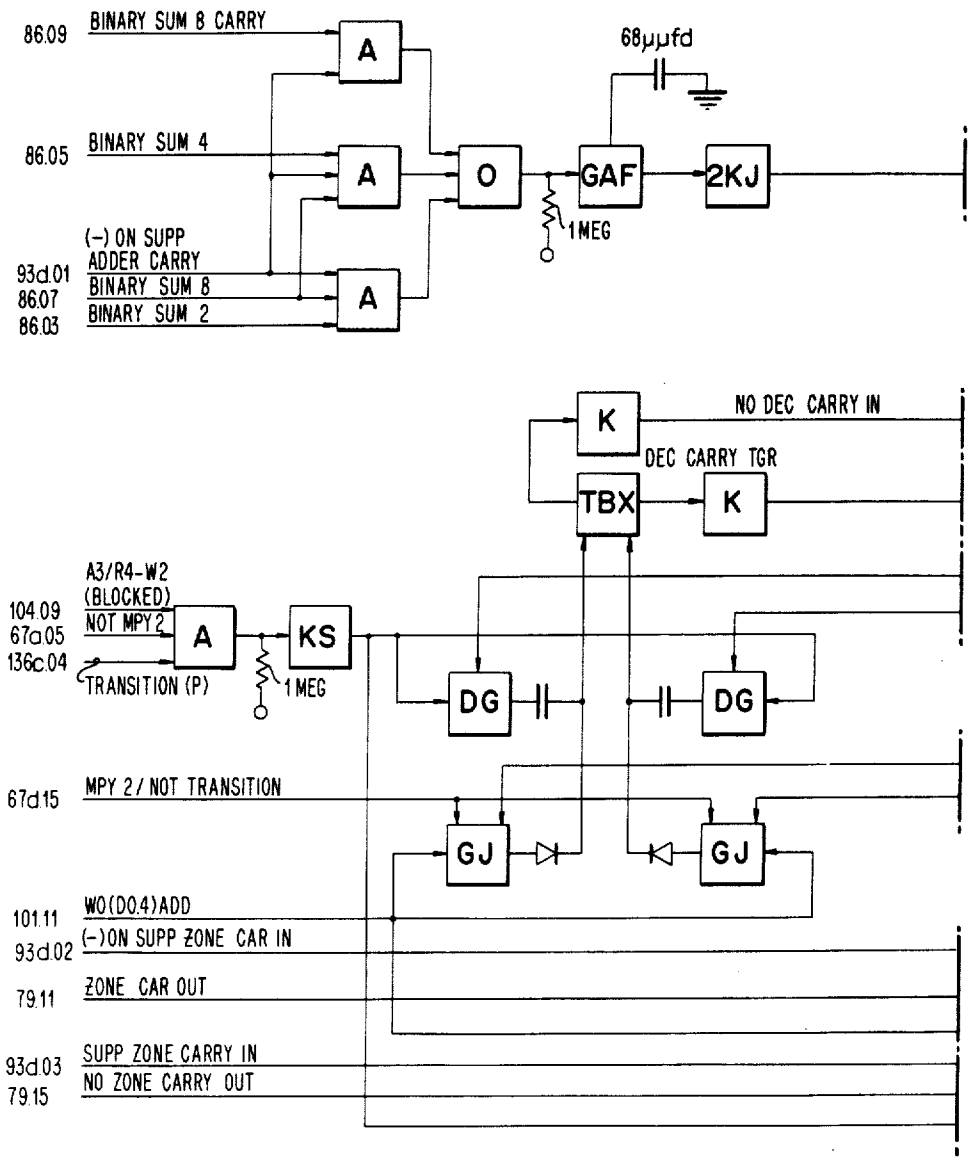

DECIMAL CORRECTION CIRCUITS DIGIT ADDER
RESULT 2(P) 87.01
RESULT 2 87.02
87.03
RESULT 4(P) 87.04
87.05
RESULT 4 87.06
87.07
87.08
RESULT 1 87.09
87.10
RESULT 1(P) 87.11
RESULT 8(P) 87.12
87.13
RESULT 8 87.14
87.15
DIGIT ADDER OUTPUT / O(P) 87.16
87.17
87.18
87.19
87.20
87.21
87.22
87.23
1 MEG
BINARY SUM 2
DEC CARRY OUT(P)
BINARY SUM 4
BINARY SUM 8 CARRY
NO DEC CARRY OUT(P)
BINARY SUM 8
DIGIT ADDER OUT (P)
SUM-1
86.02
88.02
86.04
86.08
88.07
86.0C
93c.01
86.01

FIG. 87

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FIG. 88
SHEET 1 of 2

DEC CARRY CIRCUITS & ZONE CARRY TGR



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FIG. 88
SHEET 2 of 2

DEC CARRY CIRCUITS & ZONE CARRY TGR

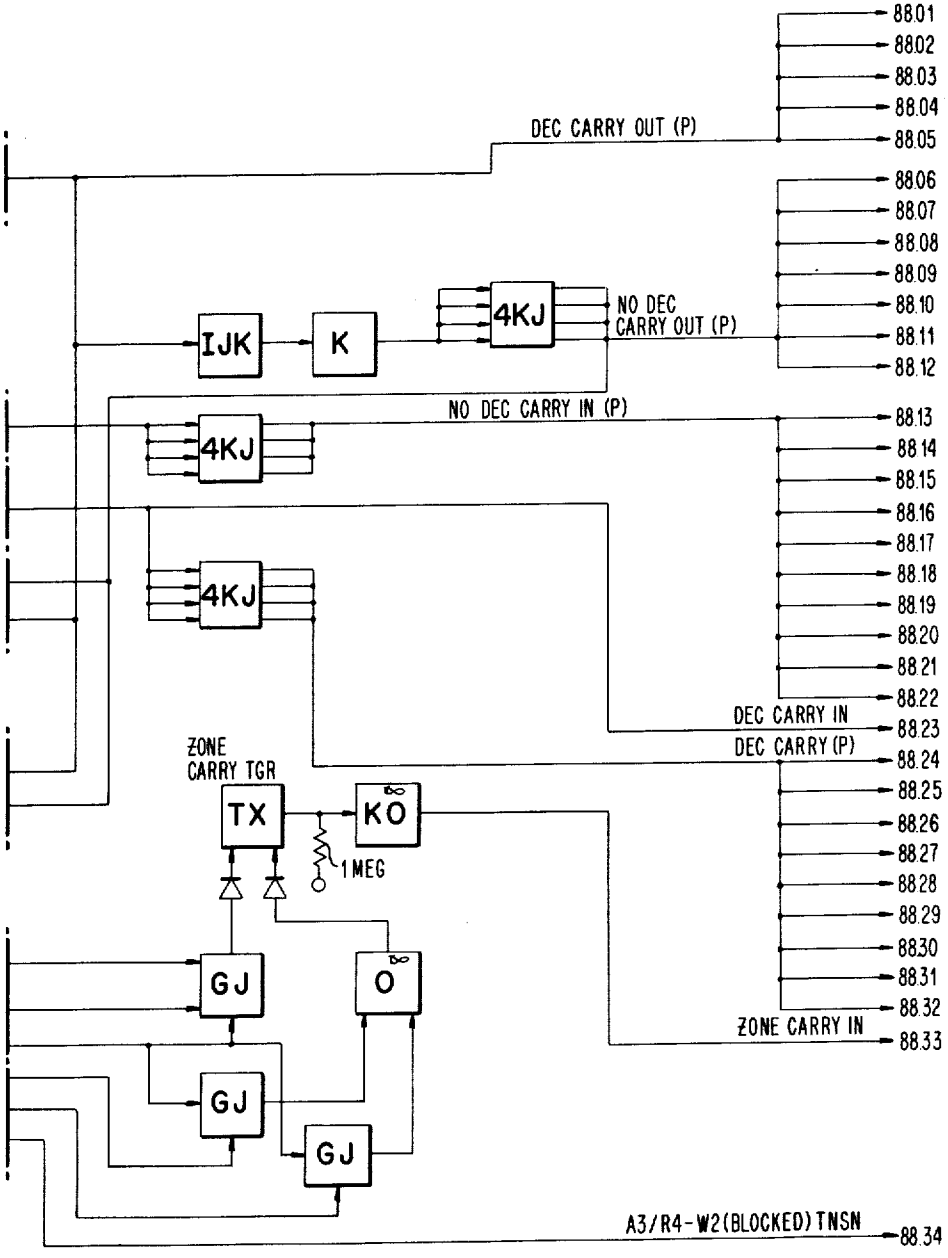


FIG. 89a

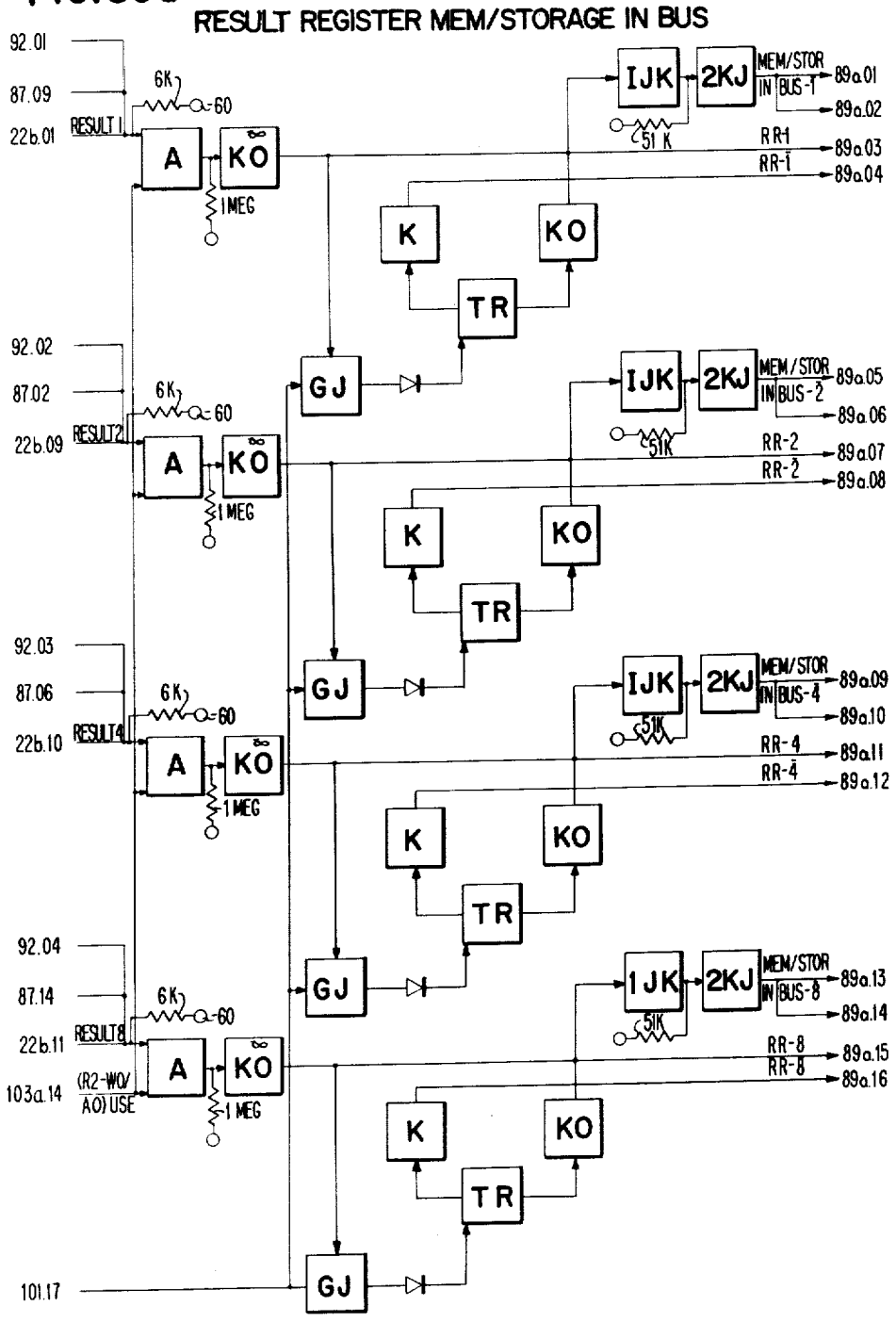

RESULT REGISTER MEM/STORAGE IN BUS
92.01
87.09
22b.01
RESULT 1
6K
60
A
KO
1 MEG
IJK
2KJ
51 K
MEM/STOR IN BUS-1
89a.01
89a.02
RR-1
RR-1
89a.03
89a.04
K
KO
TR
GJ
92.02
87.02
22b.09
RESULT2
IJK
2KJ
51K
MEM/STOR IN BUS-2
89a.05
89a.06
RR-2
RR-2
89a.07
89a.08
92.03
87.06
22b.10
RESULT4
IJK
2KJ
51K
MEM/STOR IN BUS-4
89a.09
89a.10
RR-4
RR-4
89a.11
89a.12
92.04
87.14
22b.11
RESULT8
103a.14
(R2-WO/ AO) USE
1JK
2KJ
51K
MEM/STOR IN BUS-8
89a.13
89a.14
RR-8
RR-8
89a.15
89a.16
101.17

FIG. 89b

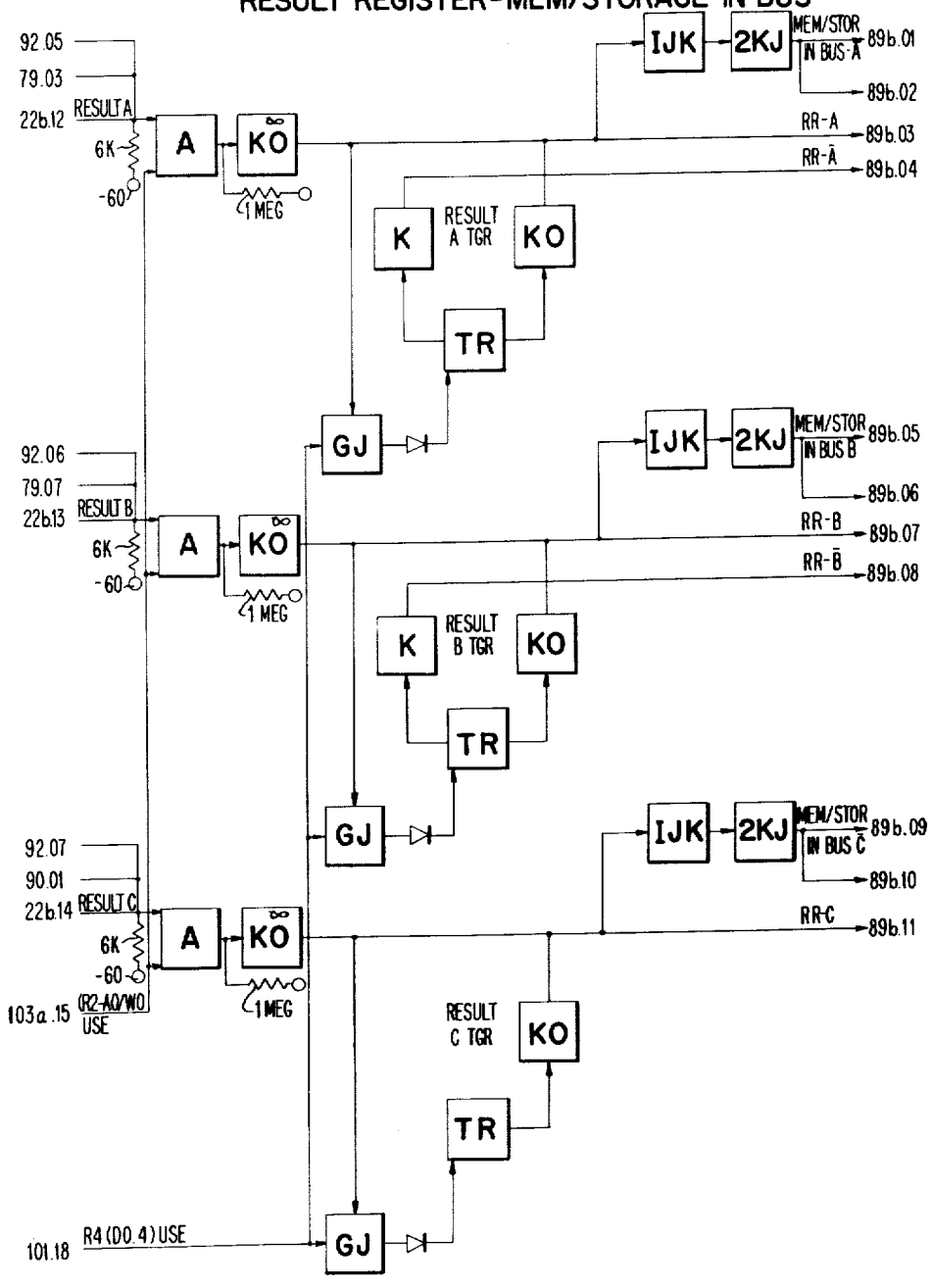

RESULT REGISTER-MEM/STORAGE IN BUS
92.05
79.03
22b.12
RESULT A
6K
-60
A
KO
1 MEG
IJK
2KJ
MEM/STOR IN BUS A
89b.01
89b.02
RR-A
89b.03
RR-Ā
89b.04
K
RESULT A TGR
KO
TR
GJ
92.06
79.07
22b.13
RESULT B
IJK
2KJ
MEM/STOR IN BUS B
89b.05
89b.06
RR-B
89b.07
RR-B̄
89b.08
RESULT B TGR
92.07
90.01
22b.14
RESULT C
IJK
2KJ
MEM/STOR IN BUS C
89b.09
89b.10
RR-C
89b.11
103a.15
(R2-A0/W0) USE
RESULT C TGR
101.18
R4 (D0.4) USE

FIG.90

C BIT GENERATOR

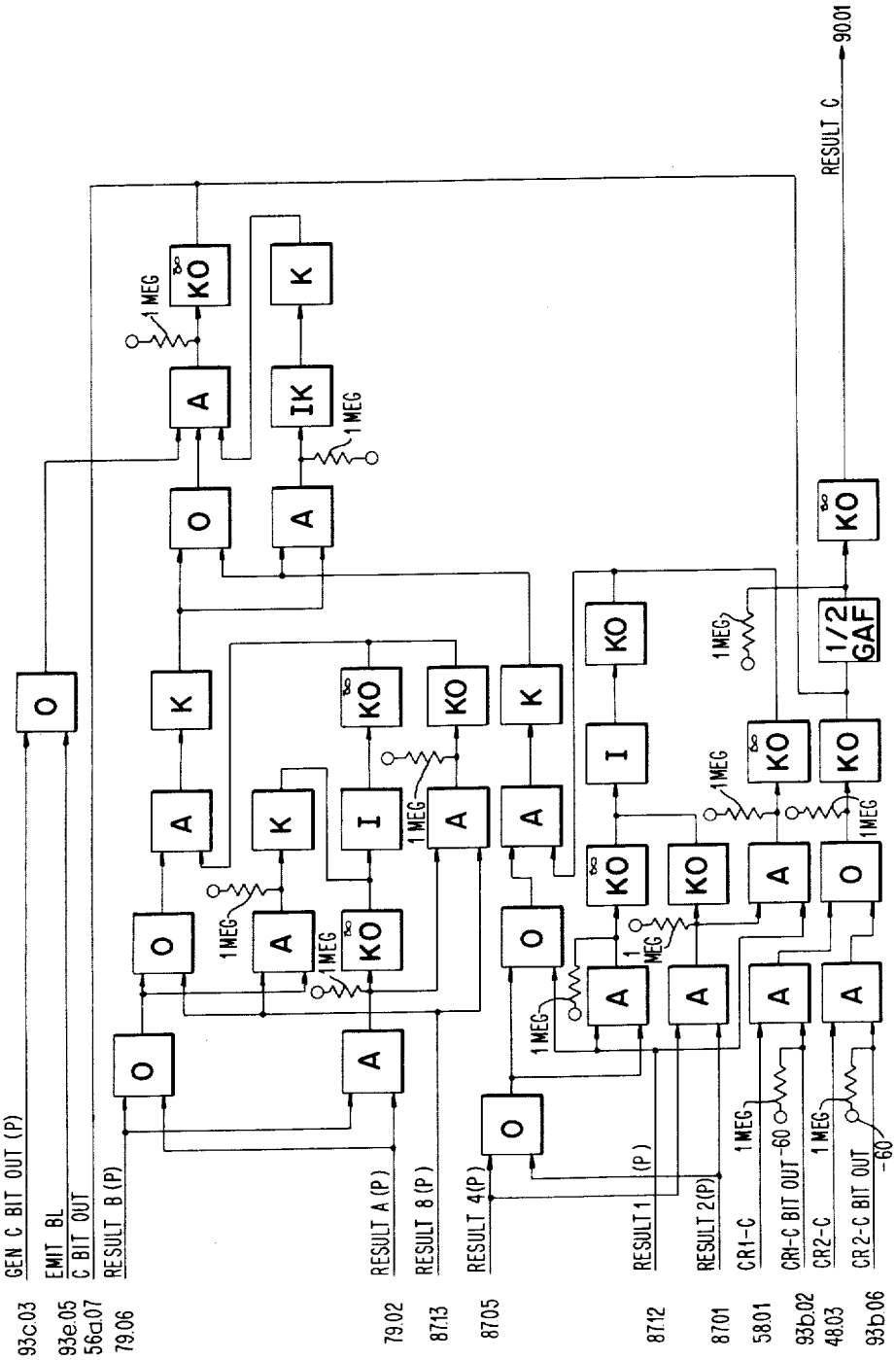


FIG. 91 RESULT REGISTER CODE CHECK - ERROR TRIGGER

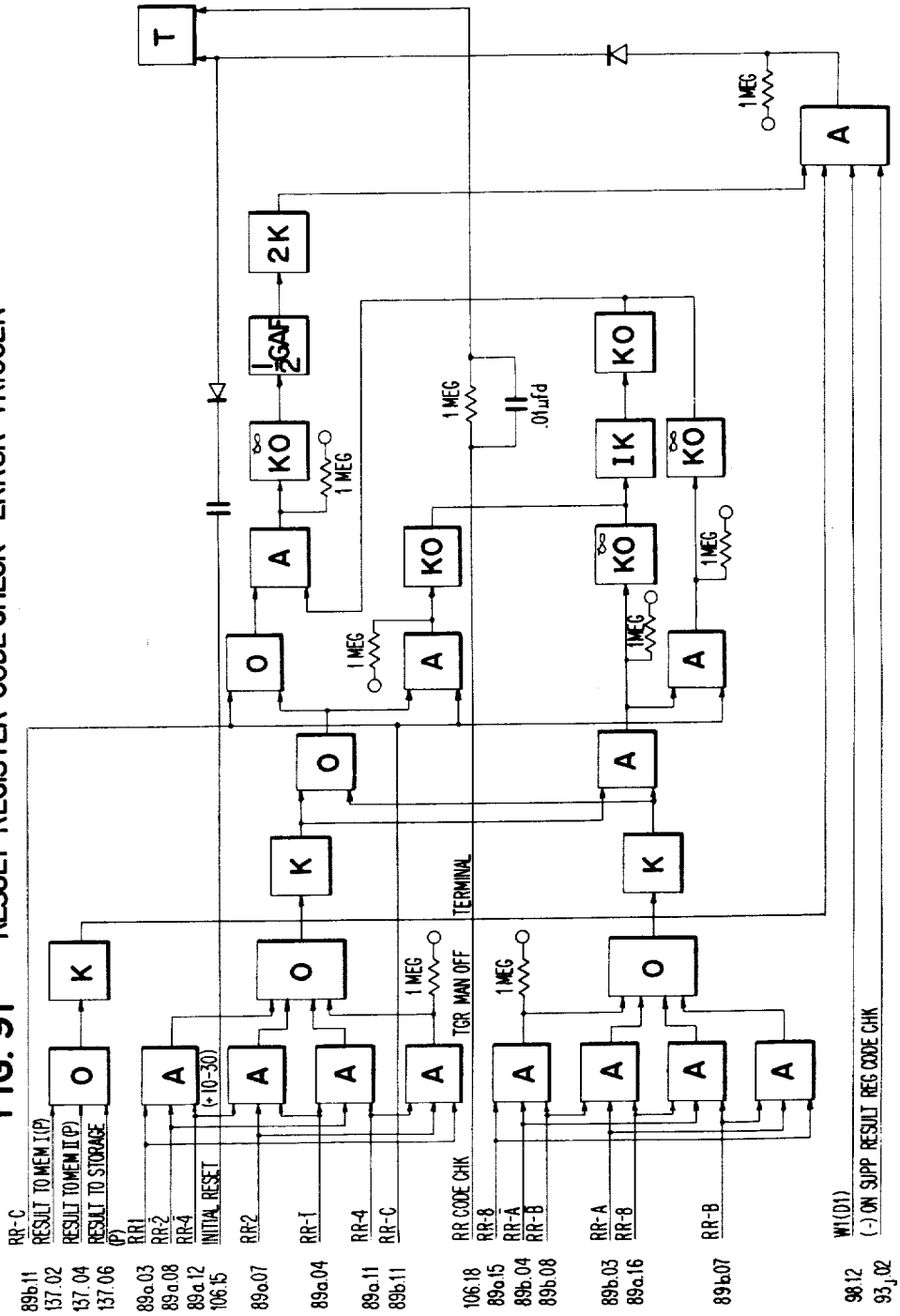


FIG.92

MEMORY TEST-CHARACTER SELECTOR

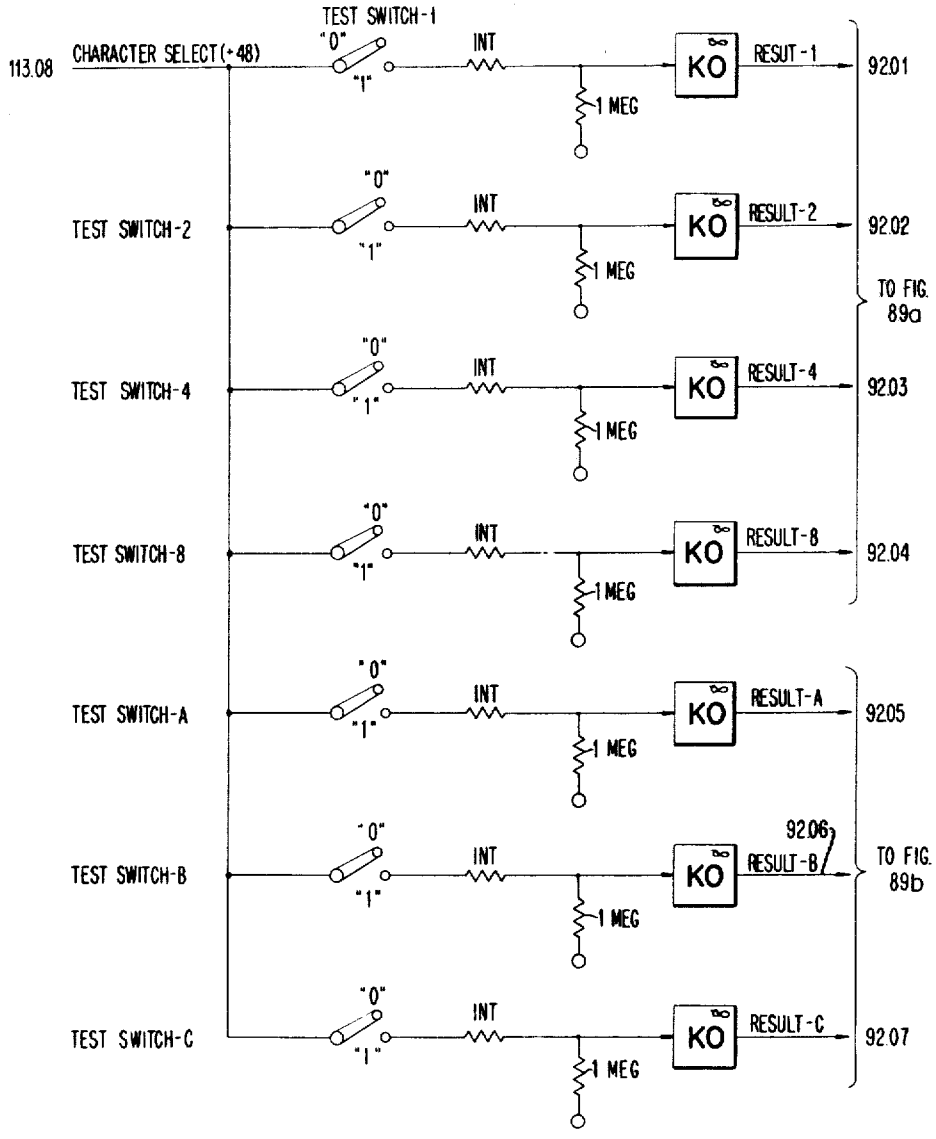


FIG.93a

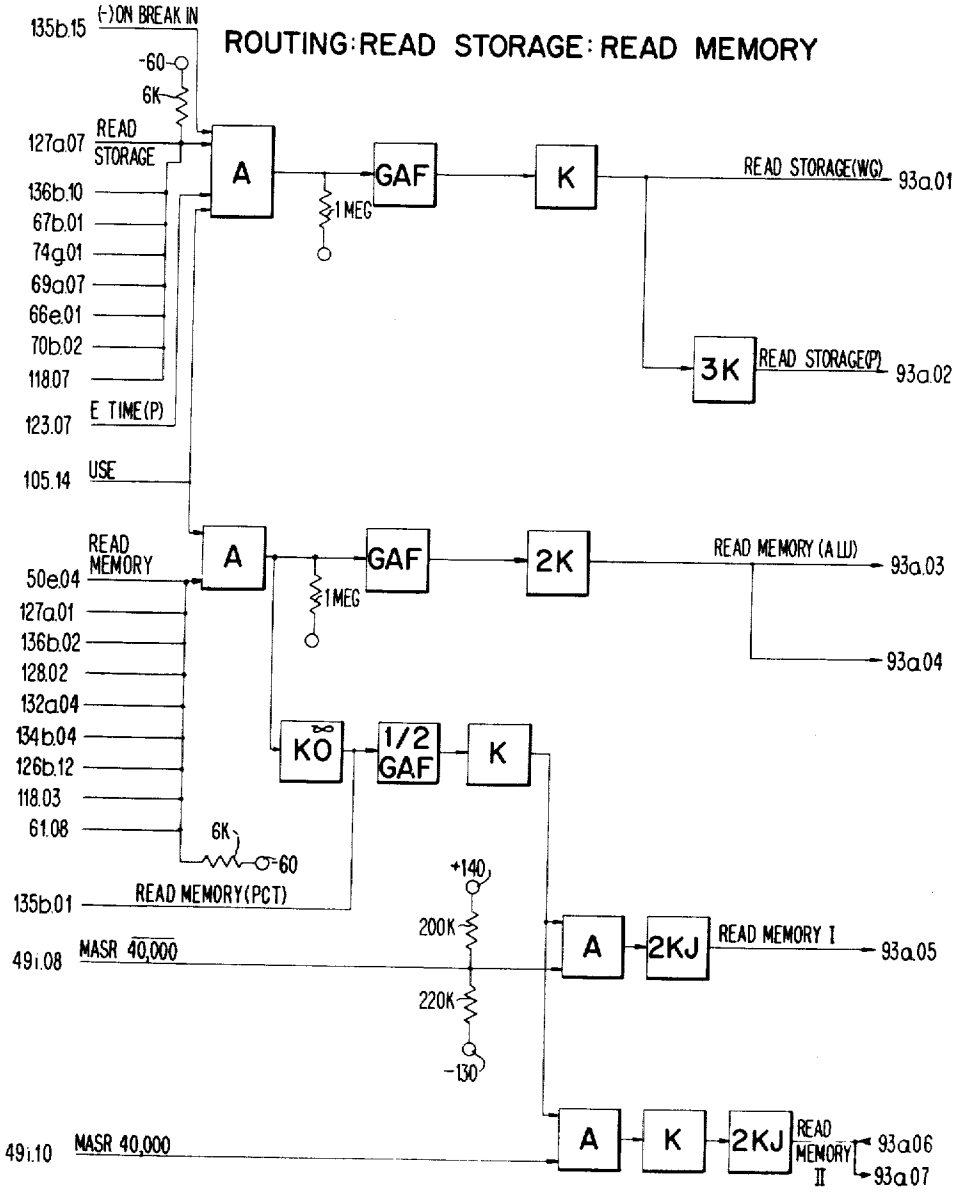

ROUTING:READ STORAGE:READ MEMORY
135b.15
(-)ON BREAK IN
-60
6K
127a.07
READ STORAGE
136b.10
67b.01
74g.01
69a.07
66e.01
70b.02
118.07
123.07
E TIME(P)
105.14
USE
A
1 MEG
GAF
K
READ STORAGE(WG)
93a.01
3K
READ STORAGE(P)
93a.02
READ MEMORY
50e.04
127a.01
136b.02
128.02
132a.04
134b.04
126b.12
118.03
61.08
A
1 MEG
GAF
2K
READ MEMORY (ALU)
93a.03
93a.04
KO
1/2 GAF
K
6K
-60
135b.01
READ MEMORY(PCT)
+140
200K
220K
-130
491.08
MASR 40,000
A
2KJ
READ MEMORY I
93a.05
491.10
MASR 40,000
A
K
2KJ
READ MEMORY II
93a.06
93a.07

FIG. 93b

CHARACTER REGISTERS TO ADDER ROUTING

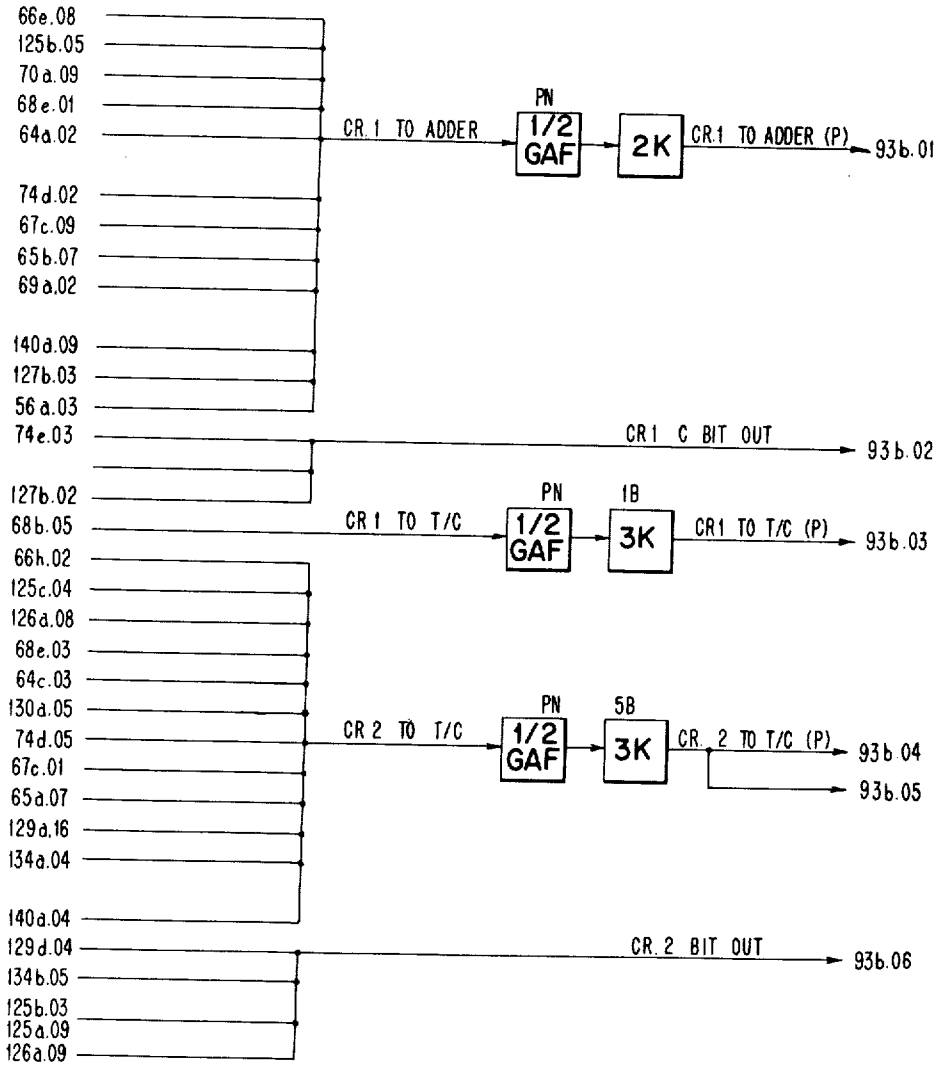


FIG. 93c
ADDER OUT ROUTING

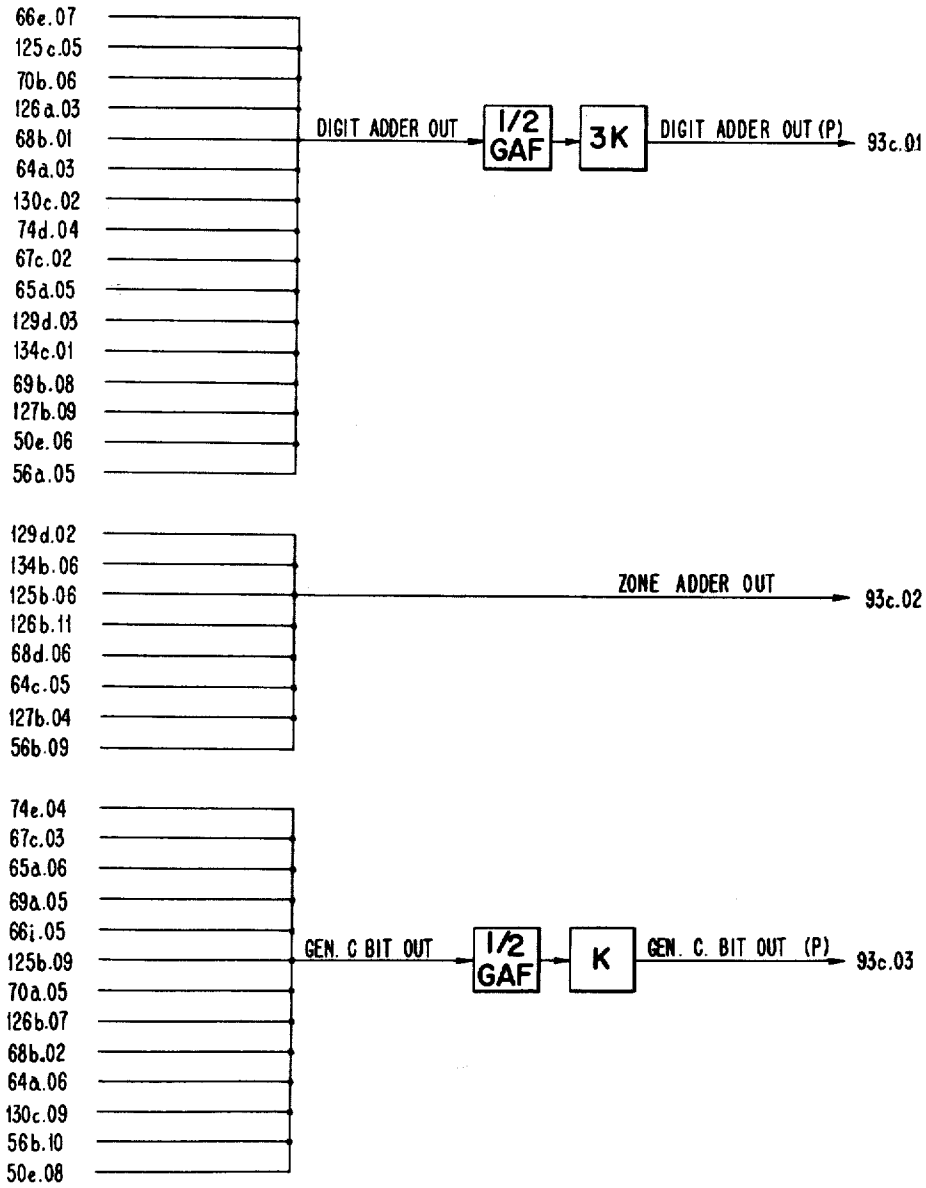


FIG. 93d
ADDER CARRY ROUTING

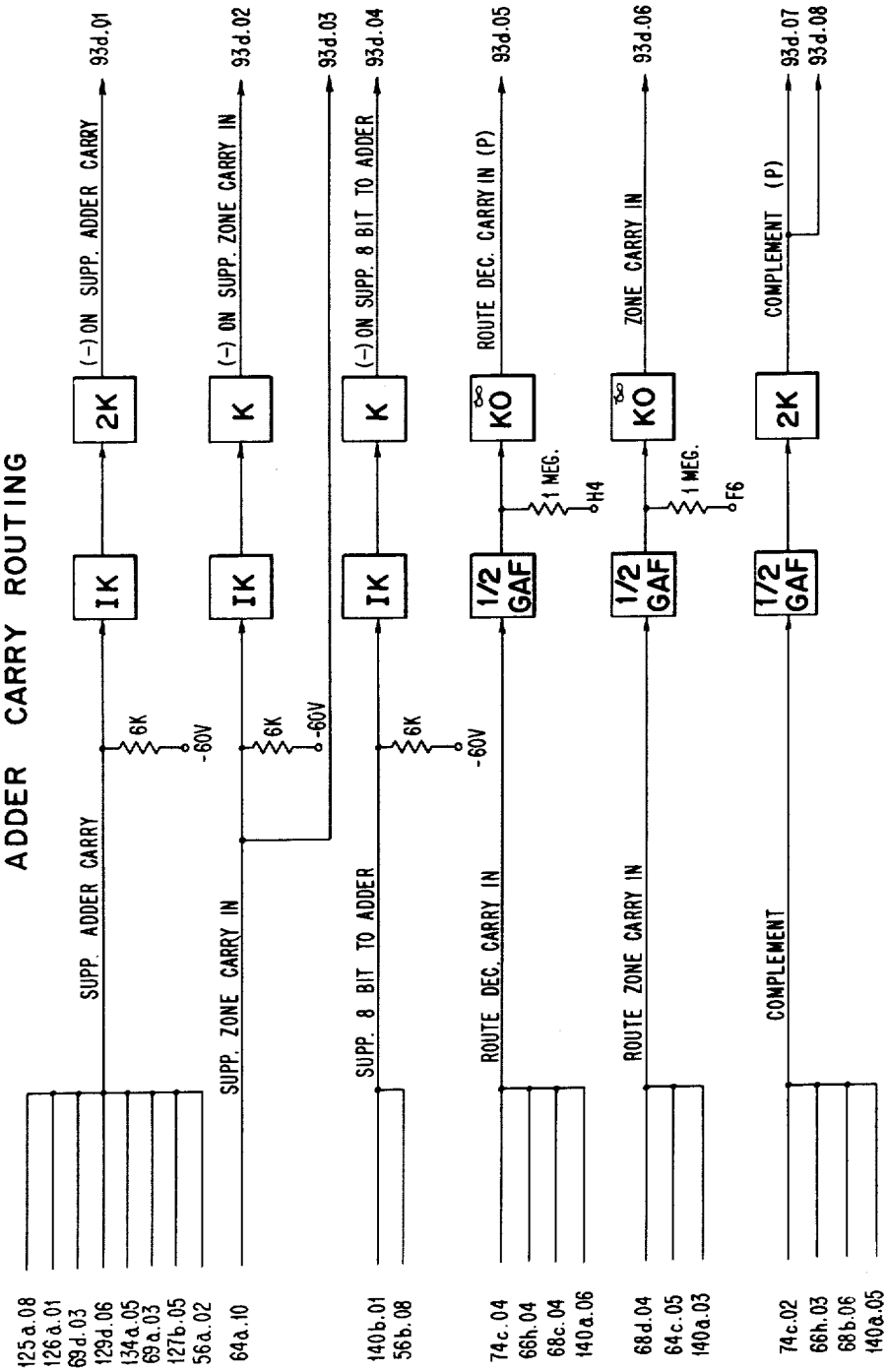


FIG. 93e
ADDER EMITTER AND MPL REG. ROUTING

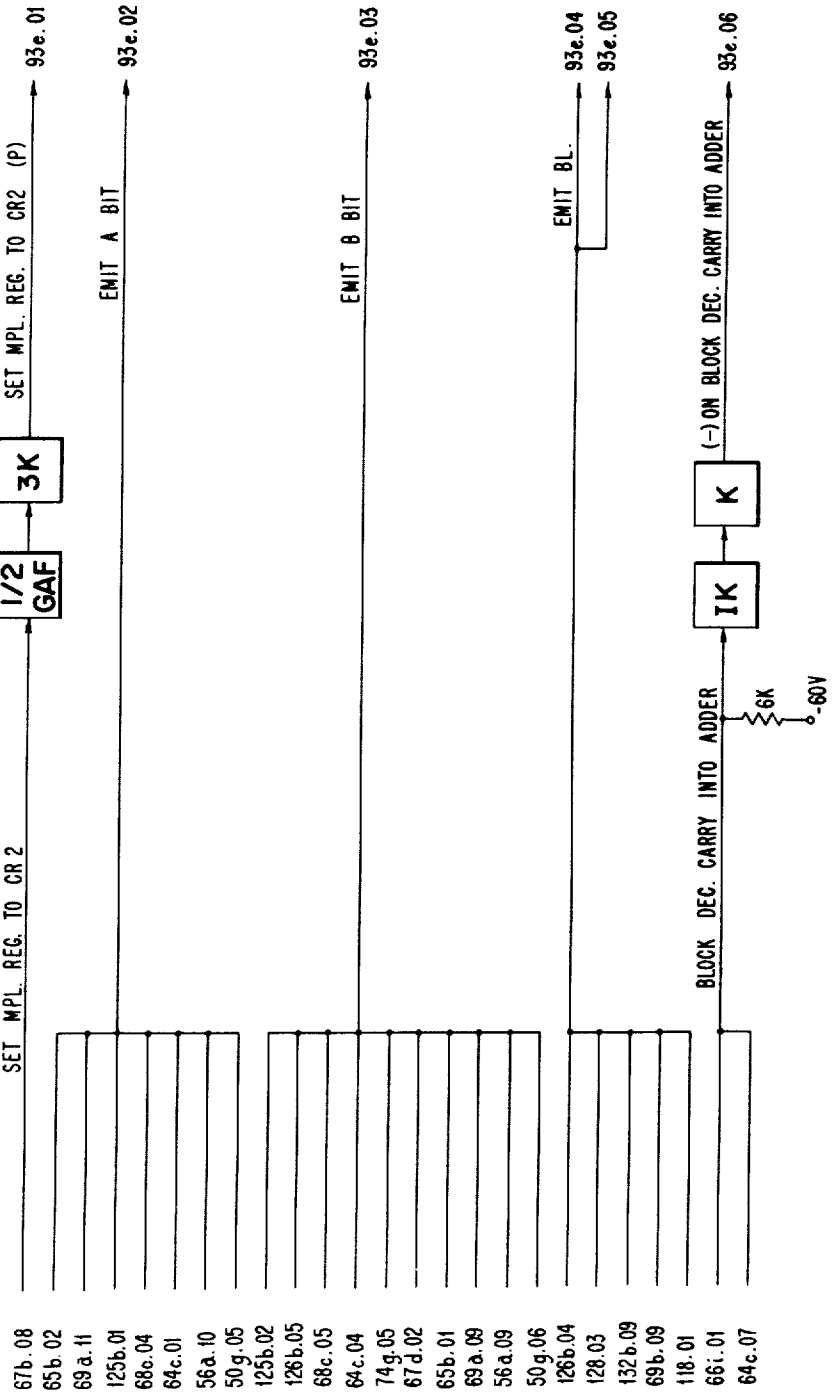


FIG. 93f

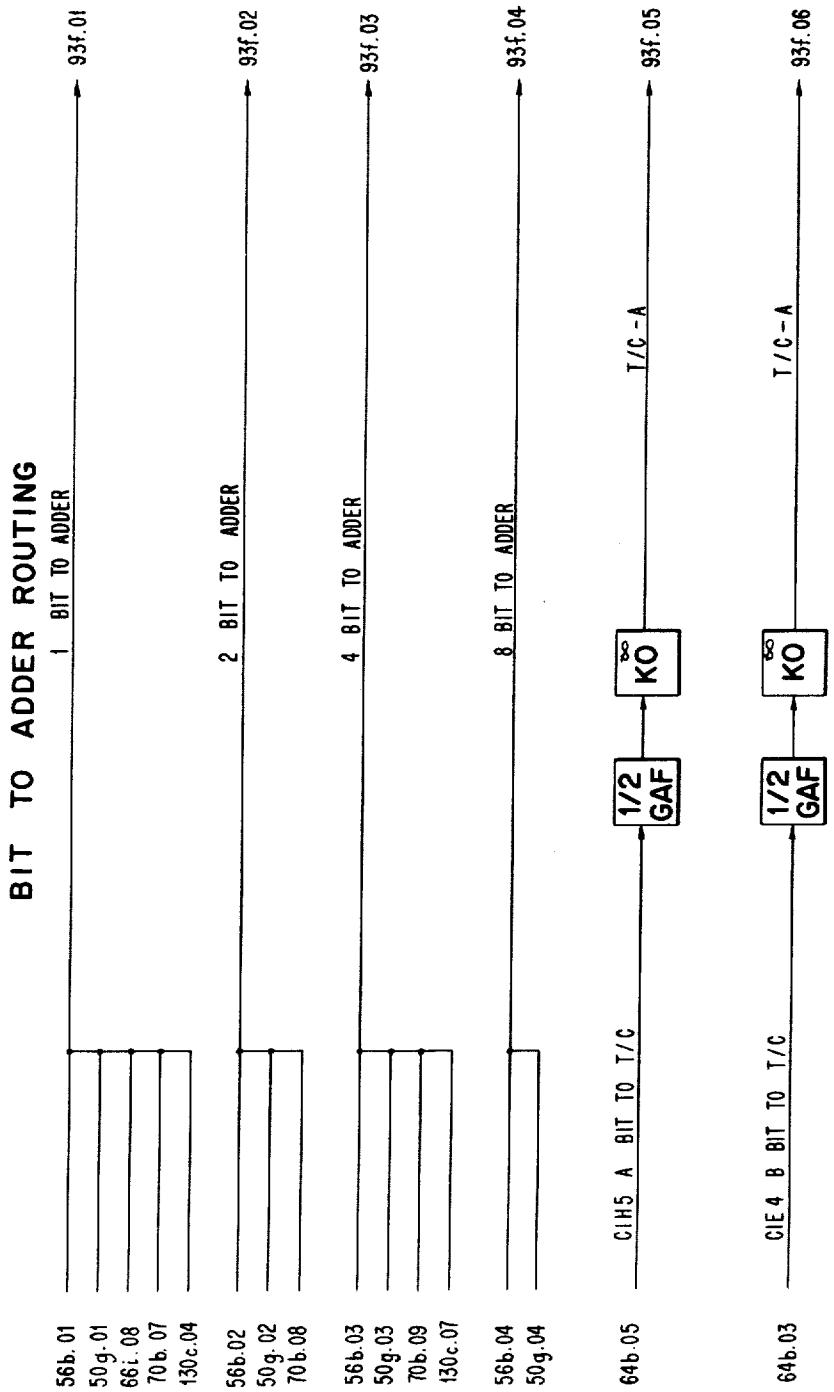

BIT TO ADDER ROUTING
1 BIT TO ADDER
2 BIT TO ADDER
4 BIT TO ADDER
8 BIT TO ADDER
93f.01
93f.02
93f.03
93f.04
93f.05
93f.06
T/C - A
T/C - A
KO
KO
1/2 GAF
1/2 GAF
C1H5 A BIT TO T/C
C1E4 B BIT TO T/C
56b.01
50g.01
66i.08
70b.07
130c.04
56b.02
50g.02
70b.08
56b.03
50g.03
70b.09
130c.07
56b.04
50g.04
64b.05
64b.03

FIG. 93g

STEP MAC. 1 ± 1 ROUTING

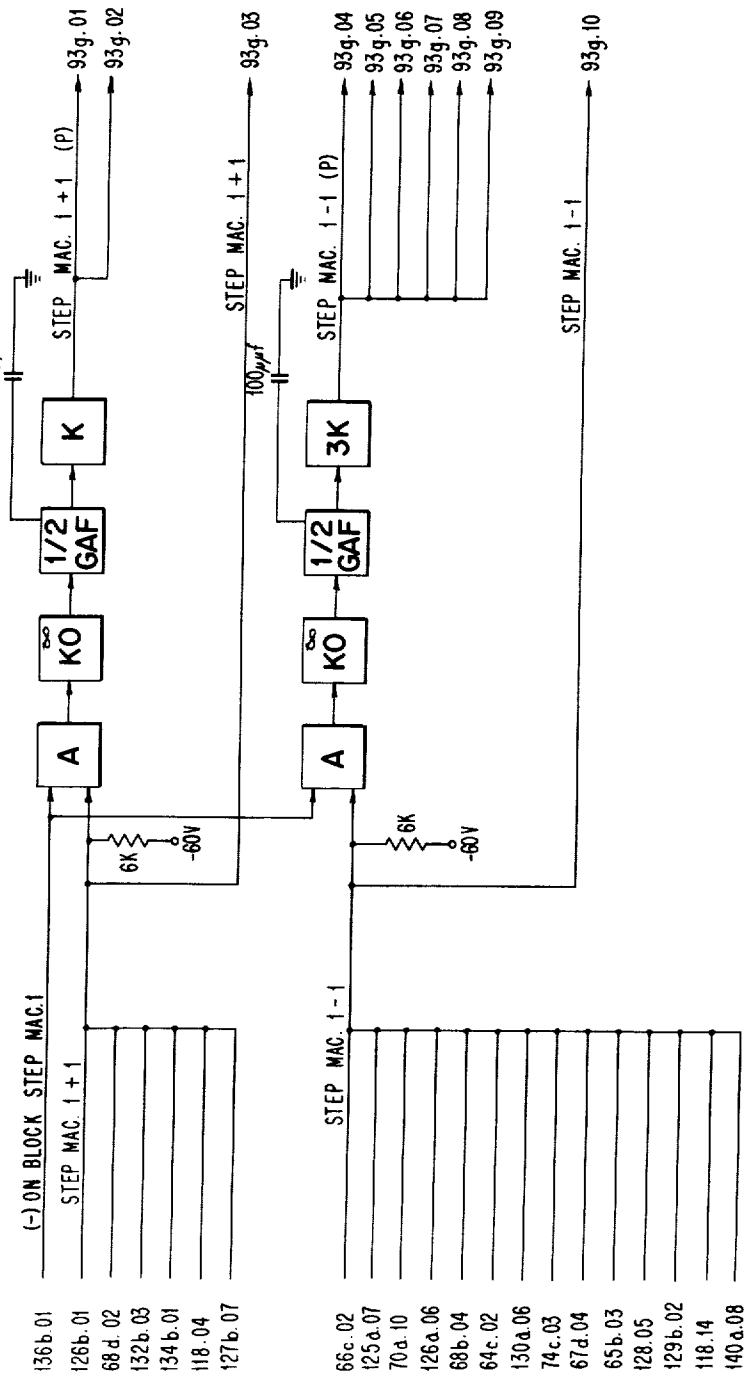


FIG. 93h

STEP MAC. 2+1, STEP MAC. 1+5, STEP MAC. 2+5

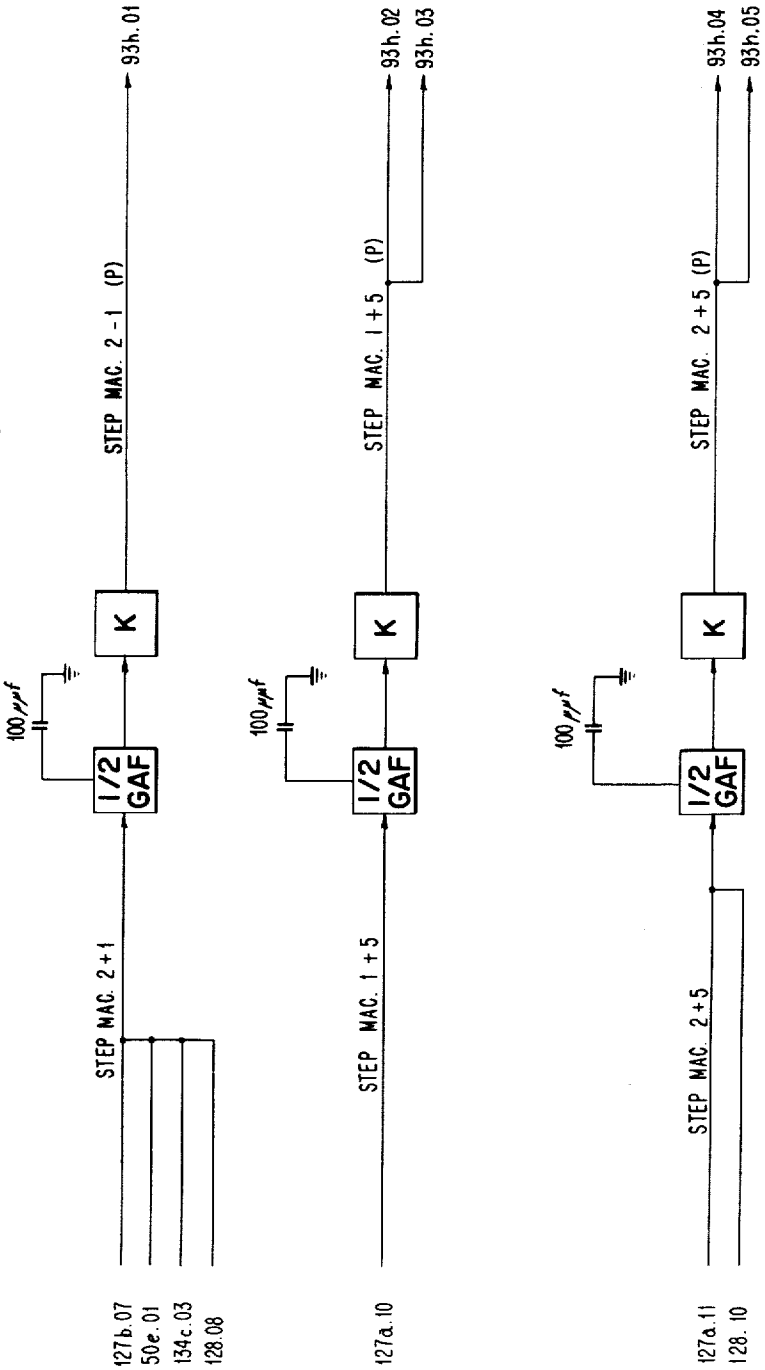
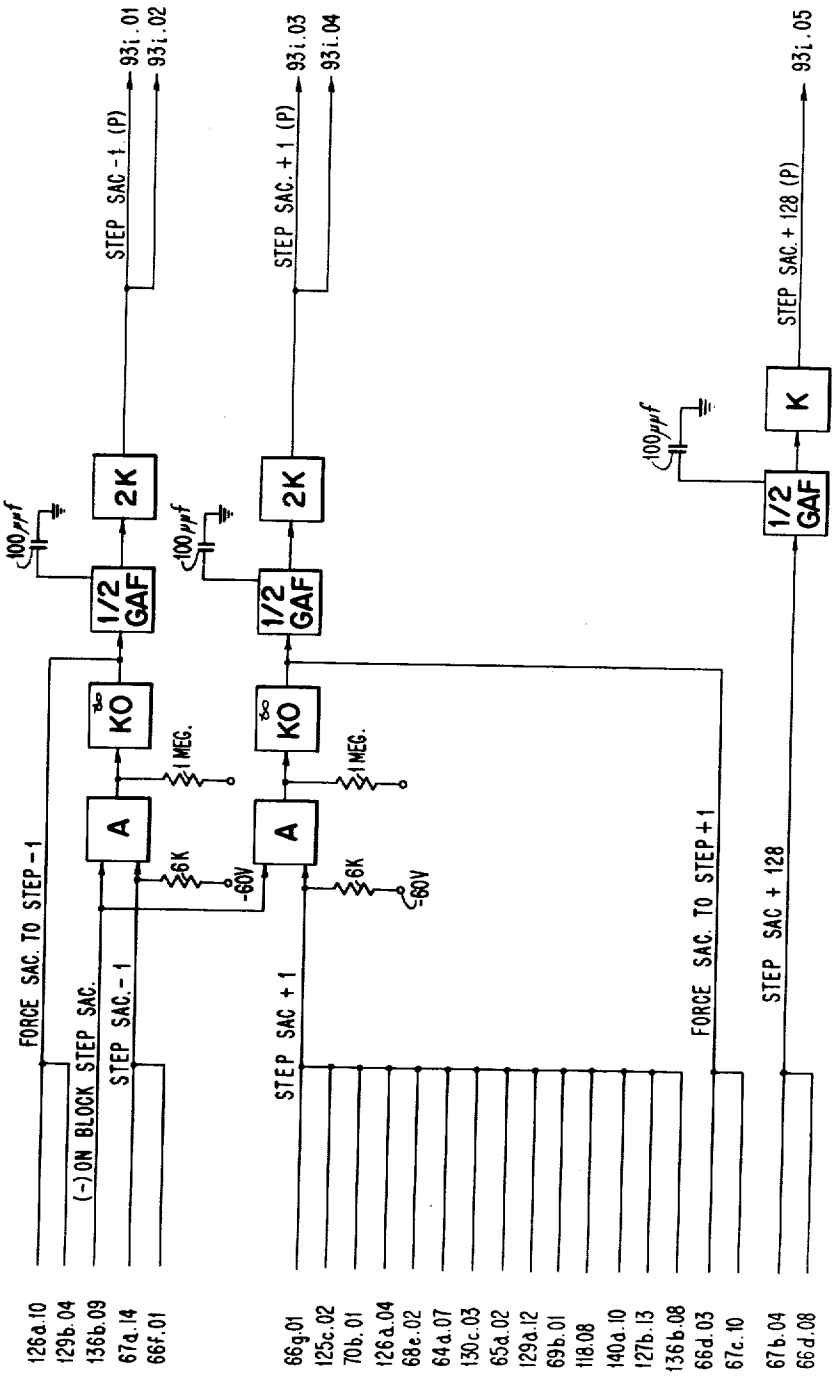


FIG. 93i

STEP SAC ROUTING



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FIG. 93j

STORAGE, MEMORY AND INSTRUCTION COUNTER ROUTING

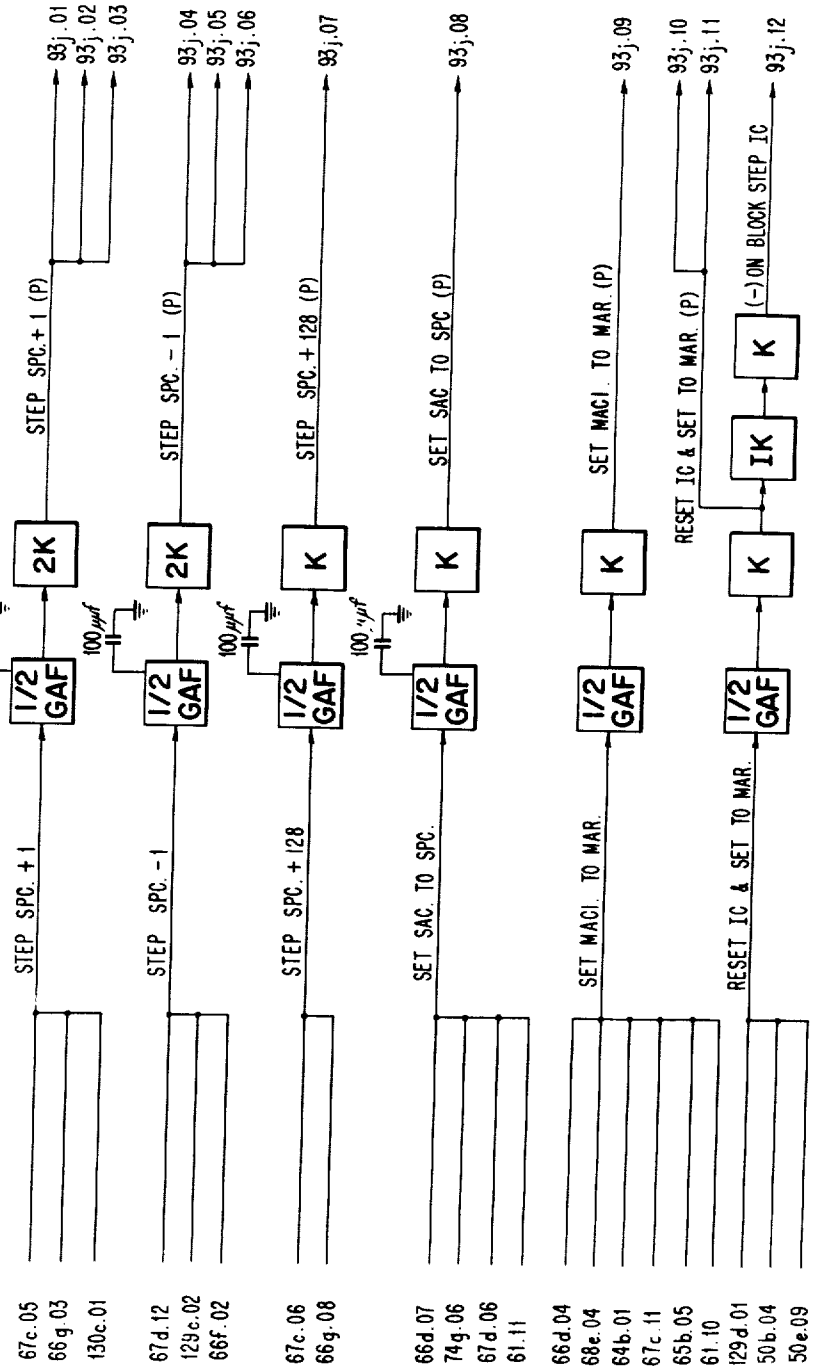


FIG. 93k

AUXILIARY TRIG.'S ROUTING

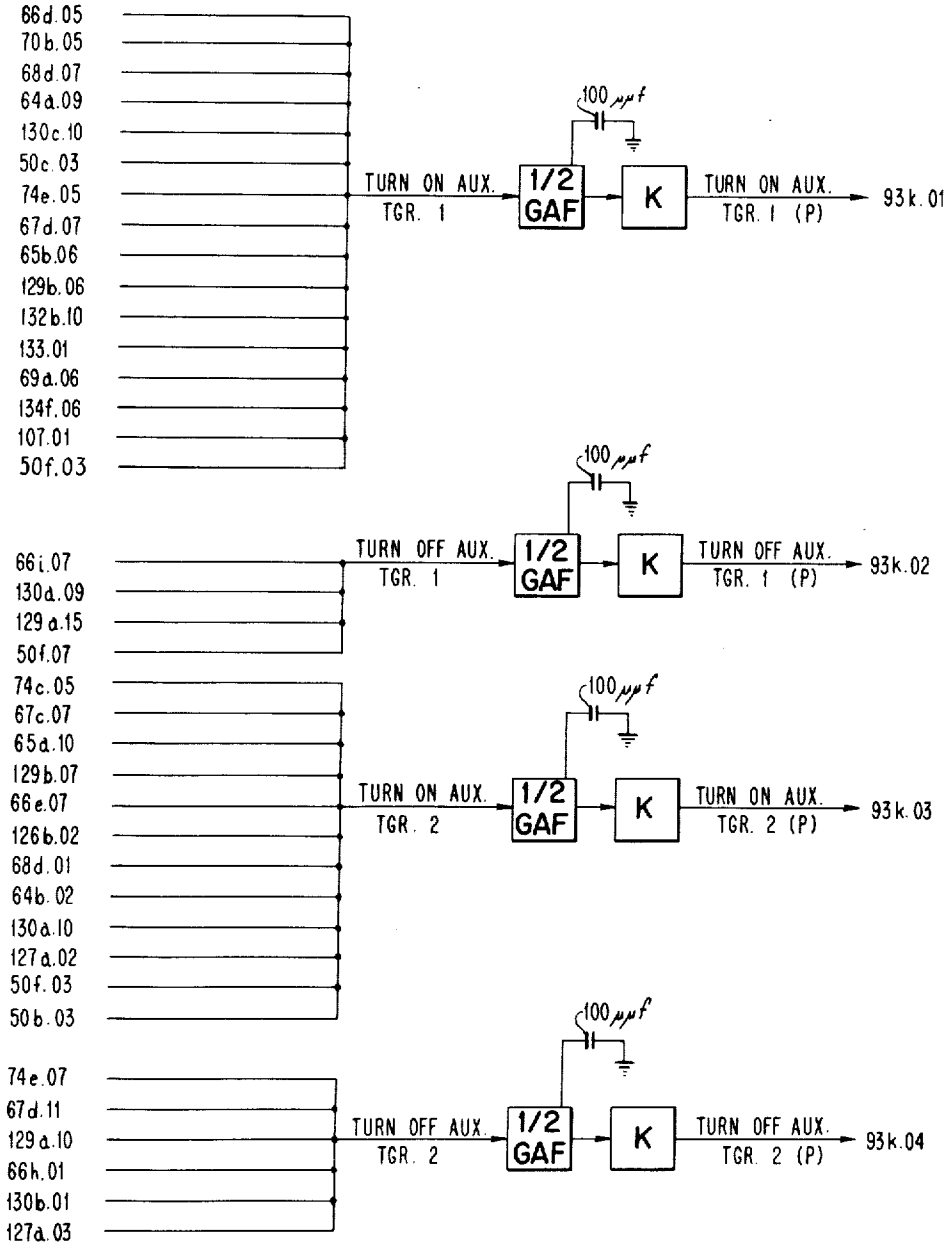


FIG. 931

AUX. TRIG. STOR. HI. TRIG., AND RMDR. TRIG. ROUTING

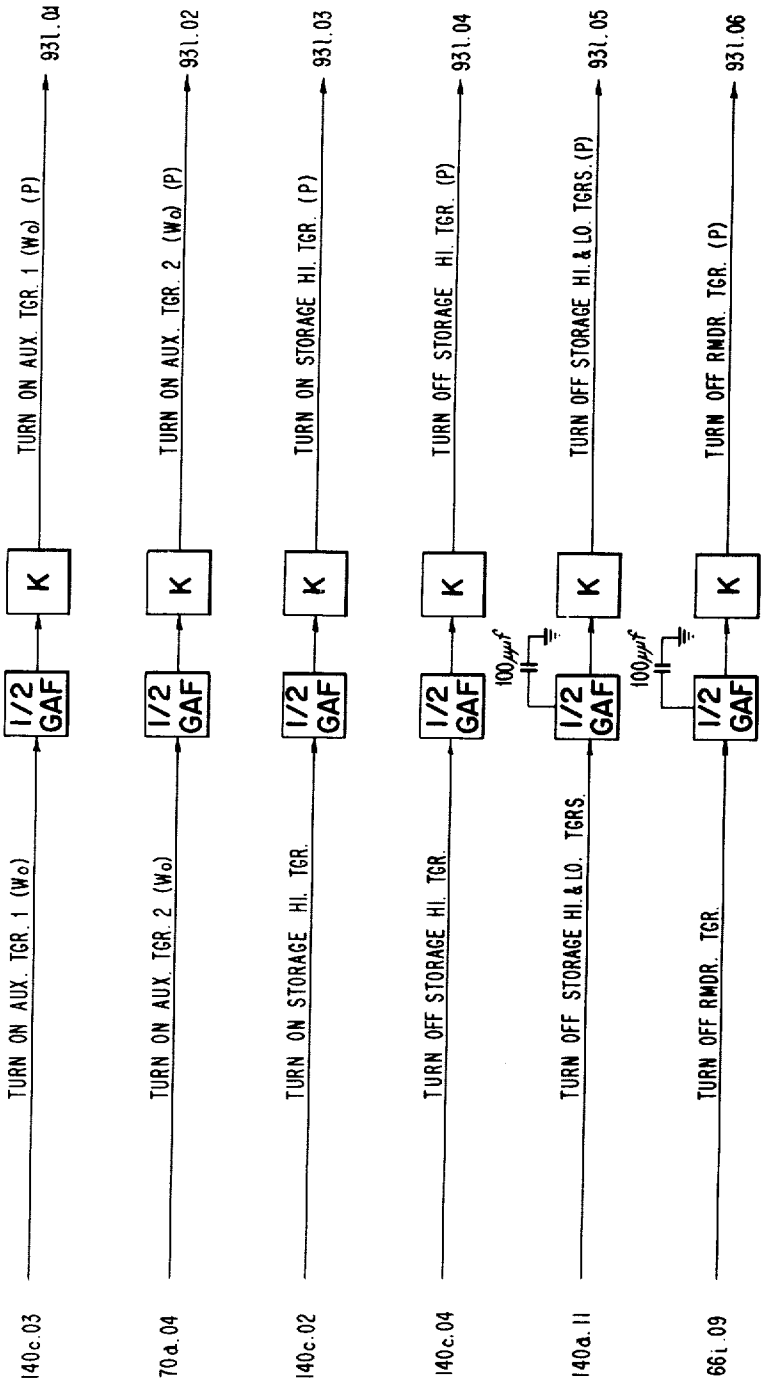
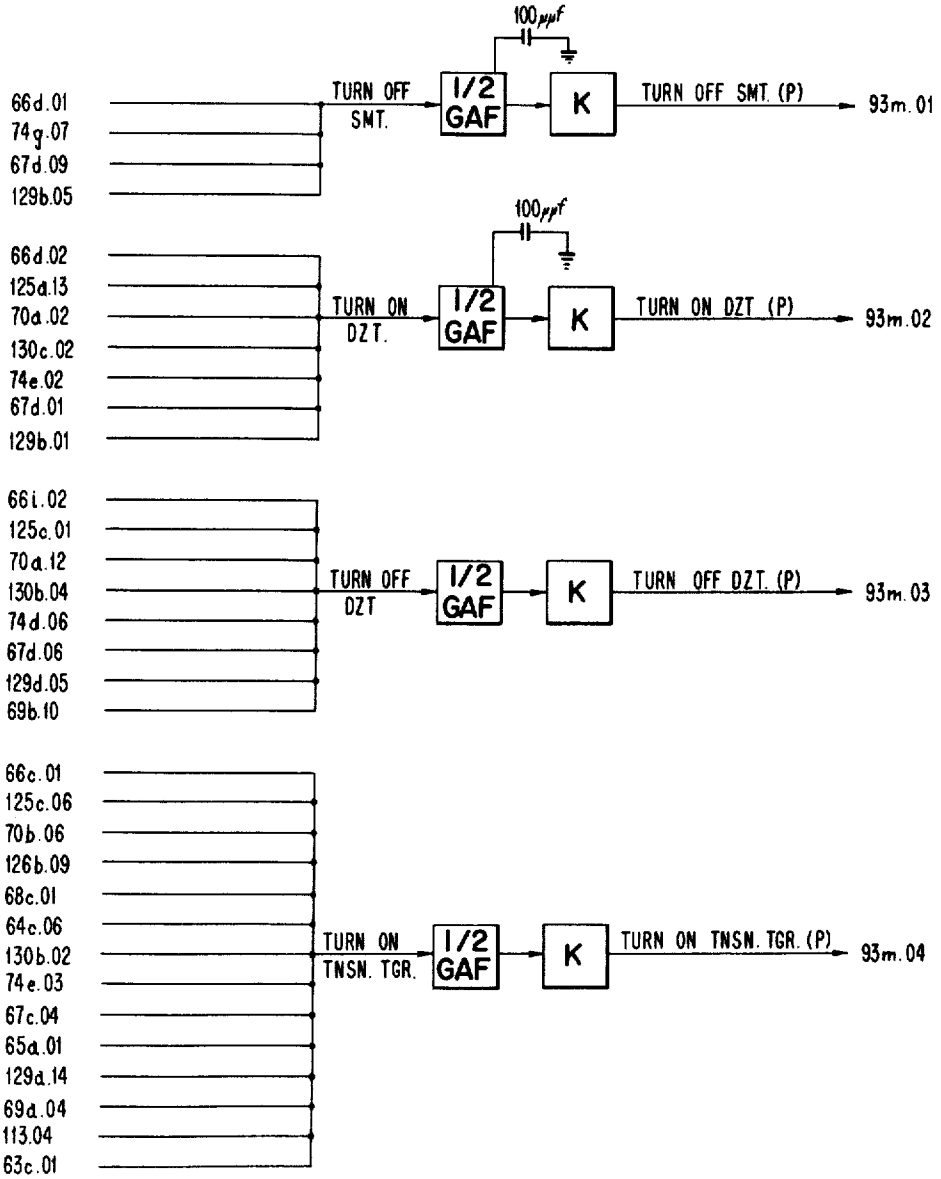


FIG. 93m

SMT. DZT. AND TNSN TRIG. ROUTING



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FIG.93n SIGN CHK TGR OVFL CHK TRIG AND STOR SIGN TRIG ROUTING

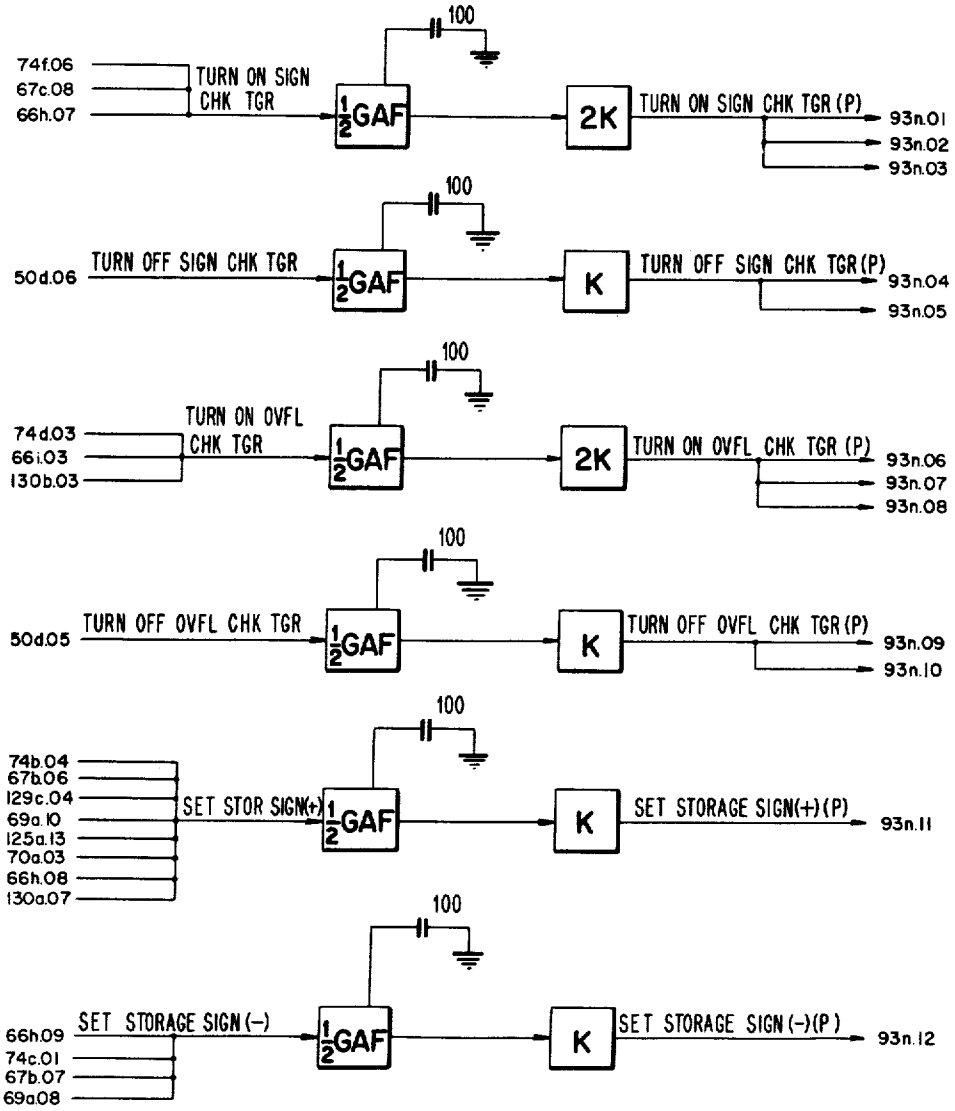


FIG.93o

R/W CHK TGR RECORD CHK TGR AND INSTR CHK TGR ROUTING

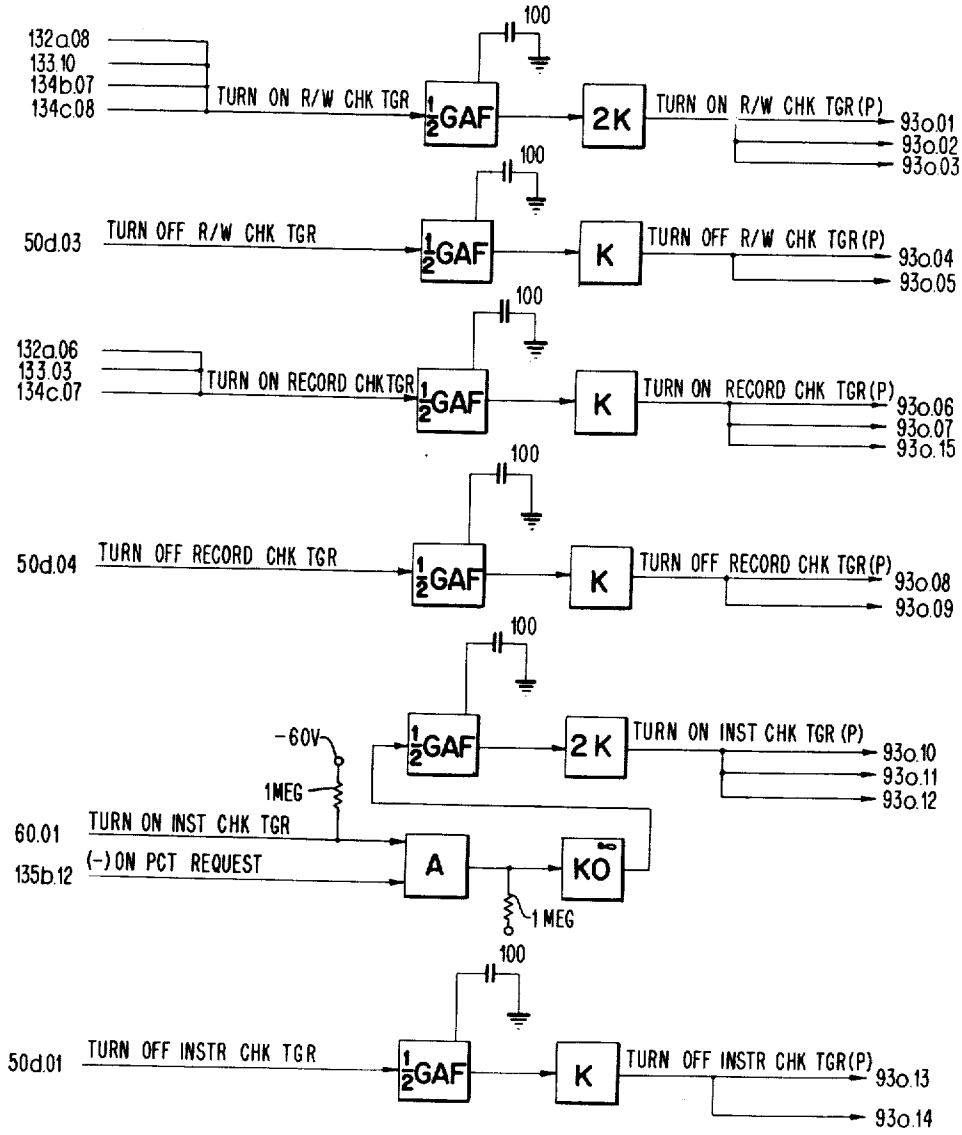


FIG.93p

MEMORY CONTROL ROUTING

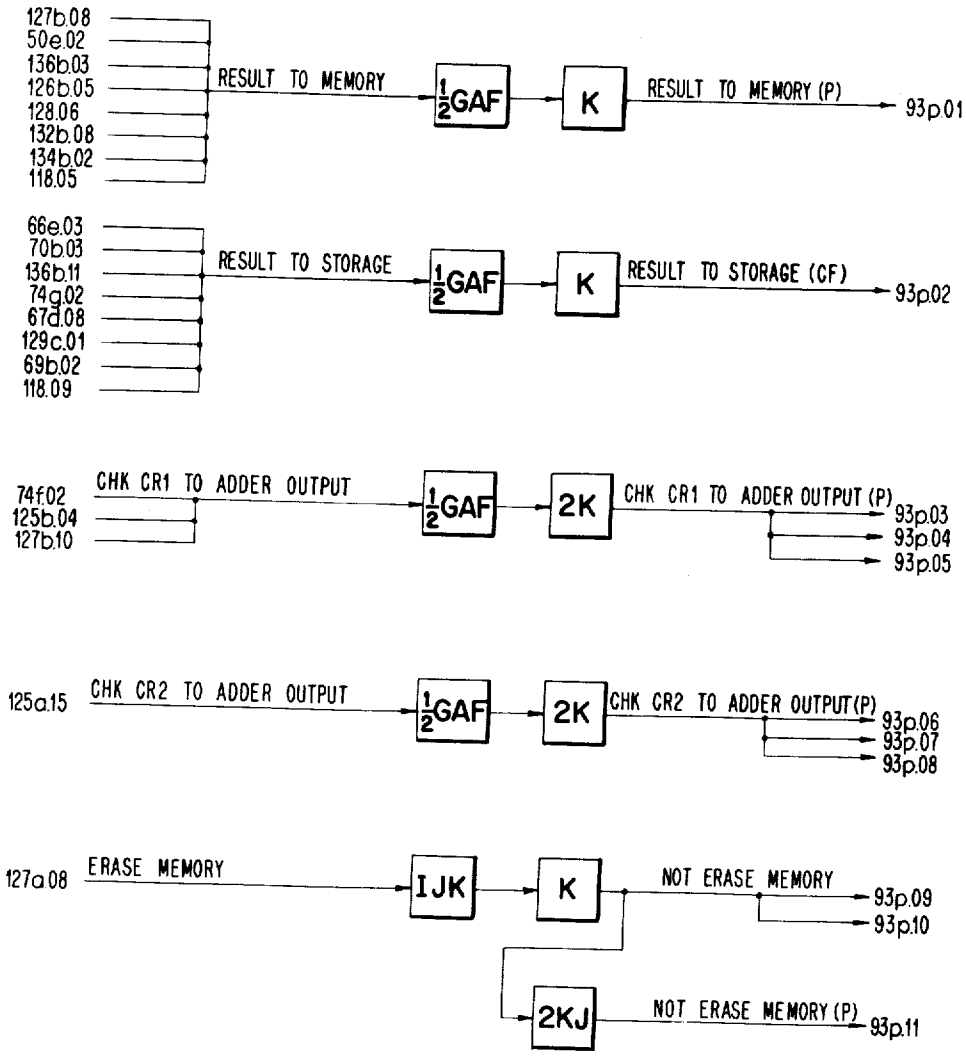


FIG.93q MODE CONTROL ROUTING

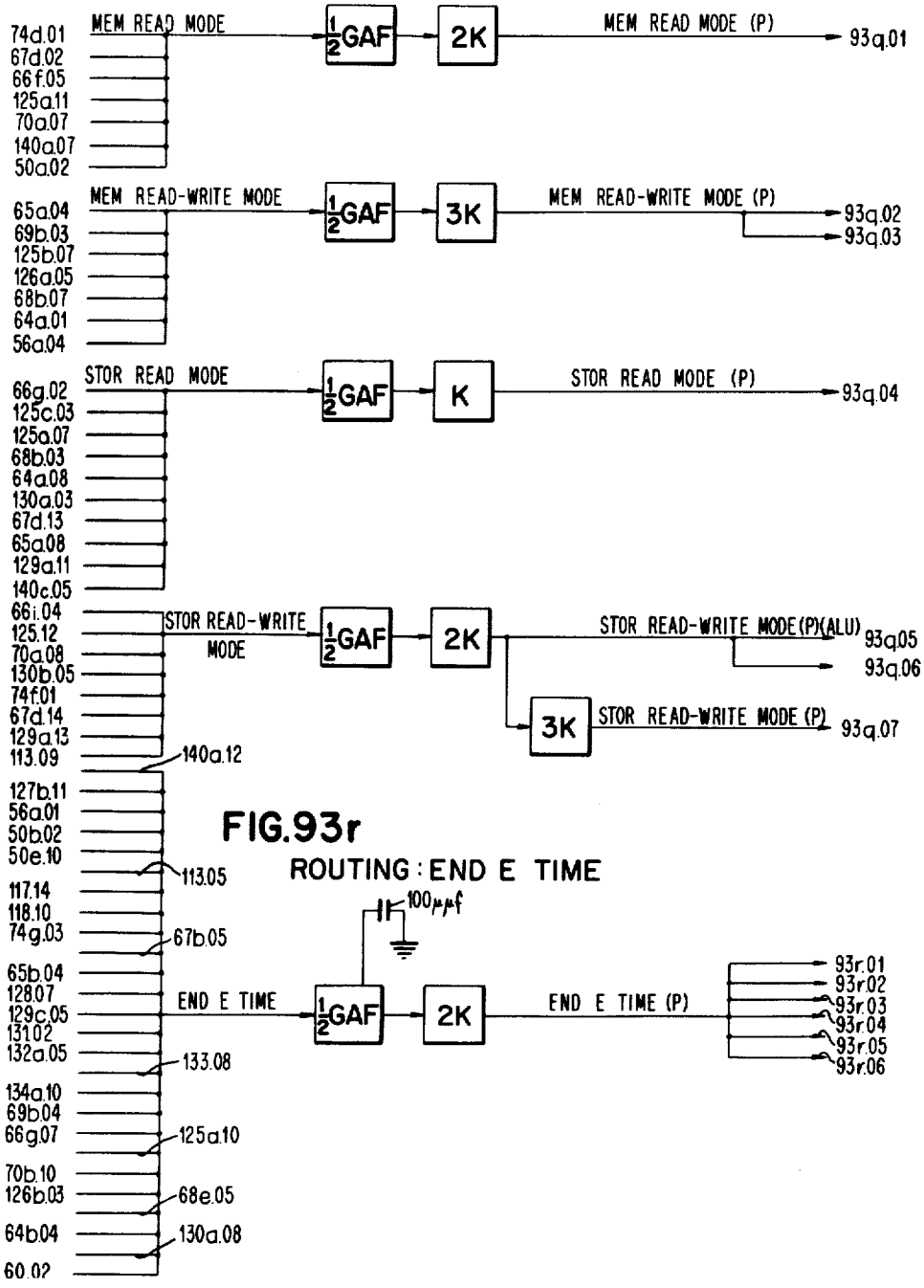


FIG.93r ROUTING: END E TIME

FIG. 93s

MASR INPUT SWITCHING

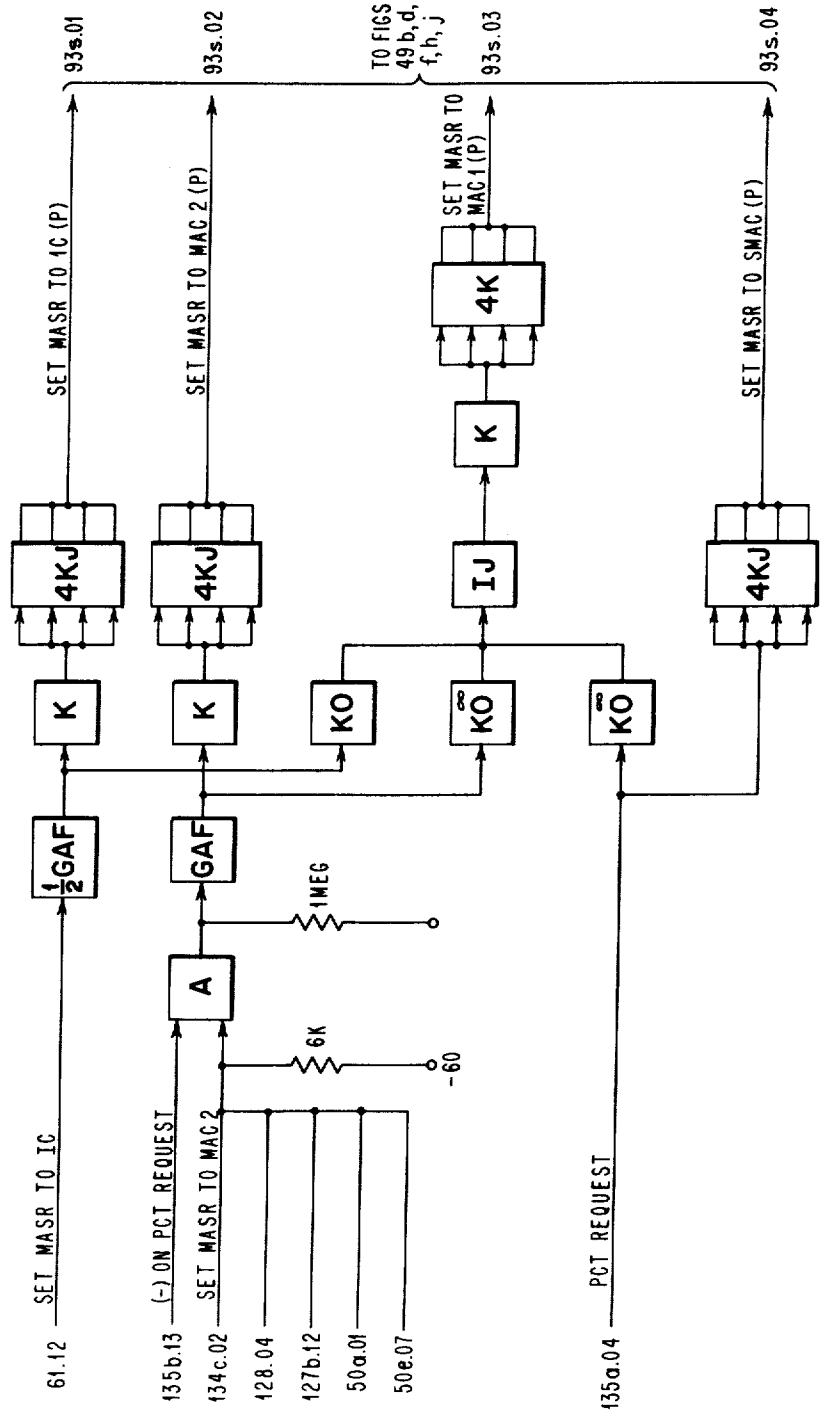


FIG. 93t

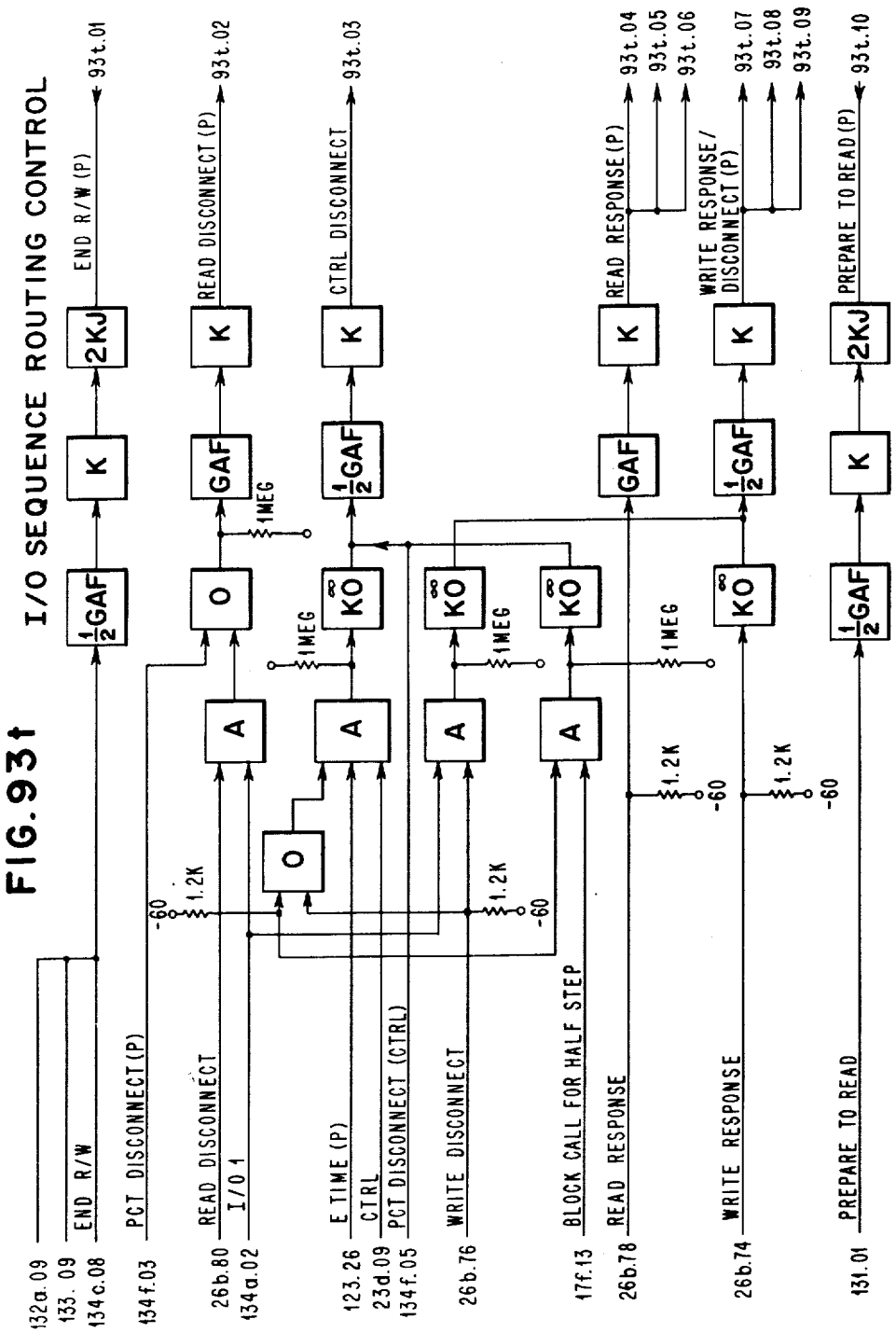
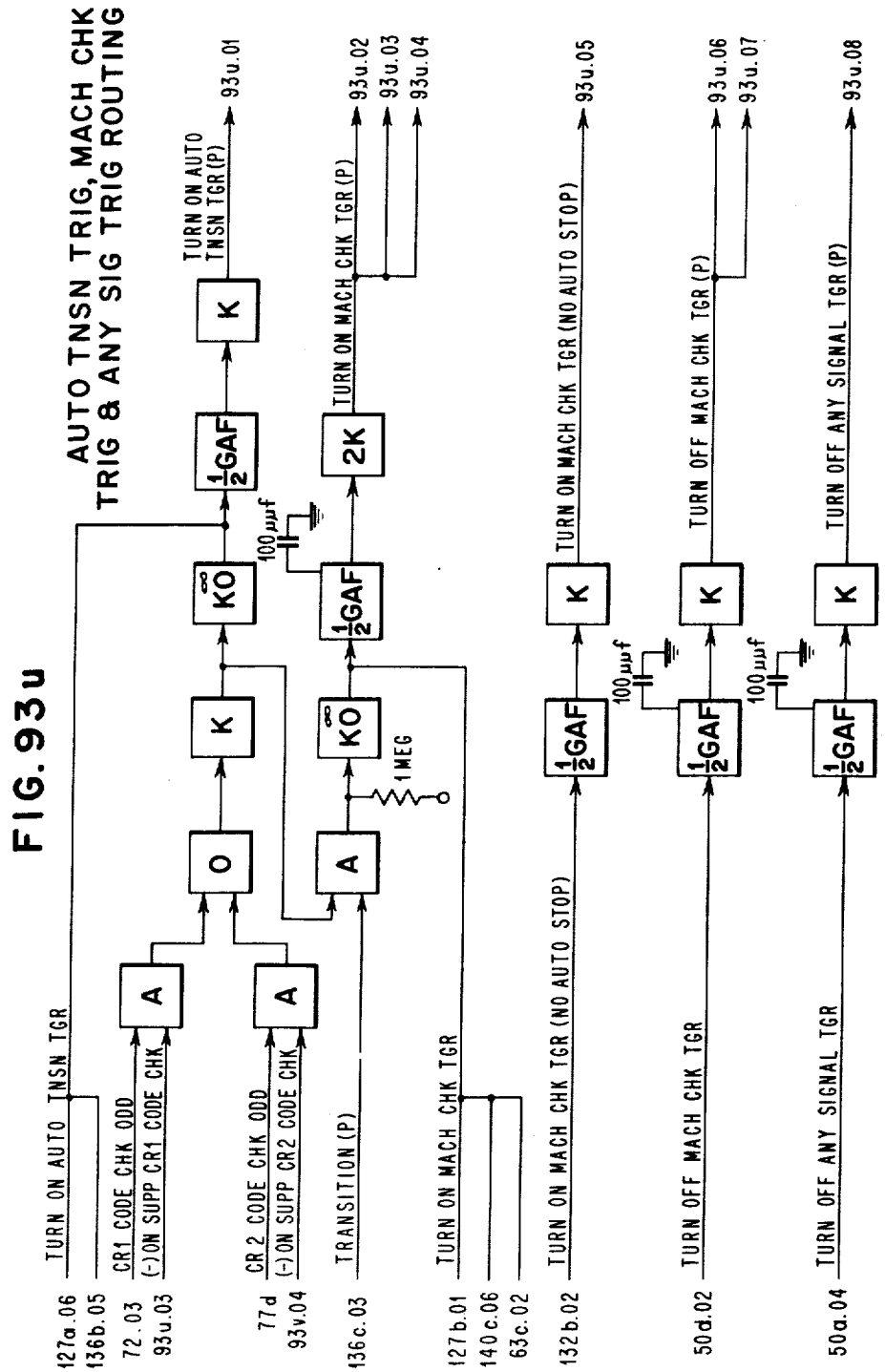

I/O SEQUENCE ROUTING CONTROL
132a.09
133.09
134c.08
134f.03
26b.80
134a.02
123.26
23d.09
134f.05
26b.76
17f.13
26b.78
26b.74
131.01
END R/W
PCT DISCONNECT (P)
READ DISCONNECT
I/O 1
E TIME (P)
CTRL
PCT DISCONNECT (CTRL)
WRITE DISCONNECT
BLOCK CALL FOR HALF STEP
READ RESPONSE
WRITE RESPONSE
PREPARE TO READ
END R/W (P)
READ DISCONNECT (P)
CTRL DISCONNECT
READ RESPONSE (P)
WRITE RESPONSE / DISCONNECT (P)
PREPARE TO READ (P)
93t.01
93t.02
93t.03
93t.04
93t.05
93t.06
93t.07
93t.08
93t.09
93t.10
1MEG
1.2K
-60
A
O
K
KO
GAF
1/2GAF
2KJ

FIG. 93u


AUTO TNSN TRIG, MACH CHK TRIG & ANY SIG TRIG ROUTING
TURN ON AUTO TNSN TGR
CR1 CODE CHK ODD
(-)ON SUPP CR1 CODE CHK
CR 2 CODE CHK ODD
(-)ON SUPP CR2 CODE CHK
TRANSITION (P)
TURN ON MACH CHK TGR
TURN ON MACH CHK TGR (NO AUTO STOP)
TURN OFF MACH CHK TGR
TURN OFF ANY SIGNAL TGR
TURN ON AUTO TNSN TGR (P)
TURN ON MACH CHK TGR (P)
TURN ON MACH CHK TGR (NO AUTO STOP)
TURN OFF MACH CHK TGR (P)
TURN OFF ANY SIGNAL TGR (P)
A
O
K
KO
1/2GAF
2K
100 μμf
1 MEG
127a.06
136b.05
72.03
93u.03
77d
93v.04
136c.03
127b.01
140c.06
63c.02
132b.02
50d.02
50a.04
93u.01
93u.02
93u.03
93u.04
93u.05
93u.06
93u.07
93u.08

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FIG. 93v

BLOCK ADD TGR, SUPP CODE CHECKING

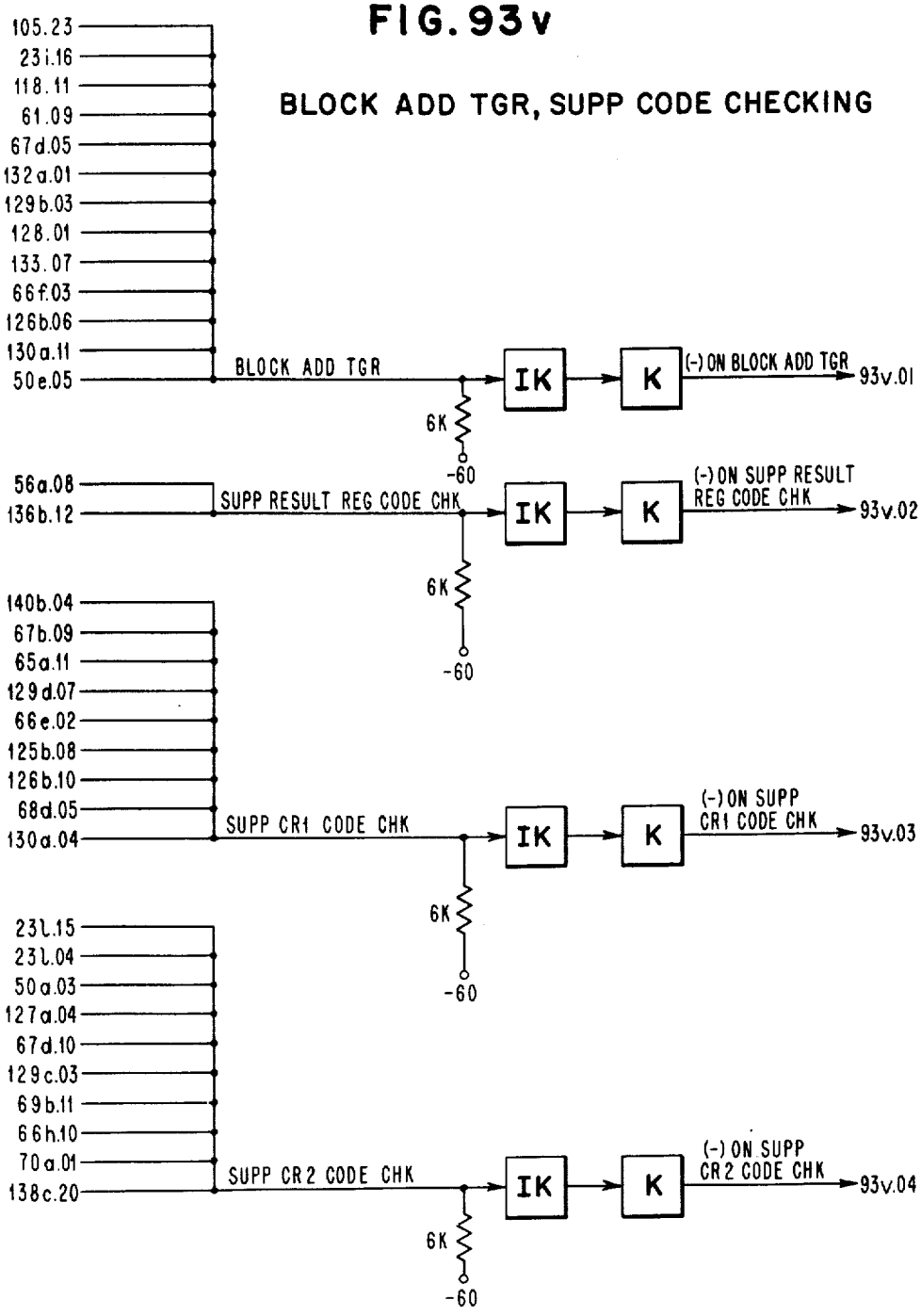


FIG. 93w TYPE CYCLE NEONS, PAR I/O CHK NEON, CODE CHK NEONS

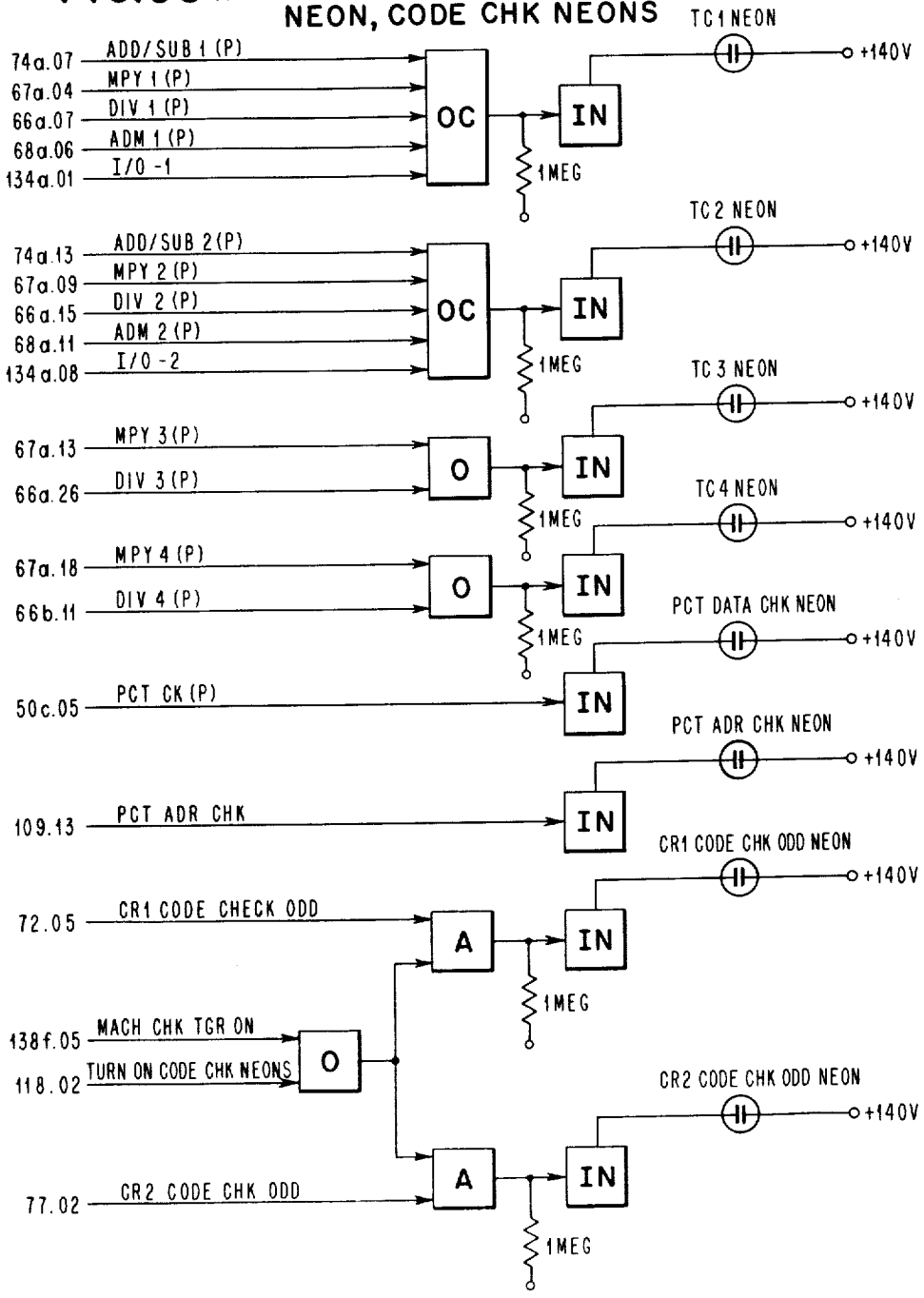


FIG. 94

P.C.T. CABLE - CONNECTOR RECEPTACLE SHOWN FROM WIRING SIDE

8 RD BUS CHAR 0-1 14b.03	7 NOT DEMAND 7	6 NOT DEMAND 6	5 NOT DEMAND 5	4 NOT DEMAND 4	3 NOT DEMAND 3	2 NOT DEMAND 2	1 NOT DEMAND 1
16 RD BUS CHAR 0-B 14b.03	15 RD BUS CHAR 0-A 14b.03	14 RD BUS CHAR 0-8 14b.03	13 GND	12 RD BUS CHAR 0-4 14b.03	11 GND	10 RD BUS CHAR 0-2 14b.03	9 GND
24 GND	23 RD BUS CHAR 1-2 14b.03	22 GND	21 RD BUS CHAR 1-1 14b.03	20 GND	19 RD BUS CHAR 0-C 14b.03	18 GND	17 MBR CODE CHK 19c.02
32 RD BUS CHAR 1-B 14b.03	31 GND	30 RD BUS CHAR 1-A 14b.03	29 GND	28 RD BUS CHAR 1-8 14b.03	27 GND	26 RD BUS CHAR 1-4 14b.03	25 GND
40 GND	39 RD BUS CHAR 2-2 14a.03	38 GND	37 RD BUS CHAR 2-1 14a.03	36 GND	35 RD BUS CHAR 1-C 14b.03	34 GND	33 SPARE
48 RD BUS CHAR 2-B 14a.03	47 GND	46 RD BUS CHAR 2-A 14a.03	45 GND	44 RD BUS CHAR 2-8 14a.03	43 GND	42 RD BUS CHAR 2-4 14a.03	41 GND
56 GND	55 RD BUS CHAR 3-2 14a.03	54 GND	53 RD BUS CHAR 3-1 14a.03	52 GND	51 RD BUS CHAR 2-C 14a.03	50 GND	49 SPARE
64 RD BUS CHAR 3-B 14a.03	63 GND	62 RD BUS CHAR 3-A 14a.03	61 GND	60 RD BUS CHAR 3-8 14a.03	59 GND	58 RD BUS CHAR 3-4 14a.03	57 GND
72 GND	71 RD BUS CHAR 4-2 14a.03	70 GND	69 RD BUS CHAR 4-1 14a.03	68 GND	67 RD BUS CHAR 3-C 14a.03	66 GND	65 SPARE
80 RD BUS CHAR 4-B 14a.03	79 GND	78 RD BUS CHAR 4-A 14a.03	77 GND	76 RD BUS CHAR 4-8 14a.03	75 GND	74 RD BUS CHAR 4-4 14a.03	73 GND
88 GND	87 WR BUS CHAR 0-2 18b.06	86 GND	85 WR BUS CHAR 0-1 18b.07	84 GND	83 RD BUS CHAR 4-C 14a.03	82 GND	81 SPARE
96 WR BUS CHAR 0-B 18b.02	95 GND	94 WR BUS CHAR 0-A 18b.03	93 GND	92 WR BUS CHAR 0-8 18b.04	91 GND	90 WR BUS CHAR 0-4 18b.05	89 GND
104 GND	103 WR BUS CHAR 1-2 18b.06	102 GND	101 WR BUS CHAR 1-1 18b.07	100 GND	99 WR BUS CHAR 0-C 18b.01	98 GND	97 SPARE
112 WR BUS CHAR 1-B 18b.02	111 GND	110 WR BUS CHAR 1-A 18b.03	109 GND	108 WR BUS CHAR 1-8 18b.04	107 GND	106 WR BUS CHAR 1-4 18b.05	105 GND
120 GND	119 WR BUS CHAR 2-2 18a.06	118 GND	117 WR BUS CHAR 2-1 18a.07	116 GND	115 WR BUS CHAR 1-C 18b.01	114 GND	113 SPARE
128 WR BUS CHAR 2-B 18a.02	127 GND	126 WR BUS CHAR 2-A 18a.03	125 GND	124 WR BUS CHAR 2-8 18a.04	123 GND	122 WR BUS CHAR 2-4 18a.05	121 GND
136 GND	135 WR BUS CHAR 3-2 18a.06	134 GND	133 WR BUS CHAR 3-1 18a.07	132 GND	131 WR BUS CHAR 2-C 18a.01	130 GND	129 SPARE
144 WR BUS CHAR 3-B 18a.02	143 GND	142 WR BUS CHAR 3-A 18a.03	141 GND	140 WR BUS CHAR 3-8 18a.04	139 GND	138 WR BUS CHAR 3-4 18a.05	137 GND
152 GND	151 WR BUS CHAR 4-4 18a.05	150 GND	149 WR BUS CHAR 4-2 18a.06	148 GND	147 WR BUS CHAR 4-1 18a.07	146 GND	145 WR BUS CHAR 3-C 18a.01
160 WR BUS CHAR 4-C 18a.01	159 GND	158 WR BUS CHAR 4-B 18a.02	157 GND	156 WR BUS CHAR 4-A 18a.03	155 GND	154 WR BUS CHAR 4-8 18a.04	153 GND

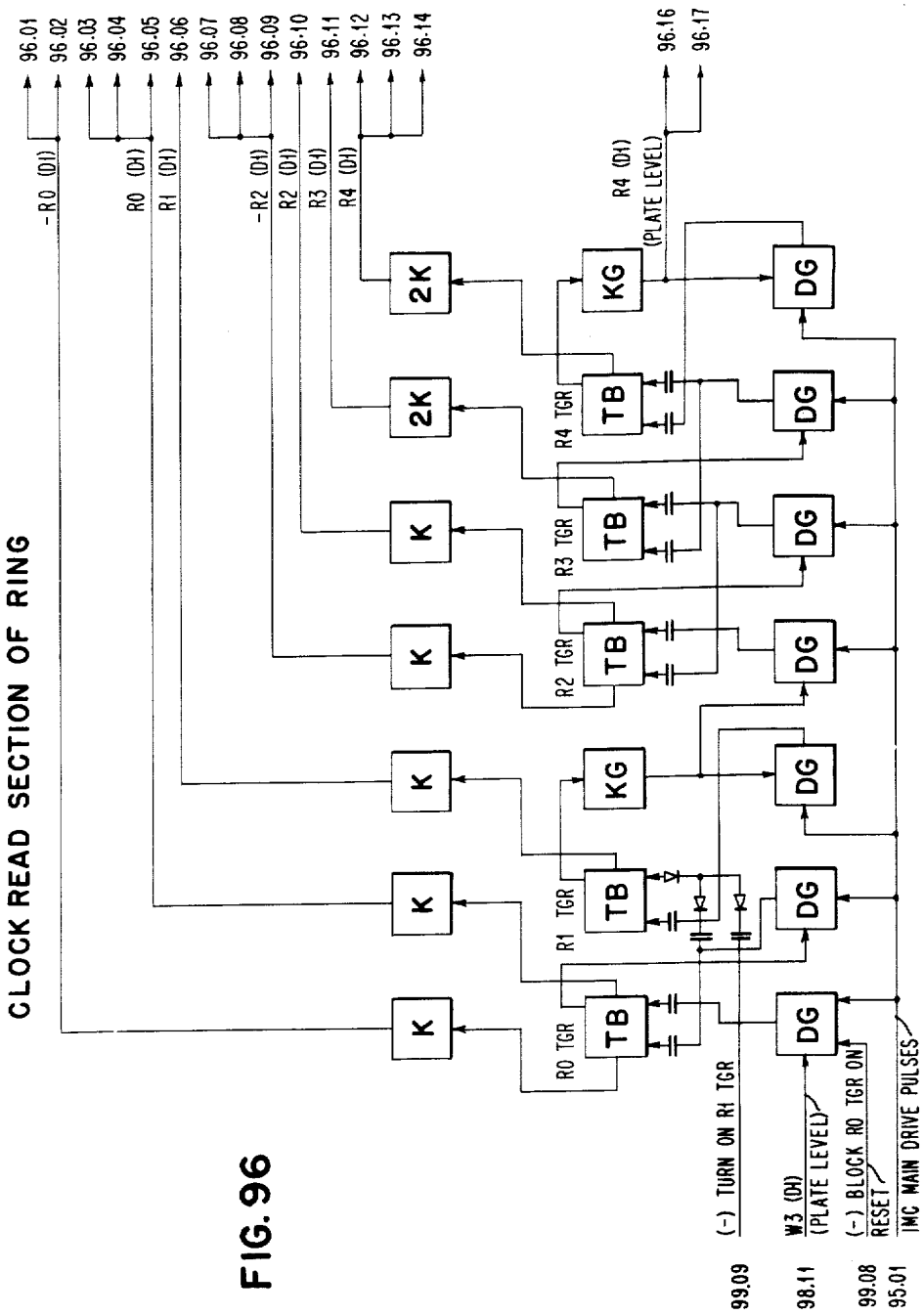

CLOCK READ SECTION OF RING
96.01
96.02
96.03
96.04
96.05
96.06
96.07
96.08
96.09
96.10
96.11
96.12
96.13
96.14
96.16
96.17
-R0 (D1)
R0 (D1)
R1 (D1)
-R2 (D1)
R2 (D1)
R3 (D1)
R4 (D1)
R4 (D1) (PLATE LEVEL)
2K
K
KG
TB
DG
R4 TGR
R3 TGR
R2 TGR
R1 TGR
R0 TGR
(-) TURN ON R1 TGR
W3 (D1) (PLATE LEVEL)
(-) BLOCK R0 TGR ON RESET
IMC MAIN DRIVE PULSES
99.09
98.11
99.08
95.01

FIG. 96

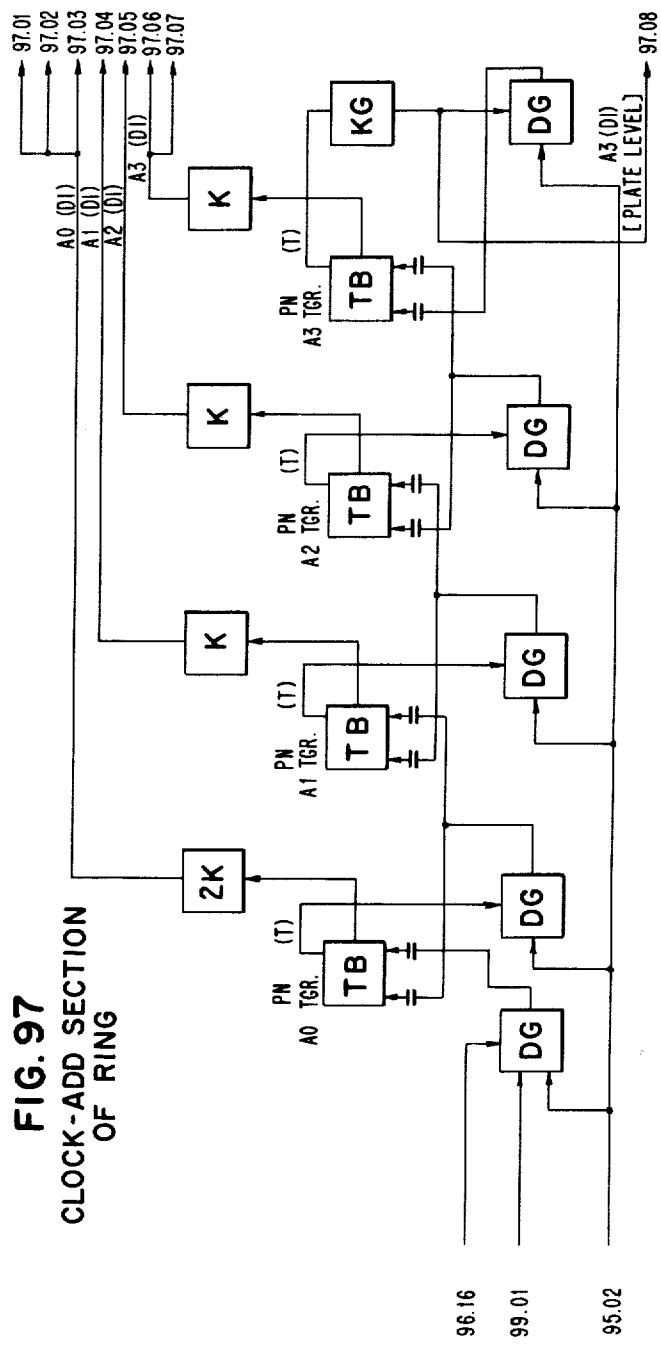


FIG. 97
CLOCK-ADD SECTION OF RING

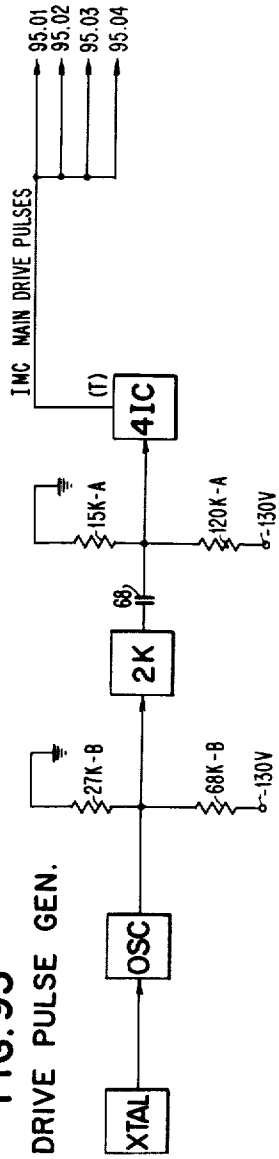


FIG. 95
IMC DRIVE PULSE GEN.

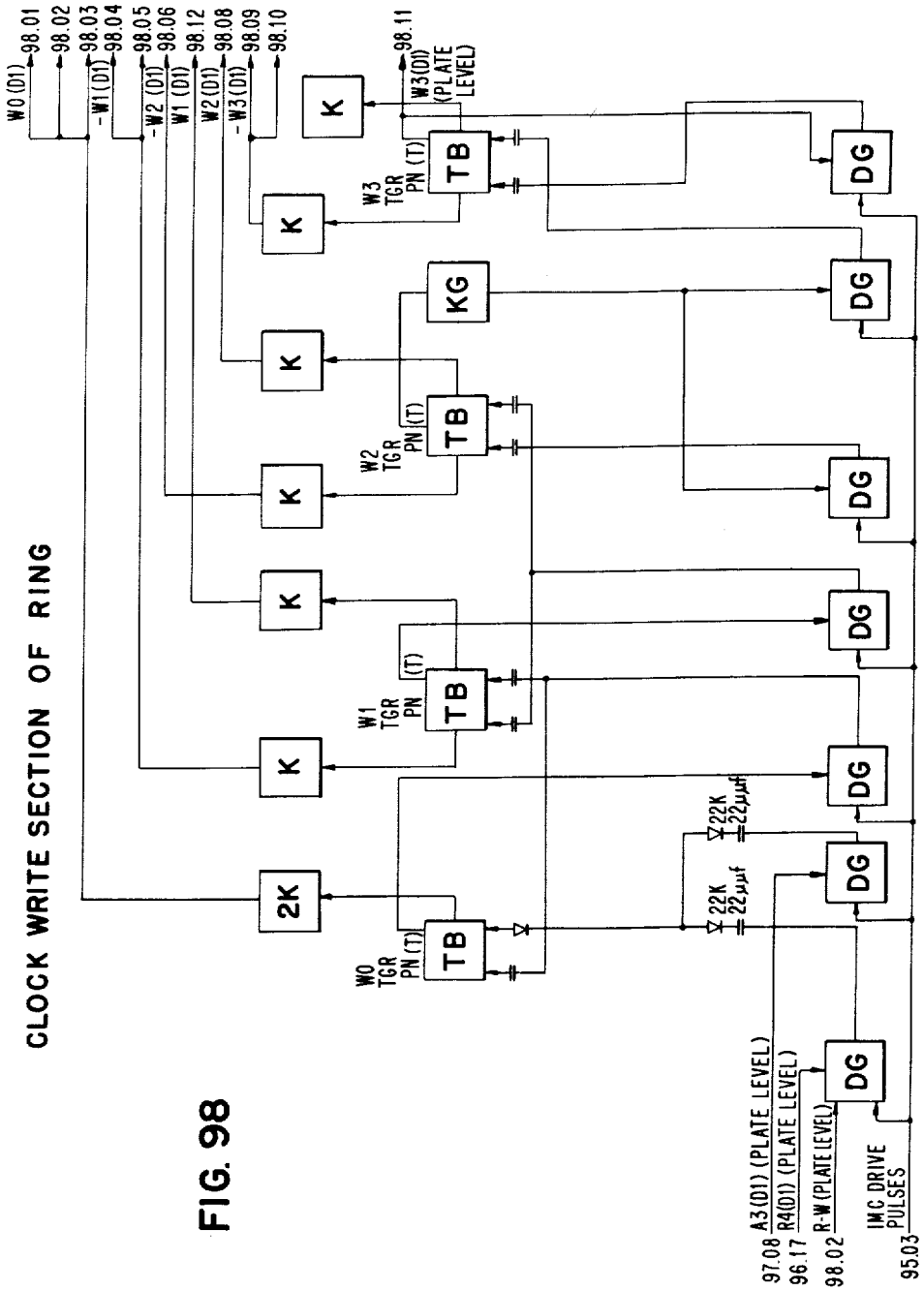

CLOCK WRITE SECTION OF RING
W0 (D1) 98.01
98.02
-W1 (D1) 98.03
98.04
-W2 (D1) 98.05
98.06
W1 (D1) 98.12
W2 (D1) 98.08
-W3 (D1) 98.09
98.10
W3 (D1) (PLATE LEVEL) 98.11
K
KG
2K
TB
DG
W3 TGR PN (T)
W2 TGR PN (T)
W1 TGR PN (T)
W0 TGR PN (T)
22K
22μμf
97.08 A3 (D1) (PLATE LEVEL)
96.17 R4 (D1) (PLATE LEVEL)
98.02 R-W (PLATE LEVEL)
IMC DRIVE PULSES 95.03

FIG. 98

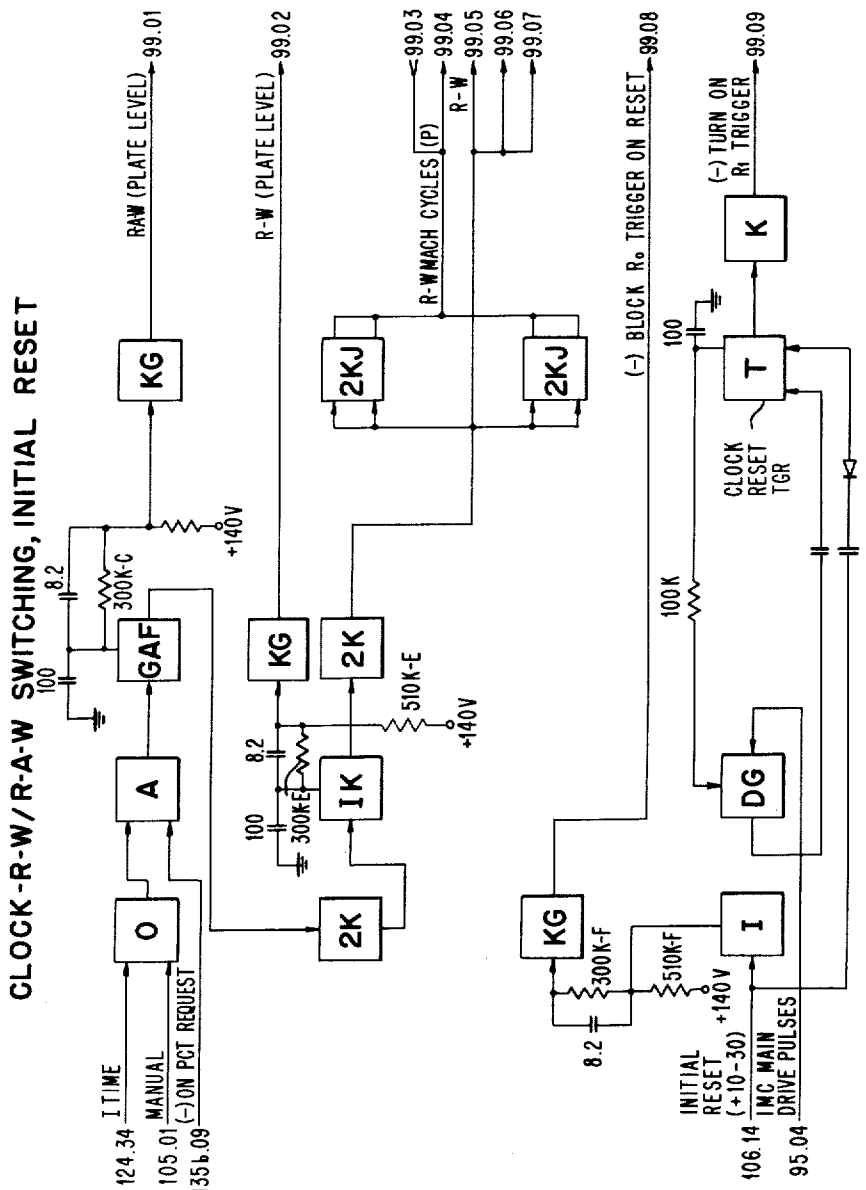

CLOCK-R-W/R-A-W SWITCHING, INITIAL RESET
124.34 ITIME
105.01 MANUAL
135b.09 (-)ON PCT REQUEST
O
A
GAF
KG
RAW (PLATE LEVEL) 99.01
+140V
300K-C
8.2
100
R-W (PLATE LEVEL) 99.02
KG
2K
IK
2K
510K-E
+140V
300K-E
8.2
100
99.03
99.04
99.05
99.06
99.07
R-W MACH CYCLES (P)
R-W
2KJ
2KJ
(-) BLOCK Ro TRIGGER ON RESET 99.08
KG
300K-F
510K-F
+140V
8.2
INITIAL RESET (+10-30) 106.14
IMC MAIN DRIVE PULSES 95.04
I
DG
100K
T
CLOCK RESET TGR
100
K
(-) TURN ON R1 TRIGGER 99.09

FIG. 99

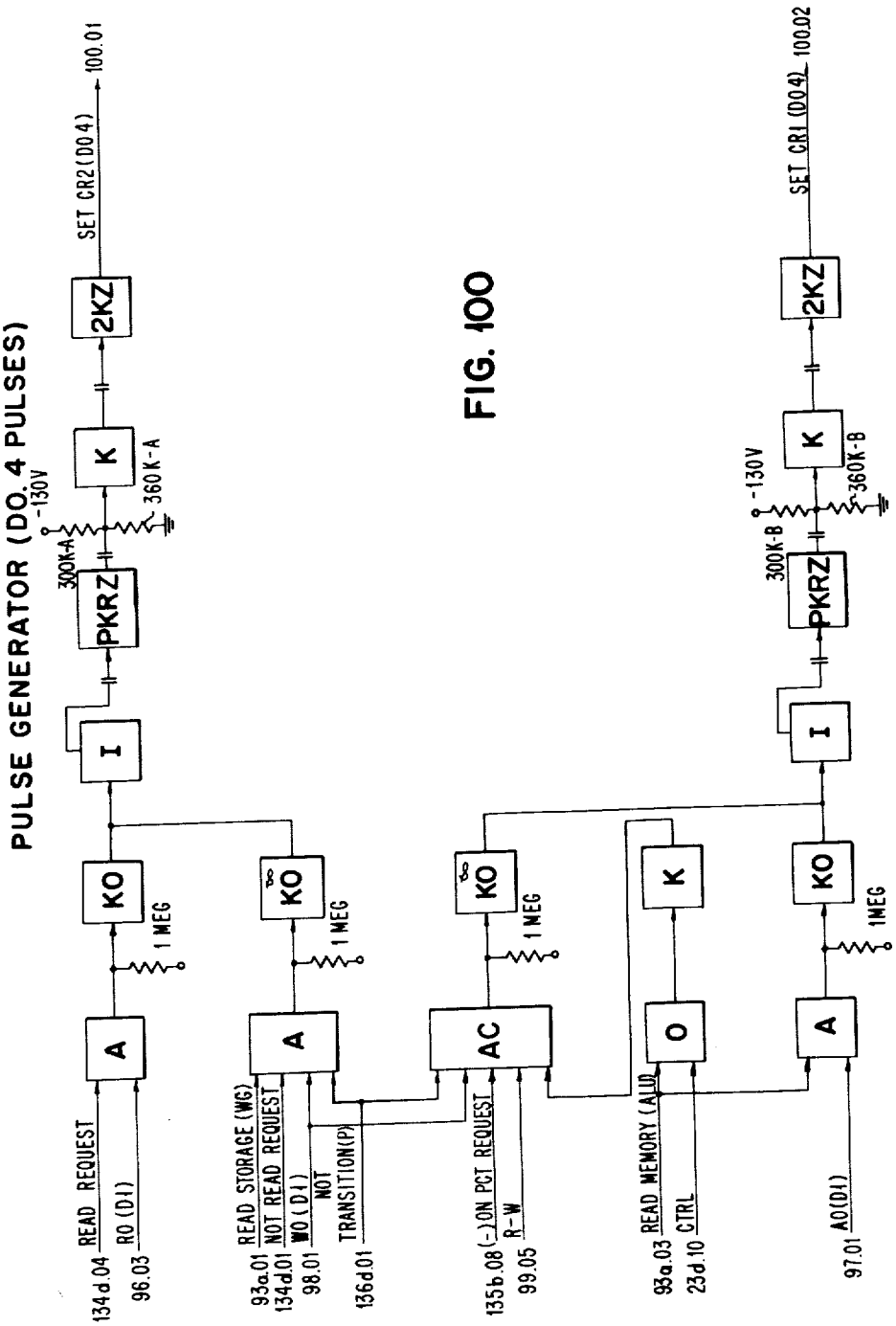
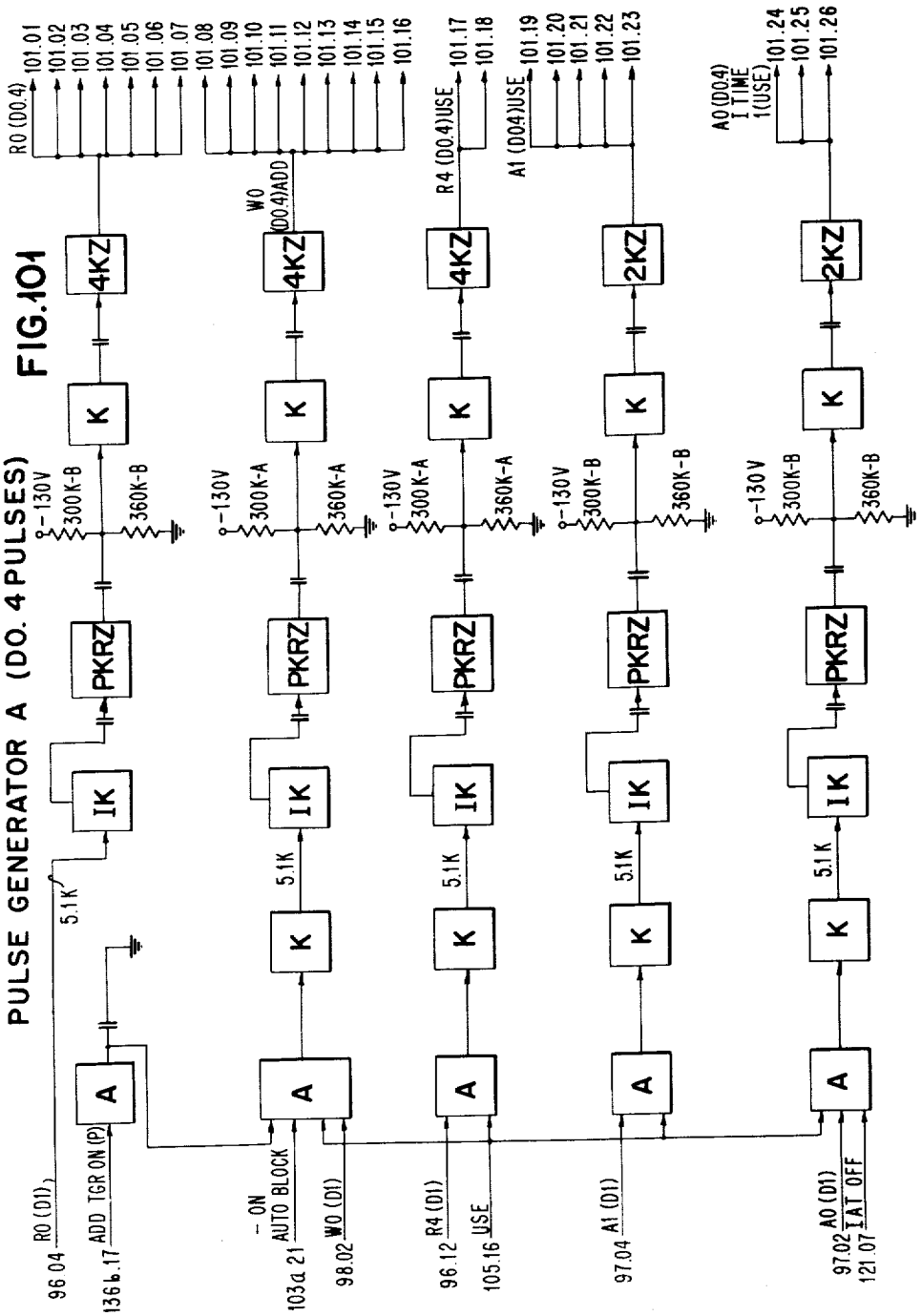

PULSE GENERATOR (DO 4 PULSES)
SET CR2 (DO 4) 100.01
SET CR1 (DO 4) 100.02
2KZ
K
360 K-A
360 K-B
300K-A
300K-B
-130V
PKRZ
I
KO
1 MEG
A
AC
O
READ REQUEST
RO (D1)
96.03
134d.04
READ STORAGE (WG)
NOT READ REQUEST
WO (D1)
NOT TRANSITION (P)
93a.01
134d.01
98.01
136d.01
(-) ON PCT REQUEST
R-W
135b.08
99.05
READ MEMORY (ALU)
CTRL
93a.03
23d.10
AO (D1)
97.01

FIG. 100

FIG. 101


PULSE GENERATOR A (DO. 4 PULSES)
R0 (D0.4)
101.01
101.02
101.03
101.04
101.05
101.06
101.07
101.08
101.09
101.10
101.11
101.12
101.13
101.14
101.15
101.16
W0 (D0.4)ADD
R4 (D0.4)USE
101.17
101.18
A1 (D0.4)USE
101.19
101.20
101.21
101.22
101.23
A0 (D0.4) I TIME 1(USE)
101.24
101.25
101.26
4KZ
2KZ
K
PKRZ
IK
5.1K
300K-B
360K-B
300K-A
360K-A
-130 V
A
96.04 R0 (D1)
136 b.17 ADD TGR ON (P)
103 a.21 - ON AUTO BLOCK
98.02 W0 (D1)
96.12 R4 (D1)
105.16 USE
97.04 A1 (D1)
97.02 A0 (D1)
121.07 IAT OFF

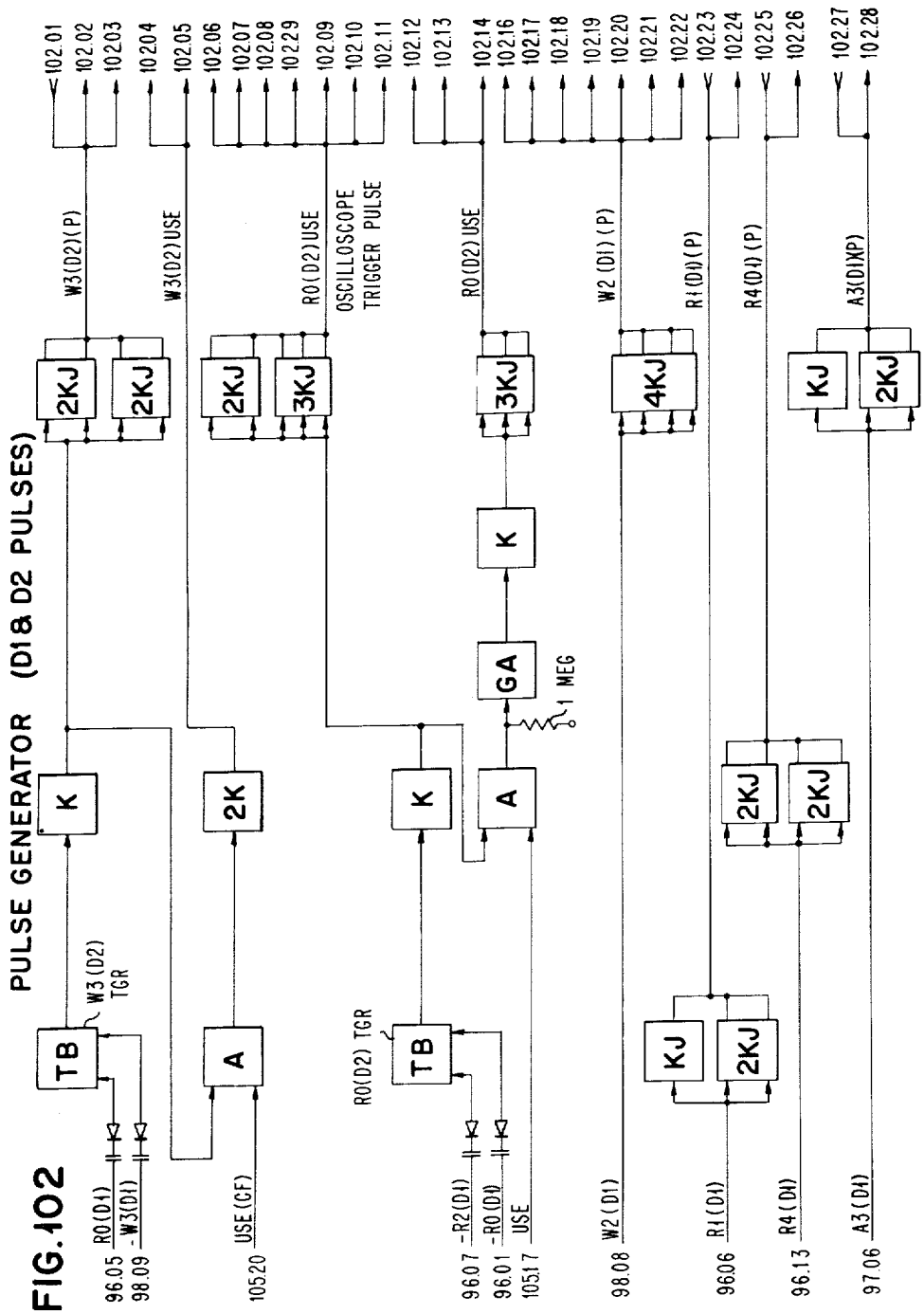

PULSE GENERATOR (D1& D2 PULSES)
102.01
102.02
102.03
102.04
102.05
102.06
102.07
102.08
102.09
102.10
102.11
102.12
102.13
102.14
102.16
102.17
102.18
102.19
102.20
102.21
102.22
102.23
102.24
102.25
102.26
102.27
102.28
W3(D2)(P)
W3(D2)USE
RO(D2)USE
OSCILLOSCOPE TRIGGER PULSE
RO(D2)USE
W2(D1)(P)
R1(D1)(P)
R4(D4)(P)
A3(D1XP)
2KJ
2KJ
2KJ
3KJ
3KJ
4KJ
KJ
2KJ
K
2K
K
A
GA
1 MEG
TB
A
TB
KJ
2KJ
2KJ
2KJ
W3(D2) TGR
RO(D2) TGR
96.05 RO(D1)
98.09 -W3(D1)
105.20 USE(CF)
96.07 -R2(D1)
96.01 -RO(D1)
105.17 USE
98.08 W2(D1)
96.06 R1(D1)
96.13 R4(D1)
97.06 A3(D1)

FIG. 102

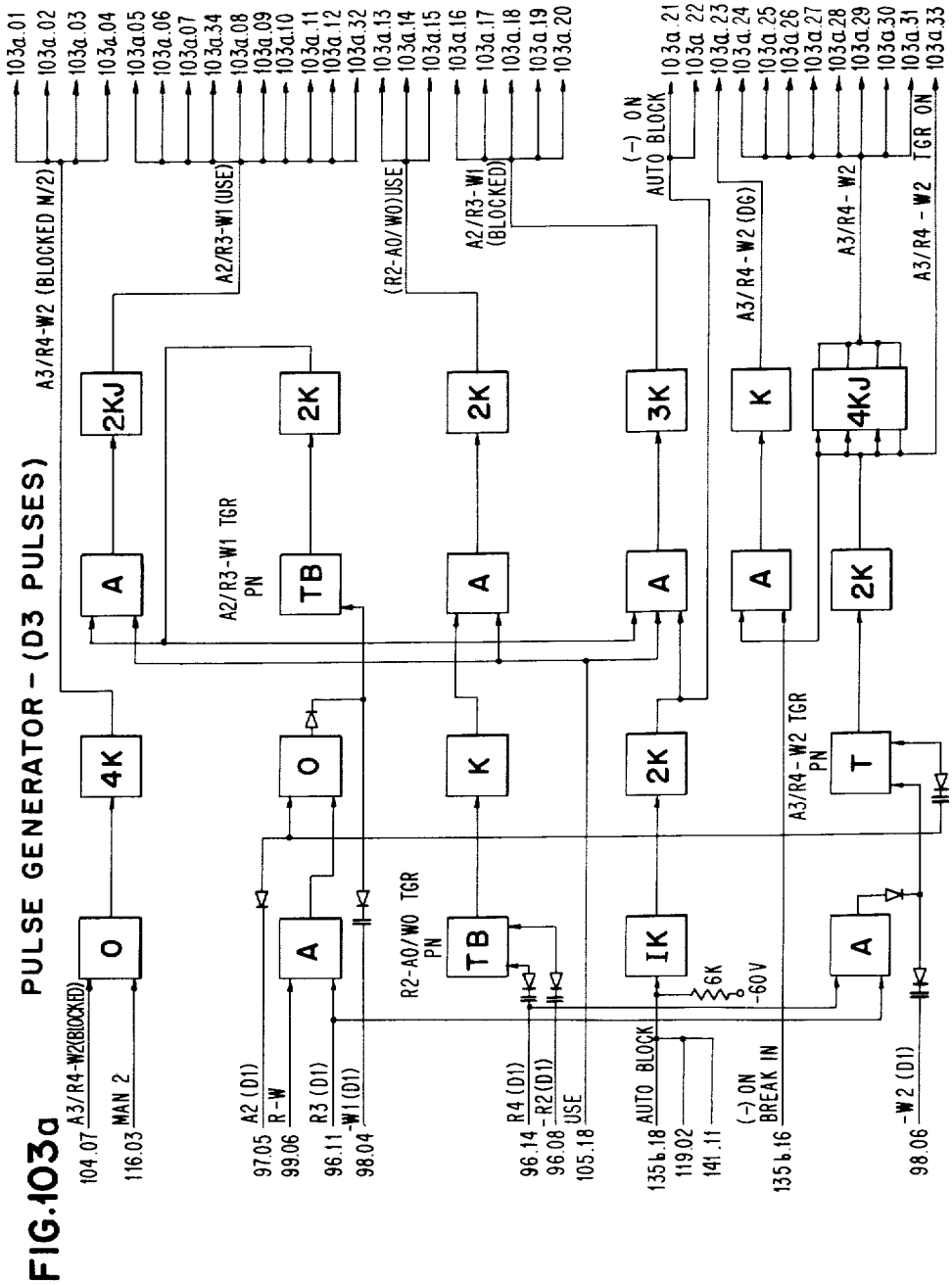
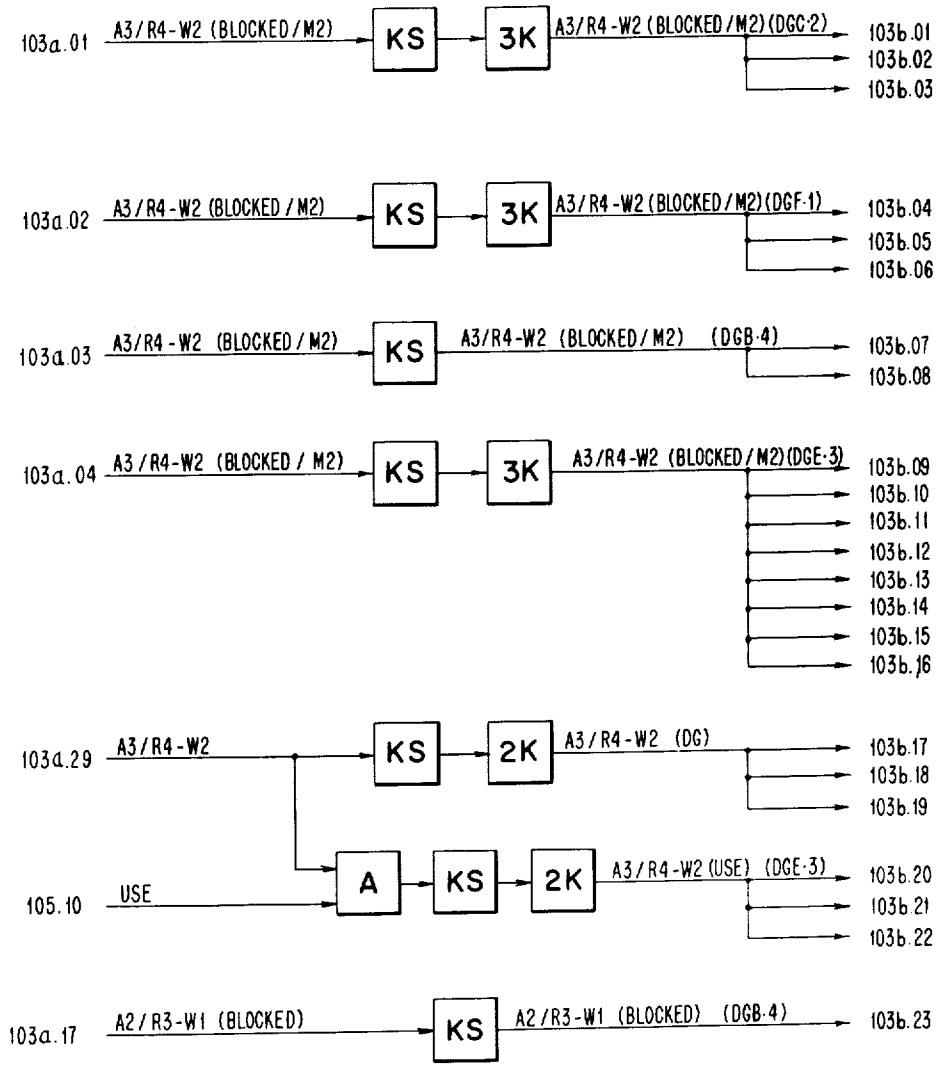

PULSE GENERATOR - (D3 PULSES)
103a.01
103a.02
103a.03
103a.04
103a.05
103a.06
103a.07
103a.34
103a.08
103a.09
103a.10
103a.11
103a.12
103a.32
103a.13
103a.14
103a.15
103a.16
103a.17
103a.18
103a.19
103a.20
103a.21
103a.22
103a.23
103a.24
103a.25
103a.26
103a.27
103a.28
103a.29
103a.30
103a.31
103a.33
A3/R4-W2 (BLOCKED W/2)
A2/R3-W1 (USE)
(R2-A0/W0)USE
A2/R3-W1 (BLOCKED)
(-) ON AUTO BLOCK
A3/R4-W2 (DG)
A3/R4-W2
A3/R4-W2 TGR ON
2KJ
2K
2K
3K
K
4KJ
A
TB
A
A
A
2K
A2/R3-W1 TGR PN
4K
O
K
2K
T
A3/R4-W2 TGR PN
O
A
TB
IK
A
R2-A0/W0 TGR PN
6K
-60 V
104.07 A3/R4-W2(BLOCKED)
116.03 MAN 2
97.05 A2 (D1)
99.06 R-W
96.11 R3 (D1)
98.04 -W1 (D1)
96.14 R4 (D1)
96.08 -R2 (D1)
105.18 USE
135b.18 AUTO BLOCK
119.02
141.11
(-) ON BREAK IN
135b.16
98.06 -W2 (D1)

FIG. 103a

FIG. 103b

C.F. PULSE POWER



PULSE GENERATOR (D3 & D4 PULSES)

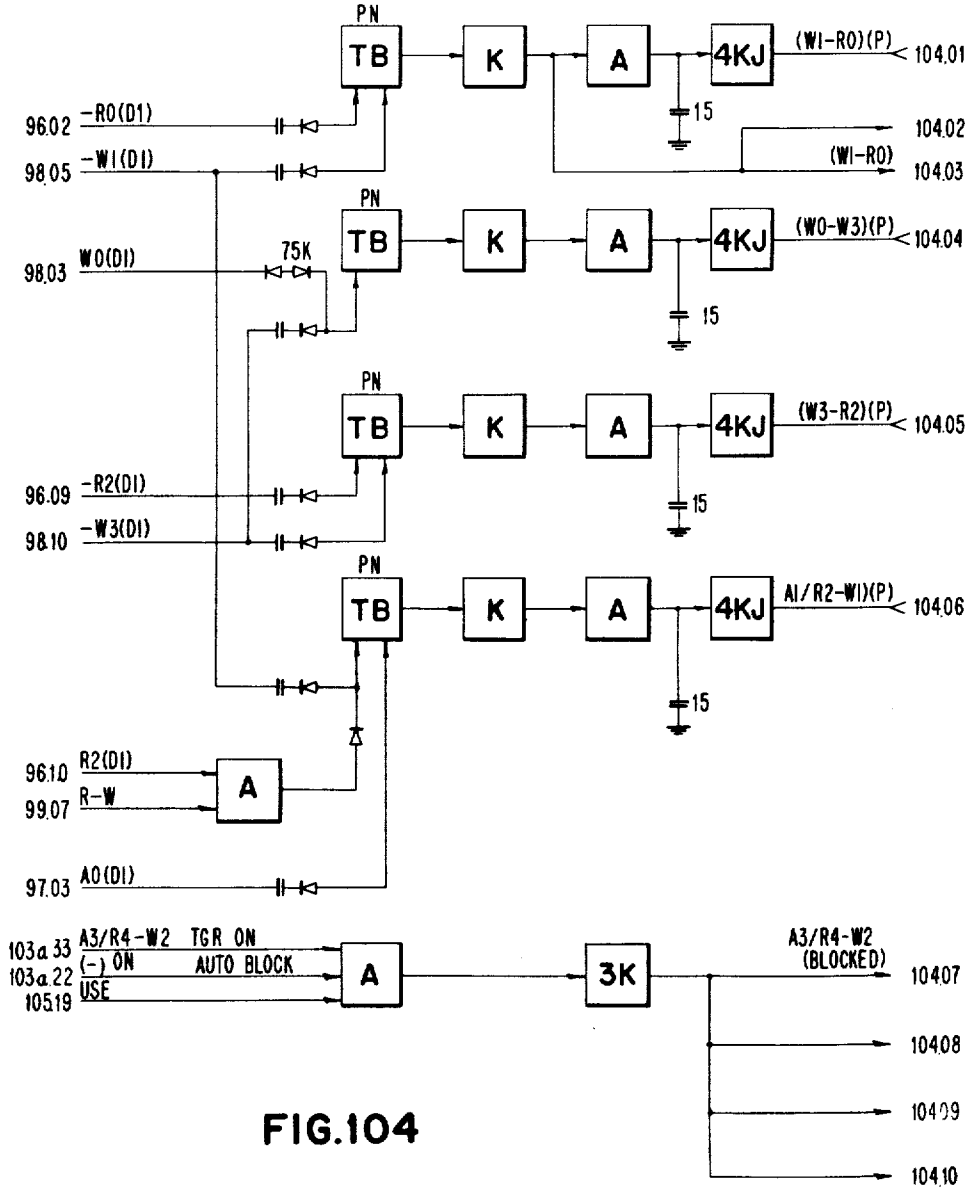


FIG.104

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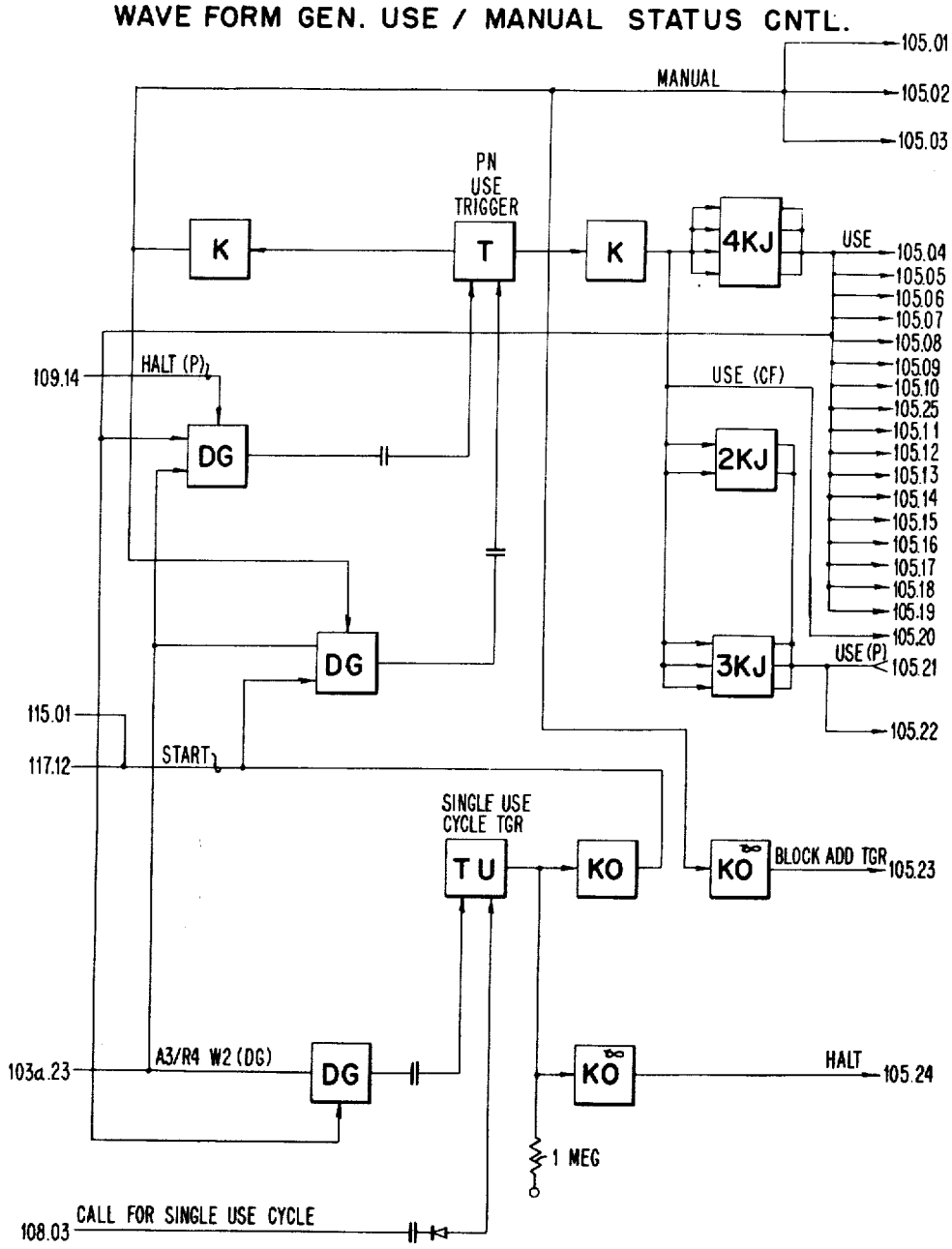


FIG. 105

FIG. 106 MANUAL RESET KEYS

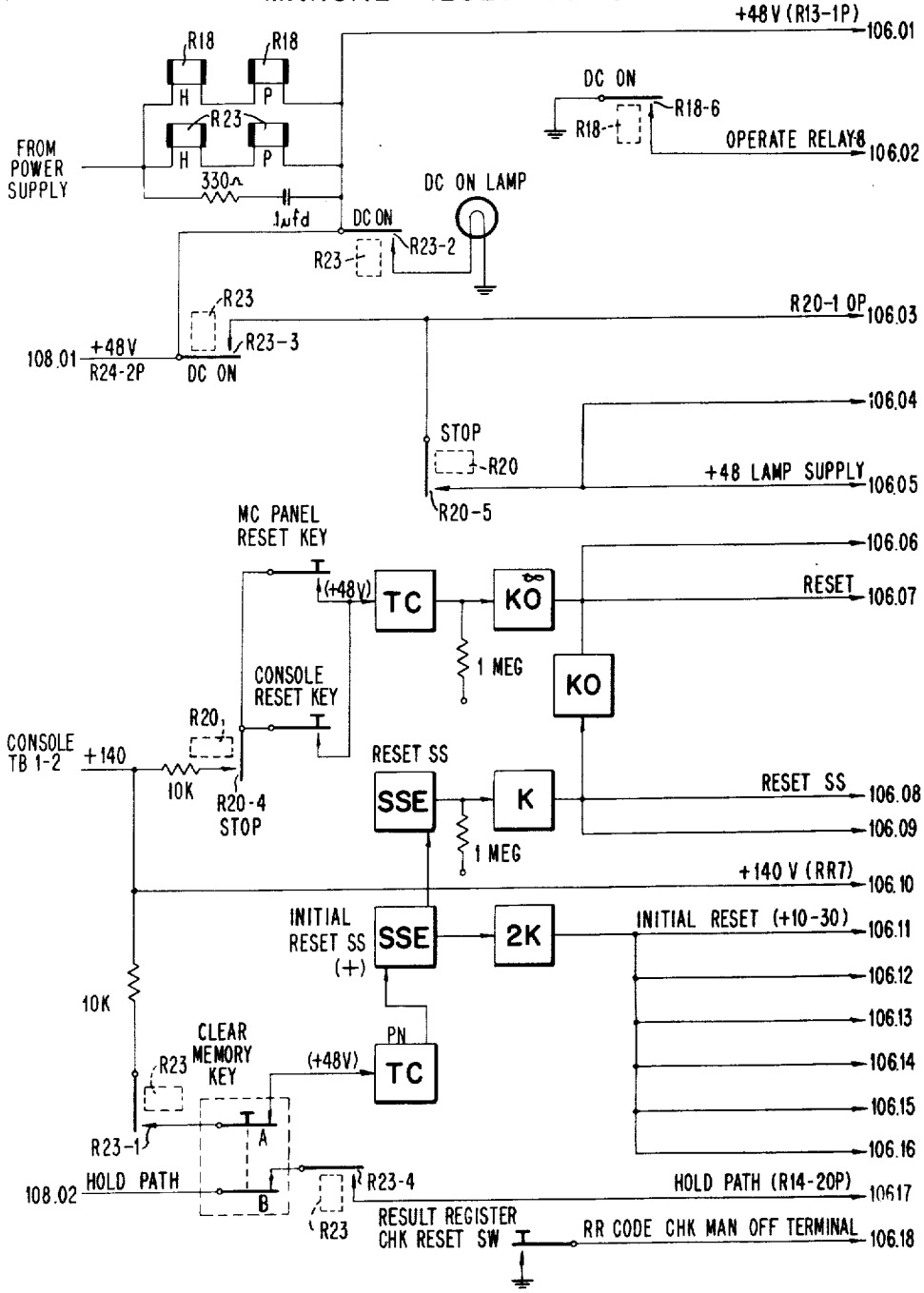
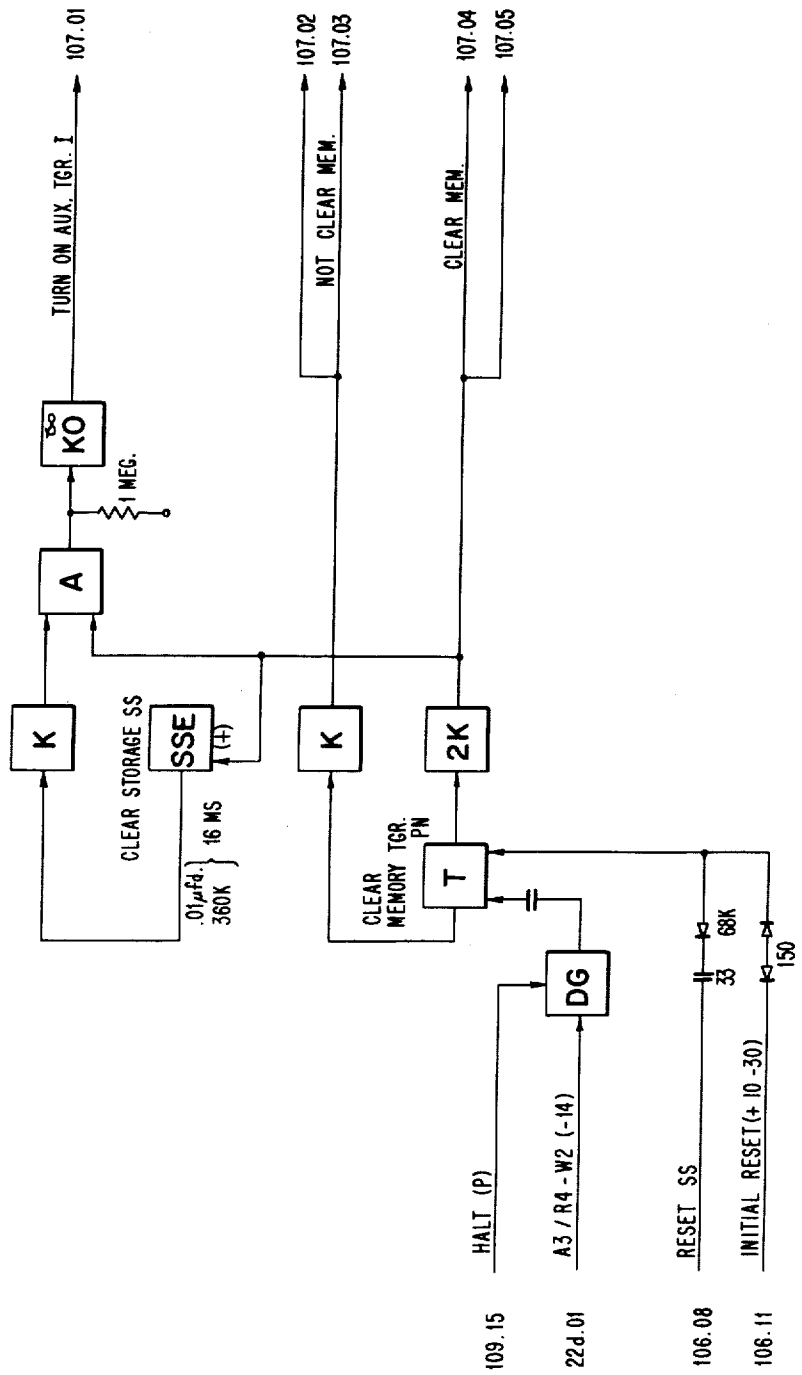


FIG. 107
CLEAR MEMORY TRIGGER



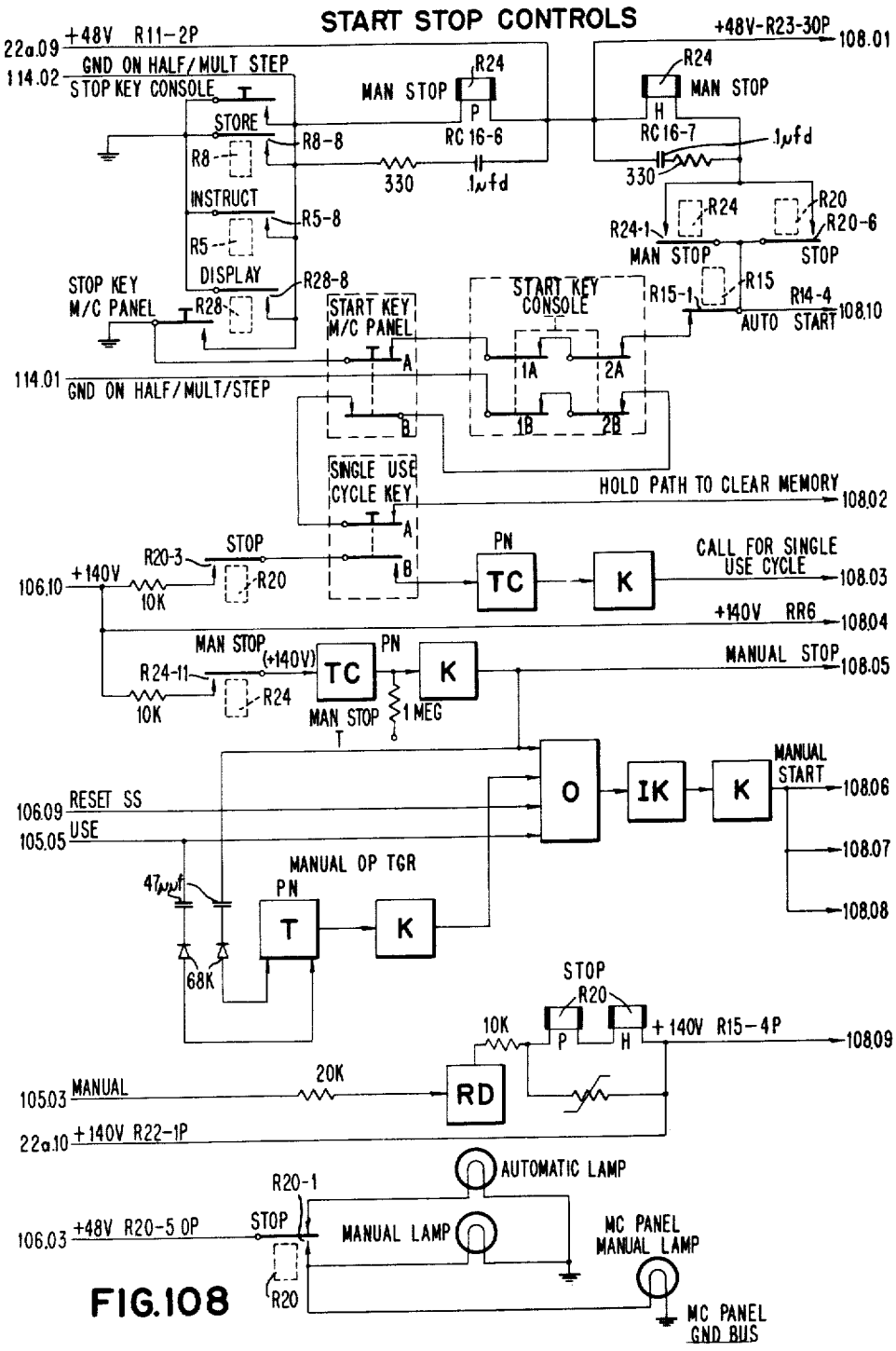

START STOP CONTROLS
22a.09 +48V R11-2P
114.02 GND ON HALF/MULT STEP
STOP KEY CONSOLE
STORE
R8
R8-8
INSTRUCT
R5
R5-8
DISPLAY
R28
R28-8
STOP KEY M/C PANEL
MAN STOP
R24
P
RC 16-6
330
.1μfd
+48V-R23-30P
108.01
H
RC 16-7
R24-1
R20
R20-6
STOP
START KEY M/C PANEL
START KEY CONSOLE
R15-1
R15
R14-4
AUTO START
108.10
114.01 GND ON HALF/MULT/STEP
1A
2A
1B
2B
SINGLE USE CYCLE KEY
HOLD PATH TO CLEAR MEMORY
108.02
R20-3
106.10 +140V
10K
PN
TC
K
CALL FOR SINGLE USE CYCLE
108.03
+140V RR6
108.04
MAN STOP
(+140V)
R24-11
MANUAL STOP
108.05
1 MEG
106.09 RESET SS
105.05 USE
O
IK
MANUAL START
108.06
108.07
108.08
MANUAL OP TGR
47μμf
T
68K
STOP
10K
+140V R15-4P
108.09
105.03 MANUAL
20K
RD
22a.10 +140V R22-1P
AUTOMATIC LAMP
R20-1
106.03 +48V R20-5 0P
MANUAL LAMP
MC PANEL MANUAL LAMP
MC PANEL GND BUS

FIG.108

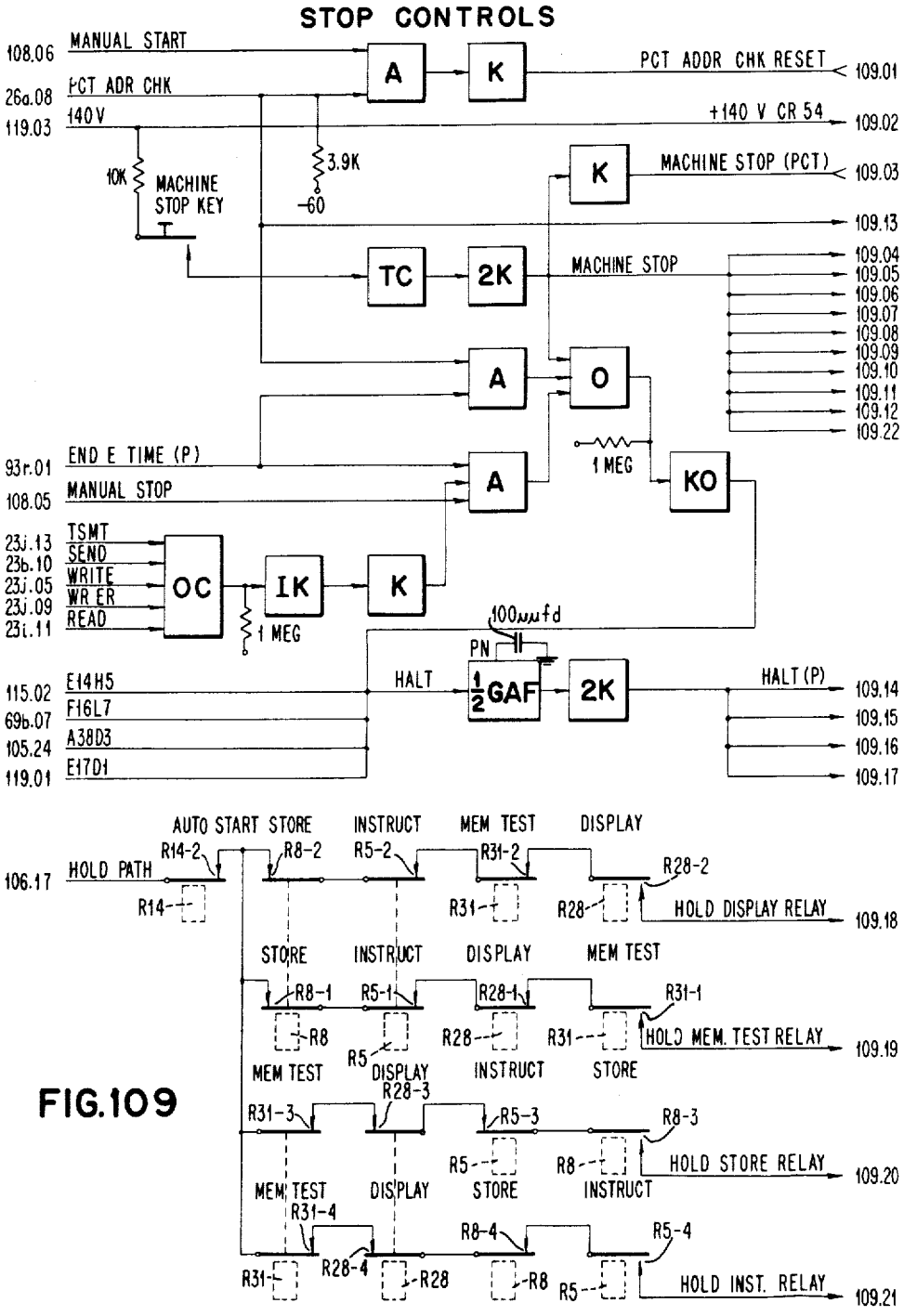

STOP CONTROLS
108.06 MANUAL START
26a.08 PCT ADR CHK
119.03 140V
10K MACHINE STOP KEY
3.9K
-60
A
K
PCT ADDR CHK RESET
109.01
+140 V CR 54
109.02
MACHINE STOP (PCT)
109.03
109.13
TC
2K
MACHINE STOP
109.04
109.05
109.06
109.07
109.08
109.09
109.10
109.11
109.12
109.22
O
1 MEG
KO
93r.01 END E TIME (P)
108.05 MANUAL STOP
23j.13 TSMT
23b.10 SEND
23j.05 WRITE
23j.09 WR ER
23i.11 READ
OC
IK
1 MEG
100μμfd
PN
115.02 E14H5
69b.07 F16L7
105.24 A38D3
119.01 E17D1
HALT
½GAF
HALT (P)
109.14
109.15
109.16
109.17
106.17 HOLD PATH
AUTO START STORE
INSTRUCT
MEM TEST
DISPLAY
R14-2
R8-2
R5-2
R31-2
R28-2
R14
R31
R28
HOLD DISPLAY RELAY
109.18
STORE
INSTRUCT
DISPLAY
MEM TEST
R8-1
R5-1
R28-1
R31-1
R8
R5
R28
R31
HOLD MEM. TEST RELAY
109.19
MEM TEST
DISPLAY
INSTRUCT
STORE
R28-3
R31-3
R5-3
R8-3
R5
R8
HOLD STORE RELAY
109.20
MEM TEST
DISPLAY
STORE
INSTRUCT
R31-4
R8-4
R5-4
R28-4
R31
R28
R8
R5
HOLD INST. RELAY
109.21

FIG.109

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MANUAL STORE CONTROLS

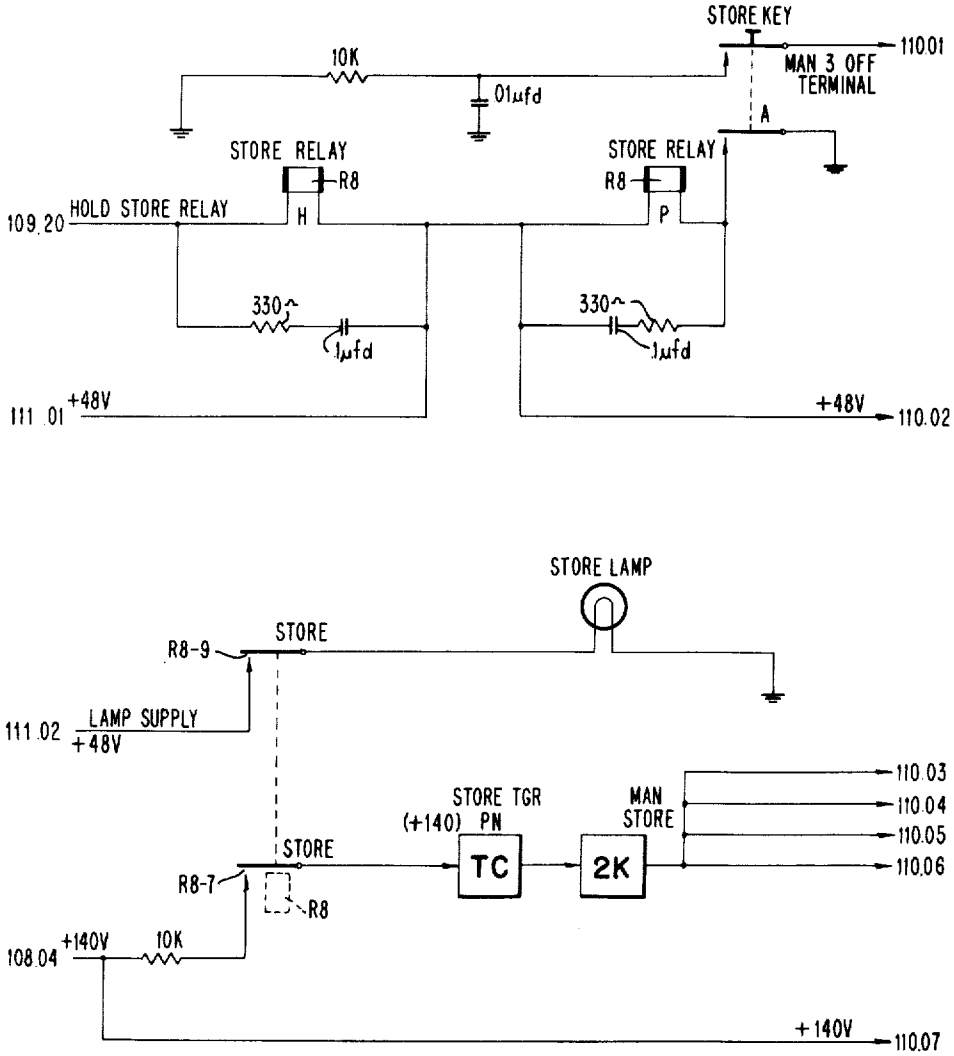


FIG. 110

FIG. 111

MANUAL INSTRUCTION CONTROLS

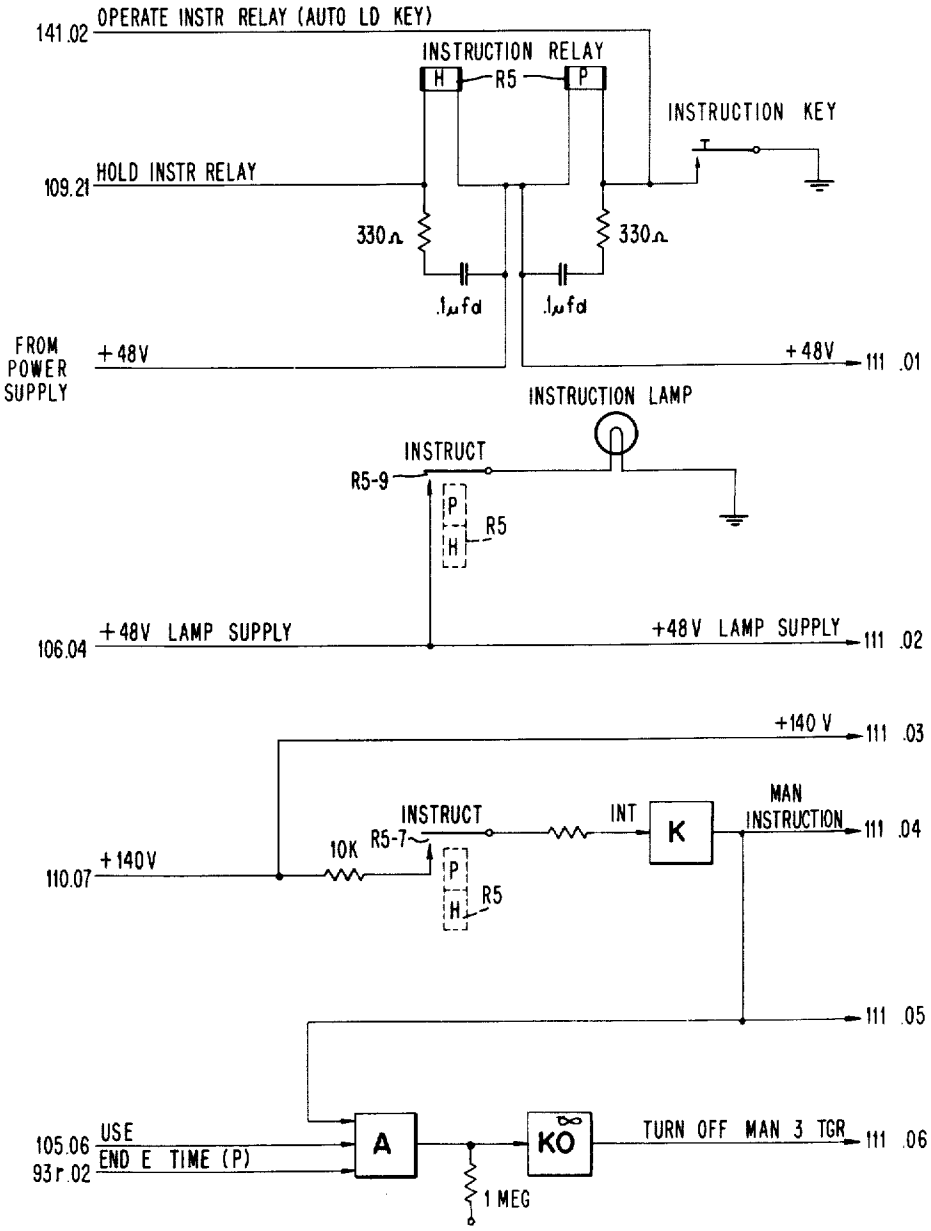
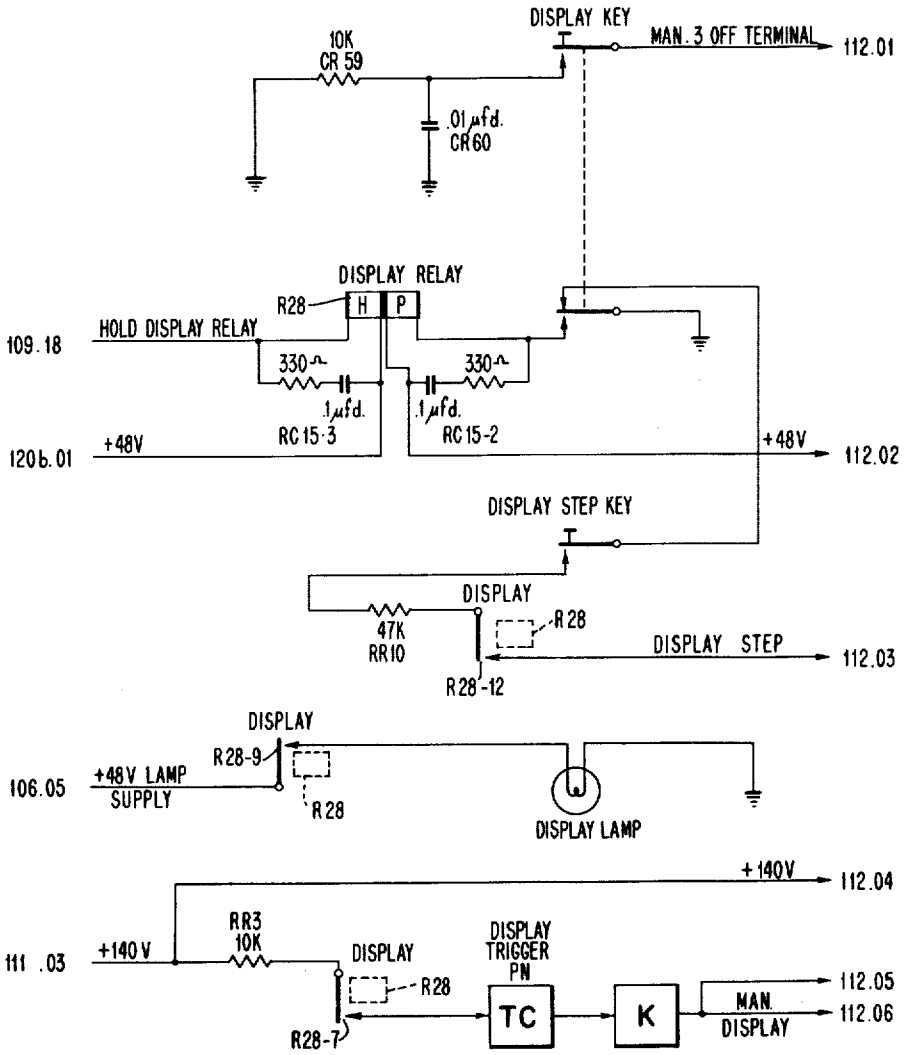


FIG. 112
MANUAL DISPLAY CONTROLS



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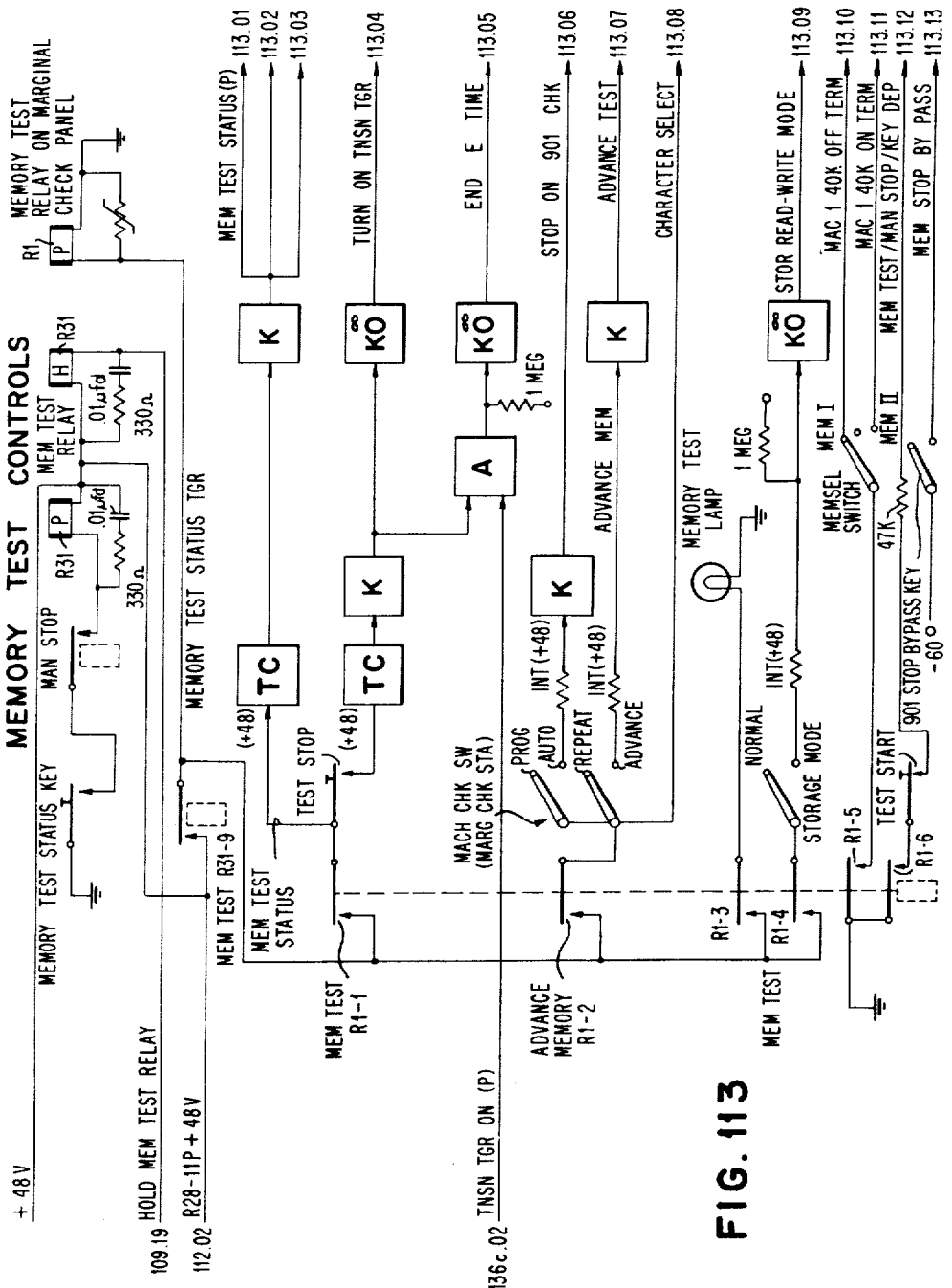


FIG. 113

FIG. 114
HALF / MULTIPLE STEP CONTROLS

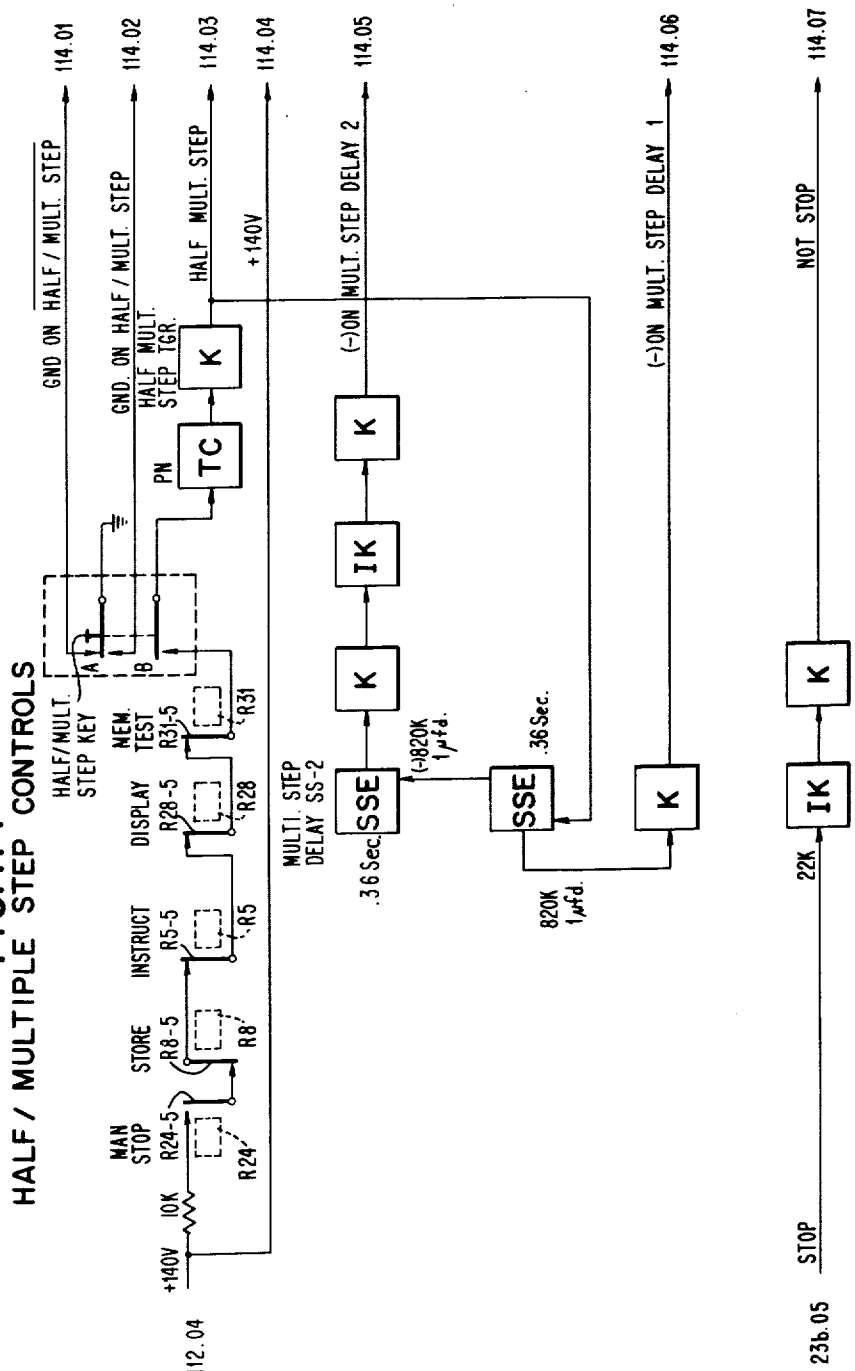
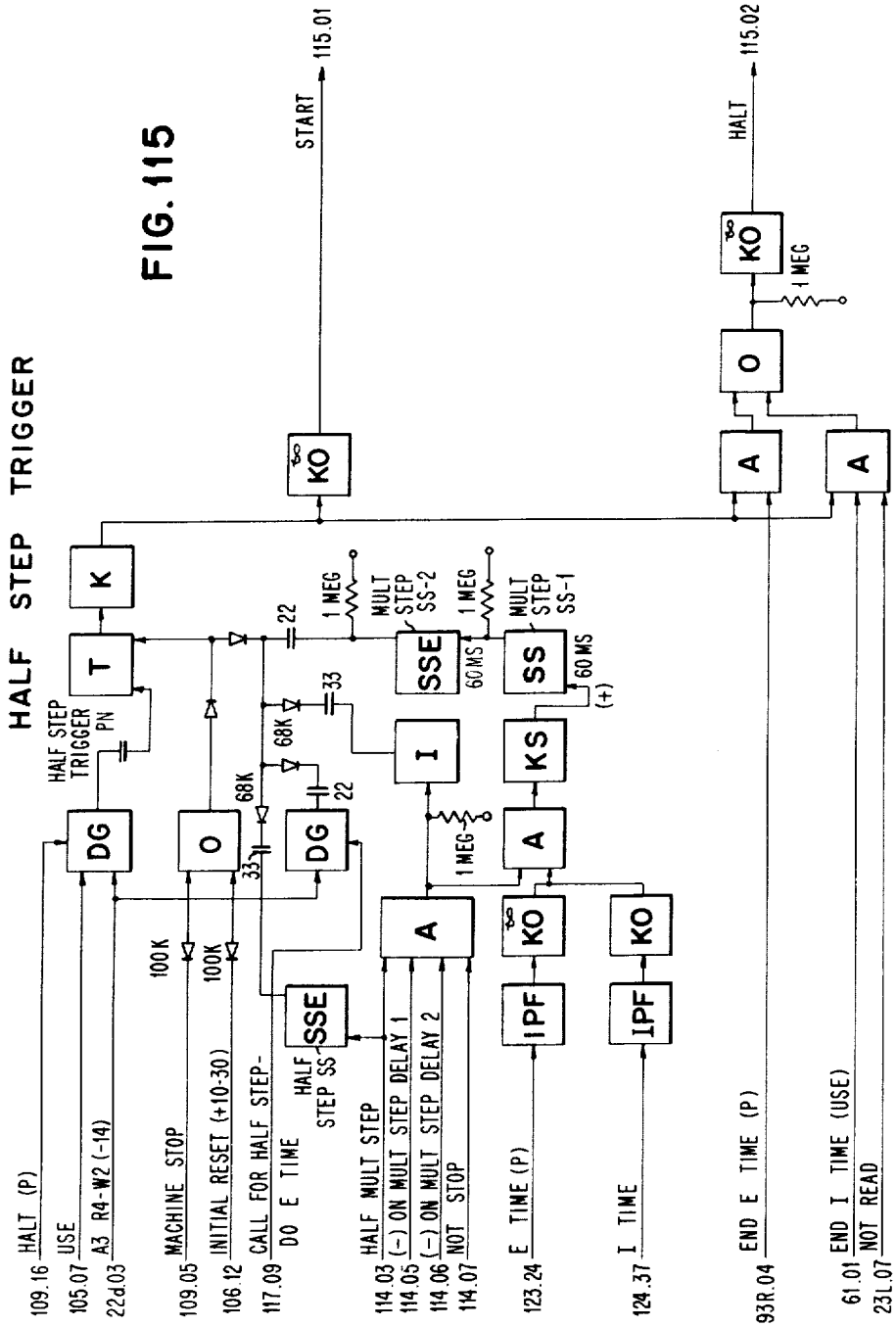


FIG. 115


HALF STEP TRIGGER
START 115.01
HALT 115.02
HALF STEP TRIGGER PN
MULT STEP SS-2
MULT STEP SS-1
60 MS
(+)
1 MEG
68K
100K
33
22
HALT (P) 109.16
USE 105.07
A3 R4-W2 (-14) 22d.03
MACHINE STOP 109.05
INITIAL RESET (+10-30) 106.12
CALL FOR HALF STEP-DO E TIME 117.09
HALF STEP SS
HALF MULT STEP 114.03
(-) ON MULT STEP DELAY 1 114.05
(-) ON MULT STEP DELAY 2 114.06
NOT STOP 114.07
E TIME (P) 123.24
I TIME 124.37
END E TIME (P) 93R.04
END I TIME (USE) 61.01
NOT READ 231.07

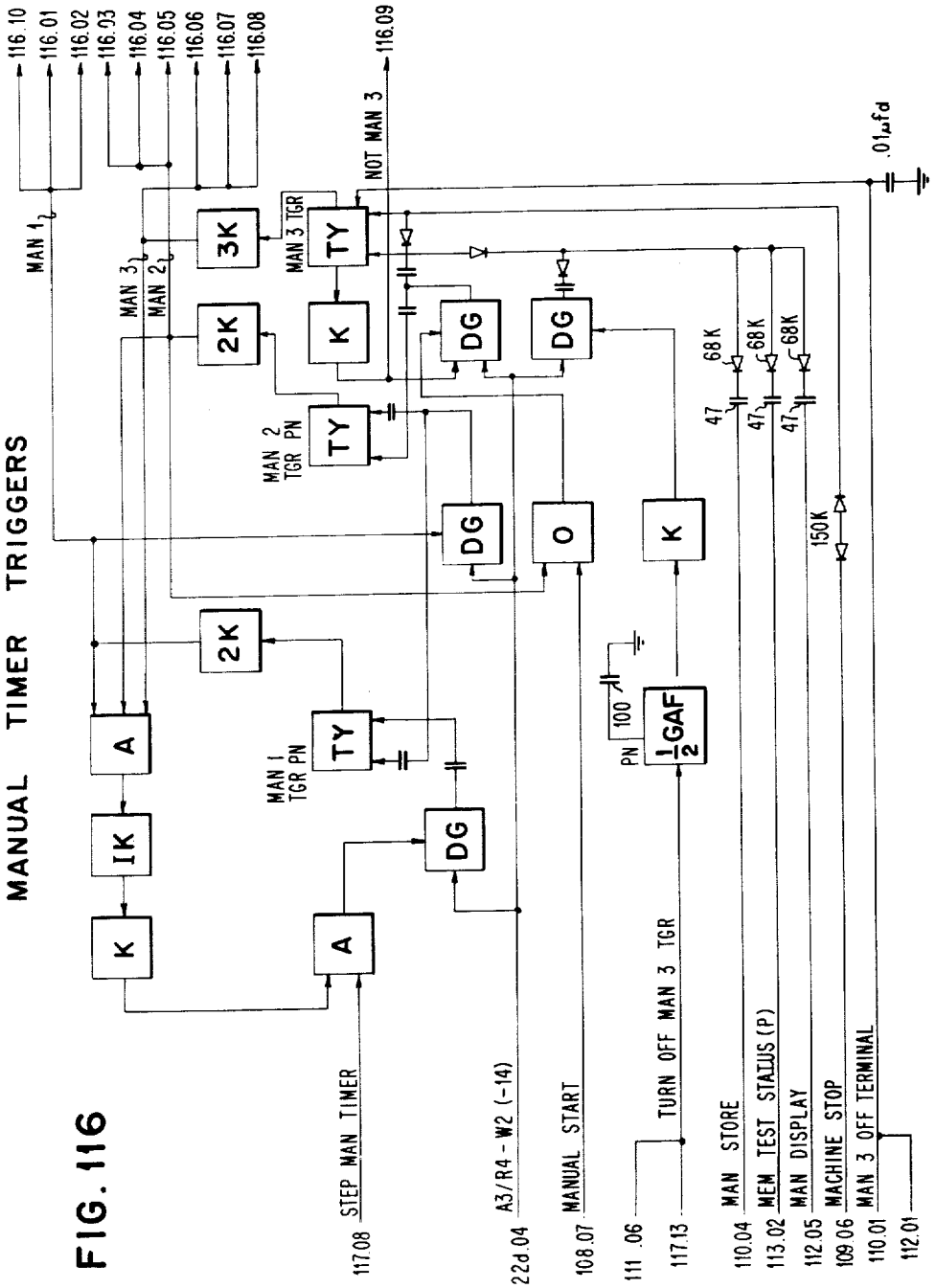

MANUAL TIMER TRIGGERS
116.10
116.01
116.02
116.03
116.04
116.05
116.06
116.07
116.08
116.09
NOT MAN 3
.01μfd
MAN 1
MAN 3
MAN 2
3K
2K
K
TY
MAN 3 TGR
DG
DG
68K
68K
68K
47
47
47
MAN 2 TGR PN
DG
O
K
150K
2K
A
IK
K
TY
MAN 1 TGR PN
DG
A
100
PN
½GAF
STEP MAN TIMER
117.08
A3/R4-W2 (-14)
22d.04
MANUAL START
108.07
TURN OFF MAN 3 TGR
111 .06
117.13
MAN STORE
110.04
MEM TEST STATUS (P)
113.02
MAN DISPLAY
112.05
MACHINE STOP
109.06
MAN 3 OFF TERMINAL
110.01
112.01

FIG. 116

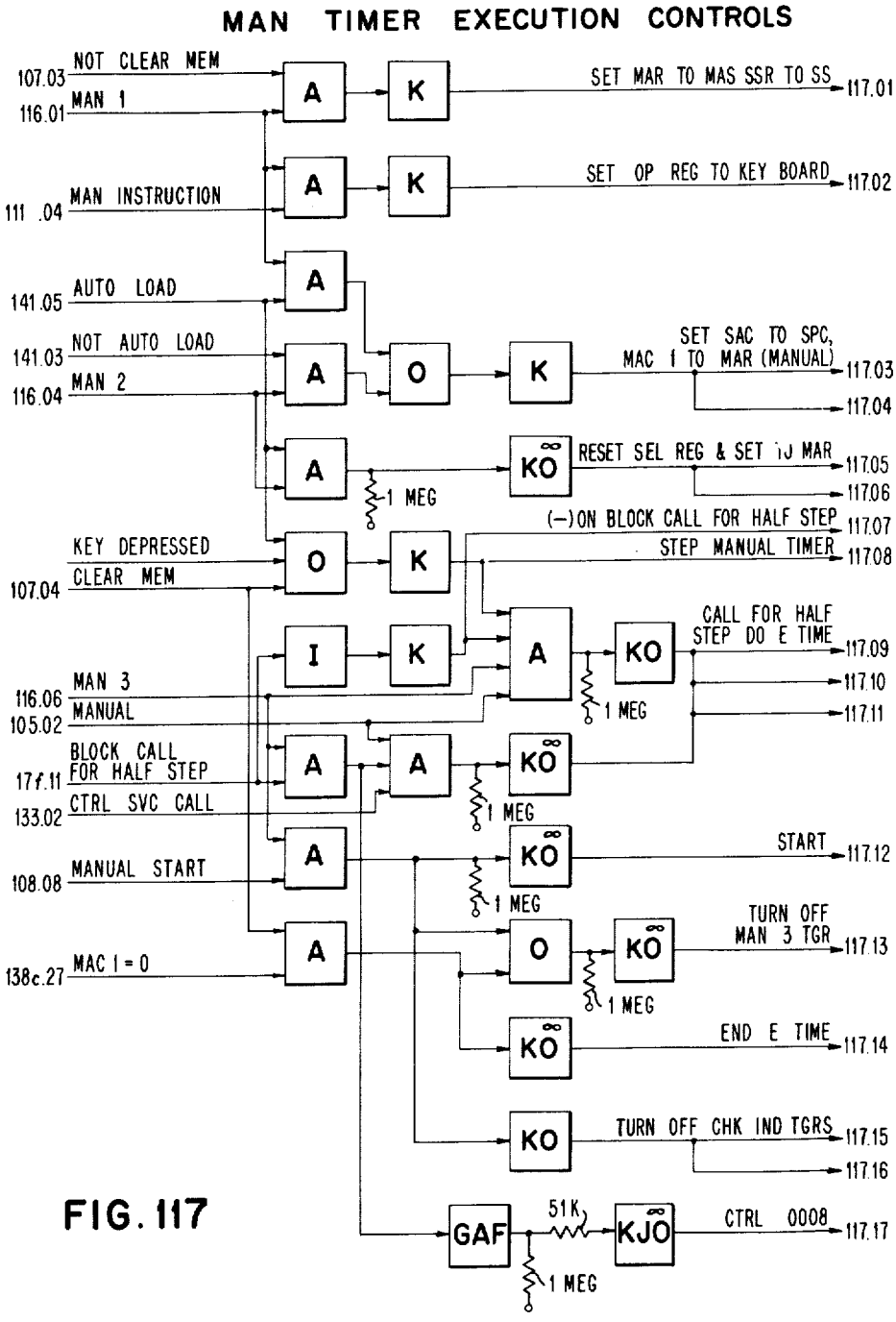

MAN TIMER EXECUTION CONTROLS
107.03 NOT CLEAR MEM
116.01 MAN 1
A
K
SET MAR TO MAS SSR TO SS 117.01
111 .04 MAN INSTRUCTION
SET OP REG TO KEY BOARD 117.02
141.05 AUTO LOAD
141.03 NOT AUTO LOAD
116.04 MAN 2
O
SET SAC TO SPC, MAC 1 TO MAR (MANUAL) 117.03 117.04
KO
RESET SEL REG & SET TO MAR 117.05 117.06
1 MEG
(-)ON BLOCK CALL FOR HALF STEP 117.07
KEY DEPRESSED
107.04 CLEAR MEM
STEP MANUAL TIMER 117.08
I
CALL FOR HALF STEP DO E TIME 117.09 117.10 117.11
116.06 MAN 3
105.02 MANUAL
171.11 BLOCK CALL FOR HALF STEP
133.02 CTRL SVC CALL
START 117.12
108.08 MANUAL START
TURN OFF MAN 3 TGR 117.13
138c.27 MAC 1 = 0
END E TIME 117.14
TURN OFF CHK IND TGRS 117.15 117.16
GAF
51K
KJO
CTRL 0008 117.17

FIG. 117

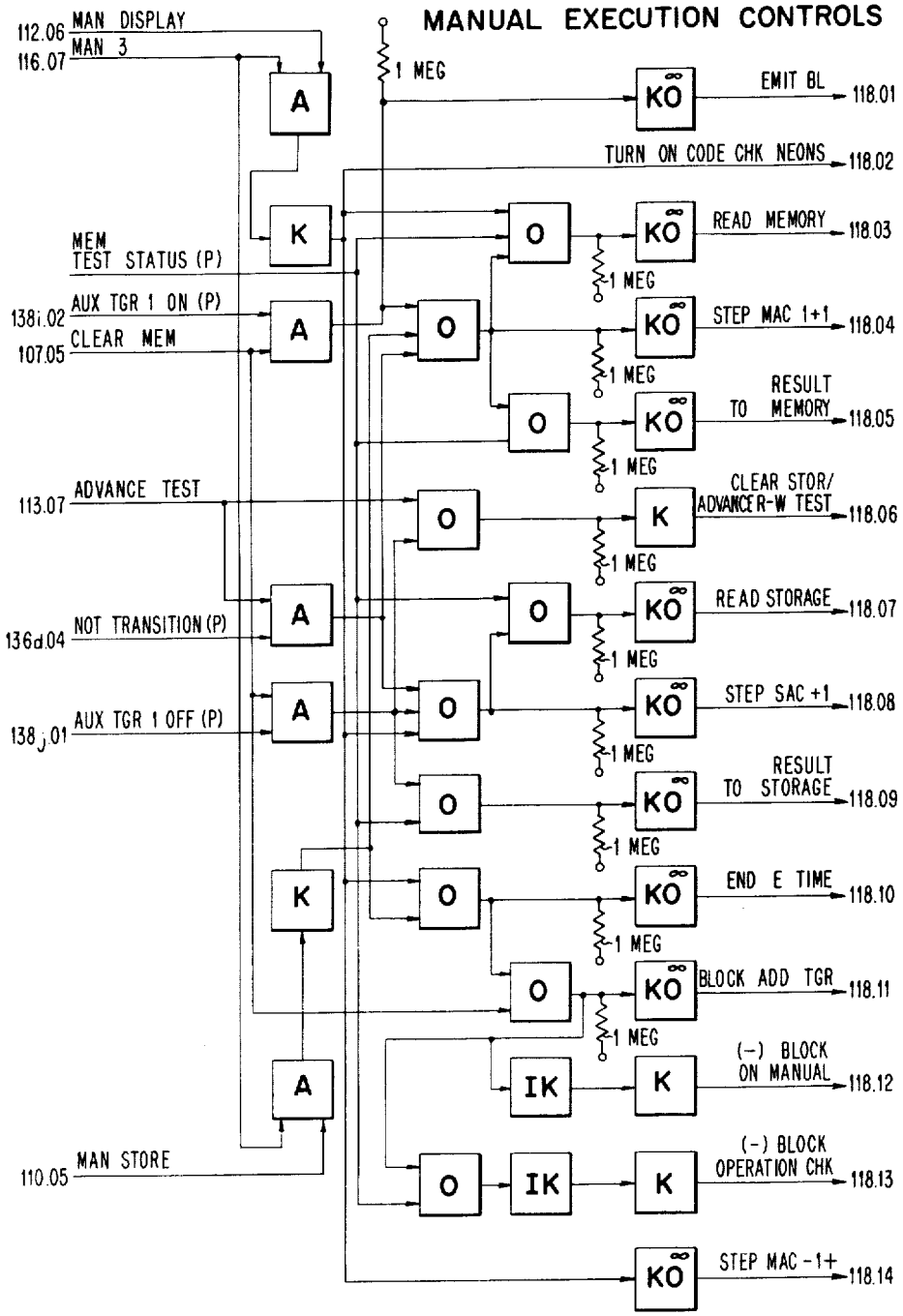

MANUAL EXECUTION CONTROLS
112.06 MAN DISPLAY
116.07 MAN 3
MEM TEST STATUS (P)
138i.02 AUX TGR 1 ON (P)
107.05 CLEAR MEM
113.07 ADVANCE TEST
136d.04 NOT TRANSITION (P)
138j.01 AUX TGR 1 OFF (P)
110.05 MAN STORE
1 MEG
A
K
O
IK
KO
EMIT BL 118.01
TURN ON CODE CHK NEONS 118.02
READ MEMORY 118.03
STEP MAC 1+1 118.04
RESULT TO MEMORY 118.05
CLEAR STOR/ ADVANCE R-W TEST 118.06
READ STORAGE 118.07
STEP SAC +1 118.08
RESULT TO STORAGE 118.09
END E TIME 118.10
BLOCK ADD TGR 118.11
(-) BLOCK ON MANUAL 118.12
(-) BLOCK OPERATION CHK 118.13
STEP MAC -1+ 118.14

FIG. 118

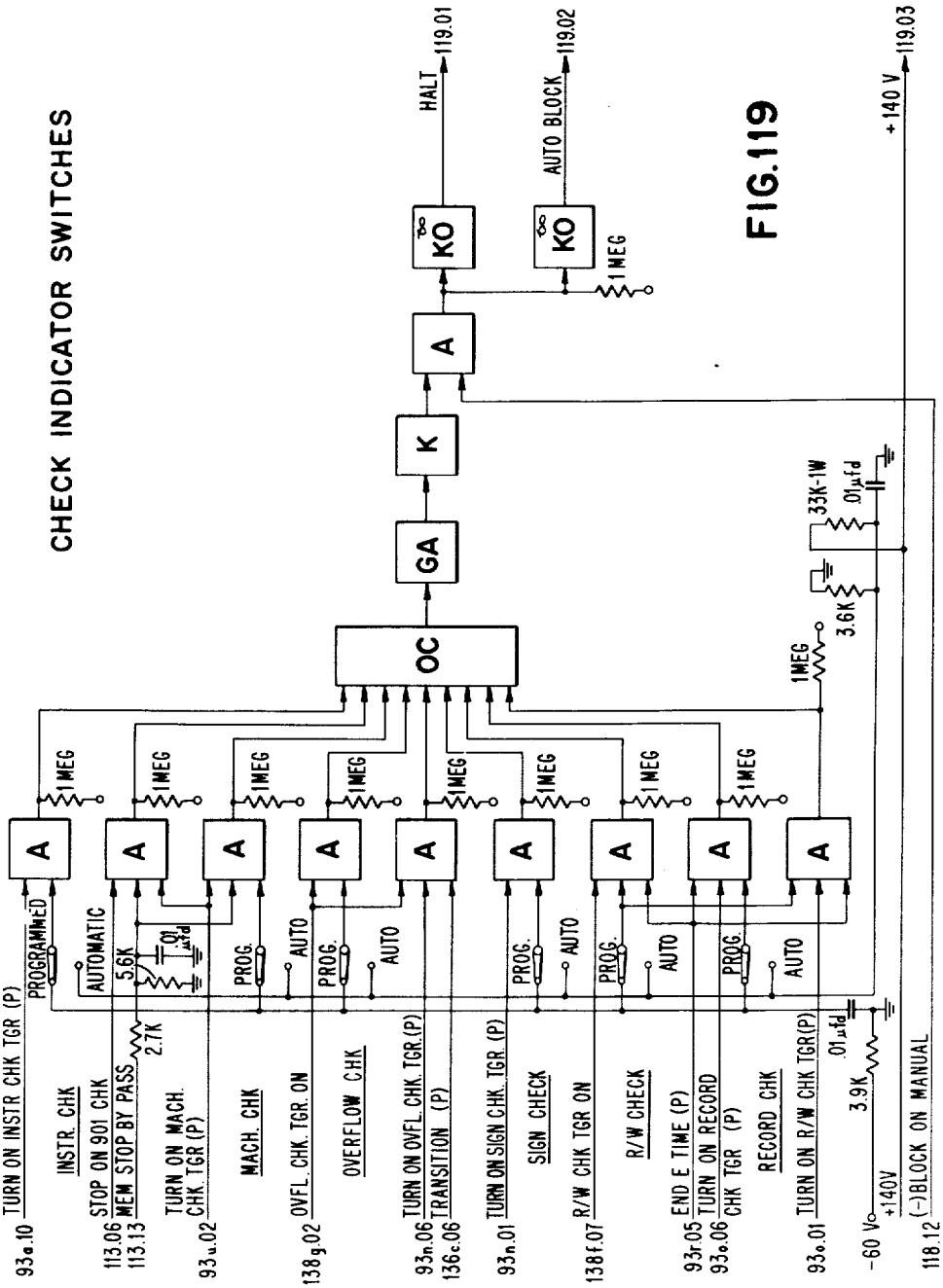
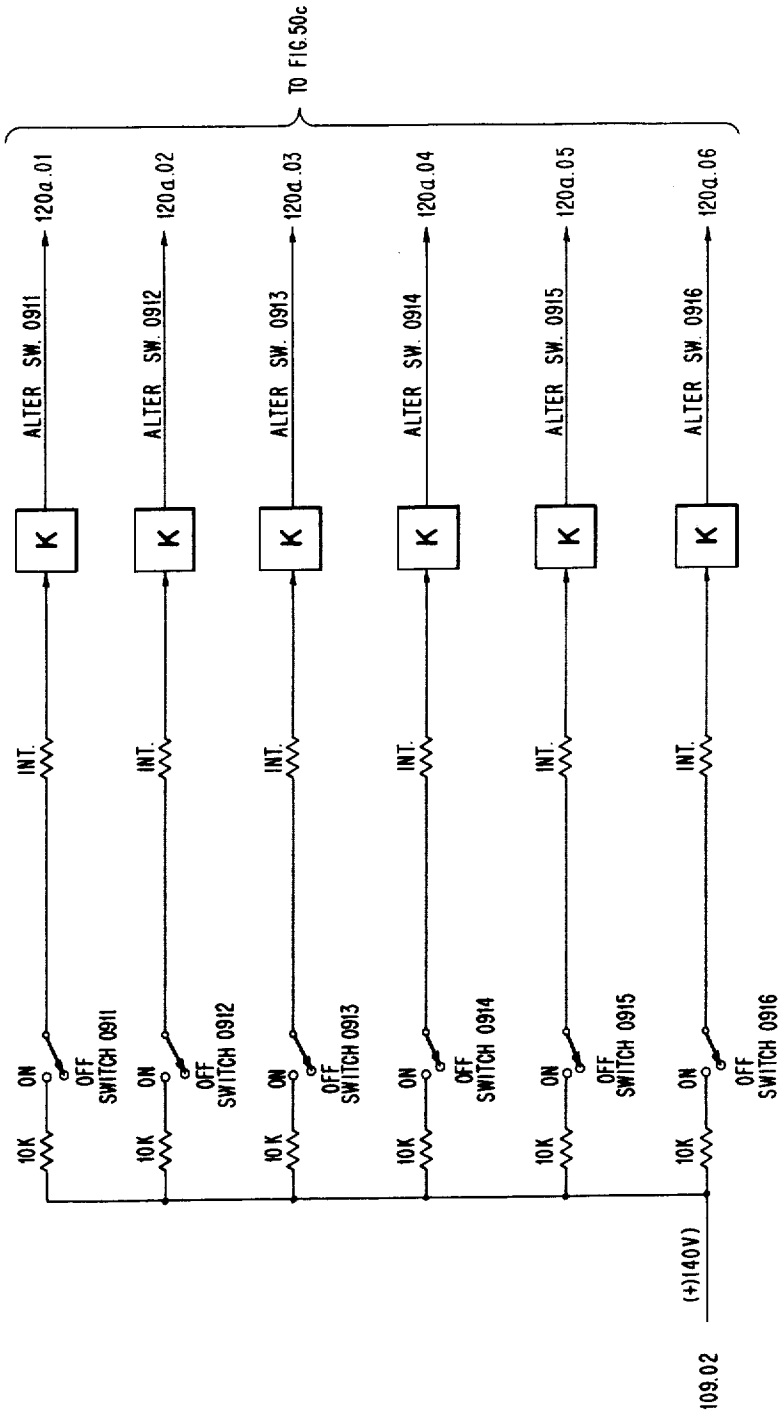

CHECK INDICATOR SWITCHES
93a.10 TURN ON INSTR CHK TGR (P)
INSTR. CHK
113.06 STOP ON 901 CHK
113.13 MEM STOP BY PASS
TURN ON MACH. CHK TGR (P)
93u.02
MACH. CHK
138g.02 OVFL. CHK. TGR. ON
OVERFLOW CHK
93n.06 TURN ON OVFL. CHK. TGR. (P)
136c.06 TRANSITION (P)
93n.01 TURN ON SIGN CHK. TGR. (P)
SIGN CHECK
138f.07 R/W CHK TGR ON
R/W CHECK
93r.05 END E TIME (P)
93o.06 TURN ON RECORD CHK TGR (P)
RECORD CHK
93o.01 TURN ON R/W CHK TGR(P)
-60 V
+140V
118.12 (-)BLOCK ON MANUAL
PROGRAMMED
AUTOMATIC
PROG.
AUTO
1MEG
5.6K
2.7K
.01 µfd
3.9K
3.6K
33K-1W
A
OC
GA
K
KO
HALT 119.01
AUTO BLOCK 119.02
+140 V 119.03

FIG.119

FIG. 120a
ALTERATION SWITCHES



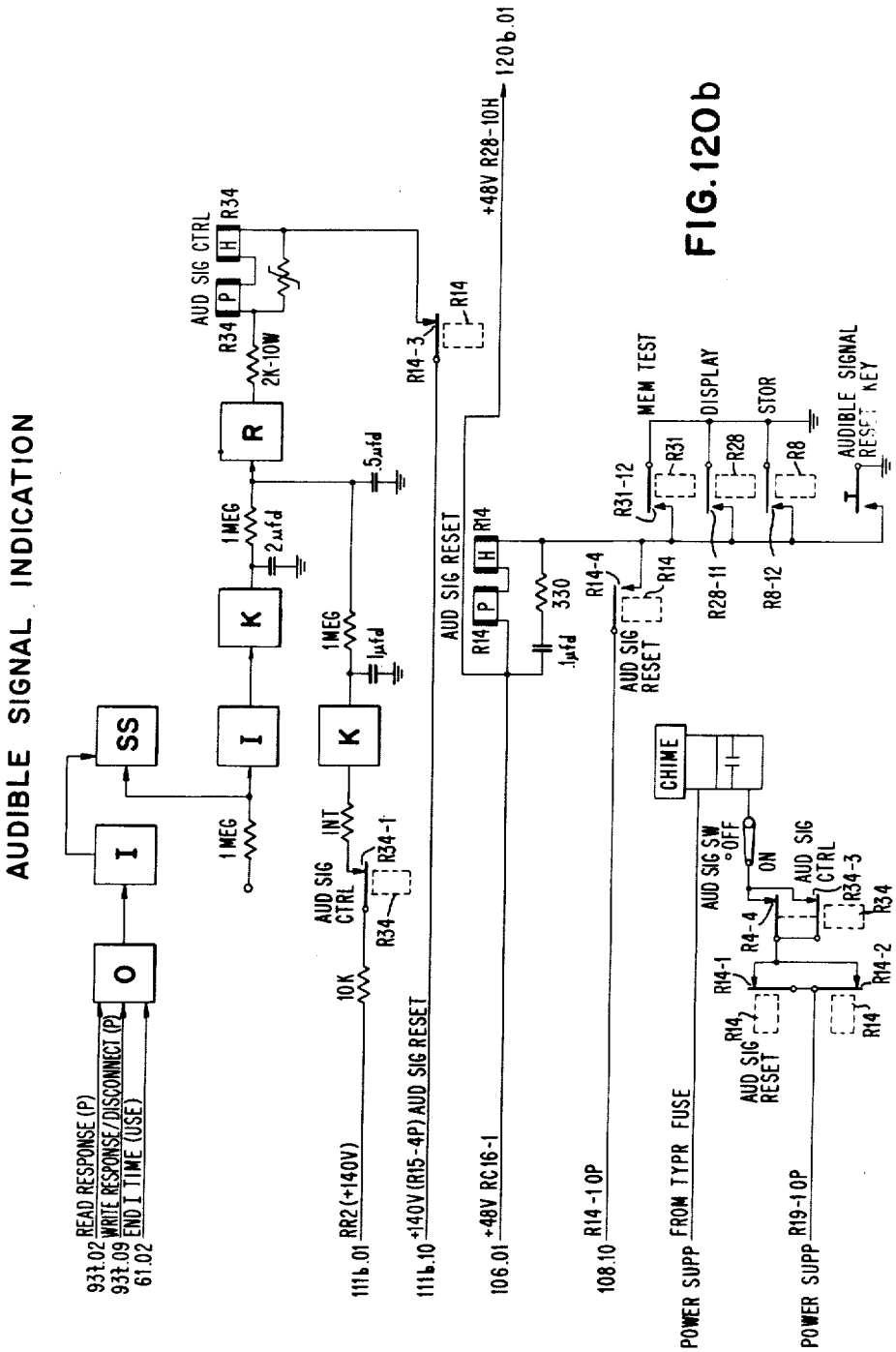

AUDIBLE SIGNAL INDICATION
O
I
SS
I
K
K
R
H
P
H
P
I
AUD SIG CTRL
R34
2K-10W
1 MEG
2 µfd
5 µfd
1 MEG
1 µfd
AUD SIG CTRL
INT
R34-1
R34
10K
AUD SIG RESET
R14
R14-3
+48V R28-10H
120b.01
R4
330
.1 µfd
R14-4
AUD SIG RESET
R14
R31-12
MEM TEST
R31
DISPLAY
R28
STOR
R8
AUDIBLE SIGNAL RESET KEY
R28-11
R8-12
CHIME
AUD SIG SW
OFF
ON
AUD SIG CTRL
R34-3
R34
R14-1
R4-4
R14-2
R14
AUD SIG RESET
R14
93t.02 READ RESPONSE (P)
93t.09 WRITE RESPONSE/DISCONNECT (P)
61.02 END I TIME (USE)
111b.01 RR2 (+140V)
111b.10 +140V (R15-4P) AUD SIG RESET
106.01 +48V RC16-1
108.10 R14-10P
POWER SUPP FROM TYPR FUSE
POWER SUPP R19-10P

FIG. 120b

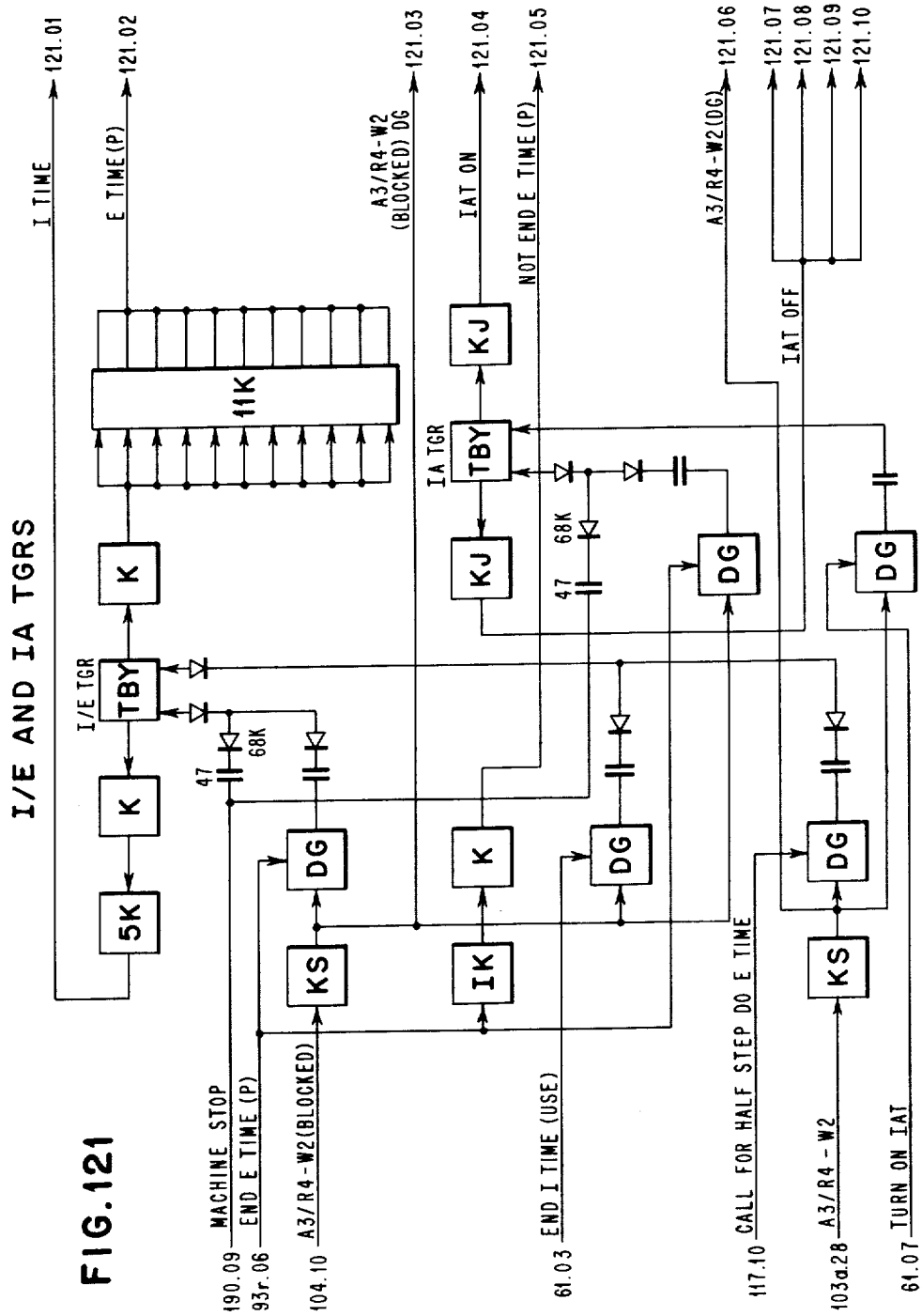

I/E AND IA TGRS
I TIME
121.01
E TIME(P)
121.02
A3/R4-W2 (BLOCKED) DG
121.03
IAT ON
121.04
NOT END E TIME(P)
121.05
A3/R4-W2(DG)
121.06
121.07
121.08
121.09
121.10
IAT OFF
11K
K
I/E TGR
TBY
5K
47
68K
DG
KS
IA TGR
KJ
IK
190.09 MACHINE STOP
93r.06 END E TIME (P)
104.10 A3/R4-W2(BLOCKED)
61.03 END I TIME (USE)
117.10 CALL FOR HALF STEP DO E TIME
103a.28 A3/R4 - W2
61.07 TURN ON IAT

FIG. 121

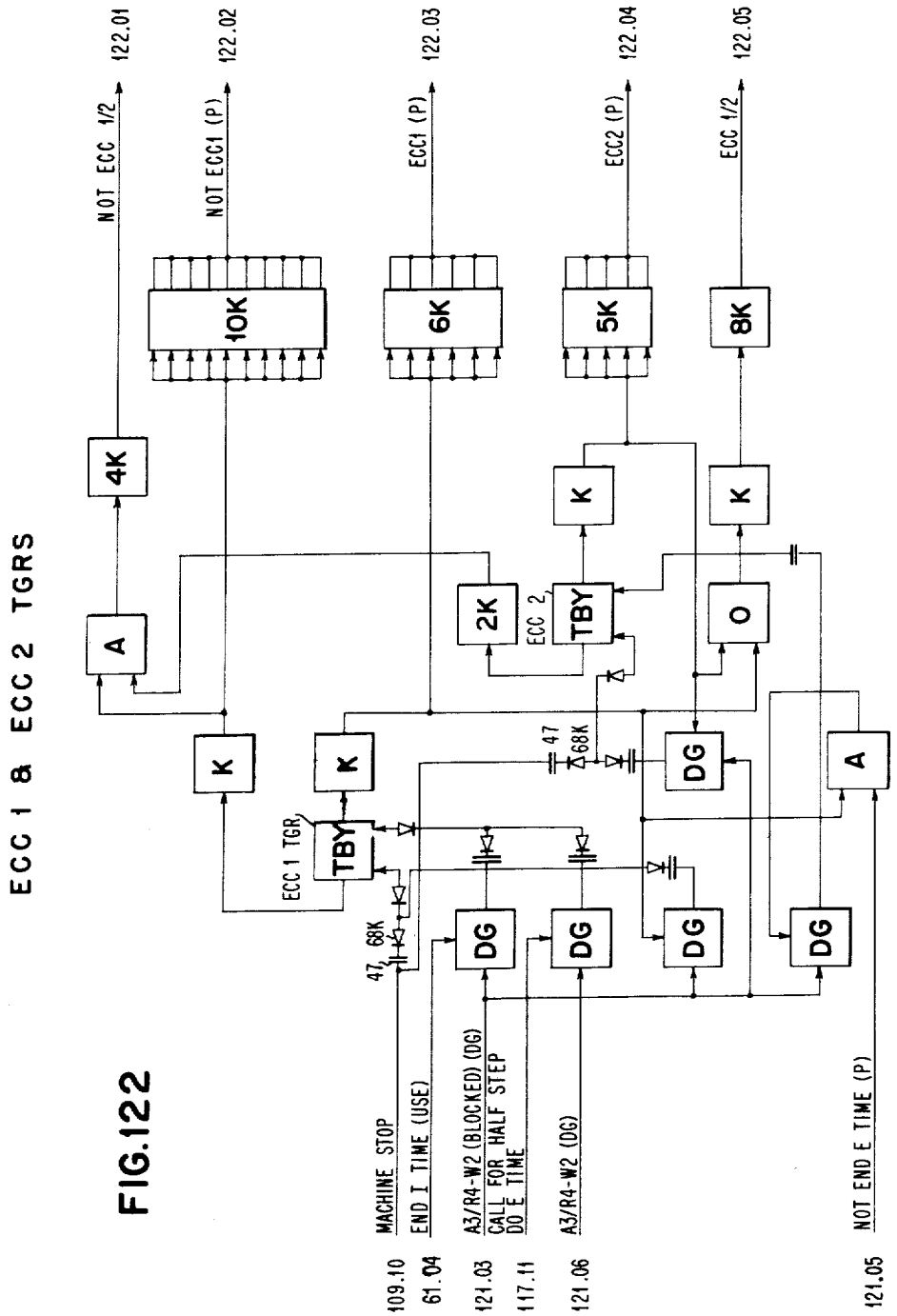

ECC 1 & ECC 2 TGRS
NOT ECC 1/2
122.01
NOT ECC1 (P)
122.02
ECC1 (P)
122.03
ECC2 (P)
122.04
ECC 1/2
122.05
10K
6K
5K
8K
4K
K
K
K
A
2K
TBY
ECC 2
O
47
68K
DG
A
K
K
TBY
ECC 1 TGR
47
68K
DG
DG
DG
DG
MACHINE STOP
109.10
END I TIME (USE)
61.04
A3/R4-W2 (BLOCKED) (DG)
121.03
CALL FOR HALF STEP
DO E TIME
117.11
A3/R4-W2 (DG)
121.06
NOT END E TIME (P)
121.05

FIG.122

FIG. 123

I/E TIMER OUTPUTS

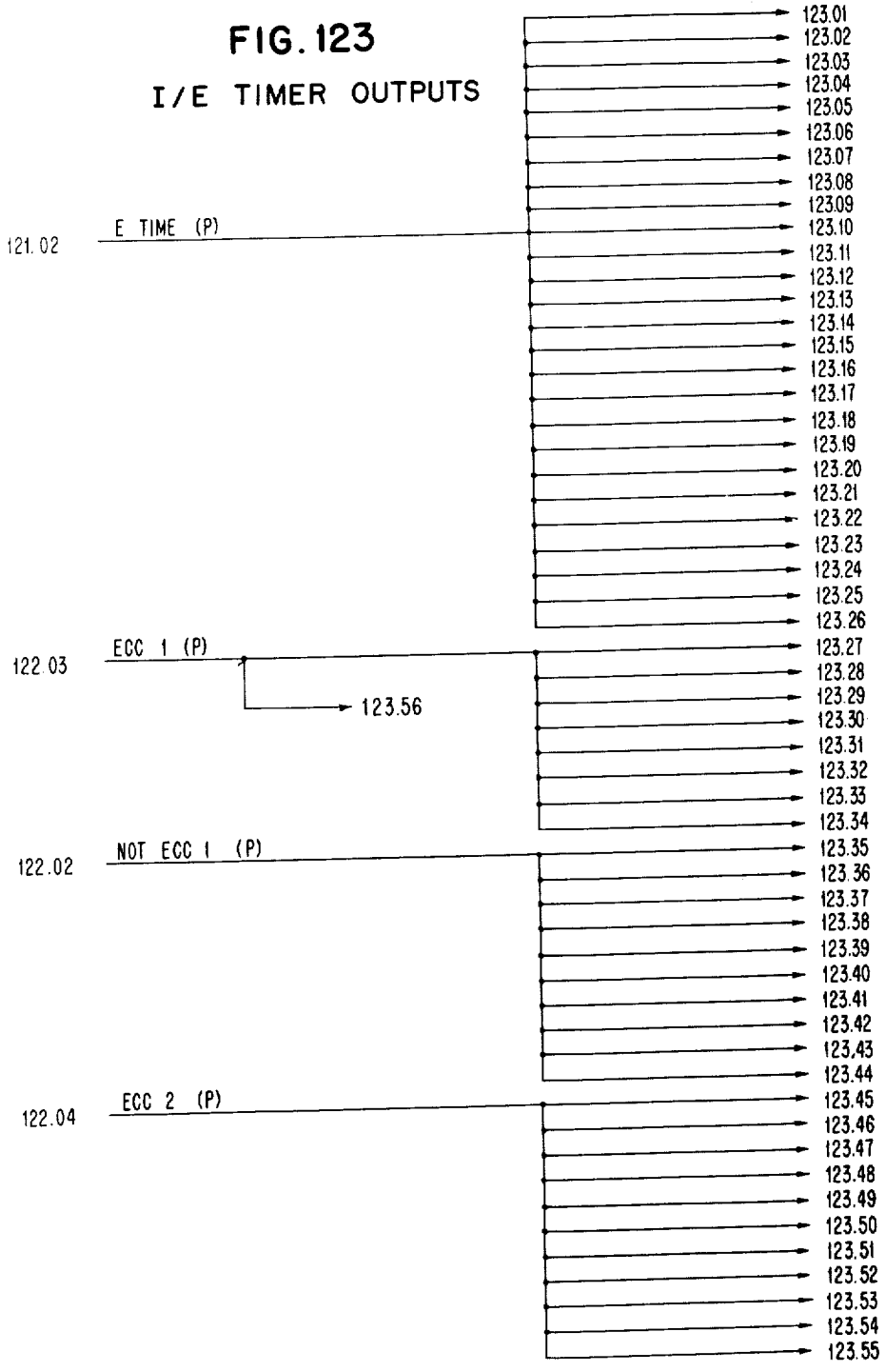
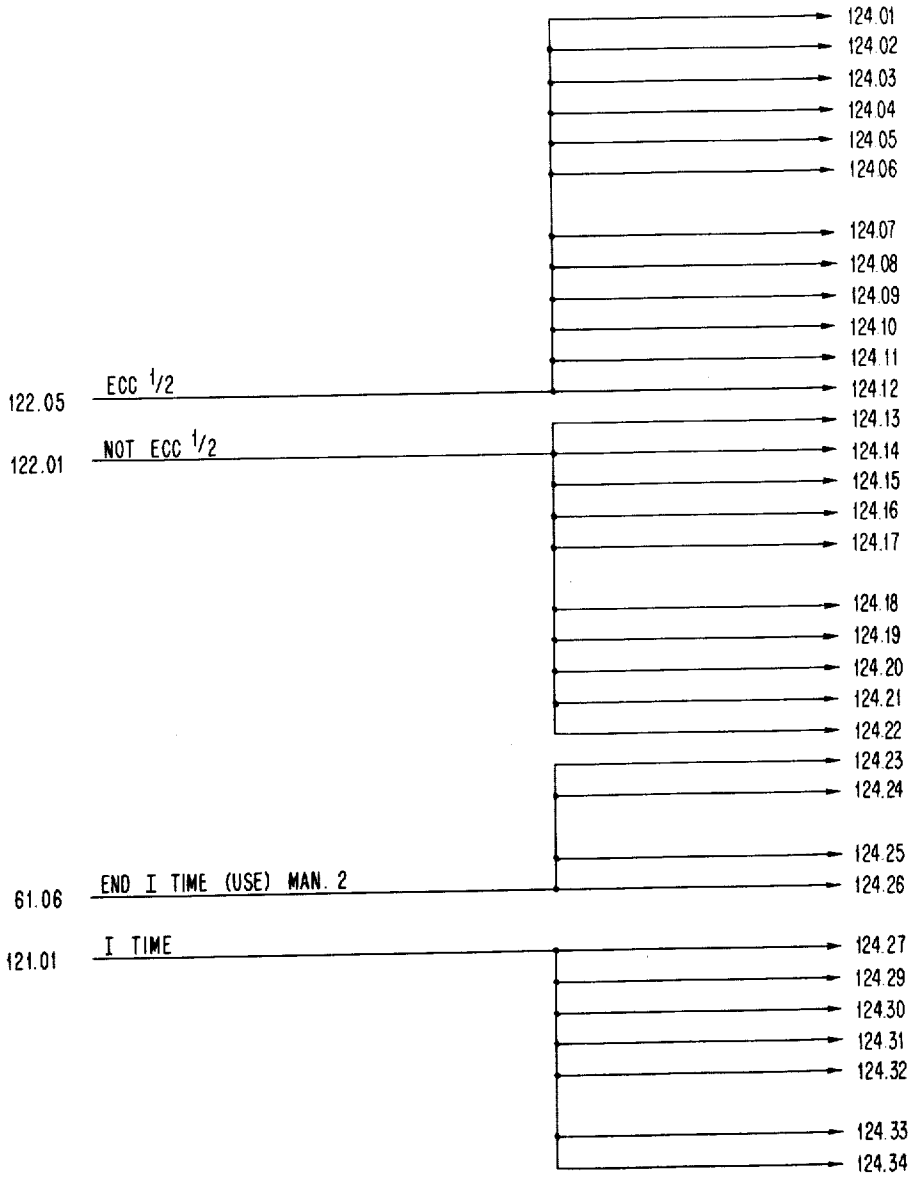


FIG. 124

I/E TIMER OUTPUTS



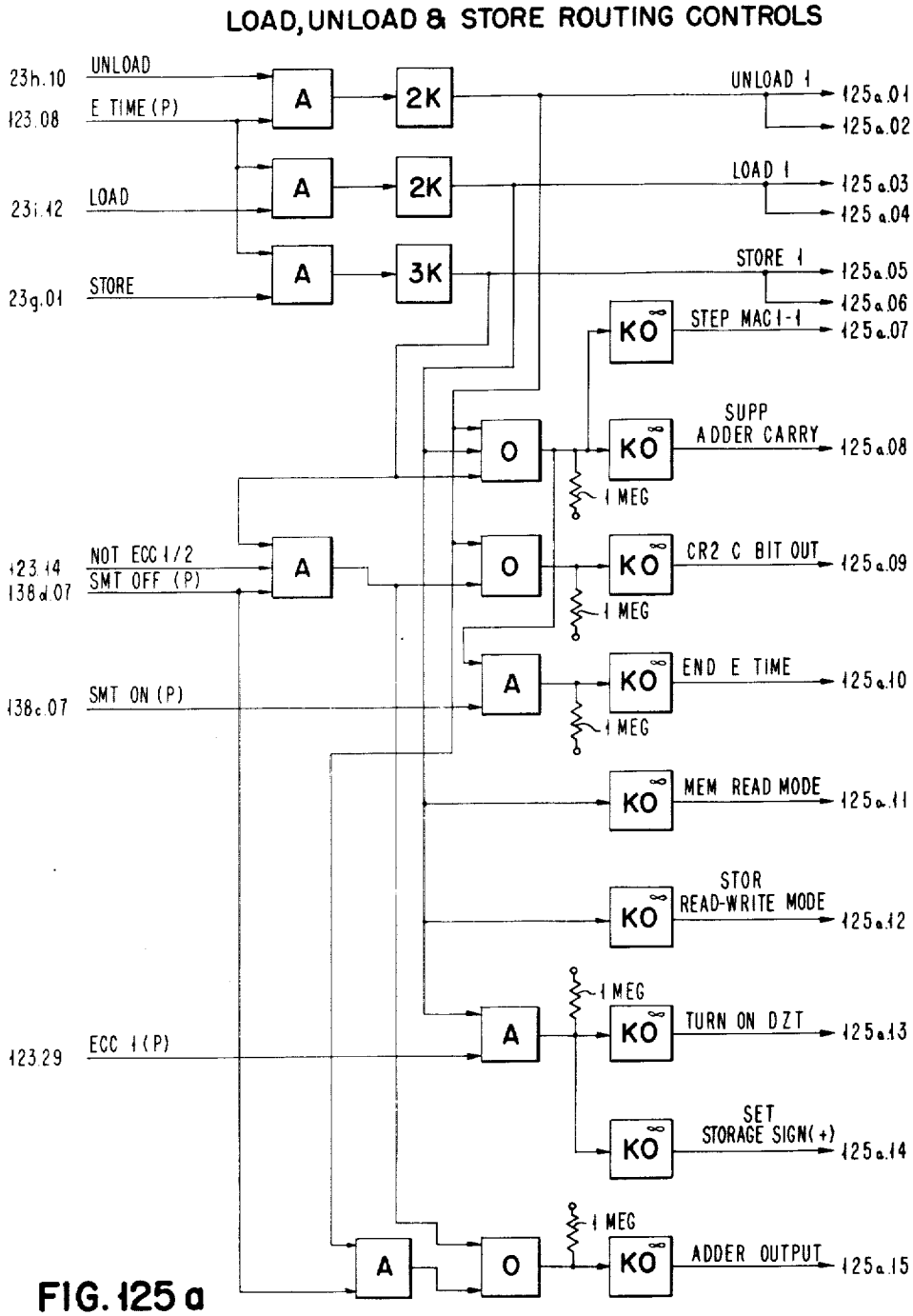

LOAD, UNLOAD & STORE ROUTING CONTROLS
23h.10
UNLOAD
123.08
E TIME (P)
23i.12
LOAD
23g.01
STORE
A
2K
A
2K
A
3K
UNLOAD 1
125a.01
125a.02
LOAD 1
125a.03
125a.04
STORE 1
125a.05
125a.06
125a.07
KO
STEP MAC1-1
KO
SUPP ADDER CARRY
125a.08
O
1 MEG
123.14
NOT ECC 1/2
138d.07
SMT OFF (P)
A
O
KO
CR2 C BIT OUT
125a.09
1 MEG
A
KO
END E TIME
125a.10
138c.07
SMT ON (P)
1 MEG
KO
MEM READ MODE
125a.11
KO
STOR READ-WRITE MODE
125a.12
1 MEG
123.29
ECC 1 (P)
A
KO
TURN ON DZT
125a.13
KO
SET STORAGE SIGN(+)
125a.14
1 MEG
A
O
KO
ADDER OUTPUT
125a.15

FIG. 125a

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LOAD, UNLOAD & STORE ROUTING CONTROLS

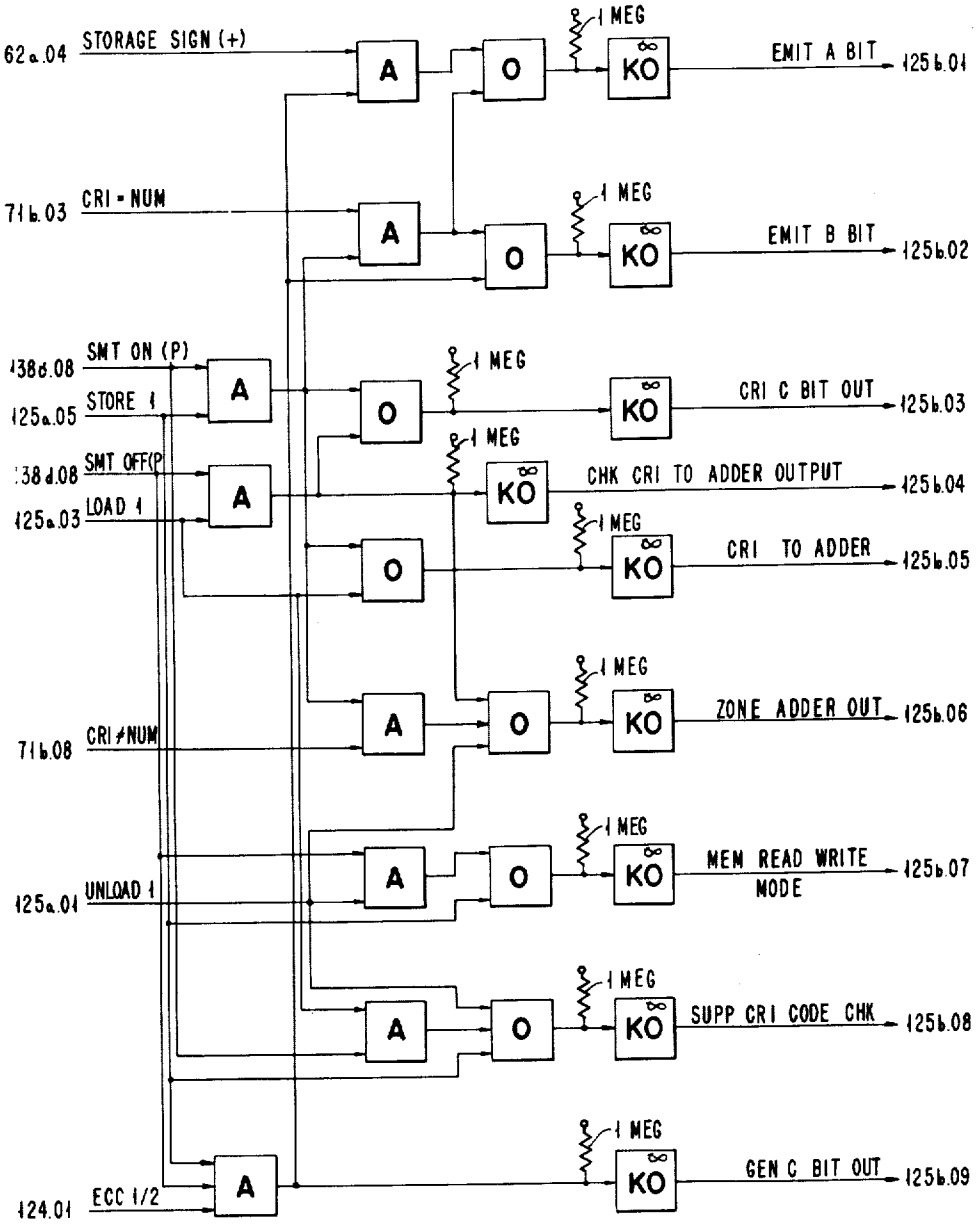


FIG. 125b

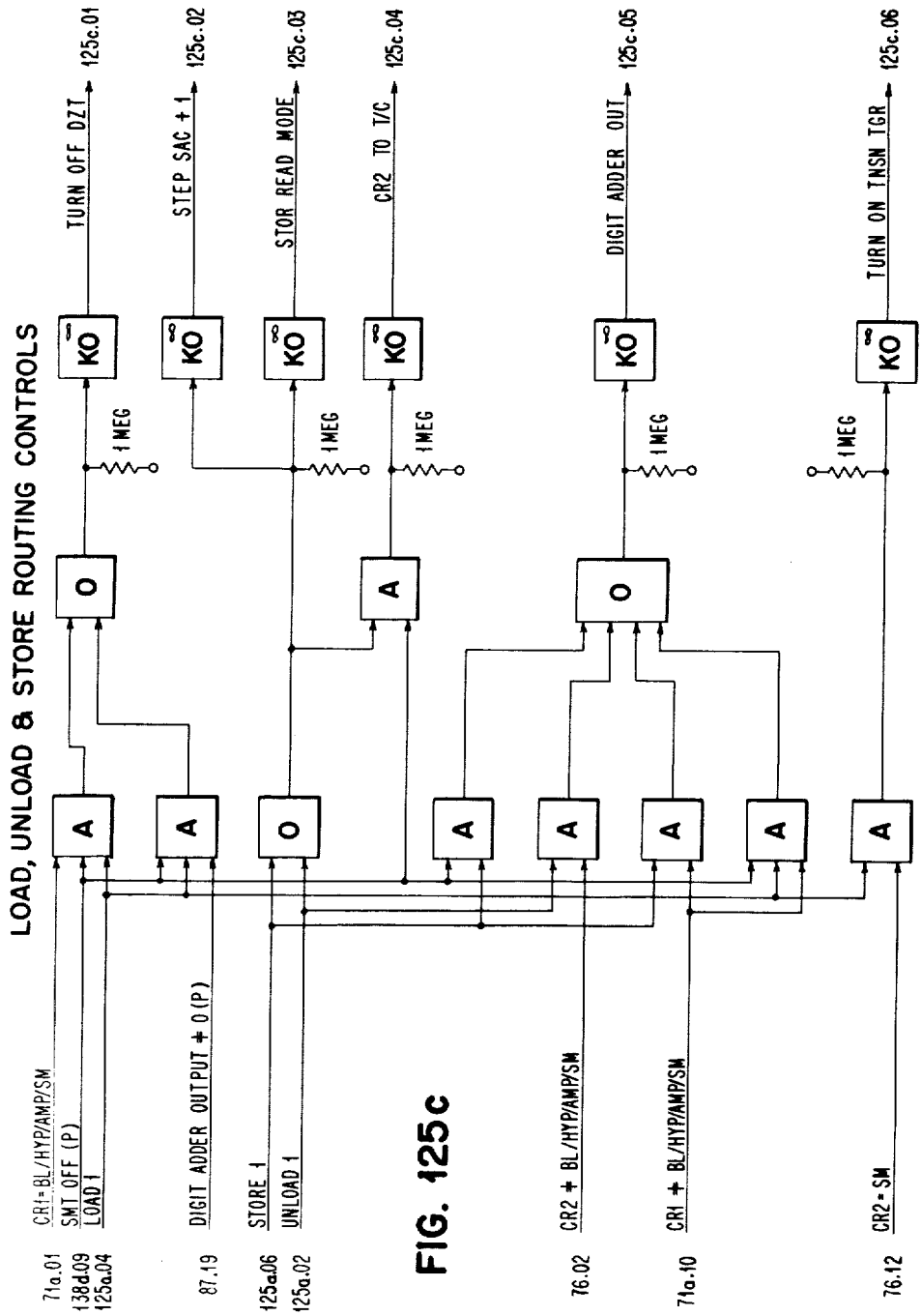

LOAD, UNLOAD & STORE ROUTING CONTROLS
TURN OFF DZT
125c.01
STEP SAC + 1
125c.02
STOR READ MODE
125c.03
CR2 TO T/C
125c.04
DIGIT ADDER OUT
125c.05
TURN ON TNSN TGR
125c.06
KO
1 MEG
O
A
CR1=BL/HYP/AMP/SM
SMT OFF (P)
LOAD 1
DIGIT ADDER OUTPUT + 0 (P)
STORE 1
UNLOAD 1
CR2 + BL/HYP/AMP/SM
CR1 + BL/HYP/AMP/SM
CR2=SM
71a.01
138d.09
125a.04
87.19
125a.06
125a.02
76.02
71a.10
76.12

FIG. 125c

FIG. 126a

STORE FOR PRINT ROUTING CONTROLS

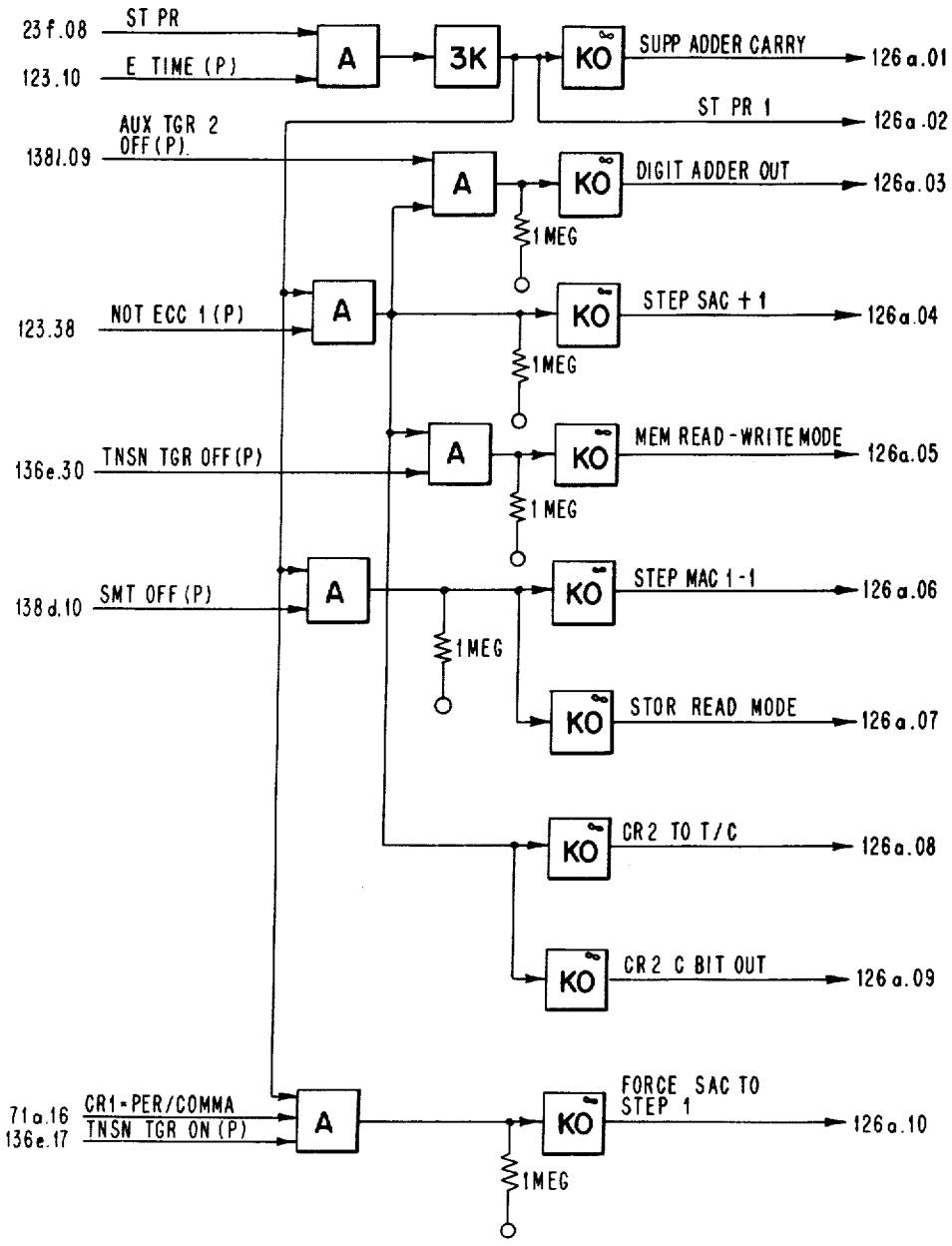


FIG. 126b

STORE FOR PRINT ROUTING CONTROLS

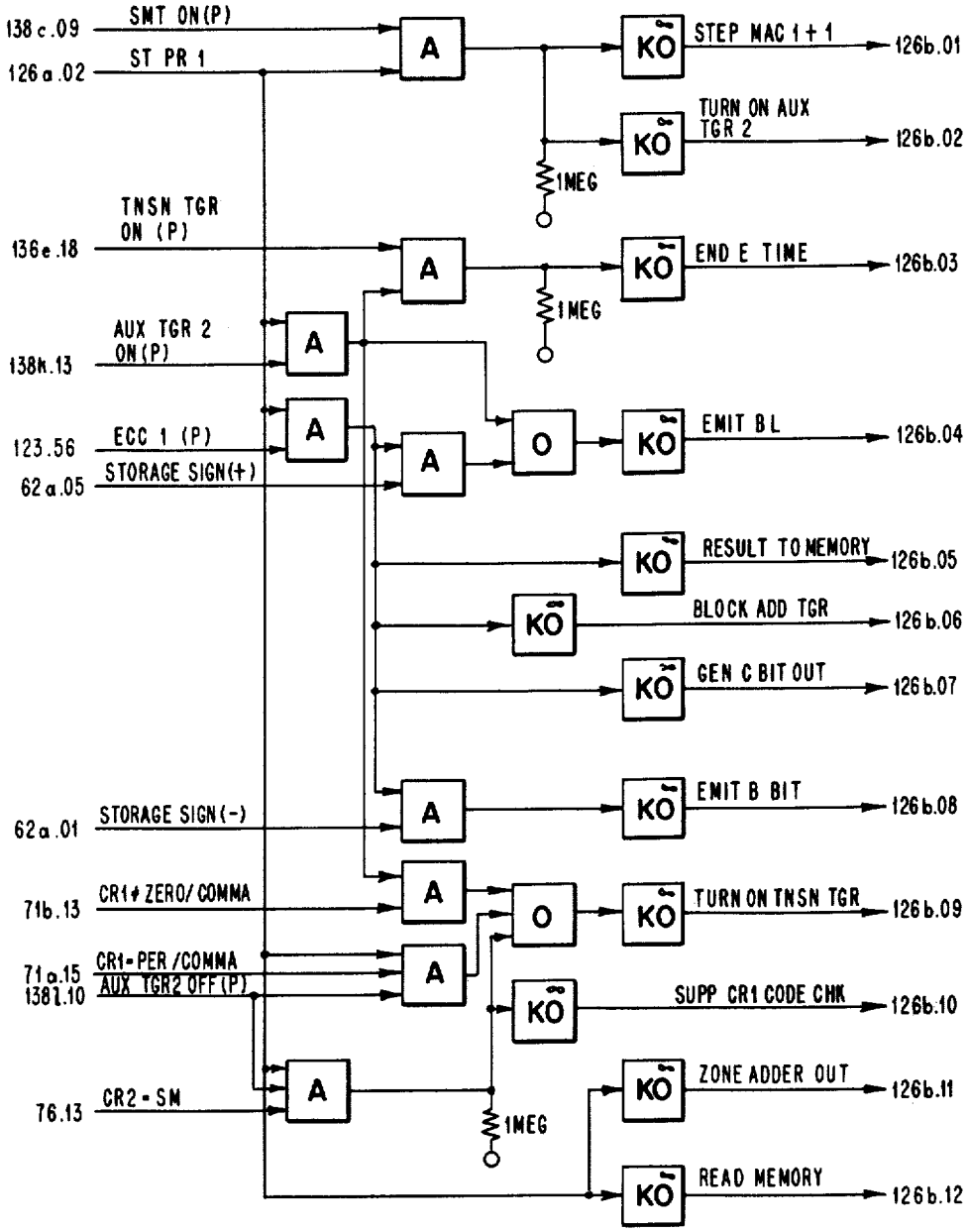


FIG. 127 a

TSMT / SEND ROUTING CONTROLS

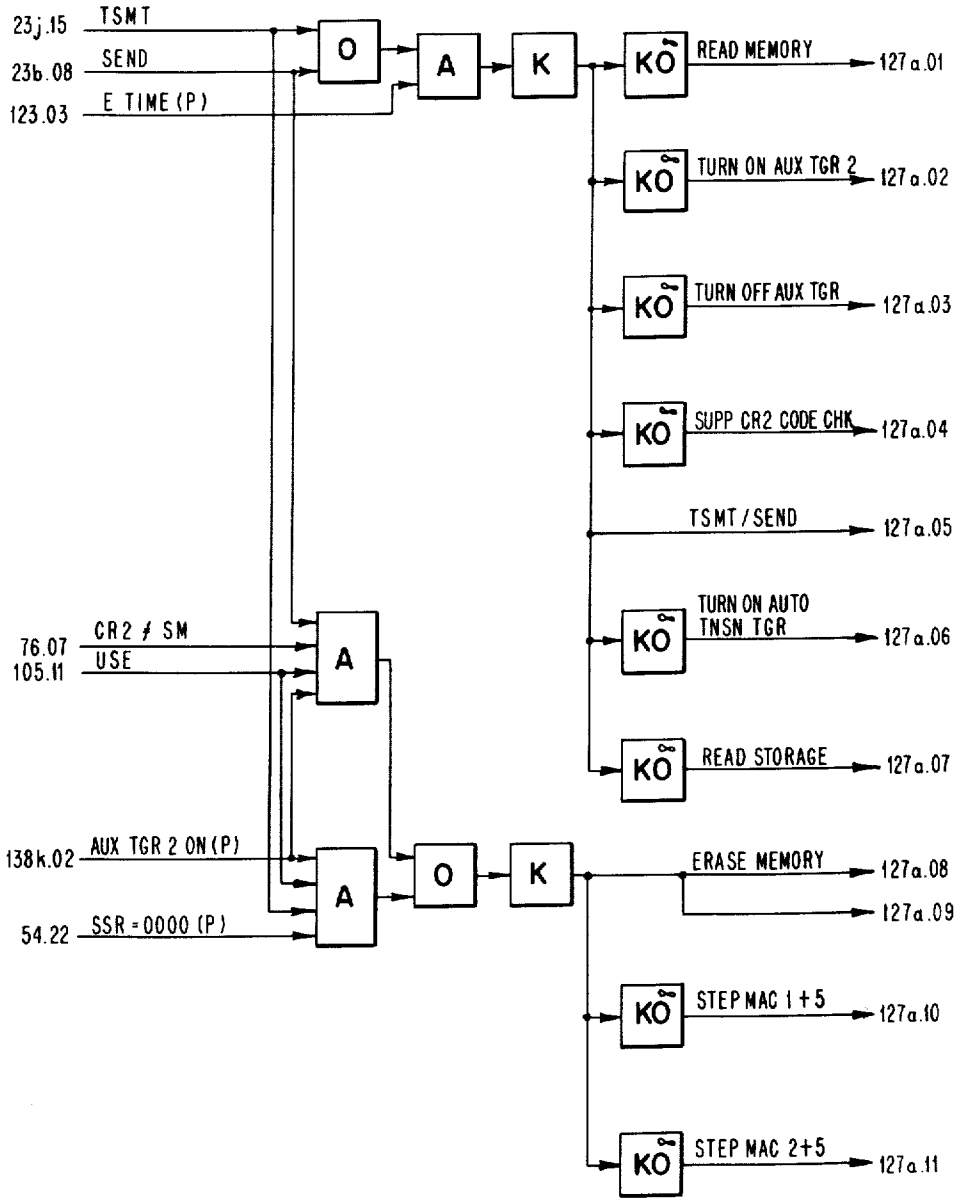
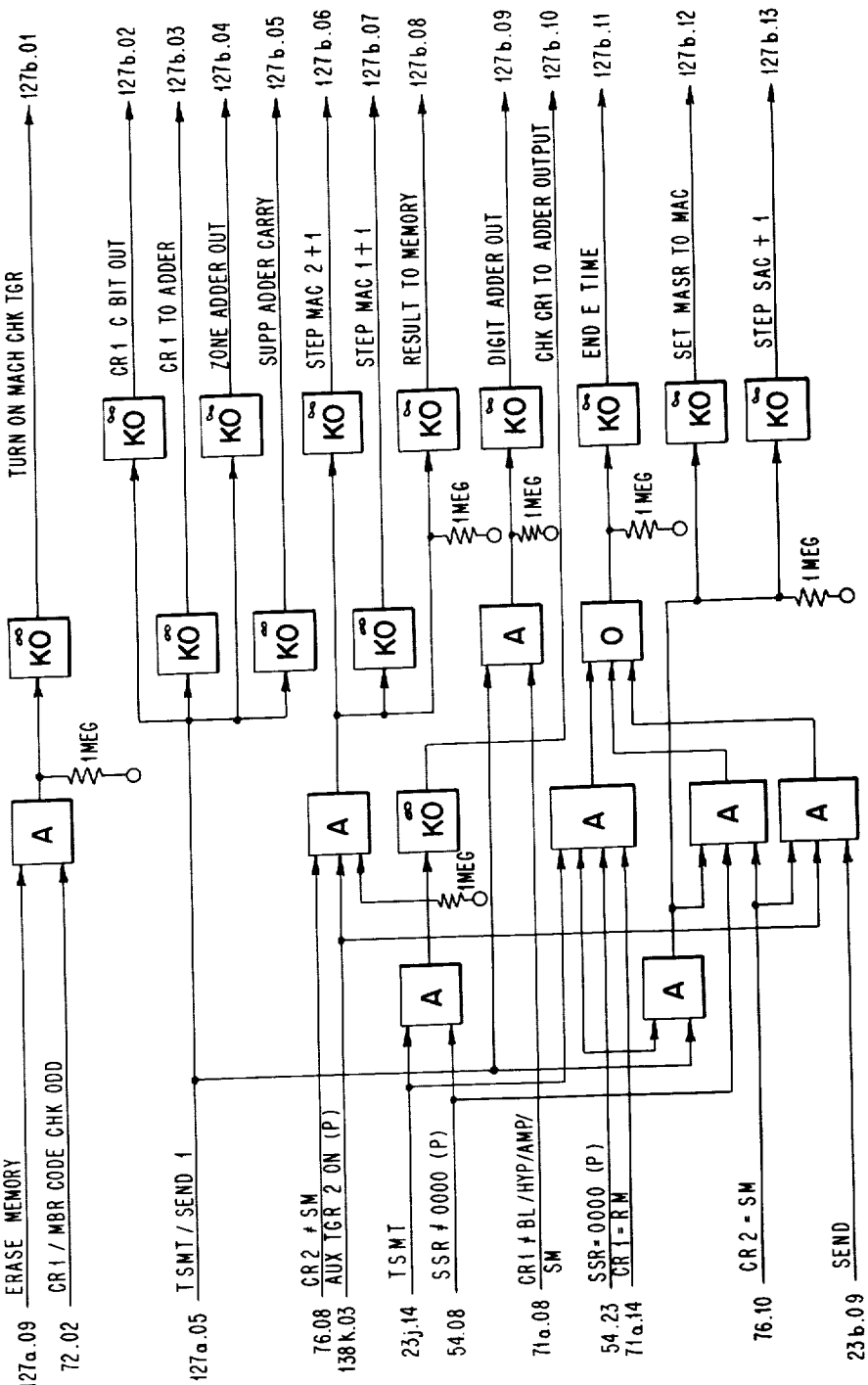


FIG. 127b TSMT / SEND ROUTING CONTROLS



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FIG. 128

BLANK MEMORY

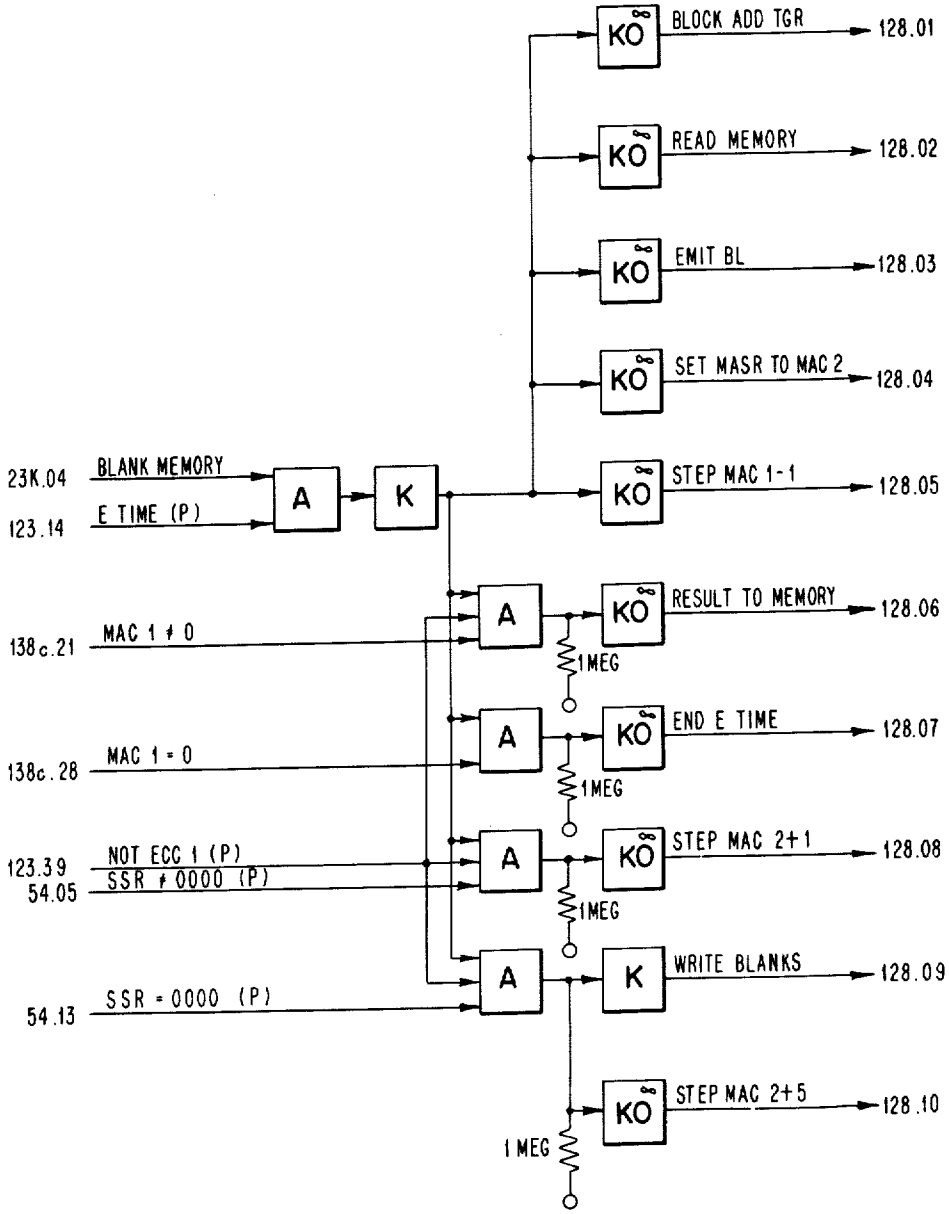
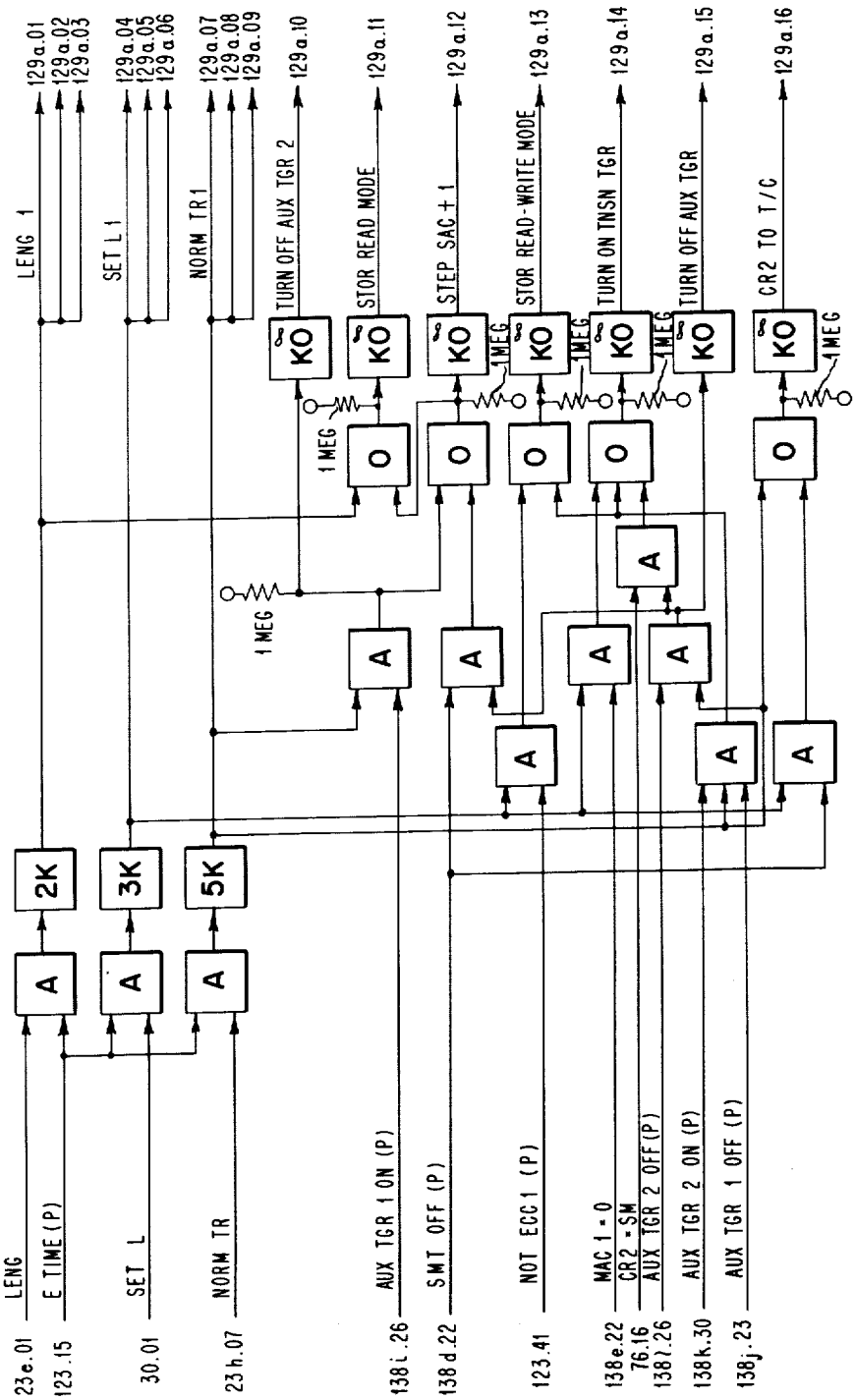


FIG. 129a

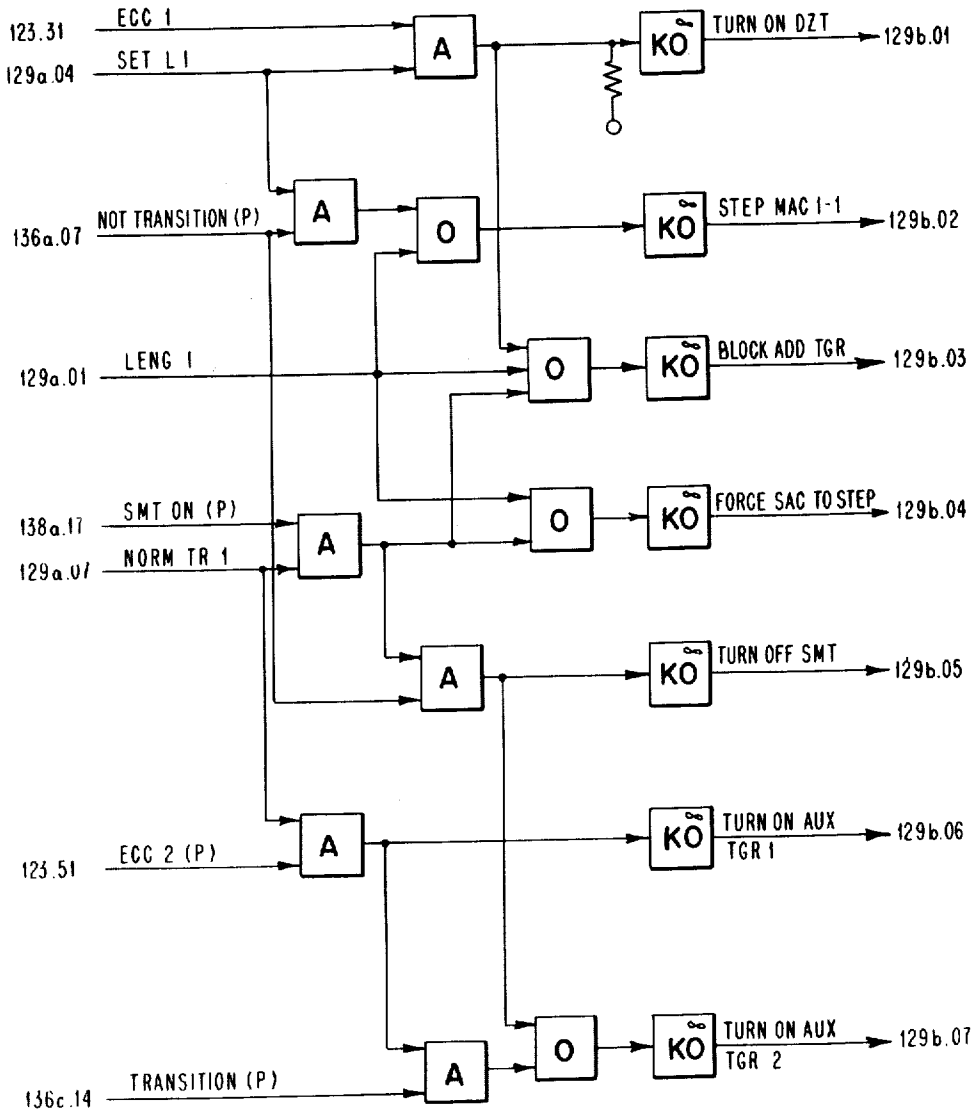
SET LEFT, LENG & NORM TR ROUTING CONTROLS



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FIG. 129b

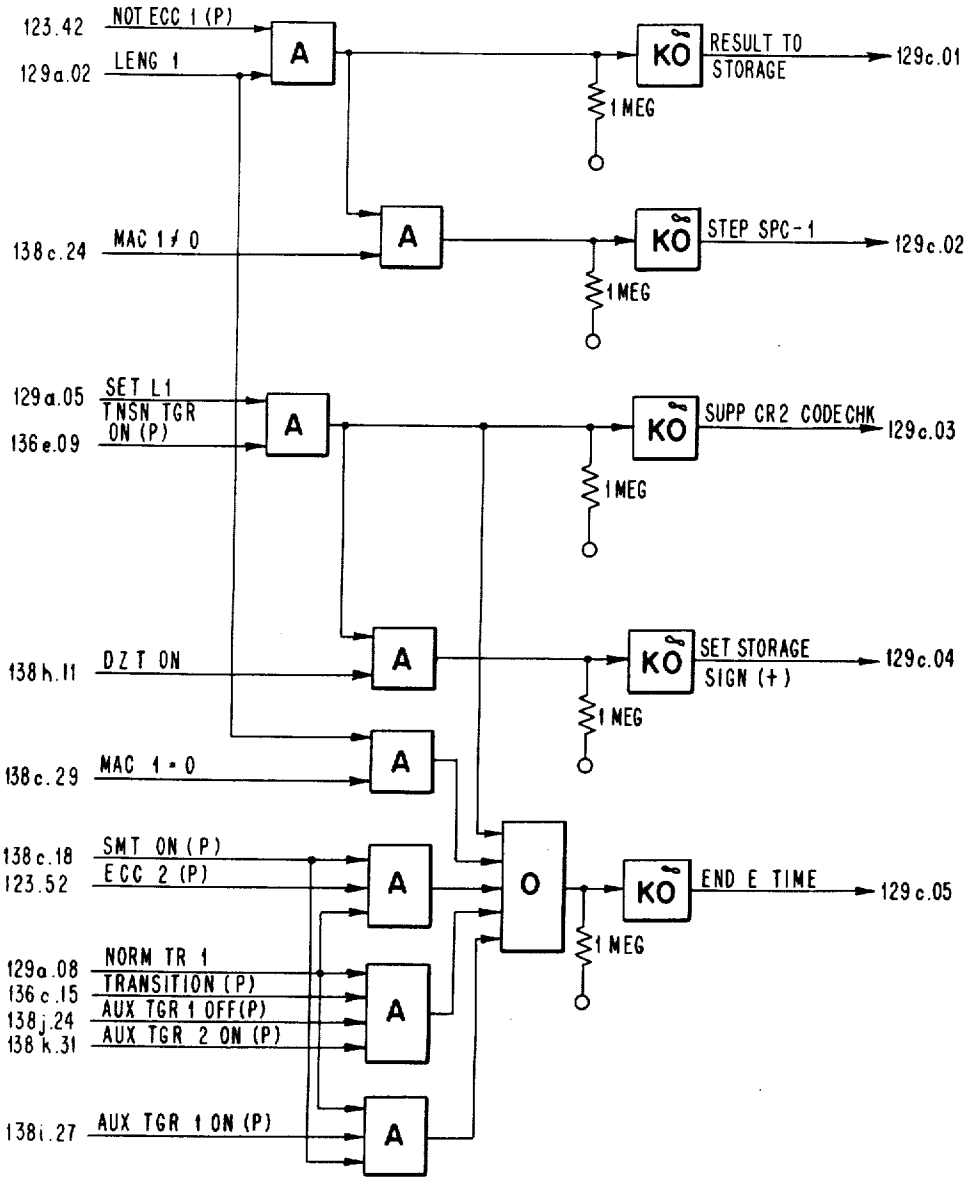
SET LEFT, LENG & NORM TR ROUTING CONTROLS



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FIG. 129c

SET LEFT, LENG & NORM TR ROUTING CONTROLS



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FIG. 129 d

SET LEFT, LENG & NORM TR ROUTING CONTROLS

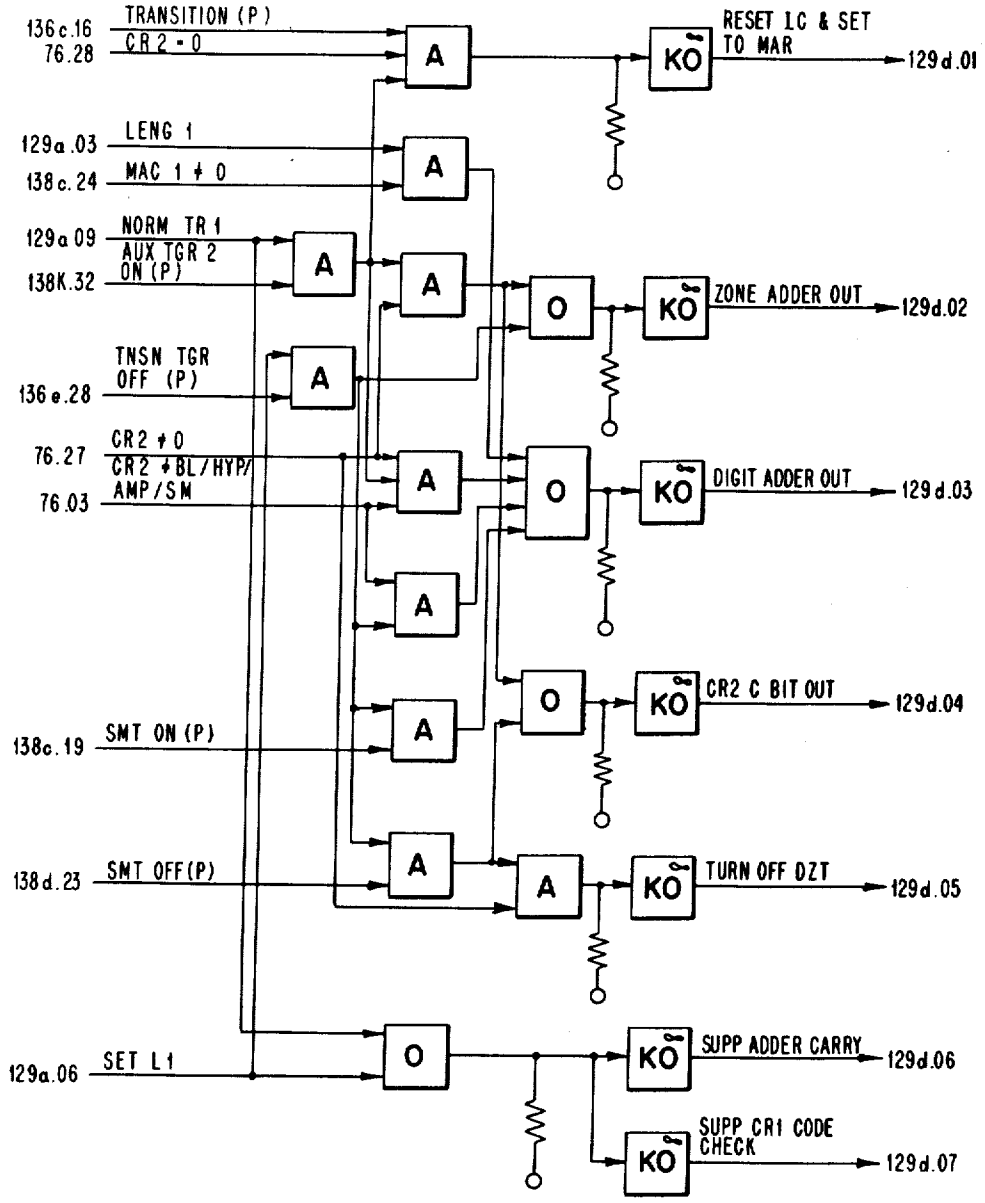


FIG. 130a

SHORTEN RIGHT / ROUND ROUTING CONTROLS

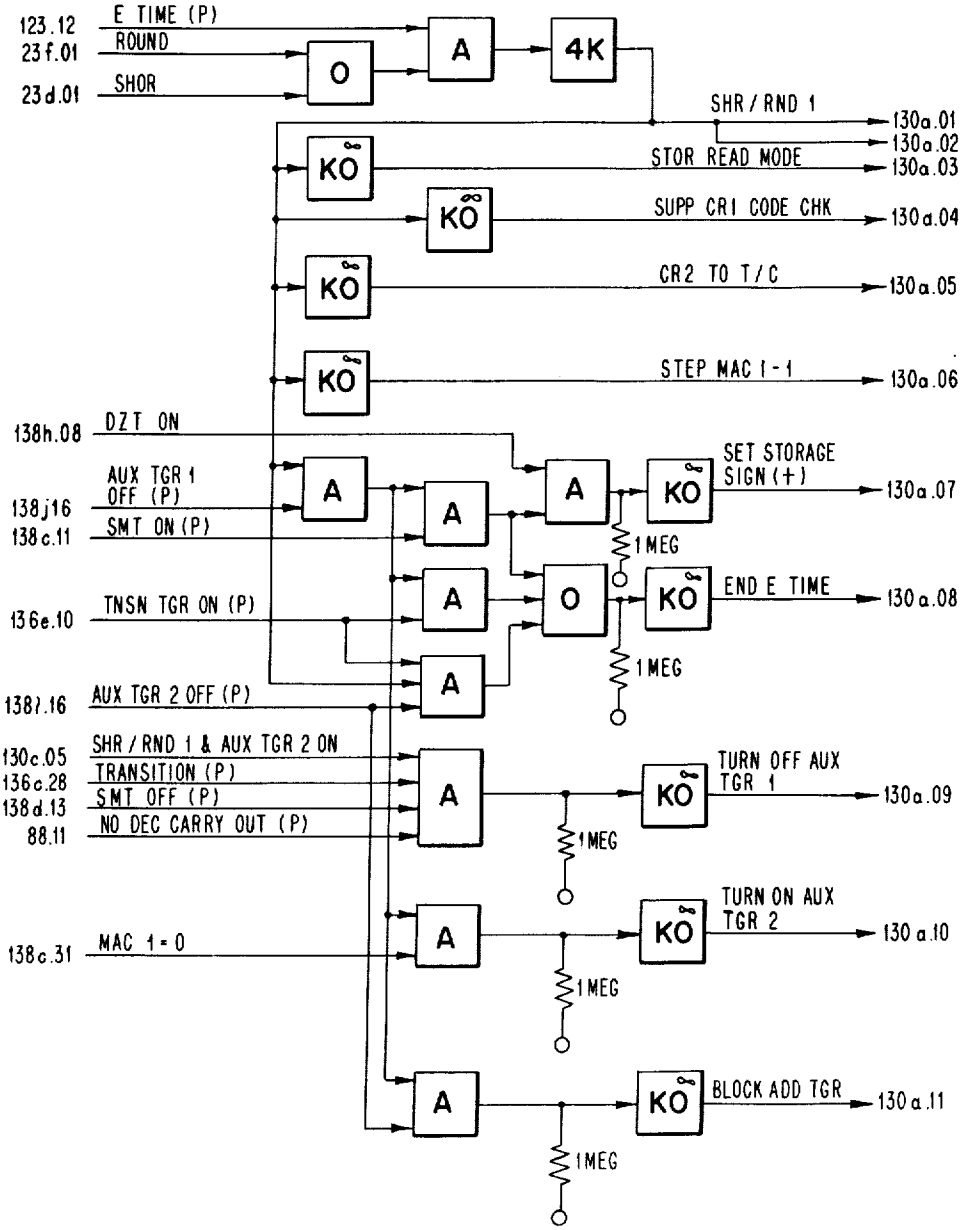
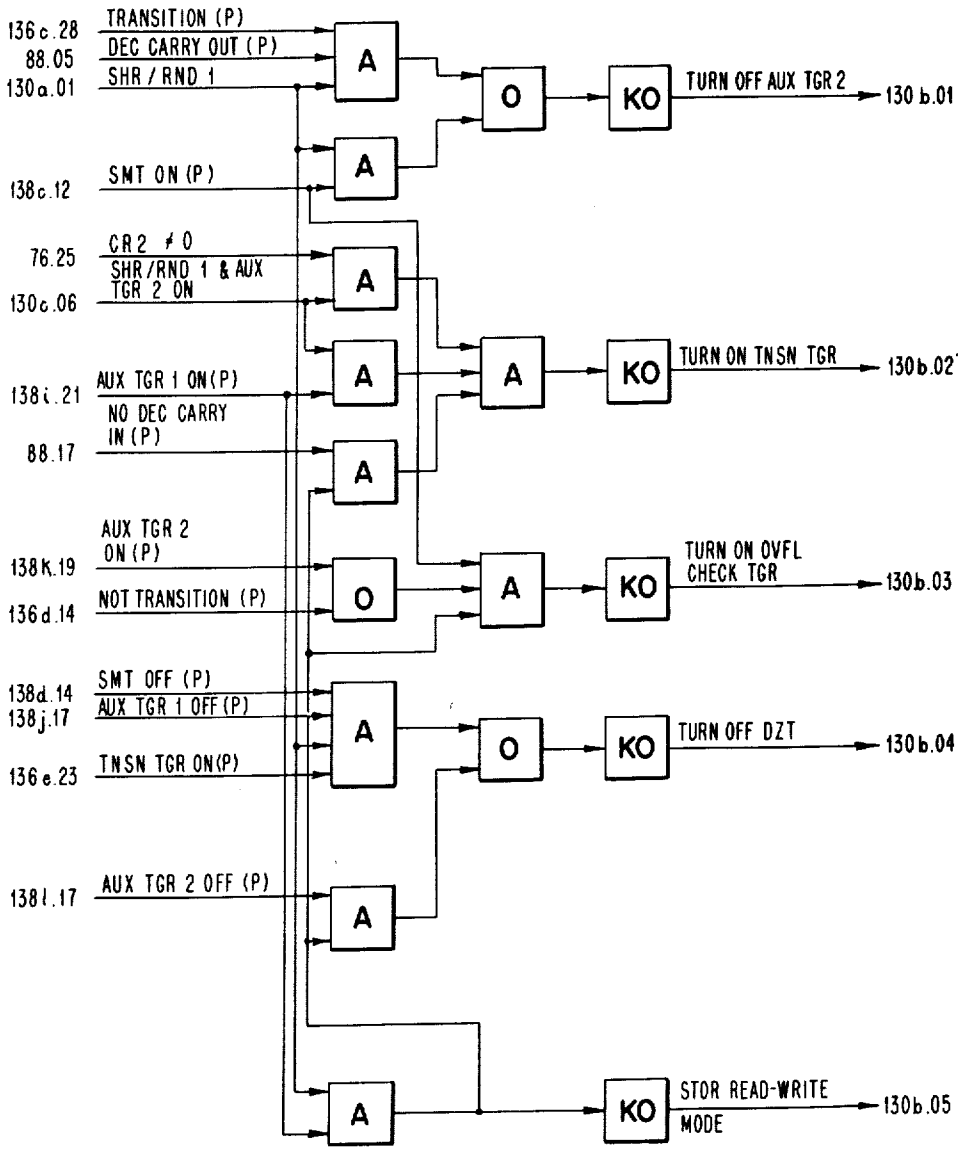


FIG. 130 b

SHORTEN RIGHT / ROUND ROUTING CONTROLS



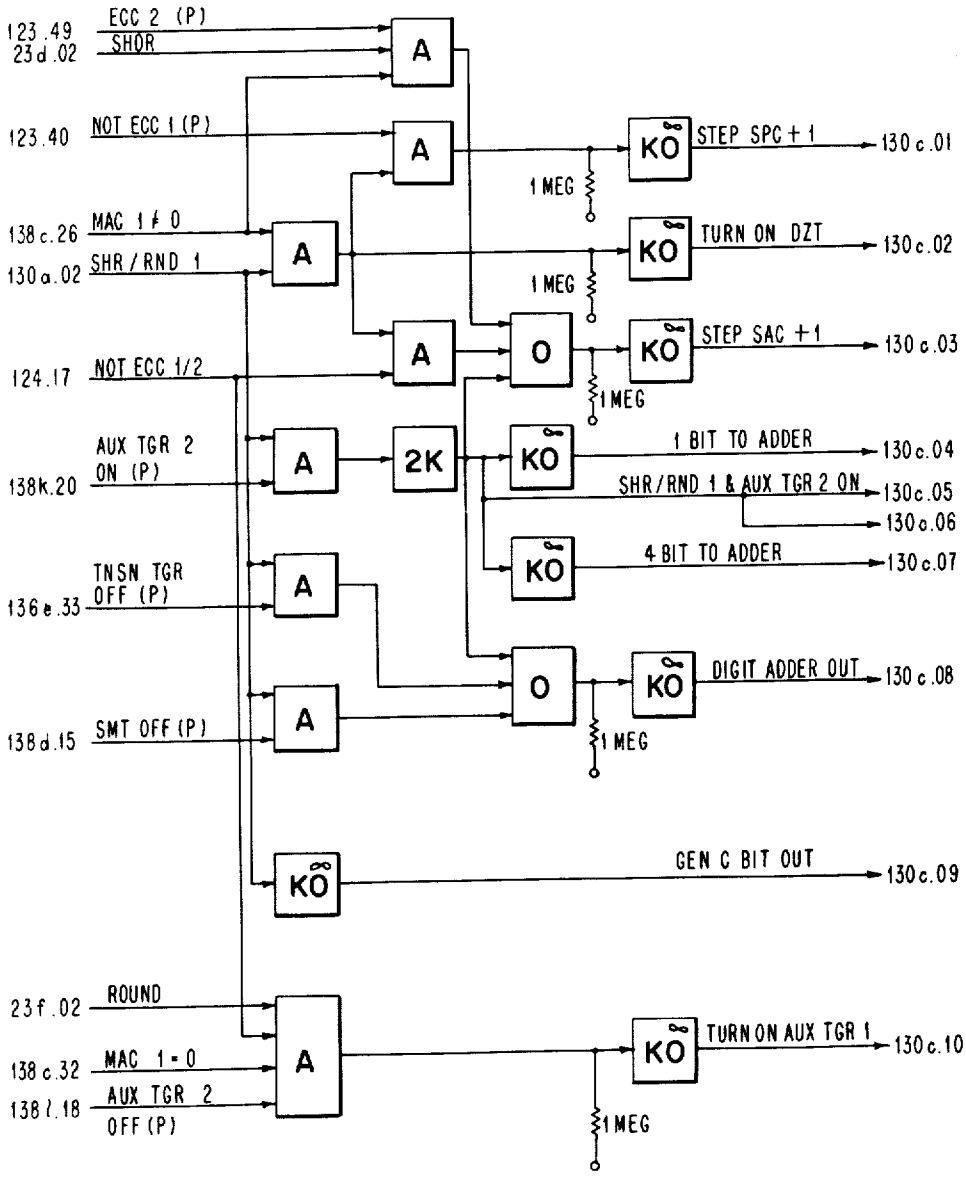
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FIG. 130c

SHORTEN RIGHT/ROUND ROUTING CONTROLS



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FIG. 131

R/W AND READ ROUTING CONTROLS

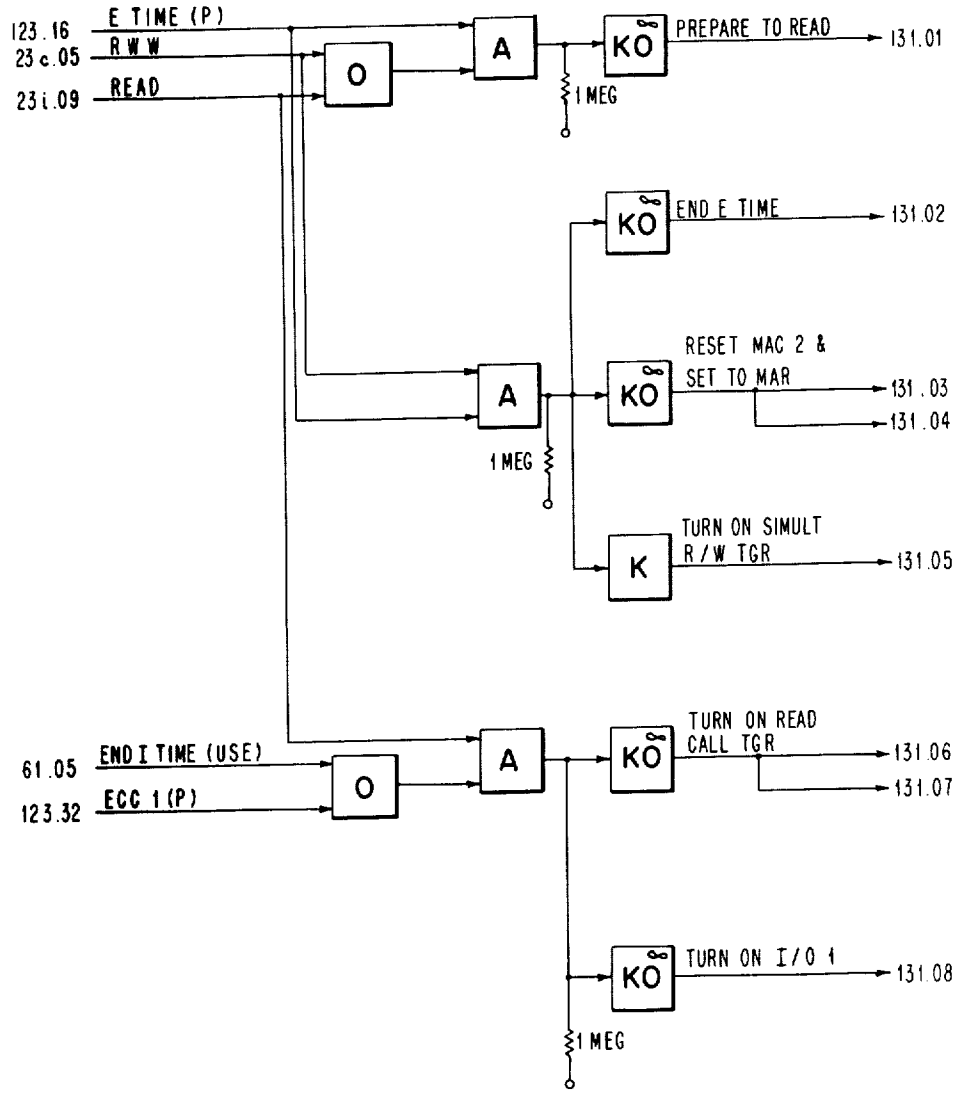
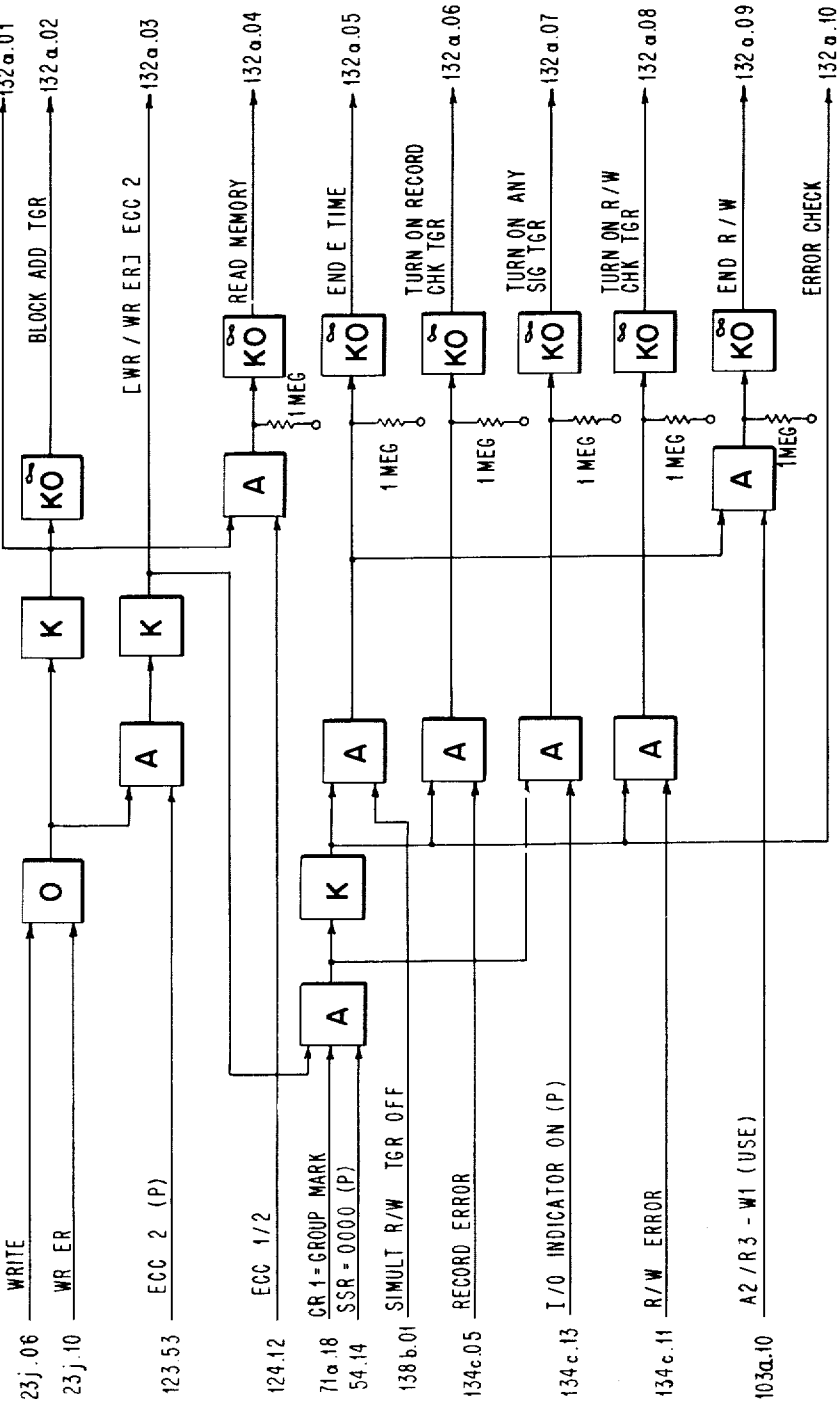


FIG. 132a WRITE-WRITE ERASE ROUTING CONTROLS



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FIG. 132 b

WRITE-WR ER ROUTING CONTROLS

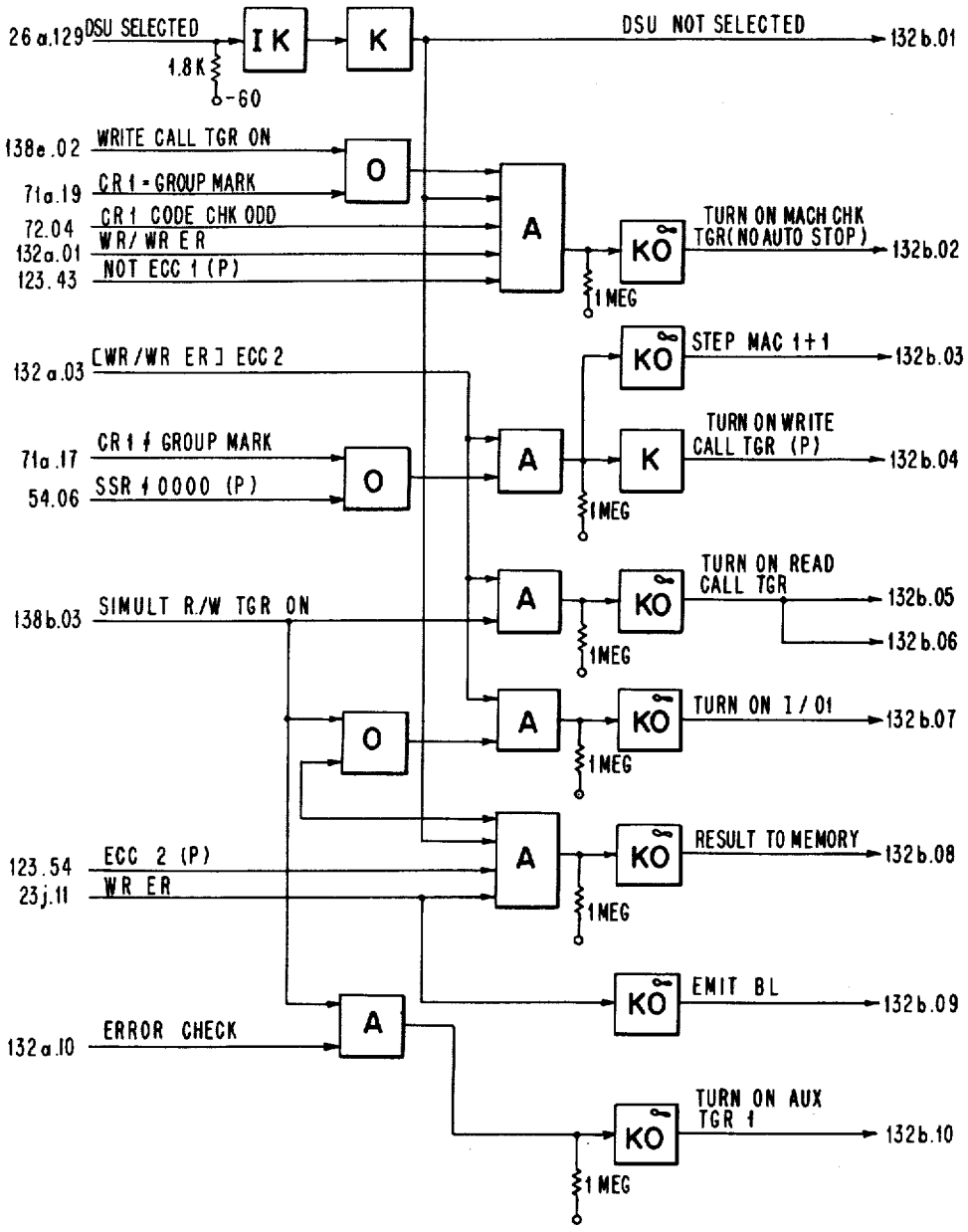


FIG. 133

SELECT & CONTROL ROUTING CONTROLS

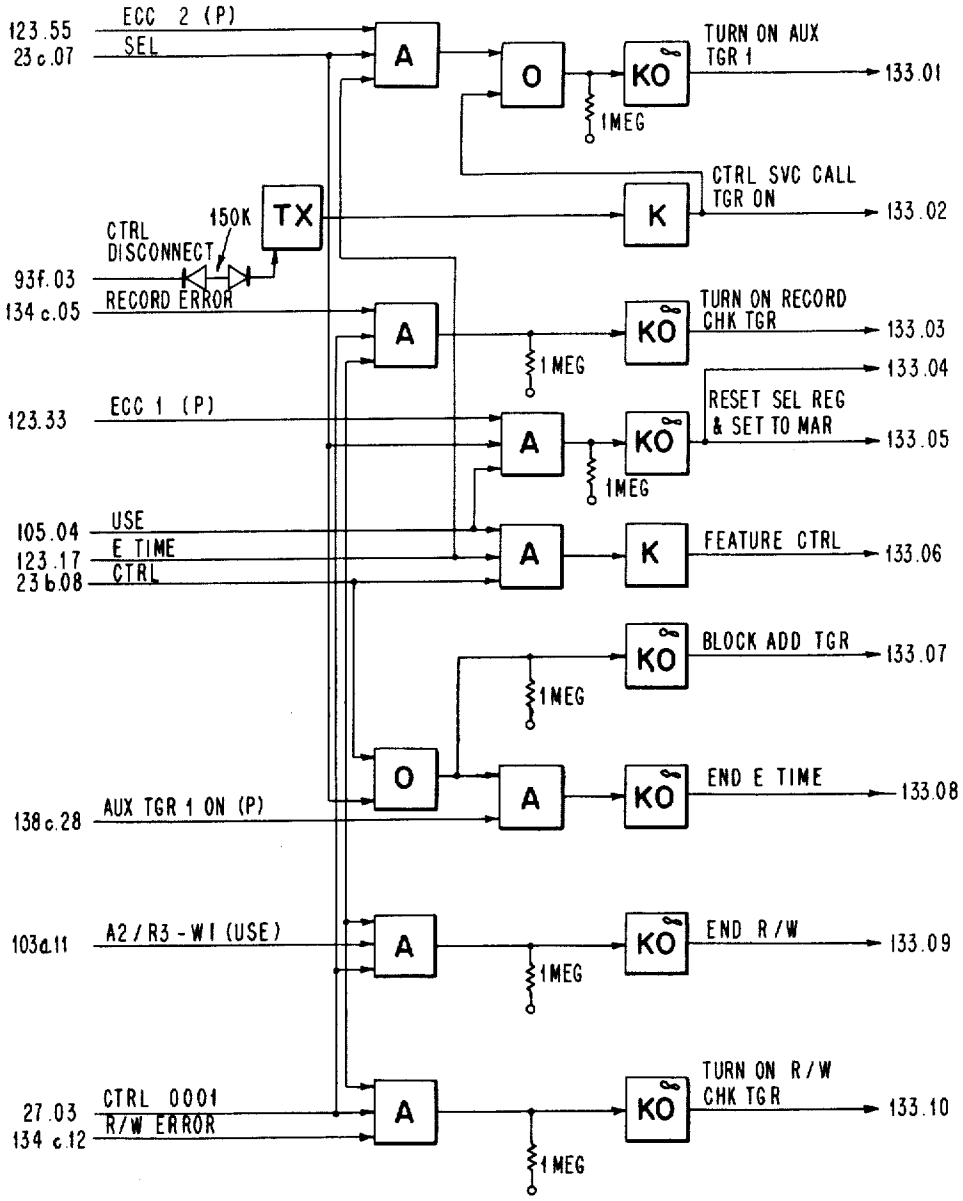
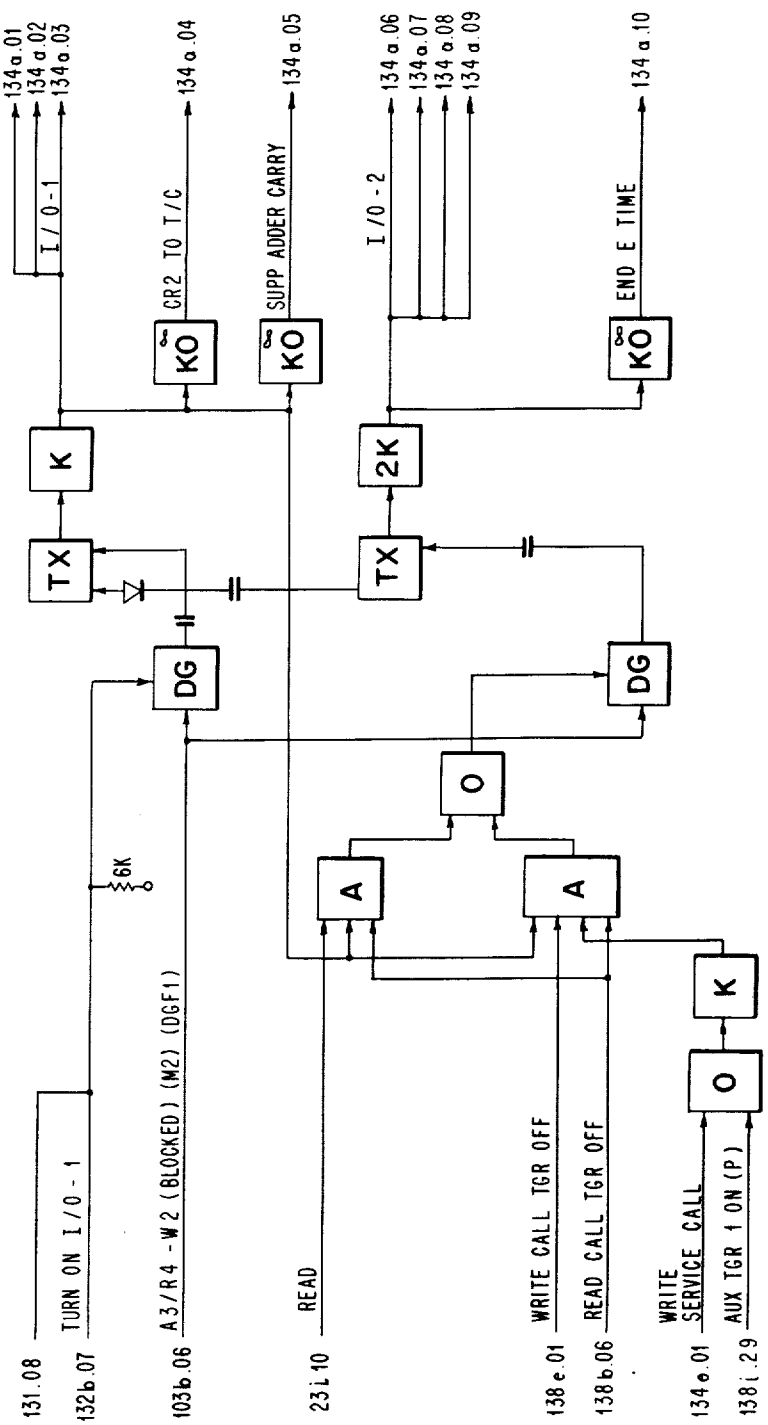


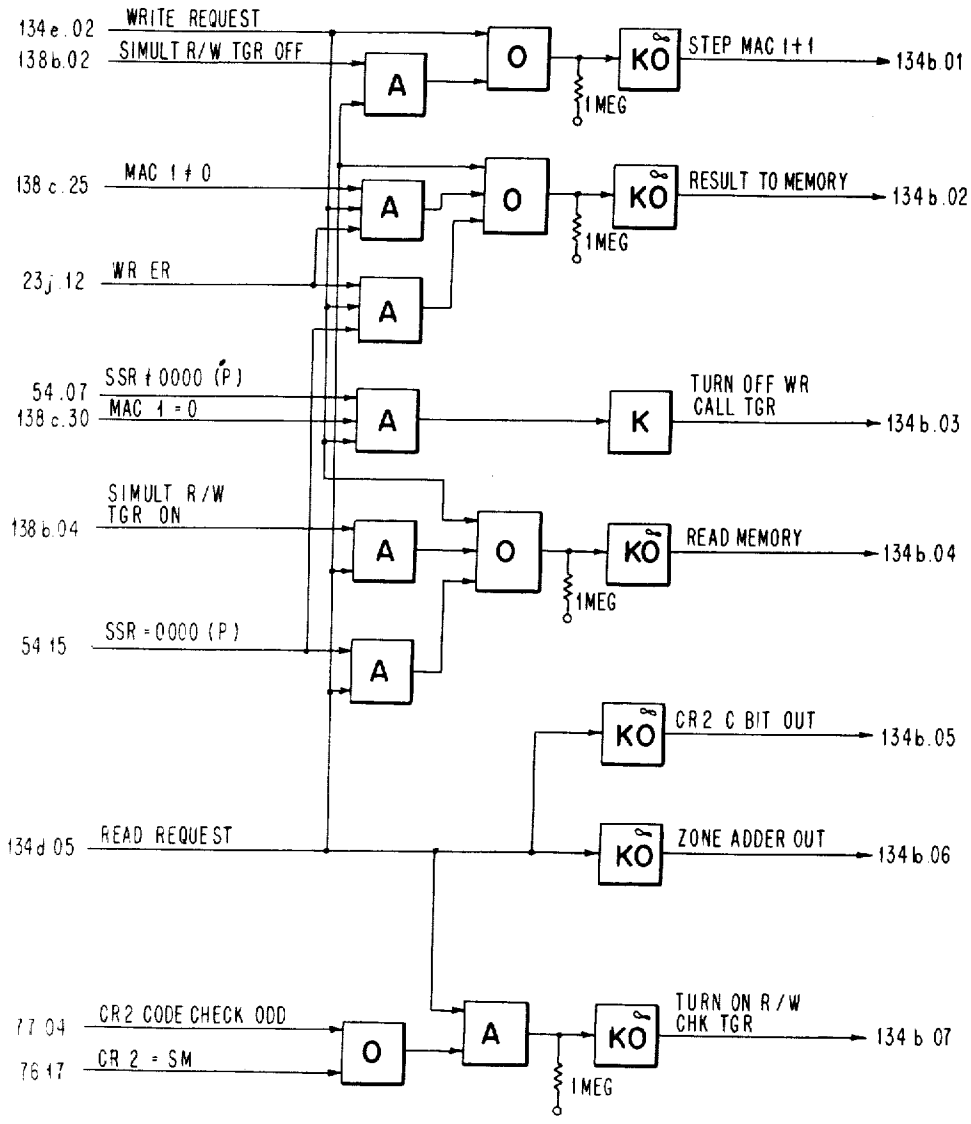
FIG. 134a I/O SEQUENCE 1 & 2 TGRS



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FIG. 134b

I/O SEQUENCE ROUTING



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FIG. 134 c

I/O SEQUENCE ROUTING

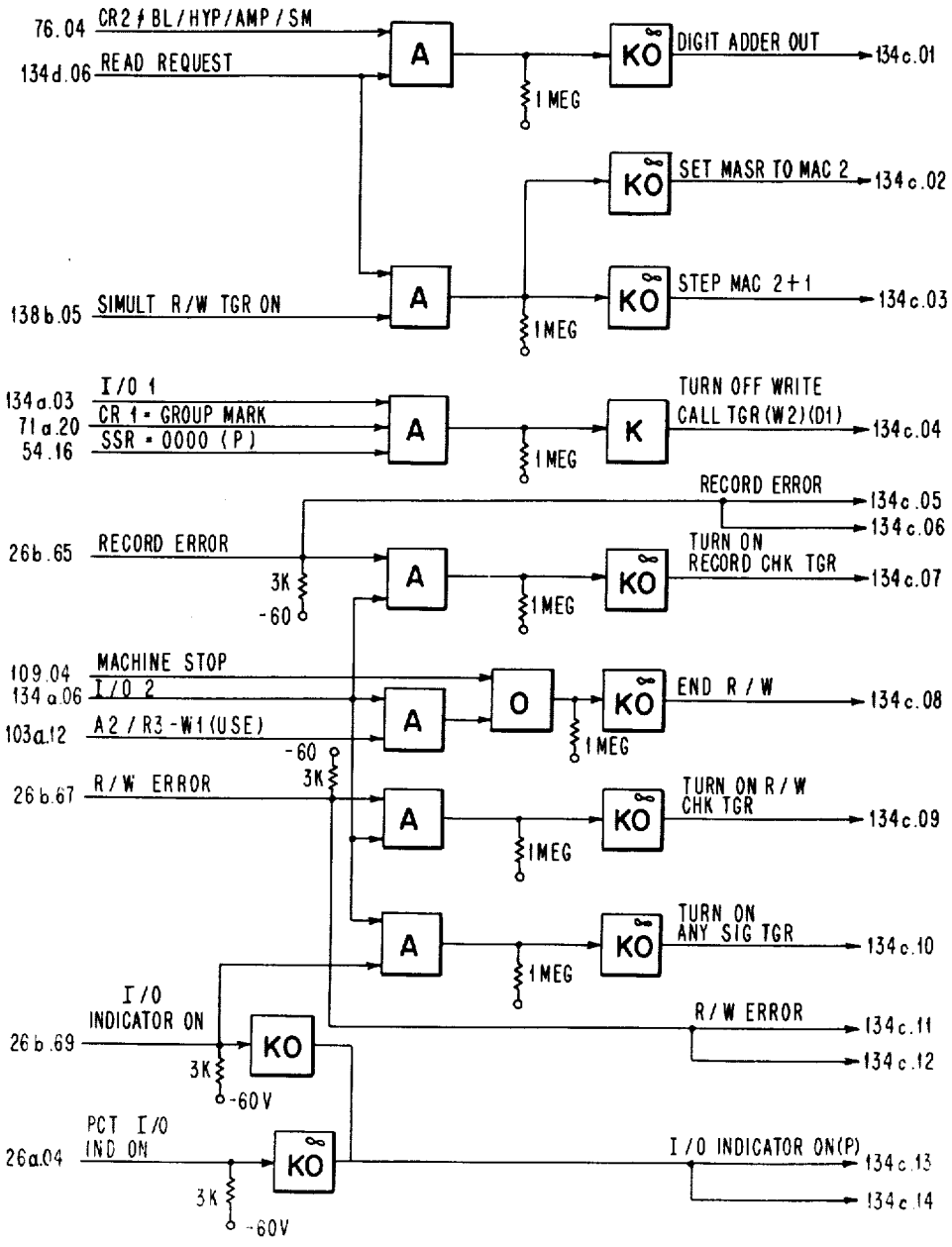


FIG. 134 d

I/O SEQUENCE - READ SERVICE CALL, READ REQUEST TGRS

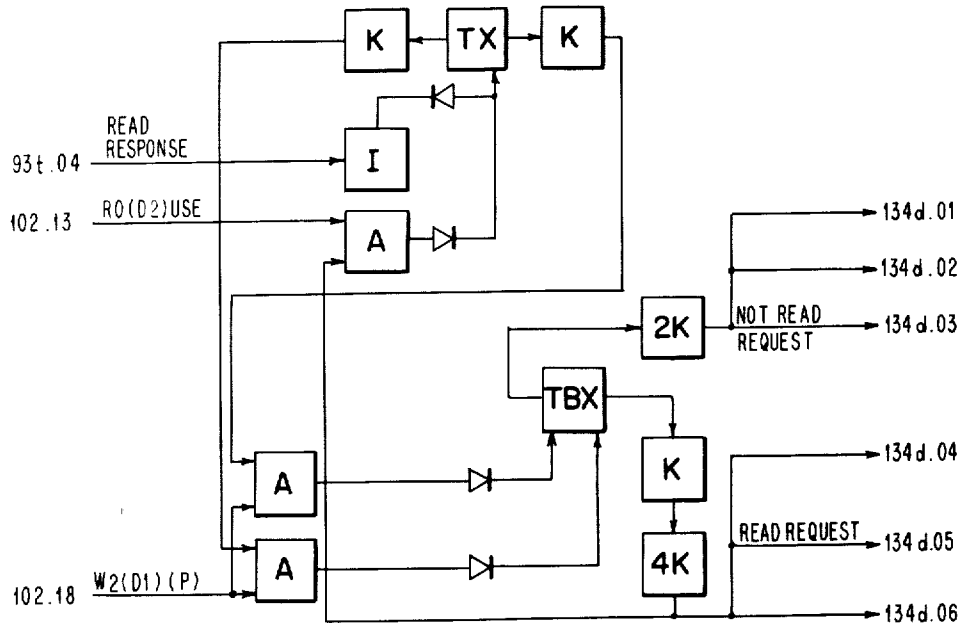


FIG. 134e

I/O SEQUENCE - WRITE SERVICE CALL, REQUEST TGRS

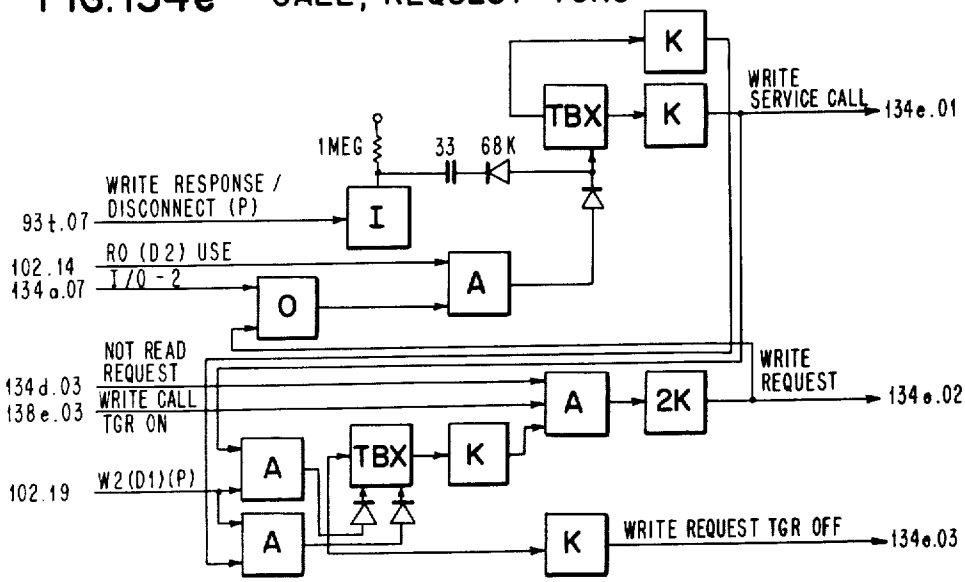


FIG. 134f TRC PULL DOWN PULSE ; I/O SYNC PULSE

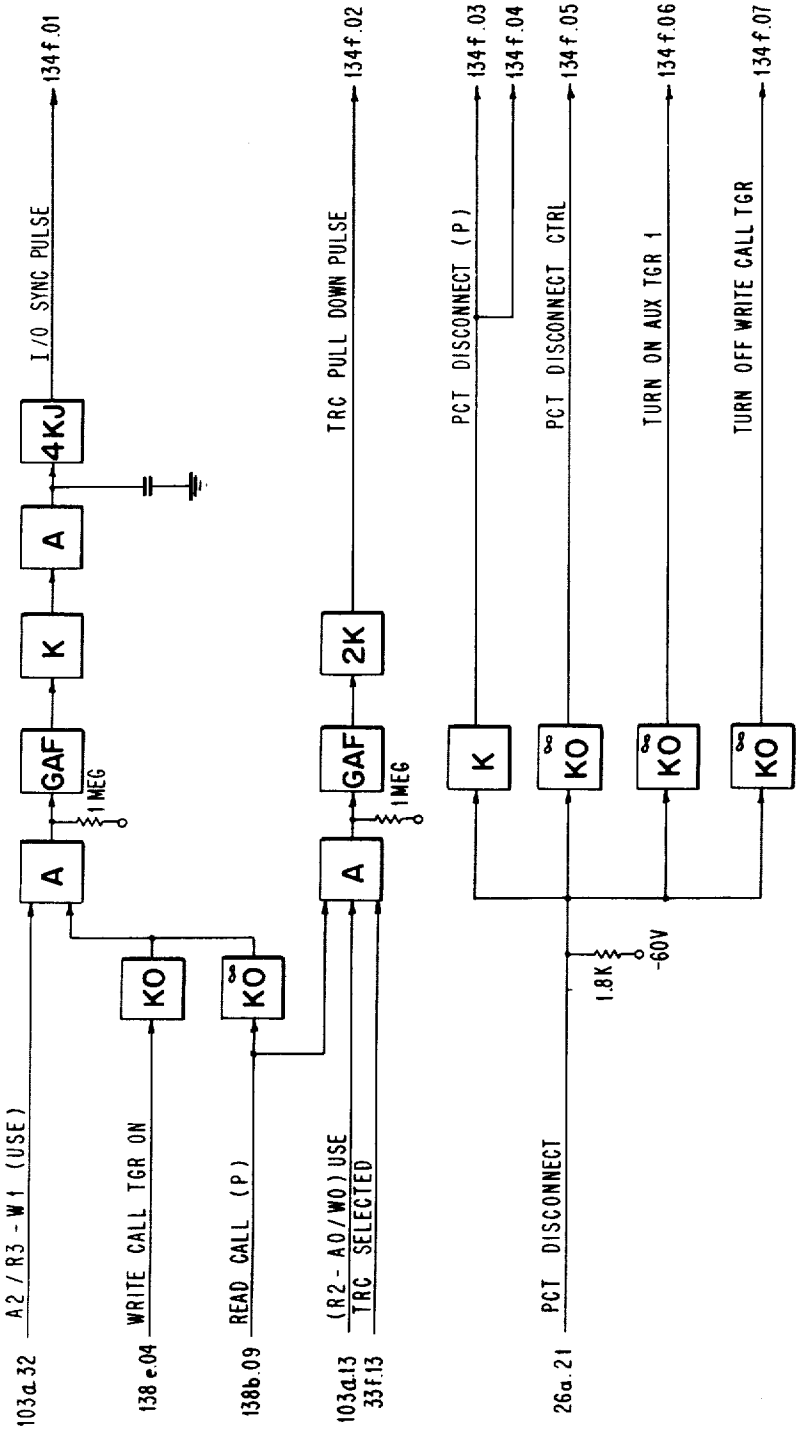


FIG. 135a

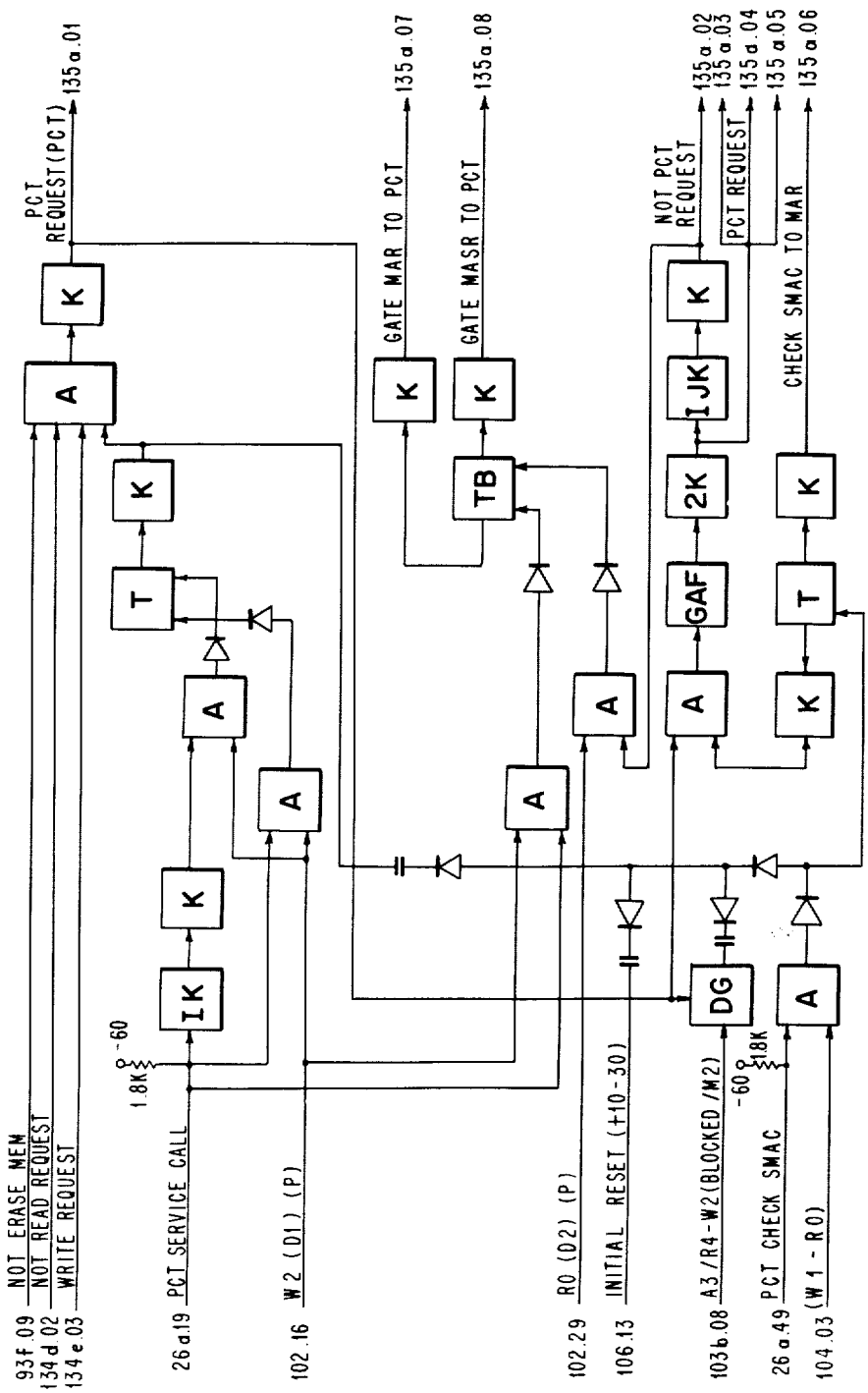
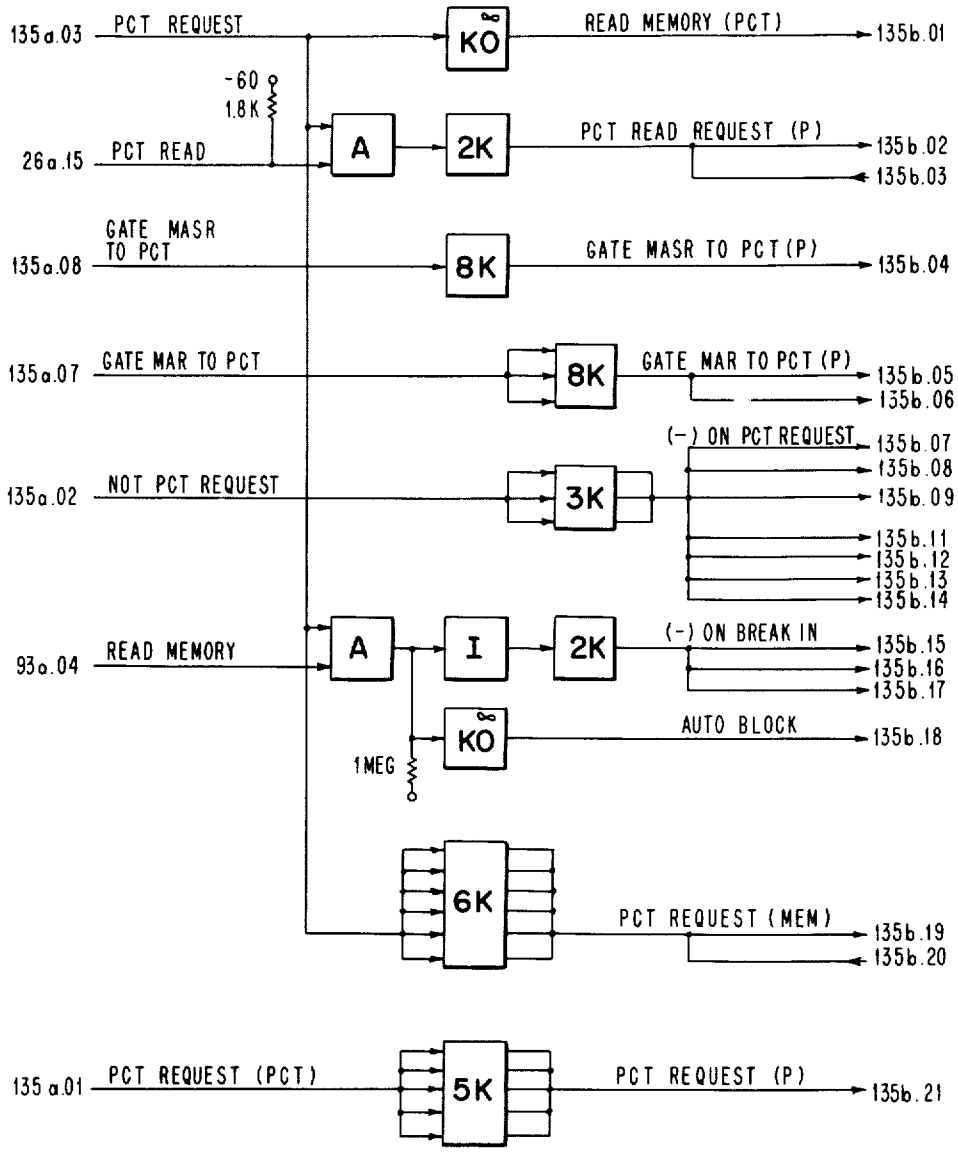

PCT REQUEST, CHK SMAC TO MAR & MASR / MAR GATE TGRS
93f.09 NOT ERASE MEM
134d.02 NOT READ REQUEST
134e.03 WRITE REQUEST
26a.19 PCT SERVICE CALL
102.16 W2 (01) (P)
102.29 R0 (02) (P)
106.13 INITIAL RESET (+10-30)
103b.08 A3/R4-W2(BLOCKED/M2)
26a.49 PCT CHECK SMAC
104.03 (W1 - R0)
1.8K -60
PCT REQUEST (PCT) 135a.01
GATE MAR TO PCT 135a.07
GATE MASR TO PCT 135a.08
NOT PCT REQUEST 135a.02
PCT REQUEST 135a.03
135a.04
135a.05
CHECK SMAC TO MAR 135a.06
K
A
T
IK
TB
GAF
2K
IJK
DG

FIG. 135b

PCT REQUEST EXECUTION CONTROLS



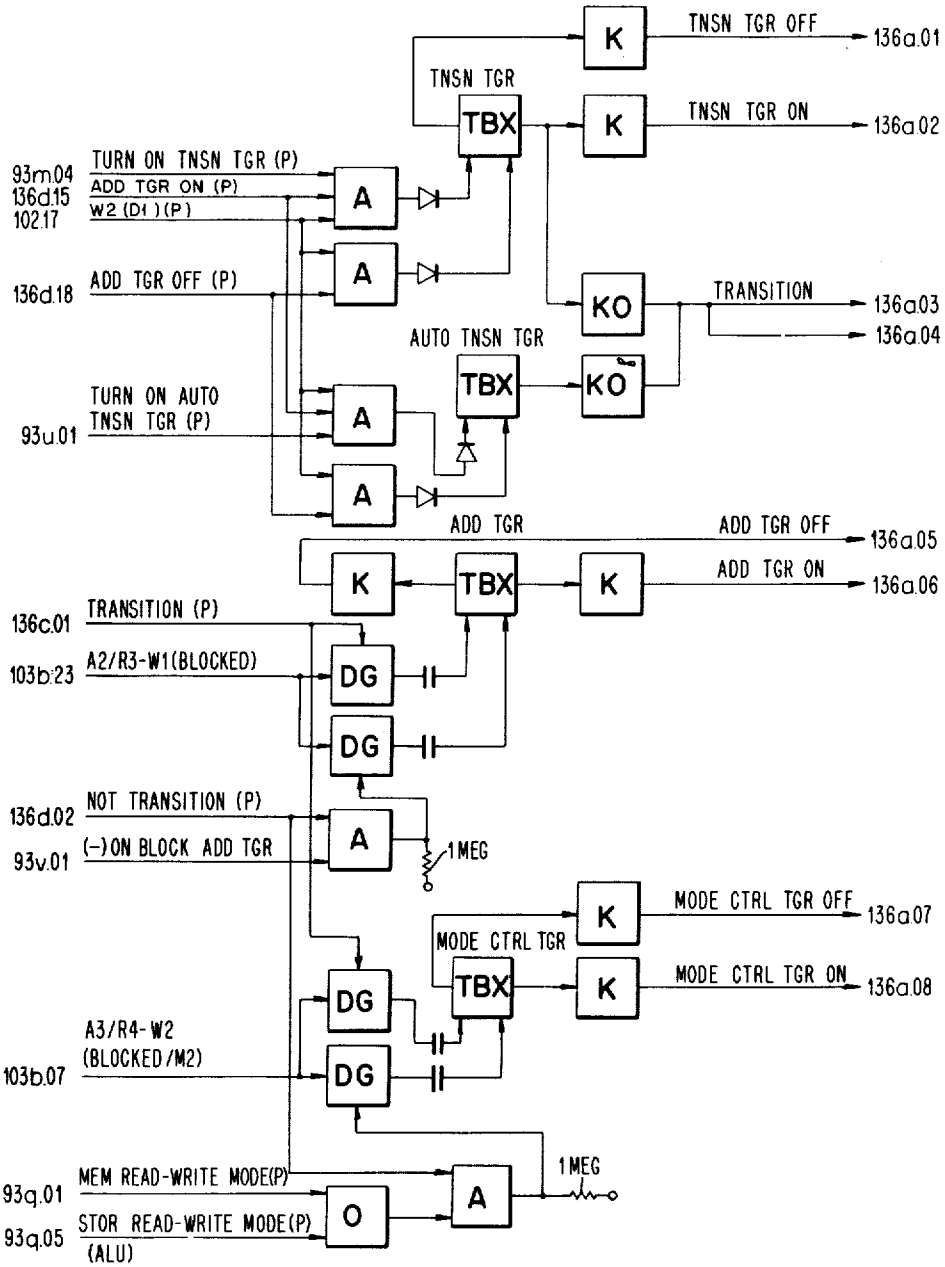
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FIG.136a

OVERLAP CONTROL TRIGGERS



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FIG. 136b OVERLAP EXECUTION CONTROLS

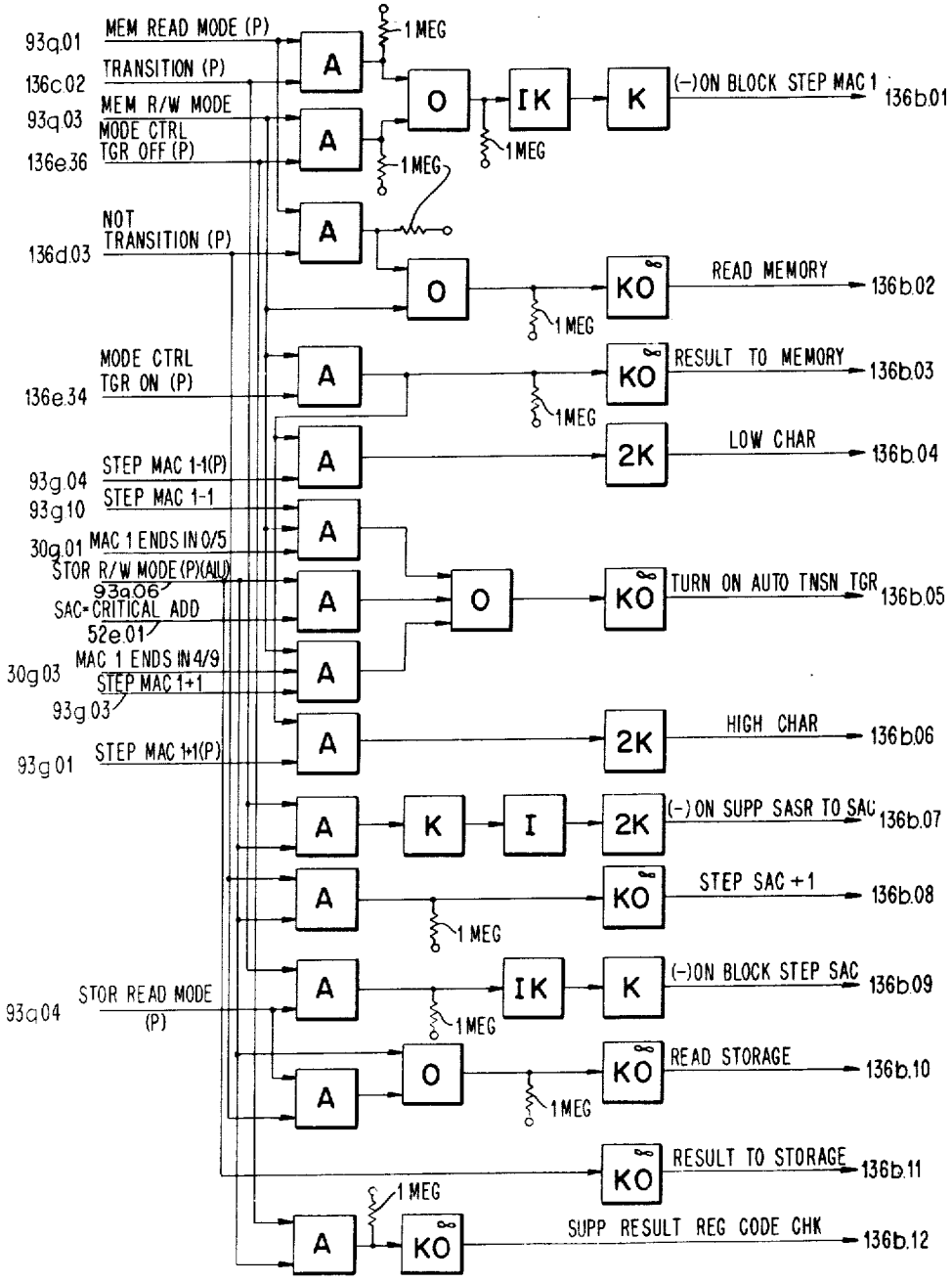


FIG.136c TRANSITION POWERING

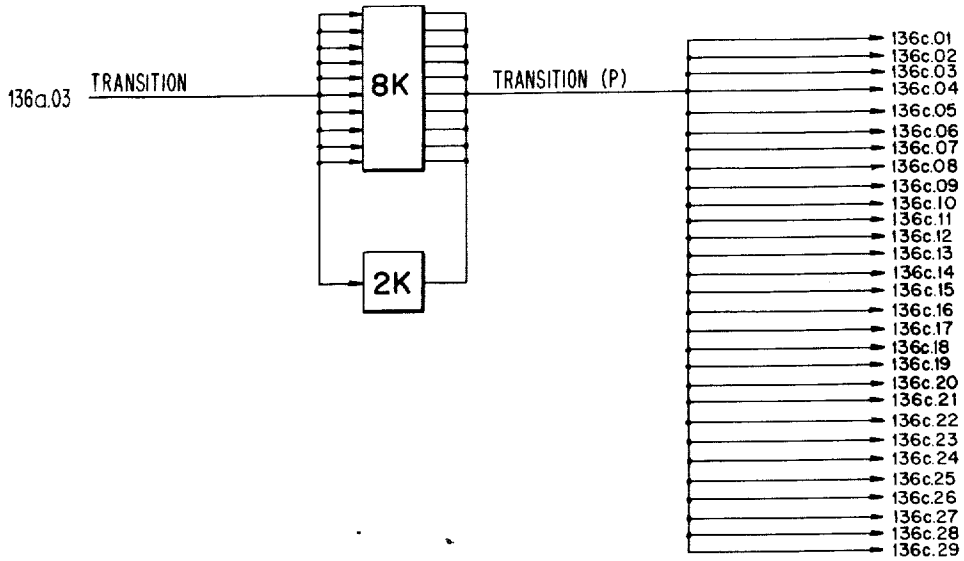


FIG.136d NOT TRANSITION & ADD TGR POWERING

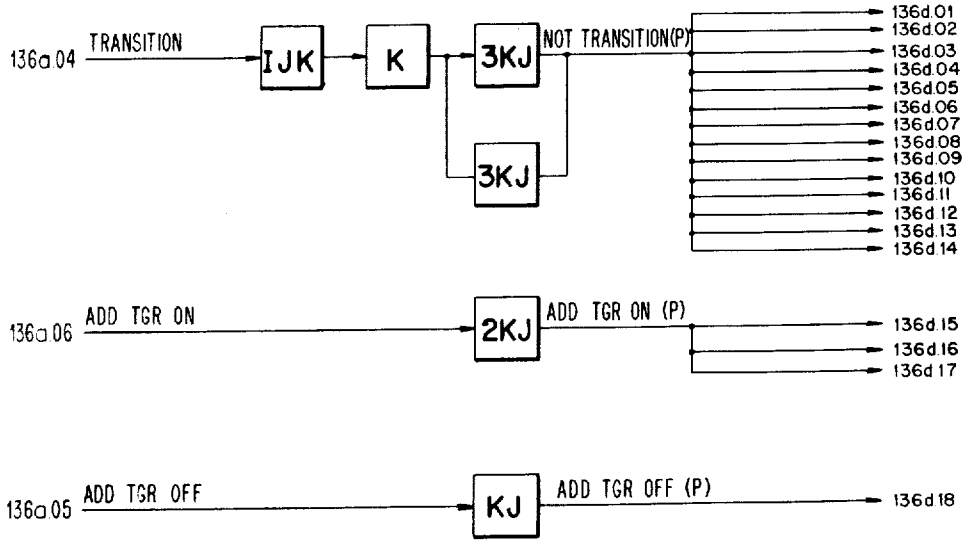


FIG. 136e

TNSN TGR MODE CTRL TGR POWERING

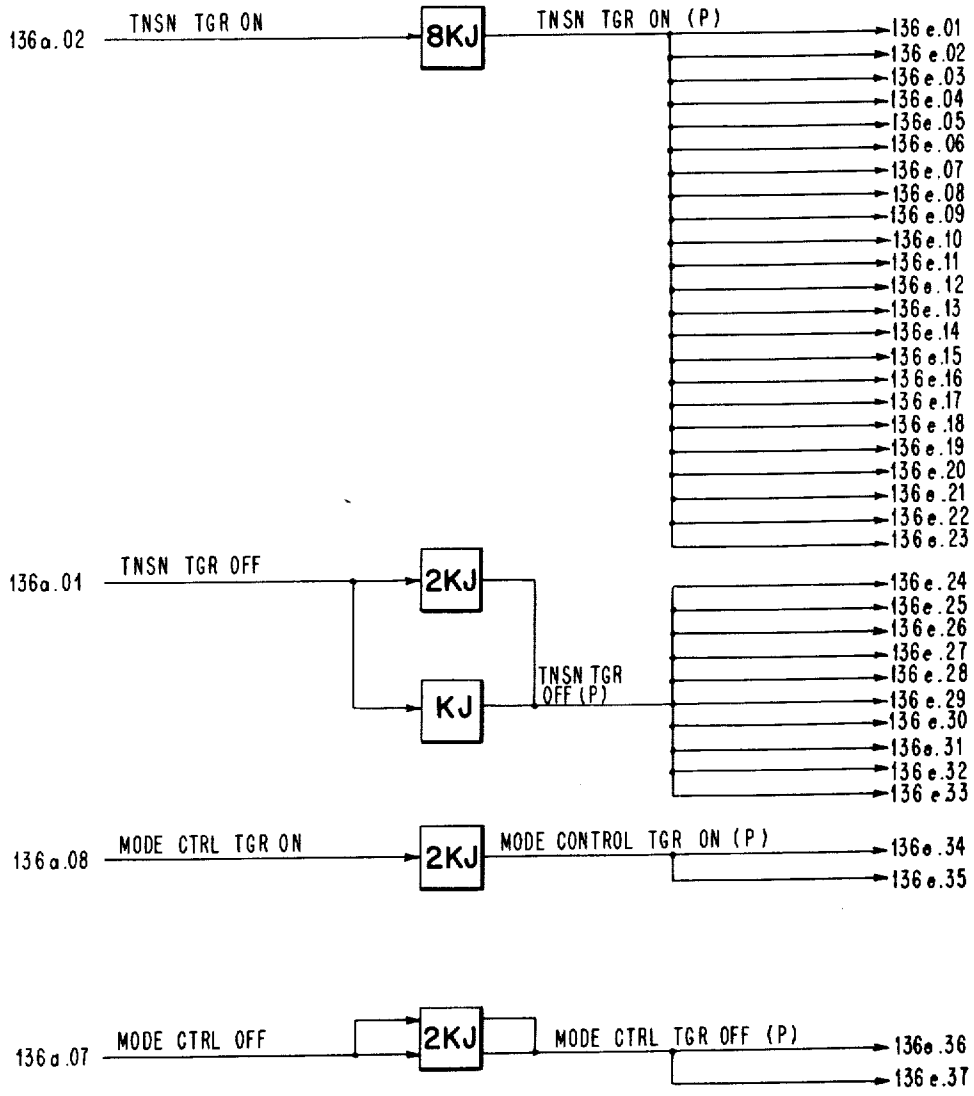


FIG. 137

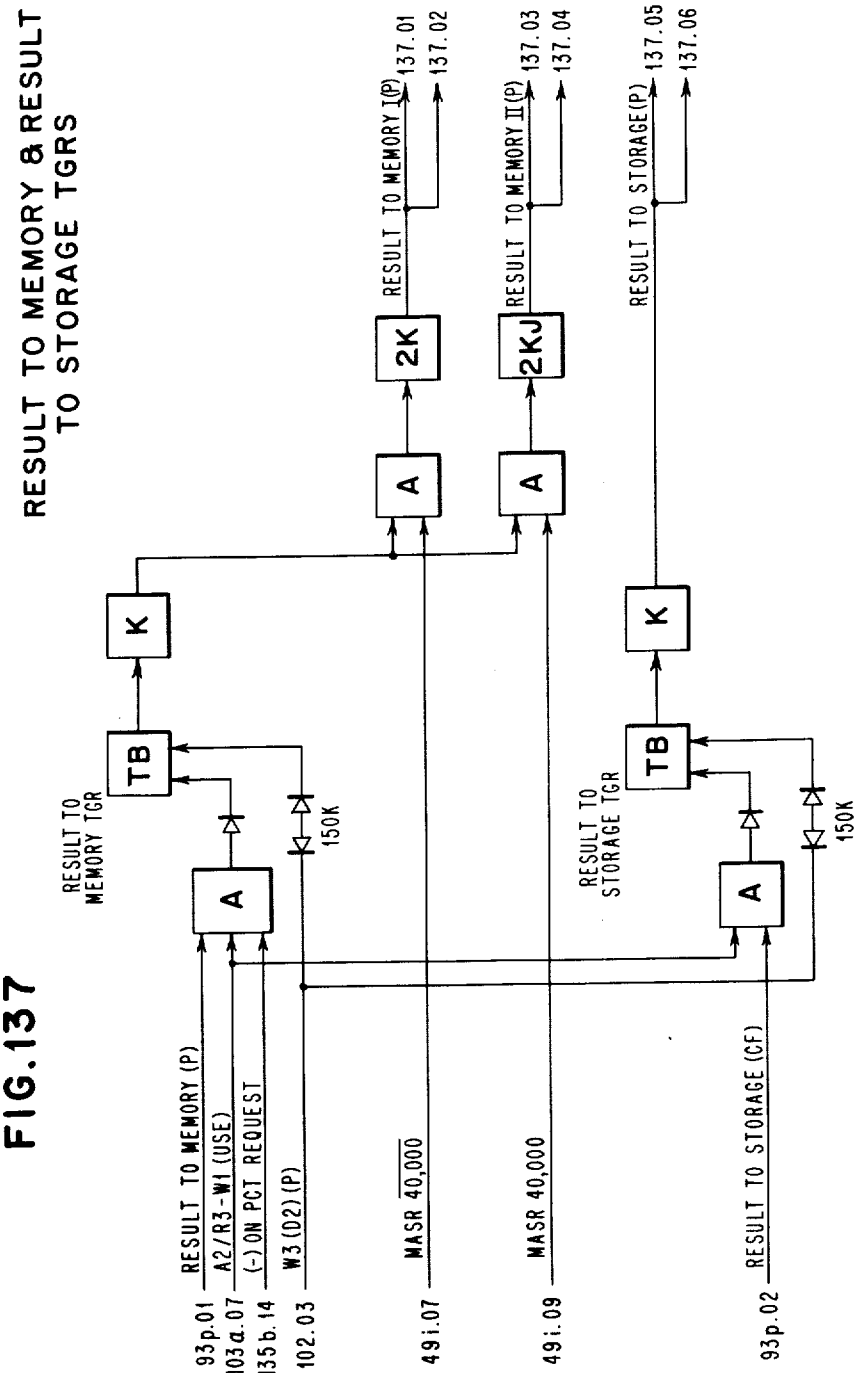
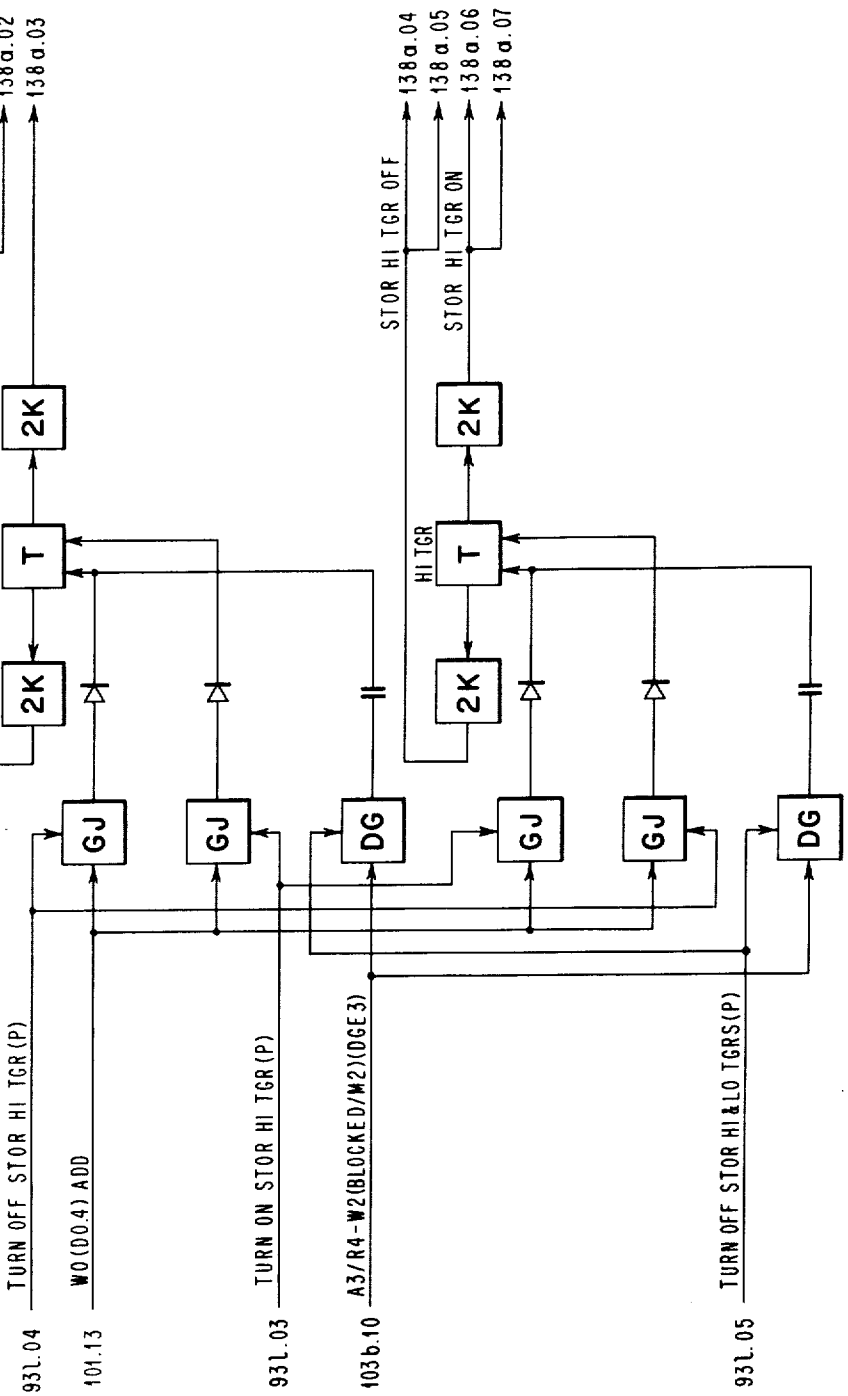

RESULT TO MEMORY & RESULT TO STORAGE TGRS
RESULT TO MEMORY TGR
RESULT TO STORAGE TGR
TB
K
A
2K
2KJ
150K
RESULT TO MEMORY I(P)
RESULT TO MEMORY II(P)
RESULT TO STORAGE(P)
137.01
137.02
137.03
137.04
137.05
137.06
93p.01 RESULT TO MEMORY (P)
103a.07 A2/R3-W1 (USE)
135b.14 (-) ON PCT REQUEST
102.03 W3 (02) (P)
49i.07 MASR 40,000
49i.09 MASR 40,000
93p.02 RESULT TO STORAGE (CF)

FIG. 138a STORAGE HI AND LO TRIGGERS



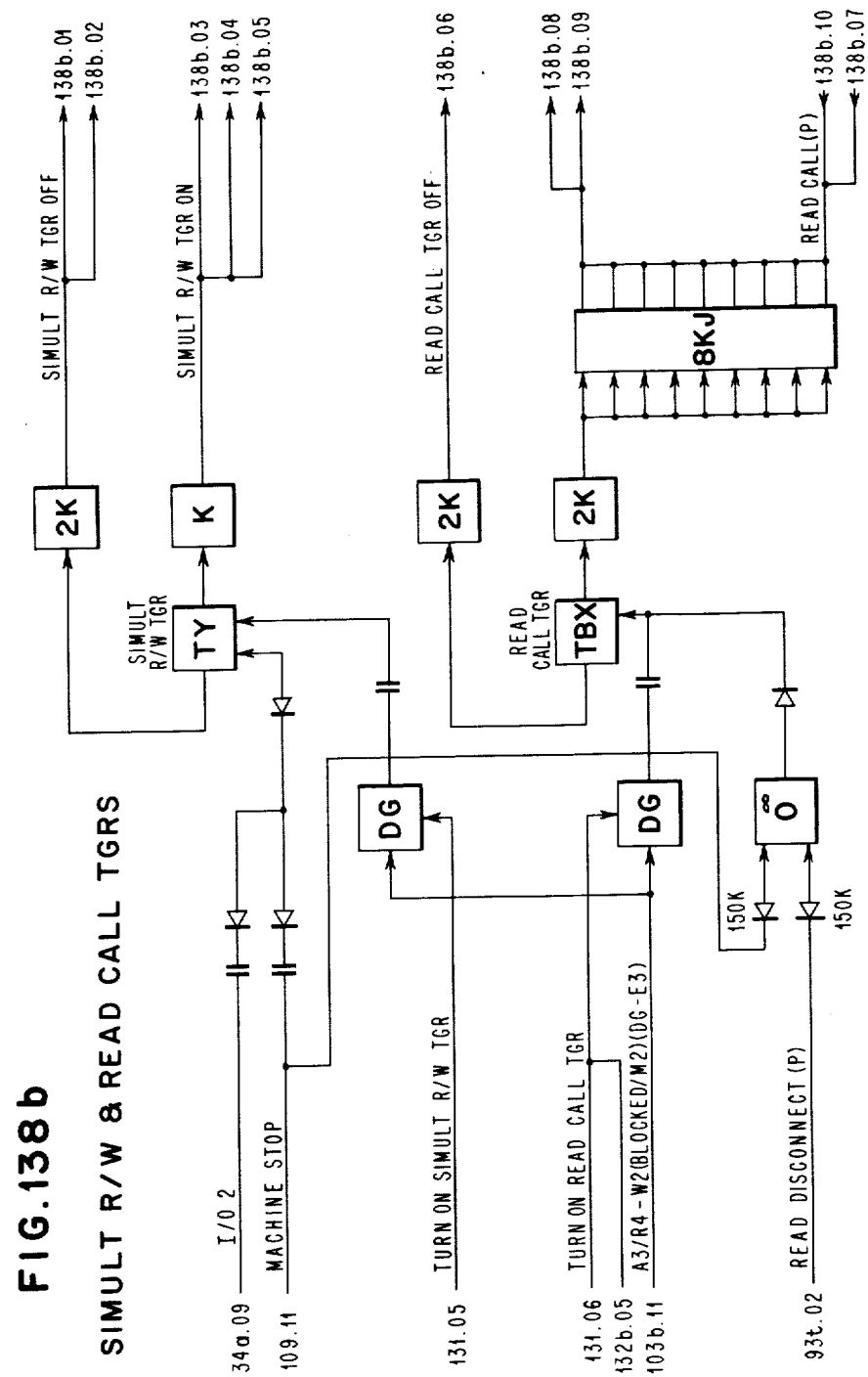


FIG. 138b

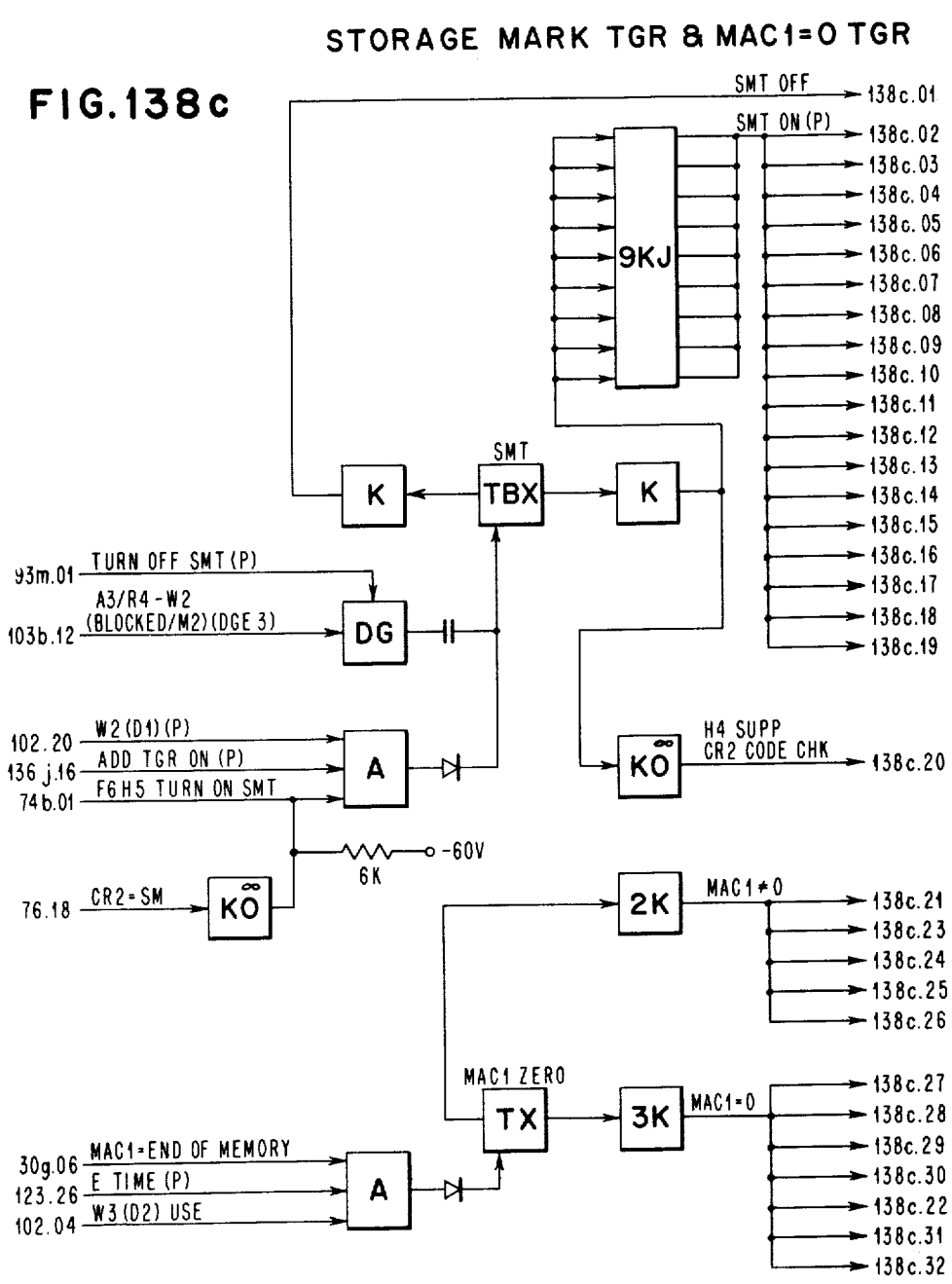
SIMULT R/W & READ CALL TGRS

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FIG. 138c



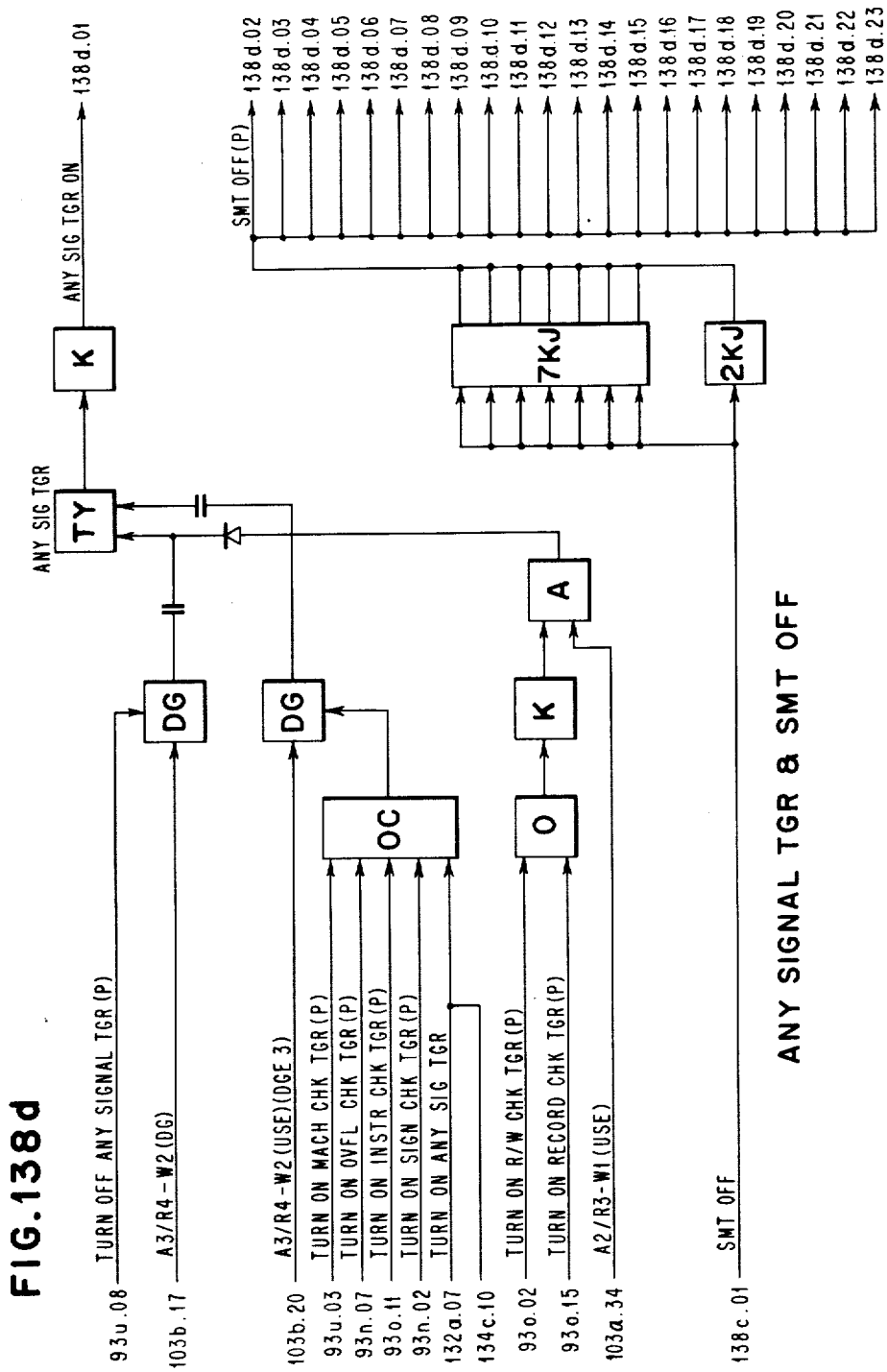

138d.01
ANY SIG TGR ON
K
ANY SIG TGR
TY
SMT OFF(P)
138d.02
138d.03
138d.04
138d.05
138d.06
138d.07
138d.08
138d.09
138d.10
138d.11
138d.12
138d.13
138d.14
138d.15
138d.16
138d.17
138d.18
138d.19
138d.20
138d.21
138d.22
138d.23
7KJ
2KJ
A
K
O
DG
DG
OC
93u.08 TURN OFF ANY SIGNAL TGR (P)
103b.17 A3/R4-W2(DG)
103b.20 A3/R4-W2(USE)(DGE 3)
93u.03 TURN ON MACH CHK TGR(P)
93n.07 TURN ON OVFL CHK TGR(P)
93o.11 TURN ON INSTR CHK TGR(P)
93n.02 TURN ON SIGN CHK TGR(P)
132a.07 TURN ON ANY SIG TGR
134c.10
93o.02 TURN ON R/W CHK TGR(P)
93o.15 TURN ON RECORD CHK TGR(P)
103a.34 A2/R3-W1(USE)
138c.01 SMT OFF
ANY SIGNAL TGR & SMT OFF

FIG.138d

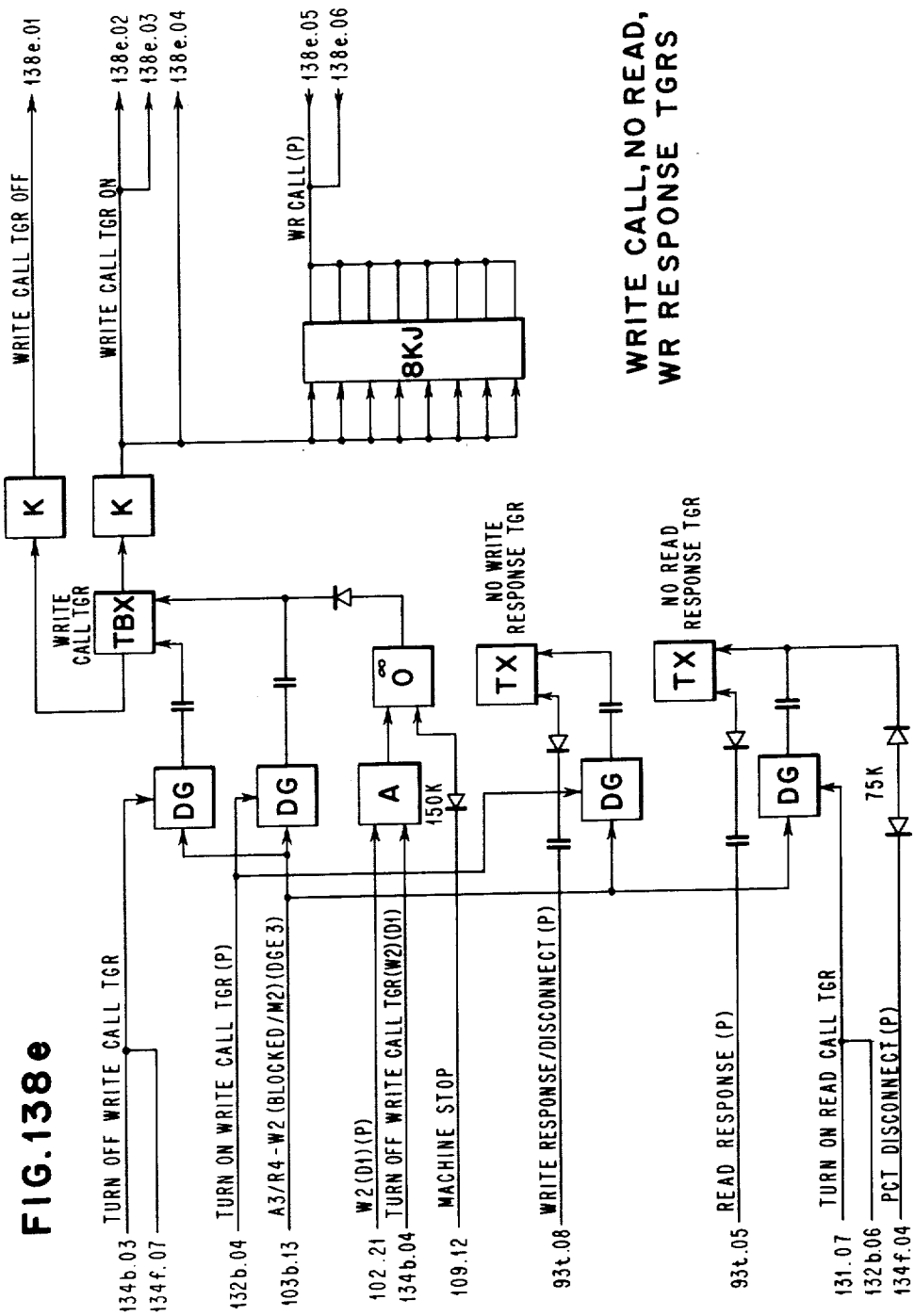

WRITE CALL, NO READ, WR RESPONSE TGRS
WRITE CALL TGR OFF
WRITE CALL TGR ON
WR CALL (P)
138e.01
138e.02
138e.03
138e.04
138e.05
138e.06
8KJ
K
K
WRITE CALL TGR
TBX
DG
DG
A
O
150K
TX
NO WRITE RESPONSE TGR
DG
TX
NO READ RESPONSE TGR
DG
75K
TURN OFF WRITE CALL TGR
134b.03
134f.07
TURN ON WRITE CALL TGR (P)
132b.04
A3/R4-W2 (BLOCKED/W2)(OGE3)
103b.13
W2(D1)(P)
102.21
TURN OFF WRITE CALL TGR(W2)(D1)
134b.04
MACHINE STOP
109.12
WRITE RESPONSE/DISCONNECT (P)
93t.08
READ RESPONSE (P)
93t.05
TURN ON READ CALL TGR
131.07
PCT DISCONNECT (P)
132b.06
134f.04

FIG. 138e

FIG. 138f

INST. CHK. MACH. CHK, & R/W CHK. TGRS.

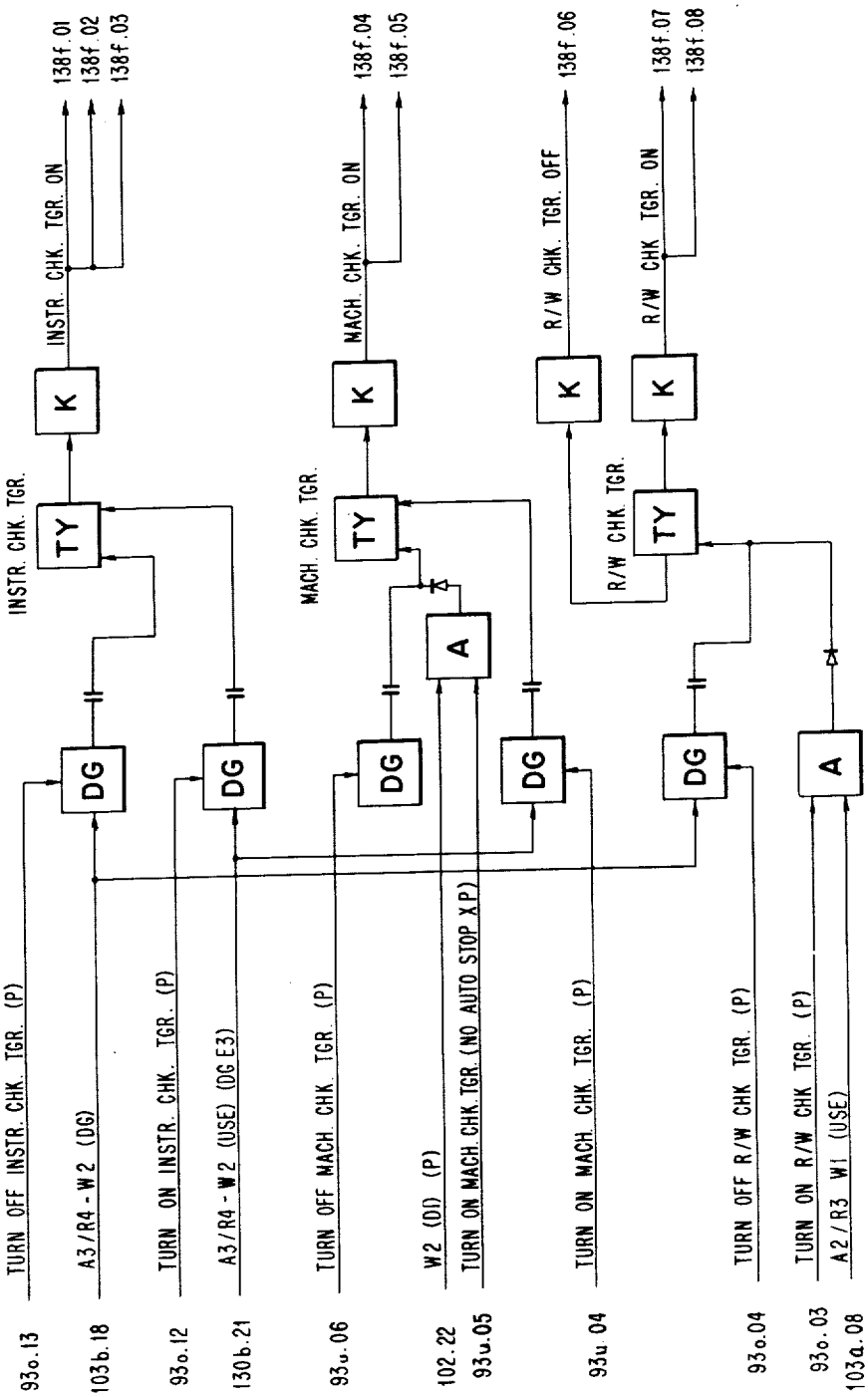


FIG. 138g
RECORD, OVFL, & SIGN-CHK. TGRS.

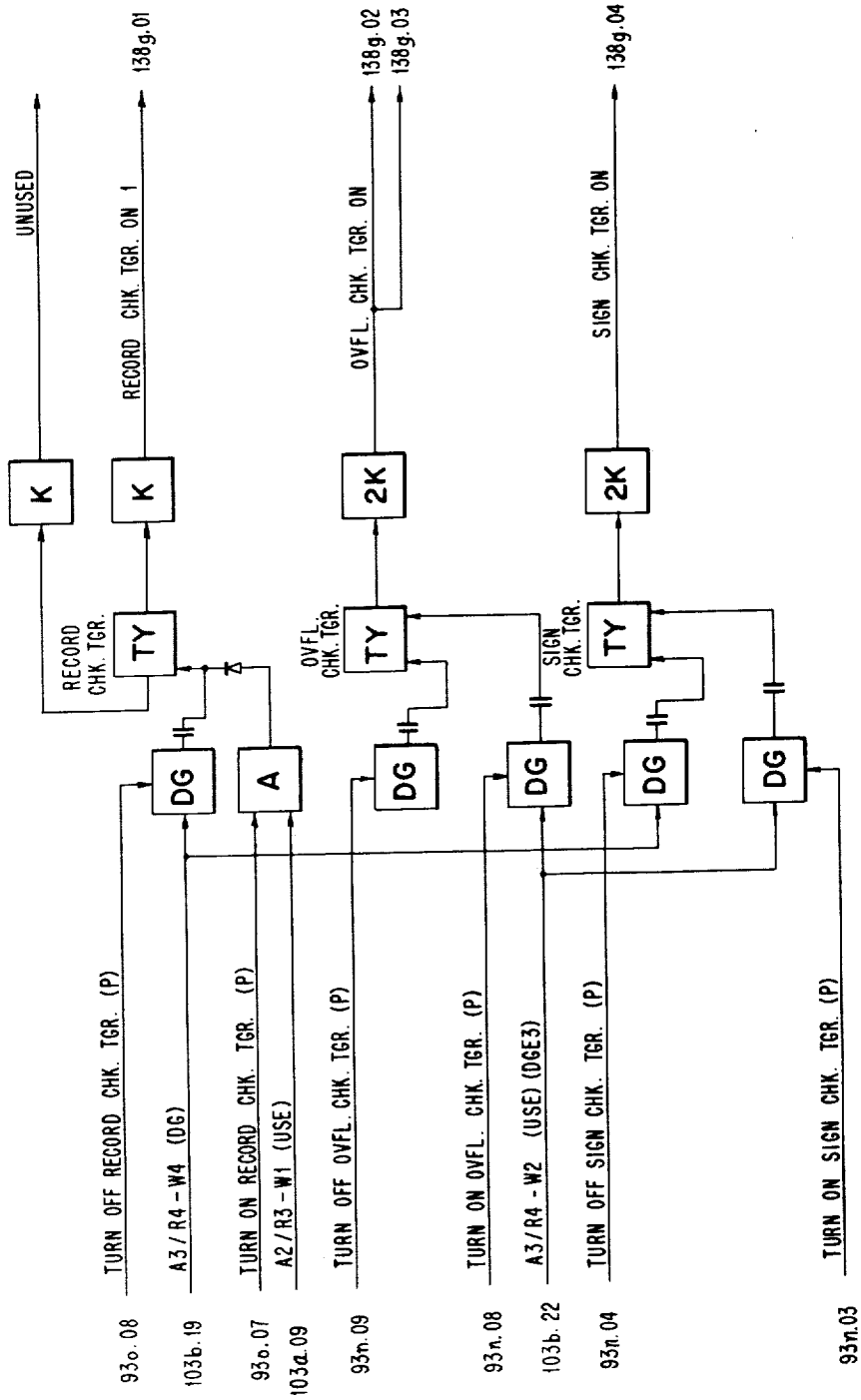


FIG. 138h

DIGIT ZERO TGRS. & REMAINDER TGR.

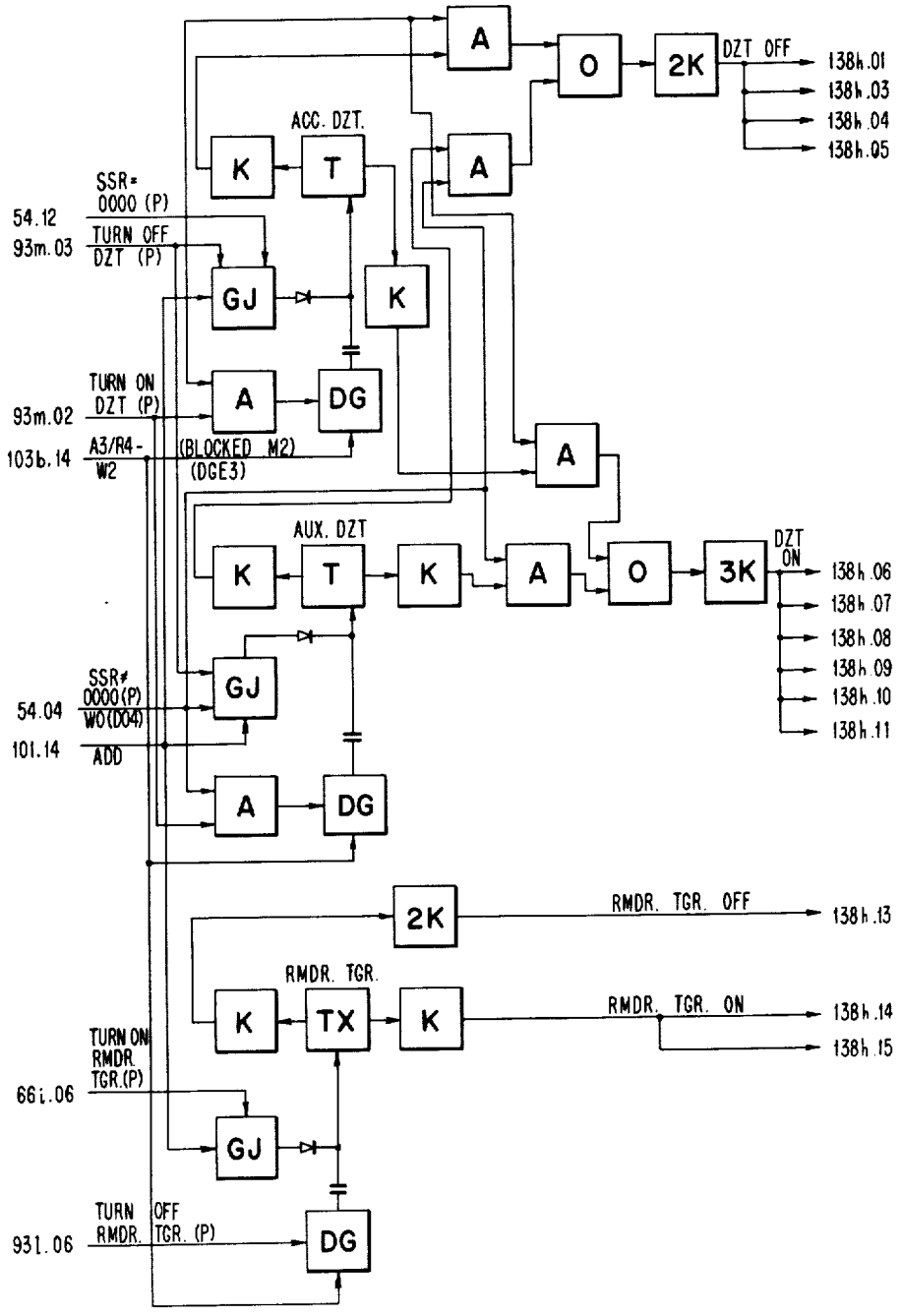


FIG. 138 i

AUXILIARY TGR. 1

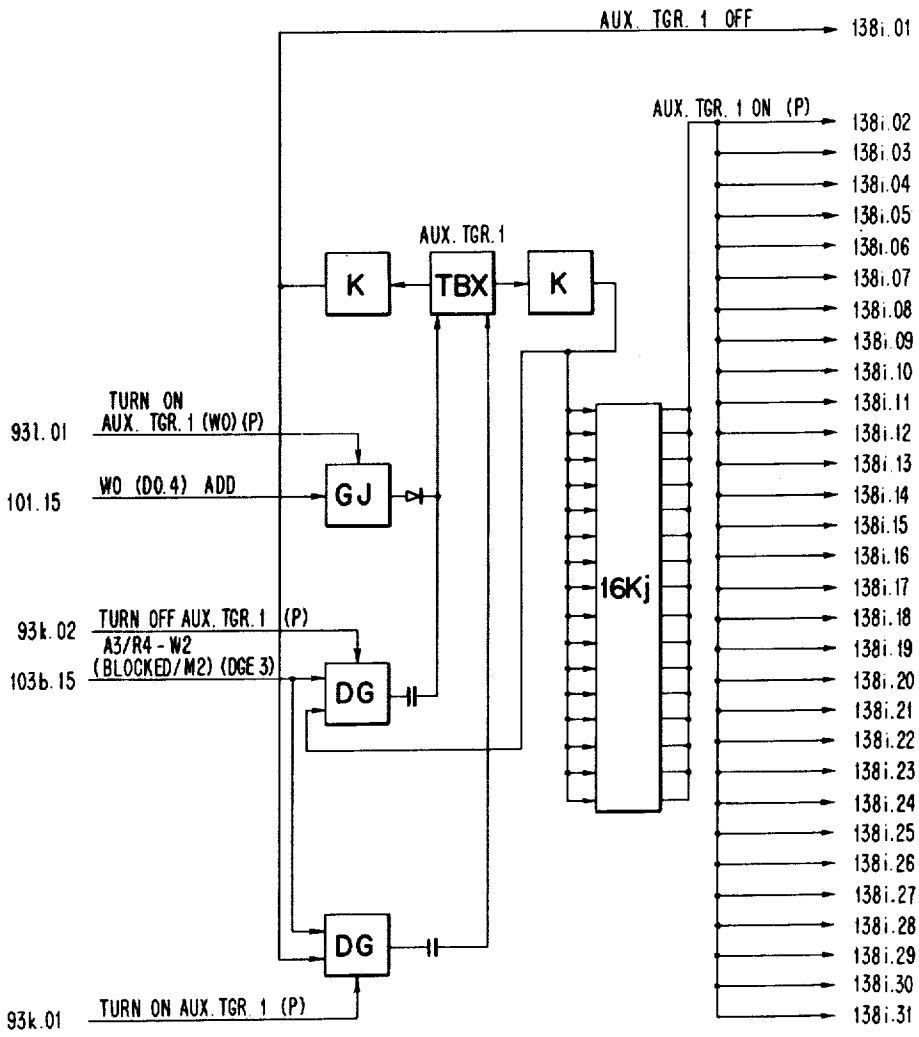


FIG. 138j
AUXILIARY TGR. 1 OFF POWERING

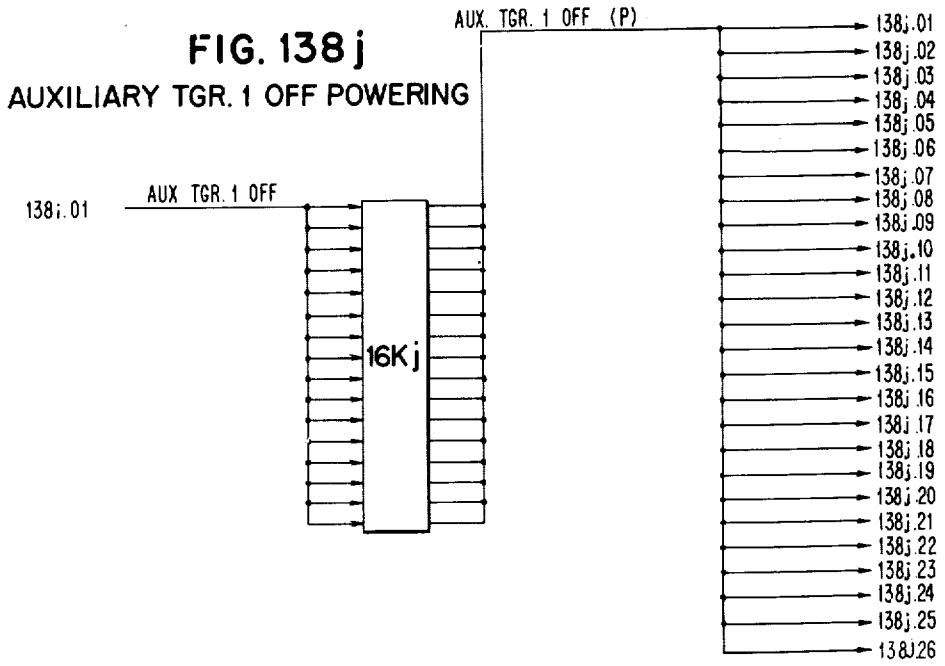


FIG. 1381
AUXILIARY TGR. 2 OFF POWERING

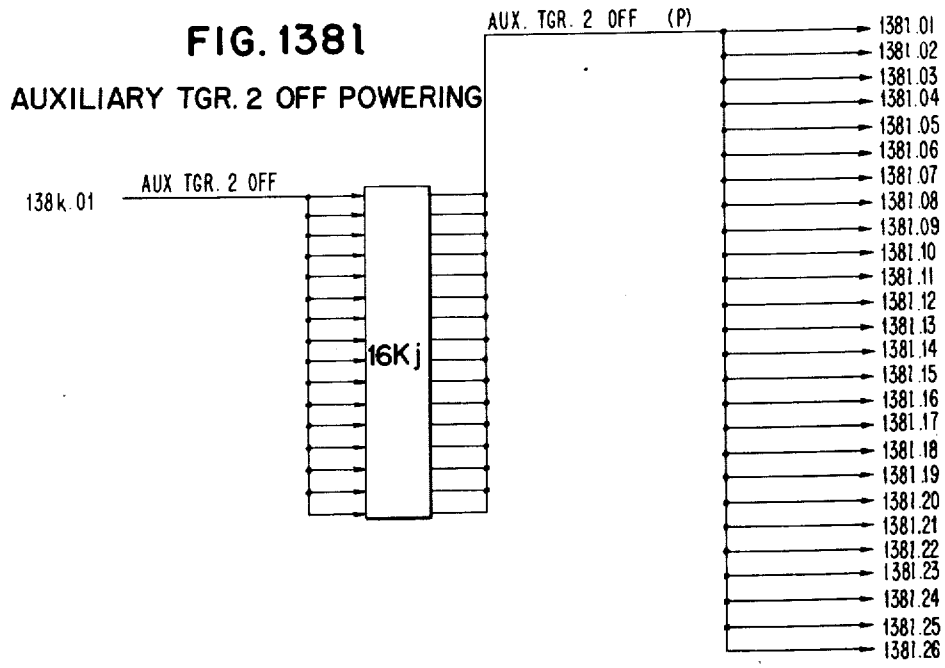


FIG. 138k

AUXILIARY TGR. 2

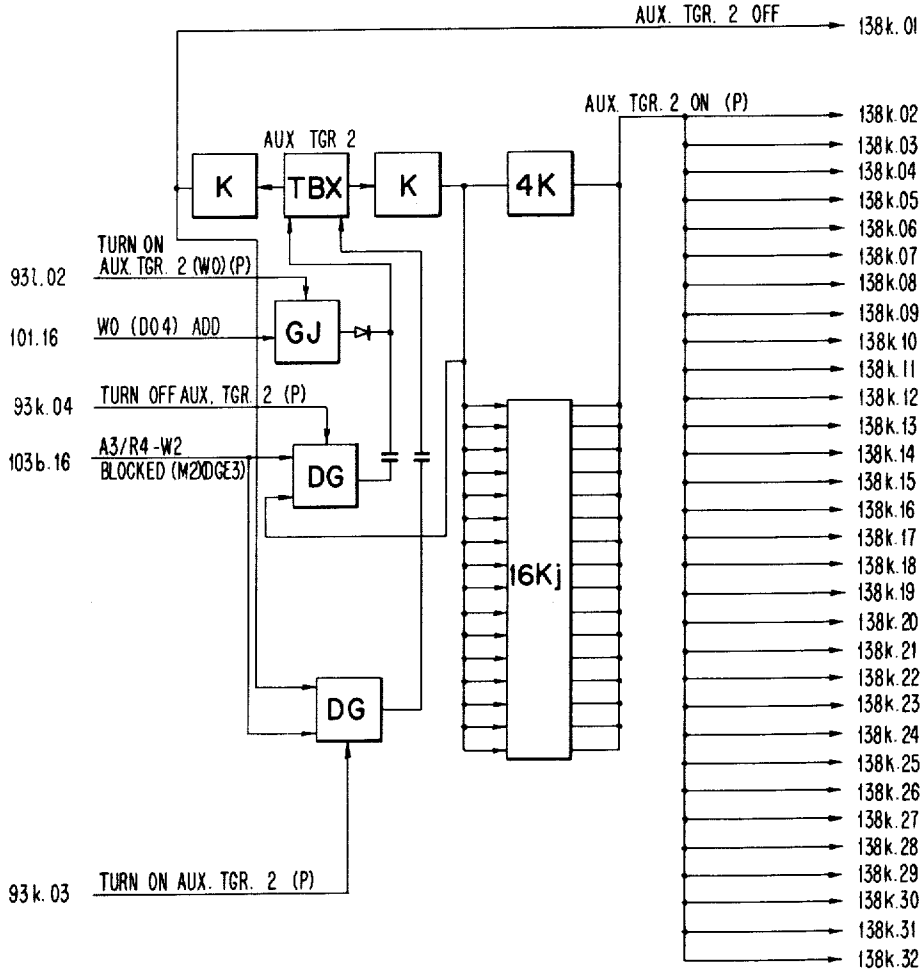
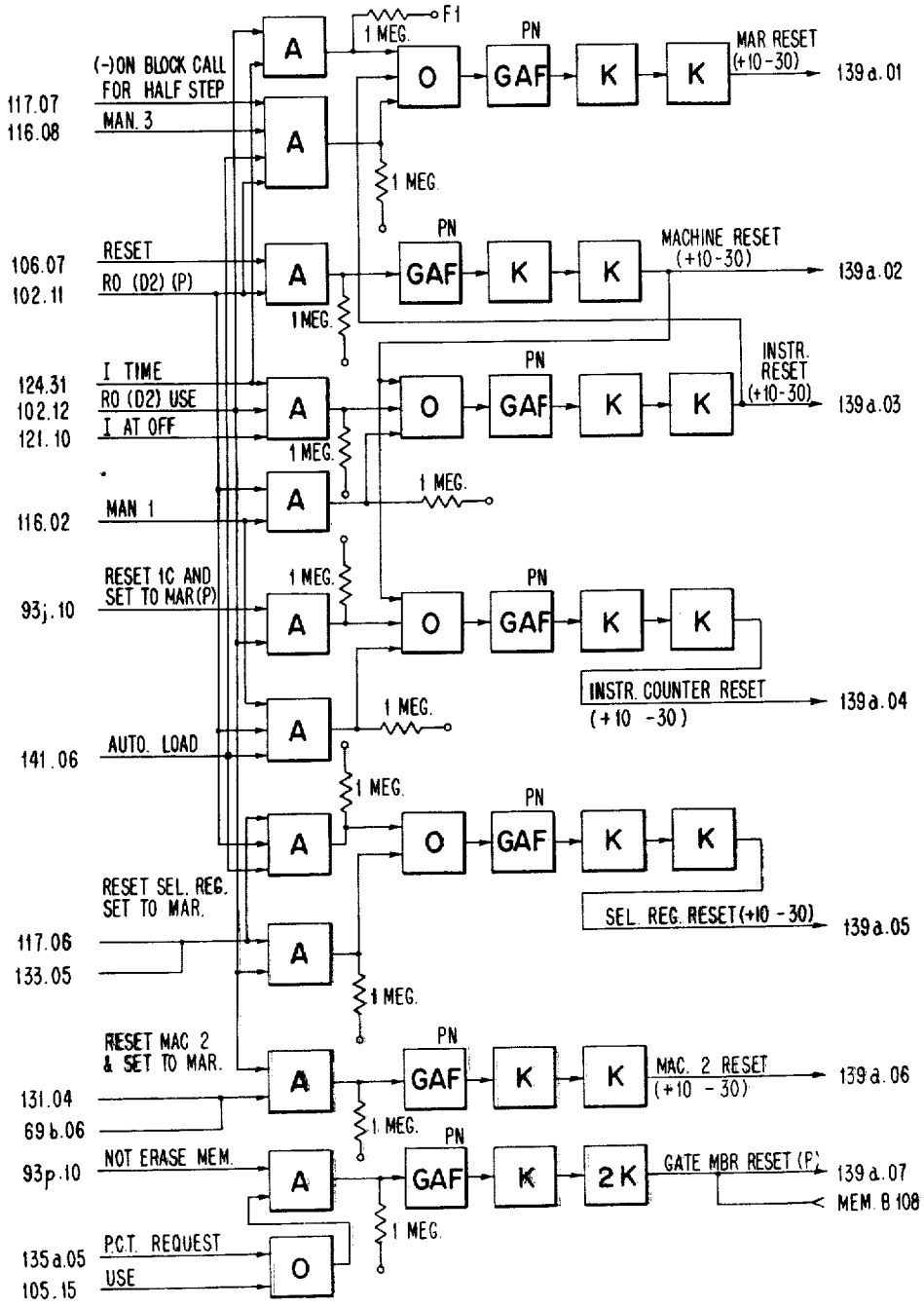


FIG. 139a
RESETS



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FIG. 139b

INSTRUCTION RESET MACHINE RESET

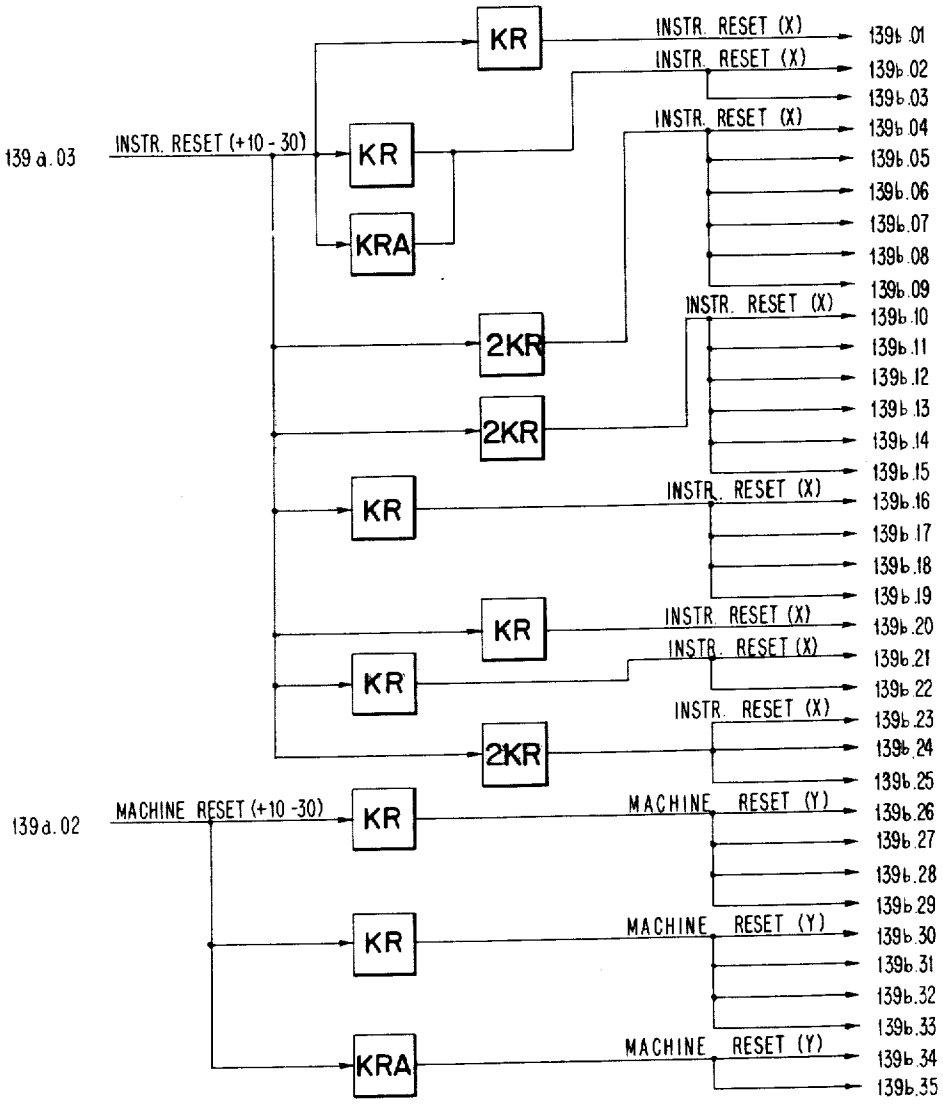


FIG. 139c

RESULT REG, MAC 2, IC, INITIAL SELECT REG. & MAR. RESETS

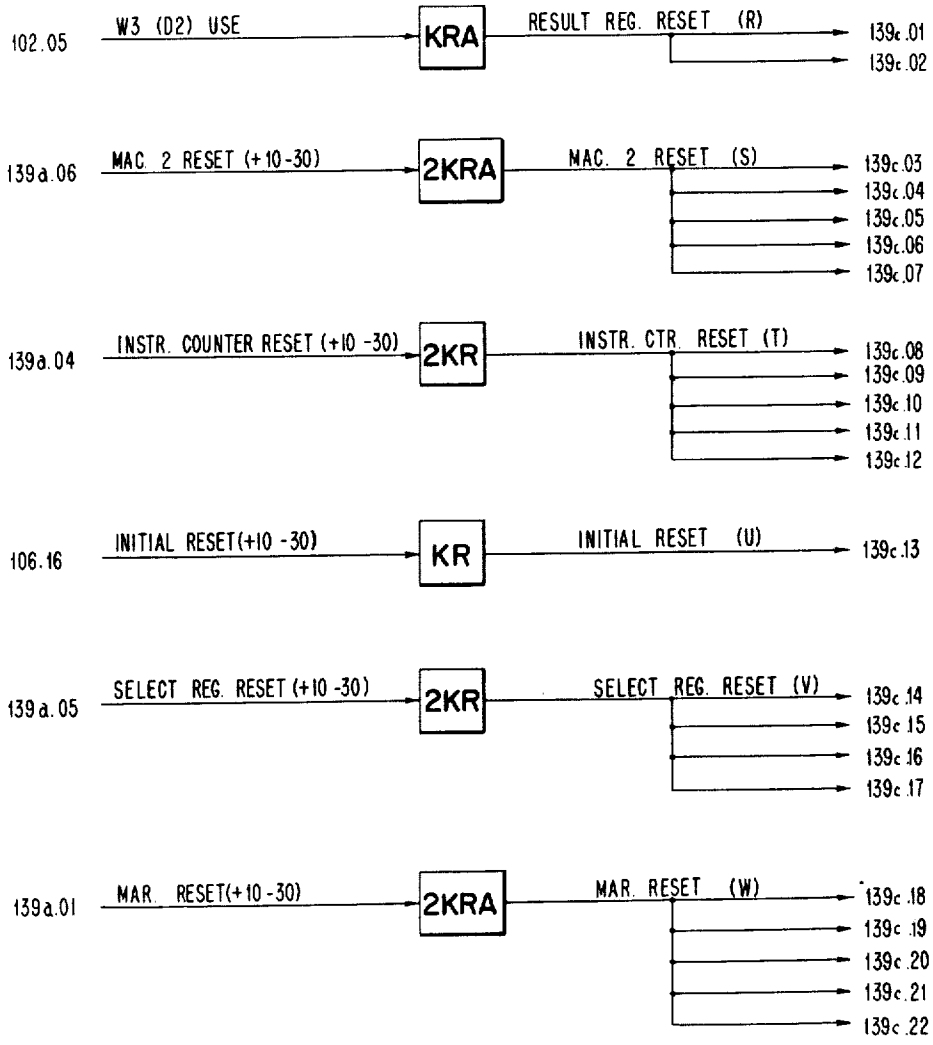
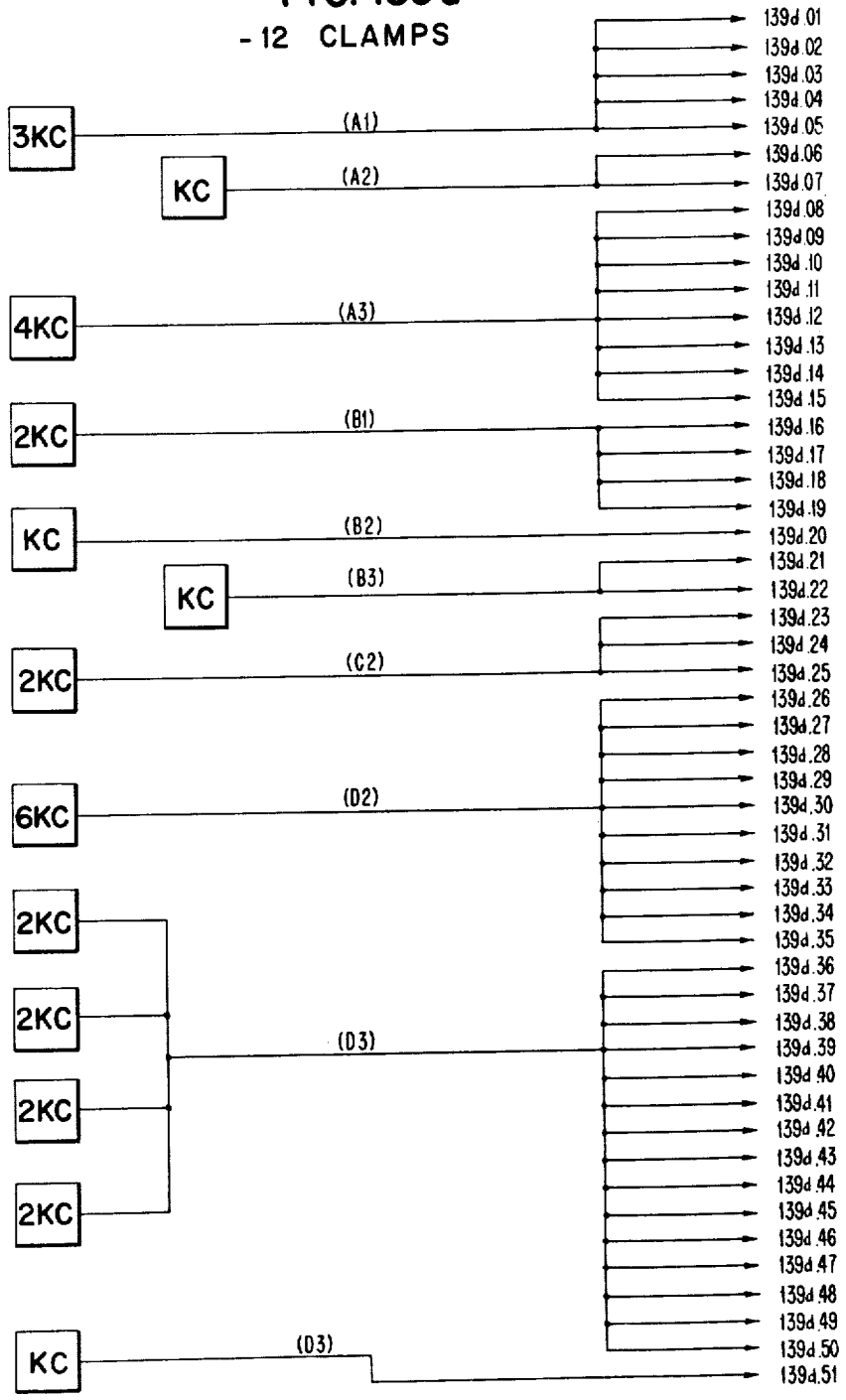


FIG. 139d
- 12 CLAMPS



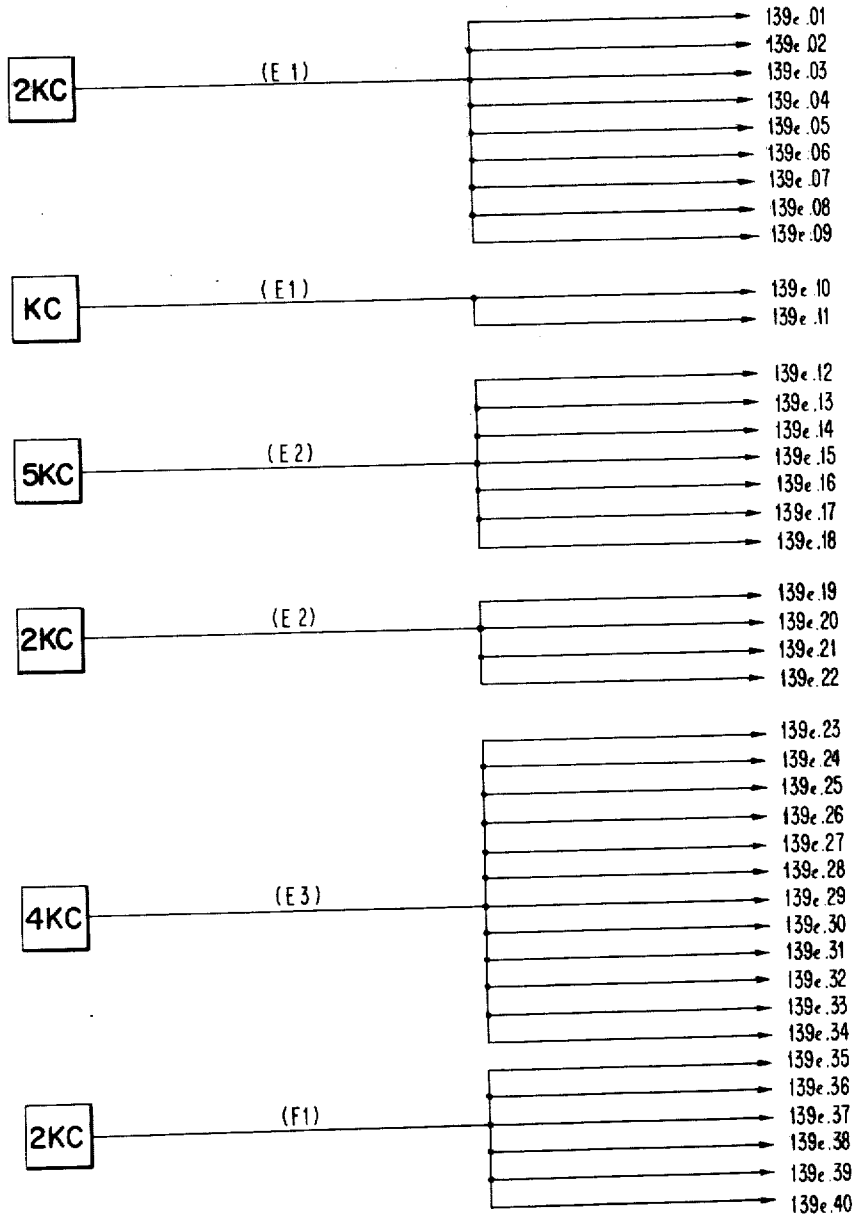
Oct. 16, 1962 W. R. DEMMER 3,059,222

TRANSFER INSTRUCTION

Filed Dec. 31, 1958 382 Sheets-Sheet 373

FIG. 139e

-12 CLAMPS



COMPARE ROUTING CONTROLS

FIG. 140a

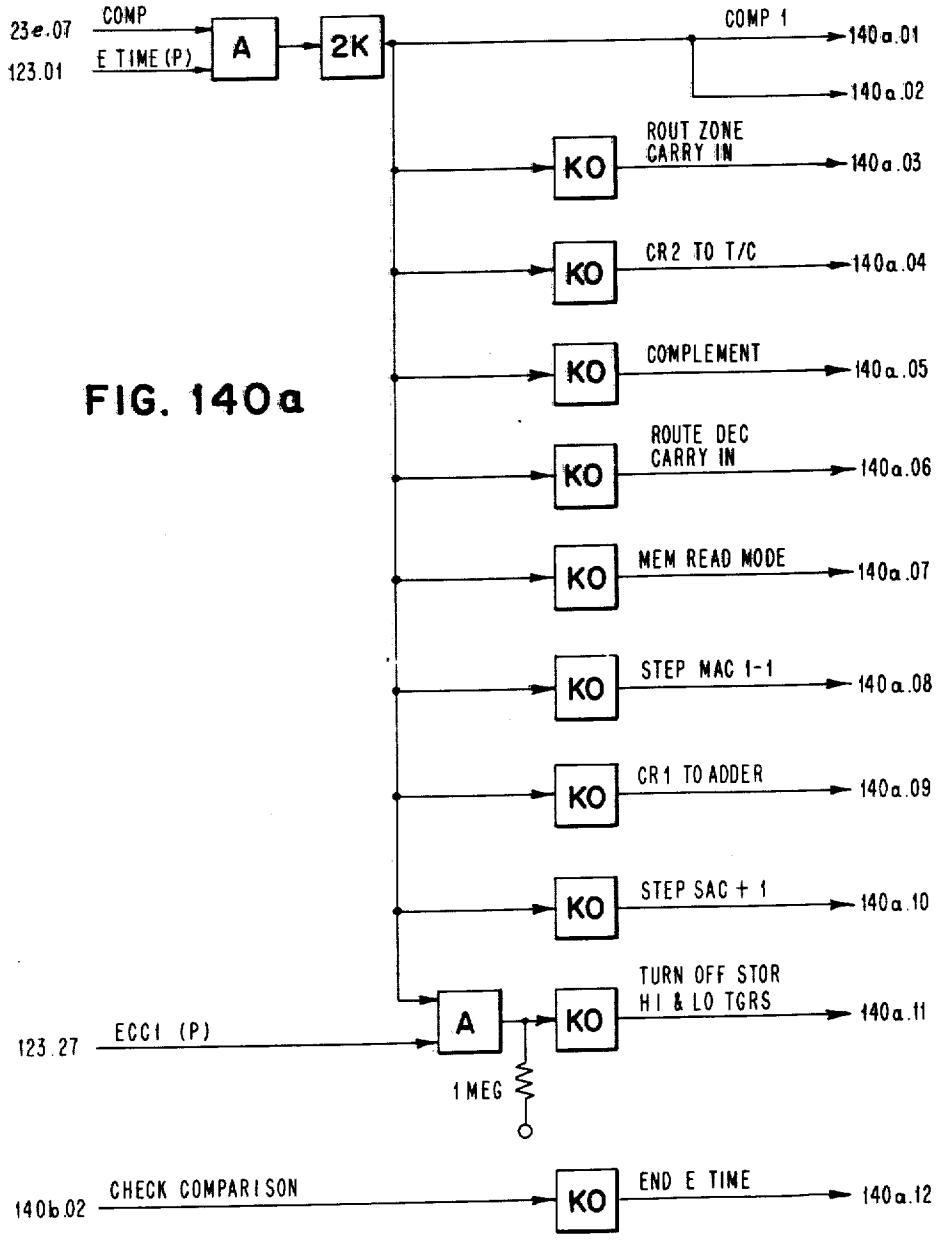


FIG. 140b COMPARE ROUTING CONTROLS

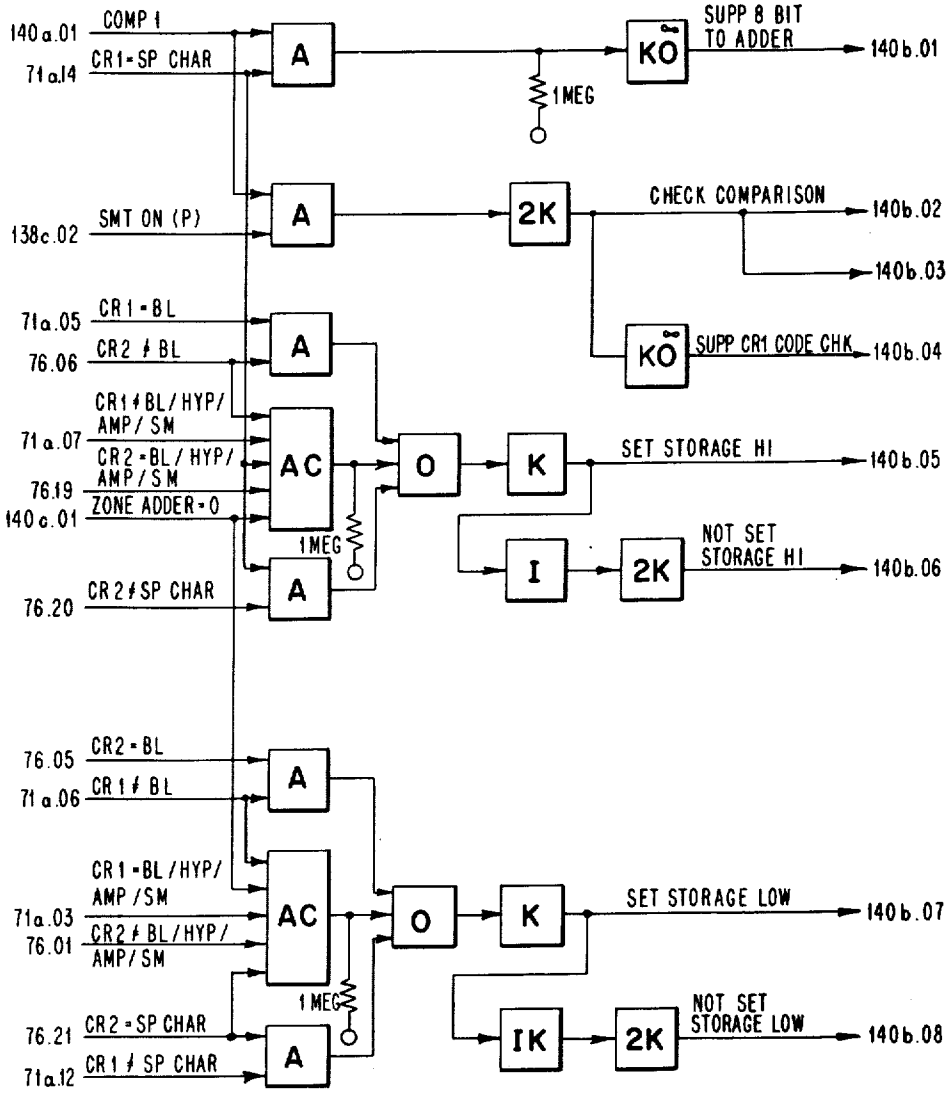


FIG. 140c COMPARE ROUTING CONTROLS

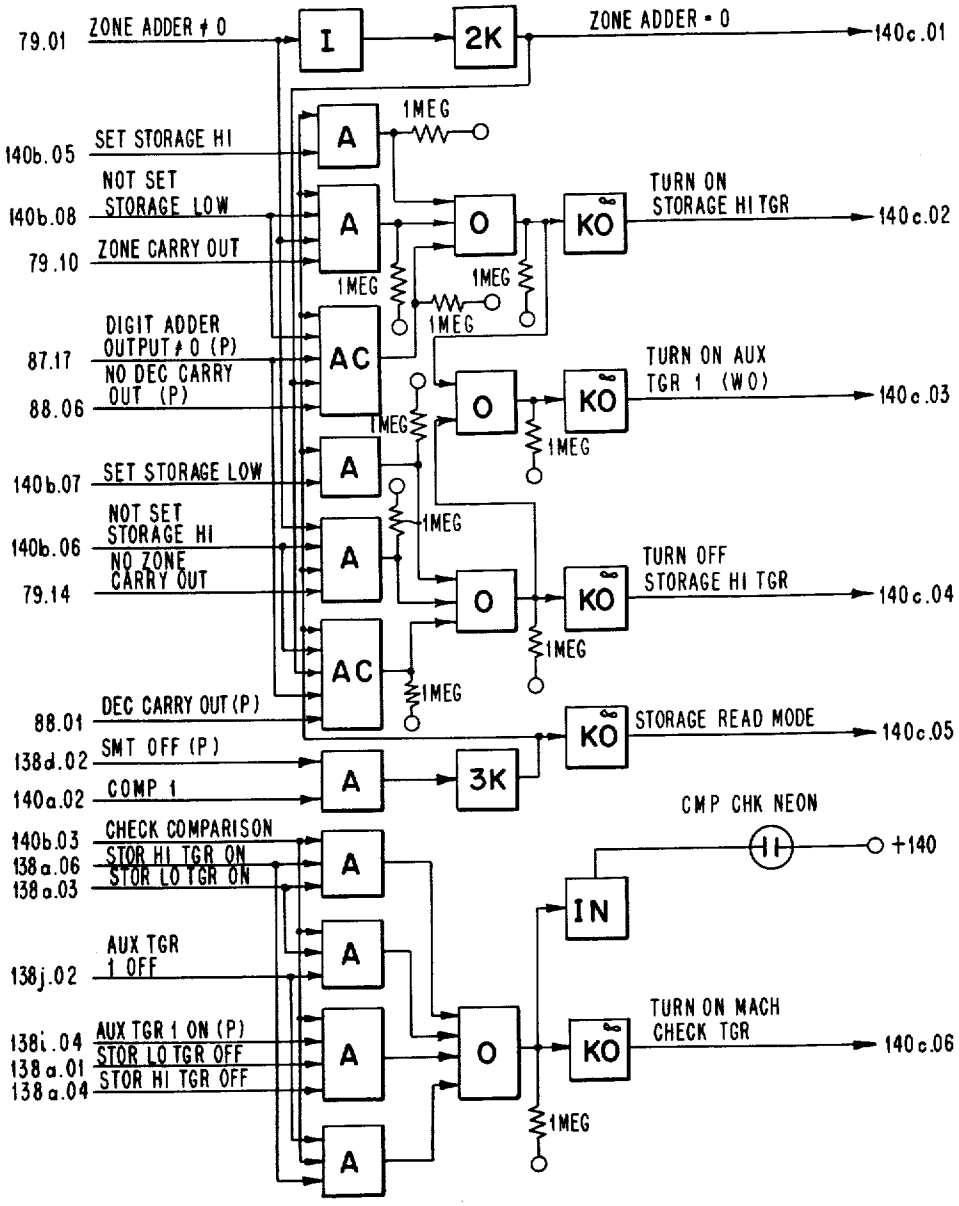


FIG. 141

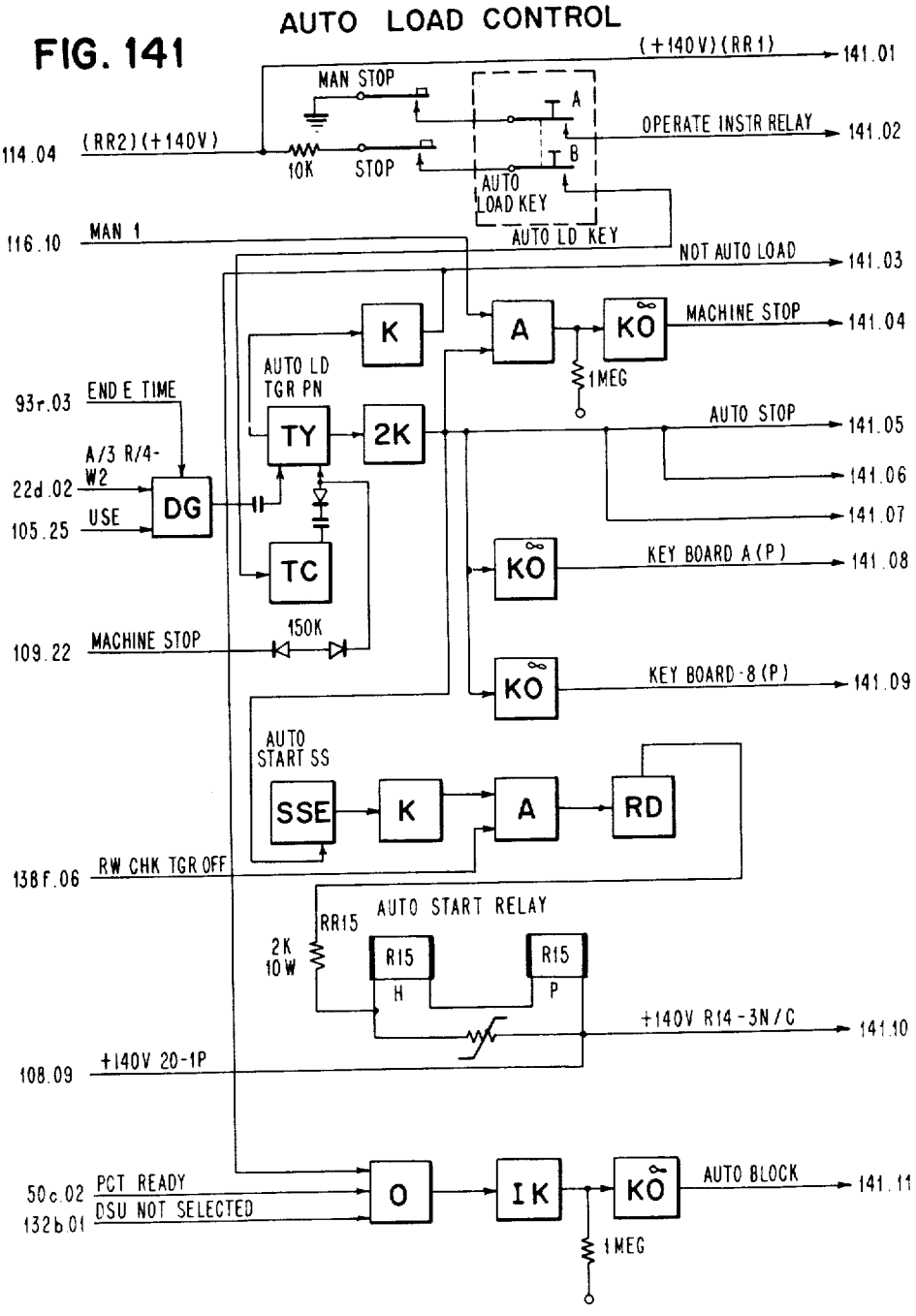
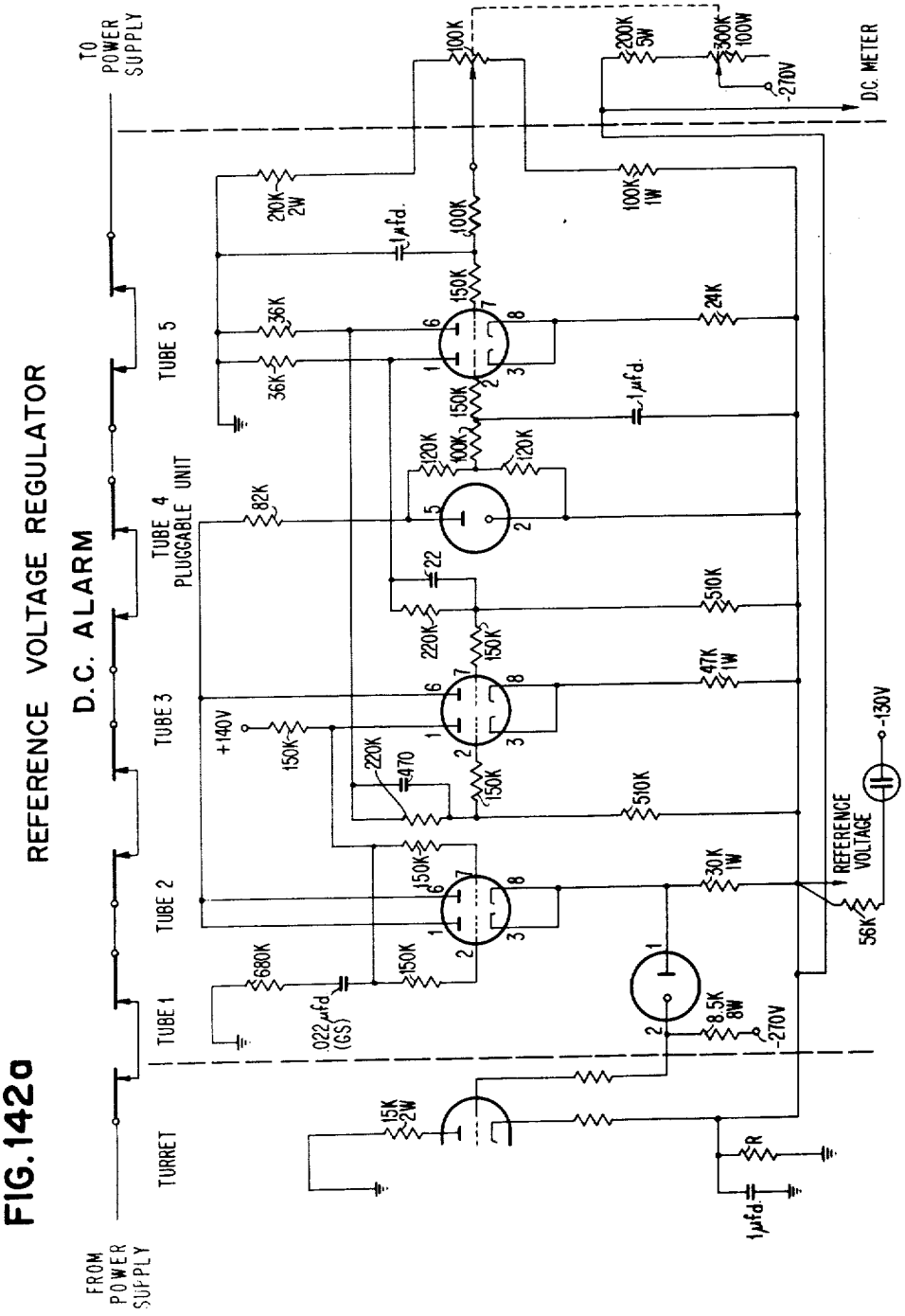

AUTO LOAD CONTROL
(+140V)(RR1)
141.01
MAN STOP
A
OPERATE INSTR RELAY
141.02
114.04
(RR2)(+140V)
10K
STOP
B
AUTO LOAD KEY
116.10
MAN 1
AUTO LD KEY
NOT AUTO LOAD
141.03
K
A
KO
MACHINE STOP
141.04
AUTO LD TGR PN
1MEG
93r.03
END E TIME
TY
2K
AUTO STOP
141.05
141.06
141.07
A/3 R/4-W2
22d.02
DG
USE
105.25
TC
KO
KEY BOARD A(P)
141.08
150K
109.22
MACHINE STOP
KO
KEY BOARD-8(P)
141.09
AUTO START SS
SSE
K
A
RD
138f.06
RW CHK TGR OFF
AUTO START RELAY
RR15
2K 10W
R15
H
R15
P
+140V R14-3N/C
141.10
108.09
+140V 20-1P
50c.02
PCT READY
132b.01
DSU NOT SELECTED
O
IK
KO
AUTO BLOCK
141.11
1MEG

FIG. 142a


REFERENCE VOLTAGE REGULATOR
D.C. ALARM
TO POWER SUPPLY
FROM POWER SUPPLY
TURRET
TUBE 1
TUBE 2
TUBE 3
TUBE 4 PLUGGABLE UNIT
TUBE 5
DC METER
REFERENCE VOLTAGE
+140V
-130V
-270V
100K
200K 5W
300K 100W
100K 1W
210K 2W
1 μfd.
150K
36K
24K
120K
82K
22
510K
220K
47K 1W
470
30K 1W
56K
680K
.022 μfd (GS)
8.5K 8W
15K 2W
R

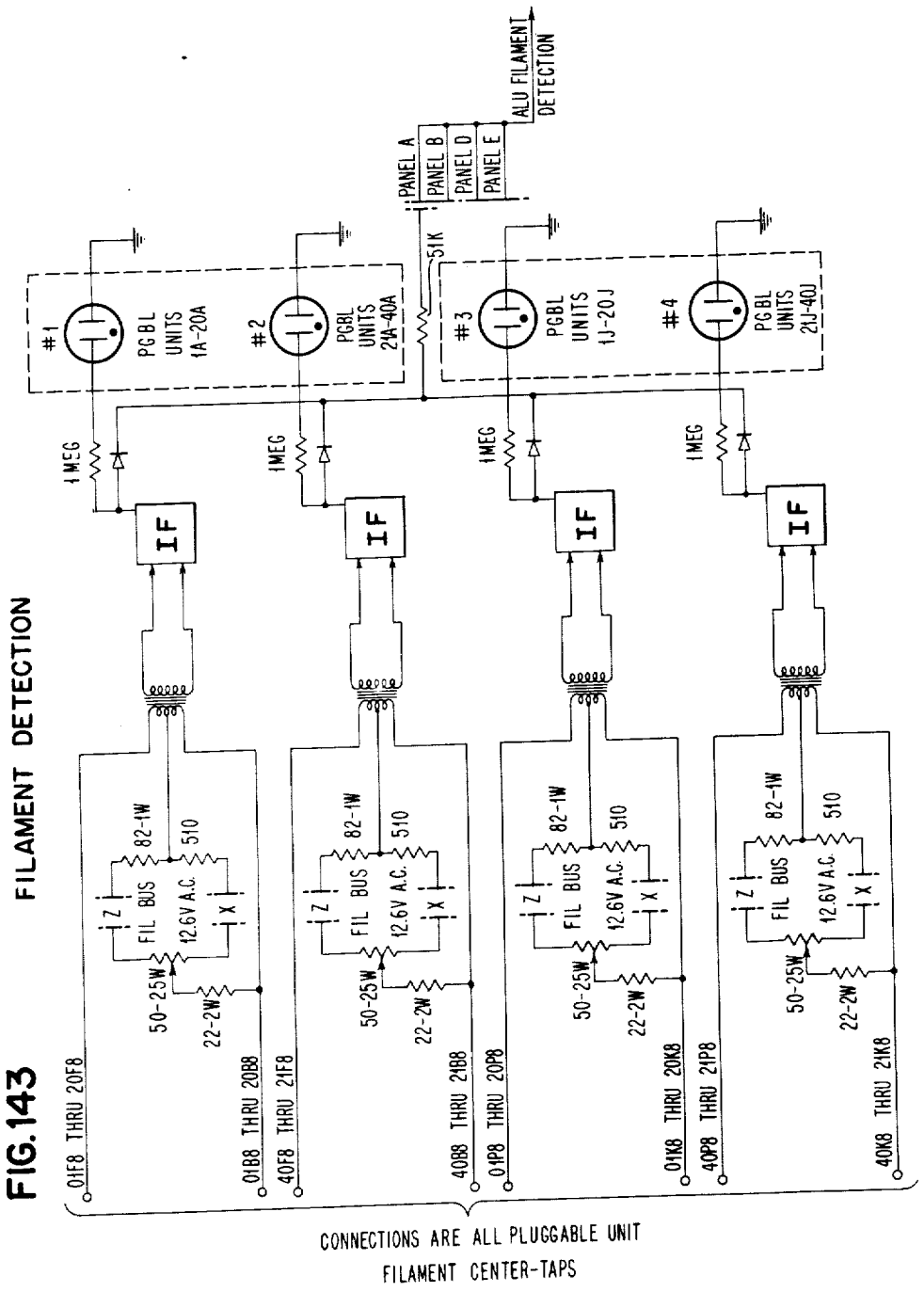


FIG. 143 FILAMENT DETECTION

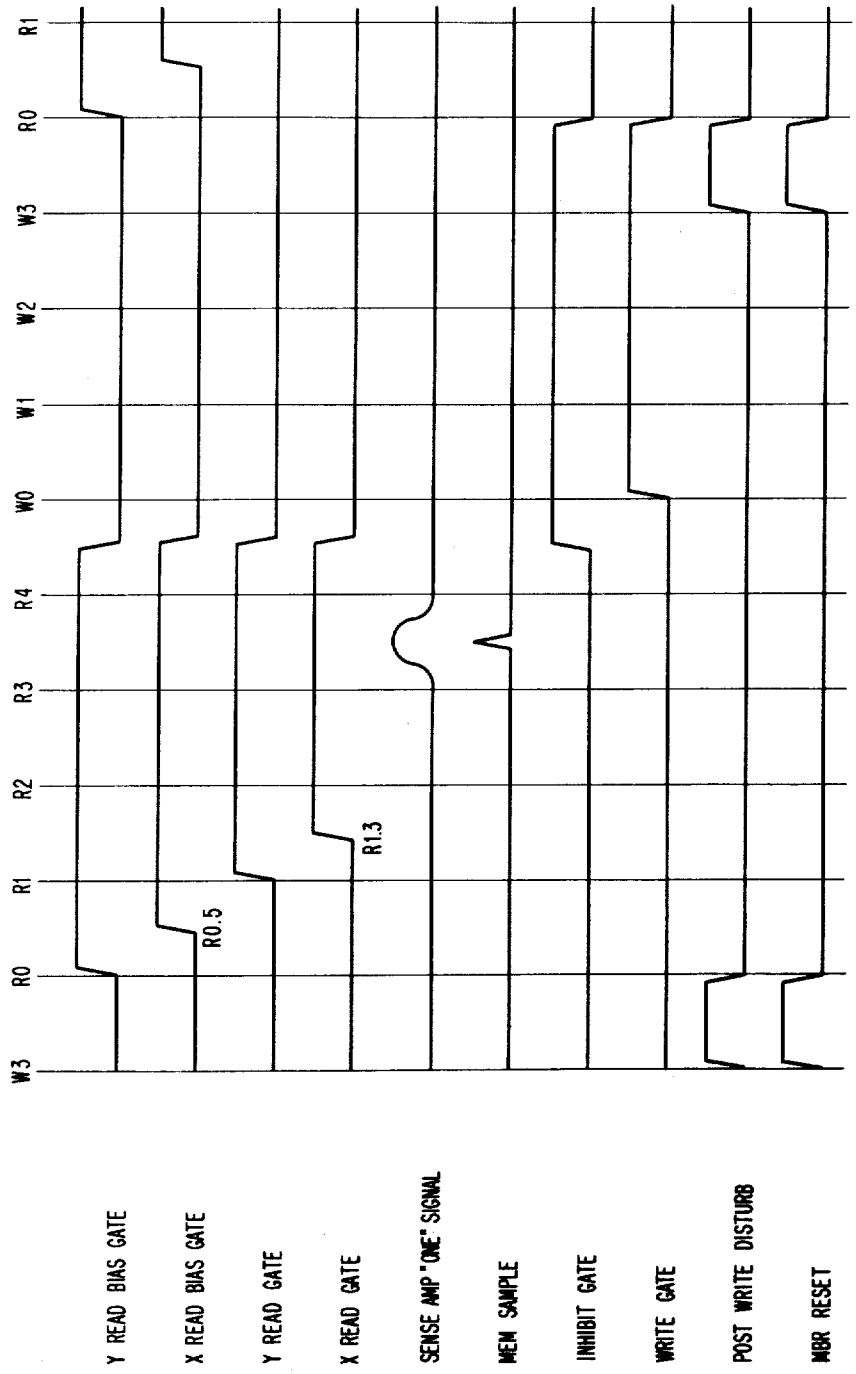


FIG. 144

MEMORY TIMING CHART

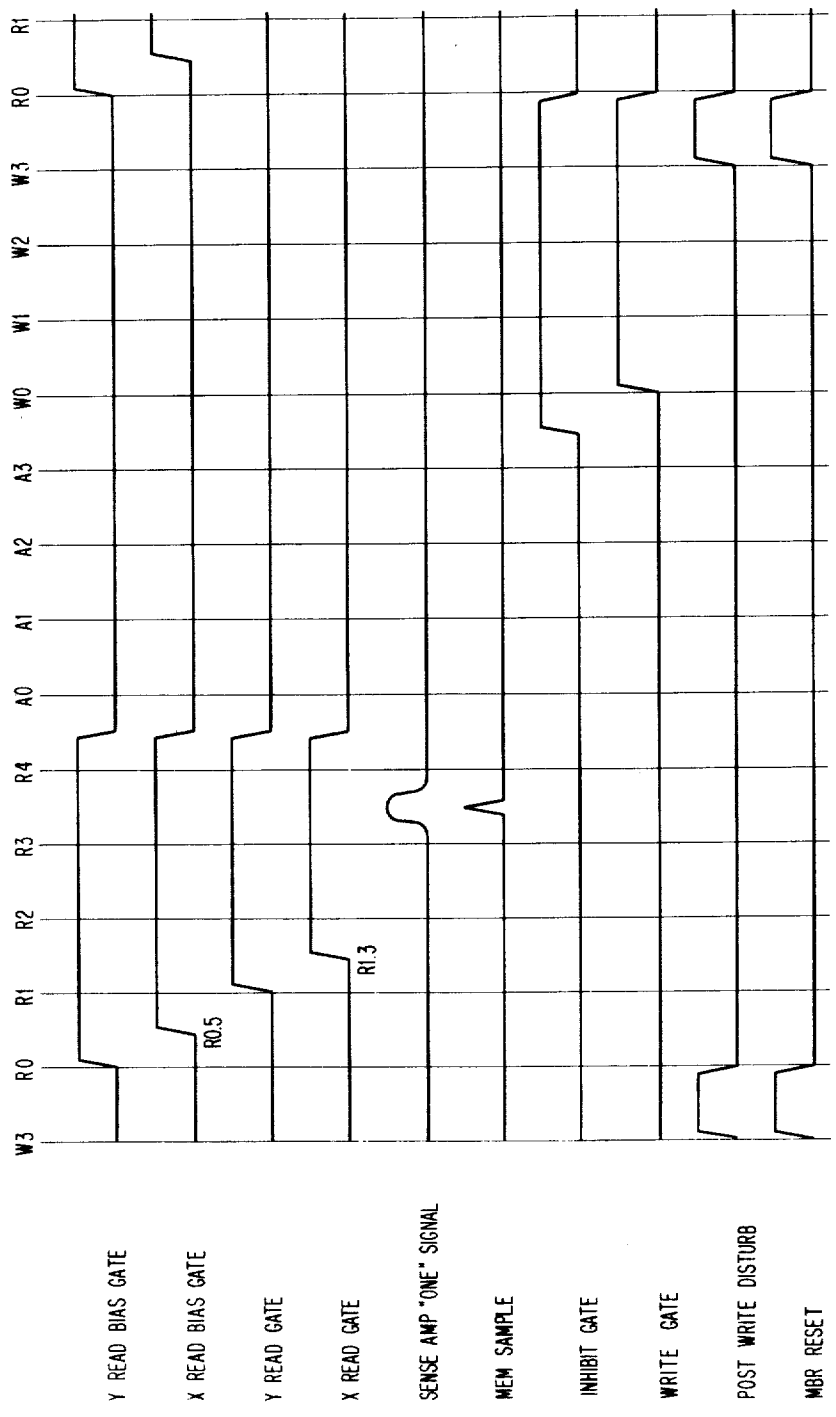
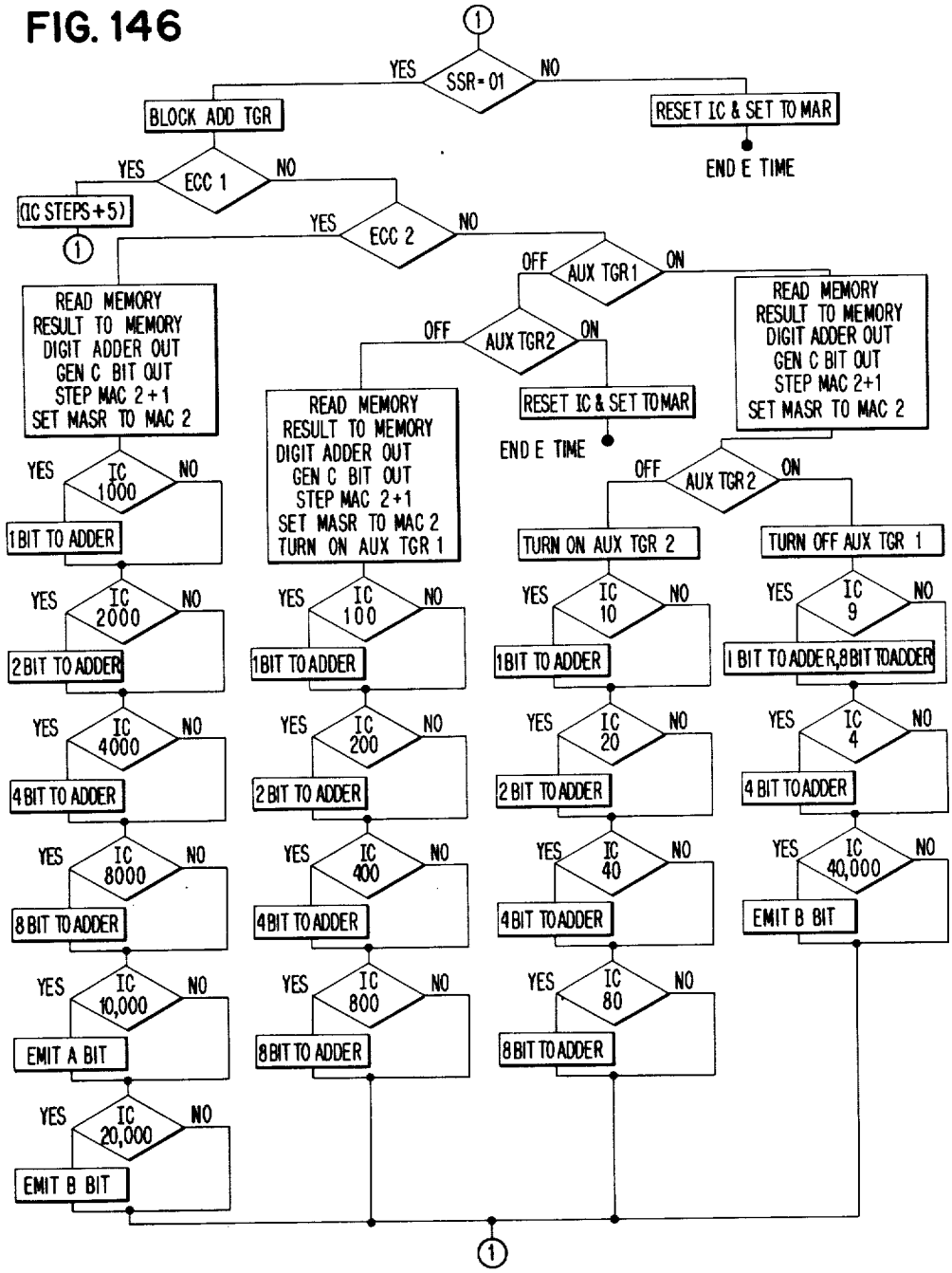


FIG. 145 MEMORY TIMING CHART

FIG. 146



TRANSFER FLOW DIAGRAM

United States Patent Office 3,059,222 Patented Oct. 16, 1962

3,059,222

TRANSFER INSTRUCTION

William R. Demmer, Wappingers Falls, N.Y., assignor to International Business Machines Corporation, New York, N.Y., a corporation of New York

Filed Dec. 31, 1958, Ser. No. 784,104
3 Claims. (Cl. 340—172.5)

This invention relates to electronic apparatus and more particularly to apparatus which is especially useful in the operation of electronic data processing systems when it is desired to leave the usual sequence of programmed operations for another and then return to the usual sequence of operations at the point of departure.

The apparatus of the invention, as described herein, employs an array of magnetic cores as principal storage designated Core Memory. It also employs an array of magnetic cores as temporary storage designated Core Storage, the latter being divided into two sections, one section comprising Accumulator Storage and another comprising Auxiliary Storage.

Characters, each of seven bits (C, B, A, 8, 4, 2, 1) with the numeric bits being coded in the binary coded decimal notation and each character in an addressable location, are combined to form words or fields whose address in Core Memory or Storage is usually designated by addressing the least significant character of the particular word or field. In Storage, the end of a field is identified by storing a Storage Mark (SM) character adjacent the most significant character in the field. In Core Memory, the sign of the field is indicated by special zoning in the A and B positions of the least significant digit. This special coding of a character in one field also serves to demarcate the length of an adjacent field or word stored at a preceding address.

The electronic data processing system provided herein is controlled by a program of instructions stored in Core Memory which prescribe the operations to be performed and the locations of data in Core Memory, which data is to be manipulated in accordance with these instructions. Instructions comprise five characters and are extracted from Core Memory and decoded to control circuits which carry out the execution of the instruction originally obtained from Core Memory before selecting another instruction. Programs may be entered into Core Memory in a number of ways. For example, the instruction may be punched in cards in the "IBM" code and read into Memory by means of a card reader or they may be recorded on tape and entered in Memory therefrom.

The Computer per se comprises Storage, arithmetic circuits and various registers which, under control of the instruction, are employed to process data which may be words, fields or portions of instructions whereby characters are added, subtracted, multiplied, revised and so forth and act on portions of instructions as if they were data. The characters may be numeric, non-numeric or mixed. Since the binary coded decimal (BCD) notation is employed for numerical information, the result of arithmetic operations on two characters may require correction which is automatic when such correction is required. It is to be noted that many of the basic elements of the Data Processing System assume one or the other of two stable states as described later and are therefore particularly well suited for the binary system of notation where one specified state is indicative of a binary "one" and the other state is indicative of a binary "zero."

An Instruction cycle, which is the time required to obtain a word from Core Memory and prepare for the operation specified by the instruction, has a duration of

thirteen microseconds. For the Instruction cycle, the Read and Write portions of the basic cycle are used and an additional four microseconds is inserted to provide a total duration of thirteen microseconds.

The stored program mentioned above contains as many Instructions as necessary to perform the intended data processing operation. The five characters of the Instruction consist of four characters designating the Address, called the Address portion, and one character designating the Operation, called the Operations portion. In the stored program computers of the present invention, the computer has no way of distinguishing between Instructions and Data except by the time of occurrence, either during Instruction (I) or Execute (E) time when it reads the information. If the computer is in Instruction time, then the information received from Core Memory is an Instruction; if it is Execute time, then the information is data to be operated upon. Upon completion of readout of an Instruction, the apparatus proceeds to Execute time which consists of a number of Execution cycles, the number depending upon the length of the particular field being processed and the particular Instruction being executed.

Recent advances in Data Processing Systems have led to integrated systems wherein Input/Output operations are carried on, for the most part, simultaneously with arithmetic operations and a general storage device such as Core Memory is shared among Input/Output units and the Central Processing Unit. Either the CPU or one of the I/O devices make reference to general storage when possible while the other is performing a function not requiring reference to general storage. Input/Output units are controlled by Data Synchronizers such as those described and claimed in application Serial No. 705,447, Data Synchronizer, Christiansen et al., filed December 26, 1957. Such Data Synchronizers are provided with initial instructions and operate thereafter on their own stored programs, usually until additional instructions are required. Although this invention is not limited to use with Data Synchronizers it is especially useful when operating therewith by providing a DSU with further instructions as soon as possible after they are required. The Transfer 01 Instruction may be inserted frequently in the program to effect a transfer to a sub-routine where DSU instructions may be furnished. Further the Transfer instruction affords a simple means for returning to the usual sequence of operations, i.e., the main or principal program, upon completion of the sub-routine. Of course, the Transfer 01 Instruction provides a convenient way to enter any desired sub-routine and return to the main program.

Briefly, the Transfer 01 Instruction may be inserted in the program following a Receive Instruction and preceding a Normal Transfer instruction. As described in "IBM" Electronic Data Machines, Type 705, Preliminary Manual of Operation, Form No. 22-6627-4, the Receive instruction contains an address which is placed in MAC 2, which advances five addresses after each five transmitted.

The Transfer 01 instruction causes the contents of the Instruction Counter to be stored as an address at the Memory Address specified by MAC 2. However, the Instruction Counter is permitted to step to the next address from the address of the Transfer 01 instruction. The Instruction Counter is then reset and subsequently set to the address contained in the Transfer 01 instruction which is the address of the sub-routine. The last instruction of the sub-routine is a normal Transfer 00 located at the address formerly specified by MAC 2, and this instruction now contains the former contents of the In-

struction Counter which refers to the next step in the main program. The format may be as follows:

Location of Instruction	Operation Code	Memory Address contained in Instruction	Function
1999	Receive	1001	Set MAC 2 to 2959.
2004	Transfer 01	2934	IC is at 2004, step IC+5, stored 2009 at address 2959 and refer to Memory address 2934 (specified by Transfer 01).
2934	Subroutine		
↓			
2959	Transfer 00	2009	Transfer to Memory 2009 and proceed.

It is pointed out that in the example above, the operation code for Transfer 00 was previously placed in character 0 of 2955–2959 and remained unmodified although a Memory address was supplied from MAC 2 and stored in characters 1 through 4. Actually, the Operation code may be any one desired by the programmer and the Transfer 00 is merely used for purposes of illustration.

It is an object of this invention to provide means responsive to a Transfer instruction for storing the address of the instruction which would be performed next at a predetermined address, for referring to the instructions determined from the address of the Transfer instruction, for subsequently referring to the predetermined address, and for then referring to the address of the instruction which would normally have been performed in the absence of the Transfer instruction.

Another object is to provide apparatus responsive to a first Instruction for supplying a desired address to an operation code located at a predetermined address and referring to a second instruction at an address specified by the first instruction.

A further object of this invention is to furnish apparatus for inserting a secondary program within a primary program in response to an instruction which refers to the secondary program, records the starting point for resuming the primary program at a predetermined location, and upon referring to the predetermined location resumes the primary program.

Other objects of the invention will be pointed out in the following description and claims and illustrated in the accompanying drawings, which disclose, by way of example, the principle of the invention and the best mode, which has been contemplated, of applying that principle.

In the drawings:

FIG. 1 is an overall block diagram illustrating generally the major components comprising the data processing system and their interconnections.

FIGS. 2*a* through 2*hhh* form the logical block diagrams of the principal data portions of the data processing system.

FIG. 2*iii* illustrates how FIGS. 2*a* through 2*hhh* inclusive, may be placed to form a composite block diagram of the major data portions of the data processing system.

FIG. 3*a* illustrates the Mem. 4×10 Decoder 1000 Order.

FIG. 3*b* illustrates the Mem. 4×10 Decoder.

FIG. 3*c* illustrates the Mem. 4×10 Decoder 100 Order.

FIG. 3*d* illustrates the Mem. 6×8 Decoder.

FIG. 3*e* illustrates the Mem. 4×5 Decoder.

FIG. 4 illustrates the Mem. "Y" Switch Core Read Drivers.

FIG. 5*a* illustrates the 4×10 Decoder Output Inverters.

FIG. 5*b* illustrates the Mem. "Y" Switch Core Write Drivers.

FIG. 5*c* illustrates the Mem. "Y" Switch Core Write Drivers.

FIG. 5*d* illustrates the Memory Write Gate & Memory Inhibit Gate.

FIG. 5*f* illustrates the Memory Read Bias Gate & Mem./P.C.T. Sample Control.

FIG. 5*e* illustrates the Memory Read Gates & P.W.D. Control.

FIG. 5*g* illustrates the Memory Gate Powering & M.B.R. Reset.

FIG. 5*h* illustrates the Memory Clamps & Sense Amp. Bias Voltage.

FIG. 5*i* illustrates the Storage Sample Pulse Generator.

FIG. 6 illustrates the Mem. X Switch Core Read Drivers.

FIG. 7*a* illustrates the 6×8 Decoder Output Inverters.

FIG. 7*b* illustrates the Mem. X Switch Core Write Drivers.

FIG. 7*c* illustrates the Mem. X Switch Core Write Drivers.

FIG. 7*d* illustrates the Stor. Read Bias GT., Read GT., Inhibit GT., Write GT. & Buff Reg. Reset.

FIG. 7*e* illustrates the Storage R/W Mode Ctrl.

FIG. 8 illustrates the Y Switch Core Matrix.

FIG. 9 illustrates the "X" Switch Core Matrix.

FIG. 10 illustrates the Mem. Input Select.

FIG. 11*a* illustrates the Mem. Input Switch Char. 4, 3, 2.

FIG. 11*b* illustrates the Mem. Input Switch Char. 0 & 1.

FIG. 12*a* illustrates the Mem. Inhibit Driver Circuits Char. 4, 3 & 2.

FIG. 12*b* illustrates the Mem. Inhibit Driver Circuits Char. 0 & 1.

FIG. 13 illustrates the Memory Core Plane To Terminating Resistors.

FIG. 14*a* illustrates the Memory Buffer Register Char. 4, 3 & 2.

FIG. 14*b* illustrates the Memory Buffer Register Char. 0 & 1.

FIG. 15*a* illustrates the Upper Sense Amplifier Circuits (Typical of all Char. 4, 3 & 2 Sense Amp.).

FIG. 15*b* illustrates the Lower Sense Amplifier Circuits (Typical of all Char. 0 & 1 Sense Amp.).

FIG. 16*a* illustrates the Storage Select Register.

FIG. 16*b* illustrates the Storage Selector.

FIG. 17*a* illustrates the 1st Order of MAR.

FIG. 17*b* illustrates the 2nd Order of MAR.

FIG. 17*c* illustrates the 3rd Order of MAR.

FIG. 17*d* illustrates the 4th Order of MAR.

FIG. 17*e* illustrates the 5th Order of MAR.

FIG. 17*f* illustrates the Memory Address Register Controls.

FIG. 18*a* illustrates the P.C.T. Write Busses Char. 4, 3 & 2.

FIG. 18*b* illustrates the P.C.T. Write Busses Char. 1 & 0.

FIG. 19*a* illustrates the Memory Buff Reg. Code Check Char. 4, 3, 2.

FIG. 19*b* illustrates the Memory Buff Reg. Code Check Char. 1, 0.

FIG. 19*c* illustrates the Memory Buff. Reg. Code Check Output.

FIG. 20*a* illustrates the Memory Output Select.

FIG. 20*b* illustrates the Output Switch Char. 1 & 0.

FIG. 20*c* illustrates the Output Switch Char. 4 & 3.

FIG. 20*d* illustrates the Output Switch Char. 2 & Memory Out Bus.

FIG. 20*e* illustrates the Memory Sample Pulse Generator & P.C.T. Sample Pulse Gen. & M.B.R. Sample Pulse Generator.

FIG. 21*a* illustrates the Operation Register 1, 2, 4, 8 Tgrs.

FIG. 21*b* illustrates the Operation Register A, B, C Triggers.

FIG. 22*a* illustrates the Manual Keyboard.

FIG. 22*b* illustrates the Keyboard Outputs.

FIG. 22*c* illustrates the Keyboard Restore Controls.

FIG. 22*d* illustrates the Key Depressed Trigger.

FIG. 23*a* illustrates the Operation Zone Decoder.

FIG. 23*b* illustrates the Operation Decoder No Op, Stop, Tr, Send.

FIG. 23*c* illustrates the Operation Decoder Set L, Tr, Hi, RWW, Sel.

FIG. 23*d* illustrates the Operation Decoder Shor, Tr, Eq, Sign Ctrl.

FIG. 23*e* illustrates the Operation Decoder Leng, Tr, PLS, RCV, Comp.

FIG. 23*f* illustrates the Operation Decoder—Round, Tr, ZRO, MPX, ST, PR.

FIG. 23*g* illustrates the Operation Decoder Store, Tr, Sig, Div, Add Mem.

FIG. 23*h* illustrates the Operation Decoder, Add, Sub, Norm Tr, Load.

FIG. 23*i* illustrates the Operation Decoder—R, Add, R Sub, Read, Load.

FIG. 23*j* illustrates the Opertion Decoder—Tr Any, Wr Er, Tsmt.

FIG. 23*k* illustrates the Operation Decoder LDA, BLM, TZB.

FIG. 23*l* illustrates the Operation Decoder ULA, AAM, SB.

FIG. 24 illustrates the Operation Check Circuits.

FIG. 25*a* illustrates the Memory Address Selector Keys.

FIG. 25*b* illustrates the Memory Address Selector Key Outputs.

FIG. 26*a* illustrates the Parallel Character Transmission Cable A Connector Layout.

FIG. 26*b* illustrates I/O Signal Cable Connector Layout SP Connector Receptable—Wiring Side.

FIG. 27 illustrates the Control Address Decoder.

FIG. 28 illustrates the SMAC Checking.

FIG. 29*a* illustrates the MASR/MAR To DSU Powering.

FIG. 29*b* illustrates the MASR/MAR To DSU Powering.

FIG. 30*a* illustrates the 1st Order of MAC 1.

FIG. 30*b* illustrates the 2nd Order of MAC 1.

FIG. 30*c* illustrates the 3rd Order of MAC 1.

FIG. 30*d* illustrates the 4th Order of MAC 1.

FIG. 30*e* illustrates the 5th Order of MAC 1.

FIG. 30*f* illustrates MAC 1 Controls.

FIG. 30*g* illustrates the MAC 1=0/5, 4/9, 1/6, MAC 1=End of Memory.

FIG. 31*a* illustrates the 1st Order of MAC 2.

FIG. 31*b* illustrates the 2nd Order of MAC 2.

FIG. 31*c* illustrates the 3rd Order of MAC 2.

FIG. 31*d* illustrates the 4th Order of MAC 2.

FIG. 31*e* illustrates the 5th Order of MAC 2.

FIG. 31*f* illustrates the MAC 2 Controls.

FIG. 32*a* illustrates the Instruction Counter Controls & 4, 9 of IC.

FIG. 32*b* illustrates the 2nd Order of IC.

FIG. 32*c* illustrates the 3rd Order of IC.

FIG. 32*d* illustrates the 4th Order of IC.

FIG. 32*e* illustrates the 5th Order of IC.

FIG. 33*a* illustrates the 1st Order of Sel Reg.

FIG. 33*b* illustrates the 2nd Order of Sel Reg.

FIG. 33*c* illustrates the 3rd Order of Sel Reg.

FIG. 33*d* illustrates the 4th Order of Sel Reg.

FIG. 33*e* illustrates the Select Register Controls.

FIG. 33*f* illustrates the ALU Sel Reg Decoder.

FIG. 33*g* illustrates the ALU Sel. Reg. Decoder.

FIG. 34*a* illustrates the Storage 2×4 Decoder 128, 256.

FIG. 34*b* illustrates the Storage 2×4 Decoder 32, 64.

FIG. 34*c* illustrates the Storage 2×4 Decoder 8, 16.

FIG. 34*d* illustrates the Storage 3×8 Decoder.

FIG. 35 illustrates X Switch Core Read Drivers.

FIG. 36*a* illustrates the 2×4 Decoder Output Inverters.

FIG. 36*b* illustrates the Y Switch Core Write Drivers.

FIG. 37 illustrates the Y Switch Core Read Drivers.

FIG. 38*a* illustrates the 3×8 Decoder Output Inverters.

FIG. 38*b* illustrates the Stor. X Switch Core Write Drivers.

FIG. 38*c* illustrates the Storage X Switch Core Write Drivers.

FIG. 39 illustrates the "Y" Switch Core Matrix.

FIG. 40 illustrates the "X" Switch Core Matrix 4×8 Diagram.

FIG. 41 illustrates the Storage Write Driver Select Circuit.

FIG. 42 illustrates the Odd-Even Gating Circuit.

FIG. 43 illustrates the Storage Input Select & Switch Ckts.

FIG. 44 illustrates the Storage Inhibit Drivers.

FIG. 45 illustrates the Storage Array.

FIG. 46 illustrates the Sense Amplifier (Storage).

FIG. 47 illustrates the Buffer Register (Storage).

FIG. 48 illustrates the CR 2.

FIG. 49*a* illustrates the 1st Order of MASR.

FIG. 49*b* illustrates the 1st Order of MASR Set Circuits.

FIG. 49*c* illustrates the 2nd Order of MASR.

FIG. 49*d* illustrates the 2nd Order of MASR Circuits.

FIG. 49*e* illustrates the 3rd Order of MASR.

FIG. 49*f* illustrates the 3rd Order of MASR Set Circuits.

FIG. 49*g* illustrates the 4th Order of MASR.

FIG. 49*h* illustrates the 4th Order of MASR Set Circuits.

FIG. 49*i* illustrates the 5th Order of MASR.

FIG. 49*j* illustrates the 5th Order MASR Set Circuits.

FIG. 50*a* illustrates the Transfer Routing Controls.

FIG. 50*b* illustrates the Transfer Routing Controls.

FIG. 50*c* illustrates the Transfer Routing Controls.

FIG. 50*d* illustrates the Transfer Routing Controls.

FIG. 50*e* illustrates the Transfer 01.

FIG. 50*f* illustrates the Transfer 01.

FIG. 50*g* illustrates the Transfer 01.

FIG. 51*a* illustrates the Stages 1–3 of SPC.

FIG. 51*b* illustrates the Stages 4–6 of SPC.

FIG. 51*c* illustrates the Stages 7–8 of SPC.

FIG. 52*a* illustrates the Stages 1–4 of SAC.

FIG. 52*b* illustrates the Stages 1–4 of SAC.

FIG. 52*c* illustrates the Stages 5–8 of SAC.

FIG. 52*d* illustrates the Stages 5–8 of SAC.

FIG. 52*e* illustrates the SAC Controls.

FIG. 53*a* illustrates the Storage Address Select Register Stages 1–4.

FIG. 53*b* illustrates the Storage Address Select Register Stages 5–8.

FIG. 54 illustrates the Storage Select Register Decoding.

FIG. 55*a* illustrates the SSR Decoder 1–8.

FIG. 55*b* illustrates the SSR Decoder 9–15.

FIG. 56*a* illustrates the Set Bit Routing Controls.

FIG. 56*b* illustrates the Set Bit Routing Controls.

FIG. 57 illustrates the CR 1.

FIG. 58 illustrates the CR 1 Right Plate Outputs.

FIG. 59 illustrates the CR 1 Left Plate Outputs.

FIG. 60 illustrates the Instruction Check Circuits.

FIG. 61 illustrates the I Time Routing Controls.

FIG. 62 illustrates the Storage Sign Tgrs. & Controls.

FIG. 63*a* illustrates the Inter-Reg Check Routing 1.

FIG. 63*b* illustrates the Inter-Reg Check Routing 2.

FIG. 63*c* illustrates the Inter-Reg Check Tgr.

FIG. 64*a* illustrates the Add Address To Memory Routing Controls.

FIG. 64*b* illustrates the Add Address To Memory Routing Controls.

FIG. 64*c* illustrates the Add Address To Memory Routing Controls.

FIG. 65*a* illustrates the Unload Address.

FIG. 65*b* illustrates the Unload Address.

FIG. 66*a* illustrates the Divide Routing Controls.

FIG. 66*b* illustrates the Divide Routing Controls.

FIG. 66*c* illustrates the Divide Routing Controls.

FIG. 66*d* illustrates the Divide Routing Controls.

FIG. 66*e* illustrates the Divide Routing Controls.
FIG. 66*f* illustrates the Divide Routing Controls.
FIG. 66*g* illustrates the Divide Routing Controls.
FIG. 66*h* illustrates the Divide Routing Controls.
FIG. 66*i* illustrates the Divide Routing Controls.
FIG. 67*a* illustrates the Multiply Routing Controls.
FIG. 67*b* illustrates the Multiply Routing Controls.
FIG. 67*c* illustrates the Multiply Routing Controls.
FIG. 67*d* illustrates the Multiply Routing Controls.
FIG. 68*a* illustrates the Add To Memory Routing Controls.
FIG. 68*b* illustrates the Add To Memory Routing Controls.
FIG. 68*c* illustrates the Add To Memory Routing Controls.
FIG. 68*d* illustrates the Add To Memory Routing Controls.
FIG. 68*e* illustrates the Add To Memory Routing Controls.
FIG. 69*a* illustrates the Sign, No, Op, Receive & Stop Routing Controls.
FIG. 69*b* illustrates the Sign, No, Op, Receive & Stop Routing Controls.
FIG. 70*a* illustrates the Load Address Routing Controls.
FIG. 70*b* illustrates the Load Address Routing Controls.
FIG. 71*a* illustrates the CR 1 Recognition.
FIG. 71*b* illustrates the CR 1 Recognition.
FIG. 72 illustrates the CR 1 Code Check.
FIG. 73 illustrates the Adder Input Switching.
FIG. 74*a* illustrates the Reset Add, Reset Sub, Add-Sub Routing Controls.
FIG. 74*b* illustrates the Reset Add, Reset Sub, Add-Sub Routing Controls.
FIG. 74*c* illustrates the Reset Add, Reset Sub, Add-Sub Routing Controls.
FIG. 74*d* illustrates the Reset Add, Reset Sub, Add-Sub Routing Controls.
FIG. 74*e* illustrates the Reset Add, Reset Sub, Add-Sub Routing Controls.
FIG. 74*f* illustrates the Reset Add, Reset Sub, Add-Sub Routing Controls.
FIG. 74*g* illustrates the Reset Add, Reset Sub, Add-Sub Routing Controls.
FIG. 75 illustrates the CR 2 Outputs.
FIG. 76 illustrates the CR 2—Recognition.
FIG. 77 illustrates the CR 2 Code Check.
FIG. 78 illustrates the Multiple Register and Decoder.
FIG. 79 illustrates the Zone Adder.
FIG. 80 illustrates the Multiplicand Doubler & Quadrupler.
FIG. 81 illustrates the Quintupler.
FIG. 82 illustrates the Multiple Selection.
FIG. 83 illustrates the True/Comp Control.
FIG. 84 illustrates the Multiple Adder.
FIG. 85 illustrates the Decimal Correction Ckts.
FIG. 86 illustrates the Digit Adder.
FIG. 87 illustrates the Decimal Correction Circuits Digit Adder.
FIG. 88 illustrates the Dec Carry Circuits & Zone Carry Tgr.
FIG. 89*a* illustrates the Result Register Mem/Storage In Bus.
FIG. 89*b* illustrates the Result Register—Mem/Storage In Bus.
FIG. 90 illustrates the C Bit Generator.
FIG. 91 illustrates the Result Register Code Check—Error Trigger.
FIG. 92 illustrates Memory Test-Character Selector.
FIG. 93*a* illustrates the Routing: Read, Storage: Read Memory.
FIG. 93*b* illustrates the Character Registers To Adder Routing.
FIG. 93*c* illustrates the Adder Out Routing.
FIG. 93*d* illustrates the Adder Carry Routing.
FIG. 93*e* illustrates the Adder Emitter and Mpl Reg. Routing.
FIG. 93*f* illustrates the Bit To Adder Routing.
FIG. 93*g* illustrates the Step MAC 1+1 Routing.
FIG. 93*h* illustrates the Step MAC 2+1, Step MAC 1+5, Step MAC 2+5.
FIG. 93*i* illustrates the Step SAC Routing.
FIG. 93*j* illustrates the Storage, Memory and Instruction Counter Routing.
FIG. 93*k* illustrates the Auxiliary Trig's. Routing.
FIG. 93*l* illustrates the Aux. Trig. Stor. High. Trig., And Rmdr. Trig. Routing.
FIG. 93*m* illustrates the Smt. Dzt. and Tnsn Trig. Routing.
FIG. 93*n* illustrates the Sign Chk Tgr Ovfl Chk Trig and Stor Sign Trig Routing.
FIG. 93*o* illustrates the R/W Chk Tgr Record Chk Tgr and Instr Chk Tgr. Routing.
FIG. 93*p* illustrates the Memory Control Routing.
FIG. 93*q* illustrates the Mode Control Routing.
FIG. 93*r* illustrates the Routing: End E Time.
FIG. 93*s* illustrates the Masr Input Switching.
FIG. 93*t* illustrates the I/O Sequence Routing Control.
FIG. 93*u* illustrates the Auto Tnsn Trig, Mach Chk Trig & Any Sig Trig Routing.
FIG. 93*v* illustrates the Block Add Tgr, Supp Code Checking.
FIG. 93*w* illustrates the Type Cycle Neons, Par I/O Chk Neon, Code Chk Neons.
FIG. 94 illustrates the P.C.T. Cable—Connector Receptacle Shown From Wiring Side.
FIG. 95 illustrates the IMC Drive Pulse Generator.
FIG. 96 illustrates the Clock Read Section of Ring.
FIG. 97 illustrates the Clock-Add Section of Ring.
FIG. 98 illustrates the Clock Write Section of Ring.
FIG. 99 illustrates the Clock-R-W/R-A-W Switching, Initial Reset.
FIG. 100 illustrates the Pulse Generator (D0. 4 Pulses).
FIG. 101 illustrates the Pulse Generator A (D0. 4 Pulses).
FIG. 102 illustrates the Pulse Generator (D1 & D2 Pulses).
FIG. 103*a* illustrates the Pulse Generator (D3 Pulses).
FIG. 103*b* illustrates the C.F. Pulse Power.
FIG. 104 illustrates the Pulse Generator (D3 & D4 Pulses).
FIG. 105 illustrates the Wave Form Gen. Use/Manual Status Cntl.
FIG. 106 illustrates the Manual Reset Keys.
FIG. 107 illustrates the Clear Memory Trigger.
FIG. 108 illustrates the Start Stop Controls.
FIG. 109 illustrates the Stop Controls.
FIG. 110 illustrates the Manual Store Controls.
FIG. 111 illustrates the Manual Instruction Controls.
FIG. 112 illustrates the Manual Display Controls.
FIG. 113 illustrates the Memory Test Controls.
FIG. 114 illustrates the Half-Multiple Step Controls.
FIG. 115 illustrates the Half Step Trigger.
FIG. 116 illustrates the Manual Timer Triggers.
FIG. 117 illustrates the Man Timer Execution Controls.
FIG. 118 illustrates the Manual Execution Controls.
FIG. 119 illustrates the Check Indicator Switches.
FIG. 120*a* illustrates the Alterations Switches.
FIG. 120*b* illustrates the Audible Signal Indication.
FIG. 121 illustrates the I/E and IA Tgrs.
FIG. 122 illustrates the ECC 1 & ECC 2 Tgrs.
FIG. 123 illustrates the I/E Timer Outputs.
FIG. 124 illustrates the I/E Timer Outputs.
FIG. 125*a* illustrates the Load, Unload, & Store Routing Controls.
FIG. 125*b* illustrates the Load, Unload & Store Routing Controls.
FIG. 125*c* illustrates the Load, Unload, & Store Routing Controls.

FIG. 126*a* illustrates the Store For Print Routing Controls.

FIG. 126*b* illustrates the Store For Print Routing Controls.

FIG. 127*a* illustrates the TSMT/Send Routing Controls.

FIG. 127*b* illustrates the TSMT/Send Routing Controls.

FIG. 128 illustrates the Blank Memory.

FIG. 129*a* illustrates the Set Left, Leng & Norm TR Routing Controls.

FIG. 129*b* illustrates the Set Left, Leng & Norm TR Routing Controls.

FIG. 129*c* illustrates the Set Left, Leng & Norm TR Routing Controls.

FIG. 129*d* illustrates the Set Left, Leng & Norm TR Routing Controls.

FIG. 130*a* illustrates the Shorten Right/Round Routing Controls.

FIG. 130*b* illustrates the Shorten Right/Round Routing Controls.

FIG. 130*c* illustrates the Shorten Right/Round Routing Controls.

FIG. 131 illustrates the R/W and Read Routing Controls.

FIG. 132*a* illustrates the Write-Write Erase Routing Controls.

FIG. 132*b* illustrates the Write-WR ER Routing Controls.

FIG. 133 illustrates the Select & Control Routing Controls.

FIG. 134*a* illustrates the I/O Sequence 1 & 2 Tgrs.

FIG. 134*b* illustrates the I/O Sequence Routing.

FIG. 134*c* illustrates the I/O Sequence Routing.

FIG. 134*d* illustrates the I/O Sequence—Read Service Call, Read Request Tgrs.

FIG. 134*e* illustrates the I/O Sequence—Write Service Call, Request Tgrs.

FIG. 134*f* illustrates the Trc Pull Down Pulse; I/O Sync Pulse.

FIG. 135*a* illustrates the Pct Request, Chk Smas To MAR & MASR/MAR Gate Tgrs.

FIG. 135*b* illustrates the Pct Request Execution Controls.

FIG. 136*a* illustrates the Overlap Control Triggers.

FIG. 136*b* illustrates the Overlap Execution Controls.

FIG. 136*c* illustrates the Transition Powering.

FIG. 136*d* illustrates the Not Transition & Add Tgr Powering.

FIG. 136*e* illustrates the Tnsn Tgr Mode Ctrl Tgr Powering.

FIG. 137 illustrates the Result To Memory & Result To Storage Tgrs.

FIG. 138*a* illustrates the Storage Hi and Lo Triggers.

FIG. 138*b* illustrates the Simult R/W & Read Call Tgrs.

FIG. 138*c* illustrates the Storage Mark Tgr & MAC 1=0 Tgr.

FIG. 138*d* illustrates the Any Signal Tgr & Smt Off.

FIG. 138*e* illustrates the Write Call, No Read, WR Response Tgrs.

FIG. 138*f* illustrates the Inst. Chk. Mach. Chk., & R/W Chk. Tgrs.

FIG. 138*g* illustrates the Record, Ovfl. & Sign—Chk. Tgrs.

FIG. 138*h* illustrates the Digit Zero Tgrs. & Remainder Tgr.

FIG. 138*i* illustrates the Auxiliary Tgr. 1.

FIG. 138*j* illustrates the Auxiliary Tgr. 1 Off Powering.

FIG. 138*k* illustrates the Auxiliary Tgr. 2.

FIG. 138*l* illustrates the Auxiliary Tgr. 2 Off Powering.

FIG. 139*a* illustrates the Resets.

FIG. 139*b* illustrates the Instruction Reset Machine Reset.

FIG. 139*c* illustrates the Result Reg. MAC 2, IC, Initial Select Reg. & MAR Resets.

FIG. 139*d* illustrates the —12 Clamps.

FIG. 139*e* illustrates the —12 Clamps.

FIG. 140*a* illustrates the Compare Routing Controls.

FIG. 140*b* illustrates the Compare Routing Controls.

FIG. 140*c* illustrates the Compare Routing Controls.

FIG. 141 illustrates the Auto Load Control.

FIG. 142*a* illustrates the Reference Voltage Regulator.

FIG. 142*b* illustrates the Driver Bias Voltage Regulator.

FIG. 143 illustrates the Filament Detection.

FIGURE 144 is a Memory Timing Chart.

FIGURE 145 is a Memory Timing Chart.

FIGURE 146 is a flow chart of the Transfer 01 Instruction.

The Data Processing System or Central Processing Unit (CPU) shown in FIG. 1 includes a pair of core storage devices designated as Core Memory **1.10** and Storage **1.12**. Memory **1.10** is the principal storage area and is capable of storing and transmitting instructions and data by means of Memory Control **1.13**. All data coming into or going out of the Arithmetic and Logical Unit (ALU), shown generally as **1.14**, must eventually go through Core Memory. On a Read Memory operation, the contents of a specified location in Memory Comprising five characters are placed in a Memory Buffer Register **1.16** and are retained there for further use. From the Memory Buffer Register, the Memory Out switch **1.17** determines which one of the five characters is placed in a Character Register 1 (CR 1) **1.18**. The numerical bits of CR 1 (8, 4, 2, 1) are sent either through Multiply circuits **1.20** by way of CR 1 to Adder controls **1.22**, or through the Digit Adder True Complement controls **1.24**, via CR 1 to True Complement control **1.26** to a Digit Adder **1.30**. Single characters are read from Core Storage **1.12** by means of Storage controls **1.32** and are placed in a Storage Buffer Register **1.34**. From the Storage Buffer Register, the information is moved to a Character Register 2 (CR 2) **1.36**. Since only one character at a time is read from Storage as opposed to five characters being read from Memory, character selection controls such as Memory Out circuits **1.17** are not required for CR 2. The numerical bits of CR 2 (8, 4, 2, 1) are sent to the Digit Adder True Complement controls **1.24** by way of CR 2 to True Complement controls **1.38**. The numerical bits of the character contained in CR 2 are placed in a Multiply register **1.40** by way of CR 2 to Multiple Register controls **1.42**. The numerical portion of the contents of CR 1 and CR 2 are either complemented or passed unmodified to the Digit Adder **1.30** under control of Complement controls **1.43**. The numerical portion of the contents of CR 1 (**1.18**) are multiplied by the contents of the Multiply register **1.40** and passed to the Digit Adder **1.30** under control of CR 1 to Adder Switch **1.22**.

In the Digit Adder **1.30**, numbers are added in the binary form; however, circuits are arranged so that the numbers are always decimally corrected by Decimal Correction circuits **1.44** unless such correction is intentionally suppressed. The zone portion (B, A) of characters contained in CR 2 are either complemented or passed unmodified to a Zone Adder **1.48** under control of Zone Adder-True Complement controls **1.50**. The zone portion (B, A) of characters contained in CR 1 are passed via CR 1 to Adder controls **1.22** to Zone Adder **1.48**. Normally, the Zone Adder does not add zone bits but merely passes such information through from either CR 1 or CR 2 (but not both) in unchanged form; however, by the use of certain instructions, zone bits may be added or subtracted. The output of the Decimal Correction Circuits **1.44** and the Zone Adder **1.48** may be placed in a Result Register **1.52** with the proper redundancy bit inserted by a C bit Generator **1.54**.

The contents of the Result Register **1.52** may be stored in Core Memory **1.10** or the original characters read from Memory into the Memory Buffer Register **1.16** may be returned to Memory under control of a Memory

In control **1.56**. Likewise, the contents of this Result Register **1.52** may be placed in storage by way of Storage In controls **1.58**. If the contents of the Result Register are not sent to Storage, then the original character in the Storage Buffer Register **1.34** is returned to Storage by way of said Storage In controls **1.58**. Communication with Memory may be had with Input-Output storage units through the use of the Memory Buffer Register and Parallel Character Transfer Busses **1.60**.

The principle employed by Overlap Mode Control is that data read from Memory and/or Storage during the Read portion of the cycle is used for computation during the Write portion of that cycle and also during the Read portion of the following cycle. The result of this computation is then returned to Memory or Storage during the Write portion of the second cycle.

As a general introduction to operation of the Data Processing System, several examples of operations performed in response to typical instructions will be described with reference to FIG. 1.

EXAMPLE I.—RESET AND ADD

A Reset and Add instruction enters a numerical field obtained from Core Memory **1.10** in Core Storage **1.12**. The address contained in the instruction specifies the location of the field in Memory and the particular part of Storage to be used. The Memory controls **1.13** cause the characters beginning with the lowest order character in the Memory field to be read from Memory into the Memory Buffer Register **1.16** in five character groups and the characters to be read serially into CR 1 (**1.18**) via the Memory Out controls **1.17**. The characters are transferred serially from CR 1 (**1.18**) to the Result Register **1.52** by way of CR 1 to Adder Controls **1.22**, Multiply circuits **1.20**, Digit Adder **1.30**, and Decimal Correction circuits **1.44**. In response to the Storage Address contained in the instruction, the Storage controls **1.32** cause the characters to be entered serially in Core Storage **1.12** via Storage In controls **1.58** from the Result Register **1.52**. The transfer of characters continues until a non-numerical character has been extracted from Core Memory **1.10** and sensed in CR 1 (**1.18**). The upper limit of the Storage field is then identified with a Storage Mark. The contents of Core Memory remain unchanged.

EXAMPLE II.—ADD

Considering now that a factor has been entered in Storage as described above, an Add instruction adds a numerical field from Core Memory **1.10** to the factor in Core Storage **1.12**. The address part of the Add instruction specifies the locations in Memory and the Core Storage unit which contain the numerical fields to be added. Starting with the lowest order of each numerical field, the characters are obtained from Memory and Storage and placed in CR 1 (**1.18**) and CR 2 (**1.36**), respectively. The numeric bits of the characters in CR 1 and CR 2 are transferred unmodified to the Digit Adder **1.30** and the sum is decimally corrected in Decimal Correction circuits **1.44** and placed in the Result Register **1.52**. The contents of the Result Register represents the sum of corresponding orders of the Memory and Storage fields and these contents replace the original factor in Storage.

Considering the timing of the operation just described, after the Instruction cycle has been completed, Execution cycles, having Read and Write portions, occur in succession. During the Read portion of the first Execution cycle two characters are obtained, one from Memory and one from Storage respectively, to be added; and during the Write portion of the first cycle no result is returned to Storage since addition of the first two numbers is in progress. The Read portion of the second cycle is used to obtain the next characters to be operated upon. During the Write portion of the second cycle, when addition of the characters obtained during the first cycle has been completed, the result of such addition is written into the address, in Storage read from during the first cycle. Overlapping of addition and Storage operations continues until the limit of the result is identified by a Storage Mark, except under certain conditions described in detail later. The contents of the Memory field remain unchanged.

EXAMPLE III.—STORE

A numerical field in Core Storage **1.12** is placed in Core Memory **1.10** by a Store instruction having an address portion specifying the Storage unit from which data is obtained and the location in Core Memory at which the field is to be stored. In response to Storage controls **1.32**, numeric characters are placed in CR 2 (**1.36**) successively and transferred to the Result Register **1.52** via CR 2 to T/C controls **1.38**, Digit Adder T/C controls **1.24**, Digit Adder **1.30** and Decimal Correction circuits **1.44**. Under control of Memory controls **1.13**, the contents of the Result Register **1.52** are placed in Core Memory at successively lower locations via Memory In controls **1.56**. The transfer between Core Storage and Core Memory continues until a Storage Mark is detected. The Store Instruction does not affect the contents of the field in Core Storage.

What has been described in the examples above will be described in more detail with reference to FIG. 2 and still more specifically with reference to the figures which follow FIG. 2.

The character code system employed for representing information uses a seven bit code for each character. A numeric portion expresses numeric information in the binary coded decimal notation (BCD), as mentioned previously, and a zone portion, in combination with the numeric portion, expresses alphabetic and symbolic information. These seven bits are divided into the following groups:

Check	Zone	Numeric
C	B, A	8, 4, 2, 1

The bit structure of a character may be expressed by placing a line over a bit not present in a character, for example, the number five (5) is written $\overline{C}\ \overline{B}\ A\ \overline{8}\ 4\ \overline{2}\ 1$. Alternately, the characters may be expressed in binary form using a "1" to denote the presence of a bit and a "0" to denote the absence of a bit, for example, the number five (5) is written 0000101. Often, it becomes convenient in the circuits to utilize the absence of a bit or bits within a character and when so doing, the bits of a character are inverted so that a "0" becomes a "1," or, for example, a line labeled $\overline{B}$ has a positive signal thereon when the B bit is "0."

The C bit or check bit is used when the number of Zone and Numeric bits in a character results in an odd sum so that, in all cases, the sum of all of the bits in the character, including a C bit, is an even amount. During the operations on information throughout the data processing system, the sum of the character bits is checked for an even total.

As shown in the examples, there is an absence of bits in the Zone positions when numeric information is represented and the value of the numeric portion is the sum of 8, 4, 2, 1 bits. When "0" is expressed, as a character, it is represented by an "8" bit and a "2" bit (0001010), but within the arithmetic and addressing units of the system, "0" is represented by the absence of bits. Alphabetic and symbolic characters are represented by combinations of Zone and Numeric bits. The following chart shows the bit configuration for each character and symbol.

Chart I

Alphabetic				Numerical			
Char	C	BA	8421	Char	C	BA	8421
A	1	11	0001	1	1	00	0001
B	1	11	0010	2	1	00	0010
C	0	11	0011	3	0	00	0011
D	1	11	0100	4	1	00	0100
E	0	11	0101	5	0	00	0101
F	0	11	0110	6	0	00	0110
G	1	11	0111	7	1	00	0111
H	1	11	1000	8	1	00	1000
I	0	11	1001	9	0	00	1001
J	0	10	0001				
K	0	10	0010	Numerical zero			
L	1	10	0011				
M	0	10	0100	0	0	00	1010
N	1	10	0101				
O	1	10	0110	Special char.			
P	0	10	0111				
Q	0	10	1000	.	1	11	1011
R	1	10	1001	□	0	11	1100
S	0	01	0010	$	0	10	1011
T	1	01	0011	*	1	10	1100
U	0	01	0100	,	0	01	1011
V	1	01	0101	%	1	01	1100
W	1	01	0110	#	1	00	1011
X	0	01	0111	@	0	00	1100
Y	0	01	1000	&	0	11	0000
Z	1	01	1001	-	1	10	0000
				Blank	1	01	0000
				/	0	01	0001

	Char	C	BA	8421
Acc. and Drum Mark	0	0	00	0000
Plus Zero	0	0	11	1010
Minus Zero	0	1	10	1010
Record Mark		1	01	1010
Group Mark		0	11	1111
Tape Mark		0	00	1111

CYCLES

An operation period is defined as the period of time during which the Data Processing System reads, interprets and performs instructions. Character cycles are classified according to the time in which they occur during an operation. The first Character cycle, of each operation, is the Instruction Character Cycle, ICC, and it is during this cycle that the five characters of an Instruction are obtained from Core Memory, the Operation code is recognized, various registers and controls are set, and the five characters comprising the Instruction are written back in the Core Memory. Following the Instruction cycle is a period defined as Execute time having a number of Execution Character cycles which depend, in part, upon the type of Instruction. For some Instructions, the number of Execution Character Cycles varies according to the length of the fields involved, although at least one Execution Character Cycle (ECC 1) is always required. The first Execute Cycle, namely, Execution Character Cycle 1 (ECC 1), is characterized by certain special functions to prepare for succeeding operations. For example, in arithmetic instructions, the Sign must be removed from a character addressed in Memory. In the Store for Print Instruction, the first character placed in Core Memory is either a Blank or a Hyphen depending on the setting of the Sign trigger of the Storage unit. In some instances, an Execution Character Cycle 2 (ECC 2) follows an ECC 1 cycle for the primarry purpose of identifying a second Execute cycle when the need arises for certain operations. Following ECC 1 or ECC 2 are as many Execute cycles as are necessary to complete the operation called for by the Instruction.

DESCRIPTION OF FIG. 2

Reference is made to FIGS. 2*a* through 2*hhh* which show, in block form, principal data portions of the Data Processing System of FIG. 1.

The convention employed in numbering lines in the logical block diagrams is as follows: from left to right, the first numbers and the letter, if any, to the period or point is the figure number from which the line originated; the next two numbers to the second point refer to a particular output line (these are usually numbered according to their positions on the originating sheet from top to bottom); and the last two numbers, when used, refer to either the character associated therewith or a particular bit within a character. In a few instances where one trigger is shown as an example of one bit position in a register of several character capacity, the output lines from the figure are numbered as follows from left to right: The first two digits and the letter, if any, refer to the figure, the next two numbers refer to a particular output line (usually numbered from top to bottom of the figure in numerical order), the next two numbers refer to the character number, and the last or right-hand number refers to the bit. For example, line X.**01.04**(B) originates in FIG. X, it is the first line at the top of the figure, and it refers to bit B of character 4. On rare occasions, a single output line is connected to several points and, thus, several lines may bear the same number. Each input line in the diagrams bears the number derived from its point of origin.

In the composite drawings of FIG. 2, data flows generally into the block at the top and out of the block at the bottom, and control lines which cause the movement of data enter the block from the left. Although the lines leaving the block diagrams are shown entering other logical block diagrams, a chart herein which follows the index facilitates location of the destination of lines leaving a diagram by giving a figure number for the destination.

FIG. 2*a* illustrates the Memory Control **1.13** of FIG. 1 and comprises Memory Decoders, FIGS. 3*a* through 3*e*, Y and X Switch Core Write and Read Drivers, FIGS. 4, 5*a*, 5*b*, 5*c*, 6, 7*a*, 7*b* and 7*c* (controls comprising FIGS. 5*d*, 5*e*, 5*f*, 5*g*, 5*h*, 7*d* and 7*e* not shown in FIG. 2), and Y and X Switch Core Matrices, FIGS. 8 and 9. The Memory In switches **1.56** of FIG. 1 are shown in FIG. 2*b* and comprise Input Select control, FIG. 10, Input Switch, FIGS. 11*a* and *b*, and Memory Inhibit circuits, FIGS. 12*a*, *b* and *c*. The Core Memory **1.10** of FIG. 1 is shown in FIG. 2*b* and in detail in FIG. 13. Additionally, FIG. 2*bx* illustrates the Instruction format, and FIG. 2*by* illustrates diagrammatically windings on one of the cores of FIG. 13. The Memory Buffer Register (MBR) **1.16** of FIG. 1 is shown in FIGS. 2*c* through 2*e* as having five orders for storing five characters comprising 35 bits. The details of sample orders of the MBR are shown in FIG. 14. The Sense Amplifiers of FIG. 2*c* are shown in detail in FIGS. 15*a* and *b* and connect the sense windings of Core Memory, by cable, with the input lines of the Memory Buffer Register. As shown in FIGS. 2*c*–2*e*, lines **15***b*.**01.00**(C through 1) are connected from the Sense Amplifiers to Character 0 position of the MBR, lines **15***b*.**01.01**(C through 1) are connected to Character 1 position of the MBR, lines **15***a*.**01.02**(C through 1) are connected to Character 2 position of MBR, lines **15***a*.**0.1.03**(C through 1) are connected to Character 3 position of MBR, and lines **15***a*.**01.04**(C through 1) are connected to Character 4 position of MBR. Output lines **14***b*.**01.00**($\overline{C}$ through $\overline{1}$), **14***b*.**01.01**($\overline{C}$ through $\overline{1}$), **14***a*.**01.02**($\overline{C}$ through $\overline{1}$), **14***a*.**01.03**($\overline{C}$ through $\overline{1}$) and **14***a*.**01.04**($\overline{C}$ through $\overline{1}$) are connected via cable to the Input Switch, FIG. 2*b*. Output lines **14***a*.**02.02**(A), **14***a*.**02.02**(B), **14***a*.**02.03**(A) and **14***a*.**02.03**(B) are provided to the Storage Select Register, FIG. 2*p* (FIGS. 16*a* through 16*d*) for Auxiliary Storage addressing. Numeric lines **14***a*.**02.03**(8), **14***a*.**02.03**(4), **14***a*.**02.03**(2), **14***a*.**02.03**(1), **14***a*.**02.02**(8), **14***a*.**02.02**(4), **14***a*.**02.02**(2), **14***a*.**02.02**(1), **14***b*.**02.01**(8), **14***b*.**02.01**(4), **14***b*.**02.01**(2) and **14***b*.**02.01**(1) are furnished from Character 1, 2 and 3 positions of MBR to the thousands, hundreds and tens order of FIGS. 2*s* and 2*t* of the Memory Address Register, FIGS. 2*r* through 2*t* (FIGS.

17*a* through 17*e*). Numeric lines **14***a*.**02.03**(2), **14***a*.-**02.03**(8), **14***a*.**02.02**(2), **14***a*.**02.02**(8), **14***b*.**02.01**(2) and **14***b*.**02.01**(8) are connected to Memory Address Register Controls of FIG. 2*u* (FIG. 17*f*). Zone lines **14***b*.**02**.-**01**(A), **14***b*.**02.01**(B) and **14***a*.**02.04**(B) are connected to the ten thousands order of MBR of FIG. 2*t* (FIG. 17*e*). Lines **14***b*.**04.00**(C through 1), **14***b*.**04.01**(C through 1), **14***a*.**04.02**(C through 1), **14***b*.**04.03**(C through 1) and **14***a*.**05.04**(C through 1) are connected as inputs to the Parallel Character Transmission Write Bus, FIG. 2*f* (FIGS 18*a* and *b*). Lines **14***b*.**04.00**(C through 1), **14***b*.**05.01**(C through 1), **14***a*.**05.02**(C through 1), **14***a*.**05.03**(C through 1) and **14***a*.**05.04**(C through 1) are coupled to the MBR Code Check of FIG. 2*f* (FIGS. 19*a* and *b*). Code Check Odd lines **19***a*.**01** and **19***b*.**01** are connected to MBR Code Check outputs of FIG. 19*c* (not shown in FIG. 2). Lines **14***b*.**06.00**(C through 1), **14***b*.**06.01**(C through 1), **14***b*.**06.02**(C through 1), **14***a*.**06.03**(C through 1) and **14***a*.**06.04**(C through 1) are coupled to Memory Out of FIG. 2*g* (FIGS. 20*a*, *b*, *c* and *d*). Output lines **14***b*.**02.00**(C through 1) from Character 0 position of the MBR are connected to the Operation Register of FIG. 2*v* (FIGS. 21*a* and *b*).

From the Keyboard of FIG. 2*v* (FIGS. 22*a* through *c*), output lines **22***b*.**07**(C), **22***b*.**06**(B), **22***b*.**05**(A), **22***b*.**04**(8), **22***b*.**03**(4), **22***b*.**02**(2) and **22***b*.**01**(1) are connected to corresponding bit positions of the Operation Register of FIG. 2*v* (FIGS. 21*a* and *b*). Outputs of the Operation Register are provided to an Operation Decoder, FIG. 2*v* (FIGS. 23*a* through 23*l*) and Operation Check Circuits, FIG. 2*v* (FIG. 24).

The units order of MAR, FIG. 2*r*, receives numeric input lines **20***d*.**04**(8), **20***d*.**05**(4), **20***d*.**06**(2) and **20***d*.**07**(1) from Character 4 position of the MBR via Memory Out controls, FIG. 2*g* (FIGS. 20*a* through 20*d*). The Memory Address Selector including manually operable keys, FIG. 2*q* (FIGS. 25*a* and *b*), provide numeric inputs to all orders of MAR via lines **25***b*.**01** through **25***b*.**19**. Input lines **26***a*.**126**, **26***a*.**135**, **26***a*.**133**, **26***a*.**130**, **26***a*.**128**, **26***a*.**144**, **26***a*.**142**, **26***a*.**140**, **26***a*.**138**, **26***a*.**154**, **26***a*.**151**, **26***a*.**149**, **26***a*.**147**, **26***a*.**156**, **26***a*.**158** and **26***a*.**160** are provided to all orders of MAR from the Synchronizer Memory Address Counter (not shown) via the Parallel Character Transmission cable, FIG. 2*r*, associated with a connector shown in FIG. 26*a* of a pair of connectors of FIGS. 26*a* and *b*.

Output lines **17***a*.**07**, **17***a*.**02**, **17***a*.**16**, **17***a*.**10**, **17***a*.**23**, **17***a*.**18**, **17***a*.**31** and **17***a*.**26** from the units order of MAR, FIG. 2*r*, are connected to a Control Address Decoder, FIG. 2*jj* (FIG. 27). Outputs of all orders of MAR, namely, lines **17***a*.**27**, **17***a*.**19**, **17***a*.**13**, **17***a*.**03**, **17***b*.**27**, **17***b*.**19**, **17***b*.**11**, **17***b*.**04**, **17***c*.**31**, **17***c*.**22**, **17***c*.**13**, **17***c*.**05**, **17***d*.**31**, **17***d*.**22**, **17***d*.**13**, **17***d*.**05**, **17***e*.**04**, **17***e*.**10** and **17***e*.**17**, are coupled to the Synchronizer Memory Address Counter Checking, FIG. 2*ii* (FIG. 28). Output lines **17***a*.**12**, **17***b*.**26**, **17***b*.**18**, **17***b*.**10**, **17***b*.**03**, **17***c*.**30**, **17***c*.**21**, **17***c*.**12**, **17***c*.**04**, **17***d*.**30**, **17***d*.**21**, **17***d*.**12**, **17***d*.**04**, **17***e*.**03**, **17***e*.**09** and **17***e*.**16** from the first through fifth order of MAR are directed to Memory Address Select Register or Memory Address Register to Data Synchronizer Unit (MASR/MAR to DSU), FIG. 2*u* (FIGS. 29*a* and *b*). Output lines **17***a*.**01**, **17***a*.**05**, **17***a*.**08**, **17***a*.**14**, **17***a*.**17**, **17***a*.**21**, **17***a*.**25**, and **17***a*.**29** from the units position of MAR are connected as inputs to the units position of MAC 1, FIG. 2*gg* (FIG. 30*a*). From the tens position of MAR, lines **17***b*.**02**, **17***b*.**05**, **17***b*.**09**, **17***b*.**12**, **17***b*.**17**, **17***b*.**20**, **17***b*.**25**, and **17***b*.**28** enter the tens position of MAC 1 (FIG. 30*b*). Lines **17***c*.**03**, **17***c*.**06**, **17***c*.**10**, **17***c*.**19**, **17***c*.**23**, **17***c*.**28**, and **17***c*.**32** from the hundreds position of MAR are connected to the hundreds order of MAC 1 (FIG. 30*c*). Lines **17***d*.**03**, **17***d*.**06**, **17***d*.**11**, **17***d*.**14**, **17***d*.**20**, **17***d*.**23**, **17***d*.**29** and **17***d*.**32** from the thousands order of MAR are connected to the thousands order of MAC 1 (FIG. 30*d*). Lines **17***e*.**02**, **17***e*.**05**, **17***e*.**08**, **17***e*.**11**, **17***e*.**15**, **17***e*.**18** from the ten thousands order of MAR are coupled to the ten thousands order of MAC 1 (FIG. 30*e*). Decoding circuits are provided for MAC 1 in FIG. 2*gg* (FIG. 30*g*) to determine the digit in the units position of MAC 1 and to determine the end of Memory. Orders of MAR are connected by cable to corresponding orders of MAC 2 of FIG. 2*hh* (FIGS. 31*a* through *e*) via lines **17***a*.**04**, **17***a*.**11**, **17***a*.**20**, **17***a*.**28**, **17***b*.**06**, **17***b*.**13**, **17***b*.**21**, **17***b*.**29**, **17***c*.**07**, **17***c*.**15**, **17***c*.**24**, **17***c*.**33**, **17***d*.**07**, **17***d*.**15**, **17***d*.**24**, **17***d*.**33**, **17***e*.**06**, **17***e*.**12**, and **17***e*.**19**. In order to obtain instructions for operation in response to the stored program, outputs are provided from MAR to an Instruction Counter, FIG. 2*ii* (FIGS. 32*a* through *e*) on the lines **17***a*.**09**, **17***a*.**07**, **17***b*.**14**, **17***b*.**22**, **17***b*.**30**, **17***c*.**08**, **17***c*.**16**, **17***c*.**25**, **17***c*.**34**, **17***d*.**08**, **17***d*.**16**, **17***d*.**25**, **17***d*.**34**, **17***e*.**07**, **17***e*.**13** and **17***e*.**20**. Outputs from the first through fourth orders of MAR are provided to the Select Register, FIG. 2*jj* (FIGS. 33*a* through *d*) on the lines **17***a*.**06**, **17***a*.**15**, **17***a*.**22**, **17***a*.**30**, **17***b*.**08**, **17***b*.**15**, **17***b*.**23**, **17***b*.**31**, **17***c*.**09**, **17***c*.**17**, **17***c*.**26**, **17***c*.**35**, **17***d*.**09**, **17***d*.**17**, **17***d*.**26** and **17***d*.**35** for selecting Input-Output units. Select Register Controls are shown in FIG. 33*e* and ALU Select Register Decoder is shown in FIGS. 33*f* and *g*. Output lines **17***c*.**20**, **17***c*.**11**, **17***c*.**29**, **17***c*.**02**, **17***d*.**28**, **17***d*.**19**, **17***d*.**10** and **17***d*.**02** from the third and fourth orders of MAR are used in MAR Controls, FIG. 2*u* (FIG. 17*f*) to provide Block Call for Half Step signals.

The Storage Controls **1.32** of FIG. 1 are shown in FIG. 2*tt* connected as shown and comprising Decoders, FIGS. 34*a* through *d*; X Switch Core Read Drivers, FIG. 35; Y Switch Core Write Drivers, FIGS. 36*a* and *b*; Y Switch Core Read Drivers, FIG. 37; X Switch Core Write Drivers, FIGS. 38*a* through *c*; Y Switch Core Matrix, FIG. 39; X Switch Core Matrix, FIG. 40; Storage Write Driver Select Circuits, FIG. 41; and Odd-Even Gating Circuits, FIG. 42.

The Storage In Controls **1.58** of FIG. 1 are shown in FIG. 2*uu* and include Storage In Select and Switching Circuits, FIG. 43, and Storage Inhibit Circuits, FIG. 44. The Core Storage **1.12** of FIG. 1 is also shown in FIG. 2*uu* and in detail in FIG. 45. Sensing outputs of the Storage Array, FIG. 2*uu*, are passed through Sense Amplifiers, FIG. 2*vv* (FIG. 46) to a Storage Buffer Register **1.34** of FIG. 1 (FIG. 2*vv*) on the lines **46.01**(C), **46.02**(B), **46.03**(A), **46.04**(8), **46.05**(4), **46.06**(2) and **46.07**(1). Logical circuits of the Storage Buffer Register are shown in FIG. 47. Outputs of the Storage Buffer Register are provided by cable to the Storage In Select and Switching circuits, FIG. 2*uu*, on the lines **47.01**($\overline{C}$), **47.02**($\overline{B}$), **47.03**($\overline{A}$), **47.04**($\overline{8}$), **47.05**($\overline{4}$), **47.06**($\overline{2}$) and and **47.07**($\overline{1}$). Another set of outputs are provided by cable from the Storage Buffer Register of FIG. 2*vv* to Character Register 2 in FIG. 2*kk* (**1.36** of FIG. 1) on the lines **47.08**(C), **47.09**(B), **47.10**(A), **47.11**(8), **47.12**(4), **47.13**(2) and **47.14**(1). Details of CR 2 are shown in FIG. 48.

Signals from the Memory Address Counter 1, FIG. 2*gg*, are provided by cable to a Memory Address Select Register (MASR), FIGS. 2*ww* through 2*yy* (FIGS. 49*a* through *j*) on the lines **30***a*.**03**, **30***a*.**07**, **30***a*.**10**, **30***a*.**13**, **30***b*.**02**, **30***b*.**05**, **30***b*.**06**, **30***b*.**07**, **30***c*.**02**, **30***c*.**05**, **30***c*.**06**, **30***c*.**07**, **30***d*.**02**, **30***d*.**05**, **30***d*.**06**, **30***d*.**07**, **30***e*.**01**, **30***e*.**03** and **30***e*.**05**. Also, signals from the Memory Address Counter 2, FIG. 2*hh*, are provided by cable to the MASR, FIGS. 2*ww* through 2*yy*, on the lines **31***a*.**01**, **31***a*.**03**, **31***a*.**04**, **31***a*.**05**, **31***b*.**01**, **31***b*.**03**, **31***b*.**04**, **31***b*.**05**, **31***c*.**01**, **31***c*.**03**, **31***c*.**04**, **31***c*.**05**, **31***d*.**01**, **31***d*.**03**, **31***d*.**04**, **31***d*.**05**, **31***e*.**01**, **31***e*.**02** and **31***e*.**03**.

Signals from the Instruction Counter, FIG. 2*ii* (FIGS. 32*a* through 32*e*) are provided by cable (broken) to Transfer Routing Controls, FIG. 2*aa* (FIGS. 50*a* through 50*g*) on the lines **32***a*.**02**, **32***a*.**05**, **32***b*.**03**, **32***b*.**05**, **32***b*.**07**, **32***b*.**09**, **32***c*.**03**, **32***c*.**05**, **32***c*.**07**, **32***c*.**09**, **32***d*.**03**, **32***d*.**05**, **32***d*.**07**, **32***d*.**09**, **32***e*.**02**, **32***e*.**04** and **32***e*.**06**. Another set

of outputs is provided on the lines **32***a*.**10**, **32***a*.**01**, **32***a*.**03**, **32***b*.**01**, **32***b*.**04**, **32***b*.**06**, **32***b*.**08**, **32***c*.**01**, **32***c*.**04**, **32***c*.**06**, **32***c*.**08**, **32***d*.**01**, **32***d*.**04**, **32***d*.**06**, **32***d*.**08**, **32***e*.**01**, **32***e*.**03** and **32***e*.**05** by cable to the Memory Address Select Register, FIGS. 2*ww* to 2*yy*.

Signals from the Starting Point Counter, FIG. 2*q*, (FIGS. 51*a* through 51*c*) are provided by cable on lines **51***c*.**04**, **51***c*.**03**, **51***c*.**02**, **51***c*.**01**, **51***b*.**06**, **51***b*.**05**, **51***b*.**04**, **51***b*.**03**, **51***b*.**02**, **51***b*.**01**, **51***a*.**06**, **51***a*.**05**, **51***a*.**04**, **51***a*.**03**, **51***a*.**02** and **51***a*.**01**, to all orders of the Storage Address Counter, FIG. 2*ff* (FIGS. 52*a* through *d*). SAC controls (not shown in FIG. 2) are illustrated in FIG. 52*e*. Additional inputs to stages 5 through 8 of SAC are provided by cable from the Storage Select Register, FIG. 2*p*, via lines **16***a*.**06**, **16***a*.**02**, **16***a*.**09**, **16***a*.**13**, **16***a*.**16**, **16***a*.**20**, **16***a*.**23** and **16***a*.**27**.

Output from all stages of SAC, FIG. 2*ff*, are furnished by cable as inputs to a Storage Address Select Register, FIG. 2*ee* (FIGS. 53*a* and *b*) on the lines **52***c*.**09**, **52***c*.**08**, **52***c*.**07**, **52***c*.**06**, **52***c*.**05**, **52***c*.**04**, **52***c*.**03**, **52***c*.**02**, **52***a*.**08**, **52***a*.**07**, **52***a*.**06**, **52***a*.**05**, **52***a*.**04**, **52***a*.**03**, **52***a*.**02** and **52***a*.**01**. In turn, SASR of FIG. 2*ee*, provides outputs on the lines **53***b*.**08**, **53***b*.**07**, **53***b*.**06**, **53***b*.**05**, **53***b*.**04**, **53***b*.**03**, **53***b*.**02**, **53***b*.**01**, **53***a*.**08**, **53***a*.**07**, **53***a*.**06**, **53***a*.**05**, **53***a*.**04**, **53***a*.**03**, **53***a*.**02** and **53***a*.**01** to the Storage Address Decoders of FIG. 2*tt*.

Two more sets of output lines from the Storage Select Register, FIG. 2*p*, are provided by separate cable to Storage Select Register Decoding, FIG. 2*ee* (FIG. 54) and SSR Decoders, FIG. 2*p* (FIGS. 55*a* and *b*). SSR lines **16***a*.**03**, **16***a*.**10**, **16***a*.**17** and **16***a*.**24** are connected to SSR Decoding and lines **16***a*.**06**, **16***a*.**02**, **16***a*.**07**, **16***a*.**08**, **16***a*.**11**, **16***a*.**12**, **16***a*.**14**, **16***a*.**15**, **16***a*.**18**, **16***a*.**19**, **16***a*.**21**, **16***a*.**22**, **16***a*.**25** and **16***a*.**26** are connected to SSR Decoders. SSR Decoding of FIG. 2*ee* (FIG. 54) furnishes outputs to the 2×4 Storage Decoder of FIG. 2*tt*. Outputs of the SSR Decoders of FIG. 2*p* (FIGS. 55*a* and *b*) are furnished by cable (broken) to Set Bit Routing Controls, FIG. 2*x* (FIGS. 56*a* and *b*) on lines **55***a*.**02**, **55***a*.**08**, **55***a*.**11**, **55***a*.**15**, **55***a*.**18**, **55***a*.**19**, **55***a*.**22**, **55***a*.**23**, **55***a*.**27**, **55***a*.**28**, **55***b*.**01**, **55***b*.**03**, **55***b*.**04**, **55***b*.**06**, **55***b*.**08**, **55***b*.**09**, **55***b*.**11** and **55***b*.**12**. Also, SSR Decoder outputs are provided to Transfer Routing Controls, FIG. 2*aa* (FIGS. 50*a* through 50*g*) on the lines **55***a*.**03**, **55***a*.**04**, **55***a*.**05**, **55***a*.**06**, **55***a*.**09**, **55***a*.**10**, **55***a*.**12**, **55***a*.**13**, **55***a*.**14**, **55***a*.**16**, **55***a*.**17**, **55***a*.**20**, **55***a*.**21**, **55***a*.**24**, **55***a*.**25**, **55***a*.**26**, **55***b*.**02**, **55***b*.**05**, **55***b*.**07**, **55***b*.**10**, **55***b*.**13** and **55***b*.**14**. Additionally, output lines from SSR Decoders 1 and 2 are sent to Input-Output Controls via the PCT bus.

Memory Out, FIG. 2*g* (FIGS. 20*a* through *d*) provide outputs to CR 1, FIG. 2*h*, on the lines **20***d*.**01**(C), **20***d*.**02**(B), **20***d*.**03**(A), **20***d*.**04**(8), **20***d*.**05**(4), **20***d*.**06**(2) and **20***d*.**07**(1). Character Register 1 (CR 1) has three sets of outputs. The Right Plate outputs are sent by cable to CR 1 Right Plate Output Distributor Circuits, FIGS. 2*k* through 2*m* (FIG. 58) on the lines **57.03**(C), **57.05**(B), **57.07**(A), **57.09**(8), **57.11**(4), **57.13**(2) and **57.15**(1). Left Plate Outputs of CR 1 are provided by cable to the Left Plate Output Distributor Circuits, FIGS. 2*i* through 2*j* (FIG. 59) on the lines **57.04**($\overline{B}$), **57.06**($\overline{A}$), **57.08**($\overline{8}$), **57.10**($\overline{4}$), **57.12**($\overline{2}$), and **57.14**($\overline{1}$). Outputs from $\overline{C}$ of Character Register 1 are provided on line **57.02**($\overline{C}$) to Transfer Routing Controls, FIG. 2*aa* (FIGS. 50*a* through *g*) and on line **57.01**($\overline{C}$) to Set Bit Controls, FIG. 2*x* (FIGS. 56*a* and *b*). A line **58.33**(A) from the Right Plate Distributor Circuits, FIG. 2*l* (FIG. 58) is sent to Instruction Time Check, FIG. 2*bb* (FIG. 60). A line **59.21**($\overline{A}$) from the Left Plate Distributor Circuits, FIG. 2*i* and line **58.27**(A) from the right Plate Distributor Circuits, FIG. 2*l* goes to Instruction Time Routing Control, FIG. 2*bb* (FIG. 61). Lines **59.22**($\overline{A}$) and **59.03**($\overline{B}$) from Left Plate Out, FIG. 2*i*, and lines **58.28**(A) and **58.17**(B) from Right Plate Out, FIGS. 2*k* and *l*, are connected as inputs to Storage Sign Trigger controls, FIG. 2*aa* (FIG. 62). The NOT lines from code bit position of CR 1 Left Plate Outputs of FIGS. 2*i* and *j* go to Inter Register Check Routing and Trigger, FIG. 2*z* (FIG. 63). Lines **58.12**(B) and **58.26**(A) from the Right Plate Distributor, FIGS. 2*k* and *l*, are connected as inputs to Add Address to Memory Routing Controls, FIG. 2*z* (FIGS. 64*b* and *c*) and lines **58.15**(B) and **58.31**(A) originating in FIGS. 2*k* and *l* go to Unload Address Controls, FIG. 2*z* (FIG. 65*b*). Line **59.04**($\overline{B}$) originates at CR 1B Left Plate Out, FIG. 2*i*, and goes to FIG. 2*y*, Divide Routing Controls, FIG. 66*h*. Line **59.09**($\overline{B}$) from FIG. 2*i*, CR 1 Left Plate Output, goes to Multiply Routing Controls, FIG. 2*y* (FIG. 67). Lines **58.09**(B), **58.10**(B), **58.11**(B) and **58.25**(A) from CR 1 Right Plate Outputs, FIG. 2*k*, and lines **59.05**($\overline{B}$) and **59.17**($\overline{A}$) from FIG. 2*i* are connected to Add to Memory Routing Controls, FIG. 2*x* (FIGS. 68*a* through *e*). Lines **58.05**(B), **58.22**(A) and **59.14**($\overline{A}$) from FIGS. 2*k*, *l* and *i* are connected as inputs to Set Bit Routing Controls, FIG. 2*x* (FIGS. 56*a* and *b*). Lines **59.10**($\overline{B}$) and **59.20**($\overline{A}$) from FIG. 2*i* and lines **58.16**(B) and **58.32**(A) from FIGS. 2*k* and *l* furnish signals to Sign, No Operation and Stop Routing Controls, FIG. 2*x* (FIGS. 69*a* and *b*). Lines **58.07**(B), **58.08**(B) and **58.24**(A) from FIGS. 2*k* and *l* are provided by cable to Load Address Routing Controls, FIG. 2*w* (FIGS. 70*a* and *b*). Lines **58.18**(B), **58.34**(A), **58.38**(8), **58.43**(4), **58.48**(2) and **58.53**(1), one line from each data bit position of CR 1, Right Plate Outputs, FIGS. 2*k*, *l* and *m*, and NOT lines **59.11**($\overline{B}$), **59.23**($\overline{A}$), **59.28**($\overline{8}$), **59.33**($\overline{4}$), **59.38**($\overline{2}$) and **59.43**($\overline{1}$) from CR 1 Left Plate Outputs, FIGS. 2*i* and *j*, are provided to CR 1 Recognition Circuits, FIG. 2*n* (FIG. 71*a*). Lines **58.02**(C), **58.19**(B), **58.39**(8), **58.44**(4), **58.49**(2), and **58.54**(1) from CR 1 Right Plate Outputs and lines **59.12**($\overline{B}$), **59.24**($\overline{A}$), **59.29**($\overline{8}$), **59.34**($\overline{4}$), **59.39**($\overline{2}$) and **59.44**($\overline{1}$) from CR 1 Left Plate Outputs are directed to CR 1 Recognition Circuits, FIG. 2*o* (FIG. 71*b*). Lines **58.03**(C), **59.20**(B), **58.35**(A), **58.40**(8), **58.45**(4), **58.50**(2) and **58.55**(1) from CR 1 Right Plate Outputs, FIGS. 2*k*, *l* and *m*, and **59.13**($\overline{B}$), **59.25**($\overline{A}$), **59.30**($\overline{8}$), **59.35**($\overline{4}$), **59.40**($\overline{2}$) and **59.45**($\overline{1}$) from CR 1 Left Plate Outputs, FIGS. 2*i* and *j*, are connected by cables to CR 1 Code Check, FIG. 2*o* (FIG. 72). Lines **58.06**(B), **58.23**(A), **58.37**(8), **58.32**(4), **58.47**(2) and **58.25**(1) from CR 1 Right Plate Outputs, FIGS. 2*k*, *l* and *m*, are connected by cable to inputs of Adder Input Switching, FIG. 2*qq* (FIG. 73). Lines **58.04**(C), **58.21**(B), **58.36**(A), **58.41**(8), **58.46**(4), **58.51**(2) and **58.56**(1) from CR 1 Right Plate Outputs are directed to the I/O Parallel Character Transfer Cable (broken), FIG. 2*m* (FIG. 26*b*).

Output lines **59.01**($\overline{B}$), **59.15**($\overline{A}$), **59.26**($\overline{8}$), **59.31**($\overline{4}$), **59.36**($\overline{2}$) and **59.41**($\overline{1}$) from CR 1 Left Plate Outputs (FIGS. 2*i*, *k* and *l*) are connected by cable to Transfer Routing Controls, FIG. 2*aa* (FIGS. 50*a* through *g*). Output lines **59.07**($\overline{B}$), **59.06**($\overline{B}$), **59.08**($\overline{B}$), **58.13**(B), **58.14**(B), **59.18**($\overline{A}$), **59.19**($\overline{A}$), **58.29**(A) and **58.30**(A) of CR 1 Right and Left Plate Output Circuits are sent by cable to Reset Add, Reset Subtract, Add and Subtract Routing Controls of FIG. 2*y* (FIGS. 74*b*, *c*, *e*, and *f*). Output lines **59.02**($\overline{B}$), **59.16**($\overline{A}$), **59.27**($\overline{8}$), **59.32**($\overline{4}$), **59.37**($\overline{2}$) and **59.42**($\overline{1}$) from CR 1 Left Plate Outputs are provided by cable as inputs to Inter Register Check Routing, FIG. 2*z*, (FIGS. 63*a*, *b* and *c*).

In FIG. 2*kk*, pairs of complementary output lines **48.04** through **48.15**, representing the bit configurations of the zone and numeric portions of the characters in CR 2 are sent by cable to CR 2 Distribution Circuits of FIGS. 2*ll* through 2*nn* (FIG. 75).

Output lines from CR 2 Distribution Circuits, FIGS. 2*ll*, *mm* and *nn*, comprising **75.07**($\overline{B}$), **75.10**(A), **75.14**($\overline{A}$), **75.18**(8), **75.22**($\overline{8}$), **75.27**(4), **75.33**($\overline{4}$), **75.39**(2), **75.43**($\overline{2}$), **75.49**(1) and **75.53**($\overline{1}$) are sent by cable to CR 2 Recognition, FIG. 2*oo* (FIG. 76). Output lines

from CR 2 Distribution Circuits, FIG. 2*ll*, *mm* and *nn*, comprising **75.04**(B) **75.08**($\overline{B}$), **75.11**(A), **75.15**($\overline{A}$), **75.19**(8), **75.23**($\overline{8}$), **75.28**(4), **75.34**($\overline{4}$), **75.40**(2), **75.44**($\overline{2}$), **75.50**(1) and **75.54**($\overline{1}$) are directed by cable to CR 2 Code Check of FIG. 2*pp* (FIG. 77). Output lines from CR 2 Distribution Circuits, FIGS. 2*mm* and 2*nn*, comprising **75.17**(8), **75.21**($\overline{8}$), **75.32**($\overline{4}$), **75.26**(4), **75.38**(2), **75.42**($\overline{2}$), **75.52**($\overline{1}$) and **75.48**(1), representing the numeric bit configuration and the complement thereof of the character in CR 2, are sent by cable to Multiplier Register and Decoder, FIG. 2*hhh* (FIG. 78), which, in turn, provides output lines **78.01**, **78.02**, **78.03**, **78.04** and **78.06** to the Multiple Selector of FIGS. 2*rr* and 2*ss* (FIG. 82).

Output lines **73.08**(B) and **73.01**(A) from the B and A positions of Adder Input Switching, FIG. 2*qq*, are furnished as inputs to the Zone Adder, FIG. 2*ccc* (FIG. 79). Lines **73.02**(8), **73.04**(4), **73.03**(2), **73.05**(1) and **73.06**($\overline{1}$) are sent to the Multiplicand Doubler and Quadrupler of FIG. 2*dd* (FIG. 80) from Adder Input Switching, FIG. 2*qq*. The numeric portion of the Multiplicand character is also provided to the Quintupler, FIG. 2*cc* (FIG. 81) from Adder Input Switching via lines **73.02**(8), **73.04**(4), **73.03**(2), **73.05**(1) and **73.07**($\overline{1}$). Similarly, the numeric position of the Multiplicand character is furnished to Multiple Selection, FIGS. 2*rr* and 2*ss* (FIG. 82), via lines **73.02**(8), **73.04**(4), **73.03**(2), and **73.05**(1) from Adder Input Switching. Also, the numeric portion of the Multiplicand character, FIG. 2*qq*, is directed to True/Complement Control, FIG. 2*fff* (FIG. 83), by the lines **73.09**(8), **73.10**(4), **73.11**(2), **73.12**($\overline{1}$) and **73.13**(1).

The Multiple Selector receives five times the multiplicand character value from the Quintupler, FIG. 2*cc*, via lines **81.01** through **81.05**, two times the value on the lines **80.02** through **80.04** from the Doubler, four times the value on the lines **80.01**, **80.06**, **80.07** and **80.08** from the Quadrupler, FIG. 2*dd*, and one times the value from Adder Input Switching, as described previously. The desired multiples are selected by the control lines **78.01**, **78.02**, **78.03**, **78.06** and **78.04** entering Multiple Selection of FIG. 2*rr* from the Multiplier Register and Decoder of FIG. 2*hhh*.

Output lines from the Multiple Selection, FIGS. 2*rr* and 2*ss*, comprising lines **82.04** through **82.08** are furnished by cable to the Multiple Adder of FIG. 2*hhh* (FIG. 84), which, in turn, provides output lines **84.03** through **84.06** to Decimal Correction Circuits of FIG. 2*ggg* (FIG. 85). An output line of the Multiple Adder, **84.01**, is connected as an input to the Digit Adder of FIG. 2*eee* (FIG. 86) and a line **84.02** is connected to Set Bit Routing Controls, FIG. 2*x* (FIG. 56*a*).

The Decimal Correction circuits of FIG. 2*ggg* (FIG. 85) furnish output lines **85.02**(2), **85.04**(4) and **85.06**(8) to Set Bit Routing Controls of FIG. 2*x* (FIG. 56*a*), and output lines **85.01**(2), **85.03**(4) and **85.05**(8) by cable to the Digit Adder, FIG. 2*eee* (FIG. 86).

The Digit Adder has two sets of output lines. One set comprising lines **86.08**(8) Carry, **86.06**(8), **86.04**(4), **86.02**(2) and **86.01**(1) goes to Decimal Correction Circuits, Digit Adder, FIG. 2*ccc* (FIG. 87), while the other set, comprising **86.09**(8), **86.07**(8), **86.05**(4) and **86.03**(2) goes to Decimal Carry Circuits and Zone Carry Trigger, FIG. 2*ddd* (FIG. 88).

In FIG. 2*ccc*, output lines **87.09**(1), **87.02**(2), **87.06**(4) and **87.14**(8) from the Decimal Correction Circuits are furnished by cable to the Result Register, FIG. 2*aaa* (FIGS. 89*a* and *b*); lines **87.13**(8), **87.05**(4), **87.01**(2) and **87.12**(1) are sent by cable to C Bit Generator, FIG. 2*bbb* (FIG. 90); and lines **87.16**(8), **87.15**(8), **87.07**(4), **87.08**(4), **87.03**(2), **87.04**(2), **87.10**(1) and **87.11**(1) are directed by cable to Inter Register Check, FIG. 2*z* (FIGS. 63*a*, *b* and *c*).

In FIG. 2*ll* (FIG. 75), output lines **75.03**(B), **75.06**($\overline{B}$), **75.09**(A), and **75.13**($\overline{A}$) from CR 2 Distribution Circuits, provide the zone bits and complements to the True/Complement portion of the Zone Adder, FIG. 2*fff* (FIG. 79). Output lines **79.16** and **79.17** from the True/Complement portion of the Zone Adder, FIG. 2*fff*, are connected to the Zone Adder, FIG. 2*ccc*. The Zone Adder has three sets of output lines. One set comprising lines **79.08**(B), **79.09**(B), **79.04**(A) and **79.05**(A) go by cable to Inter Register Check Routing, FIG. 2*z* (FIGS. 63*a*, *b* and *c*); another set comprising lines **79.07**(B) and **79.03**(A) go by cable to positions B and A respectively, of the Result Register of FIG. 2*aaa* (FIGS. 89*a* and *b*); and the third set of lines **79.06**(B) and **79.02**(A) go to the zone positions of the C Bit Generator of FIG. 2*bbb* (FIG. 90). The C Bit Generator also has inputs (not previously mentioned) **58.01**(C) from CR 1 Right Plate Out, FIG. 2*k* (FIG. 58), and **48.03**(C) from CR 2, FIG. 2*kk* (FIG. 48). Output line **90.01**(C) from C Bit Generator is connected to the C position of the Result Register, FIG. 2*aaa* (FIGS. 89*a* and *b*).

The Result Register of FIG. 2*aaa* has four sets of input lines. Two previously described are from the Decimal Correction Circuits and the Zone Adder of FIG. 2*ccc*. The third set comprising lines **22***b*.**14**(C), **22***b*.**13**(B), **22***b*.**12**(A), **22***b*.**11**(8), **22***b*.**10**(4), **22***b*.**09**(2) and **22***b*.**08**(1) is connected by cable from the Keyboard of FIG. 2*v*. The fourth set is from the Memory Test Controls, FIG. 2*zz*, and consists of lines **92.01** through **92.07**.

The Result Register of FIG. 2*aaa* provides output lines **89***b*.**11**(C), **89***b*.**07**(B), **89***b*.**08**($\overline{B}$), **89***b*.**03**(A), **89***b*.**04**($\overline{A}$), **89***a*.**15**(8), **89***a*.**16**($\overline{8}$), **89***a*.**11**(4), **89***a*.**12**($\overline{4}$), **89***a*.**07**(2), **89***a*.**08**($\overline{2}$), **89***a*.**03**(1) and **89***a*.**04**(1) to the Result Register Code Check, FIG. 2*zz* (FIG. 91). Another set of output lines **89***a*.**09**($\overline{C}$), **89***a*.**05**($\overline{B}$), **89***b*.**01**($\overline{A}$), **89***a*.**13**($\overline{8}$), **89***a*.**09**($\overline{4}$), **89***a*.**05**($\overline{2}$) and **89***a*.**01**($\overline{1}$) are directed by cable to Memory Input Switch, FIG. 2*b* (FIG. 11). Finally a set of output lines **89***b*.**10**($\overline{C}$), **89***b*.**06**($\overline{B}$), **89***b*.**02**($\overline{A}$), **89***a*.**14**($\overline{8}$), **89***a*.**10**($\overline{4}$), **89***a*.**06**($\overline{2}$) and **89***a*.**02**($\overline{1}$) are furnished by cable to Storage In Select Circuits of FIG. 2*uu* (FIG. 43).

The Memory Test Controls of FIG. 2*zz*, shown in detail in FIG. 92, are used to place a character manually into the Result Register for entry into Memory.

As mentioned previously, a stored program is a series of coded operational steps referred to as instructions, arranged in a particular sequence and stored in Core Memory. This program is obtained from Memory, instruction by instruction, and each instruction is interpreted and executed in turn.

As shown in FIG. 2*bx*, an instruction comprises five characters and is divided into two parts, the Operations part and the Address part. The Operations part is a single character (Character 0) designating the operation to be performed. The Address part is divided into two portions. The first, comprising numeric portions of Characters 1 through 4, B and A Zone bits of Character 1, and the B Zone bit of Character 4, specifies the location of data in the Core Memory which is to be operated upon in accordance with the Operation part. The A bit of Character 1 is given a value of 10,000; the B bit of Character 1 is given a value of 20,000; and the B bit of Character 4 is given a value of 40,000. The second portion of the Address part is the Storage Address part located in the Zone portion of Characters 2 and 3, and designates the address in Core Storage to be used during the execution of the instruction. For some instructions, the presence of bits in the Storage Address portion indicates a special instruction or an address not associated with Storage, but for the present, such modifications will not be explained in detail.

The following chart shows the instructions which are performed by the Data Processing System. The Mnemonic codes are merely the shorthand designations of the instructions and it is the operations part which is

contained in Character 0 of the instruction. The From and To columns refer to the movement of data when appropriate and the Remarks and Limiting Factor briefly expand on the instruction title. When necessary to the description of the invention, details of the instructions are given.

Chart II

Instruction	Mnemonic Code	Oper. Part	From	To	Remarks	Limiting Factor
Add	ADD	G	Mem	Acc./AS	Result in accumulator or Aux. Stor	Non-num. char, in mem. or Storage Mark in Storage, whichever is last.
Add Mem	ADM	6	Acc./AS	Mem	Signed Mem. field-algebraic addition Unsigned Mem. field—non-algebraic and zone addition.	Non-num. char. in mem. Acc/Aux. Stor. mark.
Add Address Mem.	AAM	@	Acc./AS	Mem	Add 5 digits in Acc/AS to the Mem. field interpreted as addr. part of an instruc.	5 characters in Acc/AS; 4 char. in Memory.
Blank Memory	BLM	$		Mem	Puts Blank characters in Mem	Address of Instruction.
Compare	CMP	4			Accumulator or aux. stor. with Memory	Acc./Aux. Stor. mark.
Ctrl 0000	IOF	3			Turn off input-output indicator	
Ctrl 0001	WTM	3			Record tape mark	
Ctrl 0002	RWD	3			Rewind tape unit	
Ctrl 0003	ION	3			Turn ON input-output indicator	
Ctrl 0004	BSP	3			Back space tape one record	
Ctrl 0005	SUP	3			Prevent printing or punching one cycle	
Divide	DIV	W			Dividend in acc. 00; divisor in Mem. Quotient in Acc. 00.	Non-num. char. in Mem. and Stor. Mark in Acc. 00.
Lengthen	LNG	D			Add zeros to right (Acc. 00)	Address of Instruction.
Load	LOD	8	Mem	Acc./AS	Loads zones as well as numbers	Acc./Aux. Stor. Mark.
Load Address	LDA	#	Mem	Acc./AS	Loads Address porton of an Instruction as a five-digit field in Acc./AS.	4 char. of Mem.
Multiply	MPY	V			Multiplier Acc. 00; multiplicand mem; product Acc. 00.	Non-num char in Mem and Stor. Mark in Storage.
No Oper	NOP	A			No operation	
Norm Tr	NTR	X			Left-hand zero in accum. or aux. stor. causes transfer. Zero deleted except last zero.	
Read	RD	Y	Input	Mem	From tape to Mem From card reader to Mem From drum to Mem. (Etc.)	¾" inter-record gap. Record Storage mark. Drum mark (By input device).
Read-Write	RWW	S			Alert reading tape unit to operate simultaneously with next write instruct.	
Receive	RCV	U			Sets MAC 2 to Addr. of Instruction	
R Add	RAD	H	Mem	Acc./AS	Resets accum. or aux. stor.; adds from Mem	Non-num. char. in Mem.
R Sub	RSU	Q	Mem	Acc./AS	Resets accum or aux. stor.; Substracts Mem. field from a zero in Acc./AS.	Non-num. char. in Mem.
Round	RND	E			Drop positions from right and ½ adjust (accum. 00) Zero balance is plus.	Address of Instr.
Send	SND	1	Mem	Mem	Use with RCV for transmitting data 5 char. at a time from Mem. to Mem. If RWW tgr. is off. If RWW tgr. is on, perform redundancy chk of Mem., beginning with instruct. addr.	If RWW Tgr. off Stor. Mark in Aux. If RWW Tgr. on End of Mem.
Select	SEL	2			Select Input unit, Output unit, Alter Sw, or check indicator.	
Set Bit	SB	%			Transfer a zero or one bit to the char. addressed into a bit position (B, A, 8, 4, 2, 1) determined by Storage Address.	
Set Left	SET	B		Acc./AS	Place storage mark to left of field in indicated storage addr. (00-15). Insert zeros if Instr. Addr. is greater than field length in Acc./AS.	Address of Instruction
Shorten	SHR	C			Drop positions from right (Acc. 00). Zero balance is plus.	Address of Instruction.
Sign	SGN	T	Mem	Acc./AS	Remove zone 11, 10 or 01 from Mem., place & or minus sign in Accum. or Aux. Stor.	
Stop	HLT	J			Stop machine	
Store	ST	F	Acc./AS	Mem	Store num. field in Mem	Acc./Aux. Stor. mark.
St Print	SPR	5	Acc./AS	Mem.	Store field for printing. Skips decimals, prints commas. Removes left-hand zeros and commas	Acc./Aux. Stor. mark.
Subtract	SUB	P	Mem	Acc./AS	Subtract in Mem. field from Stor. field. Result in acc. or aux. storage	Non-num. char. in Mem. or Stor. mark in Acc./AS., whichever is last.
Transfer	TR	1			Unconditional transfer	

Chart II—Continued

Instruction	Mnemonic Code	Oper. Part	From	To	Remarks	Limiting Factor
Tr Any	TRA	1			Trans. if condition or line specified by ASU code (00-06) is up.	
Tr Equal	TRE	L			Transfer if Equal Tgr. is ON	
Tr High	TRH	K			Transfer if High Tgr. is ON	
Tr Plus	TRP	M			Transfer if designated Acc. or Aux Stor. sign is plus	
Tr Signal	TRS	O			Transfer if selected I 10 indicator ON (ASU 00) or line indicated by ASU Coding is ON (ASU 01-15).	
Tr Zero	TRZ	N			Transfer if designaated Digit Zero Tgr. is ON	
Tr on Zero Bit	TZB	.			Tests the Bit specified by ASU coding in the char. at the MAC 2 address.	
Transmit	TMT	9	Mem	Mem	Use with RCV for Transmitting data from Mem. to Mem. Code 00; 5 char. group transmission Code 01-15; single char. transmission.	R/M in Mem. pos. ending in 4 or 9 or Aux. stor. mark.
Unload	UNL	7	Acc./AS	Mem	Unload zones and numbers	Acc./Aux. Stor. mark.
Unload Address	ULA	*	Acc./AS	Mem	Unload a 5 digit field from Acc./AS. into the Addrs. portion of designated instr. in Mem.	
Write 00	WR	R	Mem	Output	From Mem. to tape From Mem. to card punch or printer From Mem. to drum (Etc)	Group mark. Group mark. Group mark. (Group mark.)
Write 01	WR	R	Mem	Output	From Mem. to card, printer, tape, drum	20,000th Mem. pos.
Wr Erase 00	WRE	Z	Mem	Output	Replace each char. in Mem. with blank To tape To card punch or printer To drum (Etc)	 Group mark. Group mark. Group mark. (Group mark.)
Write Erase 01	WRE	Z			Same as above	Limited by end of 20,000 Mem. block.

As mentioned previously, the first address portion of the instruction may refer to any location in a number of storage devices such as Memory or to Input-Output devices. Adresses of such units are given below.

Chart III

Memory	0000-39,999 or 0000-79,999
Card Readers	0100-0199
Tape Units	0200-0299
Card Punches	0300-0399
Printers	0400-0499
Typewriter	0500
Tape Record Coordinator Tape Units	0600
Drum Sections	1000-9999
Alteration Switches	0911-0919
Instruction Check Indicator	0900
Machine Check Indicator	0901
Read-Write Check Indicator	0902
Printer-Punch Check Indicator	0903
Overflow Check Indicator	0904
Sign Check Indicator	0905

Referring to the composite of FIGS. 2*a* through 2*hhh*, information is read out of Memory, FIG. 2*b*, into Memory Buffer Register, FIGS. 2*c* through 2*e*. Then one of the characters of the Memory Buffer Register is selected by means of Memory Out Switches, FIG. 2*g*, and placed in placed in Character Register 1, FIG. 2*h*. At the same time, information may be read out of Storage, FIG. 2*uu*, into the Storage Buffer Register, FIG. 2*vv*, and then into Character Register 2, FIG. 2*kk*. Character Register 1, FIG. 2*h*, has associated therewith, Character Register 1 Recognition Circuits, FIG. 2*o*, for recognizing the presence of certain characters or classes of characters in CR 1. Furthermore, a check for accuracy of information transfer is made each time a character is entered in the Character Register 1 by CR 1 Code Check, FIG. 2*o*. In like manner, Character Register 2, FIG. 2*kk*, has associated therewith, CR 2 Recognition Circuits, FIG. 2*oo*, and CR 2 Code Check Circuits, FIG. 2*pp*. The coding of each character read into the Character Registers requires an even number of binary "ones" in the seven bits of the character and the C bit is always selected so as to provide (for correct operation) this even number of binary "ones" in a character. The Adder Input Switching, FIG. 2*qq*, is effective to gate the numeric portion of the character in Character Register 1, FIG. 2*h*, or the character in Character Register 2, FIG. 2*kk*, by way of True Complement Controls, FIG. 2*fff*, to the Digits Adder, FIG. 2*eee*; to gate the numeric portion of a character in Character Register 1, directly, to the Multiple Selection Circuits of FIGS. 2*rr* and 2*ss*, and indirectly, to the Multiple Selection Circuits of FIGS. 2*rr* and 2*ss*, by way of the Multiplicand Doubler and Quadrupler, FIG. 2*dd*, and the Quintupler, FIG. 2*cc*. The Multiplicand Doubler and Quadrupler and the Quintupler, shown in detail in FIGS. 80 and 81, respectively, are effective to double, quadruple and quintuple values of the input numbers, and thus the Multiple Selection Circuits, FIGS. 2*rr* and 2*ss*, receive inputs of 1, 2, 4 and 5 times the numeric value of the character, in Character Register 1. The Multiple Selection Circuits under control of Select 1, 2, 4 and 5 multiples from the Multiplier Register and Decoding, FIG. 2*hhh*, provide the proper multiples to the Multiple Adder, FIG. 2*hhh*, during a Multiply operation. However, for most operations the one's multiple is gated. The sum output of the Multiple Adder, FIG. 2*hhh*, being the sum of binary coded decimal numbers, may require correction which is provided by the Decimal Correction Circuits, FIG. 2*ggg*, whose outputs (2, 4 and 8), in turn, are emitted to the Digit Adder, FIG. 2*eee*. The one bit (1) from the Multiple Adder, FIG. 2*hhh*, is not altered by decimal correction and so proceeds directly to the Digit Adder, FIG. 2*eee*. The Digit Adder combines the value received via the True Complement Controls, FIG. 2*fff*; the Multiple Adder Correction Circuits, FIG. 2*ggg*, and the Multiple Adder, FIG. 2*hhh*, to provide a binary coded decimal sum. This sum may also require correction, the correction being provided by the Decimal Correction Circuits for Digit Adder, FIG. 2*ccc*. The output of the Decimal Correction Circuits, Digit Adder, FIG. 2*ccc*, which is the corrected sum, is emitted to the Result Register, FIG. 2*aaa*, to the C Bit Generator, FIG. 2*bbb*, and the Inter-Register Check Routing Circuits, FIG. 2*z*.

While addition or multiplication of the numeric portion of the character is accomplished in the circuits just described, the zone bits, A and B, may also be added. The Zone Adder, FIG. 2*ccc*, receives the A and B bits of CR 1 via Adder Input Switching, FIG. 2*qq*, and the A and B bits of CR 2 by way of CR 2 to T/C Controls, FIG. 2*fff*. The C Bit Generator, FIG. 2*bbb*, serves to generate a new check bit (C) for the corrected character, and sends it to the Result Register, FIG. 2*aaa*. The decimally corrected and redundantly correct sum output from the Digit Adder, and Zone Adder, now in the Result Register, may be gated to Memory or Storage from the Result Register.

The Memory Array of FIG. 2*b* comprises 280 thousand ferrite cores in which information is magnetically stored according to the state of each individual core. Writing a "1" into a core stores flux of one polarity, while reading a "1" from a core reverses the flux and resets the core to "0." The selection of polarities corresponding to the bistable states is, of course, entirely arbitrary. The Memory Array comprises thirty-five core planes, each plane consisting of an 80×1000 rectangular Matrix, which acts as a single block of storage having addresses numbered continuously from 00000 to 39,999, where each address corresponds to a particular 7-bit character. Groups of five characters (35 bits in all) are read simultaneously from the 35 core planes. For example, five characters located at the beginning of Memory would have addresses 00000 through 00004, but all five characters would be read from Memory simultaneously, regardless of whether the given address was 0000, 00001, 00002, 00003, or 00004. Any one of the characters of a group may be selected from the Memory Buffer Register by Memory Out, FIG. 2*g*. This is accomplished as follows: If address 00000 is given, five characters are brought from addresses 00000 through 00004 of Core Memory and placed in the Memory Buffer Register. However, since address 00000 was given, only character 0 is selected from the MBR by Memory Out, FIG. 2*g*.

During the Read and Write portions of an Instruction or Execution Character cycle, the Memory Decoders, FIG. 2*a*, receive an address by way of the Memory Address Select Circuits, FIGS. 2*ww* through 2*yy*, the latter receiving the address from either MAC 1, FIG. 2*gg*, or MAC 2, FIG. 2*hh*. Either Memory Address Counter, MAC 1 or MAC 2, may contain any of the addresses 00000 through 39,999; however, the units orders of MASR always contain a 4 or a 9 for an Instruction since five characters, the last having an address ending in 4 or 9, are required from Core Memory to be placed in the MBR and transferred in parallel to the Instruction Register and the Memory Address Register.

Referring now to FIG. 2*uu*, the Core Storage Array comprises seven planes, each plane arranged in a 16×32 matrix for the storage of 512 bits, the seven planes storing 512 characters. The addresses, then, for each character in Core Storage are 0 to 511. Individual characters are read out of Core Storage at addresses specified by means of the Storage Address Select Register and the SSR Decoding, FIG. 2*ee*, which provide outputs to the Accumulator Decoders of FIG. 2*tt* (FIGS. 34*a* through *d*). The Storage Address Select Register receives addresses from the Storage Address Counter, FIG. 2*ff*, the latter having inputs from both the Storage Select Register, FIG. 2*p*, and the Starting Point Counter, FIG. 2*q*. The Starting Point Counter keeps track of the address of the word stored in Accumulator Storage, that is, the address of the least significant digit portion. It is unnecessary that the Starting Point Counter be reset to 0 or to any particular address whenever the machine is turned on, since the 256 addresses of Accumulator Storage provide a closed loop. It will be noted in FIG. 2*ff* that the Starting Point Counter provides inputs to the Storage Address Counter positions 1, 2, 4, 8, 16, 32, 64, 128 whereas the Storage Select Register provides inputs to positions 16, 32, 64 and 128 only. The upper limit of the word stored in the Core Storage is noted and recognized by a special character called the Storage Mark. The only function of the Starting Point Counter then is to determine the starting address of the Accumulator Storage. The Starting Point Counter can count 000 through 255 and can be stepped either +1, −1 or +128. When the Counter passes 255, it starts off again at 0. The contents of addresses in the Core Storage less than 256 are obtained by using the Storage Select Register outputs to positions 16, 32, 64 and 128 of the Storage Address Counter and resetting the 1, 2, 4, 8 triggers to "zero". It should now be apparent that Core Storage is logically divided into two portions, each having 256 characters, one portion being referred to as the Accumulator Storage and the other as Auxiliary Storage. Auxiliary Storage has addresses 0 through 255 and Accumulator Storage has addresses 256 through 511. The Storage Select Register is set from either the Memory Buffer Register or from the Console, and two lines of the Storage Select Register Decoding, FIG. 2*ee*, go directly to the Storage Decoders, FIG. 2*tt*, which perform the function of determining whether Auxiliary Storage or the Accumulator Storage is selected. Two lines, **52.24** and **52.41**, from Storage Select Register Decoding, FIG. 2*ee*, to the Storage Decoders, FIG. 2*tt*, indicate whether a position equal to or above 256 or a position lower than 256 is addressed. The 1, 2, 4, and 8 bits of the Storage Select Register are transferred via cable to the 16, 32, 64, and 128 positions, respectively, of the SAC. If the Storage Select Register is not 0, in this case, the 8, 4, 2, 1 bits of SAC are set to 0. In this way the SAC is set to the Storage Unit numbers shown in the Storage Select Register. This fixed Storage Address is 16 for Auxiliary Storage Unit 01, Address 32 for Auxiliary Storage Unit 2, etc. up to Storage Address 240 for Auxiliary Storage Unit 15. The Storage Select Register determines two things: (1) whether the Storage Address Select Circuits will be set to either the upper or lower half of Core Storage, and (2) whether the Storage Address Counter will be set to the starting point Counter or to the Fixed Storage Address corresponding to the Auxiliary Storage Unit indicated in the Storage Select Register. The Starting Point is simply an address in storage. When any of the Auxiliary Storage units are used the Starting Point is a fixed Address, but when the Accumulator is selected, the Starting Point may be any address of the upper 256 positions of storage. After the Starting Point Counter has determined the Starting Address of the Accumulator its only other function is to remember the location of the Starting Point in the Accumulator for reference purposes, and to change this starting point while executing certain instructions such as Divide, Multiply, Lengthen, Shorten, etc.

ROUTING LINES

As described, with reference to FIG. 2, there are two classes of lines, namely, Data and Control. Data lines are shown entering the blocks of FIG. 2 at the top and leaving at the bottom. Control lines, which cause the Storage or the Transfer of data, are shown entering the blocks at the left. There are two classes of Control lines, namely, Routing lines and Timing lines. The signals on Routing lines are derived generally from the decoding of the Operations part of an Instruction and are further modified, during Execute cycles, to cause a movement of data to be operated upon according to the Instruction. The Timing lines are combined with the Routing lines to determine when the Routing lines shall be effective to cause the transfer or the storage of data. There are a number of basic Routing lines having signals, which are prerequisites for the execution of Instructions in the Data Processing System and other Routing lines either modify operations of the basic Routing lines or control modes of operation. In all figures following FIG. 2, the digits

after the dash to the right of output line numbers indicate the figure to which the line goes.

BASIC ROUTING LINES

In FIG. 93*a*, Read Memory lines **93***a*.**03** through **93***a*.**07** condition circuits for reading five characters out of Core Memory where addresses are determined by MASR. Read Memory (ALU) line **93***a*.**03** is used in combination with timing lines to set CR 1 to the contents of one of the character positions of MBR. Read Memory line **93***a*.**04** is used for PCT Request Execution Controls. Read Memory 1 line **93***a*.**05** goes to Memory Read Gate of FIG. 5*e* to bring up Memory X Read Gate line **5***e*.**02** and Memory Y Read Gate line **5***e*.**05** to Memory Gate Powering of FIG. 5*g*. The signal on Read Memory 1 line **5***e*.**09**, derived from line **93***a*.**05**, goes to Memory Sample Pulse Generator, FIG. 20*e*, to control the MBR Sample pulse on the lines **20***e*.**01** and **20***e*.**02**. The lines just mentioned are up during Use time as determined by the Use line **105**.**14**.

In FIG. 93*a*, Read Storage Routing controls both the reading out of Storage and the writing into Storage. When a Read Storage signal is provided, one character is read out of Storage and normally one character is written back into Storage. Read Storage line **93***a*.**01** conditions circuits for setting CR 2 to the contents of SBR. Read Storage line **93***a*.**02** conditions circuits found in FIG. 7*d* to provide Storage Read Bias Gate signals on lines **7***d*.**01** and **7***d*.**02** to FIGS. 42 and 36*b*, respectively, Storage Read Gate signals on lines **7***d*.**03** and **7***d*.**04** to FIGS. 37 and 42, respectively, Storage Inhibit Gate signals on line **7***d*.**05** to FIG. 44, and Storage Write Gate signals on lines **7***d*.**06**, **7***d*.**07** and **7***d*.**08** (one line) to FIGS. 38*b* and *c*.

In FIG. 93*b*, CR 1 to Adder (P) line **93***b*.**01** conditions circuits found in Character Registers to Adder Routing of FIG. 73 to route the numeric outputs of CR 1 to the first Doubler, FIG. 80, to the Quintupler, FIG. 81, and the Select One Multiple, FIG. 82, and to route the Zone outputs of CR 1 to the Zone Adder of FIG. 79. CR 1 C Bit Out line **93***b*.**02** goes to the C Bit Generator, FIG. 90, where it gates Result C line **90**.**01** to the Result Register, FIG. 89*b*, according to the redundancy of the combined zone and numeric portions of the result character. This permits the character in the Result Register to retain its original bit structure during a Load, Store or Transmit by 1 operation wherein the bit structure is not to be altered.

In FIG. 93*b*, CR 1 to T/C line **93***b*.**03** directs the character in CR 1 to the Digit Adder True Complement Circuits of FIG. 83, via the Adder Input Switching, FIG. 73. CR 1 to T/C line **93***b*.**03** is only up during an Add Memory 2 (Signed Field) operation as indicated in Add to Memory Routing Controls, FIG. 68*b*, when the Memory Field is to be recomplemented. As shown in FIG. 73, the line **93***b*.**03** causes the numerical outputs of the character in CR 1 to be transmitted to the complement circuits of the True Complement Controls, FIG. 83, where the Complement line **93***d*.**07** gates the Complement to the Digit Adder of FIG. 86.

In FIG. 93*b*, CR 2 to T/C lines **93***b*.**04** and **93***b*.**05** route the numerical outputs associated with the character in CR 2 to the Digit Adder True Complement circuits and the zones of the character in CR 2 to the Zone Adder True Complement circuits. The C bit is not routed by the CR 2 to T/C signal. In FIG. 73, the line **93***b*.**04** gates the input lines from CR 2 Outputs of FIG. 75, which represent the character in CR 2, to the Digit Adder True Complement circuits of FIG. 83. In the Zone Adder of FIG. 79 (Sheet 1), the line **93***b*.**05** gates the zone portion of the character in CR 2 to the Zone Adder True Complement circuits of that figure (Sheets 1 and 2).

In FIG. 93*b*, CR 2 C Bit Out line **93***b*.**06** causes the C bit from the character in CR 2, if any, to be transferred to the Result Register, thereby permitting the character in the Result Register to retain its original C bit. This line is up only during a Store for Print, Unload, Store or a Read operation where the bit structure of the character in CR 2 is not to be altered. The line **93***b*.**06** goes to the C Bit Generator of FIG. 90 where it gates the CR 2 C line **48**.**03** onto the Result C line **90**.**01** to the Result Register of FIG. 89*b*.

In FIG. 93*c*, Adder Out Routing, a Digit Adder Out line **93***c*.**01** routes the output of the Digit Adder Decimal Correction circuits to both the Result Register and the C Bit Generator. If there is no output from the Digit Adder (absence of 1 bits) this line conditions the Decimal Correction circuits to generate 8 and 2 bits (numerical zero) and send these to the Result Register. The Zone Adder Out line **93***c*.**02** routes the A and B bit lines of the Zone Adder circuits of FIG. 79 (Sheet 1) to the Result Register and the C Bit Generator. The Generate C Bit Out line **93***c*.**03** conditions the C Bit Generator for generating of a check bit to the Result Register when the zone and numeric portions of the character entering the Result Register contain an odd number of bits. This line is shown entering the C Bit Generator, FIG. 90, where it is used to generate a positive signal on the Result C line **90**.**01** when the circuits of the C Bit Generator indicate odd redundancy thereby making the sum of all the bits of the character even.

In FIG. 93*d*, Adder Carry Routing, the Minus (—) on Suppress Adder Carry line **93***d*.**01** prevents the turning On of the decimal carry trigger of FIG. 88 (Sheet 1) to permit special characters to be sent directly through the Digit Adder Decimal Correction circuits, FIG. 87, without correction. On the upper portion of FIG. 88 (Sheet 1) the Minus on Suppress Adder Carry line **93***d*.**01** prevents a carry out resulting from an 8, 4 bit combination, an 8, 2 bit combination, and a Binary Sum 8 Carry. In FIG. 93*d* the Minus on Suppress Zone Carry In line **93***d*.**02** goes to FIG. 88 (Sheet 2) via Sheet 1 of FIG. 88 to suppress setting of the Zone Carry trigger when this line is minus. The Route Decimal Carry In line **93***d*.**05** is up whenever it is necessary to obtain the "tens" complement. This line goes to the Digit Adder, FIG. 86, where it gates a 1 into the "carry in" of the C units position of the Digit Adder.

In FIG. 93*d*, Zone Carry In line **93***d*.**06** is sent to Zone Adder, FIG. 79 (Sheet 1), where it gates a "carry in" to the A bit of the Zone Adder during an Add Memory or Compare operation. In the Add Memory instruction, the Zone Carry In signal is used to add an A bit to the Zone portion of the high order character in Memory for address modification. In the Compare instruction the Zone Carry In signal is used to obtain the "two's" complement from the "one's" complement. The Complement line **93***d*.**07** goes to the True Complement controls, FIG. 83, where it is used to condition the Digit Adder True Complement circuits for complementing the numerical outputs of the character in either CR 1 or CR 2 to effect subtraction by addition in the well known manner.

In FIG. 93*e*, Set Multiple Register to CR 2 line **93***e*.**01** is made positive to put a digit of the multiplier in the Multiple register of FIG. 78 during Multiply 1. As shown in FIG. 78, the numerical outputs of CR 2 are gated to set the Multiple Register triggers. (The Multiple Register is reset to "unity" when the machine is not executing the Multiply instruction.)

Bits can be originated for various reasons and distributed via Adder Emitter lines of FIG. 93*e* and Bit to Adder Routing lines of FIG. 93*f*. The only character emitted is the Blank under control of the lines **93***e*.**04** and **93***e*.**05**. The details of operation of the foregoing lines will not be described except when incidental to the examples of machine operations which illustrate the principles of the invention as later described.

FIG. 93*g* is concerned with routing controls for MAC 1, MAC 2, SAC and SPC. Signals are passed on output lines **93***g*.**01** through **93***g*.**10** to MAC 1, FIGS. 30*a* through *f*, and to Overlap Mode Execution Controls to step MAC 1 plus 1 and minus 1. In FIG. 93*h*, routing lines are

provided to MAC 2, FIGS. 31*a* through *f*, to step MAC 2 minus 1 via line **93***h*.**01**, to step MAC 1 plus 5 via lines **93***h*.**02** and **93***h*.**03**, and to step MAC 2 plus 5 via lines **93***h*.**04** and **93***h*.**05**. In FIG. 93*i*, routing lines are provided to FIG. 52 to step SAC minus 1 via lines **93***i*.**01** and **93***i*.**02**, plus 1 via lines **93***i*.**03** and **93***i*.**04**, and plus 128 via line **93***i*.**05**. In FIG. 93*j*, Storage, Memory and Instruction Counter Routing, output lines provide signals to step the Starting Point Counter plus 1 via lines **93***j*.**01** through **93***j*.**03**, minus 1 via lines **93***j*.**04** through **93***j*.**06**, and plus 128 via line **93***j*.**07**. The line **93***j*.**08** is used in FIG. 52*e* to set SAC to the contents of the Starting Point Counter and the line **93***j*.**09** is used in FIG. 30*f* to set MAC 1 to MAR. Lines **93***j*.**10** and **93***j*.**11** to FIGS. 139*a* and 32*a*, respectively, are positive to reset the Instruction Counter and set the IC to the contents of the Memory Address Register, respectively. The line **93***j*.**12**, Minus (—) on Block Step IC, when positive and in combination with lines **116**.**09**, **123**.**34** and **130***a*.**20** serve in FIG. 32*a* to step the IC plus 5 at R_3 time of Execute Character Cycle 1 of each complete operation period in which a transfer is not effected.

Two additional basic routing lines are Result to Memory and Result to Storage. The former is used in the Memory Input Select Switching of FIG. 10 to control the Input Switch of FIGS. 10*a* and *b*, and the latter is used in the Storage Input Select and Switch Circuits of FIG. 43 to transfer the contents of the Result Register to the Storage Inhibit Drivers of FIG. 44. A detailed discussion of the exact use of these routing lines is given later in the description of Overlap Mode Control Circuits and examples of their operation.

TRIGGER CONVENTION

Triggers are widely used throughout the Data Processing System and are bistable devices considered to be Off when the right side is conducting (right plate down or minus) and considered On when the left side is conducting. When a trigger is On, it indicates a "1"; when the trigger is Off it indicates a "0." If a trigger is Off and the right grid is pulsed by negative shift, the trigger is turned On. Likewise, if the trigger is On and the left grid is pulsed by negative shift, the trigger is turned Off. A negative shift to the left grid of the trigger that is Off causes no change because the pulse is applied to the side that is already Off.

When both grids are suitably coupled together the connection is described as a "Binary Input." A negative input pulse changes the state of the trigger, since the negative shift is effective only on the positive grid thereby causing the trigger to change its state.

ROUTING FOR SETTING CONTROL TRIGGERS

In FIG. 93*k*, routing lines are provided to turn On and Off Auxiliary triggers **1** and **2**. FIG. 93*l* illustrates routing lines for turning On Auxiliary triggers **1** and **2** under different conditions than those of FIG. 93*k*. FIG. 93*l* also shows routing lines to turn On the Storage High trigger, to turn Off the Storage High trigger, to turn Off the Storage High and Low triggers, and turn Off the Remainder trigger. In FIG. 93*m*, routing lines are shown to turn Off the Storage Mark trigger, turn On the Digit Zero trigger, turn Off the Digit Zero trigger, and turn On the Transition trigger used in Overlap Mode Control. FIG. 93*n* illustrates routing lines for turning On and Off the Sign Check trigger, turning On and Off the Overflow Check trigger and setting the Storage Sign plus or minus. In FIG 93*o*, routing lines are shown to turn On and turn Off the Read/Write Check trigger, turn On and turn Off the Record Check trigger and turn On and turn Off the Instruction Check trigger. In FIG. 93*p*, routing lines are shown for Result to Memory, Result to Storage, Check CR 1 to Adder, Check CR 2 to Adder and Not Erase Memory. FIG. 93*q* illustrates Mode Control routing lines comprising Memory Read Mode, Memory Read/Write Mode, Storage Read Mode and Storage Read/Write Mode for Mode Control as previously mentioned. FIG. 93*r* shows End E Time routing lines which indicate the final Execute cycle of an operation. In FIG. 93*s*, MASR Input Switching, routing lines are shown to set MASR to the Instruction Counter, set MASR to MAC 2, set MASR to MAC 1 and set MASR to SMAC. FIG. 93*t* illustrates routing lines for controlling the Input/Output sequence of operations. FIG. 93*u* shows routing lines to turn On the Auto Transition trigger used in Overlap Mode Control, turn On the Machine Check trigger, turn Off the Machine Check trigger, and turn Off any Signal trigger. In FIG. 93*v*, Block Add Trigger, Suppress Code Checking, routing lines are provided for Minus on Block Add trigger, Minus on Suppress Result Register Code Check, Minus on Suppress CR 1 Code Check and Minus on Suppress CR 2 Code Check. FIG. 93*w* illustrates Neon Indicators which are turned On to indicate the type of cycle such as TC 1, TC 2 and so forth, Parallel Character Transfer Data Check, Parallel Character Transfer Address Check and CR 1 and 2 Code Check Odd.

PARALLEL CHARACTER TRANSMISSION CABLE CONNECTOR

In FIG. 94 a diagram of the Parallel Character Transmission cable receptacle is shown. This is the terminal for those cables shown in composite FIG. 2 and in the logical block diagrams for communicating with input/output devices which handle characters five at a time in parallel. Each of the blocks, when used, contains the name of the line and the number of the line, if any.

THE CLOCK

In FIG. 95, the 1 Megacycle Drive Pulse Generator, the circuits consist of a 1 megacycle crystal controlled oscillator, the output of which is taken from the cathode resistor. Feedback is employed to keep the oscillator running which results in positive spikes each microsecond. The voltage range of these spikes is from 0 to 80 volts and the leading edge in its linear region has a rise time of 0.1 microsecond. The output is powered and inverted yielding negative going pulses which are distributed as main drive pulses to all sections of the Clock Ring. The main drive pulses on the output lines **95**.**01** through **95**.**04** have an amplitude of approximately 45 volts from +140 volts to +95 volts.

The drive ring comprises a Clock Read section, FIG. 96, a Clock Add section, FIG. 97, and a Clock Write section, FIG. 98. The Read section of the ring, FIG. 96, provides five sequential pulses R_0, R_1, R_2, R_3 and R_4. Only one trigger in the clock ring should be On at any one time. Assume, for example, that the R_1 trigger of FIG. 96 is On. The right plate will then be up, conditioning its associated diode gates and upon the fall of the next 1 megacycle drive pulse on the line **95**.**01** the R_1 trigger is turned Off and the R_2 trigger is turned On. With the R_2 trigger On the right hand plate conditions its diode gate circuits for the next fall of the 1 megacycle drive pulse which turns Off the R_2 trigger and turns On the R_3 trigger. This operation continues until the R_4 trigger is turned Off, at which time either the W_0 trigger of the Clock Write section of the ring of FIG. 98 is turned On or the A_0 trigger of the Clock Add section of the ring of FIG. 97 is turned On. During an Instruction cycle, which is of 13 microsecond duration as explained previously, the output of the R_4 trigger on the line **96**.**16** conditions the diode gate for the A_0 trigger of FIG. 97 which is further conditioned by the **99**.**01** line which is up during Instruction time. The fall of the 1 megacycle drive pulse on the line **95**.**02** turns the A_0 trigger On. The Clock Add section of the ring then provides A_0, A_1, A_2 and A_3 pulses in sequence. The right hand plate of the A_3 trigger conditions the diode gate associated with the W_0 trigger of the Clock Write section of the ring in FIG. 98 via the line **97**.**08** and upon the fall of the 1 megacycle drive pulse on the line **95**.**03**, the W_0 trigger

is turned On. This and the W_1, W_2 and W_3 triggers in sequence generate W_0, W_1, W_2 and W_3 pulses. Therefore, it is pointed out that on Instruction cycles the Clock Add section of the ring is interposed between the Read and Write portions of the ring for providing a 13 microsecond cycle.

For Execute cycles, the Clock Add section of the ring is not used, and instead, the output of the R_4 trigger on the line **96.17** goes to FIG. 98 where it conditions a diode gate associated with the W_0 trigger. The A_3 (D1) line **97.08** is down, but the Read/Write line **99.02** is up due to the Clock Read/Write and Read/Add/Write switching of FIG. 99. It will be observed in FIG. 99 that when the I time line **124.34** is down the Read/Write line **99.02** is up to condition the diode gate in combination with the R_4 line **96.17** of FIG. 98 so that the fall of the 1 megacycle drive pulse on the line **95.03** turns On the W_0 trigger. After this, the W_1, W_2 and W_3 triggers are turned On in sequence. Then the output from the W_3 trigger is taken from the W_3 (D1) line **98.11** to the Clock Read section of the ring, FIG. 96, where it conditions the R_0 trigger which is turned On next with the 1 megacycle drive pulse. Thus, the Read and Write portions of the ring alternate to provide pulses R_0, R_1, R_2, R_3, R_4, W_0, W_1, W_2, W_3 except during an Instruction cycle when the Add portion of the ring is introduced to prolong the cycle to 13 microseconds. The Clock Reset of the lower portion of FIG. 99 puts the Clock under control of the 1 megacycle drive pulses so that it will operate continuously. When the machine is first turned On the Initial Reset line **106.14** holds the Block R_0 Trigger On Reset line **99.08** down and blocks the pulse that normally turns On the R_0 trigger. At the end of approximately 80 microseconds, the fall of the line **106.14** is used to turn On the Clock Reset trigger which in turn is turned Off by the next one megacycle main drive pulse. This fall is transmitted via line **99.09** to turn On the R_1 trigger of FIG. 96. During the 80 microseconds, the line **99.08** prevents the turning On of the R_0 trigger.

PULSE GENERATORS

Short pulses are described by using index points to designate the time of the leading edge of the wave form and the duration of the pulse to specify the time of fall. For example, if a pulse starts at W_3 and lasts for 2 microseconds, the description would be W_3 (D2). In the case of longer pulses, index points are used corresponding to the leading and trailing edge of the pulse, thereby designating the duration. For example, a pulse starting at R_0 and lasting for 3 microseconds would be described as R_0–R_3. All pulses are considered positive unless otherwise indicated. A negative 1 microsecond W_1 pulse would be described as a Minus (—) W_1 (D1).

The pulses in the Pulse Generators are of four different durations, 0.4, 1, 2 and 3 microseconds. The 0.4 microsecond pulses are developed by using peakers in the Pulse Generator of FIGS. 100 and 101. The 1 microsecond pulses of FIG. 102 are powered Clock pulses, and the 2 and 3 microsecond pulses of FIGS. 102 and 103*a* use the outputs of Clock controlled triggers, that is, a trigger is turned On by the fall of a Clock pulse and turned Off by the fall of another Clock pulse and the output pulse is taken from the right side of the trigger. Some of the pulses are mixed with conditioning lines such as Use and Instruction and are generally further conditioned in the logical circuits by control lines as stated previously. FIG. 103*b* shows powering for certain of the pulses generated in FIG. 103*a*, and, in one instance, a pulse is combined with Use line **105.10**. FIG. 104 illustrates the Pulse Generator for pulses having 3 and 4 microsecond durations, utilizing triggers which are set and reset by Clock pulses. FIG. 105 shows the Use trigger which sets the status of the calculator in Use or Manual. The Use trigger is On when the calculator is in automatic operation, during which it gates pulses necessary to carry out the reading and execution of Instructions in the stored program. When the machine is stopped and operated under control of the Operator's Console, it is in the Manual status, and the Use trigger is Off. However, Manual operations can generate one or more Use cycle to carry out the execution of the Manual operation via the Single Use Cycle trigger of FIG. 105, or else by causing the machine to pass from Manual status to Use status by turning On the Use trigger.

RESET AND START/STOP CONTROLS

In FIG. 106, the Reset keys and associated controls and the Clear Memory key and associated controls are shown. Depressing either of the Reset keys while the machine is in Manual status, turns Off all of the Check Indicators and the Any Signal Indicator and also sets the Instruction Counter to 0004. Depressing the Clear Memory key resets the clock, causes all of the functions ascribed to the Reset key and, in addition, sets all of the Core Storage to Storage Marks (an absence of bits) and sets all of the Core Memory to Blanks (a C and an A bit). The Clear Memory trigger associated with the Clear Memory key of FIG. 106 is shown in FIG. 107 along with the Clear Storage Single Shot. FIG. 108 illustrates the Manual Start/Stop controls. The Start key is used to place the system in Automatic status and when depressed, it turns Off all of the Check Indicators and the Any Indicator. Each of the Stop keys, when depressed, places the system in Manual status at the end of E time of the Instruction which is then being performed. The Single Use cycle key causes one cycle of an operation to be executed for each key depression. FIG. 109 illustrates the Stop controls. Depression of the Machine Stop key places the system in Manual status immediately and does not wait until the end of E time as the Manual Stop key does. The Manual Store key and controls are shown in FIG. 110. The Store key permits the operator to enter characters into Core Memory manual (Characters may not be stored directly in Storage). If the system is in Automatic status when the Store key is depressed, the system goes into Manual status at the end of E time of the Instruction which is then being performed. The Memory Address Selector must be set, then upon depression of a key on the Console Character Keyboard, the character entered in the Character Keyboard is thereby stored in Memory.

FIG. 111 illustrates the Manual Instruction controls to permit the operator to manually instruct the Data Processing System. Depressing the Manual Instruction key causes the machine to enter Manual status at the end of E time of the Instruction which is then being performed. The address of the Instruction, including the Storage unit designation, if any is needed, is then set in the Memory Address Selector Keyboard and in the Storage Selector. The key of the Character Keyboard corresponding to the Instruction to be performed is then depressed and will cause that instruction to be executed.

Manual display controls are illustrated in FIG. 112. The purpose of the Display key and Display Step key is to put the machine in Manual status and to permit the operator to observe the contents of the Core Memory and of the Core Storage units. Memory is shown in the Memory Display of CR 1, the Storage unit selected by Storage Selector keys is shown in Storage Display CR 2 and each time the Display Step key is depressed an adjacent character is displayed.

Memory Test controls are shown in FIG. 113. In FIG. 114 the Half Multiple Step controls are shown for the purpose only of completing circuits within the machine wherein depression of the Half Multiple Step key causes the computer to perform either the I time or E time of an Instruction operation each time the key is depressed. When the key is being continuously depressed, the computer goes into Automatic status for long enough to execute one half of an I or E cycle and then after a delay of about 0.75 second, proceeds to successively execute I

times or E times of the Stored program, but at a rate of about eight per second. Should the key be depressed while the machine is in Automatic status, the machine will be placed in Manual status. The Half Step trigger for use with the Half Multiple Step control, FIG. 114, is shown in FIG. 115. Manual Timer triggers, FIG. 116, the Manual Timer Execution controls, FIG. 117, and the Manual Execution controls, FIG. 118, taken together, provide circuits for the manual operation of the system by the depression of the manually operated keys described above.

Check Indicator switches are shown in FIG. 119 and comprise the Instruction Check switch, Machine Check switch, Overflow Check switch, Sign Check switch, Read/Write Check switch and Record Check switch. The switches are normally kept in the Automatic position and for certain errors in machine operations the Halt line **119.01** and the Auto Block line **119.02** are made positive to place the machine in the Manual status for corrective action.

ALTERATION SWITCHES

In FIG. 120*a* six Alteration switches are shown which are used to vary the sequence of machine operations according to a predetermined plan. They are manually settable and each Alteration switch has a specific address as indicated in Chart III. If a switch is On when interrogated by the program, a transfer is made; if a switch is off, no action takes place, except that the machine proceeds to the next Instruction.

AUDIBLE SIGNAL INDICATION

Referring to FIG. 120*b*, the purpose of the Audible Signal Indication is to attract the attention of the operator to the fact that the machine has stopped its processing because of either a planned condition due to the program or an unplanned condition due to a fault. A pleasant tone sounds whenever the machine shifts from Automatic to the Manual status because of conditions above. The operator may turn Off the tone by the Aubidble Signal Reset key, but the tone will sound on a subsequent stop. The operator can made the device completely inoperative during checking by use of the Audible Signal switch.

FIG. 121 shows the I/E trigger which is used for defining Instruction and Execute times. The IA (Indirect Address trigger) trigger also shown in FIG. 121 is turned On for indirect address instructing. An Instruction with an indirect address can be defined as one in which the address portion does not refer directly to the data to be processed but to a location that contains the address of data to be processed. The address contained in the Instruction is called the Indirect Address and the address to which the latter refers is called the Effective Address. Indirect Addressing is identified by a binary "1" in the A bit position of the Low Order character of the Instruction Address, and the Turn On IAT line **61.07** is up from I time routing controls of FIG. 61 due to coincidence between the Use line **105.09**, the I time line **124.29** and the CR 1 A line **59.27**.

ECC 1 and ECC 2 TRIGGERS

ECC 1 and ECC 2 are types of Execute cycles which define portions of Execute time, as mentioned previously. The first Execute cycle (ECC 1) begins at W_2 time when the I/E trigger changes from I to E and the ECC 1 trigger is turned On. Following ECC 1 is the ECC 2 cycle, after which there occur as many Execute cycles as are necessary to complete the Instruction. FIGS. 123 and 124 show the I/E Timer ouputs which are distributed from FIGS. 61, 121 and 122.

LOAD, UNLOAD AND STORE ROUTING CONTROLS

FIGS. 125*a* through 125*c* disclose the routing lines for Load, Unload and Store Instructions.

The Load instruction permits single characters, any series of characters, or fields to be entered into Storage from Memory. The number of characters or length of the field entered into Storage is determined by the position of the Storage Mark relative to the Starting Point Counter. The address part of the instruction specifies the location of the right-hand character of the field in Memory and the Storage unit to be used. Characters are entered right to left from Memory until the specified Storage space is full.

The Unload instruction is used to place a specified portion of Storage in Memory and the number of characters unloaded into Memory is equal to the number of positions in the Storage unit. The right-hand character of the designated Storage unit is unloaded into the Memory position specified by the address part of the Unload instruction and remaining characters in Storage are entered successively into Memory until a Storage Mark is sensed.

The Store instruction is used to place a specified numeric field of Storage in Memory as illustrated by example previously.

STORE FOR PRINTING

FIGS. 126*a* and *b* illustrate the logical circuits for providing signals on routing lines for carrying out the Store for Print instruction, which is normally used to transfer a numeric field from Storage to Memory where it may be used subsequently for writing by a printer. When the sign of the specified Storage unit is plus, a blank is stored in the Memory location designated by the address part of the Instruction. When the sign of the Storage unit is Minus, a dash is stored in the Memory location designated by the address part of the Instruction. The numeric Storage field is stored in the Memory locations directly to the left of the sign position until a Storage Mark is encountered which sets the left-hand limit of the field stored.

TRANSMIT AND SEND

FIGS. 127*a* and *b* illustrate the circuits for providing routing signals for Transmit and Send instructions. A Transmit instruction is used preceded by a Receive instruction for transferring data fro m one portion of Memory to another.

A Send instruction is similar to the Transmit instruction in that it causes high-speed movement of data from one location in Memory to another in five character groups, but it eliminates the necessity of placing a record mark to stop the transmission since the amount of data transmitted is controlled by the length of a preset Storage unit. More specifically, if the RWW trigger is Off, data are removed, five characters at a time, starting at the address of the Instruction to a receiving location determined by the setting of MAC 2. One group of five characters is moved for each character contained in the Accumulator or designated Auxiliary Storage Unit. If the RWW trigger is On at the time the Send instruction is decoded, a high-speed redundancy check is made on the contents of Memory starting at the address of the Send instruction and continuing through the end of the respective Memory block. Detection of a redundancy error in the specified Memory block turns On the Machine Check Indicator.

BLANK MEMORY

FIG. 128 illustrates the circuits for providing routing signals for the Blank Memory instruction. A Blank Memory instruction is used to erase Memory. A Receive instruction is given which specifies a starting address in Memory and then a Blank Memory instruction is given which specifies the number of five character groups to be erased if high speed erase is indicated by Accumulator coding and the number of characters to be erased if low speed erase is indicated by ASU coding. If the address part of the Blank Memory is Accumulator coded, Memory is erased in five character groups starting at the address contained in MAC 2. The number of five character groups to be erased is specified by the Memory address portion of the Instruction. If the Instruction is coded

ASU 01, single characters are erased at a time, and if ASU coding refers to an ASU other than 01, the machine interprets the ASU coding as 01.

SET LEFT, LENGTHEN AND NORMAL TRANSITION ROUTING CONTROLS

FIGS. 129*a* through 129*d* illustrate circuits for routing signals for Set Left and Lengthen instructions and for Normal Transition operations.

The Set Left instruction adjusts the length of the specified Storage field to the number of characters designated by the address part of the instruction by moving the Storage Mark. The operation starts with the character referred to by the Starting Point Counter and continues to the left of the field, character by character, until the number of Storage positions specified by the address have been examined. When a Storage Mark is detected, it is replaced by a zero and then zeros are placed to the left in all remaining high order positions of the adjusted field. If a Storage Mark is not sensed within the designated field, a Storage Mark is inserted to the left of the high order chtaracter of the field. Therefore, the number of characters in a field may be increased or decreased. The Set Left instruction may precede a Load instruction to adjust a field in Storage to the size of the field to be entered therein.

The Lengthen instruction causes the Starting Point Counter to be shifted right (minus) a number of positions specified by the address part of the Instruction. For each position moved by the SPC, a zero is inserted in the corresponding position of Storage.

SHORTEN RIGHT AND ROUND ROUTING CONTROLS

FIGS. 130*a* through 130*c* illustrate circuits for providing routing signals for Shorten Right and Round instructions.

The Shorten instruction shifts the SPC to the left the number of positions specified by the Memory address portion of the Instruction. Since the field in Accumulator Storage is defined by the position of SPC and the Storage Mark, the movement of SPC left (plus) has the effect of removing characters from the right end of the field.

The Round instruction moves the SPC to the left the number of positions specified by the Memory Address portion of the Instruction. Thus, the field remaining is defined by the Storage Mark and the new position of SPC. A five is added to the adjacent right-hand digit with respect to the SPC, and a resulting Carry is added to the units digit of the field. If a Carry is generated out of the highest order position, the field is extended one position to the left to include the Carry.

READ/WRITE SELECT AND CONTROL ROUTING CONTROLS AND INPUT/OUTPUT CONTROLS

FIGS. 131, 132*a* and 132*b* disclose circuits for providing routing signals for Reading and Writing operations of Input/Output devices. FIG. 133 illustrates the routing lines for Select and Control operations. FIGS. 134*a* through 134*f* disclose I/O Sequence triggers and controls for I/O operations and FIGS. 135*a* and 135*b* illustrate Parallel Charcater Transfer Request and other operations directed to parallel transmission for Input/Output devices.

OVERLAP CONTROL

FIG. 136*a* illustrates the Overlap Control triggers, namely, the Transition trigger, Auto Transition trigger, Add trigger and Mode Control trigger; FIG. 136*b* shows additional controls for the Execution of Overlap operations; FIG. 136*c* is Transition Powering for the Transition line; FIG. 136*d* is Powering for the Not Transition line and the Add Trigger; and FIG. 136*e* shows Powering for Transition trigger and the Mode Control Trigger. These triggers just recited are those which control the Overlap Modes of operation. Briefly, the Transition triggers define certain cycles during which complete overlapping of Memory and/or Storage operations and Arithmetic operations is not performed; the Add trigger defines the portion of Execute time when computation may be performed in the ALU; and the Mode Control trigger defines Overlap and Transition cycles where results are placed in Memory or Storage.

RESULT TO MEMORY AND RESULT TO STORAGE TRIGGERS

As mentioned previously when the Result to Memory and Result to Storage Routing lines were discussed, FIG. 137 shows the triggers which are set by positive pulses to Provide the Routing signals on the lines **137.01** through **137.06**.

SPECIAL CONTROL TRIGGERS

FIG. 138*a* illustrates the Storage Low trigger and the Storage High trigger; FIG. 138*b* the Simultaneous Read/Write trigger and the Read Call trigger for I/O operations; FIG. 138*c* the Storage Mark trigger and the MAC 1=0 trigger; FIG. 138*d* the Any Signal trigger and Powering the Storage Mark trigger Off line; FIG. 138*e* the Write Call trigger, No Write Response trigger and the No Read Response trigger for I/O operations; FIG. 138*f* the Instruction Check trigger, Machine Check trigger, Read/Write Check trigger for storing indications of error conditions; FIG. 138*g* the Record Check trigger, Overflow Check trigger, the Sign Check trigger for storing indications of error conditions; FIG. 138*h* the Digit Zero trigger (DZT) and the Remainder trigger; FIG. 138*i* the Auxiliary Trigger 1; FIG. 138*j* the Auxiliary 1 Off Powering; FIG. 138*l* the Auxiliary Trigger 2 Off Powering and FIG. 138*k* the Auxiliary Trigger 2.

RESETS AND CLAMPS

FIG. 139*a* shows circuits for providing reset signals for various triggers either to establish a specific status when power is first applied, to reset to a specific status intentionally via Manual Reset Keys of FIG. 106 or to reset the triggers automatically in preparation for subsequent operations when new information may be set in the triggers. To prevent delay in changing the state of a trigger, the grids of the tubes are clamped to minus 12 volts. For those tubes without electronic reset, the grids of the tubes are clamped at minus 12 volts via a diode having its plate connected to a −12 volt supply and its cathode connected to the grid of the tube. The point for electronic reset is usually the plate of a diode, similarly connected as above, which is fed by a Reset Cathode Follower (KR) having an output of −12 volts for an input of −30 volts thereby clamping the grid at −12 volts. When the input to the KR changes to +10 volts, its output goes to 0 volts and forces a non-conducting grid up via the interconnecting diode. The notation for reset is placed in the title section of the trigger logic block; for example, in FIG. 17*a*, the W of TBW indicates a "W" reset Off. In instances where a trigger is reset On, the reset indicator appears to the left, for example WTB. Reset pulses may be applied, of course, to other portions of a trigger in manners well known in the art.

Instruction reset, those occurring during Instruction time at R_0, are provided on the lines **139***a*.**01** and **139***a*.**03**. The MAR Reset signal on the line **139***a*.**01** resets MAR to zero in preparation for its receiving the Memory Address portion of the Instruction obtained from Memory during the Read portion of the Instruction cycle. The Instruction Reset line **139***a*.**03** goes to FIG. 139*b* where it is powered by cathode followers and distributed as (X) resets to the Storage Select Register, FIG. 16*a*, on the line **139***b*.**01**; the Operation Register, FIGS. 21*a* and *b*, on lines **139***b*.**02** and **139***b*.**03**; the triggers of FIGS. 139*b* through *k* on the lines **139***b*.**04** through **139***b*.**09**; the Reset Add, Reset Subtract, Add-Subtract Routing Controls of FIG. 74*a* on the line **139***b*.**10**; the Multiple Routing Controls of FIG. 67*a* on the line **139***b*.**11**; the Select and

Control Routing Controls of FIG. 133 on the line **139***b*.**12**; the I/O Controls of FIGS. 134*a*, *d* and *e*, on the lines **139***b*.**13** through **139***b*.**15**; the Quintupler, Doubler and Quadrupler, and Multiple Register of FIGS. 81, 80 and 78 on the lines **139***b*.**16** through **139***b*.**18** respectively; the Decimal Correction Circuits of FIG. 85 on the line **139***b*.**19**; the Overlap Control triggers of FIG. 136*a* on the line **139***b*.**20**; the Decimal Carry and Zone Carry triggers of FIG. 88 (2 sheets) on the line **139***b*.**21**; the Inter-Reg Check trigger of FIG. 63*c* on the line **139***b*.**22**; the Unload Address Controls of FIGS. 65*a* and *b* on the lines **139***b*.**23** and **139***b*.**24**; and the Add to Memory Routing Controls of FIG. 68*a* on the line **139***b*.**25**.

Machine Reset line **139***a*.**02** of FIG. 139*a* goes to FIG. 139*b* for powering and distribution on the lines **139***b*.**26** through **139***b*.**35**. In FIG. 139*a*, Instruction Counter Reset, Select Register Reset, and MAC 2 Reset signals are provided on the lines **139***a*.**04** through **139***a*.**06** to powering and distribution of FIG. 139*c*. To reset the Memory Buffer Register in preparation for receiving five characters from Memory, the line **139***a*.**07** is positive during Use time or PCT Request for the Not Erase Memory condition and is combined in FIG. 5*g* with a W_3 (D2) pulse on the line **7***d*.**10** to provide signals on the lines **5***g*.**13** and **5***g*.**14**, the latter being connected to MBR triggers of FIGS. 14*a* and *b* as (Z) resets.

In FIG. 139*c*, the lines **139***c*.**01** and **139***c*.**02** are positive at W_3 (D2) during Use time to provide (R) resets to the Result Register at W_3 time after its contents are no longer required for use. The Intial Reset line **139***c*.**13**, originating in Manual Reset Keys of FIG. 106, provides (U) reset to the Single Cycle Use trigger of FIG. 105. Other signals on input lines from FIG. 139*a* are merely powered and distributed to MAC 2, IC, Select Register and MAR.

FIGS. 139*d* and *e* disclose −12 volt supplies as mentioned previously for use in clamping the grids of triggers. Inputs (not shown) are from the power supply for the Data Processing System.

COMPARE ROUTING

FIGS. 140*a* through 140*c* illustrate the Routing lines for the Compare Instruction, which compares a specified Storage field with a Memory field designated by the Memory Address portion of the Instruction. The comparison begins with the units order of each data group and proceeds from right to left, character by character, until a Storage Mark is sensed. The results of comparison are made available to program interrogation (Transfer instructions) by means of High and Low triggers, FIG. 138*a*, which may be turned On for high or low comparison depending on whether the contents of Storage are higher or lower than the specified contents of Memory. In addition, any unequal condition turns On Auxiliary 1 trigger of FIG. 138*i*. If at the end of execution of the Compare instruction only one of the triggers is On or if both the High and Low triggers are On, the Machine Check trigger of FIG. 138*f* is turned On. High and Low triggers are changed only by execution of a subsequent comparison in the program and are not changed by interrogation.

MISCELLANEOUS

FIG. 141 discloses the circuits for the Auto Load control.

The Auto Load key, FIG. 141, when depressed, causes the following sequence of operations: Selects the Input/Output unit addressed by the keys of the Memory Address Selector, resets the registers and counters including the Check indicators, and sets the IC to 00004, reads one record into Memory starting at position 00000, and initiates Automatic operations whereby the stored program is introduced into Memory.

FIG. 142*a* illustrates circuits for the Reference Voltage Regulator and the D.C. Alarm. FIG. 143 discloses Open Filament Detection circuits for giving an indication of an open filament in the machine.

SETTING OF COUNTERS AND REGISTERS

Two general circuit schemes are used to accomplish the setting and resetting of counters and registers as follows: (1) an electronic reset is employed and one input line for each trigger is used for application of the setting pulse in response to a binary value as in the Memory Buffer Register of FIG. 14*a*, (2) the register is not reset in the manner above but instead two inputs to each trigger are employed. As an example of (2), the Character Register 1, FIG. 57, is turned On with a positive pulse to the left hand grid and is turned Off with a positive pulse at the right hand grid in response to the binary input indication. Therefore, means to rset all triggers to the Off condition before setting is not required since those triggers which are On and should be set On are unchanged, while those On which should be Off are turned Off and those triggers which are Off and should be On are set On.

An example of electronic reset as in (1) mentioned above is found in the circuits of FIG. 17*a* where a −12 volt clamp voltage is applied to the right-hand grid of one of the tubes of a trigger as indicated by "W." The clamp voltage is changed to 0 volts at reset time and the right side of the trigger goes into conduction indicating the Off condition of the trigger.

COUNTERS (GENERAL DISCUSSION)

Two types of counters are used in the Data Processing System. One type is of a modified binary arrangement in which four triggers are arranged to represent the decimal values of 0 through 9 with outputs of 8, 4, 2 and 1 as shown in the first order of MAC 1 in FIG. 30*a*. Storage Address counters comprise eight stage binary counters consisting of eight triggers arranged in tandem to represent 0 through 255, such as the Storage Address Counter of FIGS. 52*a* through *d*.

All the counters except the Instruction Counter of FIG. 32 can step up one count. FIG. 30*a* illustrates a group of four triggers in the modified binary arrangement. Assuming that all triggers are initially Off, one pulse on the MAC 1+1 or +5 line **30***f*.**01** to the 1 trigger would turn the trigger On causing the right plate to rise. The positive shift on the right plate lines **30***a*.**13** and **30***a*.**14** has no effect on the following trigger (2 trigger) because the diode associated with the right plate of the 1 trigger and input of the 2 trigger is conditioned to pass only a negative shift. The next pulse turns the 1 trigger Off causing the right plate to drop and the negative shift turns the 2 trigger On. With the occurrence of the third pulse, the 1 trigger is turned On and the 2 trigger remains On for a count of 3. The fourth negative shift input pulse to the 1 trigger turns Off the 1 trigger, which feeds a negative shift from its plate to the 2 trigger turning it Off. As the 2 trigger goes Off, the fall of its right plate turns On the third trigger (4 trigger). A pure four stage binary counter can count from 0 to 15, but such a counter modified to count only from 0 to 9 must restore to 0 when a count of 9 is reached. To achieve this result the negative level from the left plate of the 8 trigger is arranged to block the input to trigger 2. The ninth input pulse leaves the 1 trigger and the 8 trigger On. The tenth input pulse turns Off trigger 1 and its right plate negative output turns Off trigger 8. The result is then 0.

Counting down requires that the carries from the 1, 2 and 4 triggers be taken from their left plates and the output of the left plate of 8 trigger be coupled to the left grids of the 2 and 4 triggers. Assuming that all triggers are Off, a first input pulse on the Step MAC 1−1 line to the 1 trigger turns it On causing the left plate to drop. The fall of the left plate turns On trigger 2 and then trigger 4 and then trigger 8 are turned On in like manner. Thus, for one instant, all triggers are On and the counter has counted down from 0 to 15. But,

turning On the 8 trigger prevents the counter from staying 15 since the output of the left plate of trigger 8 is coupled to the left grids of triggers 2 and 4. When trigger 8 goes On, its left plate falls generating a negative shift that turns Off triggers 2 and 4. The result, then, is that triggers 1 and 8 are left On and the counter stands at 9. With the trigger standing at 9 (the 8 and the 1 triggers On) a second input pulse turns the 1 trigger Off and the counter stands at 8. The third input pulse turns On the 1 trigger which then causes the 2 trigger to turn On. The turning On of the 2 trigger then causes the 4 trigger to turn On which in turn causes the 8 trigger to turn Off. Accordingly, the counter now stands at 7. The counter continues to count down in the binary fashion.

The step plus 5 signal is introduced into the units position of the counter which must sit at either 4 or 9. Assume that the first order of MAC 1, FIG. 30*a*, is set at 4 (the 4 trigger is On). The Step MAC +5 line **93***h*.**02** conditions a diode gate connected in binary fashion to the 4 trigger and the pulse on line **30***f*.**06** turns Off the 4 trigger. The same pulse turns On the 1 trigger via the diode gate conditioned by the Step MAC 1+1 or +5 line **30***f*.**01** and which is connected in binary fashion to the 1 trigger. The turning Off of the 4 trigger sends a negative shift to the right grid of the 8 trigger turning the latter On. The first order of MAC 1 now stands at a value of 9. A second stepping pulse on lines **30***f*.**01** and **93***h*.**02** turns Off the 1 trigger and turns On the 4 trigger. The turning Off of the 1 trigger sends a negative shift to the left grid of trigger 8 turning Off the latter. The turning Off of the 8 trigger sends a negative carry pulse on the right plate to the second order of the MAC 1 and the first order stands at 4.

MEMORY CONTROLS

The Memory Address Select Register, FIGS. 49*a* through *h*, comprises seventeen triggers which contain the Memory Address that is to be interrogated to obtain five characters from Core Memory. All of the Memory Address Select Register outputs, except the $\overline{40{,}000}$ and the 40,000 lines of the fifth order are decoded in four Decoders of FIGS. 3*a* through *d* for X and Y selection purposes. These are the 4×10 Decoder (thousands order, FIG. 3*a*), the Memory 4×10 Decoder (tens order, FIG. 3*b*), the Memory 4×10 Decoder (hundreds order, FIG. 3*c*), and the Memory 6×8 Decoder (units order, FIG. 3*d*). Only one input from each decoder is up. The first step is to supply Read Bias and to accomplish this the 4×10 Decoder of FIG. 3*b* provides a signal on one of the output lines to its output inverters, FIG. 5*a*, the latter providing complementary outputs on the pair of lines selected to the Switch Core Write Driver circuits of FIGS. 5*b* and *c*. In FIG. 5*a*, it will be noted that only one input line is positive and the remainder are negative. The negative input signals are present on all of the odd numbered output lines except the one associated with the positive input signal, and the negative input signals are inverted by Inverters IJK to provide positive signals on all even numbered output lines (NOT lines) except the one associated with the positive input signal. The 6×8 Decoder, FIG. 3*d*, provides a signal on one of its output lines to its output inverters, FIG. 7*a*, the latter providing complementary outputs to the Switch Core Write Driver circuits of FIGS. 7*b* and *c*. In FIG. 7*a*, the circuits function as explained with reference to FIG. 5*a*. In FIGS. 7*b* and *c* the outputs from the 6×8 Decoder Output Inverters, FIG. 7*a*, are mixed with Memory Read Bias Gate pulses on the lines **5***g*.**11** and **5***g*.**12** to provide an output down signal on one of the lines to the X Switch Core Write Windings of FIG. 9. Signals from the 4×10 Decoder Output Inverters of FIG. 5*a* are mixed with Memory Read Gate Bias pulses on the lines **5***g*.**09** and **5***g*.**18** in the Memory Y Switch Core Write Drivers of FIGS. 5*b* and *c*. A single output line is thereby energized to the Y Switch Core Write Winding of FIG. 8.

To supply Read Bias Current to the X and Y Switch Core Matrices, FIGS. 8 and 9, all write inputs except one to each of the matrices are pulsed with Read Bias current. The next step is to generate Read current and to accomplish this the two 4×10 Decoders, FIGS. 3*a* and *c*, have one of their output lines up in response to signals from the Memory Address Select Register, FIGS. 49*g* and *e*. A signal from the 4×10 Decoder, FIG. 3*a*, and the signal from the 4×10 Decoder, FIG. 3*c*, is present on one of the input lines of the Switch Core Read Drivers, FIGS. 4 and 6, respectively. In FIG. 4, a signal on one of the output lines transfers a signal associated with the address to the Switch Core Read Windings of FIG. 8 when the Memory Y Read Gate line **5***g*.**08** is up. Similarly, a signal on one of the output lines of the Memory X Switch Core Read Drivers of FIG. 6 is transferred to the X Switch Core Read Windings of FIG. 9 when an impulse is provided on Memory X Read Gate line **5***g*.**07**. In FIG. 8, each of the switch cores has three windings, two primary input windings, Read and Write, and a secondary output winding are arranged to be approximately one to one between any of the windings. As an example, consider the switch core at the intersection of the lines **8.10** and **8.11**. The Primary Read winding is represented diagrammatically by the passage of the line **8.11** through the core. The Primary Write line is illustrated diagrammatically by the passage of the **8.10** line through the core. A secondary or output winding is illustrated diagrammatically as the line which bears the address 29,080. Secondary windings feed the Y lines for the Memory Core Array. All switch cores are normally reset and the object of providing inputs to this matrix is to set and reset one of the switch cores using the Read and Write inputs. Since Read and Write windings are connected in series by rows and columns current supplied from an input line magnetizes all cores in its row or column. As stated previously, all of the Write inputs except one are supplied with Read Bias current from the Y Switch Core Write Drivers, FIGS. 5*b* and *c*, whereas only one of the Read lines is energized by the Core Read Drivers of FIG. 3. Since all switch cores are normally reset and Read Bias current tends to reset the cores then the result of the Read operation is to set a core in response to a signal on one of the lines **8.11** through **8.20** in the absence of a signal on one of the lines **8.01** through **8.10**. The Selection process can best be shown by an example which will be given hereafter, but for the present let it be assumed that one of the secondary windings couples the signal caused by a switch core being set to the Core Memory Array of FIG. 13 on one of the hundred output lines from FIG. 8. Similarly in FIG. 9, the X Switch Core Matrix has a selected one of the switch cores set by application of Read Bias Current on all but one of the Write lines from the Write Drivers of FIGS. 7*b* and *c*, and Read current supplied on one of the Read lines in the Core Read Drivers of FIG. 6, causing one of the cores to be set and a current induced in the secondary which is provided on one of the 80 lines to the Core Memory Array of FIG. 13.

FERRITE CORE PLANES

In FIG. 13, four insulated wires pass through each ferrite core as indicated diagrammatically by the intersection of lines in the Matrix (also see FIG. 2*by*). One is an X Address line (such as 29,080) for each horizontal row, one is a Y Address line (such as 10,915) for each vertical column, another is a sense winding passing diagrammatically through the intersections as shown and common to all the cores in a plane and the last is an inhibit winding passing through the intersections parallel to the X winding as shown in the drawing and common to all cores in the plane. Only one core can be selected from a plane during any given cycle and the

selected core is located at the intersection of the selected X and Y lines, which are each pulsed with half select current at Read time. This coincident current at the intersection of X and Y lines applies full Read current to the selected core tending to change it to the "0" state. During Write time the same X and Y Address lines are selected and each pulsed with half select current such that full Write current is applied to the selected core tending to change it to the "1" state. By pulsing the inhibit winding which is parallel to the X winding with current opposite to the half select current flowing in the X winding (effectively half read current), the switching of the selected core to a "1" is prohibited.

A sense winding passes through all cores in each plane, and since only one core in each plane is interrogated during a cycle, no ambiguity of output will result. At the time the selected core is changing state during reading (if it contained a "1"), the sense line is sampled and the presence of a "1" detected. The Read current sets one Switch Core in each of the X and Y Matrices and the setting of the Switch Cores generates half Read current on one X and one Y Address line feeding 35 planes of Core Memory in parallel. At the points of coincident current, 35 ferrite cores (one for each plane) are provided with full Read current which resets any of the 35 cores holding "ones." Resetting the Cores holding "ones" induces pulses on the corresponding Sense Windings which are amplified in the Sense Amplifiers of FIGS. 15*a* and *b*. The outputs of the Sense Amplifiers are sampled at approximately R_3 time, and these sampled pulses turn On those ones of the Memory Buffer Register triggers of FIGS. 14*a* and *b* corresponding to the Cores that held "ones." Information is retained in the Memory Buffer Register until the end of the cycle when characters of the Memory Buffer Register are used for processing or rewriting back into Core Memory. Core Memory design fixes a relationship between the Core Plane configuration and the Memory Buffer Register since five characters are read at a time. Character addresses ending in 4 or 9 are placed in the Character 4 position of the Memory Buffer Register, while addresses ending in 3 or 8 are placed in Character 3 and so forth.

As mentioned previously, the Memory Buffer Register outputs are provided to six places: The PCT Write Bus, FIGS. 18*a* and *b*; the Output Switch, FIGS. 20*a*, *b*, *c* and *d*; the Memory Address Register, FIGS. 2*r*, *s* and *t*; the MBR Code Check, FIGS. 19*a* and *b*; the SSR, FIGS. 16*a*, *b*, *c* and *d*; and the Input Switch, FIG. 11. Characters are processed in the ALU serially, and therefore one character must be selected from the five characters retained in the Memory Buffer Register. The output Switch chooses one character of the five for processing (except for Instruction cycles and Transmit by Five operations), and the one character selected by the Output Switch is gated to the Memory Out Bus and placed in CR 1. More specifically, the X and Y Switching Circuits decode the Memory Address Select Register address and select the five character group that contains the desired character. The final selection to obtain a single character is determined by the units position of the address via the Memory 4×5 Decoder, FIG. 3*e*, sometimes called the Select Character Switch which decodes the units position of the address contained in the Memory Address Select Register. In accordance with the Core Plane to Memory Buffer Register relationship, the following conditions must be met: if the units position of the address ends in 4 or 9 then the character in position **4** of the Memory Buffer Register is designated for processing. Select character 4 from the 4×10 Decoder, line **3*e*.09** comes up if the units position of Memory Address Select Register contains a 4 or 9. This gates the desired character 4 to the Memory Out Bus. If the units position of the address is 3 or 8 then the character in position 3 of the Memory Buffer Register is wanted for processing. Therefore, Select character 3 line **3*e*.07** is up for this situation.

The following table lists the units position of the address and the corresponding select character lines:

Units position of Memory Address Select Register	Select Character Line
4 or 9	3e.09
3 or 8	3e.07
2 or 7	3e.05
1 or 6	3e.03
0 or 5	3e.01

Each cycle using Core Memory is a complete operation with respect to Memory and Reading and Writing are both performed in one cycle during the Read and Write portions explained previously. For single character processing involving Core Memory, Memory Address Counter 1 steps through the data field sequentially. Because Core Memory reads and writes fire characters simultaneously, five cycles are required to process an entire five character group. Thus, the same addresses are read out and written into Memory five times. When one group is completely processed operation shifts to the next group and so forth. However, it is pointed out that processing can start and stop anywhere in a five character group because each cycle is a complete operation with regard to Core Memory. As the Memory Address Select Register follows Memory Address Counter 1, the select character lines **3*e*.09**, **3*e*.07**, **3*e*.05**, **3*e*.03** and **3*e*.01** are routed individually as determined by the 4×5 Decoder of FIG. 3*e*. One of these select character lines **3*e*.01**, **3*e*.03**, **3*e*.05**, **3*e*.07**, **3*e*.09** remains up for the entire cycle since the Memory Address Select Register is set only at R_0.

In Instruction cycles, all five characters of the Memory Buffer Register are used. Character 0 from the MBR is placed in the Operation Register. Numeric portions of Characters 1 through 4 A and B bits of Character 1, and the B bit of Character 4 of the MBR are placed in the Memory Address Register. Numeric portions of Characters 1, 2 and 3 and the Zone bits required for addressing in Characters 1 and 4 are placed directly in MAR and the numeric portion of position 4 of MBR is transferred indirectly to the MAR via the Memory Out Bus. This latter transfer is permissable as all Instruction addresses must end in 4 or 9 which means that Select Character 4 line **3*e*.09** is always up on Instruction cycles, thus gating position 4 or MBR through the Output Switch. The Memory Out Bus feeds CR 1 as well as the units position of MAR so Character 4 in MBR is set into CR 1 in Instruction cycles and checked by CR 1 Code Check circuits of FIG. 72.

The CR 1 Code Check circuits of FIG. 72 provide code checking for serial (single character) processing. If any character is redundant, that is, has an odd number of bits, the CR 1 Code Check Odd lines **72.03** through **72.05** are positive to indicate an error. MBR Code Checking is not desirable during single character operation because unused Memory characters may be included in a five character group, and if any of the unused characters are redundant, needless error steps would occur. Accordingly, it is only when five characters from MBR are used simultaneously during Instruction cycles and Transmit by S cycles that MBR Code Checking is effective because sampling is only employed in these two instances.

The Input Switch, FIG. 10, gates characters to Memory for writing five characters into those Memory positions which have been read from previously. Six characters are available to the Input Switch, five characters held in the Memory Buffer Register and one character held in the Result Register, and five of the six characters are selected from among the Memory Buffer Register and the Result Register. Either all five characters held in the Memory Buffer Register can be written into Memory or four characters held in the Memory Buffer Register

and the one character in the Result Register can be written into Memory with the result character replacing any one Memory Buffer Register character depending upon the Input Select Gating circuits.

With reference to FIG. 10, the Input Select provides gating lines **10.01** through **10.10** to the Input Switch of FIGS. 11*a* and *b*. The Result to Memory line **137.01** and all five Select Character lines **20***a*.**03**, **20***a*.**02**, **20***a*.**01**, **20***a*.**08** and **20***a*.**10** are used to control the Input Switch. The Result to Memory line, if down, causes five characters held in the Memory Buffer Regster to be written into Memory exactly as they were before reading. However, if Result to Memory line is up, the Result character is written into Memory replacing one of the five characters contained in the Memory Buffer Register according to the Select Character line conditioned in FIG. 10 during that cycle. As an example, if the units position of the Address is 2, Select character 2 is up. Then, Memory Buffer Register characters 0, 1, 3 and 4 are written into the same cores in which they were read, and the Result character from the Result Register is written into the cores from which Character 2 of the Memory Buffer Register was read. The Memory Buffer Register is set at $R_{3.5}$ and the Result Register is set at R_4. Thus, characters in both are available for writing during the Write portion of the cycle.

The Off sides of the triggers of the Memory Buffer Register, FIGS. 14*a* and *b*, are coupled to the Memory Inhibit Driver Circuits of FIGS. 12*a* and *b* via the Input Switch of FIGS. 11*a* and *b*. Also, the On sides of the triggers of the Result Register, FIGS. 89*a* and *b*, are inverted and coupled to the Memory Inhibit Driver Circuits of FIGS. 12*a* and *b* via the Input Switch of FIGS. 11*a* and *b*. (Inverting the On side signal of a trigger is equivalent to taking the signal from the Off side.) Thus, any of the lines which feed the Memory Inhibit Driver Circuits of FIGS. 12*a* and *b* that represent "zeros" have positive signals. In FIGS. 12*a* and *b*, the lines from the Input Switch mix with the Inhibit Gate on lines **5***g*.**01** and **5***g*.**02**, and when the Inhibit Gate rises, inhibit current flows into all of those Core Planes where "zeros" are to be written and, therefore, the writing of "ones" is blocked in those planes where write current is provided as hereafter described. The Write Gate rises shortly after the Inhibit Gate and mixes with the 4×8 Decoder outputs, FIG. 3*b*, and the 6×8 Decoder outputs, FIG. 3*d*, in the Switch Core Write Driver circuits of FIGS. 5*b*, *c* and 7*b*, *c*, respectively. This causes one row in each of the X and Y Switch Core Matrices to be pulsed with Write currents resetting one Switch Core in each matrix. By resetting the Switch Core, half Write current is provided on the same X and Y lines which were pulsed for reading causing "ones" to be placed in all Planes in which Inhibit current is not flowing

Because the ferrite core's hysteresis loop is not precisely rectangular, each half selected core induces a small noise voltage in the Sense Winding having the same polarity whether the core is storing a "one" or a "zero." Therefore, a Half Selected Noise output for any core has the same polarity as the Read output for the core. The Sense Windings are so wound that the Half Selected outputs tend to cancel each other, but the noise voltage may be harmful to the desired signal. Therefore, after writing into the ferrite cores is accomplished, the cores are Post Write Disturbed. Post Write Disturbing is accomplished by resetting the Memory Buffer Register and the Result Register before the Inhibit Gate falls. Resetting these registers brings up all lines on the Off side outputs causing conduction in all 35 Inhibit Drivers. In addition, resetting the Memory Buffer Register and Result Register also prepares them for use on the following cycle.

MEMORY ADDRESS REGISTER

MAR contains the address portion of the Instruction being executed. On a Read (RD), Write (WR), Write Erase (WRE) and serial Transmit (TMT) instruction, this is the address of the high order or left-hand character of the field addressed. On the high-speed Transmit (TMT) instruction, the address is the fifth character from the high order or left-hand character addressed. On all other instructions, the address is the low order or right-hand character of the field addressed.

During Instruction time the Memory Address Register receives an address in parallel from Core Memory by way of character positions 1 through 4 of the Memory Buffer Register and retains the address during Execution. If the operation is a Transfer operation, the contents of the Memory Address Register are transferred to the Instruction Counter during Execute time so that the next Instruction will be obtained from the designated address. However, if the operation is not a Transfer operation the Memory Address Register holds the address of the data in Memory which is to be processed according to particular operation codes in Character 0 of the Instruction. The contents of the Memory Address Register may be transferred to the Memory Address Counters 1 or 2. The outputs of MAR can be sent to MAC 1, FIG. 2*gg* (FIGS. 30*a* through *e*), to MAC 2, FIG. 2*hh* (FIG. 31*a* through *e*), to IC, FIG. 2*ii* (FIGS. 32*a* through *e*), or the Select Register, FIG. 2*jj* (FIGS. 33*a* through *d*).

Since addressing counters and registers use "zero" characters in the true binary form of no "one" bits, a "zero" from MBR represented by an 8 and 2 bit must be converted to an absence of bits. A "zero" from MBR is recognized in the form of 8 and 2 bits and causes the setting lines of its corresponding position in MAR to be blocked. For example, 8 and 2 bits from Character 4 of MBR are combined to hold down Block Set 1st order MAR line **17***f*.**07** thereby preventing setting the 8, 4 and and 2 bit triggers in the first order of MAR, FIG. 17*a*.

Referring to FIG. 17*a*, a sample order of the Memory Address Register is shown comprising four triggers which are reset Off, that is, with the right side conducting, during each Instruction cycle at R_0 (D2) time (FIG. 139*a*). The digit portion of Character 4 from the Memory Buffer Register, FIG. 14*a*, is read into the units position of the Memory Address Register via the Memory Out, FIGS. 21*a* through *d*. Binary "ones" in the 1, 2, 4 and 8 positions cause lines **20***d*.**04**, **20***d*.**05**, **20***d*.**06** and **20***d*.**07** to be positive and condition Diode Gates G_j as shown in FIG. 17*a*. Then a positive signal occurs at A_1 (D0.4) time on the line **101.19** and a positive signal appears on Diode Gate output lines of the Diode Gates that are conditioned which are effective to turn On their respective triggers. Accordingly, for each binary "one" bit, a corresponding trigger in the units order of the Memory Address Register is turned On. As explained above, whenever a 0 Character is represented, i.e., a binary "one" in the 2 and 8 bit positions only, circuits are effective to block the setting of the particular order of the Memory Address Register. The negative signal on the Block Set Memory Address Register line **17***f*.**07** blocks passage of any signals through the Diode Gates which it conditions and consequently all of the triggers in that position remain Off to represent holding of binary "zeros."

MEMORY ADDRESS SELECTOR KEYS

It is also possible to manually set information into the Memory Address Register by means of the Memory Address Select Keys of FIG. 25*a* which cause positive and negative signals representing binary "ones" and binary "zeros" respectively on the MAS—8 line **25***b*.**16**, MAS—4 line **25***b*.**17** MAS—2 line **25***b*.**18** and MAS—1 line **25***b*.**19** to condition one input of the Diode Gates and when these Diode Gates are so conditioned, a signal on the line Set MAR to MAS line **17***f*.**01** is effective to set binary "ones" into the triggers according to the keys selected.

MEMORY ADDRESS COUNTER 1 (MAC 1)

MAC 1, FIGS. 30*a* through 30*e*, is a nineteen-trigger counter that represents a five digit binary coded decimal address in the range of 00000 to 39,999 for a 40K Memory (00000 through 79,999 for an **80K** Memory) which is received from the Instruction Counter or Memory Address Register. An initial address is set into MAC 1 from the Memory Address Register in each Instruction cycle, and MAC 1 is also set to MAR during some Execute cycles in the Multiply, Divide, and Add to Memory instructions. During each Execute cycle of certain parts of instructions such as Add, Subtract, Multiply, Compare and so forth, MAC 1 is stepped to contain the address of data in Core Memory that is to be processed in the next cycle. During certain parts of other instructions such as Shorten, Lengthen, and so forth, MAC 1 is not needed to refer to Memory information and is used to determine the number of cycles required for the operation. MAC 1 can be stepped by three values: plus one (+1) by the line **93***g*.**01**, minus one (−1) by the line **93***g*.**07**, and plus 5 (+5) by the line **93***h*.**02**. Both the stepping pulse gated by the foregoing lines and the setting pulse, lines **30***f*.**07** through **30***f*.**11**, are blocked pulses.

On Execute cycles for Write, Write Erase, and Serial Transmit instructions, the stepping of MAC 1 is gated by an I/O Request and by NOT Transition. MAC 1 is also stepped plus one for all Read instructions when a Read Request is made from an I/O device. During a high speed Transmit operation, MAC 1 and MAC 2 are stepped plus five on alternate cycles. The Instructions set forth above are the only ones where addressing is from high order to low order of a field, and for all other instructions (except where no stepping at all is required) MAC 1 is stepped minus one. Instructions which do not require MAC 1 to be stepped include No Operation, Transfer Any, Halt, Transfer High, Transfer Equal, Transfer Plus, Transfer Zero, Transfer Signal, Read While Writing, Sign, Receive, Normalize Transfer, Transfer, Select and Control.

If an automatic check stop occurs, MAC 1 is not set or stepped but displays on the operator's console the address where the check stop occurred. At R_0, the contents of MAC 1 are automatically set into MASR, FIGS. 49*a* through *j*, if MASR is not set to the contents of either the IC, MAC 2, or SMAC (see FIG. 93*s*). During the Execution of Multiply, Divide and Add to Memory, some steps in the operations let Memory information be used more than once. In all instances, the Memory Address Register is not altered during the execution of an instruction, so when necessary the Set MAC 1 to MAR signal can be used during the operation to set MAC 1 to MAR and use the information over again.

By stepping MAC 1 down one each cycle at R_3 time, MAC 1 reaches 00000 then 39,999 (for 40K Memory) when the outputs are decoded to recognize MAC 1=0. This indication may be used to complete or alter the operation. Also, when MAC 1 reaches the address 39,999 (for 40K Memory), an End of Memory indication is given. During a Write 01 instruction, this indication causes completion of the operation.

FIGS. 30*a* through 30*e* are diagrams of the orders of the Memory Address Counter 1. For the purpose of explanation, the units order of FIG. 30*a* is described although it will be understood that all of the orders will, as required, receive the contents of the Memory Address Register. The contents of the Memory Address Register are represented by signals on the MAR–$\overline{8}$ line **17***a*.**01**, MAR–$\overline{4}$ line **17***a*.**08**, MAR–$\overline{2}$ line **17***a*.**17** and MAR–$\overline{1}$ line **17***a*.**25**, which lines are positive if the respective bits of the Memory Address Register contain binary "zeros," and also on the MAR—8 line **17***a*.**05**, MAR—4 line **17***a*.**14**, MAR—2 line **17***a*.**21** and MAR—1 line **17***a*.**29**, which lines are positive if the respective bits of the corresponding order of the Memory Address Register contain binary "ones." These output lines from the Memory Address Register feed the Diode Gates as shown in the drawings. Thus, as the trailing edge of the signal on the Set MAC 1 to MAR line **30***f*.**07** goes negative, a signal is gated through the proper Diode Gate to cause the required binary "ones" or "zeroes" to be set into the triggers. For example, if the 1 bit of MAR contains a binary "one," the signal on the Set MAC 1 to MAR would pass the Diode Gate connected to the Mar—1 line **17***a*.**29** to turn On the trigger thereby entering a binary "one" in the one-bit position of the Memory Address Counter 1. However, if the one-bit position of MAR had contained a binary "zero," the MAR—$\overline{1}$ line would be positive and the signal on the line Set MAC 1 to MAR would pass the other Diode Gate to turn Off the trigger, thereby entering a binary "zero" in the Memory Address Counter one-bit position. Thus, it is evident that there is no need for providing a reset for the Memory Address Counter before entering the contents of MAR therein, as setting is accomplished by the trailing edge of the Set MAC 1 to MAR signal combined with a signal on one or the other of two input lines per trigger which is effective to set each trigger to either "one" or "zero" regardless of the previous states. When the Step MAC 1+1 or +5 line **30***f*.**01** is positive, the Diode Gates (DG) are conditioned for a negative A_2/R_3–W_1 pulse on the line **30***f*.**06** to the binary input of the 1 trigger which is effective to step the counter one count by changing the condition of the latter trigger. When the 1 trigger goes from an Off to an On condition, it has no effect on the succeeding 2 trigger. However, as the 1 trigger is shifted from an On to an Off condition, its output (by way of the cathode follower on the line MAC 1—1) passes via a conditioned gate to the binary input of the 2 trigger and thereby shifts the condition of the latter trigger. The Diode Gate having an input from MAC 1—$\overline{8}$ must be conditioned by a positive signal on the line **30***f*.**01**, a signal on the line MAC 1—1, and also by a positive signal on the line MAC 1—$\overline{8}$ signifying that the 8 trigger representing the 8 bit contains a binary "zero." A signal MAC 1—8 on line **30***a*.**04** feeds to the succeeding higher order of the Memory Address Counter via a Diode Gate conditioned by Step MAC 1+1 or +5 line **30***f*.**02** to enter a 1 (carry) into the lower order position of the second order of MAC 1.

The Memory Address Counter must also be capable of counting +5 which is accomplished by changing the contents of the 4 and the 1 trigger by way of the Step MAC 1+5 line **93***h*.**02** combined with the A_2/R_3–W_2 line **30***f*.**06** which sets the 4 trigger to the opposite state, and by the Step MAC 1+1 or +5 line **30***f*.**01** and the **30***f*.**06** line which sets the 1 trigger to the opposite state. The units order of MAC 1 must sit at 4 or 9 when MAC 1 is stepped +5.

The Memory Address Counter must also be capable of counting down as mentioned previously. This is effected by a positive signal Step MAC 1—1 on the line **93***g*.**05** which conditions Diode Gates which are effective to couple the left plate output of each trigger to the binary input of the succeeding higher trigger. Thus, when any trigger goes from an Off to an On condition, the succeeding higher trigger is shifted from one condition of stability to another. As any trigger shifts from an On to an Off condition, the output signal to a Diode Gate is positive and therefore has no effect on the succeeding trigger. It should be noted however, that when the 8 trigger shifts from an Off to an On condition, a carry signal is emitted on the line **30***a*.**01**. This carry signal besides feeding the succeeding higher order, also operates via 33 micromicrofarad condensers and a diode to shift the 4 and 2 triggers Off. Briefly, the Step MAC 1—1 line **93***g*.**05** conditions Diode Gates associated with the Off sides of the triggers and connected to lines MAC 1—$\overline{1}$, MAC 1—$\overline{2}$ and so forth, the signals on the respective

lines being positive when the corresponding triggers contain binary "zeros." MAC 1 controls are shown in FIG. 30*f* and their operation will be easily understood when a typical operation of the computer is described.

MEMORY ADDRESS COUNTER 2 (MAC 2)

MAC 2, FIGS. 31*a* through 31*e* is a nineteen trigger counter having the purpose of determining one address used during instructions requiring two addresses, where MAC 2 indicates the address of the information being entered into Memory. This address is set into MAC 2 from the Memory Address Register at W_1 time of the Execute cycle of the Receive (RCV) or Read-While-Writing (RWW) instruction on the fall of the lines **31***f*.**02**, **31***f*.**03**, **31***f*.**04**, **31***f*.**05** and **31***f*.**06**. The setting of MAC 2 is preceded by reset at R_0 time on lines **139***c*.**03** through **139***c*.**07** which is generated by the Reset MAC 2 and Set to MAR lines **131.04** and **69.06** in combination with R_0 (D2) Use line **102.12** (FIG. 139*a*). MAC 2 can be stepped +1 via the line **31***f*.**07** or +5 via the lines **93***h*.**04** and **31**f.**07** during Execute cycles so that the next character to be operated upon may be located. The outputs of MAC 2 are provided to the Memory Address Select Register, FIGS. 49*a* through *j*, and the contents of MAC 2 are set into MASR by way of the set MASR to MAC 2 line **93***s*.**02**.

INSTRUCTION COUNTER

The Instruction Counter, FIGS, 32*a* through *e*, is stepped five for each Instruction cycle so as to contain the address of the next instruction. In normal operations, Instructions are referred to sequentially, five addresses removed from each other since each Instruction requires five characters. During a Transfer instruction, the Instruction Counter is set to a designated address obtained from the Memory Address Register.

The Instruction Counter is reset to 0004 for Initial Reset, Machine Reset and Clear Memory operations before the Instruction Counter is set to the contents of the Memory Address Register. The Instruction Counter is a sixteen trigger counter (for 80K Memory), and the units position of the Instruction Cunter, FIG. 32*a*, has only one trigger which is Off for a 4 and On for a 9. The Off side of the 4 trigger line **17***a*.**09** in the first order of MAR, FIG. 17*a*, controls the setting of the Instruction Counter units position trigger of FIG. 32*a*. If the $\overline{4}$ line **17***a*.**09** is plus, the units position of the Instruction Counter trigger is turned On to represent a 9. This is so because an Instruction must be located at an address with a 4 or a 9 in the units position, as previously described, in order to bring out five characters of an Instruction. The Instruction Counter can receive an address from the Memory Address Register or be stepped +5 at R_3 of every ECC 1 cycle (except for Transfer operations) by changing the state of the first order trigger with the fall of a stepping $-A_2/R_3-W_1$ pulse of the blocked type.

The Instruction adress in the IC is sent to the Memory Address Select Register at R_0 time of each Instruction cycle to obtain the five Instruction characters. When the Instruction Counter is stepped +5 after being set to the original address, 00004, the trigger is turned Off causing the fall of the right plate to send the carry to the first position of the tens order of IC. An auto check stop caused by an Instruction Check Error condition blocks the $-A_2/R_3-W_1$ stepping pulse so that the Instruction Counter remains at the address of the Instruction Error.

More specifically, the IC triggers are reset to 00004 and then the contents of Memory Address Register are emitted via output lines from MAR. Those particular bits holding binary "ones" condition the Diode Gates, the signals on the Set IC to MAR lines **32***a*.**06**, **32***a*.**07**, **32***a*.**08** and **32***a*.**09** are applied and the trailing edge is effective via conditioned Diode Gates (DG) to turn On their respective triggers. In this manner, the contents of Memory Address Register are transferred into the Instruction Counter.

During the first Execute cycle after the Instruction cycle, ECC 1 line **123.34** in FIG. 32*a* is positive and is combined with NOT Manual 3 line **116.09**, Minus on Block Step IC line **93***j*.**12** and A_2/R_3-W_1 (blocked) line **103***a*.**20** to provide a positive output from the AND circuit. The fall of the output of Inverter (IK) switches the trigger to the alternate state at R_3 time. The connections between the stages of the counter are such that when one trigger is turned Off it is effective to shift the condition of the succeeding higher trigger, for example, IC–**9** line **32***a*.**04** to IC–10 trigger of FIG. 32*b*. Assume that the 80 trigger and 10 trigger of the second order of IC, FIG. 32*b*, are On and the IC–80 and IC–10 lines are up to indicate a count of 90 when the IC–9 line **32***a*.**04** goes negative. The latter line turns Off the 10 trigger whose IC–10 line drops and turns Off the 80 trigger. The fall of the IC–80 line **32***b*.**02** provides a carry to the third order of IC, FIG. 32*c*. The second order of IC now stands at 0. The outputs of the 10, 20, 40 and 80 triggers pass through the cathode followers to lines IC–10, IC–20, IC–40 and IC–80, respectively, which lines are negative when respective triggers are Off, signifying holding of a binary "zero." The hundreds, thousands and ten thousands orders of the Instruction Counter operate similarly, receiving inputs from the corresponding orders in the Memory Address Register and further receiving inputs on lines which are carry signals from the succeeding lower stages.

MEMORY ADDRESS SELECT REGISTER (MASR)

MASR, FIGS. 49*a* through 49*j*, is an eighteen trigger register (for 80K Memory) for the purpose of driving the selection circuits of Core Memory. It may be set to either MAC 1, MAC 2, IC, or SMAC at R_0 time, and retains the address of the information being operated on in Core Memory for a complete character cycle from R_0 to R_0. It is pointed out that MAC 1, MAC 2, the Instruction Counter or the Memory Address Register may change status during a machine cycle without effecting the five characters being selected in Memory since MASR is unchanged. The outputs of the Memory Address Select Register, FIGS. 2*ww* through 2*yy*, are sent to the X and Y Switching circuits, FIG. 2*a*, to select five characters from Core Memory as described previously. Outputs in the first order triggers of the Memory Address Selection Register, FIG. 2*ww* (FIGS. 49*a* and *b*) are also sent to the Memory 4×5 Decoder, otherwise known as the Character Select Switch, FIG. 3*e*, to determine which of the five characters is to be sent to CR 1, FIG. 2*h*, by way of Memory Out, FIG. 2*g* (FIGS. 20*a* through *d*.)

Referring now to FIG. 49*a*, the first order of the Memory Address Select Register is shown and its description will serve as a description of the other orders. The Diode Gates (G_j) serve to change the state of the trigger with a positive shift when conditioned by positive signals on lines representing binary "ones" or the complements thereof. The set circuits for the first order of the Memory Address Select Register are shown in FIG. 49*b* as having inputs from Memory Address Counter 1, Memory Address Counter 2, the Instruction Counter, and the SMAC (line **17***a*.**24**). The set circuits are selection circuits for selecting the contents of MAC 1, MAC 2, the Instruction Counter, or the SMAC, in response to signals on the Set MASR to MAC 1 line **93***s*.**02**, Set MASR to MAC 2 line **93***s*.**03**, Set MASR to IC line **93***s*.**01** and Set MASR to SMAC line **93***s*.**04**, which condition the AND circuits for the passage of binary "one" values to the outputs of the cathode followers. Positive outputs are provided on the 8 line **49***b*.**02**, the 4 line **49***b*.**04**, the 2 line **49***b*.**06**, the 1 line **49***b*.**08**, whenever the binary value of "one" is represented. When the last mentioned lines are down indicating binary "zeros," Inverters attached to each line provide positive outputs on the $\overline{8}$ line **49***b*.**01**, $\overline{4}$ line **49***b*.**03**, $\overline{2}$ line **49***b*.**05** and $\overline{1}$ line **49***b*.**07**. Each of the pairs of lines are connected to input lines of the first order of MASR,

FIG. 49*a*, where the lines representing binary "one" values are connected via Diode Gates to the On side of the triggers and the complement lines representing binary "zeros" having positive signals are connected via Diode Gates to the Off side of the triggers. With these connections it will be noted that it is unnecessary to reset the MASR since pairs of lines are effective to set the triggers to the required values regardless of their previous state. The R_0 (D0.4) line **101.01** conditions the Diode Gates for the passage of positive signals on the input lines from the first order of MASR set circuits, FIG. 49*b*. The other four orders of MASR and their associated MASR set circuits are provided in the remaining FIGS. 49*c* through *j* and they operate in a manner similar to the first order of MASR.

STORAGE SELECT REGISTER

The Storage Select Register (SSR), FIG. 16*a*, consists of four triggers that select a particular Storage unit by way of the Storage Address Counter, FIGS. 52*a* through *d*, and SSR Decoding, FIG. 54, or that identify a special type of Instruction by way of SSR Decoders, FIGS. 55*a* and *b*. The SSR is Instruction reset by means of a line **139***b*.**01** from Instruction Reset Controls of FIG. 139*b*, and then the Zone Bit configurations of characters 2 and 3 of the Memory Buffer Register are set into the SSR. The Memory Buffer Register character 2–B line **14***a*.**02**, Memory Buffer Register character 2–A line **14***a*.**02**, MBR character 3–B line **14***a*.**02** and MBR character 3–A line **14***a*.**02** condition Diode Gates (G_j), and at A_0 of I time, a positive signal on the line **101.24** causes those outputs of the Diode Gates to go positive which are conditioned by signals of the Memory Buffer Register indicating binary "ones" to set the corresponding triggers On. During manual operations, the Storage Select Register is reset during Manual 1 time by a manual timer via line **116.02** which causes Instruction reset, FIG. 139*a*. Keyed outputs indicative of binary "ones" are present on the SS—8 line **16***b*.**01**, SS—4 line **16***b*.**02**, SS—2 line **16***b*.**03** and SS—1 line **16***b*.**04** where binary "ones" are desired. These lines feed diode gates (D_G) and upon the fall of the Set SSR to SS line **17***f*.**06**, the negative shift at the outputs of diode gates (D_G) sets to the On state those triggers where binary "zeros" are desired. Lines **16***a*.**01**, **16***a*.**04**, **16***a*.**07**, **16***a*.**11**, **16***a*.**14**, **16***a*.**18**, **16***a*.**21** and **16***a*.**25** go to Storage Select Register Decoder stages 1 through 8 of FIG. 55*a* and lines **16***a*.**05**, **16***a*.**08**, **16***a*.**12**, **16***a*.**15**, **16***a*.**19**, **16***a*.**22** and **16***a*.**26** go to Storage Select Register Decoder stages 9 through 15 of FIG. 55*b* to modify certain instructions. The lines **16***a*.**03**, **16***a*.**16**, **16***a*.**17** and **16***a*.**24** go to Storage Select Register Decoding of FIG. 54, for distinguishing Storage Addresses in the Accumulator from Storage Addresses in Auxiliary Storage. The lines **16***a*.**02**, **16***a*.**06**, **16***a*.**09**, **16***a*.**13**, **16***a*.**16**, **16***a*.**20**, **16***a*.**23** and **16***a*.**27** go to stages 5 through 8 of the Storage Address Counter, FIG. 52*d*, for setting stages 5 through 8 of SAC in FIG. 52*c* to the SSR bits 1, 2, 4 and 8, respectively. Since there are no bits in the zone portions of characters 2 and 3 of the Instruction when the Accumulator is used, SSR is then 0 making SASR 256 line **54.24** positive and SSR=0000 lines positive in FIG. 54. SASR 256 line **54.24** goes to FIG. 34*a* to select the Accumulator portion of Storage and in combination with the Storage Address Counter address, which is set in the Storage Address Select Register, locates a particular character. The SSR=0000 lines allow SAC to be set to the Starting Point Counter, conditions the Accumulator DZT and Accumulator Sign trigger, identifies Instructions which have no bits in the zone portion of the second and third characters. When an Auxiliary Storage unit is used, one or more of the SSR triggers would be On bringing up SASR $\overline{256}$ line **54.01** and the SSR≠0000 lines, FIG. 54. SASR $\overline{256}$ line **54.01** selects the Auxiliary portion of Storage. The SSR≠0000 lines allow the four high order positions of the Storage Address Counter to be set by the Storage Select Register and resets the four low order positions of SAC. When the Storage Address Select Register is set to SAC combined with SASR $\overline{256}$, the units position of the proper Auxiliary Storage unit is selected. The SSR≠0000 lines of FIG. 54 also condition the Auxiliary Storage DZT and Auxiliary Sign trigger and identify Instructions with zone bits in the second and third order positions of the Instruction.

STARTING POINT COUNTER (SPC)

The Starting Point Counter of FIGS. 51*a*, *b* and *c*, is an eight stage binary counter of capacity 256 which keeps track of the starting or reference point of a field in the Accumulator. The Starting Point Counter has no reset to 0 and no means to be set to any particular address. When the machine is turned On, SPC may contain any numebr 0 through 255, depending upon the way in which the individual triggers establish their stable states. The SPC can be stepped up or down one unit completely around to and beyond its original starting point and can be stepped 128 positions, also. The Starting Point Counter determines the location of the units position of the field in the Accumulator, the other limit being determined by the Storage Mark. As in the case of MAC 1, if an Auto Check Stop occurs, the stepping pulses to the Starting Point Counter are blocked to prevent altering the contents of SPC from the error position.

Referring to stages 1 through 3 of the Starting Point Counter in FIG. 51*a*, the SPC may be stepped up one count by means of the line **93***j*.**01** and down one count by the Step SPC—1 line **93***j*.**03** which conditions diode gates sampled at A_2 time by the $-A_2/R_3-W_1$ line **52***e*.**02**. If the Starting Point Counter is to be stepped up, a signal on the Step SPC+1 line **93***j*.**01** goes positive to condition the upper diode gate in each position. With the line **93***j*.**01** positive, a negative signal is provided on the line **52***e*.**02** which is passed to the binary input of the 1 trigger causing the later to shift from one condition of stability to another. As the 1 trigger shifts from an On to an Off condition, a negative signal is emitted from its right plate and is fed via the cathode follower and a conditioned diode gate to a binary input of the next adjacent trigger, the 2 trigger, thereby causing the latter to shift from one condition to another. Likewise, succeeding bit triggers of the counter receive inputs from the adjacent lower order. Positive going outputs from the triggers have no effect on succeeding stages.

To step the SPC down one count, the SPC—1 line **93***j*.**03** is positive to condition the lower diode gates in each stage, and the negative signal on the line **52***e*.**02** is then passed via the diode gate to the binary input of the 1 trigger. However, in this instance, only when this trigger shifts from an Off to an On condition is a negative signal emitted and passed via the conditioned diode gate to provide a binary input to the next adjacent trigger, the 2 trigger. The same type of circuits and explanation applies to succeeding higher stages.

On occasion it is desired to step the Starting Point Counter by a count of 128. This is accomplished at W_1 time by conditioning a diode gate with a signal Step SPC+128 on the line **93***j*.**07** and sampling with an A_2/R_2-W_1 signal on the line **52***e*.**08** to the eighth order of the SPC. The output of this gate is applied to the trigger so that a negative input is effective to cause a shifting of its condition.

STORAGE ADDRESS COUNTER

The Storage Address Counter (SAC), shown in FIGS. 52*a* through 52*d*, is an eight stage binary trigger counter that designates the address of the Storage character to be processed the next cycle. In FIGS. 52*b* and 52*d*, the contents of the Starting Point Counter can be set into SAC via the lines **52***a*.**01** through **52***a*.**08** in combination with the Set SAC to SPC line **52***e*.**04** and the lines **51***b*.**03** through **51***b*.**06** and **51***c*.**01** through **51***c*.**04** in combina-

tion with the Set SAC to SPC line **52***e*.**05**. Output lines **52***b*.**01** through **52***b*.**08** and **52***d*.**01** through **52***d*.**08** are connected as inputs to the SAC triggers of FIGS. 52*a* and 52*c* respectively. When the Storage Select Register equals zero, indicating that Accumulator Storage is being used, all eight stages of SAC are set to the contents of SPC. When the Storage Select Register is not equal to zero, indicating that an Auxiliary Storage unit is being used, however, the Set SAC to SSR lines **52***e*.**06** and **52***e*.**07** are positive to cause the four high order positions of SAC to be set to the bit pattern of the SSR and to cause the four low order positions, stages 1 through 4, of SAC to be reset to "zero."

In FIGS. 52*a* and *c*, SAC can be stepped plus one by a positive signal on the lines **93***i*.**03** and **93***i*.**04** in combination with the fall of the $-A_2/R_3-W_1$ Blocked pulse on the line **52***e*.**03**, the latter being connected to the units order diode gate. In FIG. 52*a*, the line **93***i*.**03** conditions a diode gate (in the upper row of diode gates) for each trigger, and, similarly, in FIG. 52*c* the line **93***i*.**04** conditions a diode gate for each trigger of the higher orders. The output of each diode gate is connected to the binary input of each trigger, and the right plate output of each trigger is applied as an input to the diode gate of each higher order trigger. Keeping in mind that it is the fall of the pulse supplied to a conditioned diode gate that provides an output, it will be evident that it is only the change from "one" to "zero" of a trigger that can be supplied to the binary input of the next higher order trigger when the Step SAC +1 line is positive. For example, assume that SAC is zero (all triggers Off) and that the diode gates are conditioned by a positive pulse on the lines **93***i*.**03** and **93***i*.**04**. When the $-A_2/R_3-W_1$ pulse falls the 1 trigger is turned On. The right-hand plate of the one trigger goes positive but the rise is ineffective to provide an output from the upper diode gate feeding the binary input to the 2 trigger. The count is now 1 as indicated by the 1 trigger being On and all others Off. When the Step SAC +1 lines **93***i*.**03** and **93***i*.**04** are positive during the next cycle and the line **52***e*.**03** falls, the 1 trigger is turned Off and the fall of the right-hand plate of the 1 trigger is passed to the binary input of the 2 trigger via the diode gate to turn On the 2 trigger. The count is now 2 as indicated by only the 2 trigger being On. On the third cycle, the 1 trigger is turned On and its right-hand plate rises which is ineffective to turn Off the 2 trigger. The 4 trigger and other higher orders cannot be turned On since the right plate of the 4-trigger remains positive and the other higher orders are still Off. The count is now 3 as indicated by the 1 and 2 triggers being On and the remaining triggers being Off. In the fourth cycle, the fall of the Blocked pulse on the line **52***e*.**03** turns Off the 1 trigger and the fall of its right plate turns Off the 3 trigger. The fall of the right plate of the 3 trigger turns On the 4 trigger. Thus, the count is now 4 as indicated by the 4 trigger being On and all other triggers being Off. Counting up continues in the manner described. Although the example of operation was given starting from a count of zero, it will be understood that SAC may be set to any value as previously described and then stepped up by one as required.

SAC can also be stepped minus one by the Step SAC—1 lines **93***i*.**01** and **93***i*.**02** and the $-A_2/R_3-W_1$ Blocked line. The Step SAC—1 lines condition the lower rows of diode gates in FIGS. 52*a* and *c* and the Blocked pulse is applied only to the 1 trigger diode gate. The left plates of all triggers, except the one of the highest order, are connected as inputs to the lower row of diode gates. As an example of operation, assume that SAC contains a count of 4, that is, the only trigger On is the 4 trigger. With the Step SAC—1 line positive, the fall of the Blocked pulse on line **52***e*.**03** turns On the 1 trigger, the fall of the left plate of the 1 trigger turns On the 2 trigger, and the fall of the left plate of the 2 trigger turns Off the 4 trigger. Since the left plate of the 4 trigger rises, the 8 trigger is not turned On and the remaining higher order triggers are not affected. Of course, any value may be set into SAC and then decreased in steps by one as desired.

SAC can also be stepped plus 128 by the Step SAC+128 line **93***i*.05 and the A_2/R_3-W_1 (Blocked) line **52***e*.**09**. This is accomplished by changing the state of the 128 trigger of FIG. 52*e*. A positive voltage on the Step SAC+128 line conditions a diode gate for the fall of the pulse on line **52***e*.**09** which provides a negative signal to the binary input of the 128 trigger thereby reversing its condition of stability to the opposite sense.

As mentioned previously, the eight triggers of SAC count 256 addresses, and if all triggers are On indicating address 255, stepping the counter plus one turns all triggers Off to register address zero.

The output lines **52***c*.**02** through **52***c*.**09** and **52***a*.**01** through **52***a*.**08** are used to set Storage Address Select Register, FIGS. 53*a* and *b*, at R_0 time of every cycle. Therefore, the address can be altered during each cycle in preparation for the next cycle while the Storage Address Select Register holds the location of the character being processed. The output lines **52***a*.**11**, **52***a*.**12**, **52***a*.**13** and **52***a*.**14** from FIG. 52*a* and the line **52***c*.**01** from FIG. 52*c* are used in the SAC controls of FIG. 52*e* to recognize critical addresses by bringing up the output line **52***e*.**01**. The output lines **52***a*.**09** and **52***a*.**10** from FIG. 52*a* to FIG. 52*c* are those lines previously described as being used to propagate carries while stepping SAC plus one or minus one.

The SAC controls are illustrated in the lower portion of FIG. 52*e* where the minus A_2/R_3-W_1 pulse is generated, the Set SAC to SPC pulse is derived from A_2/R_3-W_1 line **103***a*.**16**, E time line **123**.**23**, Set SAC to SPC line **93***j*.**08** and SSR=0000 line **54**.**10**. The Set SAC to SSR pulse is derived by combination of the Set SAC to SPC line **93***j*.**08**, A_2/R_3-W_1 Use line **103**.**06**, I time line **124**.**33** and Storage Select Register ≠0000 line **54**.**02**. It is particularly pointed out that the Set SAC to SPC lines **52***e*.**04** and **52***e*.**05** are brought up during the Execute or Instruction cycle while the Set SAC to SSR line **52***e*.**06** is brought up during Instruction cycle.

STORAGE ADDRESS SELECT REGISTER

The Storage Address Select Register (SASR) of FIGS. 53*a* and *b* is an eight trigger register that contains the address of the character being processed in Storage. Its output lines **53***a*.**01** through **53***a*.**08** and **53***b*.**01** through **53***b*.**08** are decoded in the Decoders of FIGS. 34*a* through 34*d* to select the X and Y Switching circuits which locate the character to within a factor of two in Storage. SASR is set to the contents of the Storage Address Counter at R_0 time by pairs of output lines from each position of SAC which, when positive, condition plus diode gates gated by the R_0 (D0.4) lines **101**.**06** and **101**.**07** for every Execute cycle, except during certain Transition cycles associated with critical addresses. A Minus on Suppress SASR to SAC line **136***b*.**07** conditions the plus diode gates for the 32, 64 and 128 triggers of FIG. 53*b* for an Auto Transition cycle in the Read/Write mode as will be explained hereafter. The Storage Address Select Register retains the selected address from R_0 to R_0 time allowing SAC to obtain another address without affecting the character addressed in Storage.

SUMMARY OF SETTING COUNTERS AND REGISTERS

At W_2 time of an End Execute cycle, the I/E trigger changes to I. The Memory Buffer Register resets at W_3 time preparing to receive five new characters. At R_0 of each Instruction cycle the Memory Address Select Register is set to the Instruction address in IC and drives the X and Y switching circuits of Memory. At the same time the Memory Address Register, Storage Select Register and Operation Register are reset to receive new information. The Read Memory operation begins at R_0. A Read Sample pulse conditions the Sense Amplifiers at approxi-

mately $R_{3.5}$ and sets the 35 triggers in the Memory Buffer Register to the bit configuration of the five characters. At A_0 time the Operation Register is set with character 0 from the Memory Buffer Register, the Storage Select Register is set to the storage code of the Memory Buffer Register, and Character Register 1 is set to Character 4 of the Memory Buffer Register. The Memory Address Register is set to certain bits of the Memory Buffer Register at A_1 of an Instruction cycle and the Instruction Counter is stepped at R_3 time of ECC 1 to prepare for the next Instruction. Writing the instruction characters back into Memory is initiated by the Write Gate at W_0. At W_1 time, MAC 1 is set to the Memory Address Register so that the address of the data field is available from MAC 1 during the next machine cycle.

The first Execute cycle, ECC 1, begins at W_2 when the I/E trigger changes from I to E and the ECC 1 trigger is turned On. At W_3 time, the MBR and SBR are reset to prepare for receiving new characters. At R_0, the MASR is set to MAC 1, MAC 2, IC or SMAC and the SASR is set to SAC. At R_3 of ECC 1, there is a conditional operation in which the IC is stepped plus five provided an instruction Check Stop or a Transfer operation is not indicated. If the Read Memory and Read Storage Routing lines are brought up in this cycle, the Read Sample pulse conditions the Sense Amplifiers and sets the triggers in the MBR and SBR accordingly at $R_{3.5}$. At W_0 time of ECC 1, one character is set into each Character Register, CR 1 and CR 2. At W_2, depending upon whether the SSR is equal to zero or not, SAC is set to either the SPC or the SSR. Also, at W_1, MAC 1 is set to MAR.

Summarizing Execute cycles generally, each cycle has cycle points R_0, R_1, R_2, R_3, R_4, W_0, W_1, W_2 and W_3, where R_0 to W_0 is Read time and W_0 to R_0 is Write time as previously described. At R_0, MASR and SASR are set to their respective counters, and R_3 is stepping time for the counters. The Buffer Registers are set at about $R_{3.5}$ and R_4 is the setting time for the Result Register. W_0 is the setting time for the Character Registers and is the usual switching time for triggers associated with the ALU. W_1 is the switching time for the Add triggers which defines an arithmetic cycle. W_2 is switching time for the I/E trigger, Use trigger, ECC 1 trigger, Type Cycle triggers, Transition triggers and Mode Control triggers among others. W_3 is the switching time for the MAC 1 Equals Zero trigger and is reset time for the Result Register, Memery Buffer Register and Storage Buffer Register.

EXAMPLE OF CORE MEMORY OPERATION

Assume that the Memory Address of 19,955 is set in the triggers of the Memory Address Select Register of FIGS. 49*a* through 49*j*. Accordingly, the Memory Address Select Register $\overline{8}$ lines **49***a*.**01** and **49***a*.**02** are up, the Memory Address Select Register 4 lines **49***a*.**07** and **49***a*.**08** are up, the MASR $\overline{2}$ lines **49***a*.**10** and **49***a*.**11** are up, and MASR 1 lines **49***a*.**16** and **49***a*.**17** are up. In FIG. 49*c*, the MASR $\overline{80}$ line **49***c*.**01** is up, the line MASR 40 line **49***c*.**05** is up, the MASR $\overline{20}$ line **49***c*.**07** is up, and the MASR 10 line **49***c*.**11** is up. In FIG. 49*e*, MASR 800 line **49***e*.**02** is up, MASR $\overline{400}$ line **49***e*.**04** is up, MASR $\overline{200}$ line **49***e*.**07** is up, and MASR 100 line **49***e*.**11** is up. In FIG. 49*g*, the MASR 8000 line **49***g*.**02** is up, the MASR $\overline{4000}$ line **49***g*.**04** is up, the MASR $\overline{2000}$ line **49***g*.**06** is up, and the MASR 1000 line **49***g*.**10** is up. In FIG. 49*i*, the MASR 10,000 line **49***i*.**02** is up, the MASR $\overline{20,000}$ line **49***i*.**04** is up, and the MASR $\overline{40,000}$ lines **49***i*.**07** and **49***i*.**08** are up. In FIG. 3*b*, the Memory 4×10 Decoder, the lines **49***i*.**04**, **49***c*.**07** and **49***c*.**05** from the Memory Address Select Register, FIG. 49*c*, are combined in an AND circuit to provide an output on the 40 (P) line **3***b*.**05**. The line **3***b*.**05** goes to the Y Switch Core Write Drivers of FIG. 5*a* where it provides an output on the 40 (P) line **5***a*.**05** and brings down the $\overline{40}$ line **5***a*.**06** due to the inverter in the latter line. All of the NOT output lines are up except $\overline{40}$ line **5***a*.**06** since the input line **3***b*.**05** is the only one up. In FIGS. 5*b* and *c*, these lines $\overline{00}$, $\overline{20}$, $\overline{60}$, $\overline{80}$, $\overline{20,000}$, $\overline{20,020}$, $\overline{20,040}$, $\overline{20,060}$ and $\overline{20,080}$ are combined with Memory Read Bias Gates on lines **5***g*.**09** and **5***g*.**18** to provide outputs on the lines **5***b*.**01**, **5***b*.**02**, **5***b*.**03**, **5***b*.**04**, **5***b*.**05**, **5***c*.**01**, **5***c*.**02**, **5***c*.**03**, **5***c*.**04** and **5***c*.**05** at R_0 as shown in the Memory Timing Chart of FIG. 144. An output is not provided on the line **5***b*.**03** at this time since the 40 (P) line **5***a*.**05** is up, but the line **5***g*.**03** is down. The $\overline{40}$ line **5***a*.**06** is down so the pulse on line **5***g*.**09** does not bring up the line **5***b*.**03**. The lines just described go to the Y Switch Core Write windings of FIG. 8 where the lines enter from the bottom and drive each column of the Switch Cores except the column associated with the 40 line **5***b*.**03**.

In FIG. 3*d*, Memory 6×8 Decoder, the $\overline{8}$ line **49***a*.**01**, the $\overline{2}$ line **49***a*.**10**, the 4 line **49***a*.**07**, the 1 line **49***a*.**16**, the 10 line **49***c*.**11** and the 10,000 line **49***i*.**02** are up. The outputs of these lines are decoded to provide an output on the 10,015–10,019 line **3***d*.**15** which goes to the X Switch Core Write Drivers, FIG. 7*a*, bringing up the 10,015–10,019 (P) line **7***a*.**15** and bringing down the $\overline{10,015–10,019}$ line **7***a*.**16**. Since none of the other inputs to the 6×8 decoder are up the $\overline{0–4}$ line **7***a*.**02**, the $\overline{5–9}$ line **7***a*.**04**, the $\overline{10–14}$ line **7***a*.**06**, the $\overline{15–19}$ line **7***a*.**08**, the $\overline{10,000–10,0004}$ line **7***a*.**10**, the $\overline{10,005–10,009}$ line **7***a*.**12** and the $\overline{10,010–10,014}$ line **7***a*.**14** are up. These lines go to the X Switch Core Write Drivers of FIGS. 7*b* and *c* where they are combined with the Memory Read Bias Gate on lines **5***g*.**11** and **5***g*.**12** to provide outputs on the lines **7***b*.**01**, **7***b*.**02**, **7***b*.**03**, **7***b*.**04**, **7***c*.**01**, **7***c*.**02** and **7***c*.**03** at $R_{0.5}$ as shown in FIG. 144. The 10,015–10,019 line **7***c*.**04** is down since the $\overline{10,015–10,019}$ line **7***a*.**16** and the Memory Write Gate line **5***g*.**06** are down. The output lines from Memory X Switch Core Write Drivers, FIGS. 7*b* and *c*, go to the X Switch Core Write winding of FIG. 9, entering the figure from the top and passing through the rows of switch cores, carrying reset current (except for the 10,015–10,019 line **7***c*.**04**).

The output lines of FIG. 49*g* go to Memory 4×10 Decoder, FIG. 3*a*, where the lines **49***g*.**04**, **49***g*.**06**, **49***g*.**02** and **49***g*.**10** are up. The only lines effective are the 8000 and 1000 lines **49***g*.**02** and **49***g*.**10**, respectively, which are combined to provide an output on the 9000 (P) line **3***a*.**19**. The line **3***a*.**19** goes to the Memory Y Switch Core Read Drivers of FIG. 4 and when the Memory Y Read Gate line **5***g*.**08** comes up at R_1 as shown in FIG. 144, an output is provided on the 9000 line **4.10**. The line **4.10** goes to Y switch Core Matrix, FIG. 8, to drive the 9000 line through the upper row of switch cores, tending to set the switch cores of the top row. Reset current is flowing in all of the columns except the one associated with the 40 line **5***b*.**03** as explained previously. Accordingly, the top row of switch cores have set and reset current applied thereto except for the core at the intersection of the 9000 line **4.10** and the 40 line **5***b*.**03**. Accordingly, this Switch Core 9040 is set and an output is provided on the secondary coil 9040 which goes to the Core Array of FIG. 13 to provide half select current of the line 9040.

In FIG. 3*c*, Memory 4×10 Decoder, the $\overline{400}$ line **49***e*.**04**, the $\overline{200}$ line **49***e*.**07**, the 800 line **49***e*.**02** and the 100 line **49***e*.**11**, from the Memory Address Select Register, FIG. 49*e*, are up. The only two lines effective are the 800 line **49***e*.**02** and the 100 line **49***e*.**11**, which are combined in an AND circuit to provide an output on the 900 (P) line **3***c*.**19**. The 900 (P) line **3***c*.**19** goes to the Memory X Switch Core Read Drivers of FIG. 6 and when the Memory X Read Gate (P) line **5***g*.**07** comes up at $R_{1.3}$ as shown in FIG. 144, an output is provided on the 900 line **6.10** which goes to the X Switch Core Read windings of FIG. 9. In FIG. 9, the X Switch Core Matrix, the line **6.10** passes from left to right through the

upper row of the Switch Cores providing set current therefor and returns to FIG. 6 as line **9.01** providing feedback into the Amplifiers as shown in FIG. 6. Accordingly, the only core set is the 10915–10919 one at the intersection of lines **7***c*.**04** (also labeled line **9.11** at the bottom of the sheet) and **6.10** (also labeled line **9.01** at the bottom of the sheet), providing an output on the secondary winding for the addresses 10,915–10,919. This output goes to the Memory Core Array of FIG. 13 to provide half select current to the cores linked by the 10,915 line. The core at the intersection of the 10,915 line and the 9040 line receives full select current. It will be recognized the sum of these two addresses, 10,915 and 9040, is equal to the address 19,955. As described previously, the two half select currents tend to reset the core and if the core at the intersection of the lines just mentioned is a "1," then an output is detected on the sense line to give an indication of such as shown in FIG. 144. If the core contains a "0," the reset current is of no practical effect and a signal is not produced on the sense line. It has been pointed out that the Memory Core Planes of FIG. 13 are stacked such that thirty-five planes are arranged one above the other. The 9040 line and the 10,915 line provide the half select current not only to the Memory Core Plane as illustrated, FIG. 13, but to all thirty-five of the core planes in parallel such that thirty-five bits are read out on the sense windings, lower and upper, which are directed to the Sense Amplifier circuits of FIGS. 15*a* and *b*. The outputs of the Amplifier circuits are sampled at $R_{3.6}$ and if the core is changing from a "1" to a "0" outputs are provided on the lines 14*a* and *b* to the Memory Buffer Register of FIGS. 14*a* and *b*. In an example to follow, it will be assumed that the contents of the Memory Buffer Register are read back into the same address in Core Memory.

The inputs to the Sense Amplifiers are full wave rectifiers (TMS), comprising a pulse transformer and two diodes (not shown). The two diode plates are tied to the opposite ends of the secondary windings of the pulse transformer, the diode cathodes are tied together to ground making a full wave rectifier. The full wave rectifier feeds the first stage of a pair of amplifiers which are RC coupled pentode stages (AMS) which feed a cathode follower (K). The grid of the cathode follower (K) is diode clamped to keep it from going below a bias voltage of approximately −27 volts on the line 5*h*.**09**.

Sample positions of the Memory Buffer Register are shown in FIGS. 14*a* and *b* for the characters 4, 3 and 2 and 0 and 1 respectively. The Memory Buffer Register has thirty-five triggers and is set to the outputs of the sense amplifiers by the Memory Sample pulse at $R_{3.5}$ on the lines **20***e*.**03** and **20***e*.**04**. Information once set into the Memory Buffer Register is held by the triggers until W_3 of the character cycle. Thus, information in the MBR is available either for processing or writing back into Memory. The Memory Buffer Register output lines are connected as best illustrated in FIGS. 2*c* through 2*e* and furnish inputs to the Memory Buffer Register Code Check circuits, FIGS. 19*a* and *b*, the Memory Address Register, FIGS. 17*a* through *e*, the Input Switch, FIG. 11, and the Output Switch, FIGS. 20*a* through *d*. On Instruction cycles character 0 position of MBR furnishes a character to the Operation Register, FIGS. 21*a* and *b*; character positions 1, 2 and 3 provide numeric bits and character 1 provides B and A bits also to the Memory Address Register, FIGS. 17*a* through *e;* and the MBR character 4 position passes numeric bits through the output switch to the Memory Address Register but the B bit character position 4 goes directly to MAR. As previously mentioned, when it is desired to Write the information contained in the Memory Buffer Register of FIGS. 14*a* and *b* into the Core Array of FIG. 13, the half select currents on the lines 9040 and 10,915 are reversed for all thirty-five planes to set the cores to the "one" state. However, in these core planes where it is desired to store "zeros" in a particular core according to the state of the triggers in the Memory Buffer Register, inhibit current is supplied which counteracts the set currents thereby preventing the setting of the selected core in that plane in the "one" state.

In FIG. 10, Memory Input Select, the Result to Memory 1 line **137.01** is down since in the operation to be described the contents of the Memory Buffer Register are to be written back into the Core Memory Array. Accordingly, all of the outputs of the AND circuits of FIG. 10 are down, and the inverters cause the Buffer Register to Memory output lines **10.01**, **10.03**, **10.05**, **10.07** and **10.09** to be up. These signals are provided to the Input Switches of FIGS. 11*a* and *b* and the NOT outputs on lines **14***a*.**01**($\overline{N}$) and **14***b*.**02**($\overline{N}$) of FIGS. 14*a* and *b*, are supplied to FIGS. 11*a* and *b*, respectively, for the characters 4, 3, 2, 1 and 0. Therefore, for each bit position of the Memory Buffer Register containing a "zero" the $\overline{N}$ output will be up. In FIGS. 11*a* and *b*, when the Buffer Register to Memory lines **10.09** and **10.01** are up, outputs will be provided on the lines to the Inhibit Driver circuits of FIGS. 12*a* and *b* for each bit position of the characters 0 through 4 which contain a "zero." Referring now to FIGS. 12*a* and *b*, the lines from the input switch of FIGS. 11*a* and *b* are up according to the "zero" bit configurations of the characters in the Memory Buffer Register, and when the Memory Inhibit Gate is applied on the lines **5***g*.**02** and **5***g*.**01**, between R_4 and W_0, as shown in FIG. 144, outputs are provided from FIGS. 12*a* and *b* to the Inhibit windings of FIG. 13 for those planes where it is desired to write "zeros." In FIG. 13, the inhibit current applied to each selected plane where a "zero" is to be written opposes that current through the X Driver line tending to set the core to a "one." At W_0 the Write Gate is provided, as shown in FIG. 144, to the Y Switch Core Write Drivers of FIGS. 5*b* and *c* on the lines **5***g*.**03** and **5***g*.**04** respectively, bringing up only the 40 line **5***b*.**03** which, as mentioned previously, was not energized during the Read portion of the cycle. In FIG. 8, the only core in the set condition prior to Writing is the core 9040 at the intersection of the 9000 line **4.10** and the 40 line **5***b*.**03**, and the 40 line **5***b*.**03** provides reset current to the core 9040 and provides feed back current to the Y Switch Core Write Drivers of FIG. 5*b* on the line **8.03**. In FIG. 4, Memory Y Switch Core Read Drivers, the Read Gate on line 5*g*.**08** is down and, therefore, the signal formerly provided on the 9000 line **4.10** during Reading is absent during Writing. Referring to FIG. 8 once again, it is pointed out that the 9000 line **4.10** is not driven and that the 9040 core is reset from 1 to 0 thereby providing half select current in FIG. 13 in a direction tending to set each core in the 9040 row of each of the thirty-five planes to a "one."

In FIGS. 7*b* and *c*, X Switch Core Write Drivers, the output lines which were up during the Read portion of the cycle are down since the Read bias gate is down. However, the 10,015–10,019 output line **7***c*.**04** is up due to Memory Write Gate line **5***g*.**06** which comes up at W_0. Accordingly, in FIG. 9 only the 10,015–10,019 line **7***c*.**04** is carrying current tending to reset the cores linked thereby, and the only core which is affected by the reset current is the core corresponding to the Address 10,915–10,919 which was set during Reading. Current is not provided on the 900 line **6.10** from the Switch Core Read Drivers and therefore, the secondary of the Switch Core associated with Address 10,915–10,919 supplies half select current to the Array of FIG. 13 on the line labeled 10,915. In the absence of inhibit current, the core in FIG. 13 at the intersection of the lines 9040 and 10,915 is set to a "one," and, as previously described, inhibit current is applied to those cores corresponding to MBR positions which contain "zeros."

It will be noted that although the Memory Address Select Register, FIG. 49, contained the address 19,955, for

the operations just described, the characters were read into the Memory Buffer Register corresponding to addresses 19,955 to 19,959 and the same characters would have been read into the Memory Buffer Register for addresses 19,956; 19,957; 19,958; and 19,959. However, as mentioned previously, the Memory Out of FIG. 20 selects the character from the Memory Buffer Register for processing which corresponds to the units position of the address in the Memory Address Select Register. Accordingly, the address of 19,955 specifies character "zero" to be read from the Memory Buffer Register. In this regard, the Memory 4×5 Decoder of FIG. 3*e* determines which of the characters shall be selected according to the units position of the Address. The $\overline{8}$ line **49***a*.**02**, the $\overline{2}$ line **49***a*.**11**, the 4 line **49***a*.**08** and the 1 line **49***a*.**17** are up. These signals are decoded to provide an output on Select Character 0 line **3***e*.**01** which goes to the Memory Output Select, FIG. 20*a*. In FIG. 20*a* assume, for the present, that low character line **36***b*.**04** and high character line **36***b*.**06** are down, in which case the Normal line from the OR circuit, the Inverter, and the two cathode followers is up which gates the Select Character 0 line **3***e*.**01** to provide an output on Select Character 0 Out line **20***a*.**04**. The latter line goes to Output Switch (Characters 1 and 0) of FIG. 20*b* where the character 0 lines **14***b*.**06** (C) through **14***b*.**06**(1) from FIG. 14*b*, are gated with the Select Character 0 Out line **20***a*.**04** to provide outputs on the C bit line **20***b*.**01**, B bit line **20***b*.**02**, A bit line **20***b*.**03**, 8 bit line **20***b*.**04**, 4 bit line **20***b*.**05**, 2 bit line **20***b*.**06** and the 1 bit line **20***b*.**07**, for those positions of character 0 containing binary "ones." The Memory Out Bus of FIG. **20***d* receives the character 0 signals which are passed through on the lines **20***d*.**01** through **20***d*.**07** to CR 1, FIG. 57, where they are gated to the triggers by the Set CR 1 pulse (D0.4) on the line **100.02** to set the triggers according to the bit configuration of the character 0.

What has been described in the example of Reading from and Writing into Memory concerns a R/W cycle of 9 microseconds, but it will be appreciated that a similar operation occurs during an Instruction cycle of 13 microseconds. In FIG. 145, the sequence of events will be recognized as the one of FIG. 144 except that the period A_0 through A_3 has been inserted between R_4 and W_0. The time $A_{3.5}$ of FIG. 145 corresponds to $R_{4.5}$ of FIG. 144.

In the foregoing example where the address 19,955 was employed, it will be appreciated that the address is improper for an Instruction since only character 0 was addressed and all Instruction addresses must end in either a 4 or a 9.

GENERAL DESCRIPTION OF AUXILIARY AND ACCUMULATOR STORAGE

As mentioned previously, Auxiliary and Accumulator Storage provide 512 character positions of Storage, divided into one 256 character capacity Accumulator unit, fourteen 16 character capacity Auxiliary Storage units and one 32 character capacity Auxiliary Storage unit. The addresses for Auxiliary Storage units are 0 through 255 inclusive, and the addresses for Accumulator Storage are 256 to 511 inclusive. Only one character position in Accumulator or Auxiliary Storage can be addressed during one cycle, and it follows that Auxiliary and Accumulator Storage cannot be used simultaneously.

Since seven Core Planes such as the one shown in FIG. 45 are used in the Storage Array, seven ferrite cores (one for each core plane) are interrogated each cycle when reading Storage. Each Storage core plane comprises a 16×32 matrix (FIG. 45), interrogated by Y inputs comprising 16 address lines and X inputs comprising 32 address lines. The Storage Address Select Register, FIGS. 53*a* and *b*, is set only from the Storage Address Counter, FIGS. 52*a* through *d*, with a pulse at R_0 time that occurs at the same time that the Memory Address Register is set to the Memory Address Counter 1. The Address of the Storage Address Select Register is immediately decoded in the four decoders, namely, the 2×4 Decoder, FIG. 34*a*; the 2×4 Decoder, FIG. 34*b*; the 2×4 Decoder, FIG. 34*c*; and the 3×8 Decoder, FIG. 34*d*. The decoder outputs are mixed with Read Bias, Read and Write Gates to control the Switch Core Matrices of FIGS. 39 and 35. The Y Switch Core Matrix, FIG. 39, contains sixteen switch cores in a 4×4 array and the X Matrix, FIG. 40, contains thirty-two switch cores in two 4×4 arrays and on a Read operation, one X and one Y switch core are selected from the X and Y Switch Core Matrices respectively. These two matrices selectively energize the sixteen Y Address lines and thirty-two X Address lines which are provided in parallel to the seven planes of the Storage Array for which FIG. 45 is a sample plane.

Each core plane, such as the one illustrated in FIG. 45, has a Sense Winding linking all cores of the plane and each Sense Winding feeds a one of seven Sense Amplifiers of FIG. 46. During Reading, the Sense Amplifier outputs are sampled to place the character into the seven character capacity Storage Buffer Register, FIG. 47. One set of Storage Buffer Register output lines is connected to CR 2, FIG. 48, via the Storage Out Bus, and another set of output lines is connected to the Storage In Select and Switching Circuits, FIG. 43. Two possibilities exist for writing a character into Accumulator Storage: (1) The character retained in the Storage Buffer Register may be rewritten into Storage at the Address from which it was taken, or (2) the Result character from the Result Register available on the Storage In Bus may be written into Storage. The line which selects one or the other of the previously mentioned characters is the Result to Storage line **137.05**, and if Result Storage line is down, the Storage Buffer Register character is gated to the Input Switch of FIG. 43 for rewriting into Storage; otherwise, with the Result to Storage line up, the character on the Storage Bus from the Result Register is gated through the Input Switch and written into Storage.

The Storage Address Select Register of FIGS. 53*a* and *b* comprises triggers 1, 2, 4, 8, 16, 32, 64 and 128, having a capacity to store any Address 000 through 255. This is adequate to address the Auxiliary Storage positions; however, to permit addressing Accumulator Storage (256 through 511), the SASR 256 line **54.24** is required. This line **54.24** originates in Storage Select Register Decoding, FIG. 54, and is under the control of the Storage Select Register Triggers, FIG. 16*a*, lines **16***a*.**24**, **16***a*.**17**, **16***a*.**16** and **16***a*.**03**.

The Storage Select Register Triggers of FIG. 16*a* are set during Instruction cycles according to the zoning over the tens and hundreds position of characters 2 and 3 of the Instruction. With no zoning present, the Accumulator Storage is addressed, and, in this case, the four Storage Select Register triggers of FIG. 16*a* are Off, and the Storage Address Select Register 256 line **54.24** and the SSR=0000 lines are up. If the address contains zoning in the tens and hundreds order, Auxiliary Storage is addressed, in which case, one or more of the SSR triggers will be On thereby causing the 256 line 54.24 to be down and the $\overline{256}$ line **54.01** and the SSR≠0000 lines to be up. If the 256 line is up, the Storage position addressed will be 256 plus the address in the Storage Address Select Register, which addresses will be in Accumulator Storage. If the $\overline{256}$ line **54.01** is up, only the address held in the Storage Address Select Register is interrogated and Auxiliary Storage is addressed.

The 256 line **54.24** and the $\overline{256}$ line **54.01** go to Storage Decoding System of FIG. 34*a*, where they are mixed with the Storage Address Select Register 128 line **53***b*.**08** and the SASR $\overline{128}$ line **53***b*.**07**. The SSR=0000 lines of FIG. 54 allow SAC to be set to SPC, and identifies Instructions which have no bits in the zone portions of characters 2 and 3. SSR≠0000 allows the four high order

positions of SAC to be set by SSR and resets to "zero" the four low order positions of SAC. When SASR is set to SAC and combined with SASR $\overline{256}$, the units position of the proper Auxiliary Storage Unit is selected. In FIG. 34*a*, if Auxiliary Storage is addressed either 000 line **34***a*.**01** or 128 line **34***a*.**02** will be up, because the 256 line **54.24** is down. With the 256 line **54.24** up for addressing Accumulator Storage, either the 256 line **34***a*.**03** or 384 line **34***a*.**04** will be up. The Read Bias, Read and Write currents occur essentially in the same timing relation as those generated for Core Memory; however, duplicate generators are required because Storage and Memory may be used either simultaneously or individually and controlled accordingly.

The X and Y Switch Core addresses are each obtained by adding the numbers of the intersecting Drive lines in FIGS. 39 and 40. The addition of the X and Y Switch Core addresses so obtained produce the number contained in the Storage Address Select Register that causes the selection of the character as that address in Storage.

STORAGE ARRAY

Seven core planes such as the one shown diagrammatically in FIG. 45 plus a dummy plane make up the Storage Array. The core planes are designated C, B, A, 8, 4, 2 and 1 according to the bit position which they individually store. The dummy plane is used for connection purposes only. The X and Y Address lines link rows and columns of cores in Storage as explained with reference to Core Memory so that for each character address a particular core in each of the seven planes is interrogated to provide binary indications for seven bits of a character. Each of the thirty-two X Address lines and sixteen Y Address lines form one closed loop including the secondary winding of the appropriate switch core for each address line and the selected core is at the intersection of a driven X and a driven Y line as explained with reference to operation of Memory. Since the Storage Array is functionally, but not physically, divided into two parts, the division is effected along the Y axis by assigning to Accumulator Storage the Y lines from 256 to 480 inclusive and assigning to Auxiliary Storage the Y lines from 0 to 224 inclusive (see top of FIG. 45). Auxiliary Storage Unit 1 uses positions 16 through 31 of the Y Address line 0; Auxiliary Storage Unit 2 uses positions 0 through 15 of the Y Address line 32; Auxiliary Storage Unit 15 uses positions 16 through 32 of the Y Address line 224 and positions 0 through 15 of the Y Address line 0. The operation of Accumulator Storage utilizing a particular address follows.

OPERATION OF STORAGE

Normal operation of Storage is best illustrated by example assuming a particular address such as Unit 6 of Auxiliary Storage which is addressed by a "one" in the A bit position of character 2 and a "one' in the B bit position of character 3.

Referring now to the Storage Select Register of FIG. 16*a*, the SSR—4 and SSR—2 triggers are turned On via MBR Character 2–A line **14***a*.**02**, MBR Character 3–B line **14***a*.**02**, and the A_0 (D0.4) I time line **101.24**. With this setting of the SSR triggers, the SSR—8 Off lines **16***a*.**01** and **16***a*.**02**, the SSR—4 On lines **16***a*.**10** through **16***a*.**13**, the SSR—2 On lines **16***a*.**17** through **16***a*.**20** and the SSR—1 Off lines **16***a*.**21** through **16***a*.**23** are up. In FIG. 54, lines **16***a*.**17** and **16***a*.**16** are up, so the SASR $\overline{256}$ line **54.01** and the SSR≠0000 lines **54.02** through **54.08** are up. As mentioned previously with respect to FIG. 2, On and Off output lines from each position of SSR are connected to positions 128, 64, 32 and 16 of SAC, FIG. 52. In FIGS. 52*d*, SSR—1 Off line **16***a*.**23**, SSR—2 On line **16***a*.**20**, SSR—4 On line **16***a*.**13** and SSR—8 Off line **16***a*.**02** are up. Upon the occurrence of a pulse on the Set SAC to SSR line **52***e*.**06** at W_1, the Set SAC—$\overline{16}$ line **52***d*.**01**, Set SAC—32 line **52***d*.**04**, Set SAC–64 line **52***d*.**06** and Set SAC—$\overline{128}$ line **52***d*.**07** are up to FIG. 52*c* where the SAC triggers 64 and 32 are turned On and the SAC triggers 16 and 128 are turned Off if On previously. Since the SPC is not used when addressing Auxiliary Storage, the four lower order positions of SAC are reset Off by the Set SAC to SSR line **52***e*.**07** from SAC controls of FIG. 52*e*, which results from signals on the I time line **124.33**, SSR≠0000 line **54.02**, A_2/R_3–W_1 (Use) line **103.06** and Set SAC to SPC line **93***j*.**08**.

The outputs of SAC are used to set the SASR at R_0 time of each Execute cycle. Therefore, the address in SAC can be altered during each cycle in preparation for the next cycle while SASR holds the location of the character being processed. In FIG. 53*a*, all of the SASR triggers are turned Off by the SAC—$\overline{1}$, SAC—$\overline{2}$, SAC—$\overline{4}$ and SAC—$\overline{8}$ lines being up when the R_0 (D0.4) pulse appears on the line **101.06**. In stages 5–8 of SASR, FIG. 53*b*, the 32 and 64 triggers are turned On by the SAC—32 line **52***c*.**05** and the SAC—64 line **52***b*.**07** at R_0 (D0.4). The 16 and 128 triggers are turned Off at the same time via the SAC—$\overline{16}$ line **52***c*.**02** and the SAC—$\overline{128}$ line **52***b*.**08**.

In the 2×4 Decoder of FIG. 34*b*, the SASR—64 line **53***b*.**06** and the SASR—32 line **53***b*.**04** are up causing the **96** line **34***b*.**04** to be up. In FIG. 36*a*, the signal on the **96** line **34***b*.**04** is inverted to bring down the $\overline{96}$ line **36***a*.**04**. Since the 00 line **34***b*.**01**, the 32 line **34***b*.**02**, and the 64 line **34***b*.**03** are down, the $\overline{00}$ line **36***a*.**01**, $\overline{32}$ line **36***a*.**02** and the $\overline{64}$ line **36***a*.**03** are up. In FIG. 36*b*, the last mentioned lines are combined with Storage Read Bias Gate on line **7***d*.**02** to provide positive signals on the output lines **36***b*.**01**, **36***b*.**02** and **36***b*.**03** at R_0. The 96 line **34***b*.**04** is not gated at this time since the Storage Write Gate on line **7***d*.**08** is down at this time. In FIG. 39, reset current flows through the columns linked by the lines **36***b*.**01**, **36***b*.**02** and **36***b*.**03** and is fed back to FIG. 36*b* on the lines **39.04**, **39.03** and **39.02**.

In the 3×8 Decoder of FIG. 34*d*, the SASR $\overline{4}$ line **53***a*.**05**, the SASR $\overline{2}$ line **53***a*.**03** and the SASR $\overline{1}$ line **53***a*.**01** are up providing a positive signal on the Decimal $\overline{0}$ line **34***d*.**01** to FIG. 38*a*, where the output $\overline{0}$ line **38***a*.**01** is brought down. The remaining output lines are up because of Inverters since their inputs are down. The output signals of FIG. 38*a* are provided to the Storage X Switch Core Write Drivers of FIGS. 38*b* and *c* whereupon at $R_{0.5}$ the Storage Read Bias Gate Even on line **42.03** provides outputs on the 2 line **38***b*.**03**, 4 line **38***e*.**01** and 6 line **38***c*.**03**. The Storage Read Bias Gate Even is derived from Odd and Even Gating circuits of FIG. 42 where the SASR $\overline{1}$ line **34***d*.**10** and Storage Read Bias Gate line **7***d*.**01** are combined. In FIG. 40, the X Switch Core Matrix, the columns linked by the 6 line **38***c*.**03**, the 4 line **38***c*.**01** and the 2 line **38***b*.**03** are driven by reset current which is fed back to FIGS. 38*b* and *c* on the lines **40.07**, **40.05** and **40.03**.

In FIG. 34*a*, the SASR $\overline{128}$ line **53***b*.**07** and SASR $\overline{256}$ line **54.01** are positive as previously described bringing up the 000 line **34***a*.**01**, the latter going to the Y Switch Core Read Drivers of FIG. 37. In FIG. 37, the Storage Read Gate is provided on the line **7***d*.**03** at R_1 and, as a result, the 000 output line **37.01** is made positive to drive the 000 row of the Y Switch Core Matrix of FIG. 39 with set current and provide feedback to FIG. 37 on the line **37.08**. Since reset current is being applied on the 00 line **36***b*.**01**, the 32 line **36***b*.**02** and the 64 line **36***b*.**03** and set current is now supplied on the line **37.01**, the Switch Core at the intersection of the 96 line **36***b*.**04** and 000 line **37.01** is set causing an output on the secondary winding **96** to the Storage Array of FIG. 45.

In FIG. 34*c*, Storage 2×4 Decoder, the SASR $\overline{16}$ line **53***b*.**01** and the SASR $\overline{8}$ line **53***a*.**07** are up providing a positive signal on the 0 line **34***c*.**01** to the X Switch Core

Read Drivers of FIG. 35. In the latter figure, the 0 Even output line **35.01** is brought up at $R_{1.5}$ by the line **34***c*.**01** and the Storage Read Gate Even line **42.04**. In FIG. 40, the 0 Even line **35.01** furnishes set current to the cores linked thereby and feedback current to FIG. 35 on the line **40.16**. Since reset current is flowing in the 6 line **38***c*.**03**, the 4 line **38***c*.**01** and the 2 line **38***b*.**03** and set current is flowing in the 0 Even line **35.01**, the core at the intersection of the lines **38***b*.**01** and **35.01** is set causing an output in the secondary winding 0.

In FIG. 45, half-select currents in directions for changing the state of a core from "one" to "zero" are flowing through the 0 and 96 lines in each of the seven planes of which FIG. 45 is a sample. Accordingly, for each plane containing a binary "one" an output is provided on the Sense Windings to the Sense Amplifiers of FIG. 46.

The Sense Amplifiers of FIG. 46 are biased by the line **5***h*.**11** and provide positive outputs on those lines where corresponding cores switch from "one" to "zero." The outputs, if any, on the C, B, A, 8, 4, 2 and 1 lines **46.01** through **46.07** are furnished to the Storage Buffer Register, FIG. 47, where signals indicating binary "ones" are gated to turn On the corresponding triggers by the Sample Pulse on line **5***i*.**01** at $F_{3.5}$.

The contents of either the Storage Buffer Register or the Result Register may be written back into the same address in Storage during the Write position of the R/W cycle. Assume as an illustration that the bit configuration contained in the Storage Buffer Register of FIG. 47 is to be written into Auxiliary Storage unit 6 (location 96) which is the same address read from previously. In the same manner as explained with reference to Memory, half-select currents are applied to each core plane on the X and Y drive lines in a direction such that binary "ones" are written into the specified address in all bit positions except those where inhibit current is provided as a result of positions in the SBR containing binary "zeros." In this regard, the Off sides of the triggers of SBR, FIG. 47, are used by connecting the lines **47.01** through **47.07** to the Input Switch of FIG. 43. In FIG. 43, the Result to Storage line **137.05** is down (the unused line is always up) and the Inverter associated therewith supplies a positive voltage to the Add circuits fed by the input lines from SBR. Those output lines, among the group lines **43.01** through **43.07**, are up for each bit position of SBR which contains a "zero." In FIG. 44, the indications of the "zeros" in the SBR are received and gated by the Storage Inhibit Gate line **7***d*.**05** at $R_{4.5}$ to FIG. 45 where the Inhibit winding of each plane in which "zeros" are to be written is driven.

In FIGS. 36*a*, the lines **36***a*.**01**, **36***a*.**02**, **36***a*.**03** are up but cannot be gated to the Y Switch Core Windings of FIG. 39 via the Y Switch Core Write Drivers of FIG. 36*b* since the Storage Read Bias Gate line **7***d*.**02** is down. However, the 96 line **34***b*.**04** is up, and at W_0 the Storage Write Gate on the line **7***d*.**08** brings up the 96 line **36***b*.**04** to FIG. 39 where it provides reset current to the cores 96, 224, 352 and 480. The 96 core is the only one previously set and, therefore, the only one reset to provide an output from its secondary.

In FIG. 41, the 0 line **41.01** is up to the X Switch Core Write Drivers of FIG. 38*b*. In FIG. 7*e*, the output line **7***e*.**04** is up because of the Inverter, and in FIG. 7*d*, the Storage Write Trigger has been turned On by Read Storage line **93***a*.**02** and R_5 or A_4 (W_0) bringing up the Storage Write Gate lines **7***d*.**06** through **7***d*.**08**. Referring now to FIG. 38*b*, the 0 line **41.01** from FIG. 41 is gated by lines **7***e*.**04** and **7***d*.**06** to drive the 0 line **38***b*.**01** thereby providing reset current to the 0, 8, 16 and 24 cores of the X Switch Core Matrix of FIG. 40. In the latter figure, the 0 core was set to "one" during Read time and is now reset by the **38***b*.**01** line providing an output signal on the secondary coil 0. Referring once again to FIG. 45, half-select current is flowing in both the Y winding 96 and the X winding 0 tending to set the fully selected core in each plane to a "one," but, inhibit current prevents such a setting in those planes where a "zero" should be written according to the setting of the SBR as described previously.

Assume now that it is desired to read from an address in Accumulator Storage. The B and A bit positions of characters 2 and 3 of the Instruction address are "zeros" and, therefore, the SSR contains "zeros." Whether an Instruction cycle or an Execute cycle, the SPC determines the Accumulator address. For this example, an address of 356 set in the SPC will be used.

In FIG. 16*a*, Storage Select Register, the four triggers are Off because of the absence of zone bits in the Accumulator address coding and accordingly, in FIG. 54, the SSR=0000 and SASR 256 lines are up since SSR—1 On line **16***a*.**24**, SSR—2 On line **16***a*.**17**, SSR—4 On line **16***a*.**16** and SSR—8 On line **16***a*.**03** are all down. It is the SASR 256 line **54.26** in this instance that addresses the Accumulator generally since the SPC can only count from 0 to 255 (Recall addresses 0 through 255 are in Auxiliary Storage). Therefore, the SPC contains a count of 100 which, in effect is added to 256 to address location 356 in Accumulator Storage.

The SPC of FIGS. 51*a*, *b* and *c* contain a count of 100 so SPC—$\overline{1}$ line **51***a*.**01**, SPC—$\overline{2}$ line **51***a*.**03**, SPC—4 lines **51***a*.**06** through **51***a*.**07**, SPC—$\overline{8}$ line **51***b*.**01**, SPC—$\overline{16}$ line **51***b*.**03**, SPC—32 lines **51***b*.**06** through **51***b*.**08**, SPC 64 line **51***c*.**02** and SPC—$\overline{128}$ line **51***c*.**03** are up. These signals are provided to SAC, FIGS. 52*b* and 52*d*, to turn On the 64, 32 and 4 triggers and turn Off the remaining triggers when the Set SAC to SPC pulse is provided on the lines **52***e*.**04** and **52***e*.**05**. In FIGS. 53*a* and *b*, SASR, the SAC—$\overline{1}$ line **52***a*.**01**, the SAC—$\overline{2}$ line **52***a*.**03**, the SAC—4 line **52***a*.**06**, the SAC—$\overline{8}$ line **52***a*.**07**, the SAC—$\overline{16}$ line **52***c*.**02**, the SAC—32 line **52***c*.**05**, the SAC—64 line **52***b*.**07** and the SAC—$\overline{128}$ line **52***b*.**08** are up and at R_0 (D0.4) the lines **101.07** and **101.06** set SASR to the contents of SAC. The SASR now contains the value 100.

The principles of reading and writing into address 356 are the same as those described in the example pertaining to Auxiliary Storage and will not be repeated. From the description above, the differences of addressing Accumulator and Auxiliary Storage are apparent.

CHARACTER REGISTERS

At A_0 or W_0, a character read out of Memory is set into Character Register 1 of FIG. 57 where it remains until A_0 or W_0 of the next character cycle. Since CR 1 is not provided with a reset to "zero," a new character is merely written "over" the previous character at set time. At W_0, a character read out of Storage is set into Character Register 2 of FIG. 48 where it remains until W_0 of the next character cycle when another character may be set into the CR 1 triggers. Storage is not read from during Instruction cycles so provision is not made for setting CR 2 at A_0 as in the case of CR 1.

Refer now to the CR 1 circuits of FIG. 57. The circuits for Storage of each bit in a trigger are identical and only the details of the circuits for the 1 bit position of the character will be described.

If a binary "one" is contained in the 1 bit position of a character read from Memory and to be entered in CR 1, the Memory Out Bus 1 line **20***d*.**07** is positive to condition one input of a gate (GJ) for the left side of the 1 trigger which passes the Set CR 1 signal on a line **100.02** to turn On the 1 trigger bringing up the CR 1–1 line **57.15**. If a binary "zero" has been read out of Memory instead, the Memory Out Bus–1 line **20***d*.**07** is down, but the output of an Inverter (IK) is up to condition a diode gate (GJ) for the right side of the 1 trigger. Thus, the Set CR 1 pulse on line **100.02** sets the 1 trigger to "zero," and the CR 1–$\overline{1}$ line **57.14** is made positive.

The 1 trigger, when On, provides a positive signal on

the CR 1–1 line **57.15** to the Right Plate Outputs of FIG. 58, and the 1 trigger, when Off, provides a positive signal on the CR 1–$\bar{1}$ line **57.14** to the Left Plate Outputs of FIG. 59.

The circuits of Character Register 2 of FIG. 48 are similar to those shown and described for Character Register 1 and the description will not be duplicated.

ADDER INPUT SWITCHING

In FIG. 73, the output signals representing the numeric portions of the character in CR 1 are present on the CR 1–8 line **58.37**, CR 1–2 line **58.47**, CR 1–4 line **58.42** and CR 1–1 line **58.52**. For those bits in Character Register 1 which contain binary "ones," positive signals are present on these respective lines. The Zone bits, A and B, of CR 1 are fed from CR 1 Right Plate Outputs to Adder Input switching on the CR 1–A line **58.23** and the CR 1–B line **58.06** respectively where the zone bit lines are gated by the CR 1 to Adder line **93***b*.**01** onto the output lines **73.01** and **73.08** to the Zone Adder of FIG. 79.

If the contents of CR 1 are not "zero" as signified by the CR 1≠0 line **71***b*.**11** being positive or the machine is executing a Set Bit instruction as indicated by the Set CR 1≠ line **23***l*.**01** being positive, then, as the CR 1 to Adder line **93***b*.**01** goes positive, those AND circuits which are otherwise conditioned furnish positive output signals to FIGS. 80, 81 and 82 on the CR 1 to Adder (A) line **73.01**, CR 1 to Adder (8) line **73.02**, CR 1 to Adder (2) line **73.03**, CR 1 to Adder (4) line **73.04**, CR 1 to Adder (1) line **73.05** and CR 1 to Adder (B) line **73.08**. The Minus on Suppress 8 bit to Adder line **93***d*.**04**, Minus on Suppress 2 bit to Adder line **56***b*.**06**, Minus on Suppress 4 bit to Adder line **56***b*.**07**, Minus on Suppress 1 bit to Adder line **56***b*.**05**, are normally positive to condition their respective AND circuits. In those instances where it is desired to suppress a bit, one of the lines just mentioned is down, thereby prohibiting the passage of the signal through one AND circuit to the output lines. When the contents of CR 1 equals zero (CBA8421=0001010), provision is made for changing the 8 and 2 bits to "zero." The AND circuits controlling the 8 and 2 bits are conditioned by the CR1≠zero line **71***b*.**11**, and when this line is down (indicating CR 1=0), the 8 and 2 bits are not passed but are blocked from the output thereby making all bits of the character "zero" for numeric processing within the ALU.

When CR 1 holds a value greater than 10 during a Compare instruction, the 8 bit from CR 1 must be blocked, and this is accomplished by bringing down the (—) On Suppress 8 bit to Adder line **93***d*.**04**.

The lower portion of FIG. 73 illustrates circuits for switching either the numeric contents (8, 4, 2, 1 bits) of CR 1 or the numeric contents of CR 2 to the True/Complement Controls of FIG. 83 via OR circuits having gated inputs from the numeric portions of CR 1 and CR 2. When CR 1 to T/C line **93***b*.**03** and CR 1≠0 line **71***b*.**12** are positive, the numeric contents of CR 1 are gated onto the output lines **73***b*.**09** through **73***b*.**14**. When CR 2 to T/C line **93**.*b*.**04** and CR 2≠0 line **76.22** are positive, the numeric contents of CR 2 are gated onto the output lines.

Although a character in which the bits are all "zero" (Storage Marks) is a legitimate character in CR 2, "zero" expressed as a character (0001010) is not processed in the ALU and must be converted to all "zero" bits. Accordingly, the CR 2≠0 line **76.22** is brought down to block the 8 and 2 bits from the output of Adder Input Switching when CR 2=0.

MULTIPLICATION

As mentioned previously, multiplication is accomplished by means of a multiple generator shown generally in the Multiply circuits **1.20** and Multiply Register **1.40**, in FIG. 1. More specifically, the foregoing circuits are shown in FIGS. 2*cc*, 2*dd*, 2*rr*, 2*ss*, 2*ggg* and 2*hhh*, comprising a Multiplicand Doubler and Quadrupler, FIG. 80, a Quintupler, FIG. 81, Multiple Selection Circuits, FIG. 82, Multiple Register, FIG. 78, Multiple Adder of FIG. 84, and Decimal Correction Circuits, FIG. 85. The Multiple Generator provides multiples of each digit of the Multiplicand, specifically, one times, two times, four times and five times the digit contained in Character Register 1. Proper multiples are selected in the Multiple Selection Circuit of FIG. 82 which is controlled by Multiple Register and Decoder of FIG. 82, the latter containing the digits of the Multiplier derived from CR 2. After selection, the multiples of the digit are added in the Multiple Adder of FIG. 84 and are then passed through Multiple Adder Correction Circuits, FIG. 2*ggg* (FIG. 85), to the Digit Adder. In the Digit Adder the sum of the multiples are added to digits of the previous partial product.

Since a doubled, quadrupled or quintupled multiple of a multiplicand digit may produce a carry, means are employed to store the carry so that they may be added to the generated multiples of the succeeding higher order digit during the next character cycle, FIGS. 2*cc* and 2*dd*. More specifically, in FIGS. 80 and 81, doubled, quadrupled and quintupled values of each digit gated from Character Register 1, are generated whether or not multiplication is being performed. The Multiplier Control circuits contain the Multiple Register, FIG. 78, which during multiplication contains a multiplier digit, but is otherwise reset to represent the value of decimal 1, and thereby is effective as explained hereafter to gate a one times multiple for operations other than Multiply.

In FIG. 80, Multiplicand Doubler and Quadrupler (2 sheets) the Doubler portion comprises the lower portion of Sheet 1 of FIG. 80 where inputs from CR 1 to Adder are shown entering on the left. The two multiple is derived from the output lines **80.02** through **80.05**. The Doubler emits signals representing the double valve of the character input thereto which signals are emitted to the Multiple Selection circuits of FIG. 82 and also the Quadrupler circuits of Sheet 2 of FIG. 80. The Quadrupler is, in effect, another doubler, so that upon doubling the doubled value a quadruple value is produced. Operation of the Multiply circuits is set forth in detail in the application "Electronic Multiplier," Serial No. 512,636, filed June 2, 1955, and assigned to the assignee of this application.

TRUE/COMPLEMENT CONTROLS

Referring to FIG. 83, the True/Complement Control circuits are shown consisting of switching circuits necessary to generate a 9's complement of the input thereto and also to gate either the True of Complement representation of the particular digit to the Digit Adder of FIG. 86. The input signals to the T/C Control circuits are emitted from the Adder Input Switching circuits, described above, and may represent characters from either Memory or Storage.

The 9's complement of a digit is that digit when added to the digit being complemented which results in a sum of 9. Consider the example where the digit 3 (0011) is complemented to result in 6 (0110). In this instance, the input T/C–2 line **73.11** and the 1 to T/C line **73.13** are positive and the 8 to T/C line **73.09** and 4 to T/C line **73.10** are negative. When the Complement line **93***d*.**07** goes positive, the T/C–4 line **83.03** and the T/C–2 line **83.04** become positive. However, if the Complement line is negative, the line **83.01** is positive and the True signals are passed unmodified on the lines **83.04** and **83.05** to the Digit Adder, FIG. 86. It will be noticed that the T/C–2 line **83.04** passes directly from input to output since the binary "ones" or "zeros" for the 2 bit are the same in both True and Complement form.

DIGIT ADDER

The Digit Adder is shown in FIG. 86 and adds digits (parallel by bit and serial by digit) from CR 2 via Adder

Input Switching (FIG. 73) and True/Complement Controls (FIG. 83) and from CR 1 via Adder Input Switching (FIG. 73), Multiple Selection (FIG. 82), Multiple Adder (FIG. 84) and Decimal Correction circuits (8, 4 and 2 bits only) (FIG. 85). In FIG. 86, the Digit Adder comprises four full binary adders connected in combination so that the sum of two binary coded decimal digits may be obtained. A carry from each binary order is connected to an input of the succeeding higher order except for the "one" bit carry input which is a decimal carry resulting from the previous addition of the succeeding lower order of BCD digits. Each full adder has three inputs, a pair for corresponding bit values of the digits to be added and a carry input, for example, MPL 4 line **85.03**, T/C–4 line, and Binary Sum 2 Carry line. If binary "zeros" are applied at all three inputs, both sum and carry outputs are binary "zeros." When one input only contains a binary "one," the sum output only contains a binary "one." When any two inputs simultaneously contain binary "ones," the carry output only contains a binary "one." When all three inputs contain binary "ones," both sum and carry outputs contain binary "ones." The full adder circuits are conventional and their operation is so well known to those skilled in the art that a description of their operation is unnecessary.

The arithmetic circuits of the ALU cannot perform subtraction directly but achieve the same result by complementary addition. The True/Complement Control circuits of FIG. 83 produce only the 9's complement, and the 10's complement is required in the units order of the field being added to arrive at the correct result. Consider the following example:

The number 14 is to be subtracted from the number 48 which should give a result of 34. Accordingly, the 9's complement of 14, which is 85, is added to 48.

```
 48
 85
 --
 33 (carry neglected)
```

Since the 10's complement of a digit is the 9's complement plus 1, addition of 1 to 33 provides the required answer of 34. Therefore, when subtracting, a decimal carry is supplied to the Digit Adder on the line **93***d*.**05** during the first Execution Character Cycle (ECC 1).

The output of the entire Digit Adder, comprising four full binary adders, may represent a sum of 0 through 19. A sum of 19 would result from the addition of digit 9 (lines **85.05** and **84.01** positive) and digit 9 (lines **83.02** and **83.05** positive) plus a carry from a succeeding lower order on the Decimal Carry In line **88.23**. Because the Digit Adder is a pure binary adder, correction is necessary since the sum must be represented in the BCD form. The correction is provided by the Decimal Correction circuits of the Digit Adder of FIG. 87.

As stated previously, the character from Memory to be added is passed unmodified through CR 1 (FIG. 2*h*), Adder Input Switching (FIG. 2*qq*), Multiple Selection Circuits (FIGS. 2*rr*–2*ss*), Multiple Adder (FIG. 2*hhh*) and Multiple Adder Decimal Correction Circuits (FIG. 2*ggg*) to the Digit Adder (FIG. 2*eee*). In FIG. 78, the Multiple Register triggers are Instruction reset to the value "one" with the trigger at the top of the drawing having is left side in conduction and the remaining triggers having their right sides in conduction. Thus, the Select 1 Multiple line **78.01** is positive throughout the addition. In FIG. 82, the last-mentioned line gates the signals from CR 1 on the lines **73.05**(1), **73.03**(2), **73.04**(4) and **73.02**(8) onto the output lines **82.01** through **82.04**. In FIG. 84, the value represented by the signals present on the MPL–1B line **82.04**, MPL–2B line **82.03**, MPL–4B line **82.02** and MPL–8B line **82.01** is, in effect, added to zero and passed to the output lines **84.01** through **84.05** and, in turn, to the Decimal Correction circuits. In FIG. 85, if the Multiple Register contains a "zero" or a "one" as indicated by the MPL Reg $\neq 0/1$ line **98.05** being down, the Correction circuits are blocked, the MPL Carry Out line is down, the No MPL Carry Out line is up, and the digit value is passed to the output lines **85.01** through **85.06**. The latter lines are connected as inputs to the Digit Adder of FIG. 86 and the Set Bit Routing Controls of FIG. 56*a*.

DECIMAL CORRECTION CIRCUITS, DIGIT ADDER

Chart IV below shows all of the inputs and outputs of the Digit Adder. It can be seen that any sum greater than nine must be corrected and that any sum equal to, or greater than, 16 produces a carry from the 8 bit adder on the lines **86.08** and **86.09**.

Chart IV

Dec Sum of Input		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
Output of Adder		Bi 8 Carry															→	1	1	1	1
	8	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0
	4	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0	0	0	0
	2	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
Output of Correction Circuits		Dec Carry Out										1	1	1	1	1	1	1	1	1	1
	8	1	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	1	1
	4	0	0	0	0	1	1	1	1	0	0	0	0	0	0	1	1	1	1	0	0
	2	1	0	1	1	0	0	1	1	0	0	0	0	1	1	0	0	1	1	0	0
	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1

In FIG. 87, circuits are arranged to correct a digit represented by signals on the input lines **86.02**, **86.04**, **86.06** and **86.01** for the present cycle when the Digit Adder Out line **93***c*.**01** is made positive. Assume the decimal sum of the Adder is 12 as signified by the inputs on Binary Sum 8 line **86.06** and a Binary Sum 4 line **86.04** being positive and the Binary Sum 8 Carry line **86.08** being down. The Decimal Carry Out line **88.02** to FIG. 87 is positive because in FIG. 88 the Binary Sum 4 line **86.05**, Binary Sum 8 line **86.07** and (—) On Suppress Adder Carry line **93***d*.**01** are up. On Sheet 2 of FIG. 88 it will be observed that the positive signal on Decimal Carry Out lines **88.01** through **88.05** is inverted by IJK to make the lines **88.06** through **88.12** negative. Thus, in FIG. 87, the Binary Sum 8 and 4 signals are blocked by the No Decimal Carry Out line **88.07**, while the negative signal on the Binary Sum 2 line **86.02** is inverted and gated by the positive Decimal Carry Out line **88.02** to bring up the Result 2 lines **87.01** through **87.04**. In this manner, the 8 and 4 bit signals are corrected to a 2 bit signal (see Chart IV). Of course, cor-

rection of the value 12 requires that a carry be generated and preserved for use in the next cycle.

In FIG. 88 (Sheet 2), the positive signal on the lines **88.01** through **88.05** is directed to the gate (GJ) associated with the left side of the Decimal Carry trigger of FIG. 88 (Sheet 1). The gate is further conditioned by a positive signal on the MPY 2/NOT Transition line **67***d*.**15**, and at W_0 the line **101.11** goes positive and places the left-hand side of the Decimal Carry trigger in conduction. Therefore, the Decimal Carry In lines **88.23** through **88.32** of FIG. 88 (Sheet 2) go positive. During the next cycle, the Decimal Carry In signal on line **88.23** is used as the Carry In to the 1 bit Adder of FIG. 86 where it is added to the next digits.

In FIG. 88 (Sheet 1), the (—) On Suppress Adder Carry line **93***d*.**01** is brought down to block the AND circuits it feeds and thereby prevents the Decimal Carry Out line **88.02** (among others) from coming up. Thus, in FIG. 87, the line **88.02** is down and the No Decimal Carry Out line **86.06** is up permitting combinations of bits greater than 9 to pass to the output Result lines without being corrected. Such an operation is required in Load and Unload instructions where, for example, a $ sign having a numerical portion of the value 11 must pass through the Digit Adder and Decimal Correction circuits unchanged.

A zero output (8421=0000) from the Digit Adder must be converted to a decimal 10 (8421=1010) before entry in Memory or Storage, and this conversion is done in the Decimal Correction circuits of FIG. 87 by recognizing no bits from the Digit Adder. In the lower portion of FIG. 87, an OR circuit is fed by Sum-1, Sum-2, Sum-4 and Sum-8 lines to provide a Digit Adder Output ≠0 indication by a positive signal on the lines **87.17** through **87.23**. When none of the inputs to the OR circuit are positive, the last mentioned lines are negative, but the inverter (I) gates the Digit Adder Out signal on the line **93***c*.**01** onto the Result 2 and Result 8 output lines. Blank, Hyphen and Ampersand characters, whose numerical portions consist of 8421=0000, are recognized in either CR 1 or CR 2 and routing lines are conditioned to block the Digit Adder outputs which have the effect of sending 8421=0000 to the Result Register from the Digit Adder Correction circuits. Output signals from the Decimal Correction circuits, FIG. 87, are provided to the C Bit Generator of FIG. 90, the Result Register of FIG. 89, the Inter Register Check Routing of FIG. 63 and other circuits as previously described with reference to FIG. 2.

CHARACTER RECOGNITION CIRCUITS

Character Recognition Circiuts are provided both for CR 1, FIGS. 71*a* and *b*, and for CR 2, FIG. 76. Both of these Recognition circuits operate in a similar manner for providing positive signals on output lines to indicate various classes of characters. By way of example, refer to FIG. 76, CR 2 Recognition, wherein an AND circuit receives inputs via CR 2–$\overline{1}$ line **75.49**, CR 2–2 line **75.39**, CR 2–$\overline{4}$ line **75.33**, and CR 2–8 line **75.18**. A section of the Code Chart given previously shows that a decimal 0 is represented by a binary 10, i.e., binary 1 in the 2 and 8 positions. Thus, if all four lines just described are positive, it signifies a holding of a decimal 0 in Character Register 2, and an output is provided on the CR 2=0 lines **76.28** and **76.29**. When a digit other than a decimal 0 is provided in CR 2, it will be noted that the lines **76.22** through **76.27** are positive due to the Inverter in the line to indicate CR 2≠0.

The reference characters used to identify outputs of the Character Recognition circuits, although abbreviated, indicate the holding of the associated Character Registers. In FIG. 76, lines **76.01** through **76.04**, when positive, signify that the character in Character Register 2 is neither a Blank nor a Hyphen, nor an Ampersand. CR 2=BL line **76.05** signifies that CR 2 contains a Blank and CR2≠BL line **76.06** signifies that CR 2 does not contain a Blank. A signal on CR 2=SM lines **76.09** through **76.18** indicated a Storage Mark. CR 2=BL/HYP/AMP/SM line **76.19** signifies a Blank, Hyphen, Ampersand or Storage Mark. CR 2≠SP CHAR line **76.20** indicates by positive signal that CR 2 does not contain a special character.

Referring to FIGS. 71*a* and *b*, CR 1 Recognition Circuits, output lines **71***a*.**01** through **71***a*.**03** indicate that Character Register 1 contains a Blank, Hyphen, Ampersand, or Storage Mark. CR **1** Odd line **71***a*.**04** indicates that the contents of CR **1** contain a Storage Mark, an invalid character in Memory. Lines **71***a*.**05** and **71***a*.**06**, when positive, give an output indicating that the contents of Character Register 1 are a Blank and that the contents of Character Register 1 are not a Blank respectively. Lines **71***a*.**07** through **71***a*.**10**, when positive, signify that Character Register 1 contents are not a Blank, Hyphen, Ampersand or Storage Mark. Line **71***a*.**11** indicates that the contents of the Zone bit positions of CR 1 are $\overline{B}$ and A. Lines **71***a*.**12** and **71***a*.**13** indicate the contents of CR 1 are not a special character. Lines **71***a*.**15** and **71***a*.**16**, when positive, indicate that the contents of CR 1 to be either a period or a comma. Lines **71***a*.**18** through **71***a*.**20** are positive to indicate that the contents of CR 1 represent a Group Mark and line **71***a*.**17** is the complement of those lines, **71***a*.**18** through **71***a*.**20**.

In FIG. 71*b*, lines **71***b*.**01** through **71***b*.**04** are positive when CR 1 is a numeric character. Alternately, the lines **71***b*.**05** through **71***b*.**09** are up to give an indication when CR 1 is not a numeric character. The line **71***b*.**10** is positive to indicate those instances when CR 1 is not equal to a 4 or 9. The line **71***b*.**11** is positive to indicate that CR 1≠0 or that the instruction is a Set Bit instruction. The line **71***b*.**12**, when positive, indicates CR 1≠0, the line **71***b*.**13** indicates that CR 1≠zero or a comma and CR 1=RM line **71***a*.**14** signifies CR 1 contains a Record Mark.

CODE CHECKING CIRCUITS

Referring now to the Memory Buffer Register Code Check circuits for characters 4, 3, 2 of FIG. 19*a*, signals for the 4, 2 and 1 bits of each character representing binary "ones" or binary "zeros," as the case may be, are fed in various combinations to AND circuits so that if only a single binary "one" is contained in the three bits or if binary "ones" are contained in all three bits, the outputs of one or more of the AND circuits are positive. In an identical manner, signals representing bits B, A and 8 are fed to AND circuits to provide a positive output if an odd number of binary "ones" are contained in the combination of bits of the B, A and 8 positions. The remaining circuits in FIG. 19*a*, are utilized to determine whether an odd or even number of binary "ones" are contained in the total count of bits in Character 4. If the sum of B, A, 8, 4, 2 and 1 bits are even, then the C bit should be zero. Otherwise, the C bit should be a binary "one" to provide a sum of the character bits which is even. If a correct code exists no signal is developed on the line **19***a*.**01** but if an odd number of binary "ones" are contained in a particular seven bits, the Character 4 Code Check Odd line **19***a*.**01** is made positive and this positive signal is utilized to signify an error. Like circuits are provided in FIG. 19*b* to check the redundancy characters 1 and 0.

Similarly, circuits are provided in CR 1 Code Check, FIG. 72, to ascertain that proper redundancy exists in the bits contained in Character Register 1, and CR 2 Code Check Circuits are provided in FIG. 77 for ascertaining that the proper redundancy exists in the character contained in CR 2.

ZONE ADDER

FIG. 79 (2 sheets) discloses circuits comprising the Zone Adder and the Zone True/Complement Controls shown in block form in FIGS. 2*ccc* and 2*fff* respectively.

The Zone T/C Controls for the A bit comprises a pair of AND circuits, FIG. 79 (Sheet 1), one AND circuit having inputs on CR 2–A line **75.09**, CR 2 to T/C line **93***b*.**05** and True line **83.01** and the other having inputs on CR 2–$\overline{A}$ line **75.13**, Complement line **93***d*.**08** and CR 2 to T/C line **93***b*.**05**. The outputs of these AND circuits feed an OR circuit which supplies an output on line **79.16**(A) to the Zone Adder circuits. The Zone T/C Controls for the B bit comprise a pair of AND circuits, FIG. 79 (Sheet 2), one AND circuit having inputs on True line **83.01**, CR 2 to T/C line **93***b*.**05** and CR 2–B line **75.03** and the other having inputs on the CR 2 to T/C line **93***b*.**05**, Complement line **93***d*.**08**, and CR 2–$\overline{B}$ line **75.06**. The outputs of these AND circuits feed an OR circuit which supplies an output on line **79.17**(B). Under control of the Complement and True lines these circuits either complement or pass unaltered the Zone bit inputs of CR 2. The Zone bits of CR 1 are directed to the Zone Adder via Adder Input Switching, FIG. 73.

Complementing of the Zone bits is accomplished by merely revising the state of the bits. For example, if the Zone bits are BA=01, the Complement is BA=10. The output of the A bit position of Character Register 2 causes CR 2–A line **75.09** to be positive for a binary "one" in the A bit position, and although CR 2 to T/C line **93***b*.**05** is positive, the True line **83.01** is down thereby presenting a negative signal to the Zone Adder on the line **79.16**(A) indicative of the complement of the input. The output of the B bit position of CR 2 causes CR 2–$\overline{B}$ line **75.06** to be positive for a binary "one" in the B bit position, and CR 2 to T/C line **93***b*.**05** and Complement line **93***d*.**08** are positive thereby providing a positive signal to the Zone Adder on the line **79.17**(B) indicative of the Complement of the binary "zero" in the B bit position of CR 2.

The Zone Adder comprises two full adder orders, one for the A bit and one for the B bit. The operation of the Adders is identical to those used in the Multiple Adder of FIG. 84 and the Digit Adder of FIG. 86, and no purpose would be served by a detailed explanation. If suffices to say that the Zone Adder receives two sets of inputs, an A bit and B bit from CR 1 and/or an A bit and B bit in True or Complement form from CR 2. If the sum of the Zone bits represented by signals on the input lines generates a binary carry, the Zone Carry Out lines **79.10** through **79.12** are positive. In FIG. 88 (Sheet 1), the line **79.11** and (—) On Suppress Zone Carry In line **93***d*.**02** condition a positive gate (GJ) in FIG. 88 (Sheet 2) for the passage of a pulse on the W_0 (D0.4) Add line **101.11** to turn On the Zone Carry trigger. When the Zone Carry trigger is On, the Zone Carry In line **88.33** provides a binary "one" to the Zone Adder of FIG. 79 (Sheet 1) in the next cycle. A binary "one" can also be added into the Zone Adder via the Zone Carry In line **93***d*.**01** for certain operations such as Add to Memory, Add Address to Memory, and Compare. Outputs on Result A line **79.03** and Result B line **79.07** are sent to the Zone Bit triggers of the Result Register, FIG. 89*b*, and outputs on Result B line **79.06** and Result A line **79.02** are sent to the C Bit Generator of FIG. 90.

C BIT GENERATOR

As stated previously, the checking system utilized in the Data Processing System is that the number of binary "ones" comprising each character must be even. Thus, as characters are transmitted from one portion of the machine to another, a check is made to ascertain that each character contains an even number of binary "ones." If an odd number of binary "ones" is received to represent a character, the machine may be stopped or an error indicated. It is pointed out, however, that when two digital values are added, subtracted, multiplied or changed in any way that the sum, difference, product or result may not contain an even number of binary "ones." Also, the number of binary "ones" in a particular character may be the result of addition of two digits by the Digit Adder and/or addition by the Zone Adder. Consequently, a Check Bit Generator is provided in order that a new check bit (C) or redundancy bit may be generated as required.

Circuits for generating this check bit (C) are shown in FIG. 90 and also shown are circuits for gating the C bit of either the character in CR 1 or CR 2 to the Result Register of FIG. 89*b*.

The Check Bit Generator receives inputs from the Decimal Adder Correction circuits on the lines **87.13**(8), **87.05**(4), **87.01**(2) and **87.12**(1), the Zone Adder on the lines **79.06**(B) and **79.02**(A), CR 1 on the line **58.01**(C) and CR 2 on the line **48.03**(C). The circuits shown in FIG. 90 consist mainly of two full adders in which only the sum lines are used, one adder which combines the B, A and 8 bits on the lines **79.06**(B), **79.02**(A) and **87.13**(8) respectively, and another which combines the 4, 2 and 1 bits on the lines **87.05**(4), **87.01**(2) and **87.12**(1) respectively. The rules of addition, stated previously, apply, and the two adders determine whether or not the three particular inputs thereto comprise an even sum (indicated by a binary "zero") or an odd sum (indicated by a binary "one"). When the outputs of both adders agree, that is, both outputs are positive or both outputs are negative, the redundancy bit (C) should be negative signifying a binary "zero." When the outputs of the adders are unlike, a binary "one" output or C bit is required. A positive signal on the Generate C Bit Out line **93***c*.**03** gates a binary "one" or positive signal onto the Result C line **90.01** to the Result Register when a C bit is required, and otherwise the Result C line is negative.

At times, it is desired to gate the C bit of the character in either CR 1 or CR 2 to the Result Register. A positive signal on the CR 1–C line **58.01**, indicating a binary "one" in the C bit position of CR 1, conditions one input of an AND circuit and another line CR 1–C Bit Out, when positive, gates the C bit onto the Result C line **90.01**. Similarly, a positive signal on the CR 2–C Bit Out line **93***b*.**06** gates the C bit, if any, from CR 2 onto the Result C Output line. If the C bit position of either CR 1 or CR 2 were negative to represent a binary "zero," then the Result C line would be negative in each case.

The Emit Blank line **93***e*.**05**, when positive, causes the output Result C line **90.01** to go positive in combination with the emission of an A bit from the Zone Adder.

For some instructions, such as Load and Unload, characters that are passed through the adders unchanged also have their C bits transmitted independently to the Result Register via the input line **56***a*.**07** instead of having a C bit generated by the circuits of FIG. 90. Thus, the gaining or dropping of a bit during the transmission of a character through the arithmetic circuits is detected if the original C bit is supplied independently to Result Register when the character (C, B, A, 8, 4, 2, 1 bits assembled in the Result Register) are redundancy checked in the Result Register Code Check circuits of FIG. 91.

RESULT REGISTER

In FIGS. 89*a* and *b*, circuits of the Result Register are illustrated which comprise seven triggers, one for each bit position of a character. The Result Register provides a buffer storage between the arithmetic circuits and Memory or Storage and furnishes signals indicative of a particular character on output busses to the Input Switch of FIG. 11 and the Storage In Selection and Switching circuits of FIG. 43 for writing into Memory or Storage respectively.

The right plate outputs (On sides) of the triggers are inverted so that the Memory/Storage In Bus lines **89***a*.**01**, **89***a*.**02**, **89***a*.**05**, **89***a*.**06**, **89***a*.**09**, **89***a*.**10**, **89***a*.**13**, **89***a*.**14** **89***b*.**01**, **89***b*.**02**, **89***b*.**05**, **89***b*.**06**, **89***b*.**09** and **89***b*.**10** are positive when their respective triggers are Off indicating binary "zeros." These positive signals are combined with the Inhibit Gate, in the manner described previously with

reference to Memory and Storage, to cancel the effect of the Write Gate in those core planes where it is desired to write "zeros" according to the bit configuration of the Result Register. When a Result Register trigger is set to a "one," the positive signal from the right plate is inverted to provide a negative output signal which blocks the Inhibit Gate to that particular core plane where a "one" is to be written.

Pairs of output lines for each trigger representing the state of each trigger and the complement thereof, for example, RR–A line **89***b*.**03** and RR–$\overline{A}$ line **89***b*.**04**, are furnished to the Result Register Code Check circuits of FIG. 93.

Input lines are provided to the Result Register from the Keyboard of FIGS. 22*a*, *b*, and *c*, the Digit Adder Decimal Correction circuits of FIG. 87, the Zone Adder of FIG. 79, the Memory Test Controls of FIG. 92, and the C Bit Generator of FIG. 90.

The triggers of the Result Register are reset Off at W_3 of each cycle during Use time via the lines **139***c*.**01** and **139***c*.**02**. The input data lines are gated at R_2 by the lines **103***a*.**15** and **103***a*.**14** which is late enough to allow time for the input lines from the adders to become stable; however, the triggers are not set until R_4 when the lines **101.18** and **101.17** become positive. It will be noted that the input Result lines by-pass the triggers and may be utilized from R_2 to R_4 before the triggers are set. After the triggers are set at R_4 time, the triggers control the output lines until reset time at W_3 and, since the input Result lines are no longer required after R_4 time, they are blocked by the fall of the R_2–A_0/W_0 lines **103***a*.**15** and **103***a*.**14**. Thus blocked, any changes in the adders due to changing the states of the Carry triggers at W_2 are not reflected in the Result Register outputs. Those triggers which are set to "ones" at R_4 are reset to "zeros" at W_3 time, and those inhibit lines blocked from R_2 to W_3 become positive for the remainder of the Inhibit Gate to furnish Post Write Disturb pulses from W_3 to R_0 as shown in FIG. 144.

OVERLAP MODE CONTROL TRIGGERS

The four triggers, Mode Control, Add, Transition and Auto Transition, shown in FIG. 136*a*, define the type of Overlap Mode Control cycle in which the system is operating and control communications between the Arithmetic and Logical Unit, Memory and Storage.

ADD TRIGGER

The function of the Add Trigger is to define the period of time in which computation may be carried on in the ALU. If the Add trigger is On, then the ALU may generate results; if the Add trigger is Off, then no computation is permitted. Accordingly, the Add trigger provides a gate signal for all of those triggers associated with the ALU, such as the Multiple Carry Triggers, FIGS. 80 and 81, Multiple Carry trigger, FIG. 85, Zone Carry trigger and Decimal Carry trigger, FIG. 88, Inter Register Check trigger, FIG. 63*c*, Low and High triggers, FIG. 138*a*, Accumulator Digit Zero trigger, Auxiliary Digit Zero trigger and Remainder trigger, FIG. 138*h*, Auxiliary Trigger 1, FIG. 138*i*, and Auxiliary trigger 2, FIG. 138*k*. Under certain conditions, the triggers just enumerated are not permitted to change state unless the Add trigger is On. Another function of this trigger is to control the turning On and Off of the Transition and Automatic Transition triggers.

In FIG. 136*a* the Add trigger is turned On if Block Add trigger is Off causing line **93***v*.**01** to be up and the Transition triggers are Off causing the line **136***d*.**02** to be up thereby conditioning the Diode Gate for the fall of the line **103***b*.**23** at W_1. If either the Transition trigger or Automatic Transition trigger is On, the line **136***c*.**01** is up to condition the associated Diode Gate and the fall of the line **103***b*.**23** at W_1 turns Off the Add trigger. Even when the Transition triggers are Off, the Add trigger is prevented from being turned On in some instances by the line Block Add trigger. Instruction reset is provided from FIG. 139*b*.

TRANSITION TRIGGER

The Transition trigger is used to define Transition cycles caused by recognition of certain conditions depending upon the type of operation being performed in change in operation. The change required may be a transition from one type of operation to another during different operations caused by the same instructions or it may be a transition out of one operation due to an instruction into another operation brought about by a new instruction. Usually, the end of a sequence of operations is recognized by a special character such as a Storage Mark set in one of the character registers at W_0. The Transition trigger is turned On at W_2 in order that the On condition of this trigger may provide for a Transition cycle in the next cycle. The main features of a Transition cycle are:

(1) Computation ceases at W_1 by turning Off the Add trigger.
(2) CR 1 and CR 2 retain the characters set therein.
(3) SAC is prevented from counting.
(4) Mode Control trigger is turned Off at the end of the Transition cycle.
(5) The Transition trigger is turned Off at the end of the Transition cycle.

It is pointed out that this trigger must be Off to have full overlap operation, and that the trigger cannot be On for two consecutive cycles.

AUTOMATIC TRANSITION TRIGGER

The Automatic Transition Trigger is turned On to define Transition cycles when special conditions are recognized which are independent of the instruction being executed and such cycles constitute delays in processing. Some of these conditions are functions of either the Storage Read/Write Mode or of the Memory Read/Write Mode when MAC 1 or SAC is stepped to a "critical" address to be explained in detail later. Other conditions are those imposed in processing Sign Checks, Instruction Checks and Overflow Checks, but only the last two can be regarded as automatic. When the Auto Transition trigger is On, the same features of a Transition cycle are present as enumerated above and additionally this trigger being On causes the Machine Check trigger to be turned On if there is a Code Check and causes the system to stop operation if the Machine Check switch of FIG. 119 is set to Automatic.

In FIG. 136*a*, the Auto Transition trigger is turned On by positive signals on the Add Trigger On line **136***d*.**15**, Turn On Transition trigger line **93***u*.**01**, and W_2 (D1) line **102.17**. The trigger is turned Off by the Add trigger Off line **136***d*.**18** and the W_2 (D1) line **102.17**. When On, the trigger provides a positive signal on the Transition line **136***a*.**03** to FIG. 136*c* and line **136***a*.**04** to FIG. 136*d*.

MODE CONTROL TRIGGER

The Mode Control trigger is turned On at the end of a Start cycle when the machine is either in the Memory R/W Mode or the Storage R/W Mode to cause computed results to be placed in Memory or Storage, as the case may be, at the address from which data was obtained during the previous cycle. As shown in FIG. 136*a*, either the Memory Read/Write Mode line **93***q*.**01** or the Storage Read/Write Mode line **93***q*.**05** along with Not Transition line **136***d*.**02** conditions a Diode Gate for the fall of the line **103***b*.**07** to turn On the trigger at W_2. The trigger is turned Off by the Transition line **136***c*.**01** which conditions a Diode Gate for the fall of the line **103***b*.**07** to turn Off the trigger at W_2.

OVERLAP MODE CONTROL TRIGGERS

The following statements apply to the extent that control is exerted among the triggers. The Add trigger cannot be turned On if either the Transition trigger or the Auto Transition trigger is On, but the Add trigger must be turned Off if either of the Transition triggers is On. Neither the Transition trigger nor the Auto Transition trigger can be turned On if the Add trigger is Off, and both must be turned Off if the Add trigger is Off. The Mode Control trigger cannot be turned On if either of the Transition triggers is On and they must be turned Off if either of the Transition triggers is On.

Computation normally begins in the first cycle of the execution of an instruction, and the Add trigger is automatically turned On in this cycle unless the particular operation specifically blocks the trigger from being turned On (Block Add trigger). In most arithmetic operations, a Transition cycle causes termination of the operation, and, thus, the recognition of a Transition cycle causes the Add trigger to be turned Off. The Transition trigger comes On at W_2, causing the Add trigger to be turned Off at the next W_1 time, which, in turn, insures that the Transition trigger will be turned Off at the next W_2 time.

Chart V

OVERLAP MODE CONTROL TRIGGERS

Trigger	Function	Turned On		Turned Off By
		By	If	
Add	Defines cycles during which computation takes place.	First cycle of execution of each instruction unless specifically blocked.	Both Transition triggers are Off.	Either Transition trigger being On.
Transition	Controls Memory sequence during change in type of operation being performed in ALU.	Recognition by individual instruction of a need to change.	Add trigger is On	Add trigger being Off.
Auto transition	Controls Memory sequence during automatic processing of redundancy checks or special conditions which are functions of the Read/Write modes.	Recognition of redundancy check or special conditions of the Read/Write modes.	Add trigger is On	Add trigger being Off.
Mode control	Defines those cycles in which results are placed into Memory or Storage at the address read from in the previous cycle.	First cycle of either the Storage or Memory Read/Write Mode.	Both Transition triggers are Off.	Either Transition trigger being On.

TRANSFER 01 INSTRUCTION

During the Instruction cycle of the Transfer 01 Instruction Instruction Counter contains the Memory Address of the Transfer 01 Instruction and MAC 2 contains an address previously set therein. During the first Execute cycle the Instruction Counter is permitted to step to the next address. Then the contents of the Instruction Counter are stored at the Memory Address specified by MAC 2. The address contained in MAC 2 ends in either a 1 or a 6 and the thousands order of the Instruction Counter is stored at the address specified by MAC 2. The A and B bits for this address are formed from the 10,000 and 20,000 triggers of the Instruction Counter. The hundreds, tens and units orders of the Instruction Counter are stored in successively higher Memory Addresses with the B bit of the units position being formed by the state of the 40,000 trigger of the IC. Instruction Counter is then reset and set to the address contained in the Transfer 01 Instruction. This address should end in a 4 or a 9. Referring now to the Transfer Flow Diagram of FIG. 146 the chart begins and ends at W_2. Therefore, the first step in the operation begins at W_2 of the Instruction cycle and ends at W_2 of ECC 1. With SSR=01 the Add trigger is blocked and the Instruction Counter is stepped +5. Beginning at W_2 of ECC 1 with SSR=01 the Add trigger is again blocked and in ECC 2 the Read Memory, Digit Adder Out, Generate C Bit Out and Step MAC 2+1 and Set MASR to MAC 2 are specified. Thereafter, bits are sent to the Adder according to the setting of the thousands and ten-thousands order of the Instruction Counter. Returning once again to the top of the diagram with SSR=01, the Add trigger is blocked. This is not an EEC 1 or an ECC 2 cycle, but rather Execute Cycle 3. Accordingly, with Auxiliary Trigger 1 and Auxiliary Trigger 2 Off, Read Memory, Result to Memory, Digit Adder Out, Generate C Bit Out and Step MAC 2+1, Set MASR to MAC 2 and Turn On Auxiliary Trigger 1 is specified. Then, bits are sent to the Adder according to the hundreds order of the Instruction Counter. During Execute cycle 4, SSR=01, the Add trigger is blocked, it is not ECC 1 or ECC 2, the Auxiliary Trigger is On and Read Memory, Result to Memory, Digit Adder Out, Generate C Bit Out, Step MAC 2+1 and Set MASR to MAC 2 is specified. The Auxiliary Trigger 2 is Off. Accordingly, Turn On Auxiliary Trigger 2 is specified. Thereafter, bits are sent to the Adder according to the tens order of the Instruction Counter. Execute cycle 5 a has SSR=01, the Add trigger is blocked, it is not ECC1 or ECC 2, Auxiliary Trigger 1 is On and Auxiliary Trigger 2 is On. Turn On Auxiliary Trigger 1 is specified and thereafter the units order of the Instruction Counter controls the bits to the Adder. During Execute cycle 6 SSR=01, the Add trigger is blocked, it is not ECC 1 or ECC 2, Auxiliary Trigger 1 is not Off, but Auxiliary Triggers 2 is On. And, therefore, the Instruction Counter is reset Set to MAR and End E time is provided.

EXAMPLE OF TRANSFER 01

Assume that MAC 2 contains the address 2001 and that the Instruction Counter contains the Memory Address 0, 1, 2, 3, 4. Located in Memory Address 0, 1, 2, 3, 4 is the Transfer 01 Instruction which has an Operations part of 1, ASU Coding 01 of 19,459. During this operation the Instruction Counter will be stepped +5 during ECC 1 and the contents 0, 1, 2, 3, 9 will be stored in the address specified by MAC 2:2001. Upon completion of the execution the Instruction Counter will be set to the Memory Address specified by the Transfer 01 Instruction 19,459 and subsequent operations will proceed from this address. The format of the Transfer 01 Instruction will then be as follows:

Memory Address	MBR Character	C	B	A	8	4	2	1
01234	0	1	0	0	0	0	0	1
01233	1	1	0	0	1	0	0	1
01232	2	1	0	0	0	1	0	0
01231	3	1	0	1	0	1	0	1
01230	4	0	0	0	1	0	0	1

MAC 2 contains address 02001, IC contains address 01234 which refers to the Transfer 01 Instruction above, the IC is stepped +5 and its contents thereafter are stored at address 02001, and the next instruction is taken from Memory Address 19,459 as specified by the Transfer 01 Instruction.

At the beginning of the Instruction cycle MAC 2 contains Memory Address 2001. Accordingly, in the first order of MAC 2, the MAC 2–1 trigger is On making the MAC 2—1 line 31*a*.05 positive. The MAC 2—8, MAC

2—4 and MAC 2—2 lines are down. In the second order of MAC 2 of FIG. 31*b*, all of the triggers are Off indicating "zero." In the third order of MAC 2 of FIG. 31*c*, all of the triggers are Off indicating "zero." In the fourth order of MAC 2 of FIG. 31*d*, the MAC 2–2000 trigger is On making the MAC 2–2000 line **31***d*.**04** positive, the MAC 2–8000, MAC 2–4000 and MAC 2–1000 lines are down. In the fifth order of MAC 2 of FIG. 31*e*, all of the triggers are Off. At the start of the Instruction cycle the Instruction Counter contains 1234. In FIG. 32*a*, the units order trigger is set to make the IC–4 lines **32***a*.**01** and **32***a*.**02** positive. In the second order of the Instruction Counter of FIG. 32*a*, the 20 and 10 triggers are On making the IC–20 lines **32***a*.**06** and **32***b*.**07** and the IC–10 lines **32***b*.**08** and **32***b*.**09** positive to indicate 30. The 80 and 40 triggers are Off. In the third order of the Instruction Counter of FIG. 32*c*, the 200 trigger is On making the IC–200 lines **32***c*.**06** and **32***c*.**07** positive. The 800, 400 and 100 triggers are Off. The fourth order of the Instruction Counter, the 1000 trigger is On making the IC–1000 lines **32***d*.**08** and **32***d*.**09** positive. The 8000, 4000, and 2000 triggers are Off. In the fifth order of the Instruction Counter of FIG. 32*e*, all of the triggers are Off indicating "zero." At R_0 of the Instruction cycle the contents of the Instruction Counter are placed in the Memory Address Select Register and in FIG. 49*b*, the IC–4 line **32***a*.**01** is positive and the Set MASR to IC line **93***s*.**01** is positive to being up the 4 line **49***b*.**04**. The $\overline{8}$, $\overline{2}$ and $\overline{1}$ lines are positive via the Inverters. In FIG. 49*a*, the $\overline{8}$, $\overline{4}$, $\overline{2}$ and $\overline{1}$ lines are positive and the pulse on the R_0 line **101**.**01** turns On the MASR 4 trigger making the MASR–4 lines **49***a*.**07** and **49***a*.**08** positive. The remaining triggers of the first order of MASR are turned Off, if On previously, to make the MASR—$\overline{8}$, the MASR—$\overline{2}$ and the MASR—$\overline{1}$ lines positive. In the second order of MASR of FIG. 49*d*, the IC–20 line **32***b*.**06** and the IC–10 line **32***b*.**08** are positive and the set MASR to IC line 93*s*.**01** makes the 20 line **49***b*.**06** and the 10 line **49***b*.**08** positive. The $\overline{80}$ and $\overline{40}$ lines are positive via the Inverters. In FIG. 49*c*, the $\overline{80}$, $\overline{40}$, 20 and 10 lines are positive to condition diode gates for the pulse on the R_0 (D0.4) line **101**.**02** which turns On the 20 and 10 triggers and turns Off the 80 and 40 triggers, if On. Therefore, the MASR–$\overline{80}$, the MASR–$\overline{40}$, the MASR–20 and MASR–10 lines are positive. In FIG. 49*f*, the IC–200 line **32***c*.**06** is positive and the Set MASR to IC line **93***s*.**01** is positive to bring up the 200 line **49***f*.**06**. The $\overline{800}$, $\overline{400}$ and $\overline{100}$ lines are positive via the Inverters. In FIG. 49*e*, the $\overline{800}$, $\overline{400}$, 200 and $\overline{100}$ lines are positive to condition gates for the R_0 pulse on the line **101**.**03** to turn on the 2 trigger and turn off the 8, 4 and 1 triggers, if On. Therefore, the MASR–$\overline{800}$, MASR–$\overline{400}$, MASR–$\overline{100}$ lines are positive and the MASR–200 line **49***e*.**08** is positive. In FIG. 49*j*, the IC–1000 line **32***d*.**08** is positive and the Set MASR to IC line **93***s*.**01** is positive to make positive the 1000 line **49***h*.**08**, the $\overline{8000}$, $\overline{4000}$, and $\overline{2000}$ are positive. In FIG. 49*g*, the $\overline{8000}$, $\overline{4000}$, $\overline{2000}$ and 1000 lines condition diode gates for the R_0 pulse on the line **101**.**04** to turn On the 1000 trigger and turn Off the 8000, 2000, and 4000 triggers, if On. In FIG. 49*j*, none of the input lines from the Instruction Counter are positive. Accordingly, the $\overline{40,000}$, $\overline{20,000}$ and $\overline{10,000}$ lines are positive via the Inverters. In FIG. 49*i*, the $\overline{10,000}$, $\overline{20,000}$, $\overline{40,000}$ lines condition diode gates for the R_0 pulse on the line **101**.**05** to turn Off the fifth order triggers if On.

Begin with Reading from Memory during the Read portion of the Instruction cycle. In FIG. 3*b*, the $\overline{20,000}$ $\overline{80}$, $\overline{40}$ and 20 lines are positive to bring up the 20 line **3***b*.**03**. In FIG. 5*a*, the 20 line **3***b*.**03** brings down the $\overline{20}$ line **5***a*.**04** and makes positive the 20 line **5***a*.**03**. All of the remaining NOT lines are up because of the Inverters. In FIGS. 5*b* and 5*e* all of the output lines except the 20 line **5***b*.**02** are driven when the Memory Read Bias Gate on the line **5***g*.**09** goes positive at R_9. In FIG. 8 all of the columns of cores are driven with reset current except the lines linked by the 20 line **5***b*.**02**. In FIG. 3*d*, the $\overline{10,000}$ $\overline{8}$, $\overline{1}$, $\overline{2}$ are positive to make positive the 10–14 line **3***d*.**05**. In FIG. 7*a*, the 10–14 line **3***d*.**05** brings down the $\overline{10–14}$ line **7***a*.**06** and makes positive the 10–14 line **7***a*.**05**. All of the remaining NOT lines are up because their inputs are down. In FIGS. 7*b* and 7*c*, all of the outputs are driven except the 10–14 line **7***b*.**03** when the Memory Read Bias Gate on the line **5***g*.**11** becomes positive at $R_{0.5}$. In FIG. 9, all of the columns of cores are driven with reset current except for the one linked by the 10–14 line **7***b*.**03**. In FIG. 3*a*, the $\overline{8000}$, $\overline{4000}$, $\overline{2000}$ and 1000 lines are positive. Therefore, the 1000 line 3*a*.**03** is positive. In FIG. 4, the 1000 line **3***a*.**03** is positive and the Memory Y Read Bias Gate on the line **5***g*.**08** becomes positive at R_1 to drive the 1000 line **4**.**02**. In FIG. 8, all of the columns of cores except the one linked by the 20 line **5***b*.**02** are driven with reset current and the 1000 line **4**.**02** is driven with set current which sets the 1020 core to the "one" state and provides half-select reset current on its secondary. In FIG. 3*c* the $\overline{800}$, $\overline{400}$, 200 and $\overline{100}$ are positive to make positive the 200 line **3***c*.**05**. In FIG. 6, the 200 line **3***c*.**05** is positive and the Memory X Read Gate on the line **5***g*.**07** comes up at $R_{1.3}$ to drive the 200 line **6**.**03**. In FIG. 9, all of the columns of cores except the one linked by the 10–14 line **7***b*.**03** are driven with reset current. The 200 line **6**.**03** is driven with set current and, therefore, the 210–214 core is set to the "one" state and provides half-select reset current on its secondary to the Switch Core Array of FIG. 13. In the Core Array the 1020 line and the 200 line provide reset current to the thirty-five cores of Memory Addresses 1230 through 1234, thereby providing indications of binary "ones" on the sense windings. At $R_{3.5}$ the sense windings are sampled and the triggers of the Memory Buffer Register are set according to bit configuration of Memory Addresses 1230 through 1234. The Memory Buffer Register now contains the Transfer 01 Instruction as previously described.

At A_0 the Storage Select Register is set to the ASU Coding of the Memory Buffer Register, CR 1 receives the contents of character 4 position of MBR and at A_1 the Memory Address contained in MBR is set into the Memory Address Register. At A_0 the character 0 position of MBR is set into the Operation Register. In FIG. 21*a*, the MBR character 0–1 line is up and the MBR character 0–2 line, MBR character 0–4 line and the MBR character 0–8 lines are down. In FIG. 21*b*, the MBR character 0–A line and the MBR character 0–B line are down. The MBR character 0–C line is up, and positive signals on the A_0 I Time Use lines **101**.**26** and **101**.**25** turn On the 1 and the C triggers to specify the operation code of the Transfer 01 Instruction. In the Operation Zone Decoder of FIG. 23*a*, the Op Register $\overline{A}$ line **21***b*.**01** and the Op Register $\overline{B}$ line **21***b*.**03** are positive. Therefore, the Minus Op Register—$\overline{A}$, $\overline{B}$ lines **23***a*.**11** through **23***a*.**21** are negative. In FIG. 23*b*, the Op Register $\overline{1}$ line **21***a*.**01**, Op Register—$\overline{2}$ line **21***a*.**17**, Op Register—4 line **21***a*.**28**, Op Register—8 line **21***a*.**38** and Minus Op Register—$\overline{AB}$ line **23***a*.**11** are negative. Accordingly, the Transfer outputs **23***b*.**11** through **23***b*.**13** are positive. The line **23***b*.**11** goes to Transfer Routing Controls of FIG. 50*b* where it makes positive the Any Transfer Instruction line **50***b*.**01**. The line **23***b*.**12** goes to Transfer 01 Circuits of FIG. 50*e* where it will be effective at W_2 of the Instruction cycle when the I time line becomes positive.

In the storage Select Register of FIG. 16*a*, the MBR character 2–B line is down, MBR character 2–A line is down, the MBR character 3–B line is down and the MBR character 3–A line is positive. At A_0 the A_0 (D0.4) I

Time Use line **101.24** goes positive to turn On the SSR—1 trigger and brings up the SSR—1 On lines **16*a*.24** through **16*a*.27**. The other SSR triggers remain Off and the Off lines are positive. In **FIG. 55*a***, the SSR Decoder the SSR—1 On line **16*a*.25**, the SSR—$\overline{2}$ On line **16*a*.14**, SSR—$\overline{4}$ On line **16*a*.07**, the SSR—$\overline{8}$ On line **16*a*.01** are positive to bring up the SSR—1 lines **55*a*.01** through **55*a*.06**.

In FIG. 121 the End I time use line **61.03** is positive to condition the diode gate for the fall of the A_3/R_4–W_2 (Blocked) line **104.10** which switches the I/E trigger from I to E and brings up the E time line **21.02** and brings down the I time line **121.01**. In FIG. 122 the End I time Use line **61.04** is positive to condition the diode gate for the fall of the A_3/R_4–W_2 (Blocked) line **121.03** which turns on the ECC 1 trigger and brings up the ECC 1 line **121.03** and the ECC 1/2 line **122.05**. These signals are distributed via the IE Timer outputs of FIGS. 124 and 123, thus, a W_2 of the Instruction cycle, the I/E trigger specifies E time and the ECC 1 trigger specifies that the first Execute cycle shall be ECC 1. During the Write portion of the Instruction cycle the contents of the Memory Buffer Register are returned to Memory addresses 1230 through 1234 and at W_3 the MBR is reset.

In FIG. 50*e*, the Transfer line **23*b*.12**, the SSR—1 line **55*a*.06** and the E Time line **123.06** are positive to bring up the Transfer 01 line **50*e*.03**, Block Add Trigger line **50*e*.04**, Read Memory line **50*e*.05**, Digit Adder Out line **50*b*.06**, Set MASR to MAC 2 line **50*e*.07**, Generate C Bit Out line **50*e*.08**.

In FIG. 93*s* the line **50*e*.07** is positive, the Minus on PCT Request line **135*b*.13** is positive to bring up the Set MASR to MAC 2 line **93*s*.02**, and make negative the Set MASR to MAC 1 line **93*s*.03**. MAC 2 contains address 2001. Accordingly in FIG. 49*b*, MAC 2—8 line **31*a*.01**, MAC 2—4 line **31*a*.03** and MAC 2—2 line **31*a*.04** are negative. MAC 2—1 line **30*a*.05** is positive and the Set MASR to MAC 2 line **93*s*.03** being positive brings up the 1 line **49*b*.08**. The $\overline{8}$, $\overline{4}$ and $\overline{2}$ lines are positive via the inverters. In FIG. 49*a*, the $\overline{8}$, $\overline{4}$, $\overline{2}$ and $\overline{1}$ lines are positive to condition diode gates for the R_0 (D0.4) pulse on the line **101.01** to turn On the MASR 1 trigger and turn Off the 8, 4 and 2 triggers, if On.

In FIG. 49*b*, the MAC 2–80 line **31*b*.01**, MAC 2–40 line **31*b*.03**, MAC 2–20 line **31*b*.04** and MAC 2–10 line **31*b*.05** are negative, therefore, the $\overline{80}$, $\overline{40}$, $\overline{20}$ and $\overline{10}$ output lines are positive. In FIG. 49*c* the $\overline{80}$, $\overline{40}$, $\overline{20}$ and $\overline{10}$ lines condition diode gates for the R_0 pulse on the line **101.02** to turn Off any of the triggers which are On. Therefore the $\overline{80}$, $\overline{40}$, $\overline{20}$ and $\overline{10}$ output lines are positive.

In FIG. 49*e*, the $\overline{800}$ line **49*f*.01**, $\overline{400}$ line **49*f*.03**, $\overline{200}$ line **49*f*.05** and $\overline{100}$ line **49*f*.07** are positive since in FIG. 49*f*, the MAC 2–$\overline{800}$ line **31*c*.01**, the MAC 2–$\overline{400}$ line **31*c*.03**, the MAC 2–$\overline{200}$ line **31*c*.04** and the MAC 1–$\overline{100}$ line **30*c*.07** are negative. Thus, in FIG. 49*e*, the $\overline{800}$, $\overline{400}$ $\overline{200}$ and $\overline{100}$ lines are positive.

In FIG. 49*h*, the MAC 2–8000 line **31*b*.01**, the MAC 2–4000 line **31*b*.03** and the MAC 2–2000 line **30*b*.06** are positive and the Set MASR to MAC 2 line **93*s*.02** provides an output on the 2000 line **49*h*.06**. The $\overline{8000}$, $\overline{4000}$ and $\overline{1000}$ lines are positive via the inverters.

In FIG. 49*g*, the $\overline{8000}$, $\overline{4000}$, 2000 and $\overline{1000}$ lines are positive to condition diode gates for the R_0 pulse on the line **101.04** which turns On the 2000 trigger and turns Off the 8000, 4000 and 1000 triggers, if On.

In FIG. 49*j*, the MAC 2–40,000 line **31*e*.03**, the MAC 2–20,000 line **31*e*.02** and the MAC 2–10,000 line **31*e*.01** are down. Therefore, the $\overline{40,000}$, $\overline{20,000}$ and $\overline{10,000}$ output lines are positive.

In FIG. 49*i*, the $\overline{10,000}$, $\overline{20,000}$ and $\overline{40,000}$ lines condition diode gates for the R_0 pulse on the line **101.05** which turns Off all of the triggers of the fifth order MASR, if On. Therefore, the $\overline{10,000}$, $\overline{20,000}$ and $\overline{40,000}$ output lines are positive. Thus, at R_0 of ECC 1, MASR contains the Memory address 2001 which it obtained from MAC 2. The Instruction Counter is not stepped until R_3 of ECC 1. Therefore, ECC 1 is reserved for this operation and is shown in the Transfer Flow Diagram of FIG. 146. No other function is performed.

In FIG. 93*j*, the Reset IC and Set to MAR lines **129*b*.01**, **50*b*.04** and **50*e*.09** are down. Therefore, the Minus On Block Step IC line **93*j*.12** is positive.

In FIG. 32*a*, the NOT Manual 3 line **116.09**, the ECC 1 line **123.34**, the Minus On Block Step IC line **93*j*.12** and the A_2/R_3–W_1 (Blocked) line **103*a*.20** provide an output on the AND circuit which is inverted to provide a negative input to the units order trigger for the Instruction Counter which switches it from 4 to 9 and the IC–9 lines **32*a*.03** through **32*a*.05** are positive. Accordingly, the contents of the Instruction counter are now 1239.

In FIG. 122, the right plate of the ECC 1 trigger conditions the diode gate for the fall of the A_3/R_4–W_2 line **121.03** which turns On the ECC 2 trigger and makes positive the ECC 2 line **122.04** and the ECC 1/2 line **122.05**. The right plate of the ECC 1 trigger also conditions the diode gate for the fall of the line **121.03** which turns Off the ECC 1 trigger.

Referring now to FIG. 50*e*, Auxiliary Trigger 2 Off line **138*l*.01** and $\overline{\text{ECC}}$ $\overline{1}$ line **123.44** made positive the Step MAC 2+1 line **50*e*.01** and the Result Memory line **50*e*.02**. Although MAC 2 is stepped +1 during ECC 2 the contents of the Memory Address Select Register remains set to 2001. Also positive are Transfer 01 Block Add trigger, Read Memory, Digit Adder Out, Set MASR to MAC 2 and Generate C Bit Out.

In FIG. 50*f*, the Transfer 01 line **50*e*.03** and the ECC 2 line **123.47** are positive to bring up the store thousands order line **50*f*.01**.

In FIG. 50*g*, the ICC–1000 line **32*d*.09** is positive. The Store Thousands Order line **50*f*.01** is positive to bring up the 1 bit to Adder line **50*g*.01**.

In FIG. 93*f*, the 1 bit to Adder line **93*f*.01** is positive. In the Multiple Adder of FIG. 84 as mentioned previously, the Read Memory line **50*e*.05** is positive during ECC 2. During the Read portion of ECC 2 Memory addresses 2000 through 2004 are read from and placed in the Memory Buffer Register as in the previous cycle and therefore the switch cores in the matrices of FIGS. 8 and 9 are set to the thousands order of the Instruction Counter and the state of the 10,000 and 20,000 triggers of the Instruction Counter may be stored at address 2001. It is pointed out that CR 1 to Adder has not been made positive. Therefore at Adder input switching in the FIG. 73, the contents of CR 1 are prohibited from passing therethrough. Accordingly, there are no signals present at the inputs to the Multiple Adder except the 1 bit to Adder on the line **93*f*.01** which makes positive the Multiple 1 lines **84.01** and **84.02**.

In FIG. 86, the Multiple 1 line **84.01** is positive. Therefore the Digit Adder provides an output on the Sum 1 line **86.01** in the Decimal Correction Circuits of FIG. 87. In the Decimal Correction Circuits, the Digit Adder Out line **93*c*.01** is positive to gate the signal on the Result 1 lines **87.09** through **87.12**. The Result 1 line **87.09** goes to the Result Register of FIG. 89*a* and the Result 1 line **87.12** goes to the C Bit Generator of FIG. 90.

In FIG. 3*e*, the $\overline{8}$, $\overline{2}$, $\overline{4}$ and the 1 lines are positive from the Memory Address Select Register which brings up the Select Character 1 lines **3*e*.03** and **3*e*.04**. In FIG. 20*a*, the Select Character 1 line **20*a*.02** is positive and in FIG. 10 the Result to Memory line **137.01** and Select Character 1 line **20*a*.02** make positive the Result 1 to Memory line **10.04**. In the Result Register of FIGS. 89*a* and *b*, the Memory Storage In Bus $\overline{2}$ line **89*a*.05**, the Memory Storage In Bus $\overline{4}$ line **89*a*.09**, the Memory Storage In Bus

$\overline{8}$ line **39***a*.**13**, the Memory Storage In Bus $\overline{A}$ line **89***b*.**01** and the Memory Storage In Bus $\overline{B}$ line **89***b*.**05** are positive to indicate the complement of the "one" contained in the Result Register. In FIG. 11*b*, the $\overline{B}$, $\overline{A}$, $\overline{8}$, $\overline{4}$ and $\overline{2}$ lines from the Result Register are positive and the Result 1 to Memory line is positive making the character 1–C bit line **11***b*.**02**, the character 0–A bit line **11***b*.**03**, the character 1–$\overline{8}$ bit line **11***b*.**04**, the character 1–$\overline{4}$ bit line **11***b*.**05** and the character 0–2 bit line **11***b*.**06** positive. These lines go to the Inhibit Driver Circuits of FIG. 12*b* where they provide inhibit current in those planes where it is desired to write "zeros" in the Memory Address 2001. In the Y Switch Core Matrix of FIG. 8, the 2000 core is in the set condition and in the X Switch Core Matrix of FIG. 9 the 0–4 core is in the set condition. In FIG. 5*b*, the 00 line **5***a*.**01** is positive and the Memory Write Gate on the line **5***g*.**03** becomes positive at W_0 to drive the 00 line **5***b*.**01**. In FIG. 8, the column of cores linked by the 00 line **5***b*.**01** is driven with reset current and the 2000 core is switched to the "zero" state providing half-select current on its secondary. In FIG. 7*b*, the 0–4 line **7***a*.**01** is positive, the Memory Read Gate on the line **5***g*.**05** comes up at W_0 to drive the 0–4 line **7***b*.**01**. In FIG. 9, the column of cores linked by the 0–4 line **7***b*.**01** is driven with reset current which resets the 0–4 core to provide half-select set current on its secondary. In the Core Array the thirty-five core planes at Memory addresses 2000 through 2004 are driven with set current and inhibit current is provided from the Memory Inhibit Driver Circuits of FIG. 12*b*, and, accordingly, the digit 1 is written into Memory address 2001.

In FIG. 122, the right plate of the ECC 2 trigger conditions a diode gate for the fall of the A_3/R_4–W_2 line **121.03** which turns Off the ECC 2 trigger and makes positive the $\overline{ECC}$ $\overline{1/2}$ line **122.01**. During ECC 2, MAC 2 was stepped to 2002 and at R_0 of Execute cycle 3, the Memory Address Select Register is set to MAC. Therefore, during Execute cycle 3 Memory addresses 2000 through 2004 will be referred to, but it will be Memory address 2002 in which the hundreds order of the Instruction Counter will be stored. In FIG. 50*e*, Auxiliary Trigger 2 Off line **138***l*.**01**, $\overline{ECC}$ $\overline{1}$ line **123.44**, Transfer line **23***b*.**12**, SSR—1 line **55***a*.**06** and E Time line **123.06** make positive the Step MAC 2+1 line **50***e*.**01** and the Result to Memory line **50***e*.**02**. Transfer 01, Block Add trigger, Read Memory, Digit Adder Out, Set MASR to MAC 2 and Generate C Bit Out lines remain positive. In FIG. 50*f*, the $\overline{ECC}$ $\overline{1/2}$ line **124.13**, Auxiliary Trigger 1 Off line **138***j*.**04** and Auxiliary Trigger 2 Off line **138***l*.**02** make positive the Store Hundreds Order line **50***f*.**02** and the Turn On Auxiliary Trigger 1 line **50***f*.**03**. In FIG. 50*g*, the IC–200 line **32***c*.**07** is positive, the Store Hundreds Order line **50***f*.**02** is positive to bring up the 2 bit to Adder line **50***g*.**02**. In FIG. 93*f*, the signal is passed onto the 2 bit to Adder line **93***f*.**02** to the Decimal Correction Circuits of FIG. 85. Therefore, the Multiple 2 lines **85.01** and **85.02** are positive. In FIG. 86, the Multiple 2 line **85.01** is positive and the Binary Sum 2 lines **86.02** and **86.03** are positive. In FIG. 87, the Digit Adder Out line is positive, the Binary Sum 2 line **86.02** is positive making the Result 2 lines **87.02** through **87.04** positive. The line **87.02** goes to the Result Register of FIG. 89 where it is used to turn On the 2 trigger. The Result 2 line **87.01** goes to the C Bit Generator of FIG. 90 which then provides a binary "one" for the C trigger of the Result Register. In this instance Select Character 2 line **3***e*.**05** is made positive in FIG. 3*e* due to the $\overline{2}$, $\overline{4}$, $\overline{1}$ and 2 lines being positive from MASR. In FIG. 20*a*, the Select Character 2 line **3***e*.**05** makes positive the Select Character 2 line **20***a*.**01** of FIG. 10. In the latter figure the Select Character 2 line **20***a*.**01** and the Result to Memory 1 line **137.01** bring up the Result 2 to Memory line **10.06** and in FIG. 11*a* the $\overline{B}$, $\overline{A}$, $\overline{8}$, $\overline{4}$ and $\overline{1}$ signals are gated onto the output lines to furnish inhibit current as previously described. In FIGS. 8 and 9 the 2000 and 0–4 cores respectively, are set to the "one" state during the Read portion of the cycle and during the Write portion of the cycle will be reset to furnish half-select set current to the thirty-five cores of Memory addresses 2000 through 2004 and the digit 2 is stored in Memory address 2002.

In FIG. 138*i* the left plate of Auxiliary Trigger 1 and the Turn On Auxiliary Trigger 1 line **93***k*.**01** condition a diode gate for the fall of the A_3/R_4–W_2 line **103***b*.**15** to turn On the Auxiliary Trigger 1 and bring up the Auxiliary Trigger 1 On lines **138***i*.**02** through **138***i*.**31**. Thus, the operations during Execute cycle 4 are defined by Auxiliary Trigger 1 being On. In FIG. 50*e*, the status of the output lines remain unchanged, but in FIG. 50*f*, the Transfer 01 line **50***e*.**03**, Auxiliary Trigger 2 Off line **138***l*.**02** and Auxiliary Trigger 1 On line **139***i*.**07** provide positive level on the Store Tens Order line **50***f*.**04** and Turn On Auxiliary Trigger 2 line **50***f*.**05**. In FIG. 50*g*, the IC–10 line **32***b*.**09** and the IC–20 line **32***b*.**07** are positive. The Store Tens Order line **50***f*.**04** makes positive the 1 bit to Adder line **50***g*.**01** and the 2 bit to Adder line **50***g*.**02**. The entry of these bits into the Result Register will not be described. However, it is pointed out that in this instance the 1 and the 2 triggers are turned On and the remaining triggers are Off. No C bit is provided since the sum of the 1 bits is even. Since the Memory Address Select Register was set to 2003 at R_0 of Execute cycle 4, the $\overline{8}$, $\overline{4}$, 2 and 1 lines in FIG. 3*e* make positive the Select Character 3 lines **3***e*.**07** and **3***e*.**08**. In FIGS. 8 and 9, the 2000 core and the 0–4 core were set during the Read portion of Execute cycle 4 and will be reset during the Write portion of Execute cycle 4 to store the contents of the Result Register at Memory address 2003. In FIG. 20*a*, the Select Character 3 line **20***a*.**08** is positive and in FIG. 10 the Select Character 3 line and the Result to Memory line **137.01** make positive the Result 3 to Memory line 10.08. In FIG. 11*a* the $\overline{C}$, $\overline{B}$, $\overline{A}$, $\overline{8}$ and $\overline{4}$ lines are positive and are gated by the Result 3 to Memory line to the Inhibit Driver circuits of FIG. 12*a* to furnish inhibit current in those planes where it is desired to write "zeros." Thus, during the Write portion of Execute cycle 4, the digit 3 is stored in Memory address 2003.

During Execute cycle 4, MAC 2 was stepped to 2004 and at R_0 of Execute cycle 5 the MASR is set to the contents of MAC 2 and remains at address 2004 throughout the cycle. In FIG. 138*k*, Turn On Transition Trigger 2 line **93***k*.**03** and the left plate of Auxiliary Trigger 2 condition a diode gate for the fall of the A_3/R_4–W_2 line **103***b*.**16** to turn On Auxiliary Trigger 2 and bring up Auxiliary Trigger 2 on lines **138***k*.**02** through **138***k*.**32**. Therefore, operations during Execute cycle 5 are determined by Auxiliary Trigger 1 and Auxiliary Trigger 2 being On and it is during this cycle in which the units order of the Instruction Counter and the 40,000 order are stored at address 2004. In FIG. 50*e*, the condition of the lines remains unchanged, but in FIG. 50*f*, the Transfer 01 line **50***e*.**03**, Auxiliary Trigger 1 On line **138***i*.**07** and Auxiliary Trigger 2 On line **138***k*.**06** make positive the Store Units Order line **50***f*.**08** and the Turn Off Auxiliary Trigger 1 line **50***f*.**07**. In FIG. 50*g* the IC–9 line **32***a*.**05** is positive and the Store Units Order line **50***f*.**06** is positive to bring up the 1 bit to Adder line **50***g*.**01** and the 8 bit to Adder line **50***g*.**04**. These bits are passed to the Result Register in the manner previously described. In FIGS. 8 and 9, the 2000 switch core and the 0–4 switch core were set during the Read portion of the cycle and are reset during the Write portion of the cycle to write the contents of the Result Register in the Memory address 2004. In FIG. 3*e*, the $\overline{8}$, $\overline{2}$, $\overline{1}$ and 4 lines are positive to bring up the Select Character 4 lines **3***e*.**09** and **3***e*.**10**. The Select Character 4 signal gates the complement of the digit in the Result Register to the inhibit circuits of FIG. 12*a* and prevents the writing of "ones" in those planes where "zeros" are desired.

In FIG. 138*i*, the right plate of Auxiliary Trigger 1 and the Turn Off Auxiliary Trigger 1 line **93***k*.**02** condition a diode gate for the fall of the A_3/R_4–W_2 line **103***b*.**15** which turns Off Auxiliary Trigger 1 at W_2 of Execute cycle 5. Execute cycle 6 will have its operations defined by Auxiliary Trigger 1 being Off and Auxiliary Trigger 2 being On. In FIG. 50*e*, Auxiliary Trigger 1 On line **138***i*.**06** is down and Auxiliary Trigger 2 Off line **138***l*.**01** is down. Therefore, Step MAC 2+1 line **50***e*.**01** and Result to Memory line **50***e*.**02** are negative. Transfer line **23***b*.**12**, SSR—1 line **50***a*.**06**, E Time line **123.06**, Auxiliary Trigger Off line **138***j*.**03** and Auxiliary Trigger 2 On line **138***k*.**05** make positive the reset Instruction Counter and Set to MAR line **50***e*.**09** and End E Time **50***e*.**10**. Recall that the Memory Address Register contains the Memory address of the Transfer 01 Instruction 19,459. It is this address to which the next reference will be made for an Instruction. In FIG. 93*j*, the line **50***e*.**09** makes positive Reset IC and Set to MAR lines **93***j*.**10** and **93***j*.**11**, and brings down the Minus On Block Step IC line **93***j*.**12**. The line **93***j*.**10** goes to the Reset circuits of FIG. 139*a* where it is used to reset the Instruction Counter to 0004. The lines **93***j*.**11** and **93***j*.**12** go to FIG. 32*a*. In FIG. 32*a*, the MAR—$\bar{4}$ line **17***a*.**09** is positive to condition a diode gate for the fall of the output of the AND circuit fed by Reset IC and Set to MAR line **93***j*.**11** and the A_2/R_3–W_1 line **103***a*.**20**. This sets the Units Order trigger to **9**. The negative shift is also supplied on the lines **32***a*.**06** through **32***a*.**09**. In FIG. 32*b*, the MAR–40 line **17***b*.**14**, the MAR–10 line **17***b*.**30** are positive to condition diode gates for the fall of the line **32***a*.**06** to turn On the 40 and 10 triggers to specify 50 in the second order of IC. In FIG. 32*c*, the MAR–400 line **17***c*.**16** is positive to condition a diode gate for the fall of the line **32***a*.**07** to turn On the 400 trigger and thereby specify the value 400 in the third order of the Instruction Counter. In FIG. 32*d*, the MAR–8000 line **17***d*.**08** and the MAR–1000 line **17***d*.**34** condition diode gates for the fall of the line **32***a*.**08** which turns On the 8000 and 1000 triggers to specify 9000 in the fourth order of the Instruction Counter. In FIG. 32*e*, the MAR–10,000 line **17***e*.**07** is positive to condition a diode gate for the fall of the line **32***a*.**09** to turn On the 10,000 trigger in the fifth order of the Instruction Counter. Thus, the Instruction Counter now contains the Memory address 19,459.

The End E Time line **50***e*.**10** goes to FIG. 93*r* where it makes positive the End E Time lines **93***r*.**01** through **93***r*.**06**. In FIG. 121, the End E Time line **93***r*.**06** conditions a diode gate for the fall of the A_3/R_4–W_2 line which switches the I/E trigger from E to I and brings up the I Time line **121.01**. Therefore, the next cycle will be an Instruction cycle and the instruction referred to will be the one contained in the Instruction Counter as specified by the Memory address portion of the Transfer 01 Instruction.

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EXPLANATION OF SYMBOLS

A is an AND circuit. —A is a negative AND circuit (+OR circuit). AC is a cascaded AND circuit. AM is a driver. AMD is a switch core read driver. AMP is a switch core write driver or ring circuit driver. AMR is a switch core driver. AMS is a sense amplifier. DG is a negative diode gate. DL is a delay line. GA and GAF are grounded grid amplifiers. GJ is a positive diode gate. I is an inverter. IC is a clock inverter. IF, IJ, IZI, IJK and IK are inverters. IN and INK are neon inverters. IPF is a pulse forming inverter. K is a standard cathode follower. KB is a power cathode follower. KC is a

cathode follower clamp. KG is a plate level cathode follower. KF, KJ, KJO and KMD are cathode followers. KO is a cathode follower OR. KO∞ is a cathode follower. KR is a cathode follower with a cathode resistor common with another cathode follower. KRA is a reset cathode follower. KS is a resistance gated diode driver. KZ is a power cathode follower. O and O∞ are OR circuits. OC and OCS are cascaded OR circuits. PKRZ is a peaker. RD is a relay driver. SS is a single shot. SSE is a fast recovery single shot. T is a high speed trigger. TB is a Schmitt trigger. TC, TMS and TR are triggers. TS is a slow speed trigger. TT is a tape write trigger. XTAL is a crystal. The letter "P" signifies a powered routing line. "PN" indicates that panel neons are associated with a trigger.

While the invention has been particularly shown and described with references to preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made therein without departing from the spirit and scope of the invention.

I claim:

1. In a data processing system controlled by manifestations representative of instructions having an operation portion and an address portion and operating in instruction and execution cycles which includes storage means designated Memory having addressable locations for storing manifestations representative of characters; means connected to said Memory including a memory address counter for holding the address of character manifestations stored in Memory; means connected to said Memory, including an instruction counter operable to store manifestations for indicating the address of a transfer instruction, means connected to said instruction counter initially operable during an instruction cycle for initiating execution cycles and stepping the instruction counter to another instruction address; execution means connected to said Memory and to said instruction counter, controlled by manifestations of said transfer instruction operation portion, effective to store the contents of the instruction counter at the Memory address contained in the memory address counter and means connected to said execution means operable to place the address contained in the manifestations representative of the Transfer instruction in the instruction counter and operable to initiate an instruction cycle.

2. In a data processing system controlled by manifestations representative of instructions having an operation portion and an address portion and operating in instruction and execution cycles which includes first storage means designated Memory having addressable locations for storing manifestations representative of characters; addressing means connected to said Memory for controlling selection of storage locations in Memory; a memory address counter connected to said addressing means for holding the address of character manifestations stored in Memory; means, including an instruction counter connected to said Memory operable to store manifestations for indicating the address of a Transfer instruction; means connected to said instruction counter initially operable during an instruction cycle for initiating execution cycles and altering the contents of the instruction counter in a predetermined fashion; execution means connected to said addressing means and to said instruction counter, controlled by manifestations of said Transfer instruction, for causing the addressing means to direct the storing of the contents of the instruction counter at the address specified by said memory address counter; and means connected to said execution means for causing the manifestations representative of the address portion of the Transfer instruction to be placed in the instruction counter and for initiating an instruction cycle.

3. Apparatus for processing data in accordance with instruction manifestations each including an address portion and a number of other portions, having addressable locations, and having manifestations of a first instruction including a first address portion stored at a first location comprising: storage means; addressing circuit means connected to said storage means; a register connected to said addressing circuits for holding manifestations representative of a second address portion: an instruction counter connected to said addressing circuits for holding the location of the first instruction and capable of being modified by a predetermined amount; means connected to said instruction counter, initially operable during an instruction cycle for initiating execution time and for changing the contents of the instruction counter; execution means connected to said storage means and to said instruction counter, controlled by said other portions of said instruction causing said storage means to store the contents of the instruction counter, so changed, at the second address specified by said register; and means connected to said execution means operable to place said first address portion contained in the first instruction manifestations in the instruction counter.

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