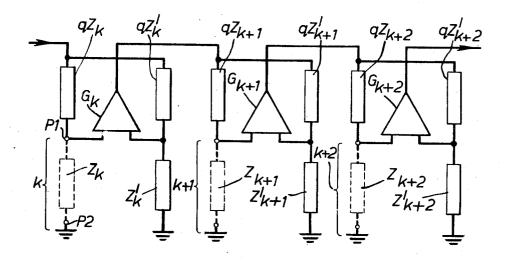
[72]	Inventors	Philip Ernest Greenaway Kenton, Harrow;	[56]		References Cited		
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[45]	Patented	June 1, 1971	3,377,570	4/1968	Dean et al	333/1.1	
[73]	Assignee	Her Majesty's Postmaster General London, England	Primary Ex	Primary Examiner—Nathan Kaufman			
[32]	Priority	Mar. 15, 1968	Attorney—I	Attorney—Hall and Houghton			
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[31]		12,766	ABSTRACT: This specification describes an electrical net-				

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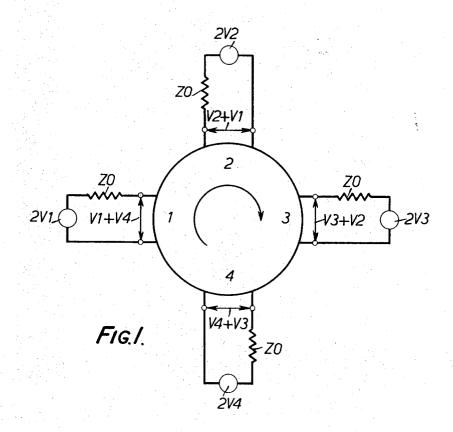
[54] ELECTRICAL NETWORKS HAVING THE PROPERTIES OF CIRCULATORS 7 Claims, 8 Drawing Figs.

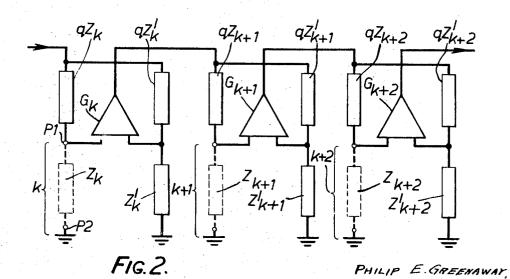
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[51]	Int. ClField of Search	330/30D 330/6	0 222/1 1
			30/53, 56;

ABSTRACT: This specification describes an electrical network having the properties of a circulator with n ports in sequence in a closed ring in which each port has associated with it a respective pair of signal transmission paths of equal but opposite gains connected from a common input point for the pair of paths to a common output point for the pair of paths, the port being coupled for signal transfer to and from only one of the paths of the pair, and the common output point for the pair of paths associated with each port being associated with the next port in the sequence so as to form a closed ring of pairs of paths. The transmission paths may consist of differential amplifiers respective to the pairs of paths together with associated resistors.



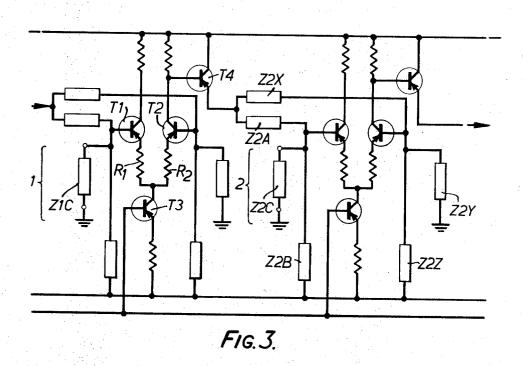
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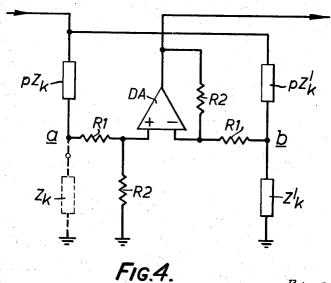




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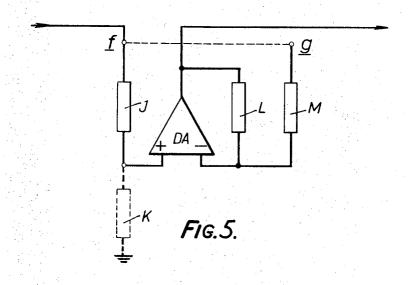


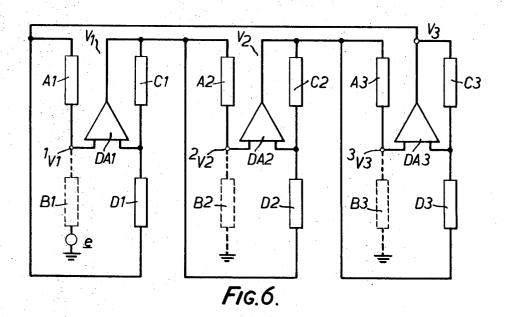


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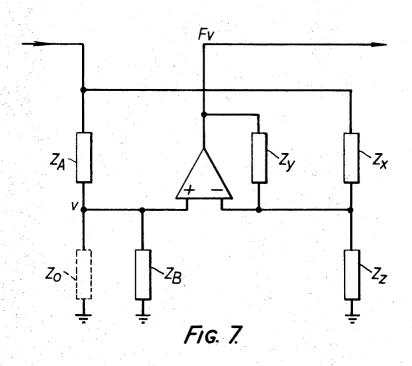
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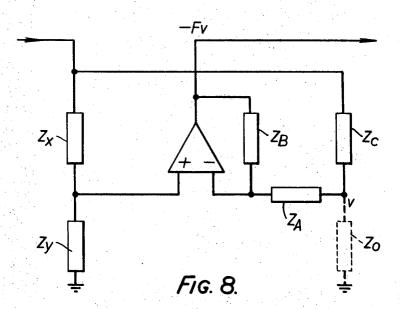
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ELECTRICAL NETWORKS HAVING THE PROPERTIES **OF CIRCULATORS**

This invention relates to electrical networks having tee properties of circulators and including active elements.

A multiport circulator having n ports is a circuit in which (if the ports are numbered consecutively from 1 to n) a signal applied at any port k appears at the next port k+1 but at no other port, when all the ports are correctly terminated. A signal applied at port n appears at port 1. A diagram of a four-port cir- 10 culator in which all ports are terminated by matching impedances Z₀ is illustrated in FIG. 1 of the accompanying drawings.

Hitherto circulators have been constructed to operate at microwave frequencies, using ferrite material but are not 15 suited to use at low frequencies. It is an object of this invention to provide a circulator which can be used at low frequencies.

The present invention is based on the use of active devices in such circulators and, according to the invention a circulator comprises a plurality of ports arranged in sequence in a closed cycle, wherein the ports have associated therewith respective pairs of paths of equal and opposite gains, the pairs of paths being connected in parallel from common input points respective to the pairs of paths to common output points respective to the pairs of paths and connections from the ports to one path of the respective pairs of paths so that signals can be fed to and taken from the one path, chosen so as to provide the desired sense of output signals, independently of the other path, the output point of the paths associated with any one port being connected to the input point of the paths associated with the next port in the sequence. Circulators in accordance with the invention can be constructed which are capable of operation down to zero frequency.

In one embodiment, the differential amplifiers each comprise a long-tailed transistor pair including emitter feedback resistors; each long-tailed pair may be fed from a constant current source and have its output connected, with or without phase reversal, to the next port by a common collector transistor stage.

In an alternative embodiment, the differential amplifiers are differential, operational amplifiers i.e. amplifiers having high gain (typically several thousands or more), high input impedance and low output impedance and negative feedback is provided over the amplifier so that a desired gain is obtained. 45 In the ideal case, the gain and input impedance would be infinite and the output impedance zero but satisfactory performance can be obtained short of these ideal values.

The invention will be described in greater detail with reference to FIGS. 2-6 of the accompanying drawings, of 50

FIG. 1 illustrates a diagram of a four-port circulator.

FIG. 2 illustrates a basic form of part of a network embodying the invention;

FIG. 3 illustrates a specific form of network of the type 55 shown in FIG. 2;

FIGS. 4 and 5 illustrate individual stages of another network embodying the invention;

FIG. 6 illustrates a network with the properties of a threeport circulator employing stages as shown in FIG. 5; and

FIGS. 7 and 8 illustrate circuits derived from FIG. 4.

FIG. 2 shows, schematically, any three successive ports of a network with the properties of a multiport circulator embodying the invention. The ports are connected in sequence k, k+1, k+2 etc.,(k=1...n). Associated with each port is a differential 65 amplifier G (an amplifier the output voltage of which is proportional to the difference in potential between the two inputs to the amplifier) having negligible reverse transmission. One terminal P1 of each port is connected to one terminal of the amplifier of that port and the other terminal P2 of each port is 70 connected to ground. In use the ports are closed by external impedances Z_k , Z_{k+1} , Z_{k+2} , etc. Each amplifier (e.g. amplifier Gk) has its output applied to both input terminals of the amplifier (G_{k+1}) associated with the next port (k+1) through two separate potential dividers shown in the drawing as (Z_{k+1}, 75 the effective gain of the stage, i.e. the signal amplitude at the

 qZk_{A1} , and $Z^{1}k_{+}1$, qZ^{1}_{k+1}) where q may differ from port to port. As shown the ratios of the dividers connected to the inputs of any amplifier are equal, so that the differential input signal to the amplifier from the previous amplifier is zero; consequently a signal applied at one port appears at the next port in the sequence but is not passed on to any other ports.

The terminating impedances (e.g. Z_k for port k) forming part of one of the potential dividers for the amplifier (G_k) associated with that port and the input impedance at each port can be made equal to the terminating impedance by suitable choice of impedance values in the potential dividers or by internal impedances connected in parallel with each port.

FIG. 3 illustrates two ports of a network embodying the invention and using differential transistor amplifiers. Each amplifier comprises a long-tailed transistor pair T1, T2 having emitter feedback resistors R1, R2 to make the voltage gain insensitive to transistor parameters and to produce a high input resistance. The emitter current is supplied by a transistor T3 connected as a constant current generator to produce a high common mode rejection.

An output is shown taken from the collector of transistor T2 but could be taken from the collector of transistor T1 if phase reversal is required. The output of a differential-input amplifier long-tailed pair of one stage is connected to the inputs of the transistors T1, T2 of the next port via potential dividers, e.g. the output of the amplifier T1, T2 of port 1 is fed to the inputs of the amplifier of port 2 via three-element potential dividers Z2A, A2B, Z2C, and Z2X, Z2Y, Z2Z, where Z_{2C} is an external terminating impedance. In the particular circuit shown in FIG. 3, a transistor T4 is used as a common collector stage to reduce the loading effect of the potential dividers on the output of the long-tailed pair.

The potential divider impedances are chosen to make the 35 DC potential at each port equal to zero with respect to ground and to give the required signal gain between ports. The threeelement potential dividers are arranged to satisfy these requirements simultaneously. The gain is equal to the voltage gain of the amplifier divided by the loss in the associated potential dividers and is commonly chosen to be unity.

A network embodying the invention may be built using a stage for each port identical to the stage shown in FIG. 4. This stage contains a differential-input operational amplifier DA, that is, a ifferential-input amplifier having very high gain, very high input impedance and negligibly low output impedance. The stage also incorporates potential dividers Z_k , pZ_k and Z_k^1 , pZ_k^1 , where p is a factor which may differ from stage to stage. Z_k is an external terminating impedance.

Because the input impedance is very high the current flowing into the input terminals is negligible and can be regarded as zero. The differential voltage gain is very high (typically of the order of 50,000) so that the potential difference between the input terminals is extremely small compared to the signal voltages; consequently, the input terminals can be regarded as virtually at the same potential.

The circuit of FIG. 4 is derived directly from one stage of the circuit of FIG. 2 by employing the operational amplifier in the conventional way as a balanced differential amplifier with defined voltage gain. The gain of the amplifier is R₂/R₁; the input terminals being a and b. If required the terminals a and bcan be interchanged so that the port is connected to terminal b. This connection gives a phase reversal between the input applied to the port and the output. Normally, the resistors R₁ and R2 have resistances which are high compared with the impedances in the potential dividers but, if this is not so, the values of Z_k and Z_a can be so chosen to take account of the shunting effects of resistors R₁ and R₂.

Two circuits which may be derived from the circuit of FIG. 4 are shown in FIGS. 7 and 8. These circuits are obtained by applying star-delta transformations to the circuit of FIG. 4 and eliminating redundant impedances. The circuit of FIG. 8 gives a phase reversal; the circuit of FIG. 7 does not.

The design of these circuits based on a constant 'F' which is

input of the amplifier is 'F' times the signal at the input port. A network can be built from any number of stages of either type, intermixed if required, one stage being necessary for each port. The values of the components of each stage can be chosen so that the input impedance of the stage is equal to the terminating impedance Z_o for that stage. Providing all stages in a network have the same value of 'F' and the component values are related as stated below, the gain between stages is unity.

Component value: Component values in Fig. 7

$$Z_{A} = \frac{F}{2}Z_{0}$$

$$Z_{B} = \frac{F}{F-2}Z_{0}$$

$$Z_{B} = \frac{F}{F-2}Z_{0}$$

$$Z_{C} = \frac{F^{2}}{F+2}Z_{0}$$

It can be seen from the expressions for the component values that, if F is made equal to two, the circuit of FIG. 7 simplifies to that of FIG. 5 whereas the circuit of FIG. 8 cannot be realized since both Z_A and Z_B become infinite and the inverting input terminal of the amplifier is isolated.

The circuit of FIG. 5 uses fewer components than any of the other circuits and is derived from the circuit of FIG. 4 as explained above by putting F=2 in the circuit of FIG. 7. The operation of this circuit can be explained as follows with reference to FIG. 5. Consider the dotted connection between points f and g broken, and separate voltage generators e_f and e_g connected at points f and g. The circuit acts as a noninverting amplifier for e_f , (using the superposition theorem), the gain $-G_g$ depending only on impedances L and M. Now if $|G_f|$ and $|G_g|$ are made equal by suitable choice of the impedances J, K, L, M, and points f and g are joined, the resultant gain will be zero. Therefore a signal from the preceding stage is not passed on to the next stage.

A circuit of a three-port network having ports 1, 2, 3 using the simplified stage of FIG. 5 is shown in FIG. 6. The impedances B₁, B₂ etc. are the matching or terminating impedances. To explain this circuit it is convenient to use the two properties of an operational amplifier, with external negative feedback applied, mentioned in the description of FIG. 4, viz: (i) negligible current flows in to either input terminal and (ii) the potential difference between the two input terminals is negligible and they may be regarded as at virtually the same 50 potential.

A generator of impedance B_1 is connected to port 1 such that the voltage appearing at this port is v_1 ; the other two ports are terminated with the matching impedances B_2 and B_3 . To simplify the explanation it is assumed that the output voltage V_3 of amplifier DA3 3 is zero. Using property above, the potential of the other input terminal of amplifier DA1 is v_1 , and hence the current in impedance D_1 is v_1/D_1 . Since no current flows into the input terminals (property (i) above), the current in impedance C_1 is also v_1/D_1 and hence $V_1 = v_1 + C_1$ 60 v_1/D_1 . The voltage v_2 appearing at port 2 is:

$$\frac{V_1B_2}{A_2+B_2} = v_1 \frac{B_2(C_1+D_1)}{D_1(A_2+B_2)}$$

and this satisfies the first condition for the circuit to be a circulator, i.e. a signal applied at one port appears at the next port.

The voltage at both input terminals of amplifier DA2 can be taken as v_2 by property above, therefore, the current in impedance D_2 is:

$$\frac{v_2 - V_1}{\overline{D}_2} = \frac{1}{D_2} \left(\frac{V_1 B_2}{A_2 + B_2} - V_1 \right) = \frac{-A_2 V_1}{D_2 (A_2 + B_2)}$$

The same current flows in impedance C2 so that:

$$V_2 = \frac{V_1 B_2}{A_2 + B_2} \frac{-A_2 C_2}{D_2 (A_2 + B_2)} V_1 = \frac{B_2 D_2 - A_2 C_2 V_1}{D_2 (A_2 + B_2)}$$

If $B_2D_2=A_2C_2$ the output voltage V_2 is zero and no signal is 10 passed on to port 3 thus satisfying the second condition for a circulator.

Since V_2 , is zero, all the signal voltages and currents associated with port 3 are zero and hence V_3 is zero which was assumed at the beginning of this explanation.

Thus it can be seen that this circuit acts as a circulator if, for each port, BD=AC. The gain between ports k and k+1 is:

$$\frac{B_{k+1}(C_k + D_k)}{D_k(A_{k+2} + B_{k+1})}$$

20 If a phase reversal between ports is required, operational amplifiers with a differential output may be used or a signal ended amplifier connected as a differential amplifier may be used as in FIG. 4 where the input terminals a, b may be interchanged to give phase reversal.

Using normal differential amplifiers and differential operational amplifiers, the input impedance at a port can be made equal to the impedance terminating the port if required but this is not necessary for operation as a circulator. The circuits may be designed to have a gain between ports of greater than unity but the circuit shown in FIG. 6 can only have equal input and terminating impedances when the gain is unity. This is because the input impedance at the port is A and if A=B then, because BD=AC, C must equal D. Putting A=B and C=D in the expression for the gain between ports it can be seen that the gain must be unity.

We claim:

- 1. An electrical network including a plurality of similar stages, each stage having an input terminal and an output terminal, two signal transmission paths connected in parallel from the input terminal of one stage to its output terminal, the paths including amplifying means of equal gains, but one of which produces at the output terminal the inverse of the signal from the other path at the output terminal, so that a signal applied to the input terminal of the stage is self-cancelling at its output terminal, and a connection from a port respective to the stage to a particular one of the paths to feed signals to the path or derive signals from it independently of the signals in the other path, the stages being connected in series, output terminal to input terminal, in a closed ring, whereby the network has the properties to a circulator connected to the ports.
 - 2. A network as claimed in claim 1, in which the two signal transmission paths connected in parallel in each stage comprise a differential amplifier and associated passive elements.
- 3. A network as claimed in claim 2, in which the differential amplifier is a differential, operational amplifier having a high gain, a high input impedance and a low output impedance and negative feedback is provided over the amplifier so that a desired gain is obtained.
- 4. A network as claimed in claim 2, in which the differential amplifier includes a long-tailed transistor pair.
- 5. A network as claimed in claim 4 in which the long-tailed pair is fed from a constant current source.
- 6. A network as claimed in claim 4, in which the long-tailed pair has its output connected with or without phase reversal to the next port by a common collector transistor stage.
 - 7. A network as claimed in claim 4 in which the long-tailed pair has its output connected with or without phase reversal to the next port by a common collector transistor stage.