A ballast control provided on a through-slot wave solderable daughter card package that is vertically mountable on a motherboard. The ballast drives a fluorescent lamp and cover is provided with internal ballast control circuit components mounted on circuit board.
For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.
BALLAST CONTROL CARD

BACKGROUND OF THE INVENTION

1. Field of the Invention:
   The present invention relates to a ballast control card, and more particularly, to a ballast control circuit provided on a through-slot wave solderable daughter card that is vertically mountable on a motherboard.

2. Description of the Related Art:
   Electronic ballasts for controlling fluorescent or high-intensity discharge (HID) lamps usually require electronics necessary for preheating the lamp filaments, striking the lamp, driving the lamp to a given power, detecting lamp fault conditions, and safely deactivating the circuit.

   Electronic ballasts for gas discharge circuits have come into widespread use because of the availability of power MOSFET switching devices and insulated gate bipolar transistors (IGBTs) that can replace previously used power bipolar switching devices. A number of integrated circuits (ICs) have been devised for driving gates of power MOSFETs or IGBTs in electronic ballasts. Examples include the IR2155, IR2157, and IR21571 products sold by International Rectifier Corporation and described in U.S. Pat. Nos. 5,545,955 and 6,211,623, the disclosures of which are incorporated herein by reference in their entireties.

SUMMARY OF THE INVENTION

The invention provides a fully integrated, fully protected 600V ballast control card designed to drive all types of fluorescent lamps. The ballast control card includes boost-type power factor correction (PFC) control and half-bridge ballast control for controlling a complete active power factor electronic ballast.
The ballast control card of the present invention incorporates the ballast control
IC with power factor correction disclosed in U.S. Patent Application Serial No.
09/981,753 filed October 19, 2001, the entire disclosure of which is incorporated
herein by reference, and includes, together with the IC, the two power FETs, the
PFC FET and related passive components.

In accordance with the present invention, ballast control circuitry,
including the control IC and FETs, is provided on a through-slot wave solderable
daughter card. The daughter card mounts vertically onto a mother board. Pads
surrounding a slot formed through the mother board are soldered to pads on the
vertical daughter card in a wave solder bath during production.

The ballast control card of the present invention greatly simplifies ballast
design and drastically reduces ballast component count. Externally
programmable features such as DC bus voltage level, preheat time and frequency,
ignition ramp characteristics, and running mode operating frequency provide a
high degree of flexibility for the ballast design engineer.

Comprehensive protection features such as protection from failure of a
lamp to strike, filament failures, asymmetrical lamp voltage (end-of-life), low AC
line condition, thermal overload, and lamp failure during normal operation, as
well as an automatic restart function, have been included in the design.

The ballast control card of the present invention has the following
features:
- Fully Integrated Ballast Control Card.
- Critical-Conduction Mode Boost Type PFC
- Half-Bridge Ballast Output
- Charge Pump Supply Input
- Programmable Preheat Time & Frequency
- Programmable Ignition Ramp
- Programmable Over-Current
- Internal Fault Counter
- Assymetrical Lamp Voltage Protection
- Lamp Filament Sensing & Protection
- Capacitive Mode Protection

5
- Brown-Out Protection
- Dynamic Restart
- Automatic Restart for Lamp Exchange
- Thermal Overload Protection
- Internal 15.6V Zener Clamp Diode on VCC

10
- Through-slot Wave-solderable Card Package

Other features and advantages of the present invention will become apparent from the following description of the invention which refers to the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

15
Fig. 1 is a typical application diagram for the ballast control card of the present invention.

Fig. 2 illustrates a top trace layer of the ballast control card of Fig. 1.

Fig. 3 shows a top solder mask for the ballast control card of Fig. 1.

Fig. 4 shows the top silk layer of the ballast control card of Fig. 1.

20
Fig. 5 shows a bottom trace layer of the ballast control card of Fig. 1.

Fig. 6 illustrates a bottom solder mask for the ballast control card of Fig. 1.

Fig. 7 illustrates bond wires of the ballast control card of Fig. 1.

Fig. 8 shows a bottom copper layer for a ballast motherboard according to the present invention.

Fig. 9 shows a top silk screen layer for a ballast motherboard according to the present invention.

Fig. 10 illustrates a bottom silk screen layer of a ballast motherboard.
according to the present invention.

Fig. 11 shows a bottom solder mask for a ballast motherboard according to the present invention.

Fig. 12 is a schematic diagram of a ballast control card circuit according to the present invention.

DETAILED DESCRIPTION OF EMBODIMENTS OF THE INVENTION

Referring to Fig. 1, a typical connection diagram for the ballast control card 2 of the present invention is shown schematically. The ballast drives a fluorescent lamp 4. A cover 6 is provided over internal ballast control circuit components (described further below) mounted on circuit board 8. The card typically is 37.05 mm by 14.5 mm. The thickness of the card is about 25 mils.

Programmable features of the ballast control, such as DC bus voltage level, preheat time and frequency, ignition ramp characteristics, and running mode operating frequency, are established by connecting external components to connecting pads provided on the edge of the ballast control card, as follows:

+ Rectified AC line input
BD Boost FET drain
ZX Zero-crossing, PFC inductor
BS Boost FET source

VBUS DC bus voltage level programming resistor
OC Over-current (SC+) threshold programming
RUN Run frequency resistor
RT Oscillator timing resistor
RPH Preheat frequency resistor and ignition ramp capacitor

25 CPH Preheat timing capacitor
VDC AC line turn-on voltage programming resistor
COM2 Programmable components ground
VCC Logic and low-side gate drive supply
HSD  High-side FET drain
VS   Half-bridge output
CP   Charge pump input
LS   Low-side FET source and current sensing input
5    COM1 IC power and signal ground
5    SD   Shutdown input

Typical external components are shown schematically in Fig. 1. The external components preferably are mounted on a mother board, which receives the ballast control daughter board, as described further below.

10   The ballast control receives power from a positive rectified AC line input which is applied, via transformer 10, to both the PFC circuitry and the main control circuitry. Resistor 12 allows external programming of a DC bus voltage level. An over-current threshold is established using resistor 14. Resistor 16 establishes a running mode frequency. Preheat timing is programmed by way of resistor 18 and capacitor 20. Capacitor 22 programs an ignition ramp.

15   Referring to Figs. 2-7, the mechanical layout of the ballast control card is shown. Fig. 2 illustrates top layer traces, and Fig. 3 shows a top solder mask. A top silk screen layer is shown in Fig. 4. Bottom trace layer is shown in Fig. 5. Fig. 6 illustrates a bottom solder mask. Bond wires are shown in Fig. 7.

20   Figs. 8-11 are mechanical drawings of the mother ballast board 40 according to the present invention. Mother board 40 includes a through-slot 42 which receives the connecting edge of ballast card 2. Fig. 8 illustrates a bottom copper layer on motherboard 40. Fig. 9 shows a top silk screen layer indicating a component layout, while Fig. 10 shows a bottom silk screen layer. Fig. 11 is a bottom solder mask for motherboard 40.

25   Referring to Fig. 12, a schematic diagram of internal and external circuitry for the ballast control card of the present invention is shown. Component labels correspond to those in other drawings, particularly Figs. 4 and 7 showing daughter card component layout. Note that the resistors labeled
RVBUS 1-3 in Fig. 12 corresponds to resistors RBUS 1-3 in Fig. 4. Also, CCOMP 1 and 2 in Fig. 4 are equivalent to CCOMP in Fig. 12. Similarly, whereas Fig. 12 shows two bootstrap capacitors CVCC 1 and 2, Fig. 4 includes an additional capacitor CVCC3. Capacitor CBOOT and resistor R7 as labeled in Fig. 12 correspond to capacitor CBS and resistor RLIM1, respectively, in the Fig. 4 layout.

The ballast control is built around IC 50, illustratively a product of assignee, International Rectifier Corporation, identified as the IR2167 IC. Further implementation details are provided in the IR2167 data sheet, available from International Rectifier Corporation and in pending U.S. Patent Application Serial No. 09/981,753, filed October 19, 2001, both of which are incorporated herein by reference in their entirety.

The ballast control card incorporates both the high and low side drive MOSFETS 52 and 54 and the power factor correction MOSFET (MPFC) on a single board.

Although the present invention has been described in relation to particular embodiments thereof, many other variations and modifications and other uses will become apparent to those skilled in the art. It is preferred, therefore, that the present invention be limited not by the specific disclosure herein, but only by the appended claims.
WHAT IS CLAIMED IS:

1. An electronic ballast comprising:
   a mother board; and
   a daughter board;
   wherein the daughter board is vertically mounted and electrically
   connected to the mother board.

2. The electronic ballast of claim 1, further comprising a plurality of
   power switching devices and a control IC for controlling the operation of said
   power switching devices, wherein said power switching devices and said control
   IC are disposed on said daughter board.

3. The electronic ballast of claim 1, wherein said daughter board includes
   edge connectors for electrically connecting to said mother board.

4. The electronic ballast of claim 1, further comprising external
   components disposed on said mother board and control components for providing
   programmable features disposed on said daughter board.

5. The electronic ballast of claim 4, wherein said programmable features
   include at least one of DC bus voltage level, preheat time and frequency, ignition
   ramp characteristics, and running mode operating frequency.
Top Layer

FIG. 2
Top Solder Mask

Fig. 3
Top Silk Layer

FIG. 4
Bottom Solder Mask

Fig. 6
Bond Wires
NOTES:
Layer 1
Fluxing none
Silk screen layers 1, 2, 4
Silk screen 8: Stencil both sides
Screen color white
Inside track to be 0.032 X of original artwork.
Silk screen to be black perforated fabric.
Green lacquer to be F2PFS-9390 glass epoxy laminate.
Solder mask on both sides using non-conductive finish, except pads.
No level all exposed copper.
All parts side 300-12 to be clearly marked on PCB.
Dy green liquid photo imaging soldermask over bare copper.

Bottom Copper Layer

Fig. 8
NOTES:
Number of layers: 1
Plating near
both ends

colored type: 158 green

colored sides: Both sides

solder mask: white
taped track to be 20% of overall area

data is given in 10 millimeter

distances are given in 0.5

decimals of millimeter

diy silk-screen in both sides using non-conductive white, opaque ink paint.
clear all exposed copper

star 15 item code 399-0 to be clearly marked on PDB

diy green liquid photo-leachable soldermask over bare copper

Top Silk Screen Layer

Fig. 9
NOTES:
- Number of layers: 1
- Etching type: 40% copper
- Soldermask type: 60% Green
- Soldermask: Both sides, screen printed white
- Soldermask thickness: to be 20% of original artwork
- Date air gap: 10 mils
- Stencil to be F2 per MIL-STD-1890 class 9919
- Dip all areas on both sides using non-conductive white, epoxy type paint
- Derivate all exposed copper
- Dip seal side 300-90 to be clearly marked on FCB
- Dip green liquid photo image soldermask over bare copper

Bottom Solder Mask
### INTERNATIONAL SEARCH REPORT

**International application No.**
PCT/US02/98561

**A. CLASSIFICATION OF SUBJECT MATTER**

IPC(7): G06F 1/00
US CL: 515/991

According to International Patent Classification (IPC) or to both national classification and IPC

**B. FIELDS SEARCHEDE**

Minimum documentation searched (classification system followed by classification symbols)

- U.S.: 515/991, 209R, 224, Dig.7; 561/1, 2, 42, 45, 54, 56, 57

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

USPTO APS EAST

**C. DOCUMENTS CONSIDERED TO BE RELEVANT**

<table>
<thead>
<tr>
<th>Category*</th>
<th>Citation of document, with indication, where appropriate, of the relevant passages</th>
<th>Relevant to claim No.</th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td>US 6,211,623 B1 (WILHELM et al) 03 April 2001 (03.04.2001), figures 2-3; column 21.</td>
<td>1-5</td>
</tr>
<tr>
<td>X</td>
<td>US 6,310,440 B1 (LANSING et al) 30 October 2001 (30.10.2001), figures 1-4; column 10.</td>
<td>1, 2, 4</td>
</tr>
<tr>
<td>A</td>
<td>US 6,157,093 A (GIANNOPoulos et al) 05 December 2000 (12.05.2000), figures 1-4; columns 2-5.</td>
<td>1-5</td>
</tr>
</tbody>
</table>

Further documents are listed in the continuation of Box C. See patent family annex.

- "A" document defining the general state of the art which is not considered to be of particular relevance
- "B" earlier document published on or after the international filing date whose publication date is not cited to establish the publication date of another citation or other special reason (as specified)
- "C" document referring to an oral disclosure, use, exhibition or other means
- "E" document published prior to the international filing date but later than the priority date claimed
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- "X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
- "Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
- "Z" document member of the same patent family

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Date of mailing of the international search report

10 APR 2003

Authorized officer
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Telephone No. (703) 605-5879