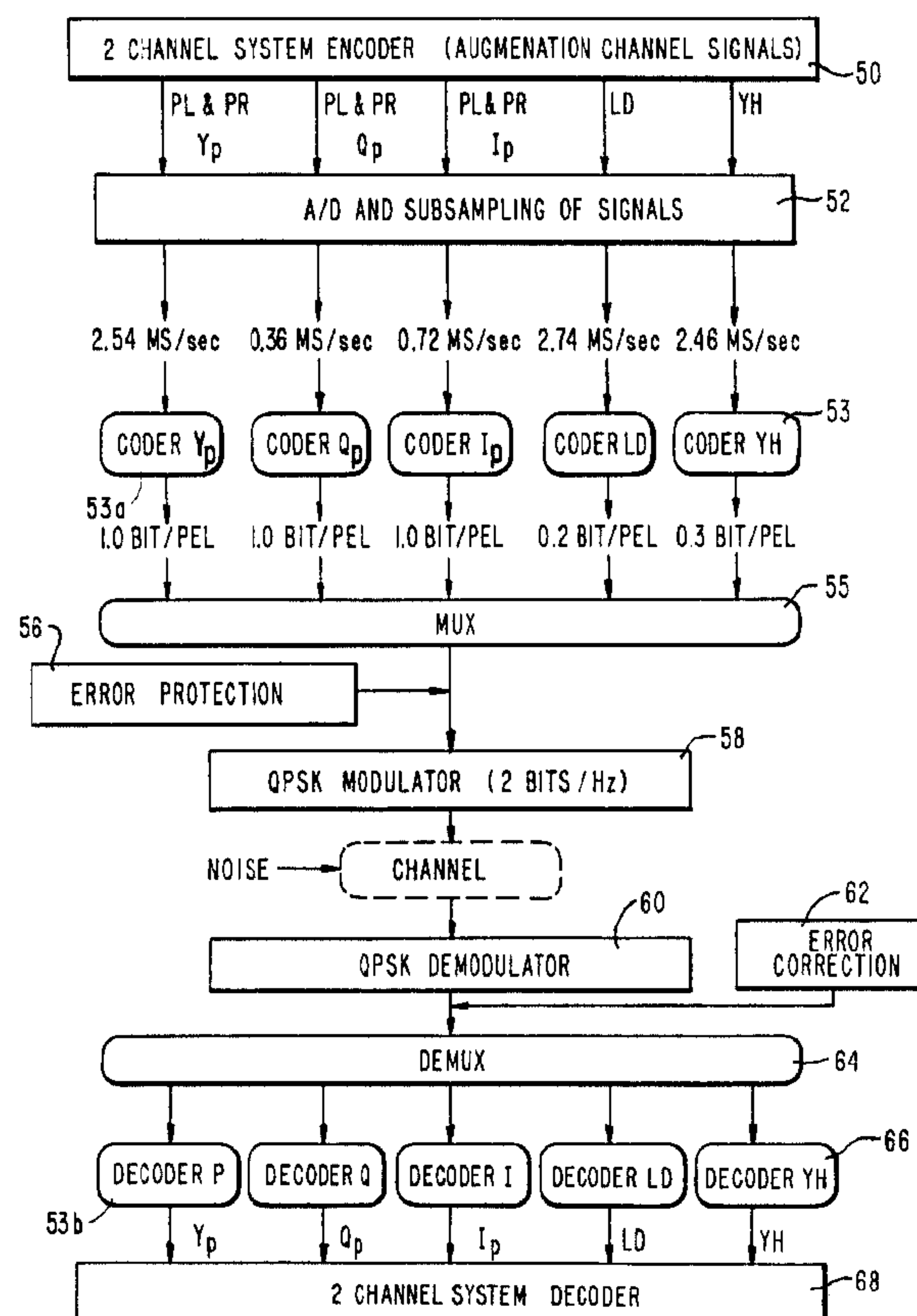




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(54) Titre : METHODE ET DISPOSITIF DE TRAITEMENT NUMERIQUE DE SIGNAUX D'AUGMENTATION DE TELEVISION A HAUTE DEFINITION
(54) Title: METHOD AND APPARATUS FOR DIGITALLY PROCESSING A HIGH DEFINITION TELEVISION AUGMENTATION SIGNAL



(57) Abrégé/Abstract:

A method and apparatus for digital encoding are described for compressing the augmentation channel signals (chrominance and luminance signals for panel information and high frequency luminance and line difference signal) so that this information



(57) Abrégé(suite)/Abstract(continued):

can be transmitted in a 3 MHz wide RF channel using a digital transmission scheme such as QPSK. Analog signal components are sampled and converted to digital signals. Each of the signals is fed into a separate coder which reduces the number of bits/pixel required to reconstruct the original signal. Compression is achieved by quantization and removal of redundancy. The compression scheme is based on the use of DCT together with VLC. Each augmentation signal has its own coder, which is adapted to the unique statistics of this signal.

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ABSTRACT:

Method and apparatus for digitally processing a high definition television augmentation signal.

5 A method and apparatus for digital encoding
are described for compressing the augmentation channel
signals (chrominance and luminance signals for panel
information and high frequency luminance and line
difference signal) so that this information can be
transmitted in a 3 MHz wide RF channel using a digital
10 transmission scheme such as QPSK. Analog signal components
are sampled and converted to digital signals. Each of
the signals is fed into a separate coder which reduces
the number of bits/pixel required to reconstruct the
original signal. Compression is achieved by quantization
15 and removal of redundancy. The compression scheme is
based on the use of DCT together with VLC. Each augmen-
tation signal has its own coder, which is adapted to the
unique statistics of this signal.

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Method and apparatus for digitally processing a high definition television augmentation signal.

BACKGROUND OF THE INVENTION

The present invention relates to a method and
5 apparatus for digitally processing the components of an
augmentation signal as part of a multi-channel high definition
television (HDTV) delivery system. Such a system has been
described for example in U.S. Patent 4,694,338. In such a
system, an HDTV source signal, having for example a 16:9 aspect
10 ratio and a 525 sequentially scanned or 1050, 2:1 interlaced
line structure, is divided into two signals. A conventional
television signal, for example an NTSC encoded signal
receivable on a standard broadcast receiver, is transmitted
over a regular television transmission medium, for example a
15 standard television channel and an augmentation signal
providing the additional wider aspect ratio and high resolution
information of the source signal is transmitted over a second
transmission medium, for example a second television channel or
part of one. A high definition receiver can then be used to
20 receive and combine both signals into a high definition
television display.

SUMMARY OF THE INVENTION

The applications referred to hereinabove describe
systems utilizing analog augmentation signal configurations.
25 For example, systems using a standard 6 MHz wide NTSC channel
and a 3 MHz wide augmentation channel which could be
transmitted on a presently unassigned television channel. The
only available terrestrial channel capacity however, appears to
be the so called "taboo" channels which are currently
30 restricted

for television transmission. If however, the amount of power needed to transmit the augmentation signal on such a channel could be effectively reduced, use of these "taboo" channels could become practical.

5 The instant application comprises a digital processing method and apparatus which digitally encodes the augmentation signal components compressing them so that the information they provide can be transmitted in a narrow RF channel having for example a 3 MHz wide
10 bandwidth, using a digital transmission scheme such as QPSK (quadrature phase shift keying). This permits a significant reduction of transmitted power on the augmentation channel, subsequently reducing the amount of interference to other channels using the same frequency band.
15 Digital transmission of the augmentation signal not only permits the use of reduced power, but also enables taking advantage of the various known error detection/correction schemes, so that a better quality signal can be achieved.

 A major disadvantage of digital transmission
20 is, however, the increase in the transmission bandwidth necessary. The increased bandwidth requires either the use of a channel with a wider bandwidth or implementation of data compression schemes to reduce the required bandwidth. The invention comprises an approach for
25 encoding the enhancement signals based on the latter solution.

 Extensive research in the area of image coding has shown that two-dimensional (2-D) discrete block cosine transform (DCT) encoding has attractive performance
30 compared to other encoding techniques while being practical for hardware implementation. However, these investigations have traditionally dealt with standard full-band signals. The compression scheme used herein is a modified version of one described in a paper entitled
35 "Adaptive Intra/Inter Frame DCT Coding of TV Pictures", June 1988, C. Remus (LEP Philips, France) and the implementation of a two-dimensional DCT with VLC for

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full band two-dimensional signals (regular images) was first introduced by W. Chen and W.K. Pratt in a paper entitled "Scene Adaptive Coder" (IEEE Transaction on Communications, March 1984). The results of these studies cannot be readily extended
5 to the encoding of augmentation signals which in part possess only high frequency content.

Augmentation signal components derived using for example, an encoder first described in U.S. Patent 4,694,338 (issued on September 15, 1987), and comprising, for example, a
10 luminance panel signal Y_p , two chrominance panel signals (I_p and Q_p), a high frequency luminance signal Y_H and a line difference signal LD , are those processed in accordance with the invention. The instant invention takes these augmentation signal components, samples them and converts them into for
15 example, 8 bit per pixel digital signals. Each of these digital signals is then fed into a separate coder which reduces the number of bits per pixel required to reconstruct the original signal components. This compression is achieved by quantization and removal of redundancy. By quantization, we
20 mean the elimination of certain information. The compression scheme is based on the use of DCT (discrete cosine transform) processing in combination with VLC (variable length coding) and each augmentation signal component has its own coder, which is adapted to its unique characteristics.

25 BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a diagram of an encoder described in U.S. Patent No. 4,694,338.

Figure 2 is a diagram of a high definition NTSC (HDNTSC) encoder described in U.S. Patent No. 4,873,567.

Figure 3 is a flow diagram representing a general description of the digital processing and transmission scheme of the instant invention.

Figure 4a describes one embodiment of a coder for the panel information.

Figure 4b describes one embodiment of a decoder for panel information.

Figure 5 describes the reordering of processed panel information.

10 Figure 6 is a graph representing the buffer regulation procedure.

Figure 7 is a graph describing the criteria for determining the weights for panel information.

Figure 8 describes one embodiment of an LD encoder.

Figure 9 describes one embodiment of an LD decoder.

Figure 10 describes the reordering of LD information.

Figure 11 describes one embodiment of a YH coder.

Figure 12 describes one embodiment of a YH decoder.

Figure 13 describes the reordering of YH information.

20 Figure 14 is Table 1 which shows how the number of Mega-samples/sec is computed for each signal component.

Figure 15 is Table 2 which illustrates the computation of bit rate for each signal component and the combined signals.

DETAILED DESCRIPTION OF THE INVENTION

Figure 1 is one embodiment of an encoder which can be used to derive luminance and chrominance signal components for both center and panel portions of a high definition television

4a

source signal. The operation of this encoder 10 and its use in the derivation of an augmentation signal is fully described in the '338 patent in which this figure appears as Fig. 4. As explained therein, a HDTV source is processed and outputs 18, 20 and 22 of the 3-channel demultiplexer 32 provide respectively, a luminance (Y_c), and two

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chrominance components, for example Q_C and I_C , for the center portion of the HDTV source. This center portion presents picture information which, as taught by the '338 patent, is then NTSC encoded and transmitted over one standard television channel. The outputs 12, 14 and 16 of 3-channel demultiplexer 32 provide respectively Y_p , Q_p and I_p components for the panels derived from the HDTV source signal.

Figure 2 describes an HDNTSC encoder which utilizes the encoder 10 in conjunction with bandpass filter 35 to derive a high frequency luminance component YH from the HDTV source signal. This encoder is disclosed as Fig. 2a of the 4,873,567 patent which describes a system providing extended horizontal resolution of luminance and chrominance in a high definition television system. The YH component 36 is available at the output of the bandpass filter (BPF) 35. A line difference (LD) signal component is available at output 38.

The described embodiment of the instant invention provides for the processing and transmission of the derived augmentation signal in an approximately 3 MHz wide RF channel. The augmentation signal consists, for example, of the following signal components: Y_p , I_p , Q_p , LD and YH.

A flow diagram of one embodiment of the digital compression and transmission scheme of the invention is shown in Figure 3. Each of the signal components is fed through a separate analog to digital converter (A/D) which uses a sampling frequency approximately twice the bandwidth of the respective signal component. In this way the lowest possible number of samples/sec is obtained before coding. The analog augmentation

signal components Y_p , Q_p , I_p , LD and YH are bandlimited as described in Table 1. Like the applications cited herein, the augmentation signal of the instant invention utilizes a line period of approximately 127 μ s and better known and described in these applications as a "superline". Fig. 14 shows how the number of Megasamples/sec. is computed for each of the signal components. After sampling, each of the digital signal components is converted into a stream of 8 bit pixels or samples 52. The resulting number of megasamples/sec for the signal components is 2.54 MS/sec, 0.36 MS/sec, 0.72 MS/sec, 2.74 MS/sec, and 2.46 MS/sec for Q_p , I_p , LD and YH, respectively. The digital signal components are then passed through separate coders labeled CoderP, CoderQ, CoderI, CoderLD, and CoderYH 53. Average resulting compression rates are about 1.0 bits/pixel for Y_p , I_p and Q_p . Rates of about 0.2 bits/pixel for LD and about 0.3 bits/pixel for YH have also been achieved.

The digital signal components are then multiplexed into a single bit stream 55. Based on previous computations of MS/sec and average compression rates, this bit stream will have bit rate of about 4.91 Megabits/sec. With an additional overhead of 20% added for error protection (see below) the bitrate is 5.89 Mb/sec.

Computation of bit rate for each of the signal components and the combined signal is illustrated by Fig. 15.

The column of Fig. 15 marked "Coding Rate" indicates the operating rate of the system for each of the signal components. This constraint is imposed on each coder.

Conventional error protection/compensation methods can be used 56 to process the bit stream prior to modulation and transmission in order to mitigate the effects of noise in the transmission channel medium. The bit stream can be transmitted in a 3 MHz wide RF channel using for example a 2 bit/sec./Hz QPSK transmission scheme 58.

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At the receiving end, the QPSK bit stream is received and demodulated 60, and any error protection/compensation method used is compensated for 62. The demodulated bit stream is then demultiplexed into individual compressed digital augmentation signal components Y_p , Q_p , I_p , LD and YH 64. These compressed signals are then decoded by passing each signal through its own decoder 66. The recovered digital augmentation signal components can now be converted back into analog form and fed into a 2 channel decoder 68 which is fully described in for example, the U.S. Patent No. 4,873,567.

The block diagram of an embodiment of a coder for panel information, i.e. Y_p , I_p , or Q_p , is shown in Fig. 4a. The panels from two consecutive fields are combined to produce one panel frame. More specifically, the even numbered lines of even numbered fields are interleaved with odd numbered lines of odd numbered fields. The resulting combination is regarded as one frame of panels and focus the input 100 of the panel encoder 53a. The frame is partitioned into separate blocks of equal size N, where $N = 16$ and two-dimensional (2-D) discrete cosine transform (DCT) processing is applied separately and independently on each block using transform means 110.

The coder 53a operates on a block by block basis and performs the same series of operations on each block. Its operation therefore, will be described only for one block represented by $x(i,j)$. Here, we will assume that the blocks in one frame are indexed from left to right and top to bottom (i.e., similar to a raster scan format) and the indexing is continued in a similar fashion for subsequent frames. After the 2-D DCT transformation, the dc coefficient, $X(0,0)$, which represents the average gray level or luminance of the block, is separately quantized using for example a 9-bit quantizer 112 (a simple float to integer rounding operation), the output of which is then provided to

multiplexer 115. The rest of the coefficients $X(u,v)$, where $\{u,v = 0,1,\dots,N, N-1; (u,v) \neq (0,0)\}$, are treated separately as described below. The activity of each block, which is indicative of amount of detail (for example edge content) of the block, is then calculated and classified using block classification means 114 according to the formula:

$$A(m,n) = \max_{(u,v) \neq (0,0)} |X(u,v)|$$

$$u,v = \{0,1,\dots,N-1\},$$

where $A(m,n)$ represents the activity of the block (m,n) . The block is then assigned to one of $K = 4$ activity classes, using a fixed set of decision levels

$$0 = \tau_0 < \tau_1 = 10 < \tau_2 = 25 < \tau_3 = 50 < \tau_4 = 255.$$

That is, block (m,n) is assigned to class k if $\tau_{k-1} \leq A(m,n) < \tau_k$. The assigned class of the block requires two bits ($\log_2 4$) of information to be uniquely identifiable. The assigned class along with the normalization factor, (described below) are then used to select a set of weights suitable for that class and normalization factor. Selection of the appropriate weights takes place using weighting means 116. The weights associated with all coefficients indexed by $n = (u+v)/2$, where $n = 0,1,\dots,2(N-1)$ are calculated according to the formula:

$$\omega_i(n) = \omega_i(N-1) + [\omega_i(N-1) - 1] (n - N + 1) / (kN),$$

where i indicates the block number or the operating state. Calculation of these weights is illustrated by the graph of Figure 7. As is clear from the previous expression, the weight assigned to each coefficient depends on the calculated value of $\omega_i(n-1)$, referred to as the central coefficient or the normalization factor which is in turn evaluated using normalization means 124 according to formula

$$\omega_i(N) = f(\omega_{i-1}(N), b_s).$$

Here, $f(.)$ is a piece-wise linear function having a huffer status (b_s) as shown in the graph of Figure 6.

The buffer status is described as the ratio of number of bits in the buffer 12 to the buffer size.

All the transform coefficients, except for the dc coefficient, are divided by the weights calculated as above 118 and then quantized using a simple float to integer rounding operation in quantizer 120. The output of the quantizer 120, $\tilde{x}(u,v)$, can then be reordered (scanned) 122 using the pseudo zig-zag scanning pattern illustrated in Fig. 5 in order to provide better match for the variable-length coder (VLC) 128.

The VLC 128 consists of several tables, each designed for a specific normalization value $\omega_i(N-1)$, and activity class, k . The normalized values provide a better match to input statistics than previously provided by single coders such as those described by the prior art. The appropriate table, selected based on the normalization value and class assignment, is then used to encode $\tilde{x}(u,v)$ to the VLC 128. The output of VLC 128 is fed to buffer 126 for further preparation (channel coding and modulation) for transmission. The status (b_s) of the buffer 126 is then updated and the normalization value for the next block, $i+1$, is calculated using normalization means 124. The output of buffer 126 is combined with the output of quantizer 112 and the respective block class provided by block classification means 114, in multiplexer 115. The multiplexed output is then modulated on to a carrier in modulator 117 and transmitted over part (i.e. 3 MHz) of a television channel 119.

The role of the decoder 53b, in the absence of transmission errors, is to recover the digital signal components input to the coder 53a, allowing for some degradation due to quantization depending on the operating rate of the system.

Figure 4b describes one embodiment of a decoder for panel information, i.e. Y_p , I_p or Q_p . The information on channel 119 is demodulated by demodulator 121 and

the dc coefficient $\hat{\chi}(0,0)$ is separated from the rest of the coefficients and the respective assigned block class in demultiplexer 125 and provided to inverse DCT transformation means 123. The rest of the demultiplexed coefficients are input to buffer 130. The output of the buffer 130 is fed to the variable-length decoder (VLD) 132 while the status of the buffer 130 is used to calculate, using normalization means 134, the normalization value used in the coder 53a. The respective assigned block class is provided from demultiplexer 125 to weighting means 13b. The normalization value from 134 and the assigned block class 125a from demultiplexer 125 are input to and thereby enable the VLD 132 to select the table used in the VLC 128 and therefore to recover the value of the coefficients, $\tilde{\chi}(u,v)$. The resulting coefficients are then processed 132a to compensate for any recording process used during encoding. Weighting means 13b derives the weight factors used in encoder 53a for the coefficients (using the block class and normalization factors) and these factors are then combined in multiplier 140 with the processed coefficients from VLD 132. Along with the dc coefficients, $\hat{\chi}(0,0)$, coefficients $\hat{\chi}(u,v)$ are inverse transformed in inverse DCT means 123 to provide the output of the decoder $\hat{\chi}(i,j)$.

The encoding and decoding procedures for LD components are similar to those for the panel components as shown in block diagrams Figs. 8 and 9. Because of peculiar nature of the LD component, there is no weighting of the DCT coefficients. That is, all the coefficients are normalized using the same normalization value. In addition, the (0,0) coefficient in DCT domain is treated the same as the rest of coefficients. Furthermore, the recording method using for LD is chosen to better suit the statistical properties of this signal and is shown in Fig. 10. Test results showed that the value of the normalization factor is

usually small and therefore only one codebook is used in the VLC and the normalization value is taken as a real number.

5 Block diagrams representing the operation of
embodiments of an encoder and decoder for YH are shown
in Figs. 11 and 12. The operation of the encoder for YH
is very similar to that for LD except that the reordering
process, shown in Fig. 13, is selected to better suit
the properties of the YH component. In the above described
10 embodiments, the means for transforming, normalizing
weighting and variable length encoding/decoding the
signal components can be accomplished using hardware
or a computer program. Persons skilled in the art
will be able to provide the means shown and use them in
15 accordance with the instant invention.

 The foregoing disclosure and description
of the invention is illustrative and explanatory thereof
and various changes in the details of the embodiments
shown may be made within the scope of the appended
20 claims without departing from the spirit of the invention.

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CLAIMS:

1. An apparatus for decoding a video signal, said video signal comprising a plurality of coded components encoded thereon by deriving a plurality of signal components from a video source signal comprising a plurality of frames which are partitioned into a plurality of separate blocks and processed on a block by block basis so as to determine the activity of each block, digitizing each of said signal components, coding each of said digitized signal components in a manner optimized for each respective component, and modulating said coded components to form said video signal, said apparatus comprising:

a) demodulation means for deriving from said video signal, said coded components;

b) means for decoding each of said coded components in a manner optimized for each of said respective components so as to form a plurality of decoded components; and

c) means for combining said decoded components into a video display.

2. The decoding apparatus as described in claim 1 wherein the activity of each block is classified according to the formula $A(m,n) = \max |X(u,v)|$ wherein m , n , u and v are integers; u and v are not equal to zero, $A(m,n)$ represents the activity of the block (m,n) and $X(u,v)$ represents respective coefficients used to process each of said blocks.

3. The decoding apparatus of claim 1 wherein said video signal is encoded so as to assign each activity to one of a plurality of activity classes, wherein each assigned class

together with a selected normalization factor is used to select a set of weight suitable for that class and normalization factor.

4. An apparatus for encoding a video source signal
5 comprising a plurality of frames, said apparatus comprising:

a) means for deriving from said video source signal, a plurality of signal components;

b) digitizing means coupled to said deriving means, for digitizing said signal components so as to form a plurality
10 of digitized components;

c) coding means coupled to said digitizing means for processing said digitized components by partitioning each frame into a plurality of separate blocks and processing each block so as to determine and classify its activity, and by processing
15 each of said digitized components in a manner optimized for each of said respective components so as to provide a plurality of coded components; and

d) means coupled to said coding means, for combining said coded components so as to form a video signal.

20 5. The apparatus described in claim 4 wherein said coding means further comprises a block classification means which calculates and classifies the amount of detail presented by each of said blocks according to the formula $A(m,n) = \max |X(u,v)|$

25 wherein m , n , u and v are integers; u and v are not equal to zero, $A(m,n)$ represents the activity of the block (m,n) and $X(u,v)$ represents respective coefficients used to process each of said blocks.

6. The apparatus of claim 5 further comprising means for
assigning said activity to one of a plurality of activity
classes, wherein each assigned class together with a selected
normalization factor is used to select a set of weights
5 suitable for that class and normalization factor.

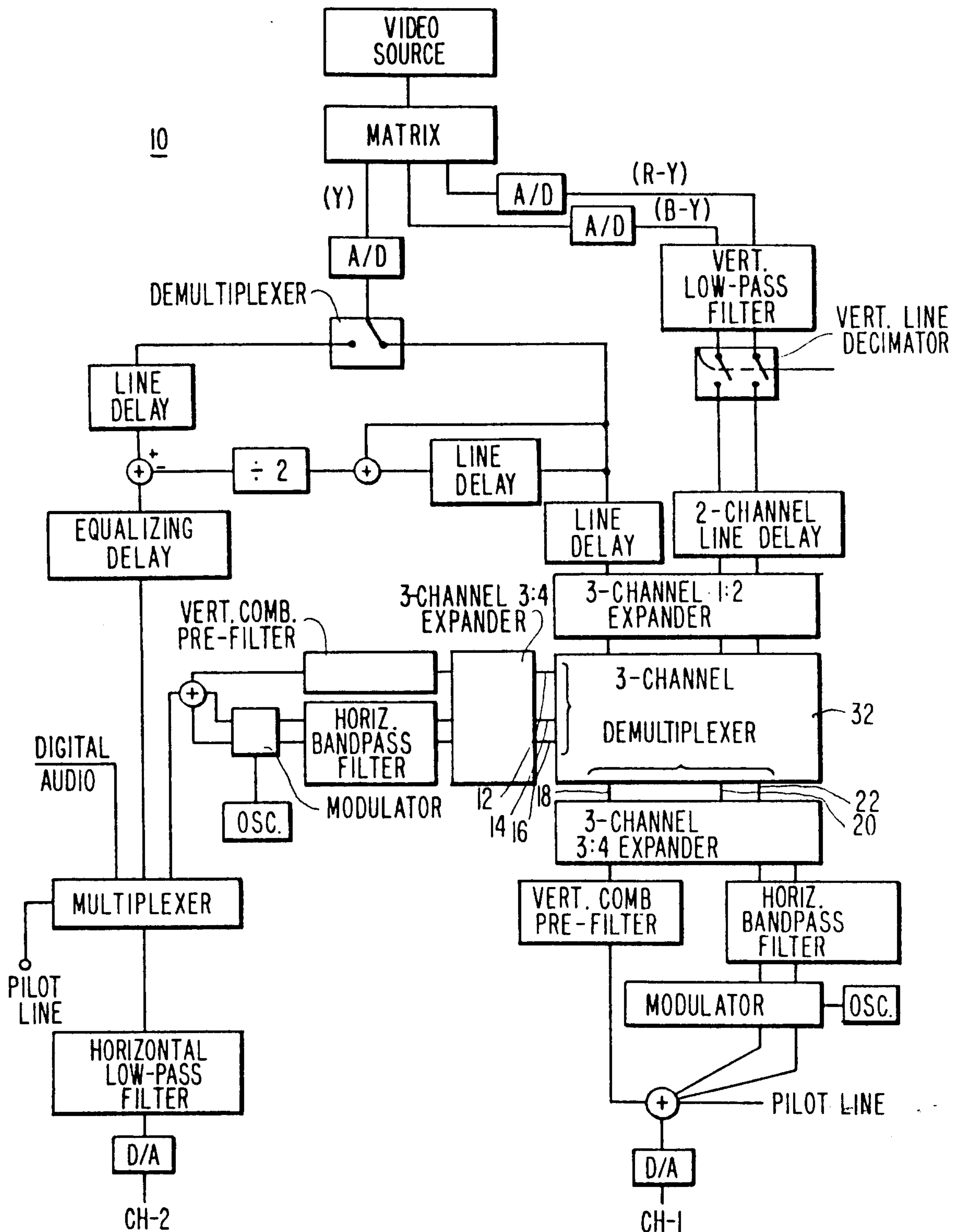
FETHERSTONHAUGH & CO.

PATENT AGENTS

OTTAWA, CANADA

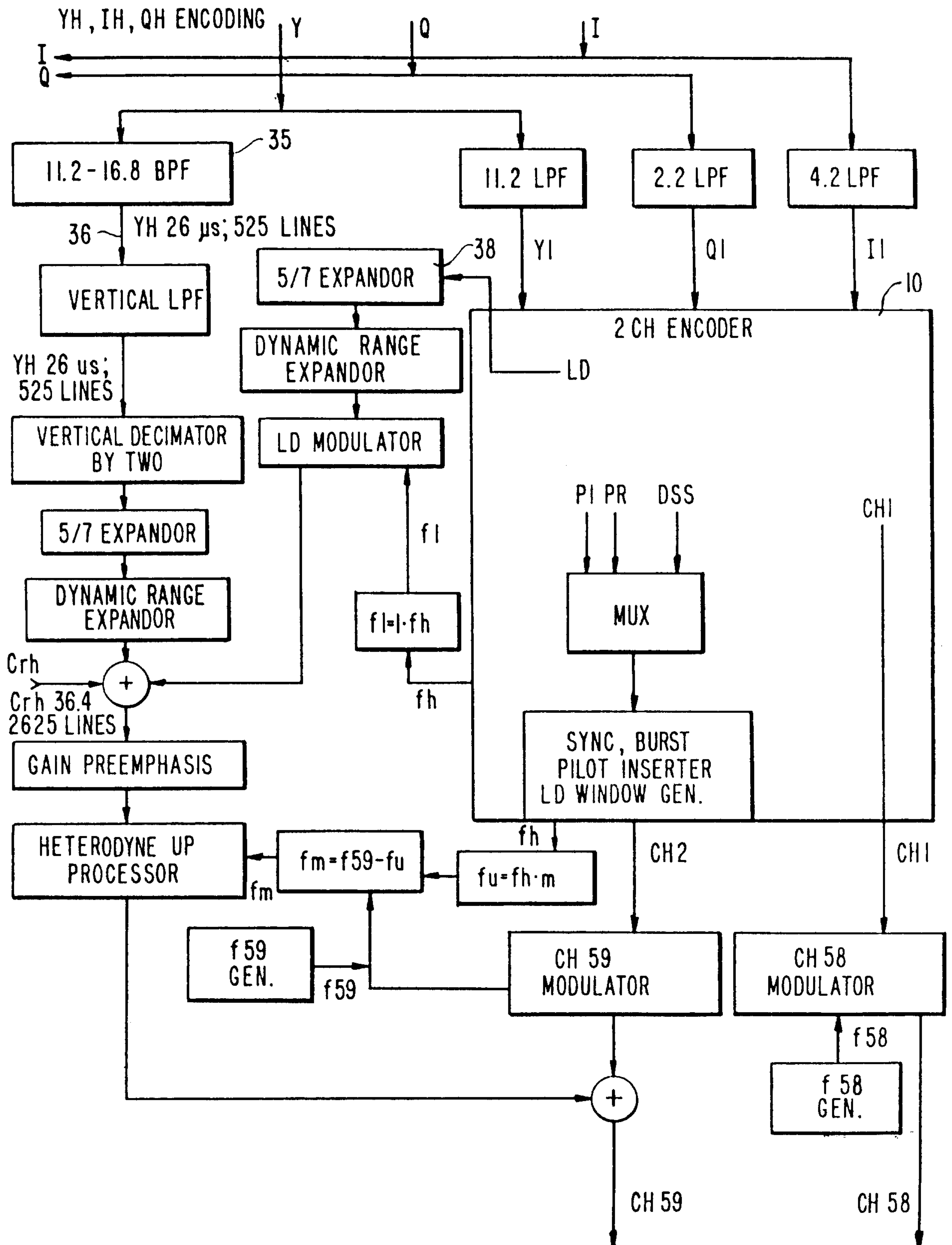
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FIG. 1
PRIOR ART



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FIG. 2



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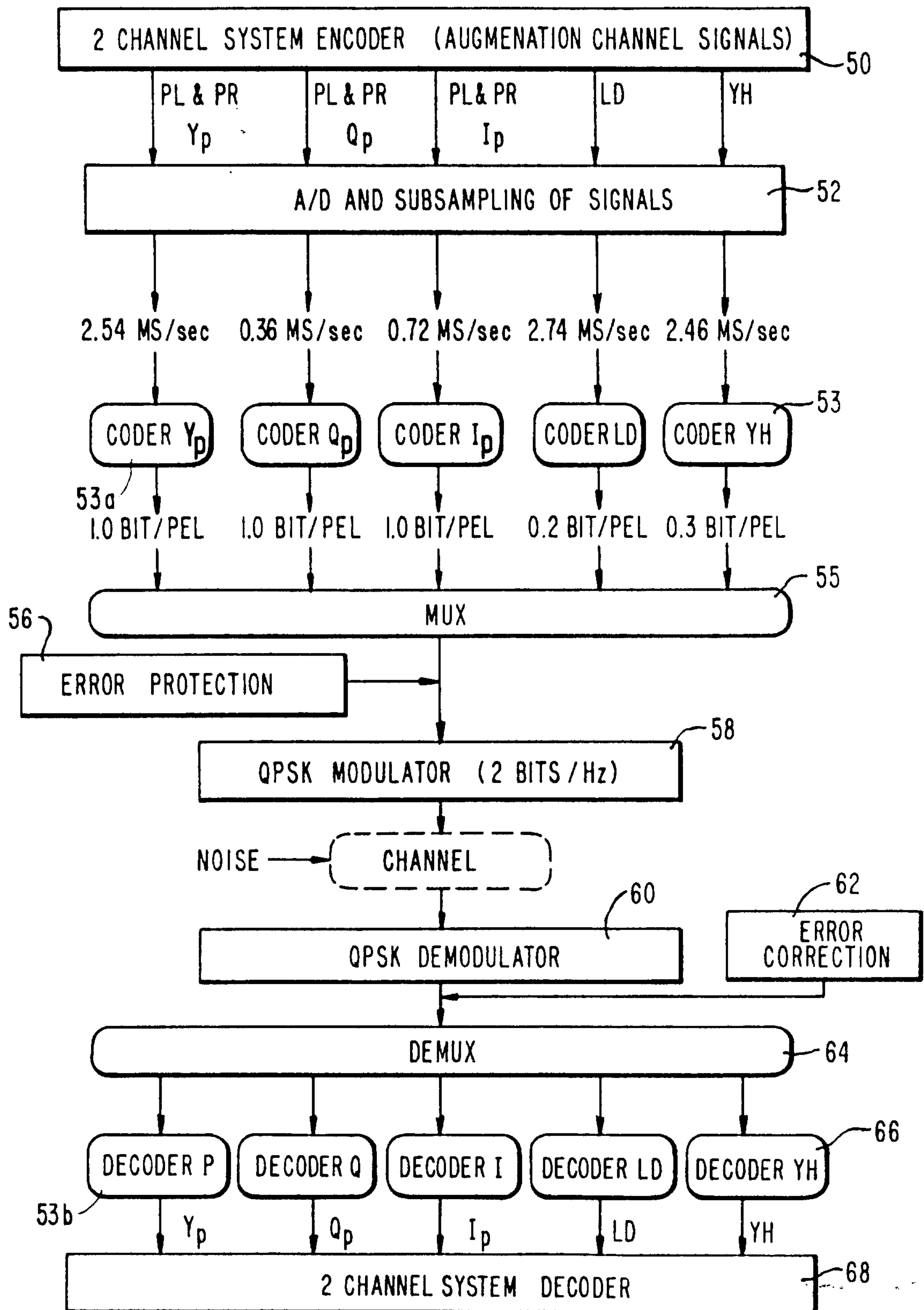


FIG. 3

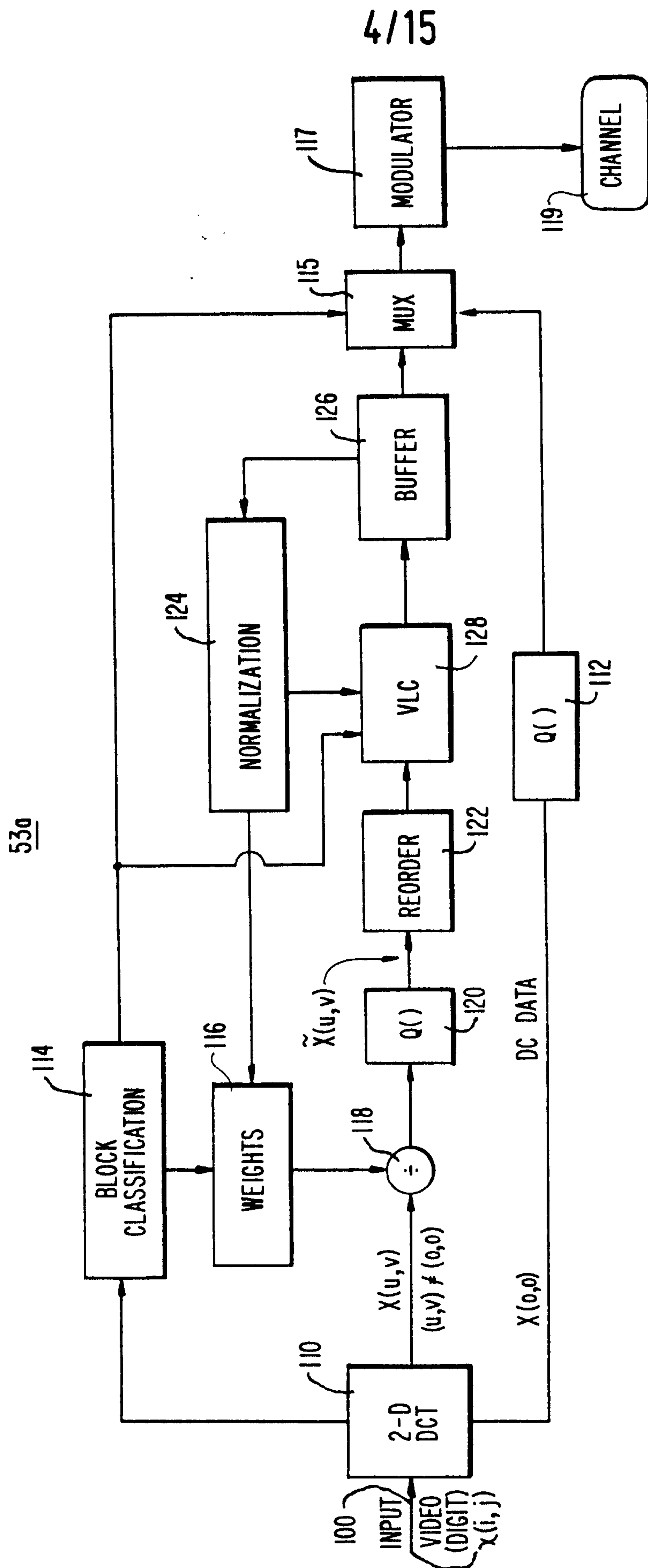


FIG. 4a

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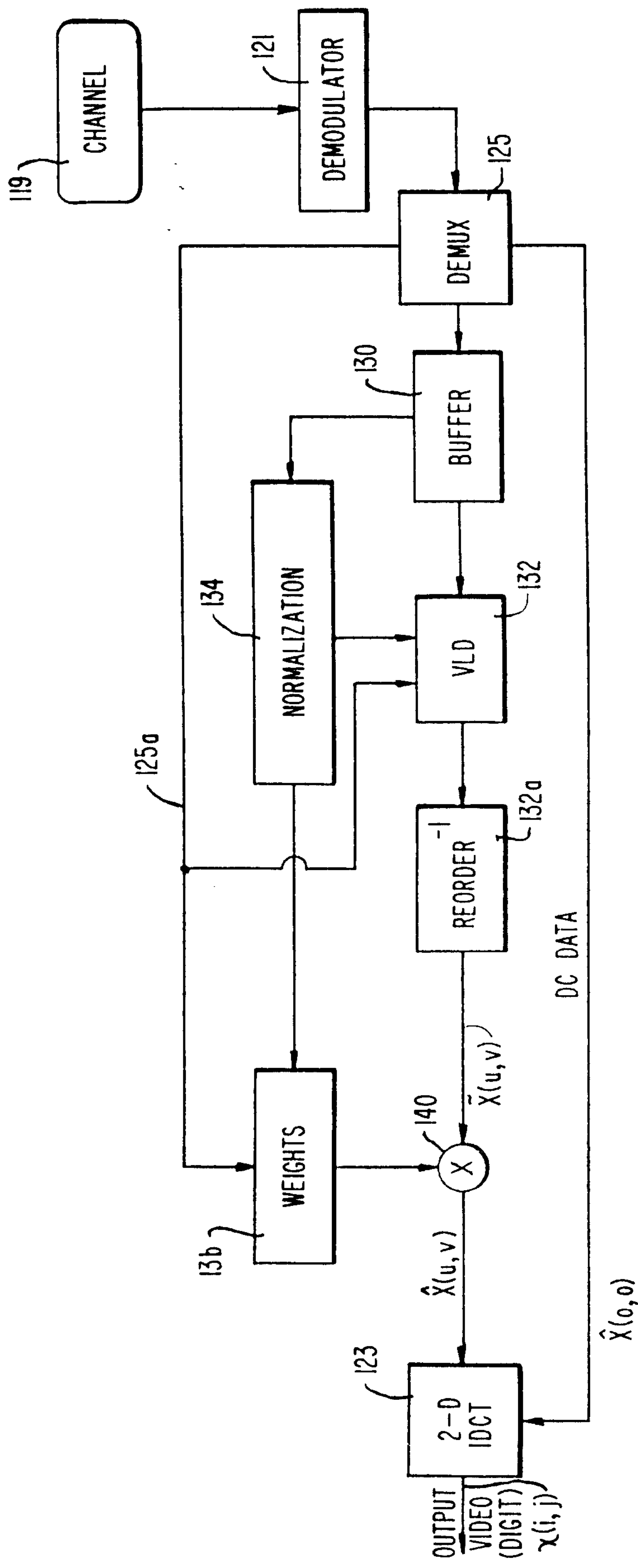
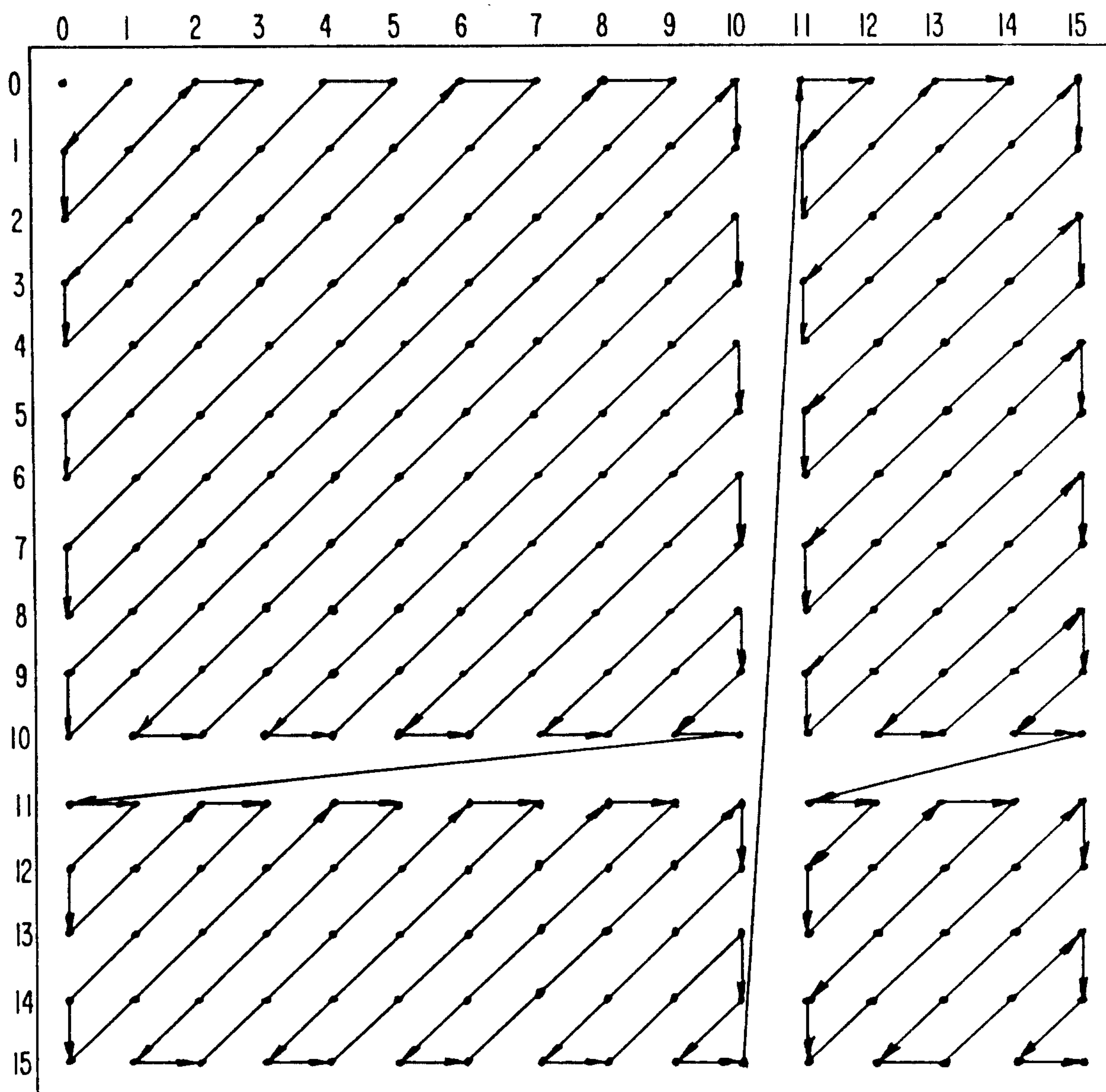


FIG. 4b

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FIG. 5

(REORDERING) SCANNING OF PANEL INFORMATION



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FIG. 6

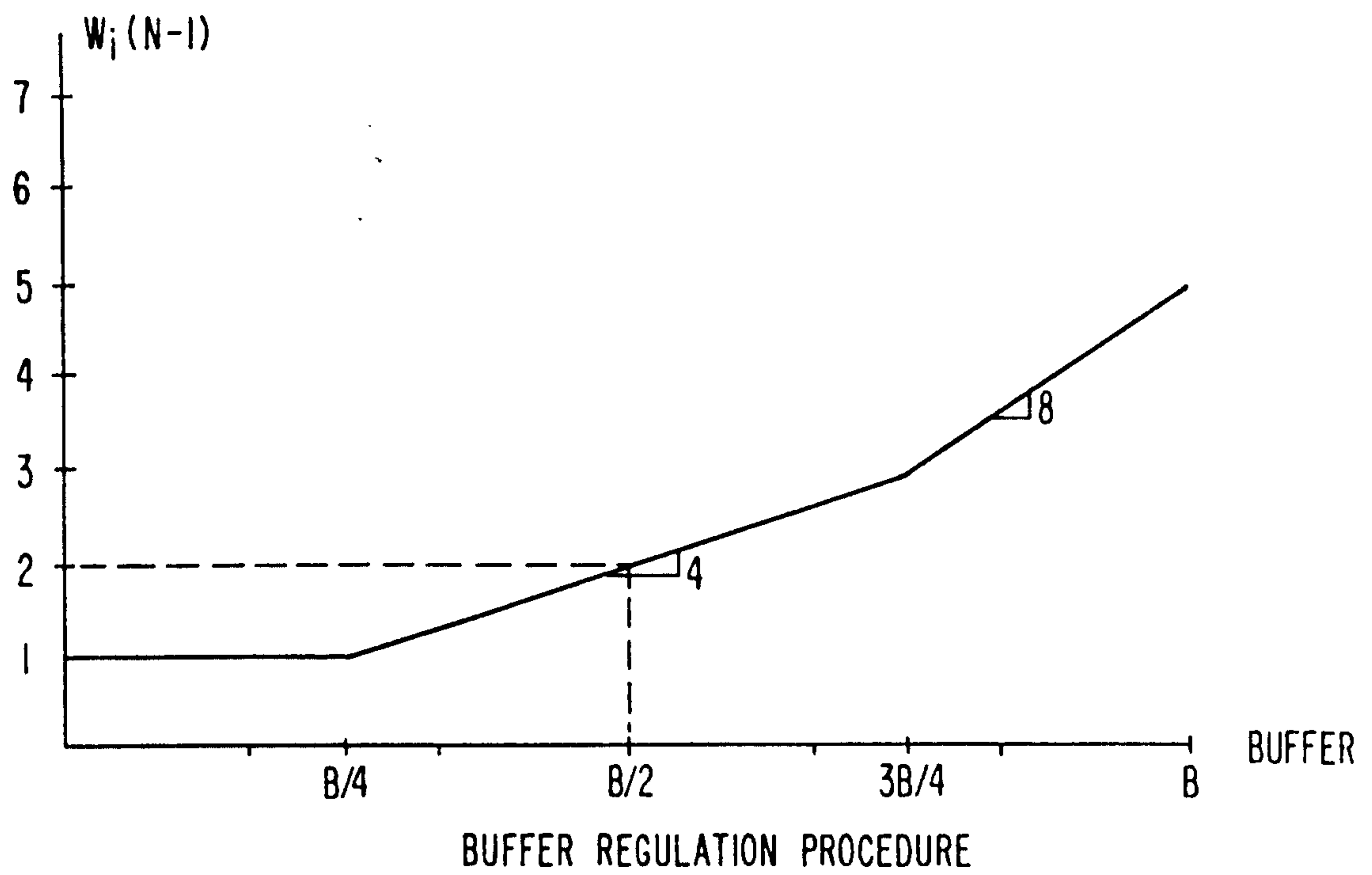
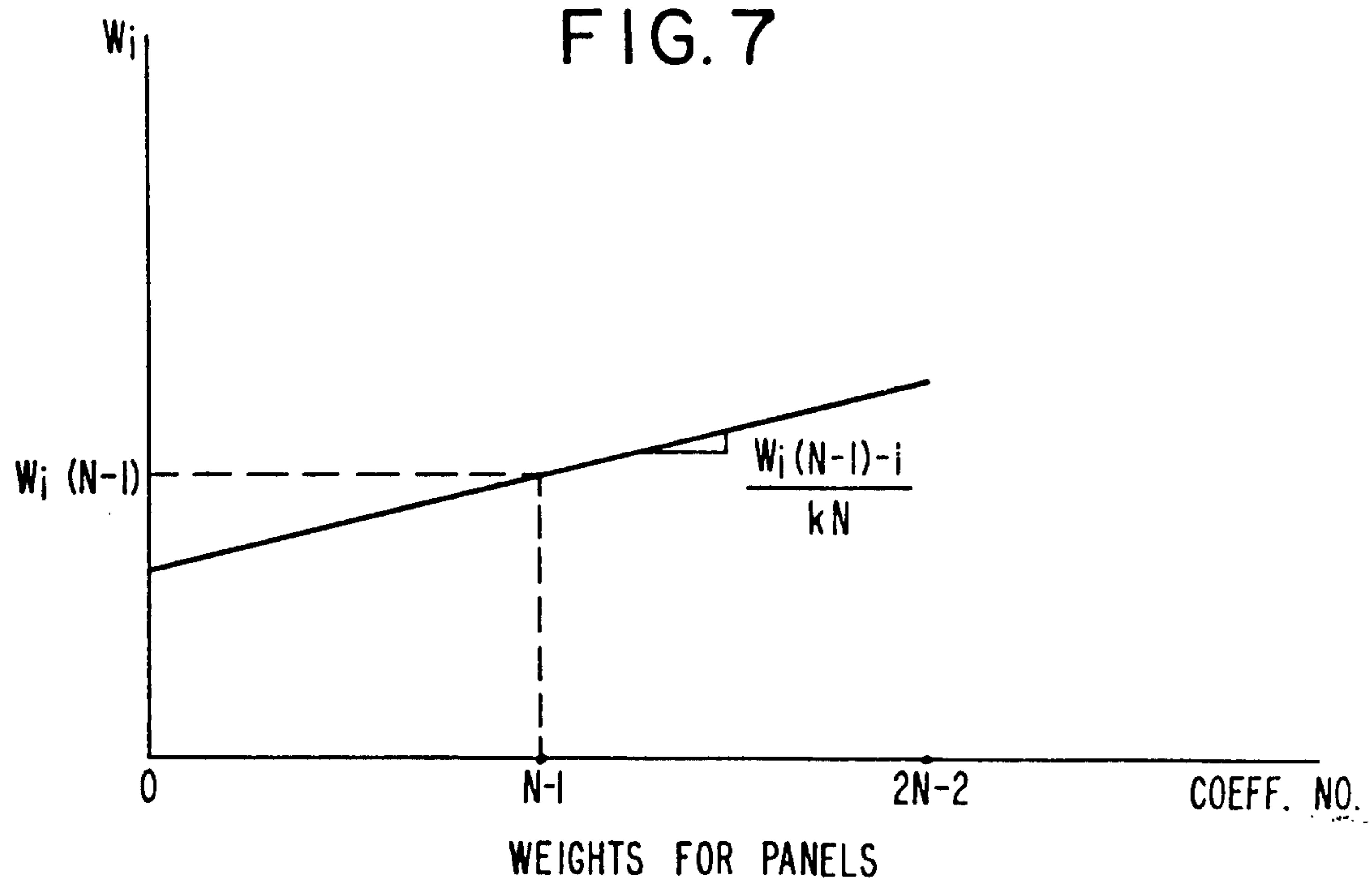


FIG. 7



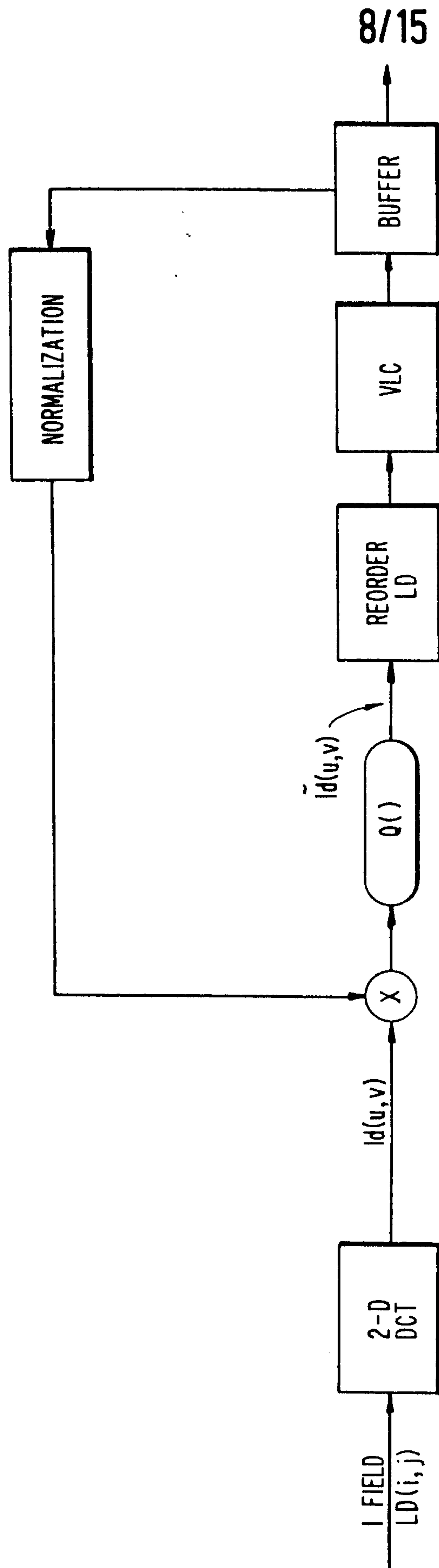
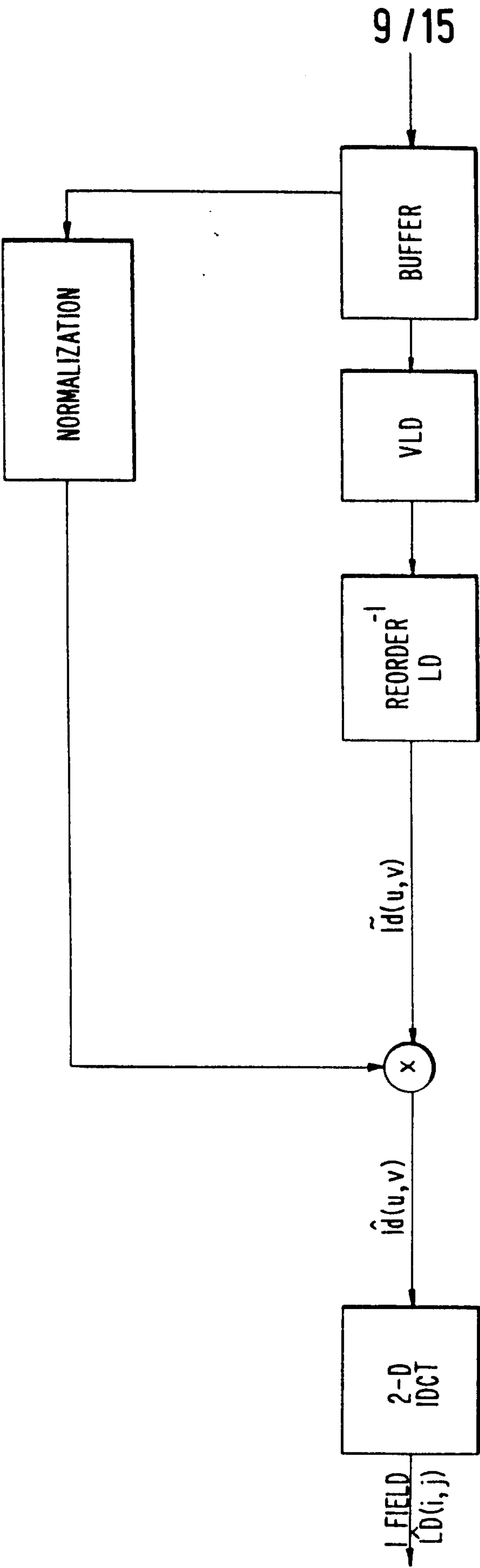


FIG. 8

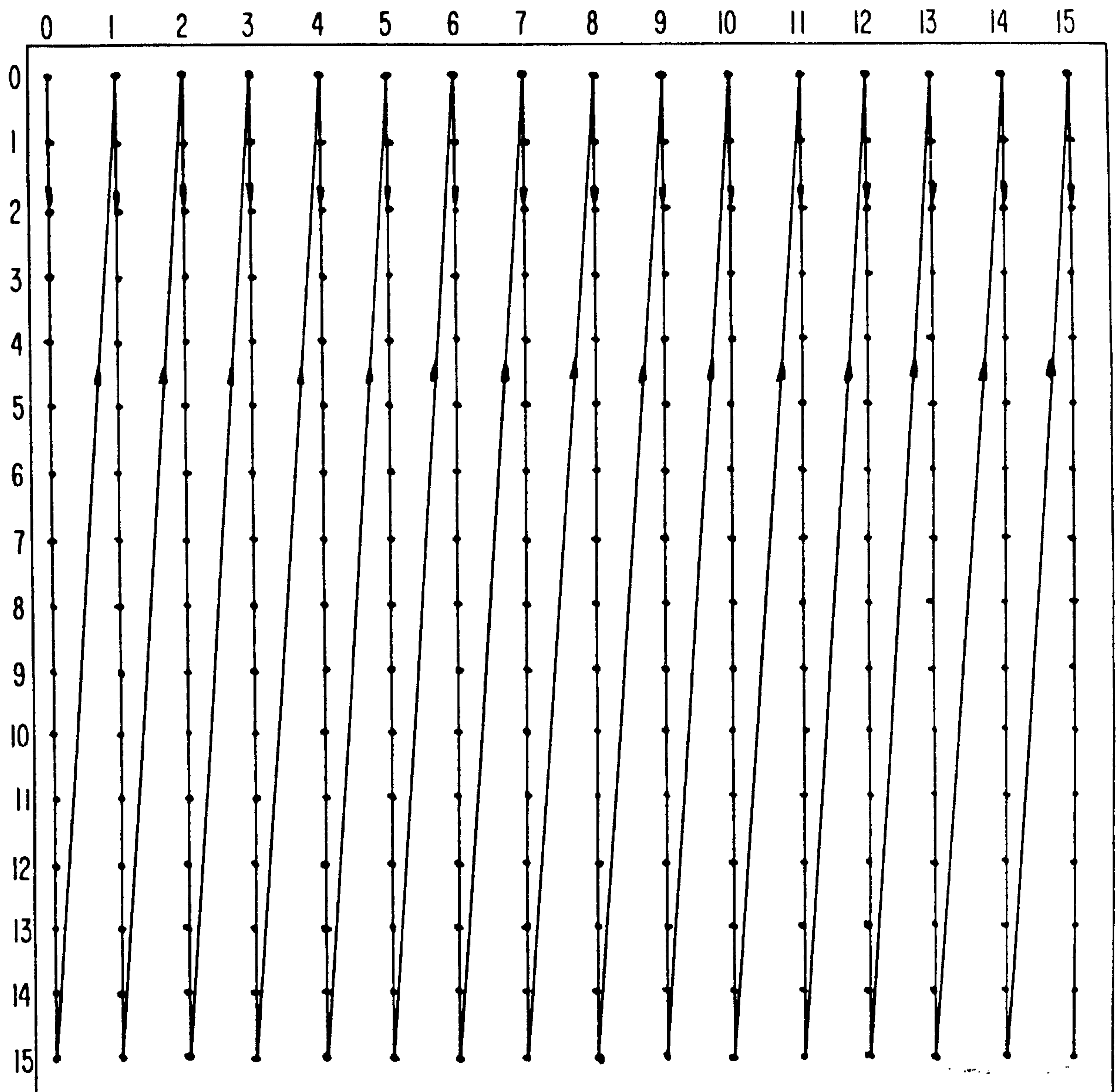


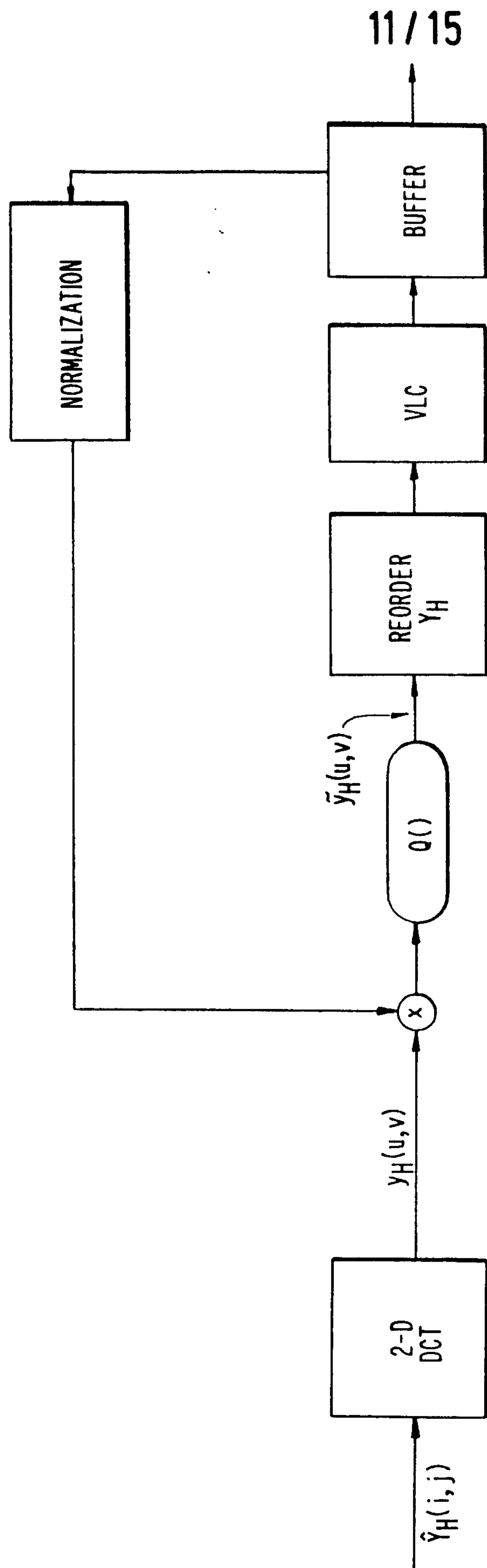
LD DECODER
FIG. 9

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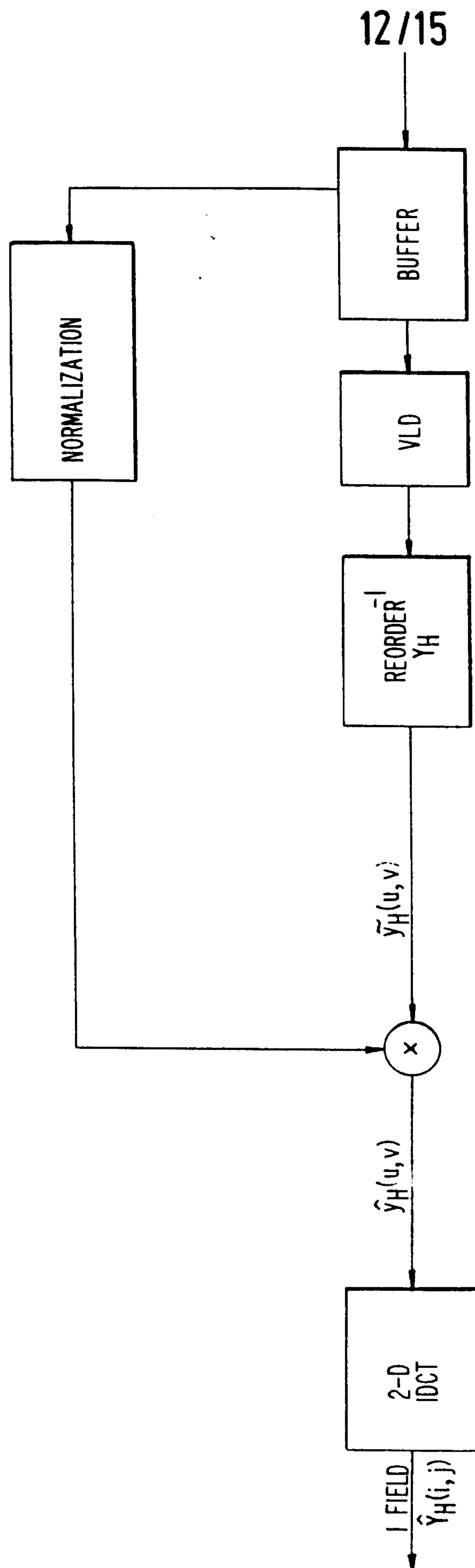
FIG.10

(REORDERING) SCANNING OF LD





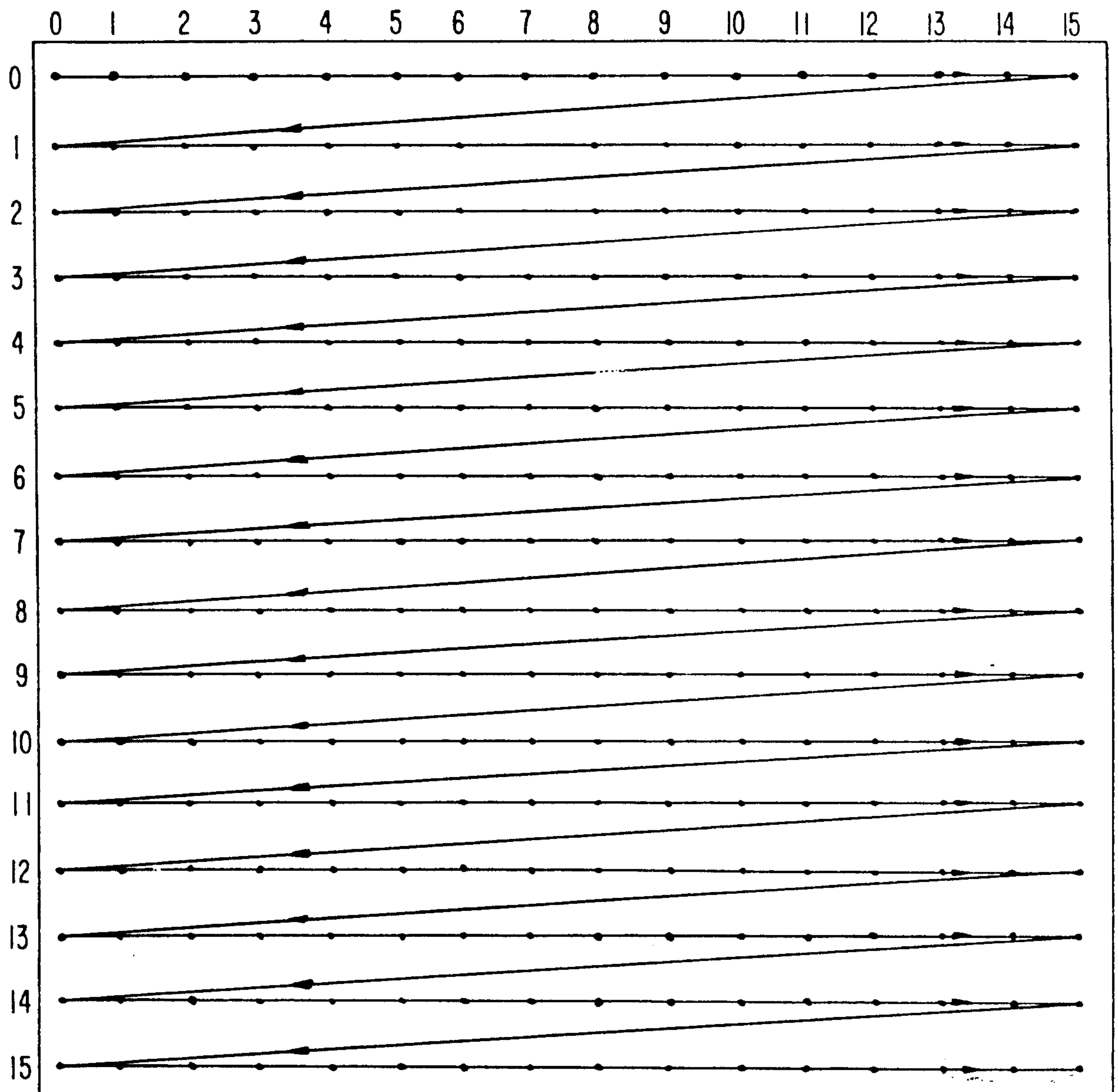
Y_H ENCODER
FIG. II



Y_H DECODER
FIG. 12

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FIG. 13

(REORDERING) SCANNING OF Y_h 

MEGASAMPLES/SEC COMPUTATIONS

Signal	Line time	Bandwidth	Sampling Rate	MS/sec
PL & PR Y _p	2x7 μsec	11.2 MHz	23.0 MHz	23 * 14 / 127 = 2.54 MS/sec
PL & PR Q _p	2x7 μsec	1.6 MHz	3.3 MHz	3.3 * 14 / 127 = 0.36 MS/sec
PL & PR I _p	2x7 μsec	3.2 MHz	6.5 MHz	6.5 * 14 / 127 = 0.72 MS/sec
LD	2x26 μsec	3.3 MHz	6.7 MHz	6.7 * 52 / 127 = 2.74 MS/sec
YH	26 μsec	5.6 MHz	12.0 MHz	12 * 26 / 127 = 2.46 MS/sec

FIG. 14(TABLE I)

BITRATE COMPUTATIONS

Signal	Coding Rate	MS/sec	Bit Rate
PL & PR	1.0 Bits/pel	2.54 MS/sec	$1.0 * 2.54 = 2.54 \text{ Mb/sec}$
PL & PR _Q	1.0 Bits/pel	0.36 MS/sec	$1.0 * 0.36 = 0.36 \text{ Mb/sec}$
PL & PR _I	1.0 Bits/pel	0.72 MS/sec	$1.0 * 0.72 = 0.72 \text{ Mb/sec}$
LD	0.2 Bits/pel	2.74 MS/sec	$0.2 * 2.74 = 0.55 \text{ Mb/sec}$
YH	0.3 Bits/pel	2.46 MS/sec	$0.3 * 2.46 = 0.74 \text{ Mb/sec}$
TOTAL			$4.91 \text{ Mb/sec} + 20\%$ $= 5.89 \text{ Mb/sec}$

FIG. 15 (TABLE 2)

