(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
16 December 2010 (16.12.2010)

PCT

(10) International Publication Number
WO 2010/142472 A1

(51) International Patent Classification:
H04J 3/16 (2006.01)

(21) International Application Number:
PCT/EP2010/052664

(22) International Filing Date:
3 March 2010 (03.03.2010)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
09290441.6 12 June 2009 (12.06.2009) EP

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(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PE, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:

— *with international search report (Art. 21(3))*

(54) Title: VARIABLE BITRATE EQUIPMENT

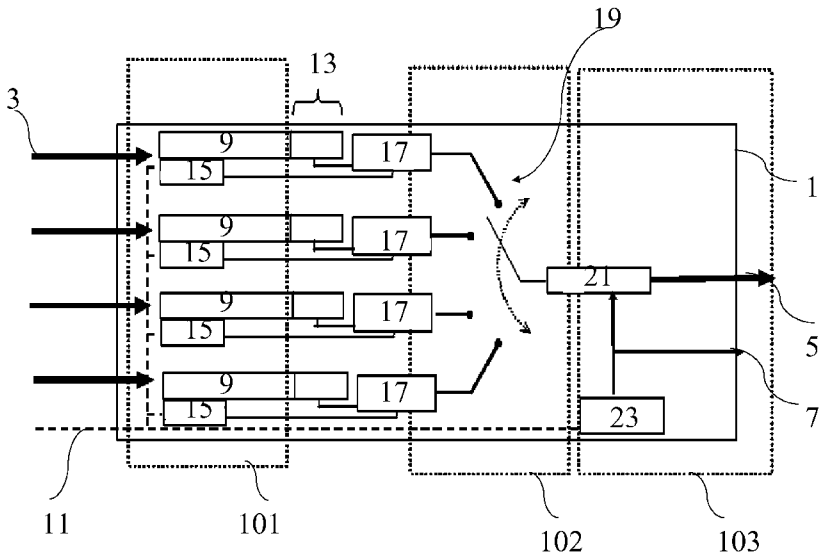

Fig.3

(57) Abstract: The present invention refers to a signal concentrator comprising: - a parallel to serial conversion device comprising a plurality of parallel inputs and a serial output, - a control unit comprising detection means adapted for detecting the activity of said plurality of parallel inputs of said parallel to serial conversion device, indication means adapted for indicating the active parallel inputs to the parallel to serial conversion device and controlling means adapted for setting an operating bitrate of the serial output in function of said activity of said plurality of parallel inputs.

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VARIABLE BITRATE EQUIPMENT

BACKGROUND OF THE INVENTION

The present invention relates to the field of communication networks and in particular to dynamic networks with bitrate agility.

Current communication networks comprises different types of transmission links having different bitrates. Thus, in order to reduce transmission costs while providing enhanced services, an idea is to aggregate a plurality of low bitrate data streams into a high bitrate data stream for high speed communications.

In the state of the art, concentrators allowing to aggregate several signals are known but the bitrate of the output transmission link is always the same whatever the number of received signals. Indeed, in case of inactive inputs, bit padding is achieved in order to compensate for the missing signal.

Thus, useless signals are transmitted which maximizes the required amount of energy and may lead to a reduced signal quality.

Besides, another solution for adapting the bitrate of the output port of a concentrator is to modify the Internet Protocol (IP) router so that it can deliver variable bitrates. However, such solution requires significant and expensive modifications and may lead to compatibility issues with existing routers.

SUMMARY OF THE INVENTION

It is therefore an object of the present invention to overcome the above cited drawbacks of the state of the art and provide a method allowing to aggregate a variable number of input low bitrate signals into an output signal with a variable high birate without requiring important modifications in the network design.

Thus, the present invention refers to a signal concentrator comprising:

- a parallel to serial conversion device comprising a plurality of parallel inputs and a

serial output,

- a control unit comprising detection means adapted for detecting the activity of said plurality of parallel inputs of said parallel to serial conversion device, indication means adapted for indicating the active parallel inputs to the parallel to serial conversion device and controlling means adapted for setting an operating bitrate of the serial output in function of said activity of said plurality of parallel inputs.

According to another embodiment, the controlling means comprise a clock signal generator for generating a clock signal in function of the activity of said plurality of parallel inputs, said clock signal allowing the setting of the operating bitrate.

According to a further embodiment, the plurality of parallel inputs of the parallel to serial conversion device are coupled to a plurality of fixed bitrate transmission lines and the activity detection of a parallel input comprises the detection of a received data signal at said parallel input.

According to an additional embodiment, the transmission lines have the same bitrate.

According to another embodiment, the operating bitrate of the serial output is determined by detecting the number of active parallel inputs.

According to a further embodiment, the signals received by the parallel inputs have different bitrates and the control unit comprises determination means adapted to determine the bitrate of the received signals.

According to an additional embodiment, the clock signal corresponds to the sum of the clock rates of the active parallel inputs.

According to another embodiment, the parallel to serial conversion device comprises a First In First Out (FIFO) queue, the active parallel inputs are sequentially scanned and a predetermined number of bits of the signals received on said active parallel inputs is transmitted to the FIFO queue the output of which corresponds to the output of the parallel to serial conversion device.

According to a further embodiment, the predetermined number of bits is equal to one.

According to an additional embodiment, the predetermined number of bits corresponds to a byte.

According to another embodiment, the predetermined number of bits corresponds to a frame.

The present invention also refers to an optical transmission system comprising:

- a signal concentrator,
- a variable bitrate optical transponder coupled to the serial output of the parallel to serial conversion device.

The present invention also refers to a signal distributor comprising:

- a serial to parallel conversion device comprising a serial input and a plurality of parallel outputs,
- a control unit comprising detection means adapted for detecting the number of independent data signal comprised in the signal received at the serial input and the organization of said signals and controlling means adapted for distributing the signal received at the serial input towards said plurality of parallel inputs.

The present invention also refers to an optical reception system comprising:

- a signal distributor,
- a variable bitrate optical transponder coupled to the serial input of the parallel to serial conversion device.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG.**1** is a diagram representing a concentrator;

FIG.**2** is a diagram representing a concentrator with an inactive input;

FIG.**3** is a diagram representing a possible embodiment of a concentrator according to the invention;

FIG.**4** is a diagram representing a possible embodiment of a receiver according to the invention;

DETAILED DESCRIPTION OF THE INVENTION

As used herein, the term "active input" refers to an input receiving data signals;

As used herein, the term "Gb/s" refers to the unit gigabit per second;

As used herein, the term "GHz" refers to the unit gigahertz;

An embodiment of the present invention refers to a concentrator or transmission system 1 as described in Fig.1 allowing to aggregate the signals received on a plurality of parallel input channels 3 onto a serial output channel 5 having a bitrate equal to the sum of the bitrates of the input channels 3. In Fig.1, the transmission system comprises four input channels 3 having each a 10Gb/s bitrate such that the output channel 5 has a 40Gb/s bitrate. Moreover, a clock signal 7 corresponding to the bitrate of the output channel (40 GHz in the present case) is provided.
Besides, if only three of the input channels 3 are active as represented in Fig.2, the bitrate of the output channel 5 becomes 30Gb/s corresponding to a clock signal 7 of 30GHz. In addition, an adaptation of the bitrate to the actual needs allows to save energy and to improve the signal quality when the bit rate is reduced.
Fig.3 represents a possible embodiment of a transmission system 1 according to the present invention. Said transmission system 1 comprises four input channels 3, also called tributaries, having each a bit rate of 10Gb/s.
It has to be noted that the value of 10Gb/s and the number of four input channels 3 are given as examples (because of the general use of 10 and 40 Gb/s transmission links in the current communication networks) but any value may be used in the scope of the present invention.
Said tributaries 3 are connected to parallel First In First Out (FIFO) inputs 9. An additional control data channel 11 provides the status (active or idle) of the input channels 3. Said control data channel 11 is connected to the activity detection means 15 of each FIFO inputs 9. In the first section 101 of the transmission system 1, the data of the active streams transmitted on the

input channels 3 are received in the corresponding queues of the FIFO inputs 9. Then, a predetermined number of bits 13, corresponding to the slot size, of each active FIFO queue is copied to the corresponding input 17 of a switch 19 at a clock rate of 10GHz.

Said predetermined number of bits 13 depends on the configuration chosen and allow to select the optimal trade-off between buffer size (queue length) and clock frequency. It can be, for example, a bit per bit, a byte per byte or a frame per frame selection.

In section 102, the switch 19 scans sequentially the selected predetermined number of bits of each active input 17 and write said bits in an output FIFO queue 21. The scanning rate is equal to (40/n)GHz where n is the predetermined number of bits 13.

Besides, the control data channel 11 is also connected to a frequency generator 23. Thus, at step 103, the frequency generator 23 generates a clock signal 7 corresponding to the actual total bitrate, for example, in the present example with four active input streams of 10Gb/s, the generated clock signal is 4*10GHz, that is to say 40GHz.

The data of the output FIFO queue 21 are therefore read out, multiplexed and transmitted to the output channel 5 at a 40Gb/s bitrate.

If one of the input channels 3 becomes inactive, as it is the case in Fig.2, the information of such inactivity (idle status) is brought by the control data channel to the transmission system 1. As a consequence, the switch 21 will only scan the three remaining active inputs 17 and the frequency generator 23 will generate a clock signal of 30GHz such that the data of the output FIFO queue 21 will be read out and transmitted to the output channel 5 at a 30Gb/s bitrate.

Besides, in the case of an optical network, a variable bitrate optical transponder may be coupled to the output channel 5 in order to convert the electronic signal into a corresponding optical signal having the same bitrate. Thus, the bitrate of the transmitted optical signal varies in function of the amount of data needed to be transmitted through the optical network.

After transmission through the communication network, the signal is received at the egress node. In the case of an optical transmission network, the signal is converted to an electronic signal thanks to an optical transponder located at the input of the egress node.

Fig.4 represents a possible embodiment of a distributor or reception system 2. The operation achieved by said reception system 2 corresponds to the converse operation with respect to the transmission system 1 presented in Fig.3.

The transmitted signal is received on a FIFO input 27 through an input channel 25. The clock signal 7 is also transmitted and received at the reception system 2. Said clock signal 7 is transmitted to the FIFO input 27 in order to allow said input to process the received data. In addition, a control data channel 37 comprising information required for demultiplexing the received signals is connected to the reception system 2. Said information comprises, for example, the total bitrate, the number of active input channels and the slot size (number of bits used for the multiplexing). Based on this information and using the clock signal 7, a switch controller 31 manages the position of the switch 29 in order to distribute the signal among the FIFO outputs 33. A clock signal (for example of 10GHz) generated by a clock generator 35 is distributed to the different FIFO outputs 33 in order to transmit the demultiplexed signals at the required bitrate (for example 10Gb/s) to the output channels 39.

Based on the previous example, if the received signal has a bitrate of 40Gb/s and is composed of four active input channels which have a slot size of one byte, then the switch controller 31 will send the first received byte to the first FIFO output 33, the second byte to the second FIFO output 33 and so on sequentially such that the four initial signals received at the four input channels 3 of the transmission system 1 will be recreated at the FIFO outputs 33. In the case described in Fig.2, the signal received on the input channel 25 has a bitrate of 30 Gb/s and is composed of three active input channels. Said information is transmitted through the control data channel 37 and in the same way, the three signals will be recreated at the three corresponding output channels 39.

According to another embodiment, the signals received on the different input channels 3 have different bitrates (for example 10Gb/s for the first two input channels and 5 Gb/s for the two following input channels) or different format corresponding to slightly different bitrates. In such situation, the position of the switch 19 will be monitored in order to take into account the different bitrates such that the time spent by the switch in a position corresponds to the time required in function of the bitrate of the corresponding input channel 3. Moreover, additional data (such as the individual bitrates) will be added in the control data signal 37 in order to allow the switch controller 31 and the switch 29 to correctly demultiplex the received signal. Besides, the clock generator 35 will have to generate individual clock signal for each signal in order to recreate the initial signal at the FIFO outputs 33. Thus with two input channels of 10Gb/s and

two channels of 5Gb/s, when all the input channels 3 are active, the operating bitrate of the output channel 5 is 30Gb/s and comprises four tributaries. The control data channel will then transmit said information to the reception system 2 in order to recreate the four signals with two signals having a 10Gb/s bitrate and two signals having a 5Gb/s bitrate at the output channels 39.

As a conclusion, the embodiments of the present invention allow to adapt the bitrate of transmitted signals in function of the number of active input channel signals. Such bitrate agility reduces the power consumption, allows adaptation of the network to the customers needs and eases the upgrade of the current networks to improved capacities. Moreover, the reduction of the bitrate of the transmitted signal reduces signal impairments and therefore leads to a better signal quality.

CLAIMS

1. Signal concentrator (1) comprising:
   - a parallel to serial conversion device comprising a plurality of parallel inputs (3) and a serial output (5),
   - a control unit comprising detection means adapted for detecting the activity of said plurality of parallel inputs of said parallel to serial conversion device, indication means adapted for indicating the active parallel inputs to the parallel to serial conversion device and controlling means adapted for setting an operating bitrate of the serial output in function of said activity of said plurality of parallel inputs, said controlling means comprising a clock signal generator (23) for generating a clock signal in function of the activity of said plurality of parallel inputs, said clock signal allowing the setting of the operating bitrate.

2. Signal concentrator (1) in accordance with claim 1 wherein the plurality of parallel inputs (3) of the parallel to serial conversion device are coupled to a plurality of fixed bitrate transmission lines and wherein the activity detection of a parallel input comprises the detection of a received data signal at said parallel input.

3. Signal concentrator (1) in accordance with claim 2 wherein the transmission lines have the same bitrate.

4. Signal concentrator (1) in accordance with claim 3 wherein the operating bitrate of the serial output (5) is determined by detecting the number of active parallel inputs (3).

5. Signal concentrator (1) in accordance with claim 1 wherein the signals received by the parallel inputs (3) have different bitrates and wherein the control unit comprises

determination means adapted to determine the bitrate of the received signals.

6. Signal concentrator (1) in accordance with claims 1 and 5 wherein the clock signal corresponds to the sum of the clock rates of the active parallel inputs.

7. Signal concentrator (1) in accordance with one of the previous claims wherein the parallel to serial conversion device comprises a First In First Out (FIFO) queue and wherein the active parallel inputs are sequentially scanned and a predetermined number of bits of the signals received on said active parallel inputs is transmitted to the FIFO queue the output of which corresponds to the output of the parallel to serial conversion device .

8. Signal concentrator (1) in accordance with claim 7 wherein the predetermined number of bits is equal to one.

9. Signal concentrator (1) in accordance with claim 7 wherein the predetermined number of bits corresponds to a byte.

10. Signal concentrator (1) in accordance with claim 7 wherein the predetermined number of bits corresponds to a frame.

11. Optical transmission system comprising:
- a signal concentrator (1) according to one of the previous claims,
- a variable bitrate optical transponder coupled to the serial output of the parallel to serial conversion device.

12. Signal distributor (2) comprising
- a serial to parallel conversion device comprising a serial input and a plurality of parallel outputs,
- a control unit comprising detection means adapted for detecting the number of

independent data signal comprised in the signal received at the serial input and the organization of said signals and controlling means adapted for distributing the signal received at the serial input towards said plurality of parallel inputs.

13. Optical reception system comprising:

- a signal distributor according to claim 12,
- a variable bitrate optical transponder coupled to the serial input of the parallel to serial conversion device.

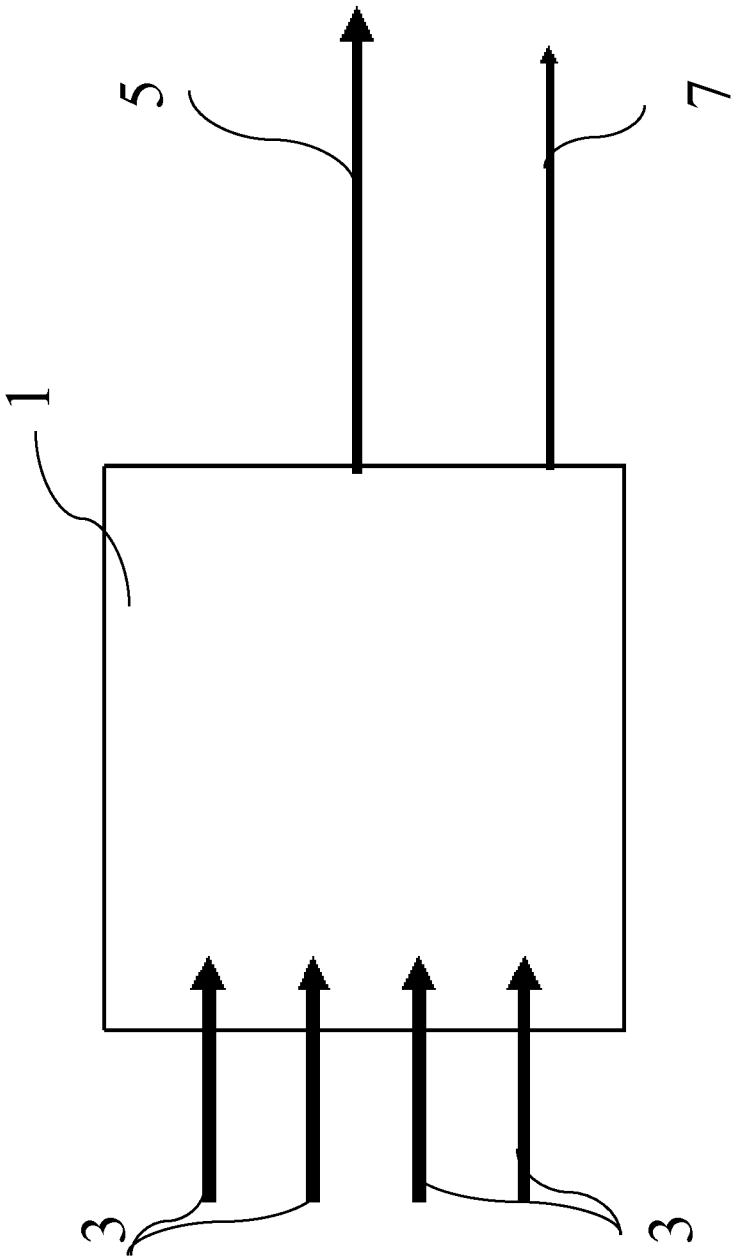

Fig.1

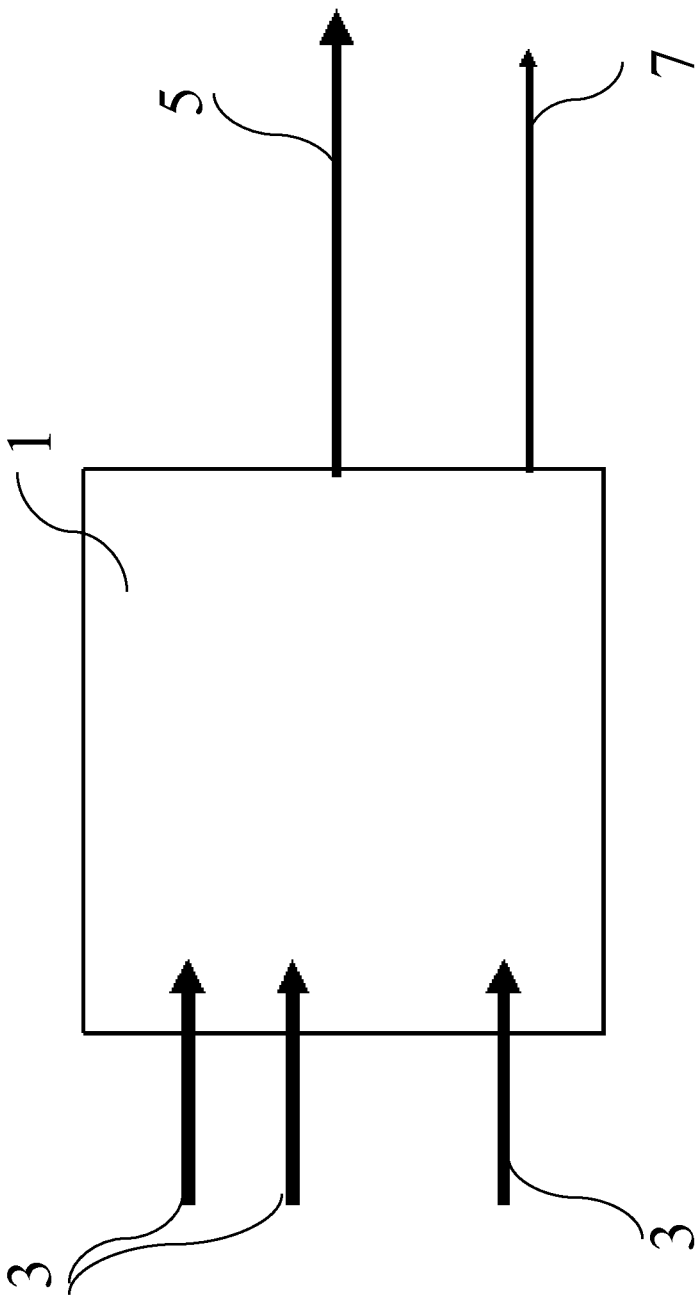

Fig.2

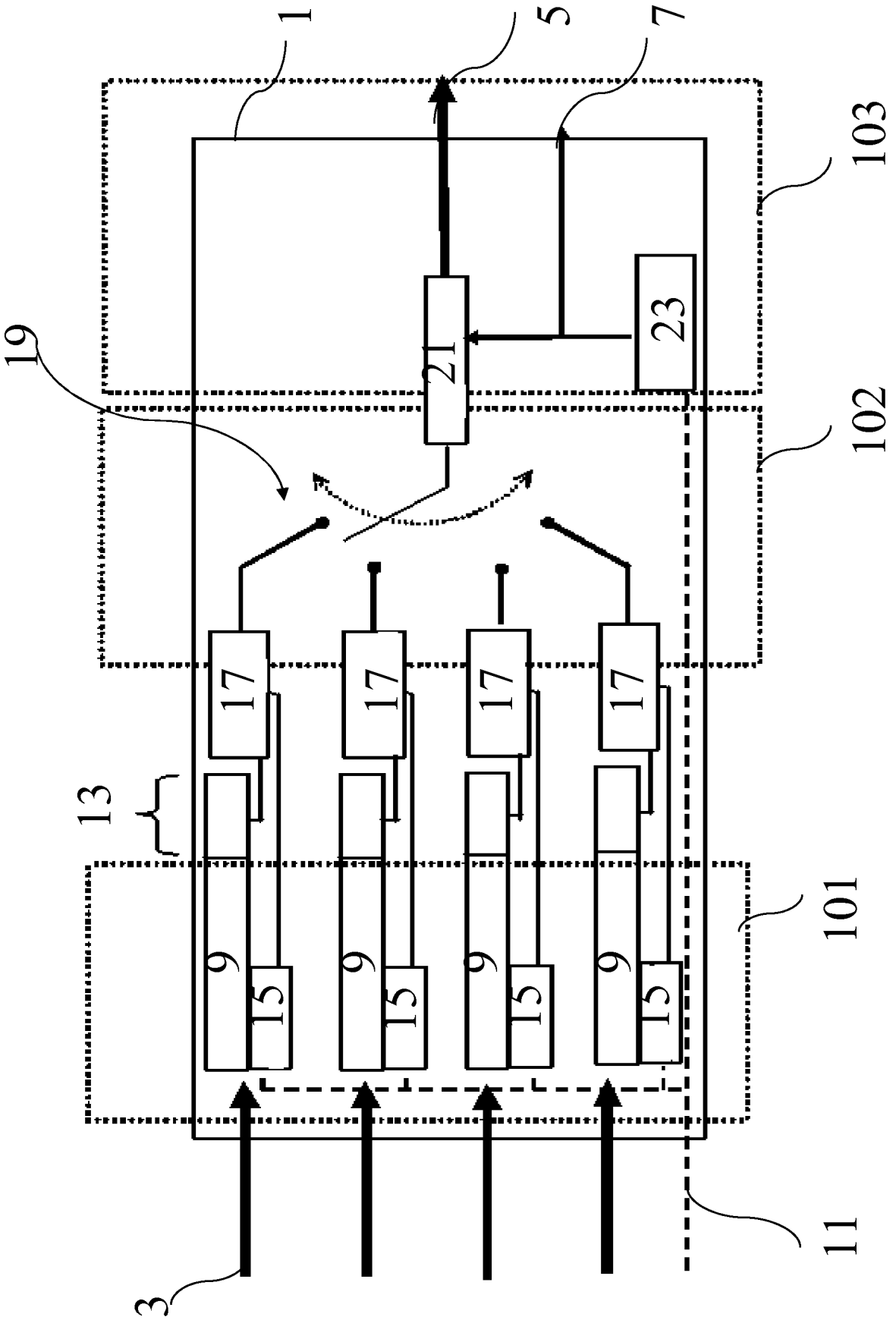

Fig.3

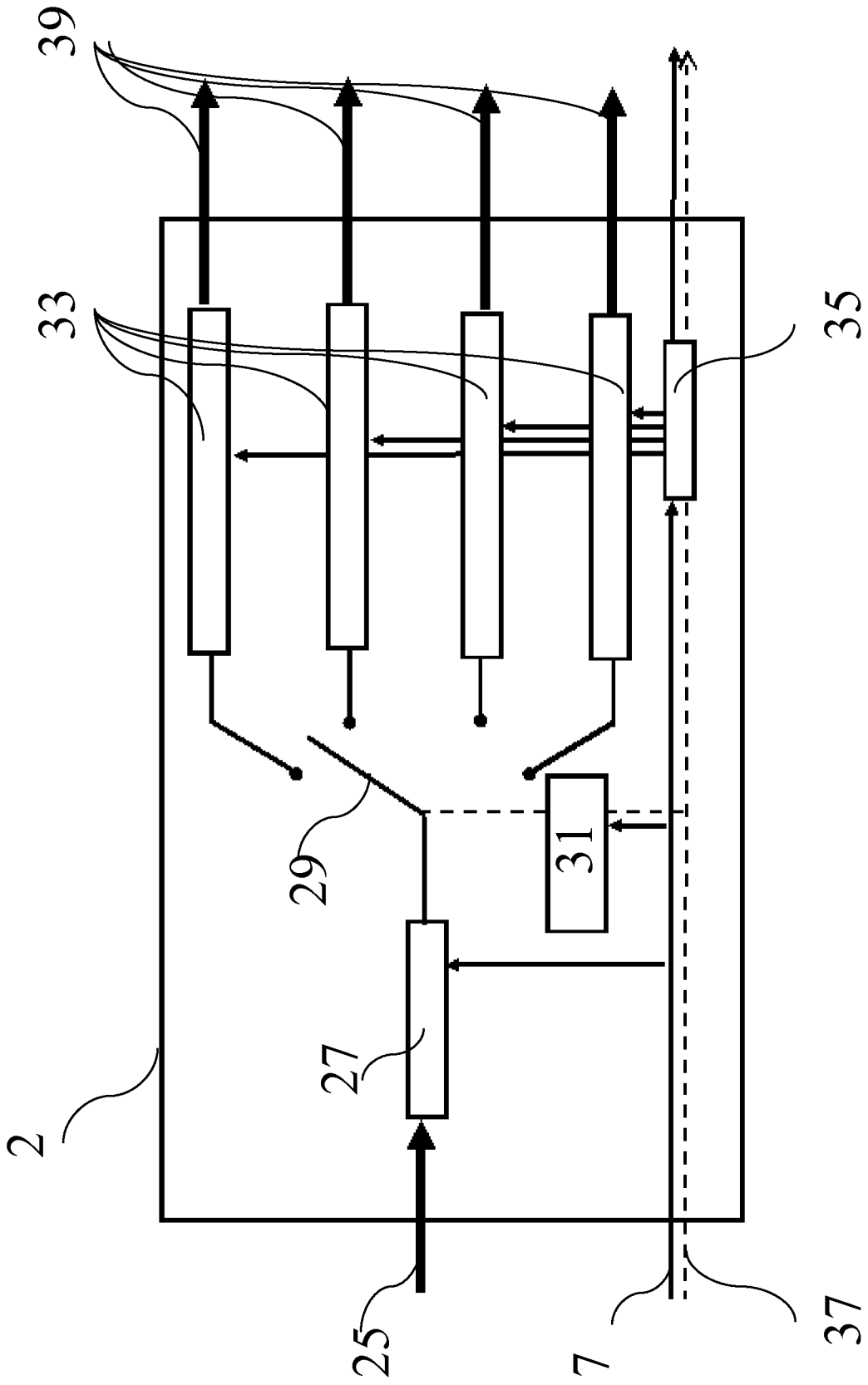

Fig.4

INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2010/052664

A. CLASSIFICATION OF SUBJECT MATTER
INV. H04J3/16

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H04J

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	WO 00/27060 A1 (KONINKL PHILIPS ELECTRONICS NV [NL]) 11 May 2000 (2000-05-11)	12-13
A	page 3, line 20 - page 4, line 17 page 6, line 11 - line 12 figure 2	1-11
X	DE 195 36 025 C1 (SIEMENS AG [DE]) 20 February 1997 (1997-02-20)	12-13
A	abstract column 1, line 3 - line 6 column 2, line 7 - line 19 column 3, line 16 - line 36 column 4, line 20 - line 25 column 6, line 42 - line 47 figures 1-3	1-11

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[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
24 March 2010	01/04/2010

Name and mailing address of the ISA/	Authorized officer
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Form PCT/ISA/210 (second sheet) (April 2005)

INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2010/052664

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	WO 00/44175 A1 (SCIENTIFIC ATLANTA [US]) 27 July 2000 (2000-07-27)	12-13
A	page 4, line 23 - line 31 page 5, line 6 - line 14 page 7, line 21 - line 33 figure 3	1-11

A	US 4 429 383 A (FINCK HERBERT [DE] ET AL) 31 January 1984 (1984-01-31) column 1, line 25 - line 30 column 3, line 51 - line 55 column 4, line 9 - line 13 figure 1	1-13

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/EP2010/052664

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