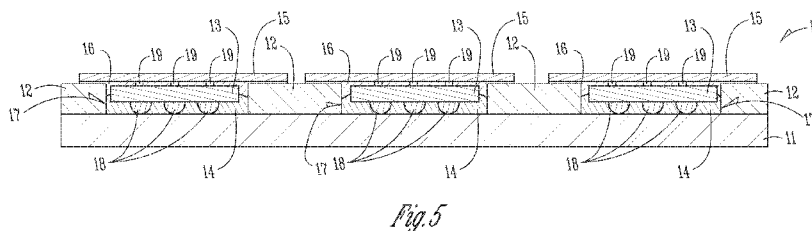




- (51) **International Patent Classification:**
H01L 25/065 (2006.01) *H01L 23/00* (2006.01)
H01L 23/13 (2006.01)
- (21) **International Application Number:**
PCT/US2016/062825
- (22) **International Filing Date:**
18 November 2016 (18.11.2016)
- (25) **Filing Language:** English
- (26) **Publication Language:** English
- (30) **Priority Data:**
14/974,811 18 December 2015 (18.12.2015) US
- (63) **Related by continuation (CON) or continuation-in-part (CIP) to earlier application:**
US 14/974,811 (CON)
Filed on 18 December 2015 (18.12.2015)
- (71) **Applicant: INTEL CORPORATION** [US/US]; 2200 Mission College Blvd., Santa Clara, California 95054 (US).
- (72) **Inventors: KARHADE, Omkar**; 2325 W Sunrise Pl, Chandler, Arizona 85248 (US). **DESHPANDE, Nitin**; 4909 W. Joshua Blvd. #2104, Chandler, Arizona 85226 (US). **ZIADEH, Bassam M.**; 3465 E Milky Way, Gilbert, Arizona 85295 (US). **TOMITA, Yoshihiro**; 1-13-4-901 Azuma, Tsukuba-Shi, Ibaraki, 08 / 305-0031 (JP).
- (74) **Agents: PERDOK, Monique M.** et al.; Schwegman Lundberg & Woessner, P.A., P.O. Box 2938, Minneapolis, Minnesota 55402 (US).
- (81) **Designated States** (*unless otherwise indicated, for every kind of national protection available*): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DJ, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JP, KE, KG, KN, KP, KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.
- (84) **Designated States** (*unless otherwise indicated, for every kind of regional protection available*): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).
- Published:**
— with international search report (Art. 21(3))

(54) **Title:** INTEGRATED CIRCUIT ASSEMBLY THAT INCLUDES STACKED DICE



(57) **Abstract:** An integrated circuit assembly that includes a substrate; a member formed on the substrate; a first die mounted to the substrate within an opening in the member such that there is space between the first die and the member and the member surrounds the first die, and wherein the first die does not extend above an upper surface of the member; an underfill between the first die and the substrate, wherein the underfill at least partially fills the space between the die and member; and a second die mounted to the first die and the member, wherein the second die is mounted to the member on all sides of the opening.



INTEGRATED CIRCUIT ASSEMBLY THAT INCLUDES STACKED DICE

5 **CROSS-REFERENCE TO RELATED APPLICATION**

[0001] This application is a continuation of U.S. Patent Application Serial No. 14/974,811, filed December 18, 2015, which is incorporated by reference herein in its entirety.

10 **Technical Field**

[0002] Embodiments described herein generally relate to an integrated circuit assembly, and more particularly to an integrated circuit assembly that includes stacked dice.

15 **Background**

[0003] Mobile products (e.g., mobile phones, smart phones, tablet computers, etc.) are typically very restricted in available space because there are often severe limitations for chip and package area and height (among other physical and electrical parameters). Therefore, it is extremely important to
20 reduce the size of electronic components (e.g., dies) on a substrate.

[0004] However, when electronic components/packages are made relatively thin in order to accommodate this need for reduced sized electronic components, there can be difficulties that are associated with fabricating such components. As an example, stacking thin components/packages have
25 historically been a huge challenge for the semiconductor industry.

[0005] Some conventional integrated circuit (IC) assemblies include three dimensional (3D) package architectures where one or more dies (e.g., memory dies) are stacked on another die (e.g., to form a system-on-chip die). The stacked dies may overhang the underlying die in some configurations. This
30 overhanging configuration often results in cracking (or other types of defects) in the stacked dies.

[0006] Therefore, the degree of overhang in conventional stacked electronic systems may be restricted in order to mitigate any type of defect that

may be caused by the overhanging configuration. In addition, since stacked electronic packages often include electronic packages of different sizes, it may be desirable to package architectures that compensate for such differences in electronic package size, especially for smaller devices (e.g., mobile devices or wearables).

Brief Description of the Drawings

- [0007] FIG. 1 illustrates an example substrate.
- 10 [0008] FIG. 2 illustrates the example substrate of FIG. 1 with a member formed on the substrate.
- [0009] FIG. 3 illustrates the example substrate and member of FIG. 2 with a die attached to the substrate.
- [0010] FIG. 4 illustrates the example substrate, member and die of FIG. 3 with an underfill added between the die and the substrate and the die and the member.
- 15 [0011] FIG. 5 illustrates the example substrate, member and die of FIG. 4 with another die mounted to the member and the die.
- [0012] FIG. 6 is a top view of an example electronic assembly.
- 20 [0013] FIG. 7 is a side view of the example electronic assembly shown in FIG. 6.
- [0014] FIG. 8 is block diagram of an electronic apparatus that includes the integrated circuit assemblies described herein.

Description of Embodiments

- 25 [0015] The following description and the drawings sufficiently illustrate specific embodiments to enable those skilled in the art to practice them. Other embodiments may incorporate structural, logical, electrical, process, and other changes. Portions and features of some embodiments may be included in, or substituted for, those of other embodiments. Embodiments set forth in the claims encompass all available equivalents of those claims.
- 30 [0016] Orientation terminology, such as “horizontal,” as used in this application is defined with respect to a plane parallel to the conventional plane

or surface of a wafer or substrate, regardless of the orientation of the wafer or substrate. The term “vertical” refers to a direction perpendicular to the horizontal as defined above. Prepositions, such as “on,” “side” (as in “sidewall”), “higher,” “lower,” “over,” and “under” are defined with respect to the conventional plane or surface being on the top surface of the wafer or substrate, regardless of the orientation of the wafer or substrate.

[0017] The integrated circuit assemblies described herein may provide support to the top dice and a stack of dices where the top dice overhangs the underlying dice or stack of dices in some configuration. The support provided by the integrated circuit assemblies may serve to prevent unsupported top dice (e.g., a memory dice) from bending or breaking during fabrication or operation of the integrated circuit assembly.

[0018] FIGS. 1-5 illustrate an example process for forming an integrated circuit assembly 10. FIG. 1 illustrates an example substrate 11. FIG. 2 illustrates the example substrate 11 of FIG. 1 with a member 12 formed on the substrate 11. FIG. 3 illustrates the example substrate 11 and member 12 of FIG. 2 with a first die 13 (or multiple first dice 13) attached to the substrate 11. FIG. 4 illustrates the example substrate 11, member 12 and first dice 13 of FIG. 3 with an underfill 14 added between the dice 13 and the substrate 11 as well as between the dice 13 and the member 12. FIG. 5 illustrates the example substrate 11, member 12 and first dice 13 of FIG. 4 with second dice 15 mounted to the member 12 and the respective dice 13.

[0019] As shown in FIG. 5, the integrated circuit assembly 10 includes a substrate 11 and a member 12 formed on the substrate 11. A first die 13 is mounted to the substrate 11 within an opening 17 in the member 12 such that there is space S between the first die 13 and the member 12. As an example, the first dice 13 may be an active component (e.g., a logic die). In the example integrated circuit assembly 10 shown in FIG. 5, there is a plurality of first dice 13 mounted to the substrate 11 within the respective openings 17 in the member 12.

[0020] An underfill 14 is between each of the first dice 13 and the substrate 11. The underfill 14 at least partially fills the spaces S between the respective first dice 13 and the member 12. In some forms, the underfill 14 will

entirely fill the space S between the first dice 13 and the member 12. In addition, it may be desirable for the underfill 14 to not extend above the first dice 13.

5 [0021] As shown in FIG. 5, a second die 15 is mounted to the first die 13 and the member 12. In the example integrated circuit assembly 10 shown in FIG. 5, a plurality second dice 15 are mounted to a respective one of the first dice 13 and the member 12.

10 [0022] As shown in FIG. 5 the second dice 15 may be mounted to the respective first dice 13 and the member 12 using an epoxy 16. The epoxy 16 may serve to form an electrical connection. It should be noted that the second dice 15 may be mounted to the first dice 13 in any manner that is known now, or discovered in the future. The manner in which the second dice 15 are mounted to the first dice 13 and the member 12 will depend in part on the materials that are used to form the second dice 15, the first dice 13 and the member 12 as well as the manufacturing techniques that are used to fabricate the integrated assembly 10 (among other factors).

20 [0023] In some forms, the first dice 13 are thermal bonded to the substrate 11. It should be noted that other forms of attachment are contemplated for mounting the first dice 13 to the substrate 11. The manner in which the first dice 13 are bonded to the substrate 11 will depend in part on the type of substrate 11 that is included in the integrated circuit assembly 10 as well as the type of first dice 13 that are included in the integrated circuit assembly 10. In the example integrated circuit assembly 10 shown in FIG. 5, the first dice 13 includes solder balls 18 that are mounted on the substrate 11.

25 [0024] As an example, the second dice 15 may be flip-chip mounted to the first dice 13. As shown in FIG. 5, interconnects 19 may electrically connect the second dice 15 to the respective first dice 13. It should be noted that interconnects 19 may be any form (or combination of) solder balls, solder pads, vias, and/or pillars (among other forms of electrical connection).

30 [0025] In some forms, the second dice 15 are mounted to the member 12 on all sides of the respective openings 17. It should be noted that the second dice 15 may be mounted to the member 12 on one, some or all sides of the openings 17. The areas where the second dice 15 are mounted to the member 12

will depend in part on the size of the second dice 15 and the size of the respective openings 17 (among other factors).

[0026] In some forms, the second dice 15 may be a passive electronic component that is not electrically connected directly to the first dice 13. In addition, the second dice 15 may be electrically connected to the substrate 11. As examples, the second dice 15 may be wire bonded to the substrate 11, or the member 12 may include interconnects (not shown) that electrically connect the second dice 15 to the substrate 11.

[0027] As examples, one, some or all of the first dice 13 may form a system-on-chip die. It should be noted that the first dice 13 may be any type of die that is known now, or discovered in the future. The type of first dice 13 that are included in the integrated circuit assembly 10 will depend in part on the application where the integrated circuit assembly 10 is to be used (among other factors).

[0028] As examples, one, some, or all of the second dice 15 may be memory, logic and/or modem. It should be noted that the second dice 15 may be any type of dice that is known now, or discovered in the future. The type of second dice 15 that included in the integrated circuit assembly 10 will depend in part on the application where the integrated circuit assembly 10 is to be used (among other factors).

[0029] As an example, the second dice 15 may be less than 250 micrometers thick. The thickness of the second dice 15 will depend on the type of second dice 15 that are included in the integrated circuit assembly 10.

[0030] The degree to which each of the second dice 15 overhangs the member 12 will depend in part on the size of the second dice 15 and the respective first dice 13 as well as the size of the openings 17 (among other factors). As an example, the second dice 15 may overhang the member 12 by anywhere between 500 and 3000 micrometers.

[0031] It should be noted that even though FIG. 5 illustrates the integrated assemblies 10 in strip form, the integrated circuit assemblies 10 may be singulated to form individual electronic packages. In addition, the integrated circuit assemblies 10 may be fabricated at a wafer or panel level.

[0032] FIG. 6 is a top view of an example electronic assembly 60. FIG. 7 is a side view of the example electronic assembly 60 shown in FIG. 6.

[0033] The electronic assembly 60 includes a substrate 61 with a die side 62. The electronic assembly 60 further includes a first die 63 including four edges 64A, 64, 64C, 64D, a first-die active surface 65, and a first die backside surface 66. The first-die active surface 65 is mounted to the substrate die side 62.

[0034] An underfill 67 (see FIG. 7) is between the first die 63 and the substrate 61. A second die 68 includes a second-die active surface 69 and a second-die backside surface 70. The second-die active surface 69 is mounted to the first die backside surface 66. The second die 68 overhangs the first die 63 on all four edges 64A, 64, 64C, 64D.

[0035] The electronic assembly 60 may further include a mold 71 that forms an opening 72 onto the substrate 61 in which the first die 63 is mounted. In some forms, the second die 68 may also be mounted to the mold 71 at a surface 77 of the substrate 61 that is substantially coplanar with the first die backside surface 66.

[0036] The first die 63 may be a system-on-chip die and the second die 68 may be a memory die. Other types of dice are contemplated for inclusion into the electronic assembly 60.

[0037] In some forms, the first die 62 may include through silicon vias 73 that electrically connect the second die 68 to the substrate 61 (see FIG. 7). In addition, the mold 71 may include through mold vias 74 that electrically connect the second die 68 to the substrate 61.

[0038] In the example form of the electronic assembly 60 that is illustrated in FIGS. 6 and 7, the second-die backside surface 70 is wire bonded to the surface 72 of the mold 71 (e.g., using leads 75). It should be noted that the second-die backside surface 70 may also (or alternatively) be wire bonded to the substrate die side 62 (e.g., using leads 76).

[0039] FIG. 8 is a block diagram of an electronic apparatus 800 incorporating at least one method electronic package described herein. Electronic apparatus 800 is merely one example of an electronic apparatus in which forms of the electronic packages 10, 20, 30 described herein may be used.

Examples of an electronic apparatus 800 include, but are not limited to, personal computers, tablet computers, mobile telephones, game devices, MP3 or other digital music players, etc.

5 [0040] In this example, electronic apparatus 800 comprises a data processing system that includes a system bus 802 to couple the various components of the electronic apparatus 800. System bus 802 provides communications links among the various components of the electronic apparatus 800 and may be implemented as a single bus, as a combination of busses, or in any other suitable manner.

10 [0041] An electronic assembly 810 as describe herein may be coupled to system bus 802. The electronic assembly 810 may include any circuit or combination of circuits. In one embodiment, the electronic assembly 810 includes a processor 812 which can be of any type. As used herein, "processor" means any type of computational circuit, such as but not limited to a
15 microprocessor, a microcontroller, a complex instruction set computing (CISC) microprocessor, a reduced instruction set computing (RISC) microprocessor, a very long instruction word (VLIW) microprocessor, a graphics processor, a digital signal processor (DSP), multiple core processor, or any other type of processor or processing circuit.

20 [0042] Other types of circuits that may be included in electronic assembly 810 are a custom circuit, an application-specific integrated circuit (ASIC), or the like, such as, for example, one or more circuits (such as a communications circuit 814) for use in wireless devices like mobile telephones, tablet computers, laptop computers, two-way radios, and similar electronic
25 systems. The IC can perform any other type of function.

[0043] The electronic apparatus 800 may also include an external memory 820, which in turn may include one or more memory elements suitable to the particular application, such as a main memory 822 in the form of random access memory (RAM), one or more hard drives 824, and/or one or more drives
30 that handle removable media 826 such as compact disks (CD), flash memory cards, digital video disk (DVD), and the like.

[0044] The electronic apparatus 800 may also include a display device 816, one or more speakers 818, and a keyboard and/or controller 830, which can

include a mouse, trackball, touch screen, voice-recognition device, or any other device that permits a system user to input information into and receive information from the electronic apparatus 800.

5 [0045] To better illustrate the integrated circuit assemblies disclosed herein, a non-limiting list of examples is provided here:

[0046] Example 1 includes an integrated circuit assembly that includes a substrate; a member formed on the substrate; a first die mounted to the substrate within openings in the member such that there is space between the first die and the member; an underfill between the first the die and the substrate, wherein the
10 underfill at least partially fills the space between the die and member; and a second die mounted to the first die and the member.

[0047] Example 2 includes the integrated circuit assembly of example 1, wherein an epoxy partially fills the space between the first die and the member, and the epoxy attaches the second die to the first die.

15 [0048] Example 3 includes the integrated circuit assembly of any one of examples 1-2, wherein the second die is mounted to the member on all sides of the opening.

[0049] Example 4 includes the integrated circuit assembly of any one of examples 1-3, wherein the first die is below an upper surface of the member.

20 [0050] Example 5 includes the integrated circuit assembly of any one of examples 1-4, wherein an upper surface of the first die is coplanar with an upper surface of the member.

[0051] Example 6 includes the integrated circuit assembly of examples 1-5, wherein the first die is a system-on-chip die, and wherein the second die is a
25 memory die.

[0052] Example 7 includes the integrated circuit assembly of any one of examples 1-6, wherein the underfill fills the space between the die and member.

[0053] Example 8 includes the integrated circuit assembly of any one of examples 1-7, wherein the second die is less than 250 micrometers thick,
30 wherein the second die overhangs the member by between 500 and 3000 micrometers.

[0054] Example 9 includes the integrated circuit assembly of any one of examples 1-8, wherein the first die includes through silicon vias that electrically connect the second die to the substrate.

5 [0055] Example 10 includes the integrated circuit assembly of any one of examples 1-9, wherein the member includes through member vias that electrically connect the second die to the substrate.

[0056] Example 11 includes the electronic assembly of any one of examples 1-10, wherein an upper surface of the second die is wire bonded to an upper surface of the member.

10 [0057] Example 12 includes the electronic assembly of any one of examples 10-11, wherein an upper surface of the second die is wire bonded to the substrate.

[0058] Example 13 includes an integrated circuit assembly that includes a substrate; a member formed on the substrate; a first die mounted to the
15 substrate within openings in the member such that there is space between the first die and the member and the member surrounds the first die, and wherein the first die does not extend above an upper surface of the member; an underfill between the first the die and the substrate, wherein the underfill at least partially fills the space between the die and member; and a second die mounted to the
20 first die and the member, wherein the second die is mounted to the member on all sides of the opening.

[0059] Example 14 includes the integrated circuit assembly of example 13, wherein the second die is mounted to the first die and the member using an epoxy, and wherein the epoxy at least partially fills the space between the die
25 and member.

[0060] Example 15 includes the integrated circuit assembly of any one of examples 13-14, wherein the first die is thermal compression bonded to the substrate, and wherein the second die is flip-chip mounted to the first die.

[0061] Example 16 includes the integrated circuit assembly of any one of
30 examples 13-15, wherein the first die is a system-on-chip die, and wherein the second die is a memory die.

[0062] Example 17 includes the integrated circuit assembly of any one of examples 13-16, wherein the second die is less than 250 micrometers thick, and

wherein the second die overhangs the member by between 500 and 3000 micrometers.

[0063] Example 18 includes an integrated circuit assembly. The integrated circuit assembly includes a substrate with a die side; a first die including four edges, a first-die active surface, and a first-die backside surface, wherein the first-die active surface is mounted to the substrate die side; an underfill between the first die and the substrate; a second die including a second-die active surface and a second-die backside surface, wherein the second-die active surface is mounted to the first die backside surface, and wherein the second die overhangs the first die on all four edges.

[0064] Example 19 includes the integrated circuit assembly of example 18, and further including a mold that forms an opening onto the substrate in which the first die is mounted.

[0065] Example 20 includes the integrated circuit assembly of examples 18-19, wherein the second die is also mounted to an upper surface of the mold substrate that is substantially coplanar with the first-die backside surface.

[0066] Example 21 includes the integrated circuit assembly of examples 18-20, and further including a mold that forms an opening onto the substrate in which the first die is mounted, and wherein the second die is also mounted to an upper surface of the mold substrate that is substantially coplanar with the first-die backside surface

[0067] Example 22 includes the integrated circuit assembly of examples 18-21, and further including a mold that forms an opening onto the substrate in which the first die is mounted, wherein the second die is also mounted to an upper surface of the mold substrate that is substantially coplanar with the first-die backside surface, and wherein the first die is a system-on-chip die and the second die is a memory die.

[0068] This overview is intended to provide non-limiting examples of the present subject matter. It is not intended to provide an exclusive or exhaustive explanation. The detailed description is included to provide further information about the integrated circuit assemblies described herein.

[0069] The above detailed description includes references to the accompanying drawings, which form a part of the detailed description. The

drawings show, by way of illustration, specific embodiments in which the invention can be practiced. These embodiments are also referred to herein as “examples.” Such examples can include elements in addition to those shown or described. However, the present inventors also contemplate examples in which only those elements shown or described are provided. Moreover, the present inventors also contemplate examples using any combination or permutation of those elements shown or described (or one or more aspects thereof), either with respect to a particular example (or one or more aspects thereof), or with respect to other examples (or one or more aspects thereof) shown or described herein.

10 **[0070]** In this document, the terms “a” or “an” are used, as is common in patent documents, to include one or more than one, independent of any other instances or usages of “at least one” or “one or more.” In this document, the term “or” is used to refer to a nonexclusive or, such that “A or B” includes “A but not B,” “B but not A,” and “A and B,” unless otherwise indicated. In this document, the terms “including” and “in which” are used as the plain-English equivalents of the respective terms “comprising” and “wherein.” Also, in the following claims, the terms “including” and “comprising” are open-ended, that is, a system, device, article, composition, formulation, or process that includes elements in addition to those listed after such a term in a claim are still deemed to fall within the scope of that claim. Moreover, in the following claims, the terms “first,” “second,” and “third,” etc. are used merely as labels, and are not intended to impose numerical requirements on their objects.

25 **[0071]** The above description is intended to be illustrative, and not restrictive. For example, the above-described examples (or one or more aspects thereof) may be used in combination with each other. Other embodiments can be used, such as by one of ordinary skill in the art upon reviewing the above description.

30 **[0072]** The Abstract is provided to allow the reader to quickly ascertain the nature of the technical disclosure. It is submitted with the understanding that it will not be used to interpret or limit the scope or meaning of the claims.

[0073] Also, in the above Detailed Description, various features may be grouped together to streamline the disclosure. This should not be interpreted as intending that an unclaimed disclosed feature is essential to any claim. Rather,

inventive subject matter may lie in less than all features of a particular disclosed embodiment. Thus, the following claims are hereby incorporated into the Detailed Description, with each claim standing on its own as a separate embodiment, and it is contemplated that such embodiments can be combined
5 with each other in various combinations or permutations. The scope of the invention should be determined with reference to the appended claims, along with the full scope of equivalents to which such claims are entitled.

CLAIMS

1. An integrated circuit assembly, comprising:
a substrate;
5 a member on the substrate;
a first die mounted to the substrate within an opening in the member such
that there is space between the first die and the member;
an underfill between the first the die and the substrate, wherein the
underfill at least partially fills the space between the die and member; and
10 a second die mounted to the first die and the member.
2. The integrated circuit assembly of claim 1, wherein an epoxy partially
fills the space between the first die and the member, and the epoxy attaches the
second die to the first die.
- 15 3. The integrated circuit assembly of claim 1, wherein the second die is
mounted to the member on all sides of the opening.
4. The integrated circuit assembly of claim 1, wherein the first die is below
20 an upper surface of the member.
5. The integrated circuit assembly of claim 1, wherein an upper surface of
the first die is coplanar with an upper surface of the member.
- 25 6. The integrated circuit assembly of claim 1, wherein the first die is a
system-on-chip die, and wherein the second die is a memory die.
7. The integrated circuit assembly of claim 1, wherein the underfill fills the
space between the die and member.
- 30 8. The integrated circuit assembly of claim 1, wherein the second die is less
than 250 micrometers thick, wherein the second die overhangs the member by
between 500 and 3000 micrometers.

9. The integrated circuit assembly of claim 1, wherein the first die includes through silicon vias that electrically connect the second die to the substrate.
10. The integrated circuit assembly of claim 1, wherein the member includes
5 through member vias that electrically connect the second die to the substrate.
11. The integrated circuit assembly of claim 1, wherein an upper surface of the second die is wire bonded to an upper surface of the member.
- 10 12. The integrated circuit assembly of claim 1, wherein an upper surface of the second die is wire bonded to the substrate.
13. An integrated circuit assembly, comprising:
a substrate;
15 a member formed on the substrate;
a first die mounted to the substrate within an opening in the member such that there is space between the first die and the member and the member surrounds the first die, and wherein an upper surface of first die does is coplanar upper surface of the member;
20 an underfill between the first the die and the substrate, wherein the underfill at least partially fills the space between the die and member; and
a second die mounted to the first die and the member, wherein the second die is mounted to the member on all sides of the opening.
- 25 14. The integrated circuit assembly of claim 13, wherein the second die is mounted to the first die and the member using an epoxy, and wherein the epoxy at least partially fills the space between the die and member.
15. The integrated circuit assembly of claim 13, wherein the first die is
30 thermal compression bonded to the substrate, and wherein the second die is flip-chip mounted to the first die.

16. The integrated circuit assembly of claim 13, wherein the first die is a system-on-chip die, and wherein the second die is a memory die.

17. The integrated circuit assembly of claim 13, wherein the second die is
5 less than 250 micrometers thick, and wherein the second die overhangs the member by between 500 and 3000 micrometers.

18. An integrated circuit assembly, comprising:
a substrate with a die side;
10 a first die including four edges, a first-die active surface, and a first-die backside surface, wherein the first-die active surface is mounted to the substrate die side;
an underfill between the first die and the substrate;
a second die including a second-die active surface and a second-die
15 backside surface, wherein the second-die active surface is mounted to the first die backside surface, and
wherein the second die overhangs the first die on all four edges.

19. The integrated circuit assembly of claim 18, further including a mold that
20 forms an opening onto the substrate in which the first die is mounted.

20. The integrated circuit assembly of claim 18, wherein the second die is
also mounted to an upper surface of the mold substrate that is substantially
coplanar with the first-die backside surface.

25

21. The integrated circuit assembly of claim 18, further including a mold that
forms an opening onto the substrate in which the first die is mounted, and
wherein the second die is also mounted to an upper surface of the mold substrate
that is substantially coplanar with the first-die backside surface.

30

22. The integrated circuit assembly of claim 18, further including a mold that forms an opening onto the substrate in which the first die is mounted, wherein the second die is also mounted to an upper surface of the mold substrate that is substantially coplanar with the first-die backside surface, and wherein the first
- 5 die is a system-on-chip die and the second die is a memory die.

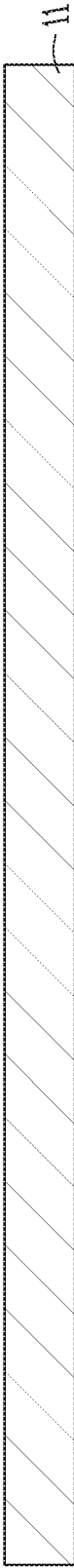


Fig. 1

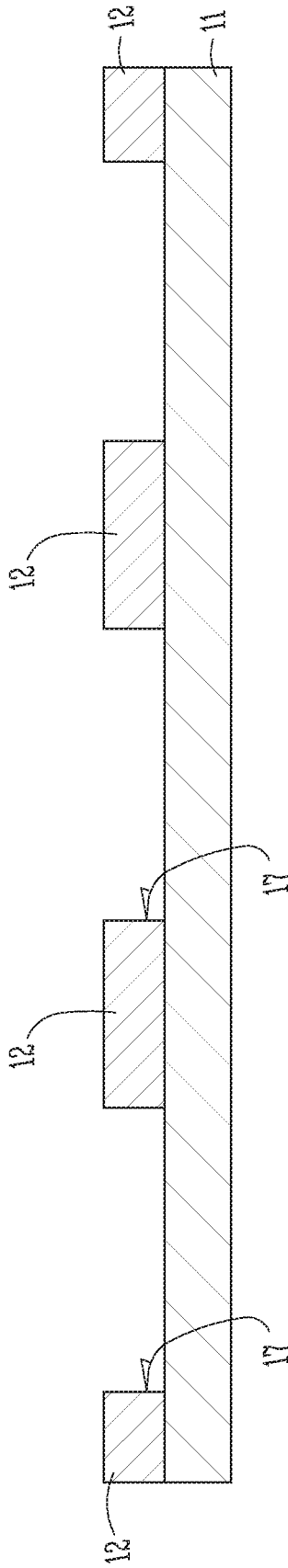


Fig. 2

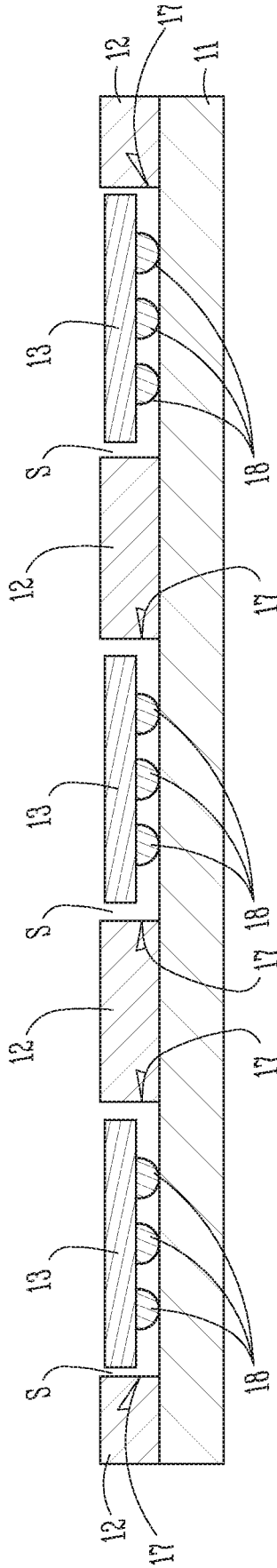


Fig. 3

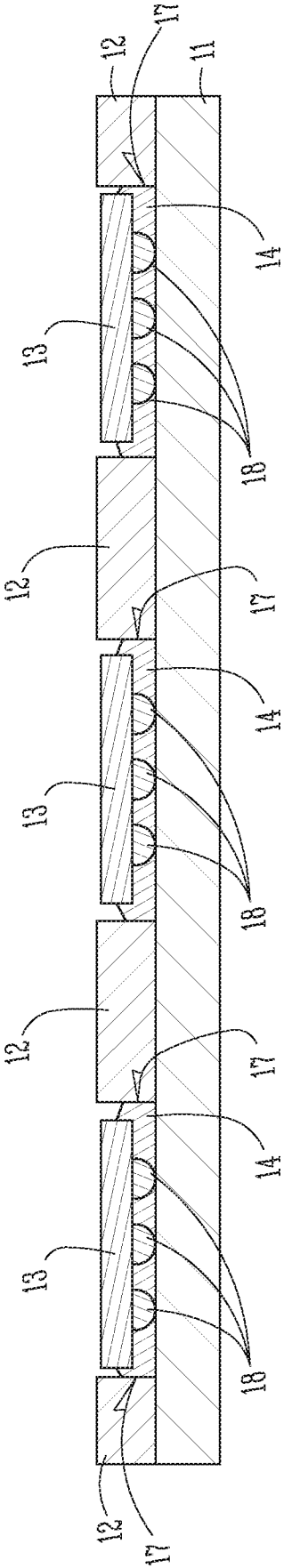


Fig. 4

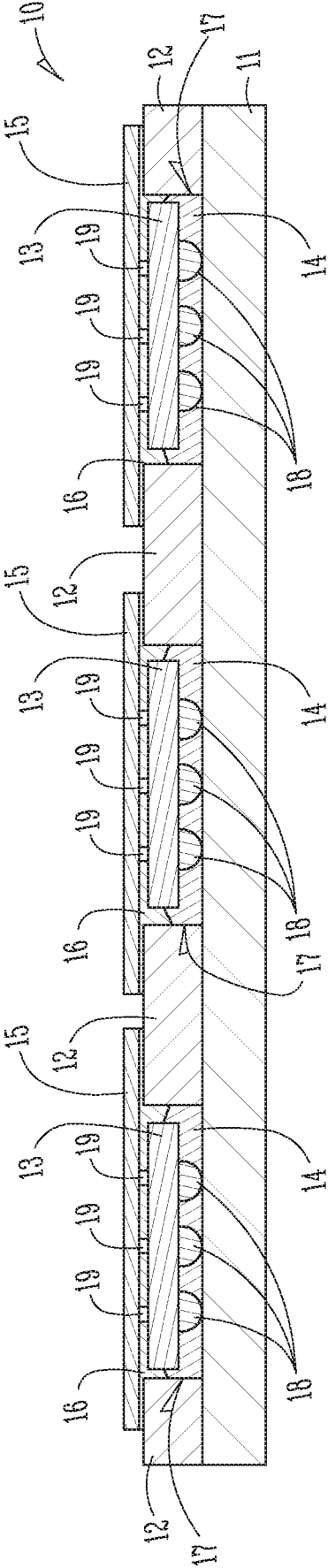


Fig. 5

3/4

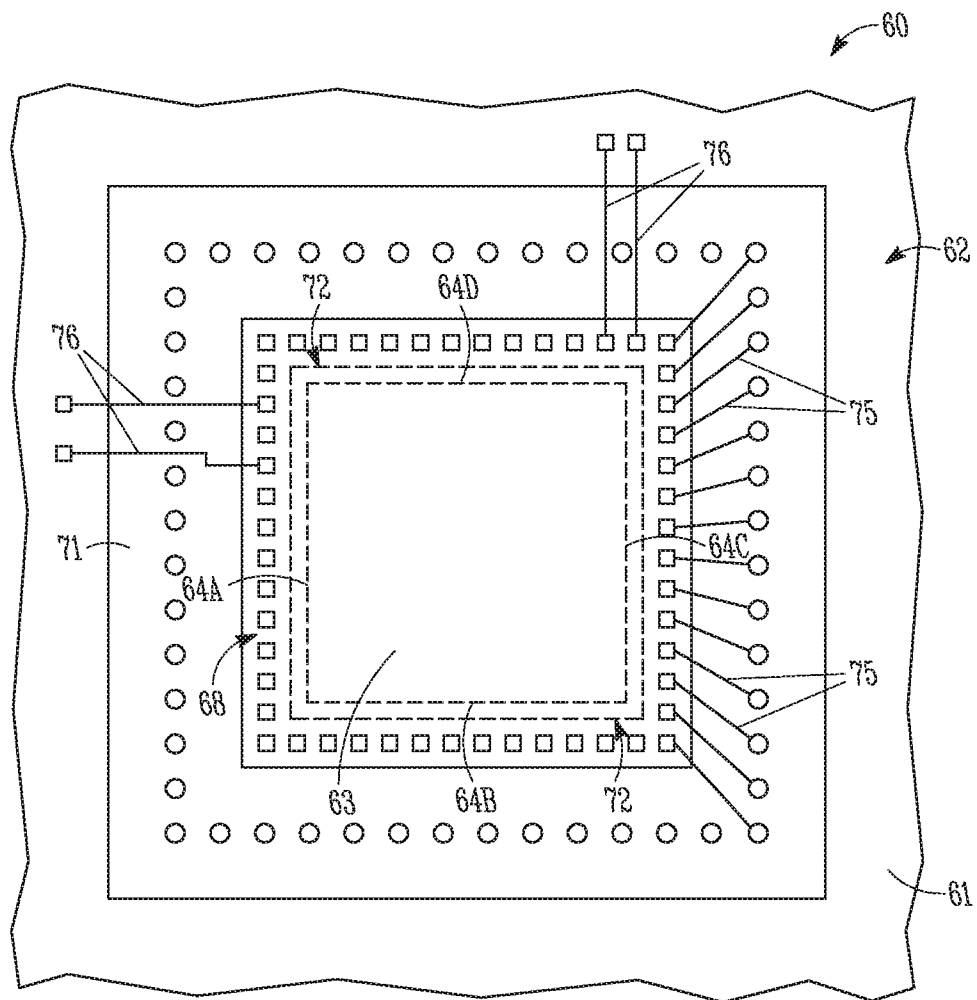


Fig. 6

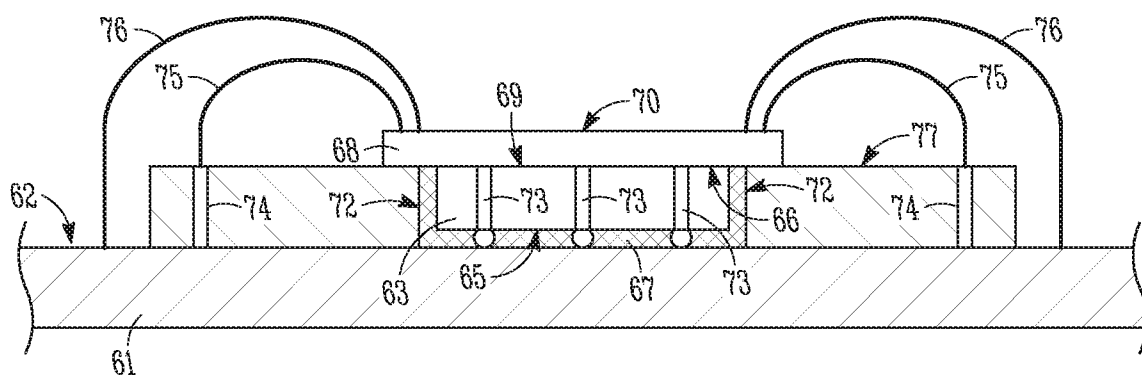
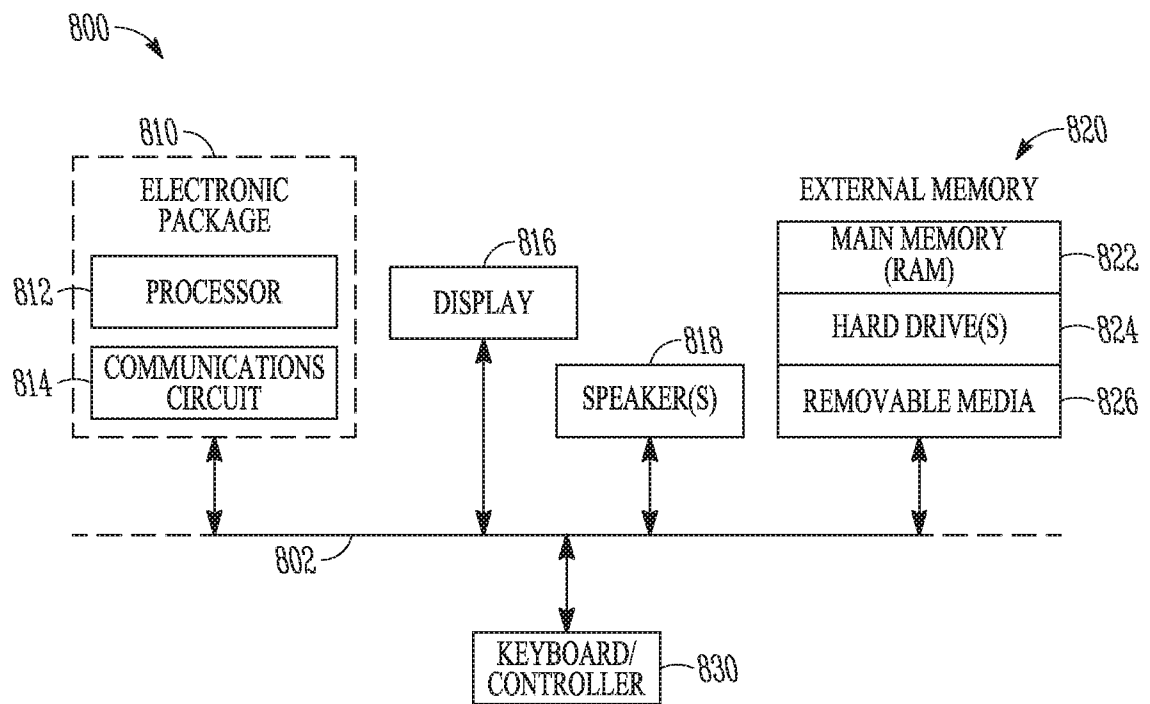


Fig. 7

4/4

*Fig. 8*

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2016/062825**A. CLASSIFICATION OF SUBJECT MATTER****H01L 25/065(2006.01)i, H01L 23/13(2006.01)i, H01L 23/00(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 25/065; H01L 23/31; H01L 25/11; H01L 21/50; H01L 23/02; H01L 21/82; H01L 23/58; H01L 25/07; H01L 21/44; H01L 23/13; H01L 23/00

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: integrated, circuit, assembly, stack, dice

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2012-0049332 A1 (JEN-CHUAN CHEN et al.) 01 March 2012 See paragraphs [0015],[0020]-[0021],[0024], claims 1,3,7,11,13,16-17 and figures 2C,2G,2H,2K,4.	1-22
A	US 2010-0078791 A1 (CHOONG-BIN YIM et al.) 01 April 2010 See paragraphs [0024],[0030]-[0034] and figure 1A.	1-22
A	JP 2013-069988 A (TOSHIBA CORP.) 18 April 2013 See claims 1-5 and figure 3(a).	1-22
A	US 8446000 B2 (CHI-CHIH SHEN et al.) 21 May 2013 See claims 1,7 and figures 1C-1G.	1-22
A	US 6727119 B2 (TAKAKI SAITOU) 27 April 2004 See claims 1-5 and figures 13-15.	1-22



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

06 March 2017 (06.03.2017)

Date of mailing of the international search report

06 March 2017 (06.03.2017)

Name and mailing address of the ISA/KR

International Application Division

Korean Intellectual Property Office

189 Cheongsa-ro, Seo-gu, Daejeon, 35208, Republic of Korea



Facsimile No. +82-42-481-8578

Authorized officer

Lee, Eun Kyu

Telephone No. +82-42-481-3580



INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2016/062825

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2012-0049332 A1	01/03/2012	TW 201209936 A TW I445104 B	01/03/2012 11/07/2014
US 2010-0078791 A1	01/04/2010	JP 2010-087516 A KR 10-1481577 B1 KR 10-2010-0036073 A US 2011-0275177 A1 US 7999368 B2 US 8187921 B2	15/04/2010 13/01/2015 07/04/2010 10/11/2011 16/08/2011 29/05/2012
JP 2013-069988 A	18/04/2013	None	
US 8446000 B2	21/05/2013	TW 201118991 A TW I392069 B US 2011-0121442 A1	01/06/2011 01/04/2013 26/05/2011
US 6727119 B2	27/04/2004	JP 03865606 B2 JP 2003-109982 A US 2003-0064549 A1	10/01/2007 11/04/2003 03/04/2003