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(54) Title: LOW SPEED, LOAD INDEPENDENT, SLEW RATE CONTROLLED OUTPUT BUFFER WITH NO DC POWER CONSUMPTION

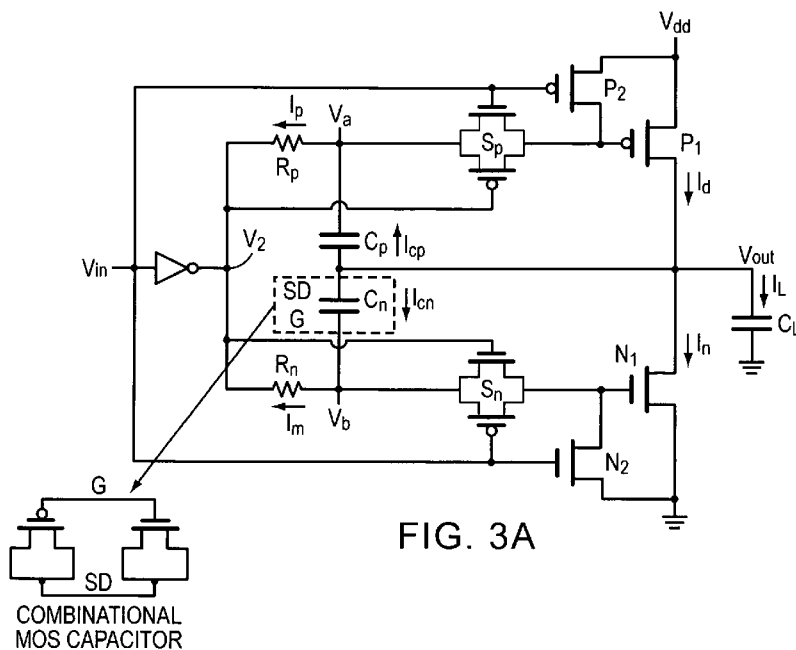


FIG. 3A

FIG. 3B

(57) Abstract: An output buffer utilizes capacitive feedback to control the output slew rate largely independent of load capacitance. The invention slows the rising and falling slew rates and via a capacitance feedback reduces the effect of load capacitance on slew rate, and uses no DC current. Transistor switches are employed to isolate and reduce noise and interaction among the circuit components and functions.



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LOW SPEED, LOAD INDEPENDENT, SLEW RATE CONTROLLED OUTPUT BUFFER WITH NO DC POWER CONSUMPTION

BACKGROUND OF THE INVENTION

Field of the Invention

5 The present invention relates to CMOS output buffers, and more particularly to output buffers with controlled slow slew rates that are relatively independent of capacitive loads and draw no DC power.

Background Information

10 Output buffers must be fast enough to match the high data rates of the signals the buffer is sending, but they must be slow enough to not cause EMI (ElectroMagnetic Interference) with nearby electronics. "Fast enough" and "slow enough" refers to the speed of rising and falling edges. Slew rates, edge "rise and fall times," and other such terms as may be used in the art may have different definitions, but they are used interchangeably herein.

15 Output load capacitance has a substantial effect of slew rates. With a 20/1 capacitive load variation, prior art slew rates may vary proportionally or even more depending on the equivalent resistance operating with the load capacitance.

20 FIG. 1 illustrates a prior art output buffer's voltage profiles with 10pF, 75pF and 150pF capacitive loads. So, for example, if a square wave is input, the output edge rise and fall times 10 are about one nanosecond with a 10pF load capacitor, and those times increase to twenty-four nanoseconds with a 150pF load capacitor. In this example a 15 to 1 increase in output capacitance results in a 24 to 1 edge slow down.

25 Limitations of the prior art include one nano-second edge times that may generate EMI noise adversely affecting other electronics, and, with large load capacitors, slow edge rise and fall times may not meet the data rates of the signals involved.

 U.S. Patent No. 5,748,019 ('019) owned by VLSI Technologies, Inc. of San Jose, CA compensates for load capacitance. The '019 reference, however, uses reference

voltage supplies, current sources and capacitive feedback. But the '019 use voltage references, that constantly drain DC current, and capacitors and current sources that distinguish this reference from the present invention.

It would be advantageous to have an output buffer with an output edge time that remained about constant with capacitive load variations; that was slow enough to not cause EMI disturbances, but was fast enough to meet the data rates of the circuitry involved. For example, an output buffer with an edge rising and falling time of about 20 to 40 nanoseconds when loaded with 10 to 200pF capacitors, respectively.

SUMMARY OF THE INVENTION

The present invention provides a capacitive feedback circuit that substantially reduces, with respect to prior art, slew rate variations when the capacitive load varies substantially.

Separate RC (Resistor/Capacitor) networks are formed for both positive and negative voltage edges at the output of the buffer. These RC's are arranged to provide a negative feed back to control the slew rates relatively independent of the load capacitors.

Illustratively, the present invention provides for a single inverter input and the charging and discharging of load capacitors and the feedback capacitors through the same output transistor. Current through the feedback capacitor to the gate or control input of the output transistor slows the turn on of the output transistor, reduces the current to the load capacitor thereby slowing the edge rise and fall times of the output voltage. The net effect is to make the slew rate relatively independent of the load capacitors. One way of describing the effect is that the feedback current is dependent upon the load capacitance current. As more load current is delivered, a negative feedback current reduces the rate of increase of load current.

Illustratively, the present invention employs a combination of PMOS and parallel "native NMOS transistors" as the feedback capacitors. This embodiment provides cleaner output rise and fall times. Herein a "native NMOS transistor" refers to a an NMOS transistor that has not undergone channel doping. Such transistors have lower threshold voltages (usually 0 to 3V, or even negative) because it must rely on the intrinsic

background or body of the transistor to set the threshold voltage. Because the threshold voltage is lower, a native device provides a better capacitor with a wider voltage range.

It will be appreciated by those skilled in the art that although the following Detailed Description will proceed with reference being made to illustrative embodiments, the drawings, and methods of use, the present invention is not intended to be limited to these embodiments and methods of use. Rather, the present invention is of broad scope and is intended to be defined as only set forth in the accompanying claims.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention description below refers to the accompanying drawings, of which:

FIG. 1 is a timing diagram of a prior art output buffer response;

FIG. 2A is a schematic illustrating the feedback character of the present invention;

FIG. 2B is a timing chart of signals associated with FIG 2A;

FIG. 3A is a more detailed schematic illustrating the present invention;

FIG. 3B is schematic of an implementation of the MOS capacitors;

FIG. 4 is a timing diagram of the circuit of FIG. 3A output buffer response; and

FIG. 5 is a timing chart illustrating a transition area of the circuit of FIG. 3A.

DETAILED DESCRIPTION OF AN ILLUSTRATIVE EMBODIMENT

FIG. 2A is a simplified schematic illustrating a capacitive feedback circuit embodiment of the present invention. FIG. 2B is the associated timing diagram.

With V_{in} low 26, V_2 is high and P2 on driving V_a high and keeping P1 off. V_b is high turning on N1 that drives V_{out} low. When V_{in} goes high 28, V_2 goes low, and N2 turns on, drives V_b low and turns N1 off. I_p rises drawing current from C_p , C_n and C_l , and V_a starts to fall 30. Since P1 is not yet on I_d is delayed 21, and V_{out} falls slightly 20 as some of I_p is taken from C_l .

V_a falls to a point 22 where P1 starts to turn on supplying I_d . I_d charges C_l and V_{out} rises 24. As V_{out} rises some of I_d flows through C_p to V_a . This feedback action slows the fall of V_a , slows the turn on of P1 and the rise if I_d . Note that as V_{out} rises

some of I_d is diverted through C_n . Nonetheless, V_{out} rises more slowly but with more control and less dependence on C_l than in prior art buffers. Using other words, the feedback operation operates as follows, if C_l is larger, with the same I_d current, V_{out} will rise more slowly thereby driving less current through C_p . V_a falls more quickly, turning
5 on P_1 more quickly and increasing I_d to charge C_l more quickly. If C_l is smaller, C_l charges more quickly, V_a rises more quickly slowing the turn on of P_1 and slowing the rise of I_d and the charging of C_l .

When V_{in} goes back low 31, P_1 is turned off via P_2 and N_2 is turned off allowing N_1 to turn on. V_b is low and starts going high 32. As V_b rises it drives current through
10 C_n , C_p and C_l where V_{out} rises 34 slightly. The turn on of N_1 is delayed 33, but at point 36 N_1 starts to turn on supplying I_n to drive V_{out} low 38. Here the low going V_{out} draws current from V_b via C_n and slows the rise of V_b and thus the turn on of N_1 . the operation is similar to that for the rising V_{out} as described before.

FIG. 3A is a more detailed schematic of the base circuit of FIG. 2A. The additions
15 in FIG. 3A are: the S_p switch that connect R_p to P_1 gate when V_{in} goes high; and the S_n switch that connects R_n to N_1 gate when V_{in} is low. As shown in FIG. 3B, the capacitors C_p and C_n are each formed from a combination of a P and a native N type CMOS transistor.

In other embodiments the C_p and C_n capacitors may be of virtually any structure,
20 e.g. from a capacitor, not formed from a diode or transistor, but from electrodes separated by a dielectric. Other examples of C_p and C_n include: a single or multiple PMOS structures; a single or multiple NMOS structures; any combination of PMOS and non-native NMOS structures; reciprocally connected PMOS and NMOS (NMOS gate to PMOS source/drain, PMOS gate to NMOS source/drain, and other such
25 combination); and even in some embodiments reverse biased bipolar structures.

The output transistors P_1 and N_1 are isolated by the S_p and S_n switches, and held off by P_2 and N_2 , thereby isolating the output transistors P_1 and N_1 from each other virtually eliminating any "crowbar" current. Moreover, the circuit draws no DC current since there are no DC current paths.

30 FIG. 4 shows the output buffer response of the circuit of FIG. 3A, 3B with a square wave voltage input and load capacitors of 10pF trace 40, 75pF, trace 42, and

150pF, trace 44. The corresponding rise times are 17 nanoseconds for trace 40 to 37 nanoseconds for trace 44.

FIG. 5 illustrates a rising edge of the V_{out} and the falling edge V_a (at the gate of P1) as P1 turns on at 22 producing current I_d . Note the dip in V_{out} 20 where P2 is not yet on, and current is first drawn via C_p from C_l . The circled part is where I_l about equals I_{cp} .

It should be understood that above-described embodiments are being presented herein as examples and that many variations and alternatives thereof are possible. Accordingly, the present invention should be viewed broadly as being defined only as set forth in the hereinafter appended claims.

What is claimed is:

CLAIMS

- 1 1. An output buffer comprising:
2 an inverter with an input connected to an input signal, the inverter defining an
3 inverter output;
4 a pull up output transistor with its drain connected to a signal output;
5 a resistor with one end connected to the inverter output and the other end
6 connected to the gate of the pull up transistor;
7 a feedback capacitor connected between the gate of the pull up transistor and the
8 signal output; wherein when the input signal goes high, the inverter output goes low and
9 the gate voltage starts to go low turning on the pull up output transistor, the signal output
10 starts to go high, wherein the signal output going high drives current through the
11 feedback capacitor thereby slowing the fall of the gate voltage and slows the rises of the
12 signal output, and wherein the output buffer uses no DC current.
- 1 2. The output buffer of claim 1 further comprising:
2 a pull down transistor with its drain connected to the output;
3 a second resistor with one end connected to the inverter output and the other end
4 connected to the gate of the pull down transistor;
5 a second feedback capacitor connected between the gate of the pull down
6 transistor and the output; wherein when the inverter output goes high, the gate voltage
7 starts to go high turning on the pull down output transistor, the signal output starts to go
8 low, wherein the signal output going low drives current through the second feedback
9 capacitor thereby slowing the rise of the pull down transistor gate voltage and slows the
10 fall of the signal output.
- 1 3. The output buffer of claim 2 further comprising:
2 a third transistor with its source connected to a power supply, its gate connected
3 to the input signal, and its drain to the gate of the pull up transistor, wherein when the
4 input signal goes high, the third transistor is turned on and turns off the pull up transistor;
5 and a fourth transistor with its source connected to a ground, its gate connected to the

6 input signal, and its drain to the gate of the pull down transistor, wherein when the input
7 signal goes low, the fourth transistor is tuned on and turns off the pull down transistor.

1 4. The output buffer of claim 3 further comprising a first switch connected between
2 the gate of the pull up output transistor and the feedback capacitor and the end of the
3 resistor, wherein the switch is turned on when the inverter output goes low and off when
4 the inverter output goes high, and a second switch connected between the gate of the pull
5 down output transistor and the second feedback capacitor and the end of the second
6 resistor, wherein the switch is turned on when the inverter output goes high and off when
7 the inverter output goes low.

1 5. The output buffer of claim 2 wherein the feedback capacitor and the second
2 feedback capacitor both comprise combinational PMOS and a parallel NMOS transistors.

1 6. A method for controlling the edge rise and fall times of an output, the method
2 comprising the steps of:
3 inverting an input signal and producing an inverter output;
4 driving the gate from the inverter output and turning on a pull up transistor via a
5 resistor
6 driving the output from the drain of the pull up output transistor;
7 feeding back the output via a capacitor connected to the gate of the pull up
8 transistor; wherein when the feedback operates to counter the inverter output, and
9 wherein no DC current is used.

1 7. The method of claim 6 further comprising the steps of:
2 driving the gate from the inverter output and turning on a pull down transistor via
3 a second resistor;
4 driving the output from the drain of the second transistor;
5 second feeding back the output via a second capacitor connected to the gate of the
6 pull down transistor, wherein the second feedback operated to counter the inverter output.

- 1 8. The method of claim 7 further comprising the steps of:
2 turning on a third transistor from the input signal, wherein when the third
3 transistor turns on it turns off the pull up transistor; and
4 turning on a fourth transistor from the input signal, wherein when the fourth
5 transistor turns on it turns off the pull down transistor.
- 1 9. The method of claim 8 further comprising the steps of:
2 disconnecting the gate of the pull up output transistor from the feedback capacitor
3 and the resistor when the pull down transistor is being turned on; and ,
4 disconnecting the gate of the pull down output transistor from the second
5 feedback capacitor and the second resistor when the pull up transistor is being turned on.

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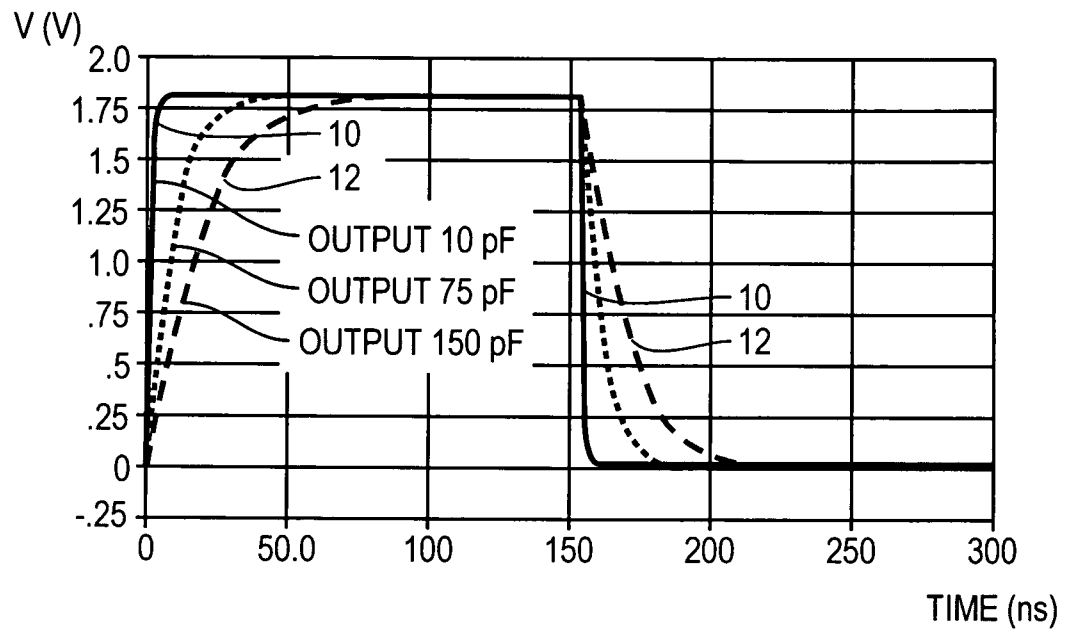


FIG. 1
PRIOR ART

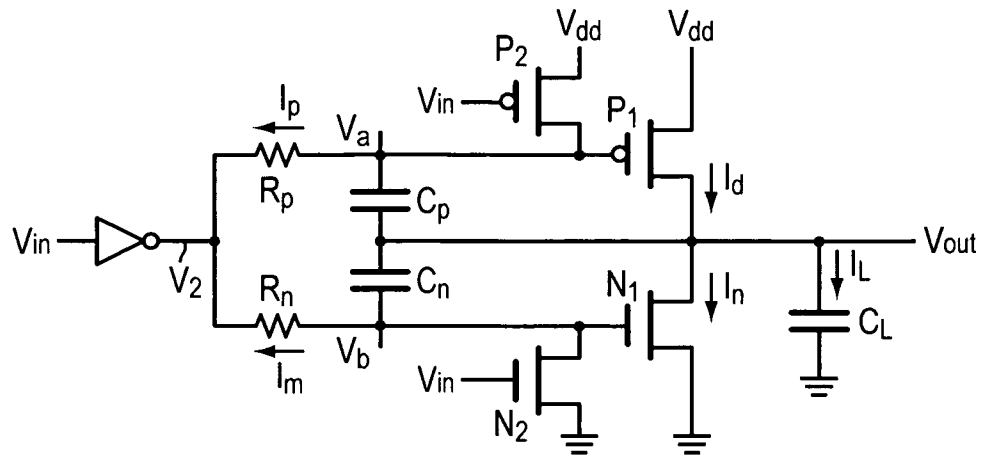


FIG. 2A

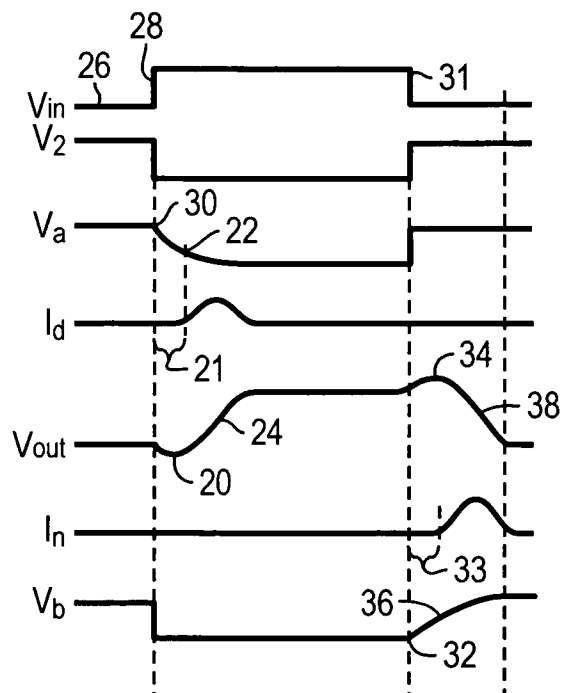


FIG. 2B

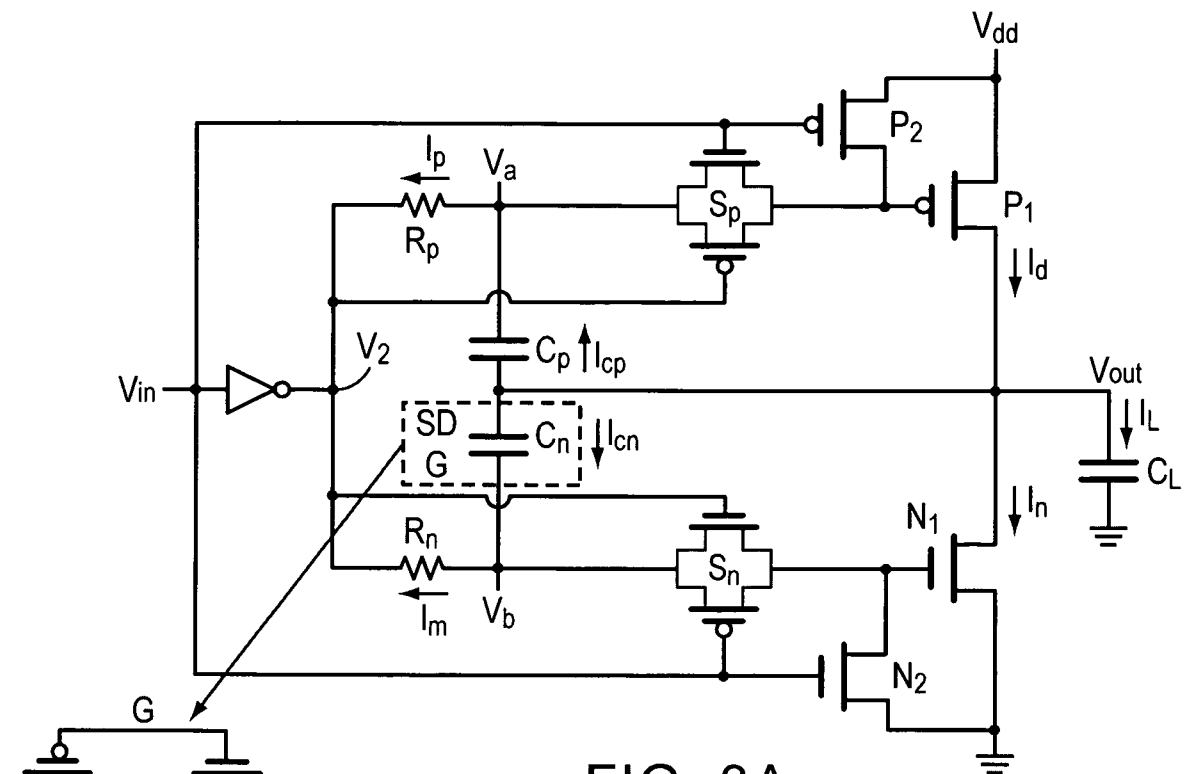


FIG. 3A

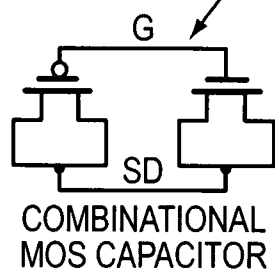


FIG. 3B

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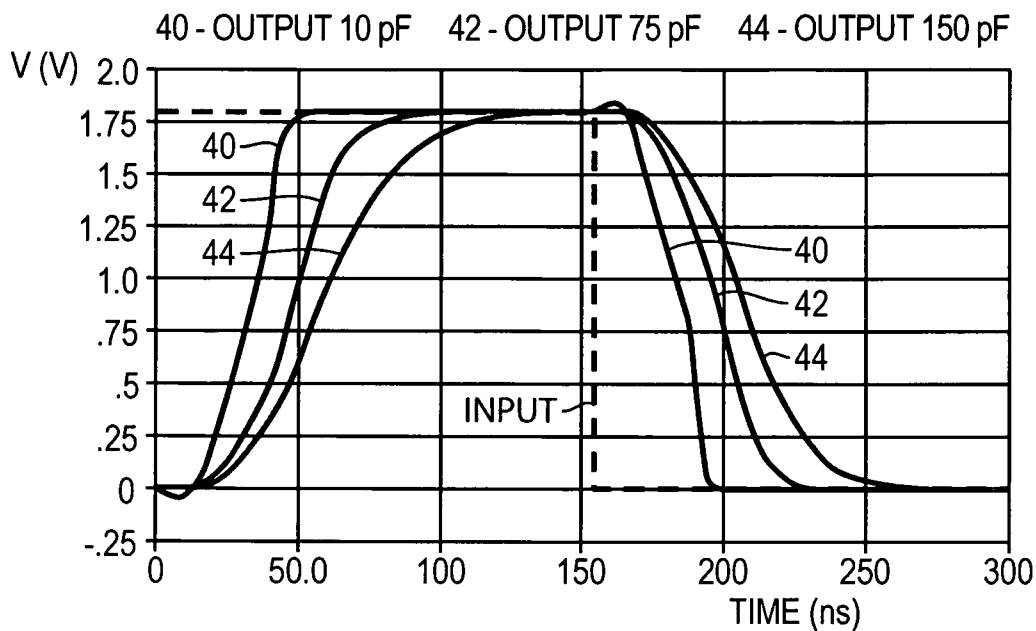


FIG. 4

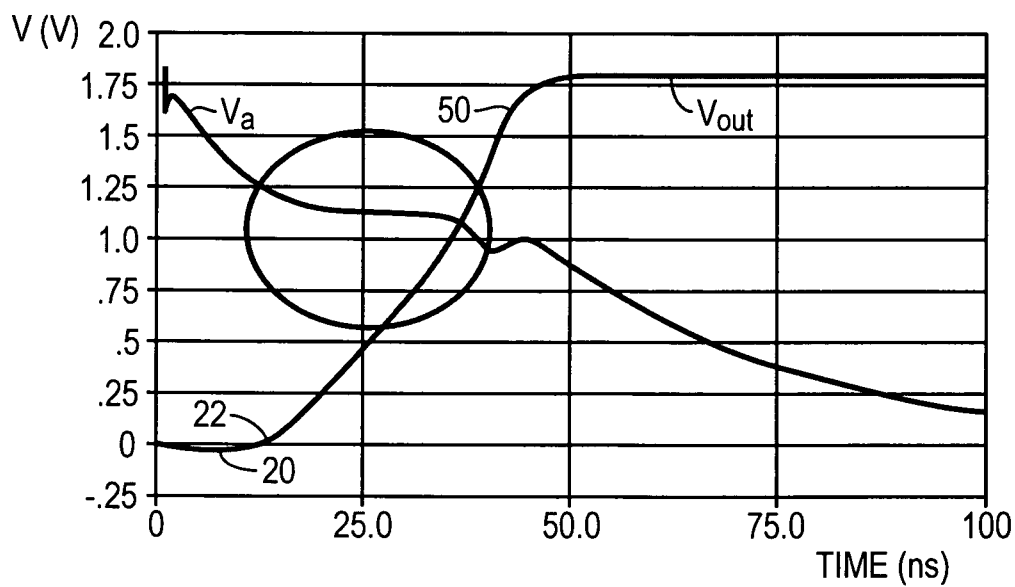


FIG. 5

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