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Declarations under Rule 4.17:
— *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))*
— *as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))*

(54) Title: LOCOS WITH SIDEWALL SPACER FOR DIFFERENT CAPACITANCE DENSITY CAPACITORS

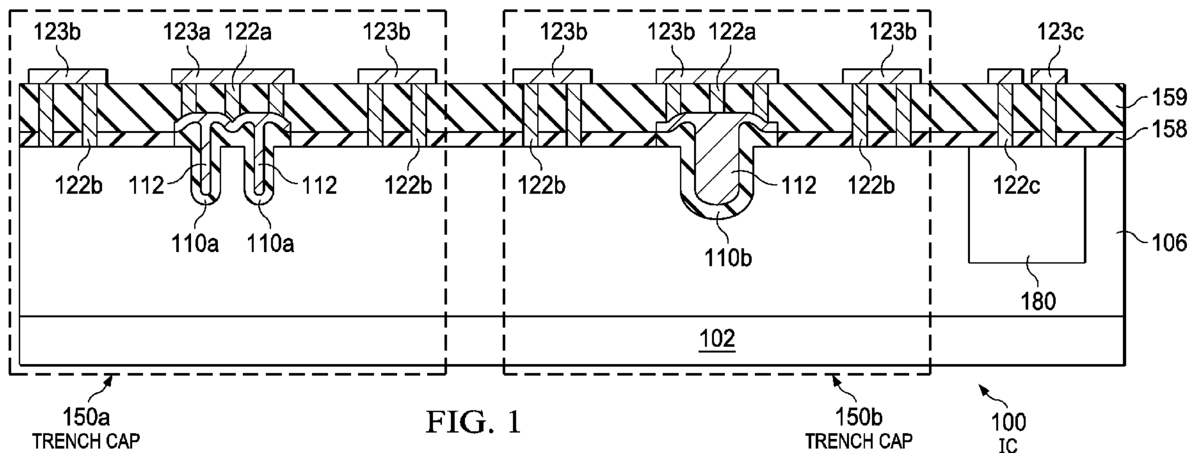

FIG. 1

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(57) Abstract: An integrated circuit (IC) (100) includes a first capacitor (150a), a second capacitor (150b), and functional circuitry (180) configured together with the capacitors for realizing at least one circuit function in a semiconductor surface layer (106) on a substrate (102). The capacitors include a top plate (112) over a LOCal Oxidation of Silicon (LOCOS) oxide (110a, 110b), wherein a thickness of the LOCOS oxide for the second capacitor is thicker than a thickness of the LOCOS oxide for the first capacitor. There is a contact (122a) for the top plate and a contact (122b) for the bottom plate for the first and second capacitors.

[Continued on next page]

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LOCOS WITH SIDEWALL SPACER FOR DIFFERENT CAPACITANCE DENSITY CAPACITORS

[0001] This description relates to integrated circuits having LOCOS capacitors.

BACKGROUND

[0002] LOCal Oxidation of Silicon (LOCOS) is a semiconductor fabrication process that uses a patterned oxygen diffusion barrier layer, commonly a silicon nitride layer over areas not meant to be oxidized, where a thermally grown silicon dioxide layer is formed in etched apertures in the oxygen diffusion barrier layer at a given thickness, with a thinner tapered silicon oxide region being formed along the edges of the oxygen diffusion barrier layer. A Si-silicon oxide interface is formed at a lower point than the rest of the silicon surface. Some capacitors utilize a LOCOS oxide as their dielectric. Although the active areas widths bordered by a LOCOS oxide can be varied, LOCOS like other oxide growth processes provide a single given oxide thickness across the die and across the wafer.

SUMMARY

[0003] This Summary is provided to introduce a brief selection of described concepts in a simplified form that are further described below in the Detailed Description including the drawings provided. This Summary is not intended to limit the claimed subject matter's scope.

[0004] Disclosed aspects include an integrated circuit (IC) formed in a semiconductor surface layer on a substrate that includes a first capacitor and a second capacitor. The first and second capacitors include top plate over a LOCOS oxide, and the thickness of the LOCOS oxide for the second capacitor is thicker than the thickness of the LOCOS oxide for the first capacitor. There is a contact for the top plate and a contact for a bottom plate for both the first and second capacitors.

BRIEF DESCRIPTION OF THE DRAWINGS

[0005] Reference will now be made to the accompanying drawings, which are not necessarily drawn to scale, wherein:

[0006] FIG. 1 is a cross sectional depiction of an example IC including a first and a second LOCOS capacitor that have different LOCOS oxide thicknesses to provide different capacitance

densities, according to an example.

[0007] FIGS. 2A-2F are cross-sectional diagrams showing processing progression for an example method of forming an IC having including a first and a second planar LOCOS capacitor having different capacitance densities, according to an example.

[0008] FIGS. 3A-3G are cross-sectional diagrams showing processing progression for an example method of forming an IC including a first and a second trench LOCOS capacitor having different capacitance densities, according to an example.

[0009] FIGS. 4A-4F are cross-sectional diagrams showing processing progression for another example method of forming an IC having a first planar LOCOS capacitor and a second trench LOCOS capacitor that have different capacitance densities, according to an example.

DETAILED DESCRIPTION OF EXAMPLE EMBODIMENTS

[0010] Examples are described with reference to the drawings, wherein like reference numerals are used to designate similar or equivalent elements. Illustrated ordering of acts or events should not be considered as limiting, as some acts or events may occur in different order and/or concurrently with other acts or events. Furthermore, some illustrated acts or events may not be required to implement a methodology in accordance with this description.

[0011] Also, the terms "coupled to" or "couples with" (and the like) as used herein without further qualification are intended to describe either an indirect or direct electrical connection. Thus, if a first device "couples" to a second device, that connection can be through a direct electrical connection where there are only parasitics in the pathway, or through an indirect electrical connection via intervening items including other devices and connections. For indirect coupling, the intervening item generally does not modify the information of a signal but may adjust its current level, voltage level, and/or power level.

[0012] Disclosed aspects recognize it is desirable to be able to form different capacitance density (capacitance/unit area) capacitors using a single masking level and a single patterning step. For some power transistors integrated into a Bipolar Complementary Metal Oxide Semiconductor (BiCMOS) process, this presents a cost and/or complexity problem, because multiple different capacitance density capacitors are needed to co-exist in the same technology, including in some cases on the same IC product. It is also recognized that some LOCOS approaches like other oxidation processes have the disadvantage of only providing a single oxide thickness. This description describes a LOCOS oxidation process flow that utilizes sidewall

spacers to produce two or more distinct LOCOS oxide thicknesses.

[0013] Forming sidewall spacers in wider oxygen diffusion barrier (ODB) layer opening(s) over the semiconductor surface layer, but not forming sidewall spacers in a narrower width ODB layer opening(s) over the semiconductor surface enables creating at least two different LOCOS oxide thicknesses from a single mask level and patterning step. The thicker LOCOS oxide for planar LOCOS capacitors will be thicker in the thickest center region as well as in the thinner bird's beak region at the edge of the LOCOS oxide as compared to the thinner LOCOS oxide. Sidewall spacers (e.g., comprising silicon nitride) formed in a wider first ODB layer opening(s) but not in a narrower first ODB layer opening(s) creates two (or more) different LOCOS layer thicknesses, which thus depend on the width of the first ODB layer opening. The width of the wider first ODB layer opening (referred to herein as the 2nd first ODB layer opening) is generally at least 0.05 µm wider than the width of the narrower first ODB layer opening (referred to herein as the 1st first ODB layer opening).

[0014] FIG. 1 is a cross sectional depiction of an example IC 100 including a first trench capacitor 150a and a second trench capacitor 150b that have different LOCOS oxide thicknesses to provide different capacitance densities. The second trench capacitor 150b can be seen to be considerably wider and have a significantly thicker LOCOS oxide 110b thickness as compared to the width and thickness of LOCOS oxide 110a for the first trench capacitor 150a. The trench capacitors 150a, 150b each have a top plate 112. The IC 100 also includes functional circuitry 180 shown as a block that comprises circuit elements (including transistors, and generally diodes, resistors, capacitors, etc.) formed in the semiconductor surface layer 106 of or on the substrate 102 that is configured together with the trench capacitors 150a and 150b for realizing at least one circuit function such as analog (e.g., an amplifier, power converter or power field effect transistor (FET)), RF, digital, or a memory function.

[0015] Although no field oxide is shown, IC 100 generally includes field oxide that may comprise a shallow trench isolation (STI) structure or the field oxide may also have a LOCOS oxide structure. A pre-metal dielectric (PMD) layer is shown as 159 and has thereunder a pad oxide layer as 158. Top side contacts are shown formed through the PMD layer 159 and the pad oxide layer 158 including contacts 122a to the top plates 112 and contacts 122b to the portion of the semiconductor surface layer 106 providing the bottom plates that have metal contacts 123a, and 123b shown as metal 1 (M1) contacts thereon. Top side contacts shown also include

contacts 122c to the functional circuitry 180 having M1 contacts 123c thereon. Although the trench capacitor 150a is shown having two trenches, and trench capacitor 150b having one trench, trench capacitors can generally have any number of trenches.

[0016] FIGS. 2A-2G are cross-sectional diagrams showing processing progression for an example method of forming an IC including a first planar capacitor 180a and a second planar capacitor 180b that have different LOCOS oxide thicknesses to provide different capacitance densities. Referring to FIG. 2A, the in-process IC is shown after forming a 1st first ODB layer opening 164a that is relatively narrower and a 2nd first ODB layer opening 164b that is relatively wider in a first ODB layer 160 that is on a pad oxide layer 158 layer which is on semiconductor surface layer 106 of a substrate 102. The ODB layer openings 164a, 164b are generally formed using a photoresist pattern as an etch mask and then etching apertures including a first width and at least a second width in the first ODB layer 160.

[0017] The substrate 102 may be formed by starting with a p-type silicon wafer, possibly with at least one epitaxial layer thereon, and forming a n-type buried layer by implanting n-type dopants such as antimony or arsenic at a dose of $1\times10^{15}\ cm^{-2}$ to $1\times10^{16}\ cm^{-2}$. A thermal drive process heats the wafer to activate and diffuse the implanted n-type dopants. A p-type layer for the semiconductor surface layer 106 may be formed on the wafer by an epitaxial process with in-situ p-type doping. The epitaxially formed material may be, for example 4 microns to 6 microns thick. Although not shown, there may be an n-type buried layer that overlaps a boundary between the original silicon wafer and the epitaxially grown material for the semiconductor surface layer 106. An average bulk resistivity of the p-type layer may be, for example, 1 ohm-cm to 10 ohm-cm. An optional p-type buried layer may be also formed in the case of a p-type semiconductor surface layer 106 by implanting boron at an energy, for example, of 2 mega-electron volts (MeV) to 3 MeV.

[0018] The pad oxide layer 158 may be, for example, 20 to 250A thick, 100A thick, and may be formed by thermal oxidation or by any of several chemical vapor deposition (CVD) processes. The first ODB layer 160 may include, for example, silicon nitride, such as formed by a low pressure chemical vapor deposition (LPCVD) process using dichlorosilane and ammonia. Alternatively, silicon nitride for the first ODB layer 160 may be formed by decomposition of bis(tertiary-butyl-amino) silane (BTBAS). Other processes to form the first ODB layer 160 are possible.

[0019] The etch mask may include photoresist formed by a photolithographic process, and may also include hard mask material such as amorphous carbon, and may include an anti-reflection layer such as an organic bottom anti-reflection coat (BARC). The exposed area of the top surface of the semiconductor surface layer 106 is defined by the 2nd first ODB layer opening 164b for the second planar capacitor 180b has dimensions that are wider than a width of the 1st first ODB layer opening 164a for the first planar capacitor 180a. The 2nd first ODB layer opening 164b is sufficiently wide so that after etching the second ODB layer 181 as described below relative to FIG. 2C a central portion of the etched area becomes cleared resulting in the formation of sidewall spacers, while the 1st first ODB layer opening 164a for the first planar capacitor 180a has a width narrow enough so that after etching the second ODB layer 181 the entire 1st first ODB layer opening 164a remains covered with the second ODB layer 181. The first ODB layer 160 in areas exposed by the etch mask may be removed by a wet etch, for example an aqueous solution of phosphoric acid, which undercuts the etch mask. A portion of the pad oxide 158 may also be removed in the areas exposed by the etch mask.

[0020] Referring now to FIG. 2B, this FIG. shows results after growing a first LOCOS oxide layer 210, with an example thickness between 200 to 1,000A. The characteristic LOCOS oxidation bird's beak with a thinner LOCOS oxide at the edges under the first ODB layer 160 is shown.

[0021] An example furnace thermal oxidation process for growing a first LOCOS oxide layer 210 may include ramping a temperature of the furnace to about 1000° C in a time period of 45 minutes to 90 minutes with an ambient of 2 percent to 10 percent oxygen, maintaining the temperature of the furnace at about 1000° C for a time period of 10 minutes to 20 minutes while increasing the oxygen in the ambient to 80 percent to 95 percent oxygen, maintaining the temperature of the furnace at about 1000° C for a time period of 60 minutes to 120 minutes while maintaining the oxygen in the ambient at 80 percent to 95 percent oxygen and adding hydrogen chloride gas to the ambient, maintaining the temperature of the furnace at about 1000° C for a time period of 30 minutes to 90 minutes while maintaining the oxygen in the ambient at 80 percent to 95 percent oxygen with no hydrogen chloride, and ramping the temperature of the furnace down in a nitrogen ambient.

[0022] FIG. 2C shows results after depositing a second ODB layer 181 then a sacrificial sidewall film 182 on the second ODB layer 181 that functions as a sacrificial sidewall layer,

then maskless etching of the sacrificial sidewall film 182 to form spacers 182a in the 2nd first ODB layer opening 164b as it is sufficiently wide. The second ODB layer 181 is removed in the 2nd first ODB layer opening 164b because it is not protected by the sacrificial sidewall film 182. Sidewall spacers are not shown in the 1st first ODB layer opening 164a as it is narrower compared to the 2nd first ODB layer opening 164b, so that the 1st first ODB layer opening 164a is again shown as the sacrificial sidewall film 182 on the second ODB layer 181 in the 1st first ODB layer opening 164a.

[0023] FIG. 2D shows results after stripping the sacrificial sidewall film 182 and spacers 182a which reveals spacers 181a in the 2nd first ODB layer opening 164b. FIG. 2E shows results after growing a second LOCOS oxide layer resulting in an additional LOCOS portion shown as LOCOS 2 having a portion above and below the first LOCOS oxide layer 210, generally being 500 to 1,500A of LOCOS 2 at the center of the wider 2nd first ODB layer opening 164b for the second planar capacitor 180b, with no LOCOS 2 shown grown in the 1st first ODB layer opening 164a being a narrower opening due to the presence of the second ODB layer 181 over the whole opening.

[0024] Thus for the 1st first ODB layer opening 164a being narrower the sidewalls of the second ODB layer 181 remain merged so that only the first LOCOS oxidation process is able to oxidize the exposed silicon surface. This thinner LOCOS oxide is used to form all the oxide for the first planar capacitor 180a. For the 2nd first ODB layer opening 164b being wider, the sidewalls are distinct (as shown as spacers 181a in FIG. 2D) so that the second LOCOS oxidation can thicken the LOCOS layer by adding LOCOS 2 in the 2nd first ODB layer opening 164b. As with the first LOCOS oxide layer 210, the LOCOS 2 oxide will be tapered under the spacers 181a, which is equivalent to a bird's beak region.

[0025] This completes the oxide thickness so that the LOCOS oxide is thicker for the second planar capacitator 180b as it includes LOCOS oxide from both first LOCOS oxide layer 210 and the LOCOS 2 oxide as compared to the LOCOS oxide for the first planar capacitor 180a that only includes the first LOCOS oxide layer 210. FIG. 2F shows results after removing the first ODB layer 160 and the second ODB layer 181 and then depositing a top plate layer, and patterning this top plate layer to form top plates 112, such as a top plate comprising polysilicon over the LOCOS oxide for the first and second planar capacitors 180a, 180b. Spacers 191 are shown on the sidewalls of the top plates 112.

[0026] FIGS. 3A-3G are cross-sectional diagrams showing processing progression for an example method of forming an IC including a first trench capacitor 350a and a second trench capacitor 350b having different LOCOS oxide thicknesses to provide different capacitance densities. FIG. 3A shows results after forming a 1st first ODB layer opening 164a (shown relatively narrower) and a 2nd first ODB layer opening 164b (shown relatively wider) in a first ODB layer 160 that is on a pad oxide layer 158 layer that is on a semiconductor surface layer 106 on a substrate 102. The ODB layer openings are generally formed by using a photoresist patterned etch mask and then etching the first ODB layer 160 to form the 1st first ODB layer opening 164a for the trench capacitor 350a and the 2nd first ODB layer opening 164b for the trench capacitor 350b. FIG. 3B shows the results after a silicon etch of the top surface of the semiconductor surface layer 106 after an oxide etch to remove pad oxide 158 in the 1st and 2nd first ODB layer opening openings 164a, 164b. An example silicon etch depth is 100 A to 6,000A.

[0027] FIG. 3C shows results after growing a first LOCOS oxide layer 210, with an example thickness between 200A and 1,000A. The characteristic LOCOS oxidation bird's beak is shown. FIG. 3D shows results after results after depositing a second ODB layer 181 then a sacrificial sidewall film 182 on the second ODB layer 181 that functions as a sacrificial sidewall layer, then maskless etching the sacrificial sidewall film 182 to form spacers 182a in the 2nd first ODB layer opening 164b being relatively wider, but not forming sidewall spacers show as sacrificial sidewall film 182 over the entire 1st first ODB layer opening 164a being relatively narrower, and then removing the second ODB layer 181 where not protected by the sacrificial sidewall film 182. FIG. 3E shows results after results after removal of the sacrificial sidewall film 182 including spacers 182a.

[0028] FIG. 3F shows results after growing a second LOCOS oxide layer in the 2nd first ODB layer opening 164b for the trench capacitor 350b resulting in an additional LOCOS portion shown as LOCOS 2 above and below the first LOCOS oxide layer 210, generally being 500 to 1,500A of LOCOS at the center of the wider 2nd first ODB layer opening 164b. There is no LOCOS 2 shown grown in the narrower first ODB layer opening 164a due to the presence of the second ODB layer 181 over the whole opening.

[0029] Thus for the narrower 1st first ODB layer opening 164a the sidewalls of the second ODB layer 181 remain merged and only the first LOCOS oxidation process is able to oxidize the

exposed silicon. This thinner oxide is used to form the LOCOS oxide for the trench capacitor 350a. For the wider 2nd first ODB layer opening 164b, the sidewalls are distinct (as shown as spacers 182a in FIG. 3D), so that the second LOCOS oxidation adds LOCOS 2 which thickens the LOCOS layer in the middle of the 2nd first ODB layer opening 164b for trench capacitor 350b. The LOCOS oxide will be tapered under the spacers 182a, which is equivalent to a bird's beak region that is controlled by the spacer thickness. This thicker LOCOS oxide is used to form the trench capacitor 350b.

[0030] This completes the oxide thickness so that the LOCOS oxide is thicker for the trench capacitor 350b as compared to the LOCOS oxide for the trench capacitor 350a. FIG. 3G shows results after removing the first ODB layer 160 and the second ODB layer 181 and then forming a patterned top plate 112 that can comprise polysilicon over the LOCOS oxides for the trench capacitors 350a and 350b.

[0031] FIGS. 4A-4F are cross-sectional diagrams showing processing progression for another example method of forming an IC having including a first planar capacitor shown as 450a and a second trench capacitor shown as 450b having different LOCOS thicknesses, according to an example. FIG. 4A shows results after forming a relatively narrower 1st first ODB layer opening 164a for the first trench capacitor and a relatively wider 2nd first ODB layer opening 164b for the second trench capacitor 164b in a first ODB layer 160 that is on a pad oxide layer 158 layer that is on a substrate 102 having a semiconductor surface layer 106. This process generally comprises using a photoresist patterned etch mask and then etching the first ODB layer 160 to form the 1st and 2nd first ODB layer openings 164a, 164b.

[0032] FIG. 4B shows results after growing a first LOCOS oxide layer 210, with an example thickness between 200 and 1,000A. The characteristic LOCOS oxidation bird's beak is shown. FIG. 4C shows results after depositing a second ODB layer 181, then depositing a sacrificial sidewall film 182 on the second ODB layer 181 that functions as a sacrificial sidewall layer, then maskless etching of the sacrificial sidewall film 182 and the second ODB layer 181. In the 2nd first ODB layer opening 164b associated with the second trench capacitor 450b as it is relatively wider, etching of the sacrificial sidewall film 182 forms the spacers 182a shown which enables the maskless etching to etch the second ODB layer 181 away from the edges in the 2nd first ODB layer opening 164b to form spacers 181a because the second ODB layer 181 is not protected there by the sacrificial sidewall film 182. Sidewall spacers are not shown in the 1st first ODB

layer opening 164a associated with the first trench capacitor 450a as it is narrower so that after the maskless etching there is as a result the sacrificial sidewall film 182 on the second ODB layer 181 over the full area of the 1st first ODB layer opening 164a.

[0033] FIG. 4D shows results after stripping the sacrificial sidewall film 182 in the 1st first ODB layer opening 164a for the first trench capacitor 450a and the spacers 182a in the 2nd first ODB layer opening 164b for the second trench capacitor 450b and then silicon etching in the exposed semiconductor surface layer 106 in the 2nd first ODB layer opening 164b, where the second ODB layer 181 extending over the entire 1st first ODB layer opening 164a for the first trench capacitor 450a prevents any etching of the semiconductor surface layer 106. The silicon etch depth for the second trench capacitor 450b can be 100A to 30 μm, with an example silicon etch depth being between 500A and 2 μm.

[0034] FIG. 4E shows results after growing a second LOCOS oxide layer resulting in an a LOCOS portion shown as LOCOS 2 above and below the first LOCOS oxide layer 210, generally being 500 to 1,500A of LOCOS oxide at the center of the wider 2nd first ODB layer opening 164b for the second trench capacitor 450b, with no LOCOS 2 shown grown in the narrower 1st first ODB layer opening 164a for the first trench capacitor 450a due to the presence of the second ODB layer 181 over the whole opening.

[0035] Thus for the narrower 1st first ODB layer opening 164a for the first trench capacitor 450a the sidewalls of the second ODB layer 181 remain merged and only the first LOCOS oxidation process is able to oxidize the exposed silicon. This thinner oxide is used to form the oxide for the first trench capacitor 450a. For the wider 2nd first ODB layer opening 164b for the second trench capacitor 450b, the sidewalls are distinct so the second LOCOS oxidation can grow in the middle of the 2nd first ODB layer opening 164b. The oxide will be tapered under the spacers 182a, which is equivalent to a bird's beak region that is controlled by the spacer thickness. This thicker oxide is used to form the trench capacitor 450b. FIG. 4E shows results after results after removal of the sacrificial sidewall film 182 including spacers 182a. FIG. 4F shows results after removing the first ODB layer 160 and the second ODB layer 181 and spacers 181a, and then forming a patterned top plate 112 that can comprise polysilicon over the LOCOS oxide for the trench capacitors 450a, 450b.

[0036] Described below is front-end-of-the-line (FEOL) MOS processing to complete formation of the capacitors comprising forming a top plate and contacts. A patterned layer of top

plate material shown as 112 in FIG. 1 is formed over the layers of LOCOS oxide 110a, 110b. The top plate 112 may include, for example, polycrystalline silicon, referred to herein as polysilicon, possibly doped with n-type dopants. Polysilicon as the layer of top plate 112 may be, for example, 300 nanometers to 800 nanometers thick.

[0037] Disclosed aspects can be used to form semiconductor die that may be integrated into a variety of assembly flows to form a variety of different devices and related products. The semiconductor die may include various elements therein and/or layers thereon, including barrier layers, dielectric layers, device structures, active elements and passive elements including source regions, drain regions, bit lines, bases, emitters, collectors, conductive lines, conductive vias, etc. Moreover, the semiconductor die can be formed from a variety of processes including bipolar, Insulated Gate Bipolar Transistor (IGBT), CMOS, BiCMOS and MEMS.

[0038] Those skilled in the art to which this description relates will appreciate that many other aspects are possible within the scope of the claimed invention, and further additions, deletions, substitutions and modifications may be made to the described aspects without departing from the scope of this description.

CLAIMS

What is claimed is:

1. A method of fabricating an integrated circuit (IC), comprising:

depositing a first oxygen diffusion barrier (ODB) layer on a pad oxide layer on a semiconductor surface layer on a substrate;

patterning and then etching the first ODB layer to form a 1st first ODB layer opening and at least a 2nd first ODB layer opening, wherein a width of the 2nd first ODB layer opening is larger than a width of the 1st first ODB layer opening;

growing a first LOCal Oxidation of Silicon (LOCOS) layer in the 1st first ODB layer opening and in the 2nd first ODB layer opening;

depositing a second ODB layer and then depositing a sacrificial sidewall film on the second ODB layer;

etching the sacrificial sidewall film to form a spacer in the 2nd first ODB layer opening but not in the 1st first ODB layer opening which remains blocked by the sacrificial sidewall film and removing the second ODB layer where not protected by the sacrificial sidewall film;

stripping the sacrificial sidewall film;

growing a second LOCOS layer in the 2nd first ODB layer opening but not in the 1st first ODB layer opening;

removing the first and the second ODB layer, and

forming a top plate over the first opening to complete a first capacitor and over the second opening to complete a second capacitor.

2. The method of claim 1, wherein the first capacitor and the second capacitor both comprise planar capacitors.

3. The method of claim 1, further comprising after the patterning and then etching the first ODB layer and before the growing the first LOCOS layer, etching the semiconductor surface layer in the first opening and in the second opening to a predetermined depth, wherein the first capacitor and the second capacitor both comprise trench capacitors.

4. The method of claim 1, further comprising after the stripping the sacrificial sidewall film and before the growing the second LOCOS layer, etching the semiconductor surface layer in the second opening to a predetermined depth, wherein the first capacitor is a planar capacitor and the second capacitor is a trench capacitor.

5. The method of claim 1, wherein a thickness of the first LOCOS layer is 200 to 1,000 A.

6. The method of claim 1, wherein the first ODB layer and the second ODB layer both comprise silicon nitride.

7. The method of claim 1, wherein the width of the 2nd first ODB layer opening is at least 0.05 µm greater than the width of the 1st first ODB layer opening.

8. The method of claim 1, wherein the first ODB layer comprises silicon nitride and is 300 to 2,000A thick.

9. The method of claim 1, wherein the top plate comprises polysilicon.

10. An integrated circuit (IC), comprising:

a first capacitor, a second capacitor, and functional circuitry configured together with the capacitors for realizing at least one circuit function in a semiconductor surface layer on a substrate;

the capacitors comprising:

a top plate over a LOCal Oxidation of Silicon (LOCOS) oxide layer, wherein a thickness of the LOCOS oxide layer for the second capacitor is thicker than a thickness of the LOCOS oxide layer for the first capacitor, and

a contact for the top plate and a contact for a bottom plate for the first and second capacitors.

11. The IC of claim 10, wherein the thickness for the LOCOS oxide layer for the second capacitor is at least 500 A thicker than the thickness for the LOCOS oxide layer for the first capacitor.

12. The IC of claim 10, wherein the first capacitor and the second capacitor both comprise planar capacitors.

13. The IC of claim 10, wherein the first capacitor and the second capacitor both comprise trench capacitors.

14. The IC of claim 13, wherein the semiconductor surface layer is recessed for the second capacitor as compared to the first capacitor.

15. The IC of claim 10, wherein a width of an opening for the LOCOS oxide layer for the second capacitor is at least 0.05 µm greater than a width of an opening for the LOCOS oxide layer for the first capacitor.

16. The IC of claim 10, wherein the top plate comprises polysilicon.

17. The IC of claim 10, wherein the semiconductor surface layer comprises an epitaxial layer.

18. The IC of claim 10, wherein the contacts for the top plate and for the bottom plate for the first and the second capacitors are all top side contacts.

123c 159 158 106 122c 180 100 IC

123b 122b 150b TRENCH CAP 112 122a 123b 110b 102 123b 122b

123b 122b 112 122a 110a 123a 110a 112 123b 122b 150a TRENCH CAP

FIG. 1

160 158 180b 164b 106 102 160 180a 164a

FIG. 2A

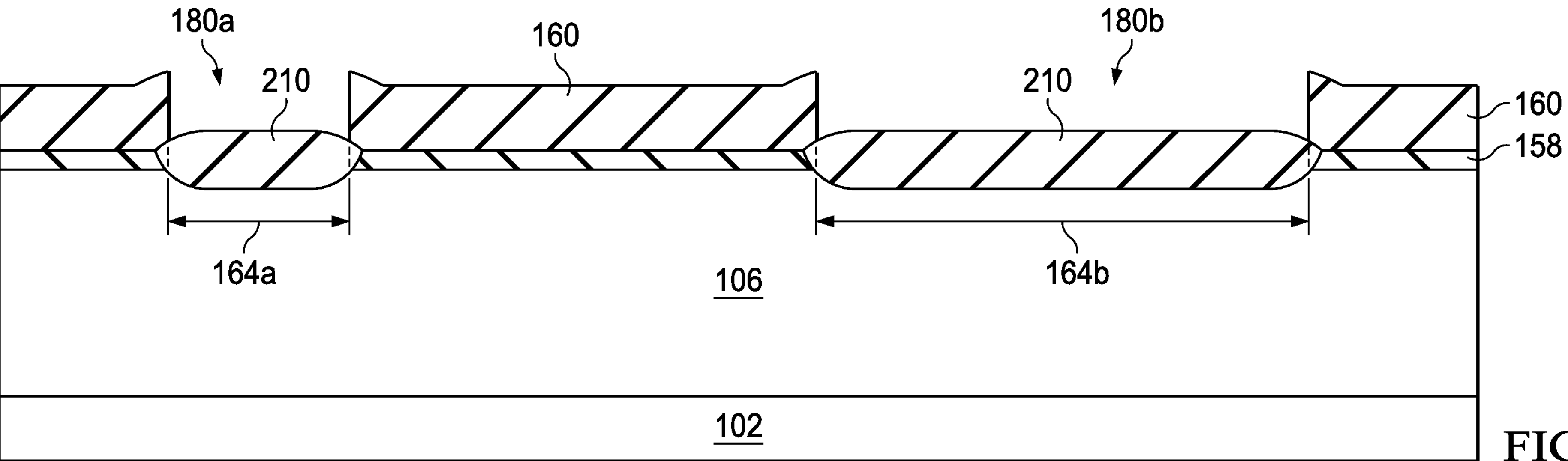

FIG. 2B

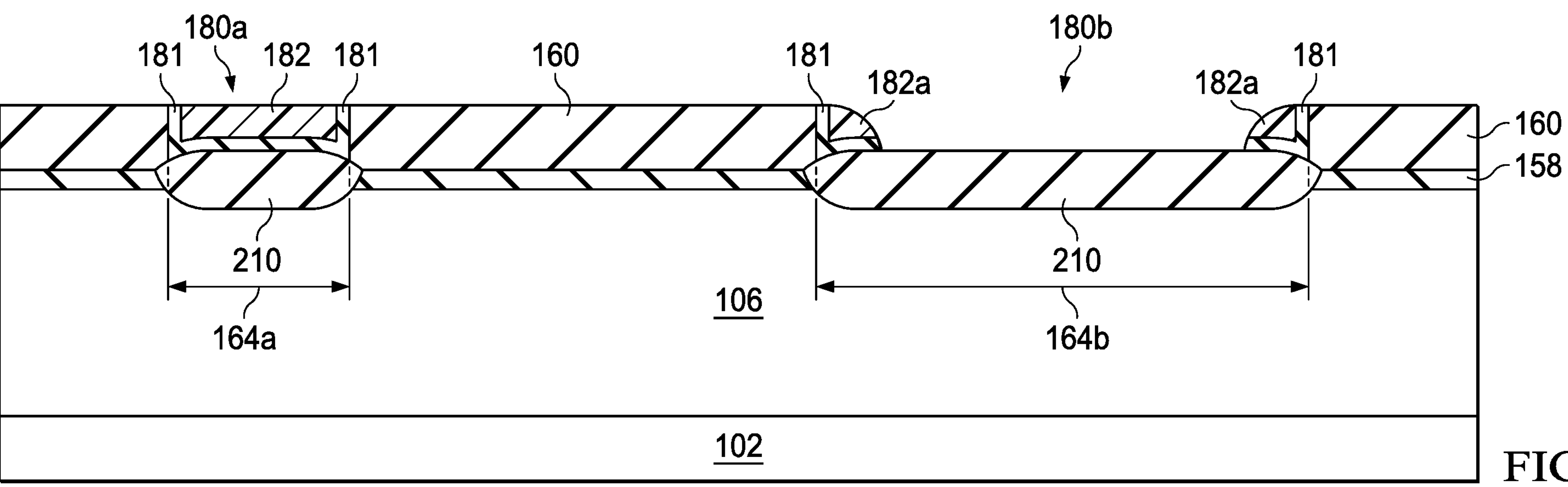

FIG. 2C

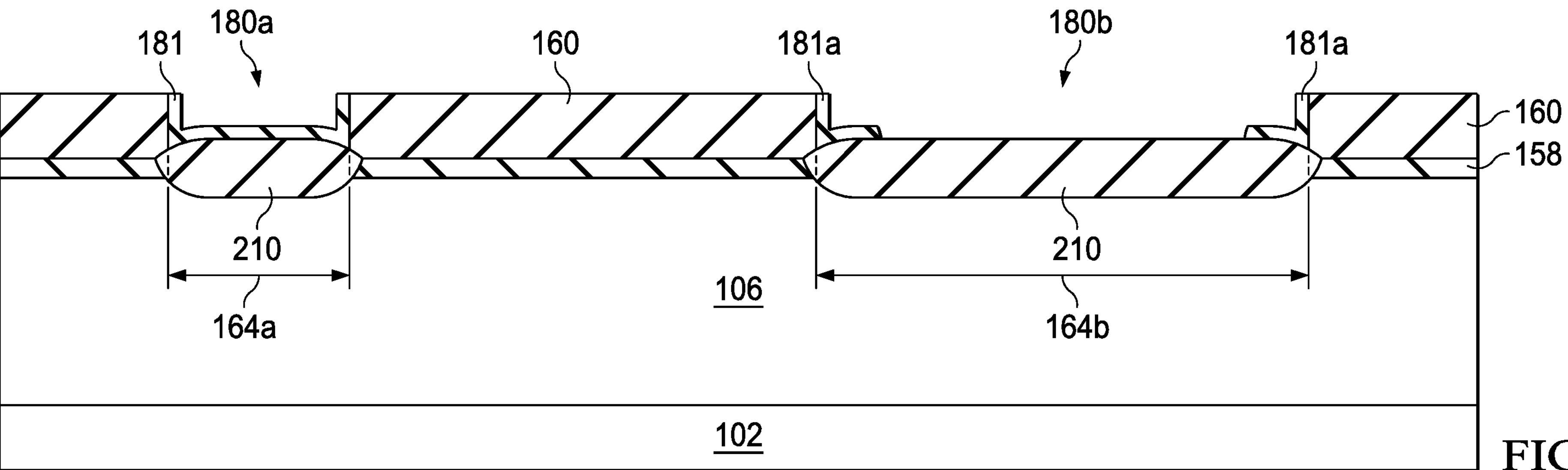

FIG. 2D

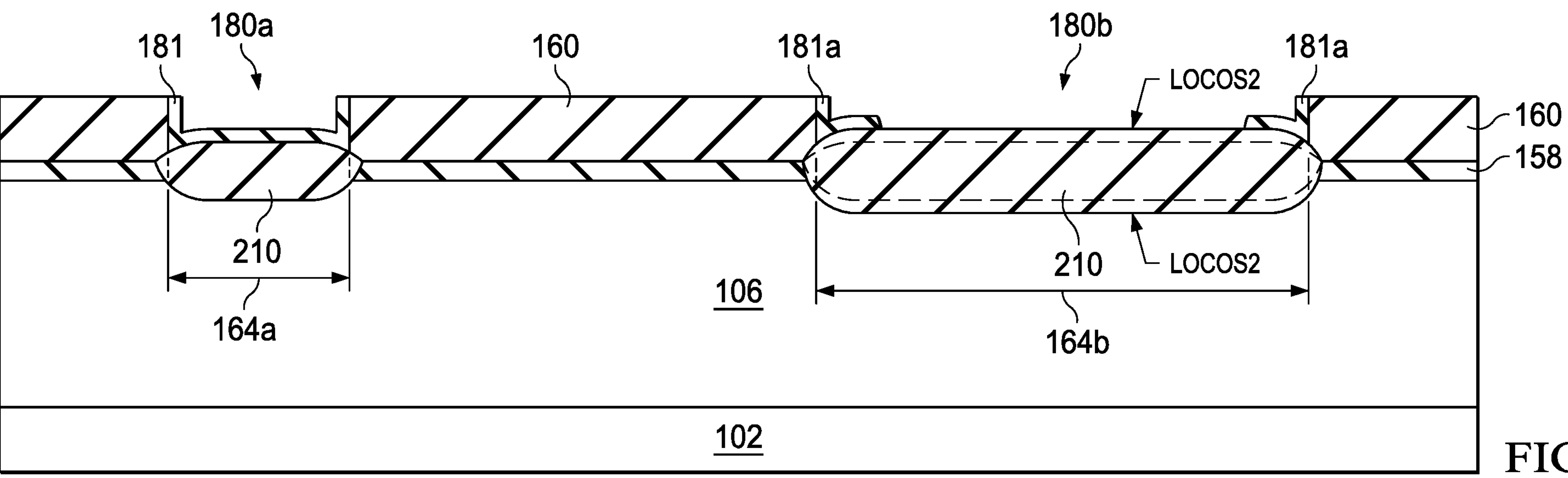

FIG. 2E

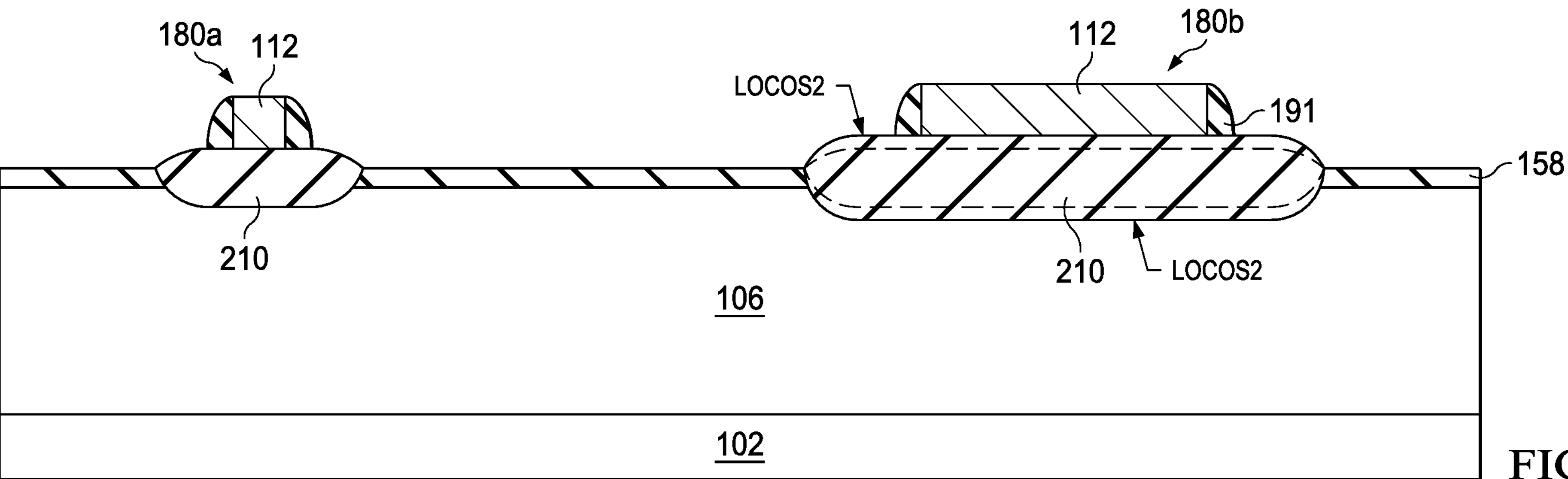

FIG. 2F

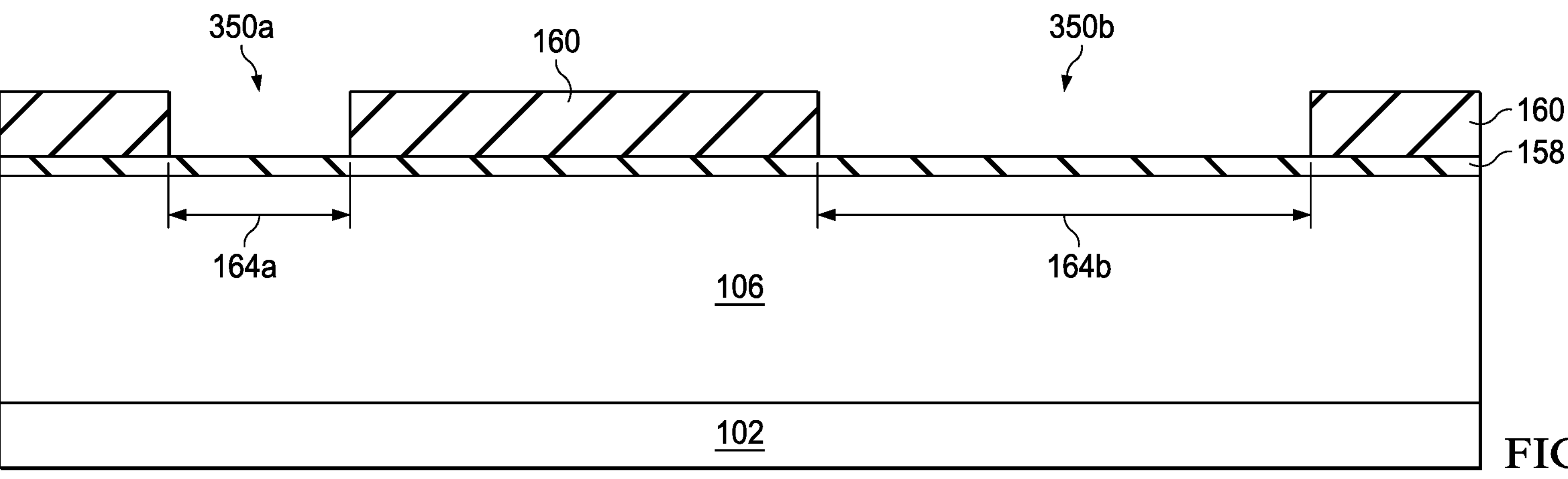

FIG. 3A

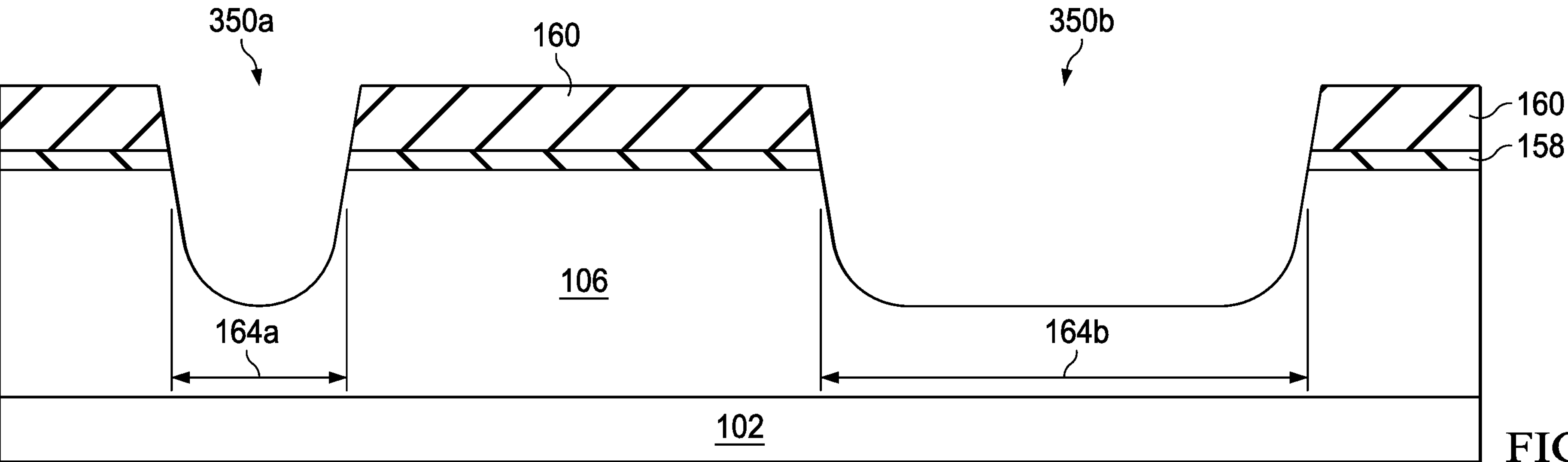

FIG. 3B

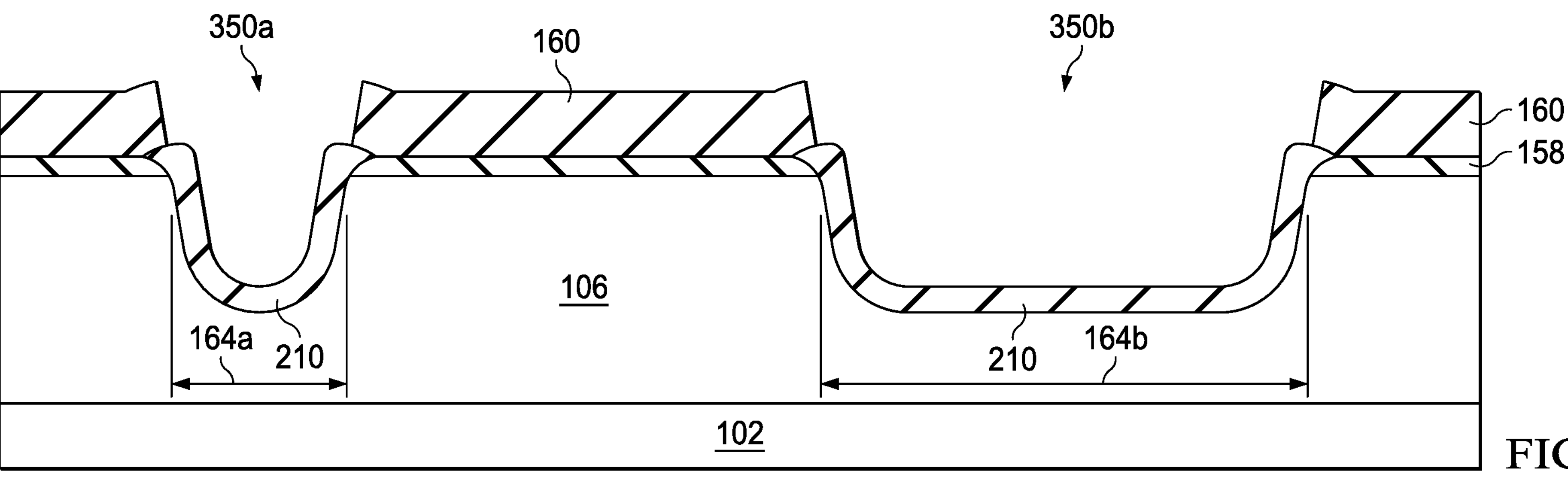

FIG. 3C

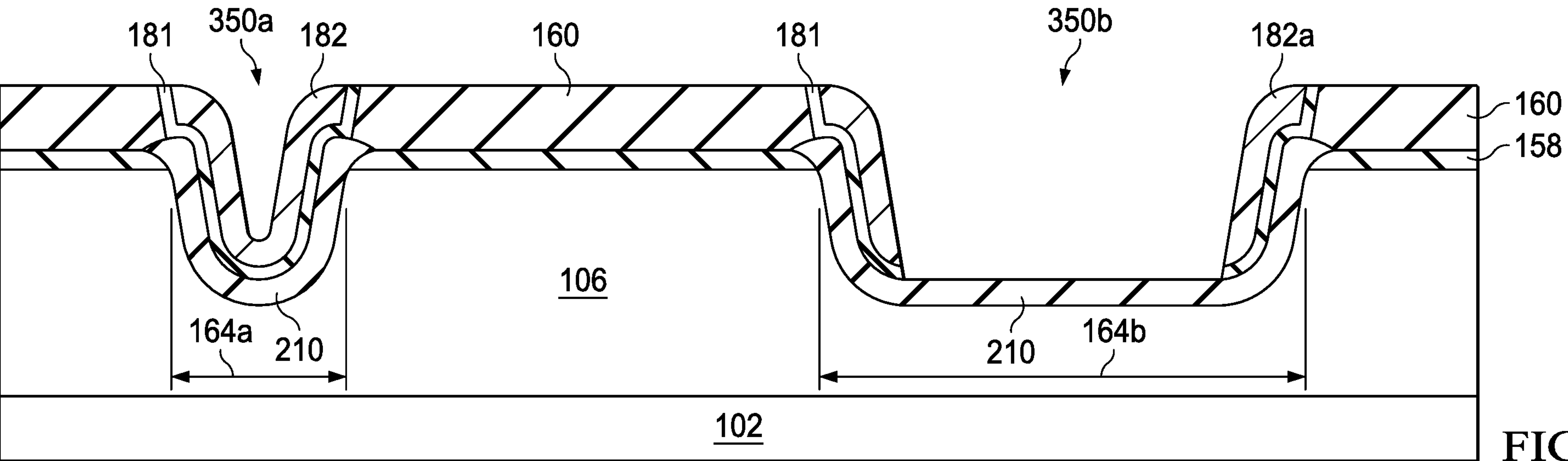

FIG. 3D

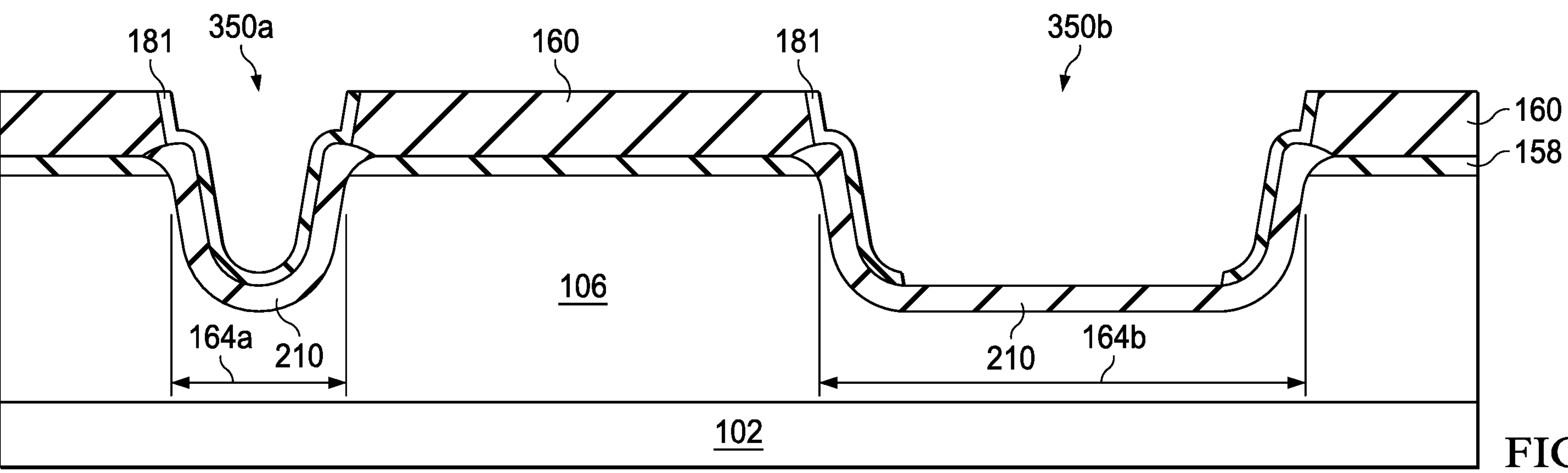

FIG. 3E

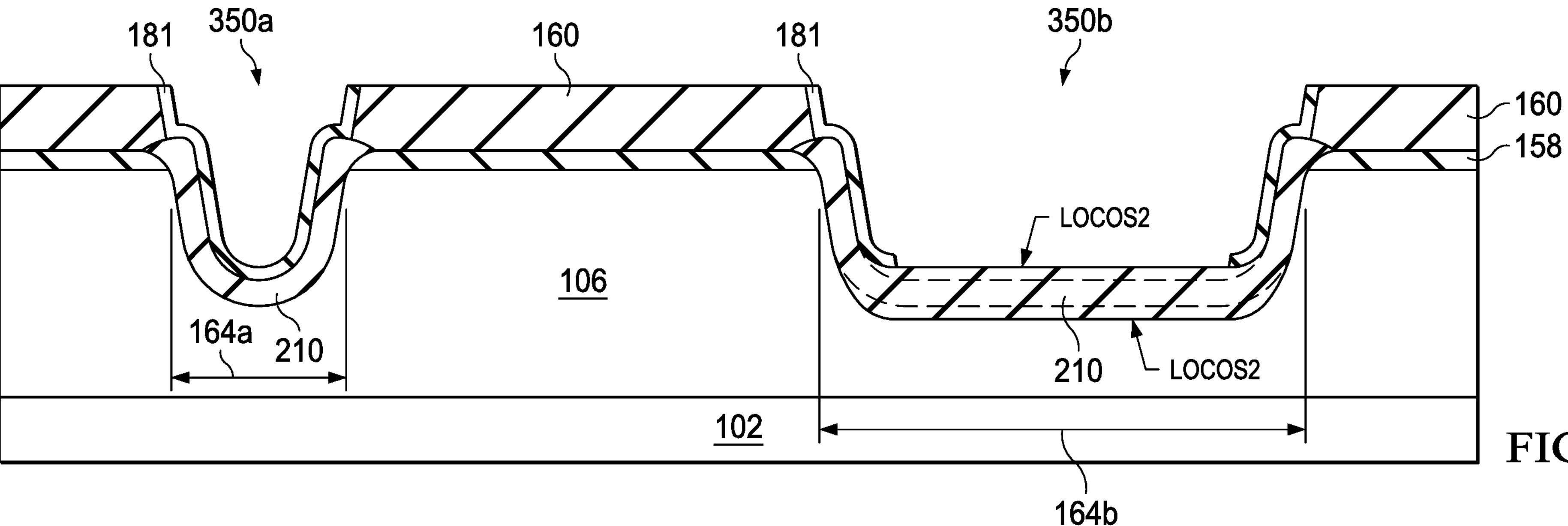

FIG. 3F

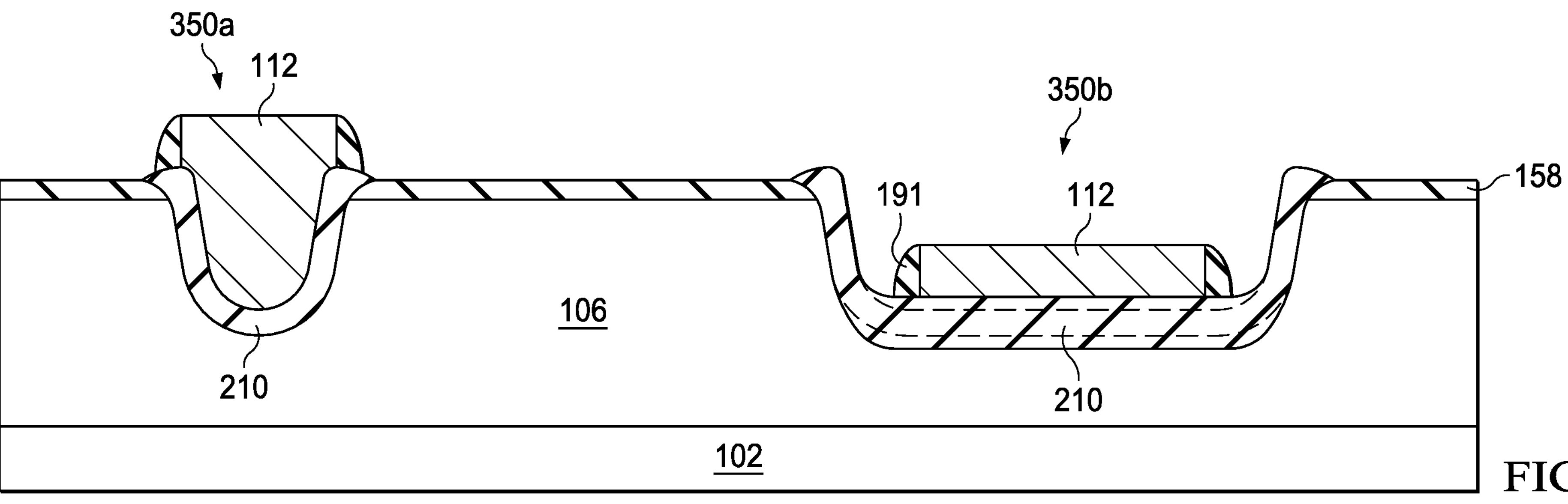

FIG. 3G

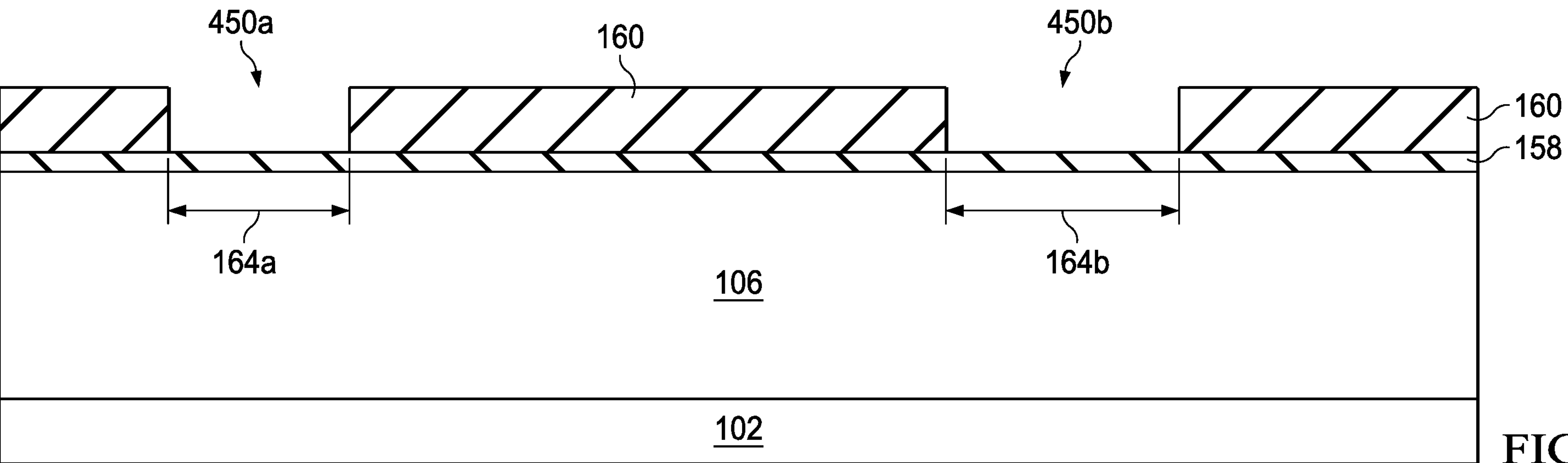

FIG. 4A

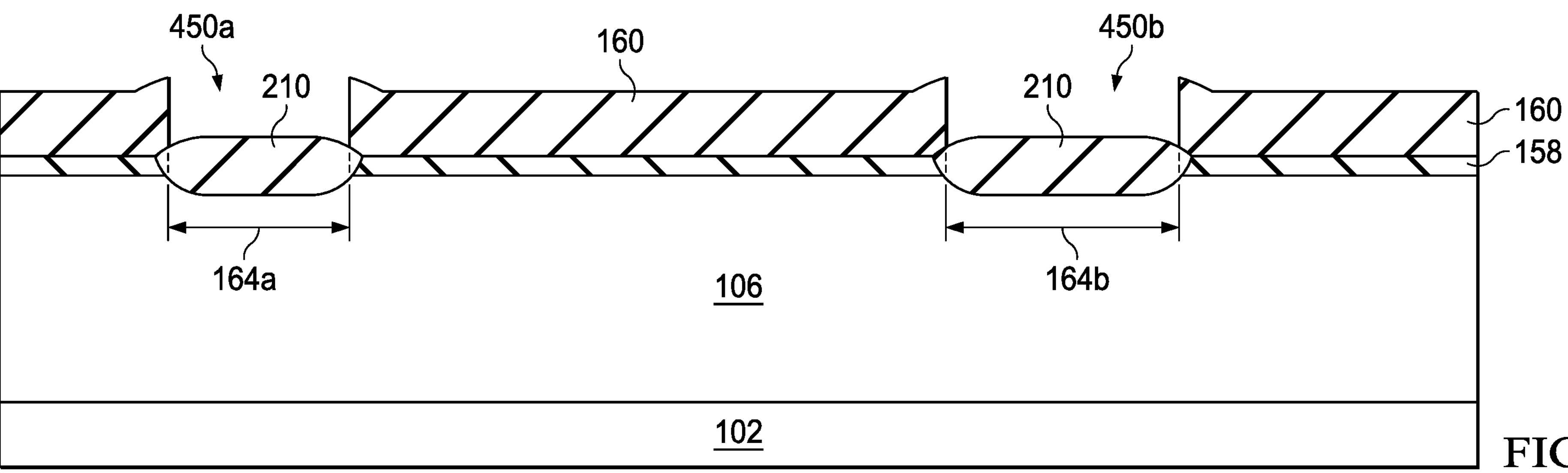

FIG. 4B

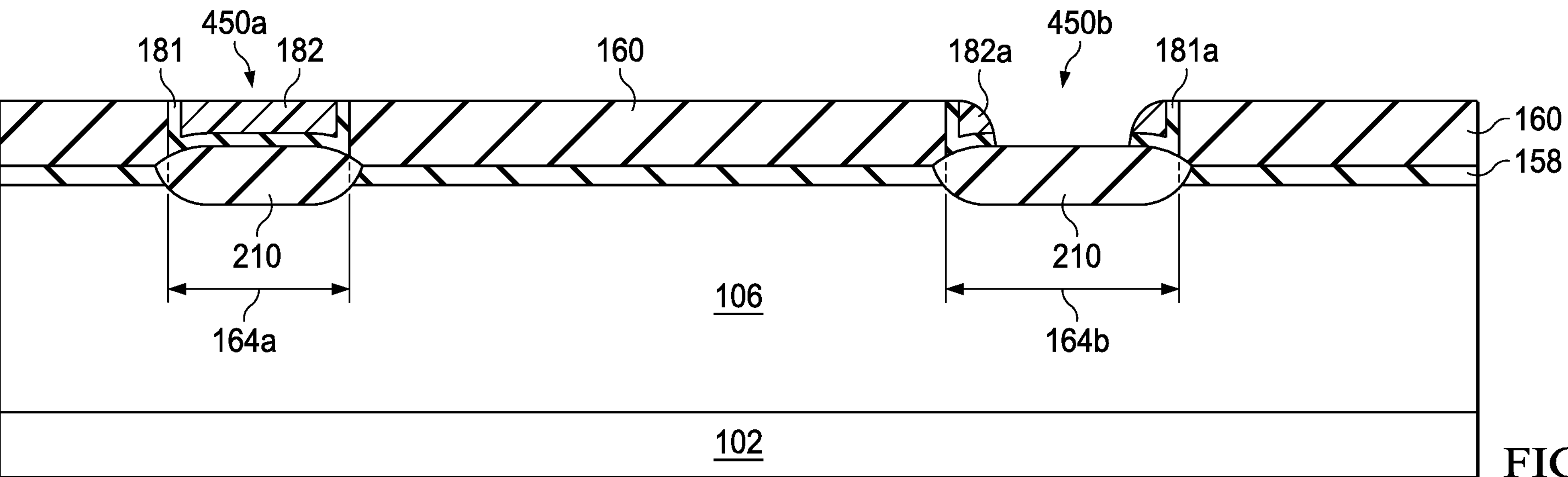

FIG. 4C

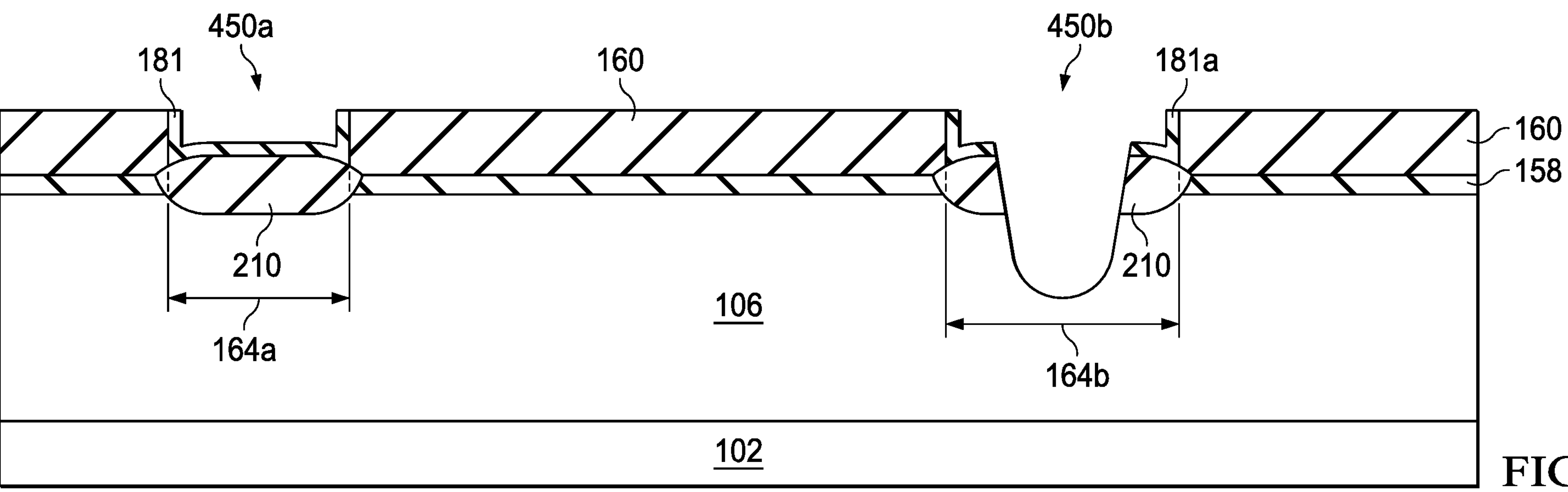

FIG. 4D

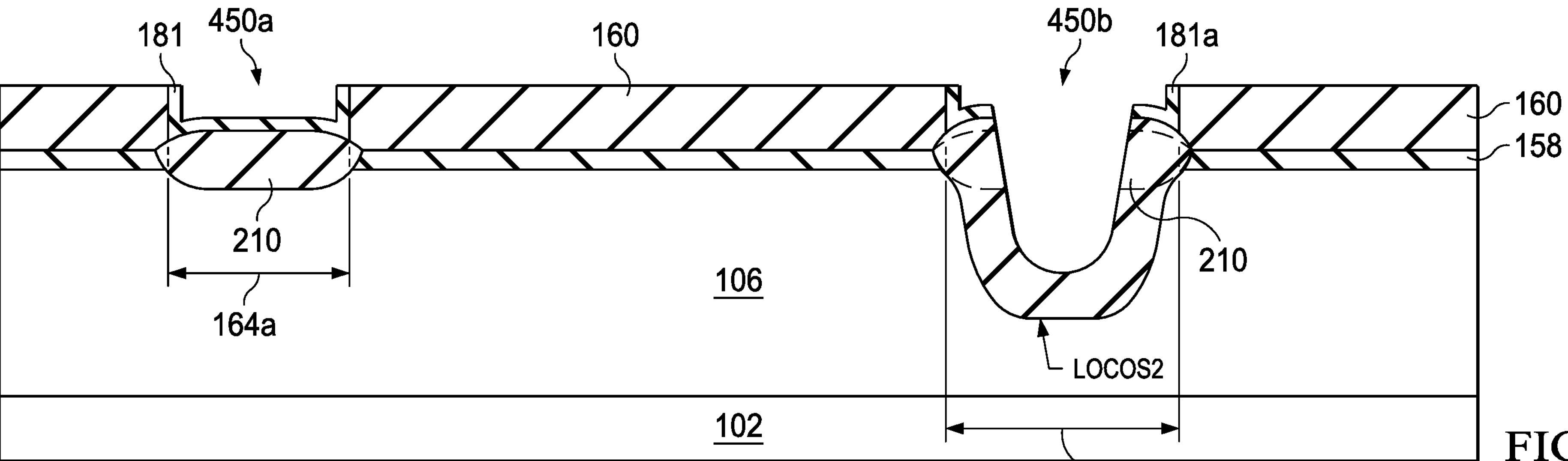

FIG. 4E

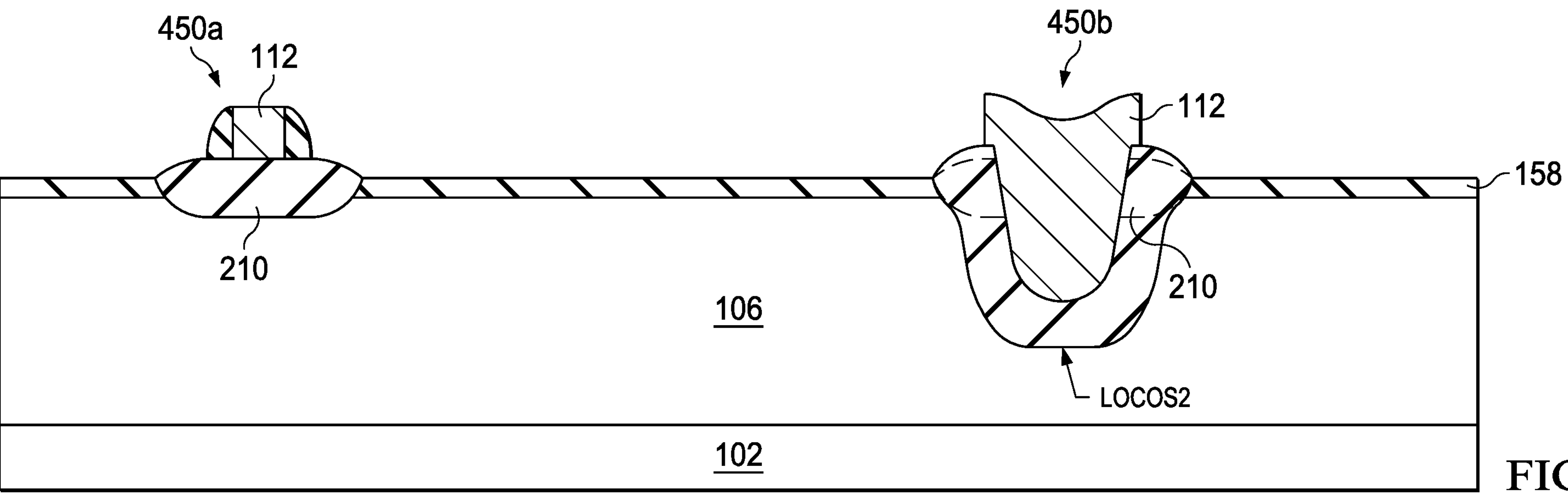

FIG. 4F

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US 2019/055217

A. CLASSIFICATION OF SUBJECT MATTER

H01L 27/04 *(2006.01)*

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 21/00, 21/70, 21/98, 27/00, 27/02, 27/04, 29/00, 29/66, 29/86, 29/92

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

PatSearch, Espacenet, Patentscope, Google.ru

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2003/0136988 A1 (MICRON TECHNOLOGY, INC.) 24.07.2003	1-18
A	US 2012/0256177 A1 (SEMICONDUCTER ENERGY LABORATORY CO., LTD.) 11.10.2012	1-18
A	WO 2017/137864 A1 (SEMICONDUCTER ENERGY LABORATORY CO., LTD.) 17.08.2017	1-18

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:

- "A" document defining the general state of the art which is not considered to be of particular relevance
- "E" earlier document but published on or after the international filing date
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- "O" document referring to an oral disclosure, use, exhibition or other means
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- "T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
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- "Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
- "&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
30 December 2019 (30.12.2019)	16 January 2020 (16.01.2020)

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