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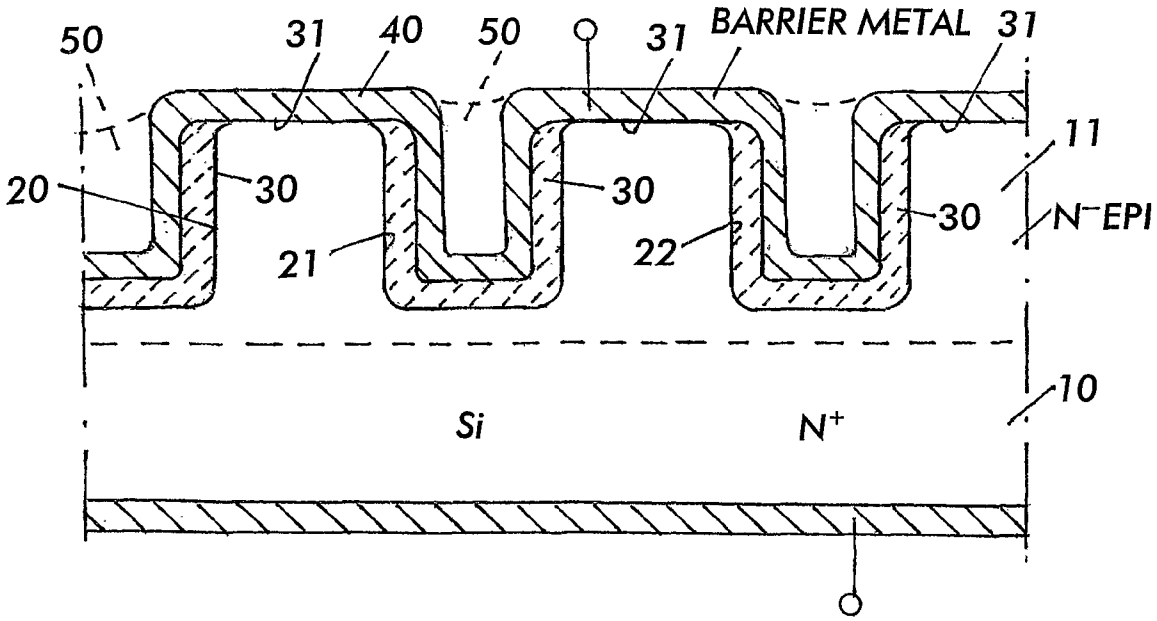
(54) **Title:** TRENCH SCHOTTKY DEVICE WITH SINGLE BARRIER



(57) **Abstract:** A process for forming a trench Schottky barrier device includes the forming of an oxide layer within the trenches in the surface of a silicon wafer, and then depositing a full continuous metal barrier layer over the full upper surface of the wafer including the trench interiors and the mesas between trenches with a barrier contact made to the mesas only. Palladium, titanium or any conventional barrier metal can be used.

WO 2007/047713 A2

TRENCH SCHOTTKY DEVICE WITH SINGLE BARRIER

RELATED APPLICATION

[0001] This application is based on and claims the benefit of United States Provisional Application Serial No. 60/727,712, filed on October 18, 2005, entitled TRENCH SCHOTTKY DEVICE WITH SINGLE BARRIER, to which a claim of priority is hereby made and the disclosure of which is incorporated by reference.

FIELD OF THE INVENTION

[0002] This invention relates to semiconductor devices and more specifically relates to trench Schottky devices and processes for their manufacture.

BACKGROUND OF THE INVENTION

[0003] Trench Schottky devices are well known and are shown, for example, in U.S. Patent 6,855,593 entitled Trench Schottky Barrier Diode in the names of Andoh and Chiola (IR-1663). Planar Schottky devices are also well known and are shown in U.S. Patent 4,398,344 in the name of Gould (IR-659).

[0004] The manufacture of the trench Schottky is complicated by the need for extra process steps required to ensure that the barrier metal on the tops of the mesas formed by the trenches is removed from the trench walls.

[0005] It would be desirable to provide such a process but having fewer process steps without affecting the final device characteristics.

BRIEF DESCRIPTION OF THE INVENTION

[0006] In accordance with the invention, spaced trenches are formed in a silicon substrate and an oxide layer is thermally grown on the full upper surface and on the trench side walls. The oxide layer is then removed from the tops of the

mesas, and a barrier metal which adheres to both oxide and silicon is then deposited, as by sputtering on the full upper surface of the wafer (or die), adhering to the exposed silicon surface at the tops of the mesas, forming the desired Schottky barrier, and adhering to the oxide layer on the walls and bottom of the trenches. Metals which can be used are, for example, titanium and palladium. The process used to form the barrier metal may be that described in Gould patent 4,398,344 previously referred.

[0007] The dimensions used for the trench depth and width and for the mesa width may be those described in U.S. Patent 6,855,593 described above.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] Figure 1 is a cross-section of a small portion of a wafer (or die) after the formation of parallel trenches, the oxidation of the upper surface of the wafer and the removal of the oxide from the tops of the mesas.

[0009] Figure 2 shows the wafer of Figure 1 after the deposition of a barrier metal over the entire wafer surface, but in contact with only the tops of the mesas.

DETAILED DESCRIPTION OF THE DRAWINGS

[0010] Referring first to Figure 1, there is shown a silicon wafer (or die) 10 which is of monocrystalline silicon of the N^+ conductivity type, and which may have an upper epitaxially formed surface layer 11. The top of the wafer receives a plurality of identical trenches 20, 21, 22 in the epitaxially formed layer 11.

[0011] In an early process step, the full upper surface of the wafer 10 has a thermal oxide 30 grown thereon, over the full interior of each trench and over the mesas between the trenches. The oxide 30 is then suitably removed from the tops 31 of the mesas. Alternatively, the masks used during the trench etch process may be left in place to block the growth of oxide on the mesas.

[0012] The wafer is then suitably cleaned, and a Schottky-forming barrier metal 40 (Figure 2) is then applied, as by sputtering over the fully unmasked active surface of the wafer. The barrier metal chosen is one which will adhere to silicon to form the Schottky barrier at the tops 31 of the mesas, and which will also adhere to the oxide 30 within the trenches. Thus, the metal 40 is insulated from the interior walls and bottoms of trenches 20, 21 and 22.

[0013] Barrier metals which can be used are, for example, titanium and palladium; and the like are described in patent 4,398,344 referred to above.

[0014] Thereafter, the trench interiors can be filled with any suitable filler 50 to planarize the upper surface of the device.

[0015] Top and bottom electrodes can then be attached to the top and bottom respectively of the wafer. Bottom electrode 50 is shown attached to the bottom of N^+ wafer 10.

[0016] Although the present invention has been described in relation to particular embodiments thereof, many other variations and modifications and other uses will become apparent to those skilled in the art. It is preferred, therefore, that the present invention be limited not by the specific disclosure herein.

What is claimed is:

1. The process for forming a trench Schottky device comprising the steps of forming parallel trenches into the upper surface of a semiconductor wafer; forming an oxide layer over the inner walls of each of said trenches and leaving the tops of the mesas between said trenches free of insulation; applying a Schottky barrier layer metal over the full exposed upper surface of said wafer and over and in contact with said mesas and over said oxide layer in said trenches and thereby being insulated from said trench walls, whereby said single barrier layer metal defines a Schottky barrier to said silicon.

2. The process of claims 1, wherein the upper portion of said wafer is an epitaxially formed layer of silicon; said trenches being formed in said epitaxially formed layer.

3. The process of claim 1, wherein said oxide is formed over the full exposed surface at the top of said wafers and is subsequently removed from said mesas.

4. The process of claim 1, where said barrier forming metal is one of titanium or palladium.

5. The process of claim 2, where said barrier forming metal is one of titanium or palladium.

6. The process of claim 3, where said barrier forming metal is one of titanium or palladium.

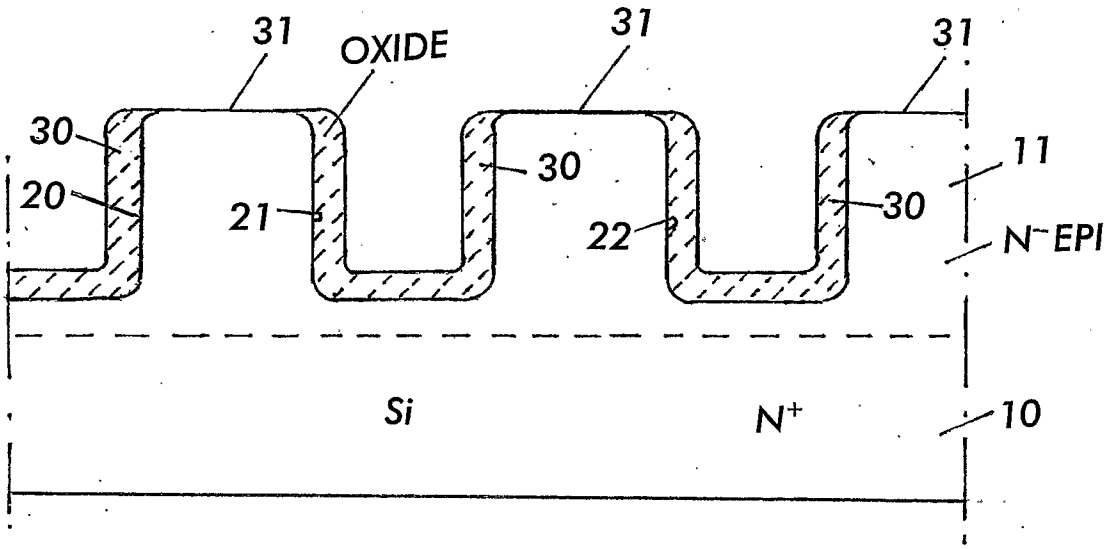

31
OXIDE
31
31
30
20
21
30
22
30
11
N⁻EPI
Si
N⁺
10

FIG. 1

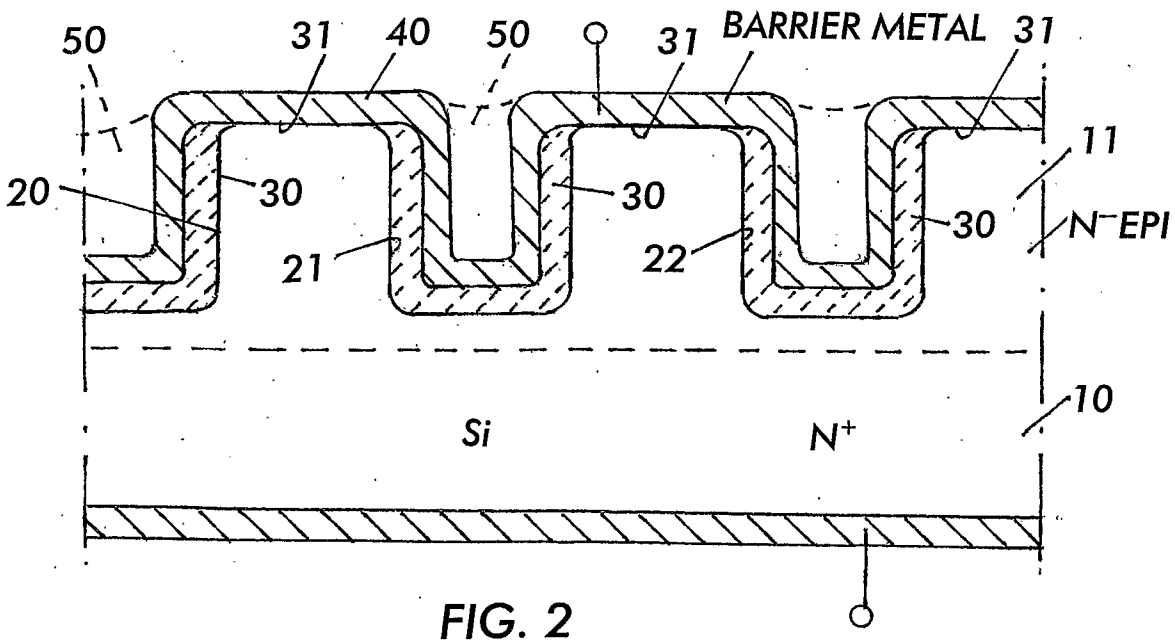

50
31
40
50
31
BARRIER METAL
31
11
20
30
30
30
N⁻EPI
21
22
Si
N⁺
10

FIG. 2