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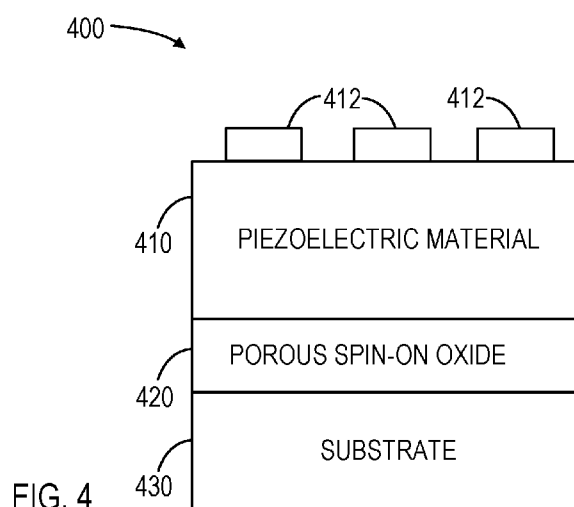
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(54) Title: DEVICES INCLUDING ACOUSTIC DEVICES ISOLATED USING POROUS SPIN-ON DIELECTRICS, AND RELATED METHODS



(57) Abstract: Electronic devices, computing devices, and related methods are disclosed. An electronic device includes an acoustic device on or in a semiconductor structure, and an acoustic isolator including a porous spin-on (PSO) dielectric configured to acoustically isolate the acoustic device from the semiconductor structure. A method includes disposing an acoustic device onto or into a semiconductor structure, spinning a PSO dielectric onto or into the semiconductor structure, and curing the PSO dielectric.



DEVICES INCLUDING ACOUSTIC DEVICES ISOLATED USING POROUS SPIN-ON DIELECTRICS, AND RELATED METHODS

Technical Field

[0001] This disclosure relates generally to acoustic isolation of acoustic devices, and more specifically to acoustically isolating resonator devices with porous spin-on dielectrics (e.g., porous spin-on oxides).

Background

[0002] Radio Frequency (RF) filters, duplexers, oscillators, and mechanical sensors are examples of devices that sometimes include acoustic resonators (e.g., Film Bulk Acoustic Resonators (FBARs), Contour Mode Resonators (CMRs), Surface Acoustic Wave (SAW) resonators, etc.). In these devices, acoustic isolation is used to prevent energy from leaking in and out of acoustic resonators, which may decrease system efficiency and performance, or result in interference between nearby devices.

Brief Description of the Drawings

[0003] FIG. 1 is a simplified block diagram of an electronic device, according to some embodiments.

[0004] FIG. 2 is a simplified cross-sectional view of an example of the electronic device of FIG. 1, according to some embodiments.

[0005] FIG. 3 is a simplified cross-sectional view of another example of the electronic device of FIG. 1, according to some embodiments.

[0006] FIG. 4 is a simplified cross-sectional view of yet another example of the electronic device of FIG. 1, according to some embodiments.

[0007] FIG. 5 is a simplified cross-sectional view of a further example of the electronic device of FIG. 1, according to some embodiments.

[0008] FIG. 6 is a simplified cross-sectional view of yet another example of the electronic device of FIG. 1, according to some embodiments.

[0009] FIG. 7 is a simplified cross-sectional view of a further example of the electronic device of FIG. 1, according to some embodiments.

[0010] FIG. 8 is a simplified flowchart illustrating a method of manufacturing an electronic device, according to some embodiments.

[0011] FIG. 9 is an interposer according to some embodiments.

[0012] FIG. 10 is a computing device according to some embodiments.

Detailed Description of Preferred Embodiments

[0013] Disclosed herein are electronic devices, computing devices, and related methods for acoustic devices that are acoustically isolated using porous spin-on dielectrics. In the following description, various aspects of the illustrative implementations will be described using terms commonly employed by those skilled in the art. It will be apparent, however, to those skilled in the art that embodiments disclosed herein may be practiced with only some of the described aspects. For purposes of explanation, specific numbers, materials, and configurations are set forth in order to provide a thorough understanding of the illustrative embodiments. It will be apparent, however, to one skilled in the art that embodiments disclosed herein may be practiced without the specific details disclosed herein. In some embodiments disclosed herein, well-known features are omitted or simplified in order not to obscure the illustrative implementations.

[0014] Various operations will be described as multiple discrete operations, in turn, in a manner that is helpful in understanding the present disclosure. The order, however, of description should not be construed to imply that these operations are necessarily order dependent. In particular, these operations need not be performed in the order of presentation.

[0015] The terms “over,” “under,” “between,” and “on,” as used herein, refer to a relative position of one material (e.g., a material layer) or component with respect to other materials or components. For example, one material disposed over or under another material may be directly in contact with the other material or may have one or more intervening materials in between. Moreover, one material disposed between two materials may be directly in contact with the two materials or may have one or more intervening materials. In contrast, a first material “on” a second material is in direct contact with that second material. Similarly, unless explicitly stated otherwise, one feature disposed between two features may be in direct contact with the adjacent features or may have one or more intervening materials or features.

[0016] Embodiments disclosed herein may be formed or carried out on a substrate, such as a semiconductor substrate. In one implementation, the semiconductor substrate may be a crystalline substrate formed using a bulk silicon or a silicon-on-insulator substructure. In other implementations, the semiconductor substrate may be formed using alternative materials, which may or may not be combined with silicon, that include but are not limited to germanium, indium

antimonide, lead telluride, indium arsenide, indium phosphide, gallium arsenide, indium gallium arsenide, gallium antimonide, or other combinations of group III-V or group IV materials. Although a few examples of materials from which the substrate may be formed are described here, any material that may serve as a foundation upon which a semiconductor device may be built falls within the spirit and scope of the present disclosure.

[0017] Low acoustic impedance materials have versatile use in acoustic devices as isolation or reflection materials (e.g., layers). Polymer is one example of a class of materials that have low acoustic impedance values. Polymers, however, generally have low thermal budgets, which limit their use in practical semiconductor device fabrication because high-temperature curing or annealing operations are frequently used in semiconductor manufacturing. As a result, silicon oxide may be used as a low acoustic impedance material in semiconductor devices because of its robustness and fabrication compatibility.

[0018] Silicon oxide has a relatively low acoustic impedance value associated therewith. This acoustic impedance value, however, may be decreased if pores are introduced into the silicon oxide. Attempts to dispose porous silicon oxide using Chemical Vapor Deposition (CVD) and sputtering have resulted in limited porosity, high material stress, and rough surfaces.

[0019] Disclosed herein are low acoustic impedance materials including porous spin-on dielectrics (e.g., porous spin-on oxides such as porous spin-on silicon oxide or porous spin-on silicon dioxide formed using spin-on techniques). These low acoustic impedance materials may be disposed between an acoustic device on or in a semiconductor structure (e.g., a semiconductor substrate, adjacent structures such as rigid structures or other acoustic devices, etc.) and the semiconductor structure.

[0020] As used herein, the terms “porous spin-on dielectric” and “porous spin-on oxide” (or equivalently “PSO dielectric” and “PSO oxide”) refer to porous dielectrics and oxides that have been disposed on or in a device using spin-on techniques. Accordingly, PSO dielectric and PSO oxide materials manifest structural features that are unique to porous spin-on materials. In some embodiments, PSO dielectric or oxide may include crosslinked cyclic carbosilanes wherein a cyclic carbosilane has a ring structure including carbon and silicon. In such embodiments, the PSO dielectric may include between 45 and 60 atomic percent carbon (C), between 25 and 35 atomic percent silicon (Si), and between 10 and 20 atomic percent oxygen

(O). Such PSO dielectrics and oxides are disclosed in U.S. Patent 9,070,553 to Michalak et al., issued on June 30, 2015.

[0021] Also, higher porosity (and consequently lower acoustic impedance values) may be achieved in PSO dielectric and PSO oxide materials, as compared to corresponding CVD and sputtered materials (e.g., about 50% porosity or more). Furthermore, pore structures may be created in PSO dielectrics and PSO oxide materials using organic based porogens. Accordingly, a PSO dielectric or oxide may include residuals of such organic based porogens. Also by way of non-limiting example, PSO dielectric and PSO oxide materials may manifest smoother surfaces as compared to corresponding CVD materials (e.g., about one nanometer root mean square (RMS) roughness or less compared to a few nanometers RMS roughness or more for corresponding CVD or sputtered materials in the range of hundreds of nanometers of material thickness). Furthermore, PSO dielectric and PSO oxide materials may manifest less material stress than corresponding sputtered materials. Although spin-on dielectrics may in general be somewhat susceptible to material stress, pores of PSO dielectrics and oxides may manifest reduced stiffness due to the pores, and near zero residual stress is feasible.

[0022] PSO dielectrics and oxides are semiconductor fabrication compatible in high volume manufacturing. The porosity of these PSO dielectrics and oxides can be relatively easily and precisely controlled using precursor chemistry in a range from non-porous to greater than 50% porous. Due to its spinning nature, surfaces of PSO dielectrics and oxides are very smooth, reducing acoustic loss that may result from acoustic scattering due to a relatively rough surface. Another advantage of PSO dielectrics and oxides is that material (e.g., film) thickness may be readily controlled either by spin conditions (e.g., solid contents, spin speed, etc.) or by merely repeating spin-on operations.

[0023] Low acoustic impedance materials may be used in acoustic devices to manipulate acoustic wave propagation characteristics. For example, one application of low acoustic materials is device acoustic isolation from surrounding structures (e.g., semiconductor structures). Such acoustic isolation directly improves device performance.

[0024] FIG. 1 is a simplified block diagram of an electronic device 100, according to some embodiments. The electronic device 100 includes a semiconductor structure 130 (e.g., a semiconductor substrate, a semiconductor device, non-semiconductor

material disposed on or in a semiconductor substrate or device, or combinations thereof), an acoustic isolator 120 on or in the semiconductor structure, and an acoustic device 110 (e.g., an FBAR, a CMR, a SAW resonator, etc.). The acoustic isolator 120 includes a PSO dielectric (e.g., a high porosity spin-on oxide) configured to acoustically isolate the acoustic device 110 from at least a portion of the semiconductor structure 130.

[0025] Although a PSO dielectric may have a relatively low acoustic impedance value, the PSO dielectric may be used as an interface with a material with a relatively high acoustic impedance value to form a high contrast interface between acoustic impedance values. Such high contrast interfaces may result in improved acoustic isolation. Also, in embodiments where an air region may typically be used for acoustically isolating the acoustic device 110, the acoustic isolator 120 may be used in place of the air region, especially where the porosity of the acoustic isolator 120 is relatively high (e.g., greater than 50% porous).

[0026] In some embodiments, the PSO dielectric may be in direct physical contact with an electrode of the acoustic device 110. In some embodiments, the PSO dielectric may be in direct physical contact with a piezoelectric material of the acoustic device 110.

[0027] FIG. 2 is a simplified cross-sectional view of an example of the electronic device 100 of FIG. 1, according to some embodiments. An electronic device 200 includes a semiconductor structure (e.g., a substrate 230), an acoustic device 210 (e.g., an FBAR including a piezoelectric material 214 between electrodes 212, 216) on or in the semiconductor structure, and an acoustic isolator 220. The acoustic isolator 220 includes a Bragg reflector, which includes a periodic structure of low acoustic impedance materials 222 having relatively low acoustic impedance values and high acoustic impedance materials 224 having acoustic impedance values that are higher than those of the low acoustic impedance materials 222.

[0028] Bragg reflectors perform well when the difference between the acoustic impedance values of the low acoustic impedance materials 222 and the acoustic impedance values of the high acoustic impedance materials 224 is high. Accordingly, the low acoustic impedance materials 222 include a PSO dielectric (e.g., a PSO oxide such as PSO silicon oxide or PSO silicon dioxide). The high acoustic impedance materials 224 are selected to impose a high difference between the acoustic impedance values of the low acoustic impedance materials 222 and the

high acoustic impedance materials 224. By way of non-limiting example, the high acoustic impedance materials 224 may include a metal (e.g., tungsten, which is widely used in semiconductor fabrication). The low acoustic impedance materials 222 and the high acoustic impedance materials 224 may each be on the order of about one micron thick in embodiments where cellular RF frequencies (about two gigahertz) are used.

[0029] Also by way of non-limiting example, the high acoustic impedance materials 224 may include dielectric materials (e.g., non-porous or low porous dielectrics or oxides that have been disposed using CVD, sputtering, or spin-on techniques) having higher acoustic impedance values than those of the low acoustic impedance materials 222. As a result, the acoustic isolator 220 may include an all dielectric Bragg reflector. By not using metals for the high acoustic impedance materials 224, substrate loss through induced current may be reduced or eliminated. Metals may, in general, have higher acoustic impedance values than high acoustic impedance dielectrics. The lower acoustic impedance values of high acoustic impedance dielectrics makes it difficult to implement efficient all dielectric Bragg reflectors using CVD and sputtering techniques. The high controllability of porosity of the low acoustic impedance materials 222, however, enables very low acoustic impedance values. These very low acoustic impedance values are sufficiently low to create sufficient contrast with the acoustic impedance values of the high acoustic impedance dielectrics to make all acoustic Bragg reflectors feasible.

[0030] FIG. 3 is a simplified cross-sectional view of another example of the electronic device of FIG. 1, according to some embodiments. An electronic device 300 includes a semiconductor structure (e.g., a substrate 330), an acoustic device 310 (e.g., an FBAR including a piezoelectric material 314 between electrodes 312, 316) on or in the semiconductor structure, and an acoustic isolator 320. The acoustic isolator 320 is similar to the acoustic isolator 220 discussed above with reference to FIG. 2, including a Bragg reflector. The acoustic isolator 320 includes a periodic structure of low acoustic impedance materials 322 having relatively low acoustic impedance values and high acoustic impedance materials 324 having acoustic impedance values that are higher than those of the low acoustic impedance materials 322. One or more of the low acoustic impedance materials 322, however, are grated (e.g., a multilayer configuration) into subregions 322A, 322B, 322C, 322D,

322E (sometimes referred to herein as “subregions” 322A-E) having varying porosity (and consequently, varying acoustic impedance values).

[0031] A spin-on process used to dispose the low acoustic impedance materials 322 may be controlled such that the subregions 322A-E manifest multistep indices (e.g., a graded porosity profile), such as triangular or sinusoidal steps. These multistep indices can improve reflection efficiency over simple bi-level steps. By repeating multiple different porosity precursor spinning, very well controlled step profiles can be fabricated. By way of non-limiting example, a graded porosity profile of the low acoustic impedance material 322 may be graded according to a triangular function of space. Also by way of non-limiting example, a graded porosity profile of the low acoustic impedance material 322 may be graded according to a sinusoidal function of space.

[0032] Referring once again to FIG. 1, if porosity of the PSO material of the acoustic isolator 120 is sufficiently high (e.g., greater than or equal to 50% porosity), the PSO material can behave similarly to an air-like isolation region. Accordingly, in such embodiments, the PSO material may be used to replace air regions in semiconductor devices without compromising mechanical strength. In such embodiments, a very simple integration scheme, such as integration schemes discussed with respect to and illustrated in FIGS. 4-7, can be implemented (e.g., as an alternative to membrane undercut processes).

[0033] FIG. 4 is a simplified cross-sectional view of yet another example of the electronic device of FIG. 1, according to some embodiments. An electronic device 400 includes a substrate 430, a PSO oxide 420, and a piezoelectric material 410 having electrodes 412 in contact therewith. The piezoelectric material 410 and electrodes 412 may together be at least part of a CMR. Rather than including an undercut region isolating the piezoelectric material 410 from the substrate 430, the electronic device 400 includes the PSO oxide 420 having a high porosity (e.g., about 50% or higher porosity). The PSO oxide 420 may behave similarly to an air gap because of its high porosity. A mechanical strength of the electronic device 400, however, may be greater than that of a similar structure with an air gap. Also, since spin-on dielectrics are relatively flowable, the spin-on oxide 420 may be flowed under the piezoelectric material 410 after the piezoelectric material 410 is disposed on or in the substrate 430. More generally, because of its flowable nature, PSO dielectrics

may be used to back-fill into a region that would typically include an air gap after undercut. This gives flexible integration options.

[0034] FIG. 5 is a simplified cross-sectional view of a further example of the electronic device of FIG. 1, according to some embodiments. An electronic device 500 includes a substrate 530, a PSO 520, and an acoustic device 510 (e.g., an FBAR including a piezoelectric material 514 between electrodes 512, 516). Rather than including an undercut region isolating the acoustic device 510 from the substrate 530, the electronic device 500 includes the PSO oxide 520 having a high porosity (e.g., about 50% or higher porosity). The PSO oxide 520 may behave similarly to an air gap because of its high porosity. A mechanical strength of the electronic device 500, however, may be greater than that of a similar structure with an air gap.

[0035] Another possible implementation for PSO dielectrics is an anchor-less acoustic device. For mechanical rigidity, some membrane based acoustic devices are anchored to a substrate or surrounding structure using a thick lateral anchor. In some instances, this anchor can be a significant energy loss path. By solidly mounting an acoustic device with a PSO oxide instead of or in addition to the lateral anchor, the anchor loss can be reduced (e.g., eliminated) and/or the mechanical strength may be improved. FIGS. 6 and 7 illustrate examples of such embodiments.

[0036] FIG. 6 is a simplified cross-sectional view of yet another example of the electronic device of FIG. 1, according to some embodiments. An electronic device 600 includes a substrate 630, a piezoelectric material 614 disposed on or in the substrate 630, electrodes 612 on the piezoelectric material 614, and a PSO oxide 620 isolating the piezoelectric material 614 from the substrate 630. The piezoelectric material 614 and the electrodes 612 may make up at least part of a CMR. The electronic device 600 also includes a lateral anchor 640 providing mechanical support to the piezoelectric material 614. The lateral anchor 640 may include a rigid material that is different from the PSO oxide 620. Since the PSO oxide 620 provides mechanical support to the piezoelectric material 614, the anchor 640 may be relatively thin, reducing the energy loss through the anchor 640.

[0037] FIG. 7 is a simplified cross-sectional view of a further example of the electronic device of FIG. 1, according to some embodiments. An electronic device 700 is similar to the electronic device 600 of FIG. 6. The electronic device 700

includes a substrate 730, a PSO oxide 720, a piezoelectric material 714, and electrodes 712, similar to the substrate 630, the PSO oxide 620, the piezoelectric material 614, and the electrodes 612 of FIG. 6. The electronic device 700, however, does not include a lateral anchor. Rather, the piezoelectric material 714 may be mechanically supported (e.g., completely, mostly, etc.) by the PSO oxide 720. As the electronic device 700 does not include a lateral anchor, no energy loss occurs through a lateral anchor.

[0038] FIG. 8 is a simplified flowchart illustrating a method 800 of manufacturing an electronic device (e.g., the electronic device 100 of FIG. 1), according to some embodiments. Referring to FIGS. 1 and 8 together, the method 800 includes forming 810 an acoustic device 110 including at least one electrode onto or into a semiconductor structure 130. In some embodiments, disposing 810 an acoustic device 110 onto or into a semiconductor structure 130 includes disposing the acoustic device 110 onto the PSO dielectric. In some embodiments, forming 810 an acoustic device 110 onto or into a semiconductor structure 130 includes forming one of an FBAR, a CMR, or a SAW resonator onto or into the semiconductor structure 130.

[0039] The method 800 also includes spinning 820 a PSO dielectric onto or into the semiconductor structure 130 to acoustically isolate the acoustic device 110 from the semiconductor structure 130. In some embodiments, spinning 820 a PSO dielectric onto or into the semiconductor structure 130 includes spinning the PSO dielectric into an undercut region between the semiconductor structure 130 and the acoustic device 110. The method 800 further includes curing 830 the PSO dielectric onto or into the semiconductor structure 130. In some embodiments, curing 830 the PSO dielectric includes annealing the PSO dielectric.

[0040] FIG. 9 illustrates an interposer 1000, according to some embodiments. The interposer 1000 is an intervening substrate used to bridge a first substrate 1002 to a second substrate 1004. The first substrate 1002 may be, for instance, an integrated circuit die. The second substrate 1004 may be, for instance, a memory module, a computer motherboard, or another integrated circuit die. In some embodiments, one of the first substrate 1002 or the second substrate 1004 may include the electronic device 100 of FIG. 1. Generally, the purpose of an interposer 1000 is to spread a connection to a wider pitch or to reroute a connection to a different connection. For example, an interposer 1000 may couple an integrated circuit die to a ball grid array

(BGA) 1006 that can subsequently be coupled to the second substrate 1004. In some embodiments, the first and second substrates 1002/1004 are attached to opposing sides of the interposer 1000. In other embodiments, the first and second substrates 1002/1004 are attached to the same side of the interposer 1000. And in further embodiments, three or more substrates are interconnected by way of the interposer 1000.

[0041] The interposer 1000 may be formed of an epoxy resin, a fiberglass-reinforced epoxy resin, a ceramic material, or a polymer material such as polyimide. In further implementations, the interposer may be formed of alternate rigid or flexible materials that may include the same materials described above for use in a semiconductor substrate, such as silicon, germanium, and other group III-V and group IV materials.

[0042] The interposer 1000 may include metal interconnects 1008 and vias 1010, including but not limited to through-silicon vias (TSVs) 1012. The interposer 1000 may further include embedded devices 1014, including both passive and active devices. Such devices include, but are not limited to, capacitors, decoupling capacitors, resistors, inductors, fuses, diodes, transformers, sensors, and electrostatic discharge (ESD) devices. More complex devices such as RF devices, power amplifiers, power management devices, antennas, arrays, sensors, and MEMS devices may also be formed on the interposer 1000.

[0043] In accordance with embodiments disclosed herein, apparatuses or processes disclosed herein may be used in the fabrication of interposer 1000.

[0044] FIG. 10 illustrates a computing device 1200, according to some embodiments. The computing device 1200 may include a number of components. In one embodiment, these components are attached to one or more motherboards. In an alternative embodiment, some or all of these components are fabricated onto a single system-on-a-chip (SoC) die, such as an SoC used for mobile devices. The components in the computing device 1200 include, but are not limited to, an integrated circuit die 1202 and at least one communications logic unit 1208. In some implementations the communications logic unit 1208 is fabricated within the integrated circuit die 1202 while in other implementations the communications logic unit 1208 is fabricated in a separate integrated circuit chip that may be bonded to a substrate or motherboard that is shared with or electronically coupled to the integrated circuit die 1202. In some embodiments, the communications logic unit 1208 may include the electronic device 100. By way of non-limiting example, the

communications logic unit 1208 may include an RF filter, a duplexer, or an oscillator including the acoustic device 110 of FIG. 1. The integrated circuit die 1202 may include a processor 1204 (e.g., a CPU) as well as on-die memory 1206, often used as cache memory, that can be provided by technologies such as embedded DRAM (eDRAM), SRAM, or spin-transfer torque memory (STT-MRAM).

[0045] Computing device 1200 may include other components that may or may not be physically and electrically coupled to the motherboard or fabricated within an SoC die. These other components include, but are not limited to, volatile memory 1210 (e.g., DRAM), non-volatile memory 1212 (e.g., ROM or flash memory), a graphics processing unit 1214 (GPU), a digital signal processor 1216, a crypto processor 1242 (e.g., a specialized processor that executes cryptographic algorithms within hardware), a chipset 1220, at least one antenna 1222 (in some implementations two or more antenna may be used), a display or a touchscreen display 1224, a touchscreen controller 1226, a battery 1228 or other power source, a power amplifier (not shown), a voltage regulator (not shown), a global positioning system (GPS) device 1222, a compass, a motion coprocessor or sensors 1232 (that may include an accelerometer, a gyroscope, and a compass), a microphone (not shown), a speaker 1234, a camera 1236, user input devices 1238 (such as a keyboard, mouse, stylus, and touchpad), and a mass storage device 1240 (such as hard disk drive, compact disk (CD), digital versatile disk (DVD), and so forth). The computing device 1200 may incorporate further transmission, telecommunication, or radio functionality not already described herein. In some implementations, the computing device 1200 includes a radio that is used to communicate over a distance by modulating and radiating electromagnetic waves in air or space. In further implementations, the computing device 1200 includes a transmitter and a receiver (or a transceiver) that is used to communicate over a distance by modulating and radiating electromagnetic waves in air or space.

[0046] The communications logic unit 1208 enables wireless communications for the transfer of data to and from the computing device 1200. The term “wireless” and its derivatives may be used to describe circuits, devices, systems, methods, techniques, communications channels, etc., that may communicate data through the use of modulated electromagnetic radiation through a non-solid medium. The term does not imply that the associated devices do not contain any wires, although in some embodiments they might not. The communications logic unit 1208 may implement

any of a number of wireless standards or protocols, including but not limited to Wi-Fi (IEEE 802.11 family), WiMAX (IEEE 802.16 family), IEEE 802.20, long term evolution (LTE), Ev-DO, HSPA+, HSDPA+, HSUPA+, EDGE, GSM, GPRS, CDMA, TDMA, DECT, Infrared (IR), Near Field Communication (NFC), Bluetooth, derivatives thereof, as well as any other wireless protocols that are designated as 3G, 4G, 5G, and beyond. The computing device 1200 may include a plurality of communications logic units 1208. For instance, a first communications logic unit 1208 may be dedicated to shorter range wireless communications such as Wi-Fi, NFC, and Bluetooth and a second communications logic unit 1208 may be dedicated to longer range wireless communications such as GPS, EDGE, GPRS, CDMA, WiMAX, LTE, Ev-DO, and others.

[0047] In some embodiments, the processor 1204 of the computing device 1200 includes one or more devices, such as the acoustic device 110, the acoustic isolator 120, and the semiconductor structure 130, that are formed in accordance with embodiments disclosed herein. By way of non-limiting example, the processor 1204 may include an RF filter, a duplexer, or an oscillator including the acoustic device 110. The term “processor” may refer to any device or portion of a device that processes electronic data from registers and/or memory to transform that electronic data into other electronic data that may be stored in registers and/or memory.

[0048] The communications logic unit 1208 may also include one or more devices, such as RF filters, duplexers, or oscillators, that are formed in accordance with embodiments of the disclosure. By way of non-limiting example, an RF filter, a duplexer, or an oscillator may include the electronic device 100 of FIG. 1.

[0049] In further embodiments, another component housed within the computing device 1200 may contain one or more devices, such as RF filters, duplexers, oscillators, or mechanical sensors including the electronic device 100 of FIG. 1, which are formed in accordance with implementations of the disclosure.

[0050] In various embodiments, the computing device 1200 may be a laptop computer, a netbook computer, a notebook computer, an ultrabook computer, a smartphone, a dumbphone, a tablet, a tablet/laptop hybrid, a personal digital assistant (PDA), an ultra mobile PC, a mobile phone, a desktop computer, a server, a printer, a scanner, a monitor, a set-top box, an entertainment control unit, a digital camera, a portable music player, or a digital video recorder. In further

implementations, the computing device 1200 may be any other electronic device that processes data.

[0051] In some embodiments, a plurality of transistors, such as metal-oxide-semiconductor field-effect transistors (MOSFET or simply MOS transistors), may be fabricated on or in a substrate. In various embodiments, the MOS transistors may be planar transistors, nonplanar transistors, or a combination of both. Nonplanar transistors include FinFET transistors such as double-gate transistors and tri-gate transistors, and wrap-around or all-around gate transistors such as nanoribbon and nanowire transistors.

[0052] Each MOS transistor includes a gate stack formed of at least two layers, a gate dielectric layer and a gate electrode layer. The gate dielectric layer may include one layer or a stack of layers. The one or more layers may include silicon oxide, silicon dioxide (SiO_2), and/or a high-k dielectric material. The high-k dielectric material may include elements such as hafnium, silicon, oxygen, titanium, tantalum, lanthanum, aluminum, zirconium, barium, strontium, yttrium, lead, scandium, niobium, and zinc. Examples of high-k materials that may be used in the gate dielectric layer include, but are not limited to, hafnium oxide, hafnium silicon oxide, lanthanum oxide, lanthanum aluminum oxide, zirconium oxide, zirconium silicon oxide, tantalum oxide, titanium oxide, barium strontium titanium oxide, barium titanium oxide, strontium titanium oxide, yttrium oxide, aluminum oxide, lead scandium tantalum oxide, and lead zinc niobate. In some embodiments, an annealing process may be carried out on the gate dielectric layer to improve its quality when a high-k material is used.

[0053] The gate electrode layer is formed on the gate dielectric layer and may include at least one P-type workfunction metal or N-type workfunction metal, depending on whether the transistor is to be a PMOS or an NMOS transistor. In some implementations, the gate electrode layer may include a stack of two or more metal layers, where one or more metal layers are workfunction metal layers and at least one metal layer is a fill metal layer. Further metal layers may be included for other purposes, such as a barrier layer.

[0054] For a PMOS transistor, metals that may be used for the gate electrode include, but are not limited to, ruthenium, palladium, platinum, cobalt, nickel, and conductive metal oxides, e.g., ruthenium oxide. A P-type metal layer will enable the formation of a PMOS gate electrode with a workfunction that is between about 4.9

eV and about 5.2 eV. For an NMOS transistor, metals that may be used for the gate electrode include, but are not limited to, hafnium, zirconium, titanium, tantalum, aluminum, alloys of these metals, and carbides of these metals such as hafnium carbide, zirconium carbide, titanium carbide, tantalum carbide, and aluminum carbide. An N-type metal layer will enable the formation of an NMOS gate electrode with a workfunction that is between about 3.9 eV and about 4.2 eV.

[0055] In some implementations, when viewed as a cross-section of the transistor along the source-channel-drain direction, the gate electrode may consist of a “U”-shaped structure that includes a bottom portion substantially parallel to the surface of the substrate and two sidewall portions that are substantially perpendicular to the top surface of the substrate. In another implementation, at least one of the metal layers that form the gate electrode may simply be a planar layer that is substantially parallel to the top surface of the substrate and does not include sidewall portions substantially perpendicular to the top surface of the substrate. In further embodiments, the gate electrode may consist of a combination of U-shaped structures and planar, non-U-shaped structures. For example, the gate electrode may consist of one or more U-shaped metal layers formed atop one or more planar, non-U-shaped layers.

[0056] In some embodiments, a pair of sidewall spacers may be formed on opposing sides of the gate stack that bracket the gate stack. The sidewall spacers may be formed from a material such as silicon nitride, silicon oxide, silicon carbide, silicon nitride doped with carbon, and silicon oxynitride. Processes for forming sidewall spacers are well known in the art and generally include deposition and etching process steps. In an alternative implementation, a plurality of spacer pairs may be used, for instance, two pairs, three pairs, or four pairs of sidewall spacers may be formed on opposing sides of the gate stack.

[0057] As is well known in the art, source and drain regions are formed within the substrate adjacent to the gate stack of each MOS transistor. The source and drain regions are generally formed using either an implantation/diffusion process or an etching/deposition process. In the former process, dopants such as boron, aluminum, antimony, phosphorous, or arsenic may be ion-implanted into the substrate to form the source and drain regions. An annealing process that activates the dopants and causes them to diffuse further into the substrate typically follows the ion implantation process. In the latter process, the substrate may first be etched to

form recesses at the locations of the source and drain regions. An epitaxial deposition process may then be carried out to fill the recesses with material that is used to fabricate the source and drain regions. In some implementations, the source and drain regions may be fabricated using a silicon alloy such as silicon germanium or silicon carbide. In some implementations the epitaxially deposited silicon alloy may be doped in situ with dopants such as boron, arsenic, or phosphorous. In further embodiments, the source and drain regions may be formed using one or more alternative semiconductor materials such as germanium or a group III-V material or alloy. And in further embodiments, one or more layers of metal and/or metal alloys may be used to form the source and drain regions.

[0058] One or more interlayer dielectrics (ILD) are deposited over the MOS transistors. The ILD layers may be formed using dielectric materials known for their applicability in integrated circuit structures, such as low-k dielectric materials. Examples of dielectric materials that may be used include, but are not limited to, silicon dioxide (SiO_2), carbon doped oxide (CDO), silicon nitride, organic polymers such as perfluorocyclobutane or polytetrafluoroethylene, fluorosilicate glass (FSG), and organosilicates such as silsesquioxane, siloxane, or organosilicate glass. The ILD layers may include pores or air gaps to further reduce their dielectric constant.

Examples

[0059] A list of example embodiments follows. In the interest of brevity and simplicity, not each of the example embodiments in the list is specifically and expressly indicated as being combinable with others of the example embodiments in the list and other embodiments disclosed hereinabove. Unless it would be understood by one of ordinary skill in the art, however, that these example embodiments are not combinable, it is contemplated herein that these example embodiments are combinable with each other and with the other embodiments disclosed hereinabove.

[0060] Example 1: An electronic device, including: a semiconductor structure; an acoustic device on or in the semiconductor structure; and an acoustic isolator including a porous spin-on (PSO) dielectric configured to acoustically isolate the acoustic device from at least a portion of the semiconductor structure, the PSO dielectric having a smoother surface interfacing with the acoustic device than that of a surface of a chemical-vapor deposition (CVD) dielectric and less material stress than that of a porous sputtered dielectric.

[0061] Example 2: The electronic device of Example 1, wherein the PSO dielectric includes a PSO silicon oxide.

[0062] Example 3: The electronic device according to any one of Examples 1 and 2, wherein the PSO dielectric includes a PSO silicon dioxide.

[0063] Example 4: The electronic device according to any one of Examples 1-3, wherein the acoustic isolator includes a plurality of PSO regions separated from each other by a plurality of high acoustic impedance (HAI) regions having an acoustic impedance that is higher than that of the PSO regions.

[0064] Example 5: The electronic device of Example 4, wherein at least one of the HAI regions includes tungsten.

[0065] Example 6: The electronic device according to any one of Examples 4 and 5, wherein at least one of the PSO regions includes a grated PSO material having a grated porosity profile.

[0066] Example 7: The electronic device of Example 6, wherein the grated porosity profile of the at least one of the PSO regions is grated according to a triangular function of space.

[0067] Example 8: The electronic device of Example 6, wherein the grated porosity profile of the at least one of the PSO regions is grated according to a sinusoidal function of space.

[0068] Example 9: The electronic device according to any one of Examples 4-8, wherein at least one of the HAI regions includes a non-porous dielectric.

[0069] Example 10: The electronic device of Example 9, wherein the non-porous dielectric includes a non-porous spin-on dielectric.

[0070] Example 11: The electronic device according to any one of Examples 1-10, wherein the acoustic device includes a Contour Mode Resonator (CMR) that is acoustically isolated by the acoustic isolator and not by an air gap.

[0071] Example 12: The electronic device of Example 11, wherein the CMR is mechanically supported by the PSO dielectric and not a lateral anchor.

[0072] Example 13: The electronic device according to any one of Examples 1-10, wherein the acoustic device includes a Film Bulk Acoustic Resonator (FBAR).

[0073] Example 14: The electronic device according to any one of Examples 1-10, wherein the acoustic device includes a Surface Acoustic Wave (SAW) resonator.

[0074] Example 15: The electronic device according to any one of Examples 1-14, wherein the acoustic isolator directly physically interfaces with at least one electrode of the acoustic device.

[0075] Example 16: The electronic device according to any one of Examples 1-15, wherein the acoustic isolator directly physically interfaces with a piezoelectric material of the acoustic device.

[0076] Example 17: A method of forming an electronic device, the method including: forming an acoustic device onto or into a semiconductor structure; spinning a porous spin-on (PSO) dielectric onto or into the semiconductor structure to acoustically isolate the acoustic device from the semiconductor structure; and curing the PSO dielectric.

[0077] Example 18: The method of Example 17, wherein spinning a PSO dielectric onto or into the semiconductor structure includes spinning the PSO dielectric into an undercut region between the semiconductor structure and the acoustic device.

[0078] Example 19: The method of Example 17, wherein forming an acoustic device onto or into a semiconductor structure includes forming the acoustic device on the PSO dielectric.

[0079] Example 20: The method according to any one of Examples 17-19, wherein forming an acoustic device onto or into a semiconductor structure includes forming one of a Film Bulk Acoustic Resonator (FBAR), a Contour Mode Resonator (CMR), or a Surface Acoustic Wave (SAW) resonator onto or into the semiconductor structure.

[0080] Example 21: A computing device, including: a communication unit including: a semiconductor structure; an acoustic device including a piezoelectric material disposed on or in the semiconductor structure; and a porous spin-on dielectric configured to acoustically isolate the acoustic device from the semiconductor structure.

[0081] Example 22: The computing device of Example 21, further including: a processor mounted on a substrate; a memory unit capable of storing data; a graphics processing unit; an antenna within the computing device; a display on the computing device; a battery within the computing device; a power amplifier within the processor; and a voltage regulator within the processor.

[0082] Example 23: A method of manufacturing an electronic device, the method including: forming a semiconductor structure; disposing an acoustic device on or in

the semiconductor structure; and spinning an acoustic isolator onto the semiconductor structure, the acoustic isolator including a porous spin-on (PSO) dielectric configured to acoustically isolate the acoustic device from at least a portion of the semiconductor structure, the PSO dielectric having a smoother surface interfacing with the acoustic device than that of a surface of a chemical-vapor deposition (CVD) dielectric and less material stress than that of a porous sputtered dielectric.

[0083] Example 24: The method of Example 23, wherein spinning an acoustic isolator onto the semiconductor structure includes spinning a PSO silicon oxide onto the semiconductor structure.

[0084] Example 25: The method according to any one of Examples 23 and 24, wherein spinning an acoustic isolator onto the semiconductor structure includes spinning a PSO silicon dioxide onto the semiconductor structure.

[0085] Example 26: The method according to any one of Examples 23-25, wherein spinning an acoustic isolator onto the semiconductor structure includes alternating between spinning PSO regions and high acoustic impedance (HAI) regions having an acoustic impedance that is higher than that of the PSO regions onto the semiconductor structure.

[0086] Example 27: The method of Example 26, wherein alternating between spinning PSO regions and HAI regions includes alternating between spinning PSO regions and tungsten regions onto the semiconductor structure.

[0087] Example 28: The method according to any one of Examples 26-27, wherein alternating between spinning PSO regions and HAI regions includes alternating between spinning graded PSO materials having a graded porosity profile and HAI regions onto the semiconductor structure.

[0088] Example 29: The method of Example 28, wherein spinning graded PSO materials having a graded porosity profile onto the semiconductor structure includes spinning PSO materials graded according to a triangular function of space onto the semiconductor structure.

[0089] Example 30: The method of Example 28, wherein spinning graded PSO materials having a graded porosity profile onto the semiconductor structure includes spinning PSO materials graded according to a sinusoidal function of space onto the semiconductor structure.

[0090] Example 31: The method according to any one of Examples 26-30, wherein spinning HAI regions onto the semiconductor structure includes spinning at least one non-porous dielectric onto the semiconductor structure.

[0091] Example 32: The method of Example 31, wherein spinning at least one non-porous dielectric onto the semiconductor structure includes spinning a non-porous spin-on dielectric onto the semiconductor structure.

[0092] Example 33: The method according to any one of Examples 23-32, wherein disposing an acoustic device on or in the semiconductor structure includes: disposing a Contour Mode Resonator (CMR) on or in the semiconductor structure; and acoustically isolating the CMR with the acoustic isolator and not with an air gap.

[0093] Example 34: The method of Example 33, further including mechanically supporting the CMR with the PSO dielectric and not with a lateral anchor.

[0094] Example 35: The method according to any one of Examples 23-32, wherein disposing an acoustic device on or in the semiconductor structure includes disposing a Film Bulk Acoustic Resonator (FBAR) on or in the semiconductor structure.

[0095] Example 36: The method according to any one of Examples 23-32, wherein disposing an acoustic device on or in the semiconductor structure includes disposing a Surface Acoustic Wave (SAW) resonator on or in the semiconductor structure.

[0096] Example 37: The method according to any one of Examples 23-36, wherein spinning an acoustic isolator onto the semiconductor structure includes spinning the acoustic isolator onto the semiconductor structure and disposing the at least one electrode directly on the acoustic isolator.

[0097] Example 38: The method according to any one of Examples 23-37, wherein spinning an acoustic isolator onto the semiconductor structure includes spinning the acoustic isolator onto the semiconductor structure and disposing a piezoelectric material of the acoustic device directly onto the acoustic isolator.

[0098] Example 39: An electronic device including: an acoustic device on or in a semiconductor structure; and a porous spin-on (PSO) dielectric on or in the semiconductor structure to acoustically isolate the acoustic device from the semiconductor structure.

[0099] Example 40: The electronic device of Example 39, wherein the PSO dielectric is located in an undercut region between the semiconductor structure and the acoustic device.

[0100] Example 41: The electronic device of Example 39, wherein the acoustic device is disposed on the PSO dielectric.

[0101] Example 42: The electronic device according to any one of Examples 39-41, wherein the acoustic device includes one of a Film Bulk Acoustic Resonator (FBAR), a Contour Mode Resonator (CMR), or a Surface Acoustic Wave (SAW) resonator.

[0102] Example 43: A method of operating a computing device, the method including: operating a communication unit including: a semiconductor structure; an acoustic device including a piezoelectric material disposed on or in the semiconductor structure; and a porous spin-on dielectric configured to acoustically isolate the acoustic device from the semiconductor structure.

[0103] Example 44: The method of Example 21, further including: operating a processor mounted on a substrate; operating a memory unit capable of storing data; operating a graphics processing unit; operating an antenna within the computing device; operating a display on the computing device; operating a battery within the computing device; operating a power amplifier within the processor; and operating a voltage regulator within the processor.

[0104] Example 45: An electronic device, comprising: an acoustic device on or in a semiconductor structure; and a porous spin-on (PSO) dielectric configured to acoustically isolate the acoustic device from at least a portion of the semiconductor structure, the PSO dielectric having a root mean square roughness of a surface interfacing with the acoustic device that is less than or equal to about one nanometer (1 nm).

[0105] Example 46: The electronic device of Example 45, wherein a porosity of the PSO dielectric is at least about fifty percent (50%).

[0106] Example 47: The electronic device according to any one of Examples 45 and 46, wherein the PSO dielectric includes crosslinked cyclic carbosilanes.

[0107] Example 48: A method of operating an electronic device, the method comprising: forming an acoustic device on or in a semiconductor structure; and spinning on a porous spin-on (PSO) dielectric configured to acoustically isolate the acoustic device from at least a portion of the semiconductor structure, the PSO dielectric having a root mean square roughness of a surface interfacing with the acoustic device that is less than or equal to about one nanometer (1 nm).

[0108] Example 49: The method of Example 48, wherein spinning on a PSO dielectric includes spinning on the PSO dielectric having a porosity that is at least about fifty percent (50%).

[0109] Example 50: The method according to any one of examples 48 and 49, wherein spinning on a PSO dielectric includes spinning on the PSO dielectric having crosslinked cyclic carbosilanes.

[0110] Example 51: A means for performing at least a portion of the method according to any one of Examples 17-20, 23-38, 43, 44, and 48-50.

Conclusion

[0111] The above description of illustrated embodiments, including what is described in the Abstract, is not intended to be exhaustive or to limit the disclosure to the precise forms disclosed. While specific implementations, embodiments, and examples are described herein for illustrative purposes, various equivalent modifications are possible within the scope of the disclosure, as those skilled in the relevant art will recognize.

Claims

1. An electronic device, comprising:
a semiconductor structure;
an acoustic device on or in the semiconductor structure; and
an acoustic isolator including a porous spin-on (PSO) dielectric configured to acoustically isolate the acoustic device from at least a portion of the semiconductor structure, the PSO dielectric having a smoother surface interfacing with the acoustic device than that of a surface of a chemical-vapor deposition (CVD) dielectric and less material stress than that of a porous sputtered dielectric.
2. The electronic device of claim 1, wherein the PSO dielectric includes a PSO silicon oxide.
3. The electronic device of claim 1, wherein the PSO dielectric includes a PSO silicon dioxide.
4. The electronic device according to any one of claims 1-3, wherein the acoustic isolator includes a plurality of PSO regions separated from each other by a plurality of high acoustic impedance (HAI) regions having an acoustic impedance that is higher than that of the PSO regions.
5. The electronic device of claim 4, wherein at least one of the HAI regions includes tungsten.
6. The electronic device of claim 4, wherein at least one of the PSO regions includes a grated PSO material having a grated porosity profile.
7. The electronic device of claim 6, wherein the grated porosity profile of the at least one of the PSO regions is grated according to a triangular function of space.
8. The electronic device of claim 6, wherein the grated porosity profile of the at least one of the PSO regions is grated according to a sinusoidal function of space.
9. The electronic device of claim 4, wherein at least one of the HAI regions includes a non-porous dielectric.
10. The electronic device of claim 9, wherein the non-porous dielectric includes a non-porous spin-on dielectric.
11. The electronic device according to any one of claims 1-3, wherein the acoustic device includes a Contour Mode Resonator (CMR) that is acoustically isolated by the acoustic isolator and not by an air gap.

12. The electronic device of claim 11, wherein the CMR is mechanically supported by the PSO dielectric and not a lateral anchor.

13. The electronic device according to any one of claims 1-3, wherein the acoustic device includes a Film Bulk Acoustic Resonator (FBAR).

14. The electronic device according to any one of claims 1-3, wherein the acoustic device includes a Surface Acoustic Wave (SAW) resonator.

15. The electronic device according to any one of claims 1-3, wherein the acoustic isolator directly physically interfaces with at least one electrode of the acoustic device.

16. The electronic device according to any one of claims 1-3, wherein the acoustic isolator directly physically interfaces with a piezoelectric material of the acoustic device.

17. A method of forming an electronic device, the method comprising:
forming an acoustic device onto or into a semiconductor structure;
spinning a porous spin-on (PSO) dielectric onto or into the semiconductor structure to acoustically isolate the acoustic device from the semiconductor structure;
and
curing the PSO dielectric.

18. The method of claim 17, wherein spinning a PSO dielectric onto or into the semiconductor structure includes spinning the PSO dielectric into an undercut region between the semiconductor structure and the acoustic device.

19. The method of claim 17, wherein forming an acoustic device onto or into a semiconductor structure includes forming the acoustic device on the PSO dielectric.

20. The method according to any one of claims 17-19, wherein forming an acoustic device onto or into a semiconductor structure includes forming one of a Film Bulk Acoustic Resonator (FBAR), a Contour Mode Resonator (CMR), or a Surface Acoustic Wave (SAW) resonator onto or into the semiconductor structure.

21. A computing device, comprising:
a communication unit including:
a semiconductor structure;
an acoustic device including a piezoelectric material disposed on or in the semiconductor structure; and

a porous spin-on dielectric configured to acoustically isolate the acoustic device from the semiconductor structure.

22. The computing device of claim 21, further comprising:

a processor mounted on a substrate;
a memory unit capable of storing data;
a graphics processing unit;
an antenna within the computing device;
a display on the computing device;
a battery within the computing device;
a power amplifier within the processor; and
a voltage regulator within the processor.

23. An electronic device, comprising:

an acoustic device on or in a semiconductor structure; and
a porous spin-on (PSO) dielectric configured to acoustically isolate the acoustic device from at least a portion of the semiconductor structure, the PSO dielectric having a root mean square roughness of a surface interfacing with the acoustic device that is less than or equal to about one nanometer (1 nm).

24. The electronic device of claim 23, wherein a porosity of the PSO dielectric is at least about fifty percent (50%).

25. The electronic device according to any one of claims 23 and 24, wherein the PSO dielectric includes crosslinked cyclic carbosilanes.

100 →

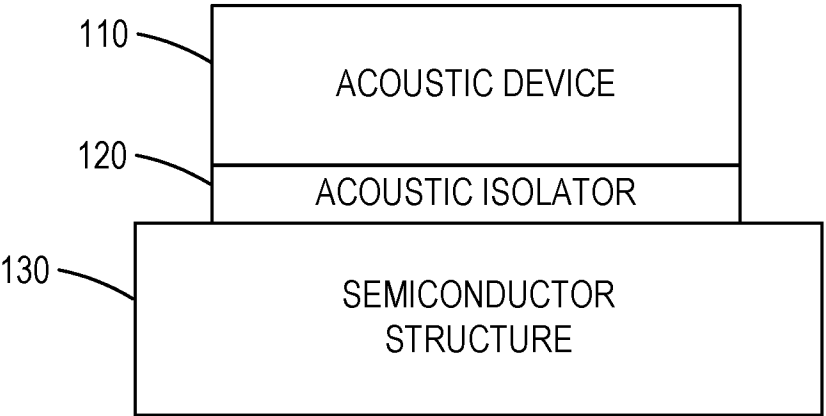


FIG. 1

200 →

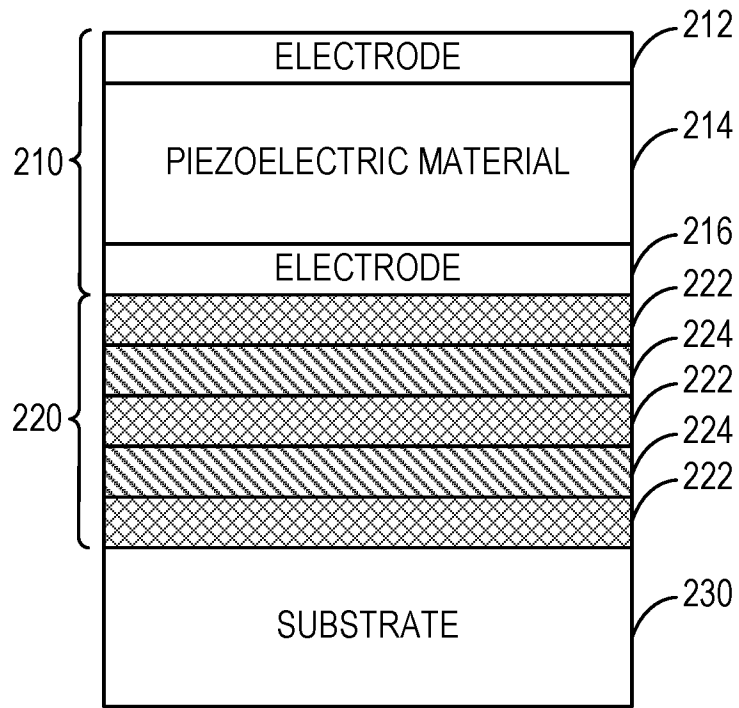


FIG. 2

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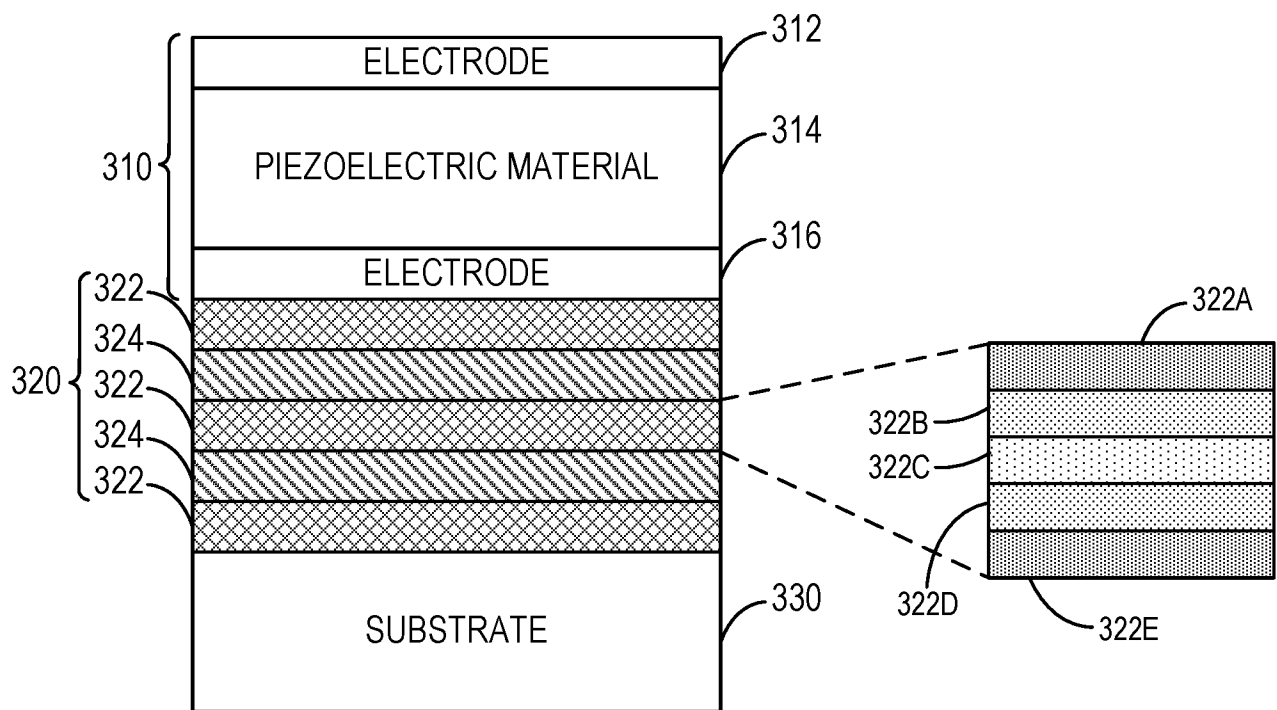


FIG. 3

400

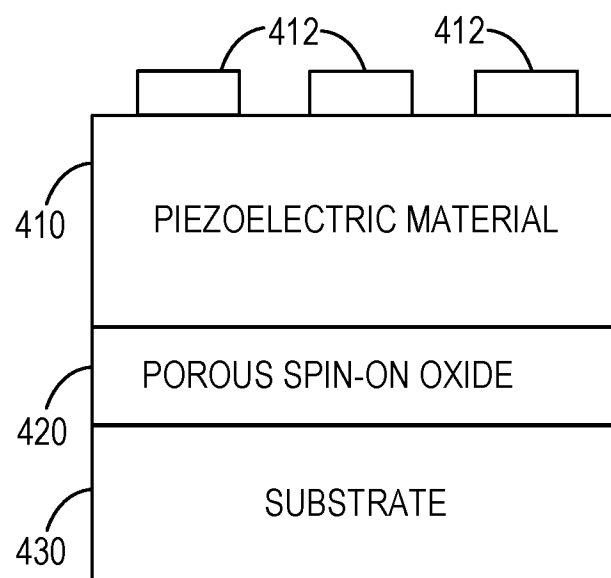


FIG. 4

500 →

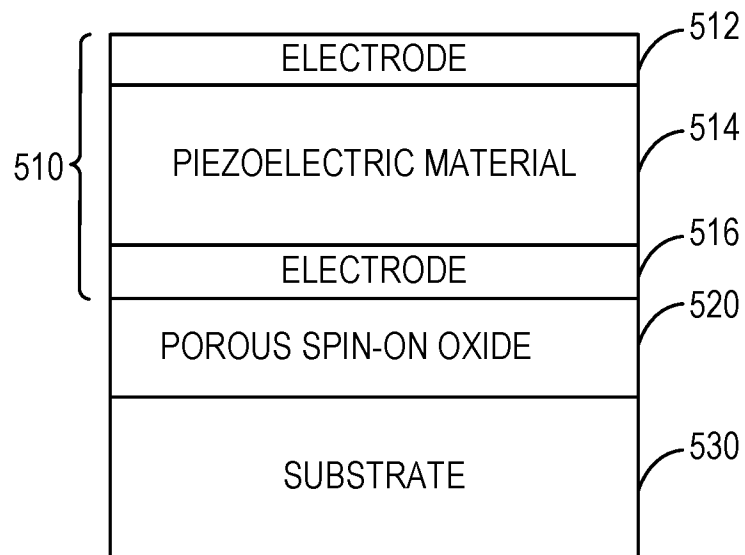


FIG. 5

600 →

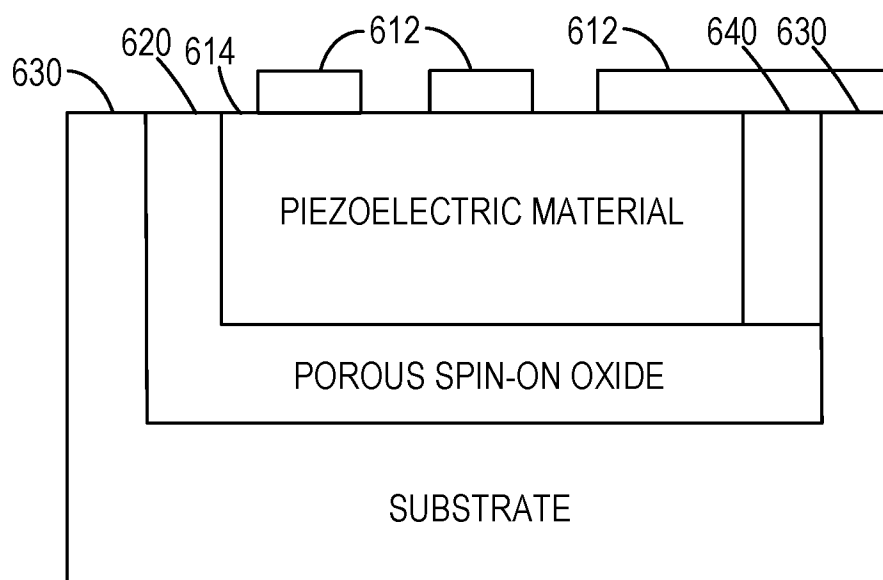


FIG. 6

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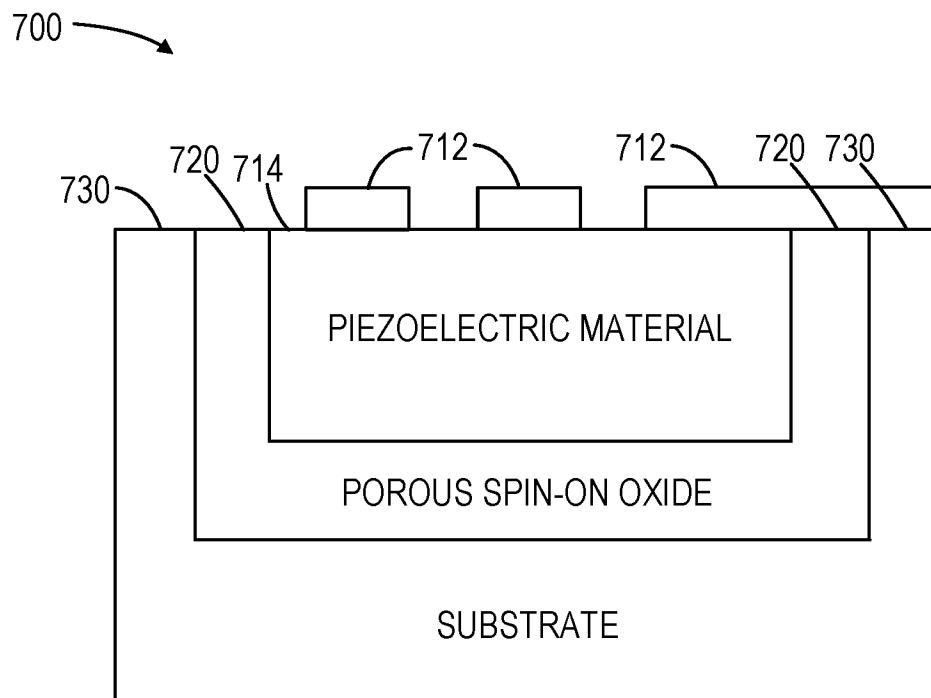


FIG. 7

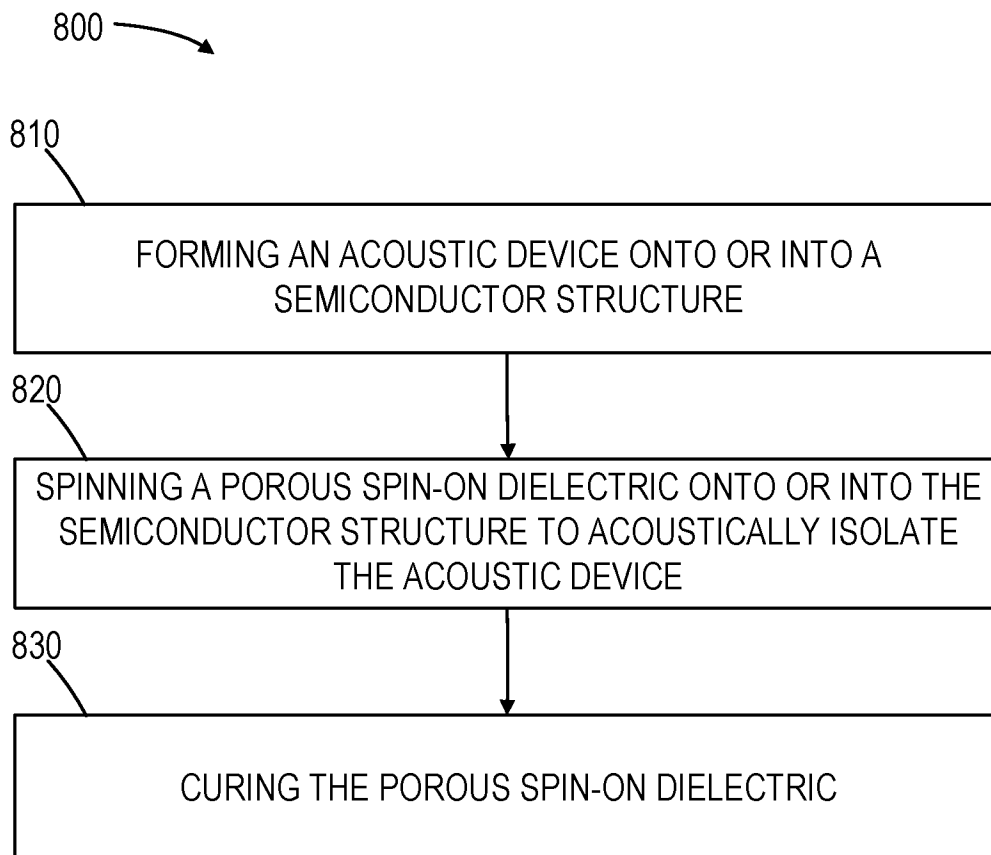


FIG. 8

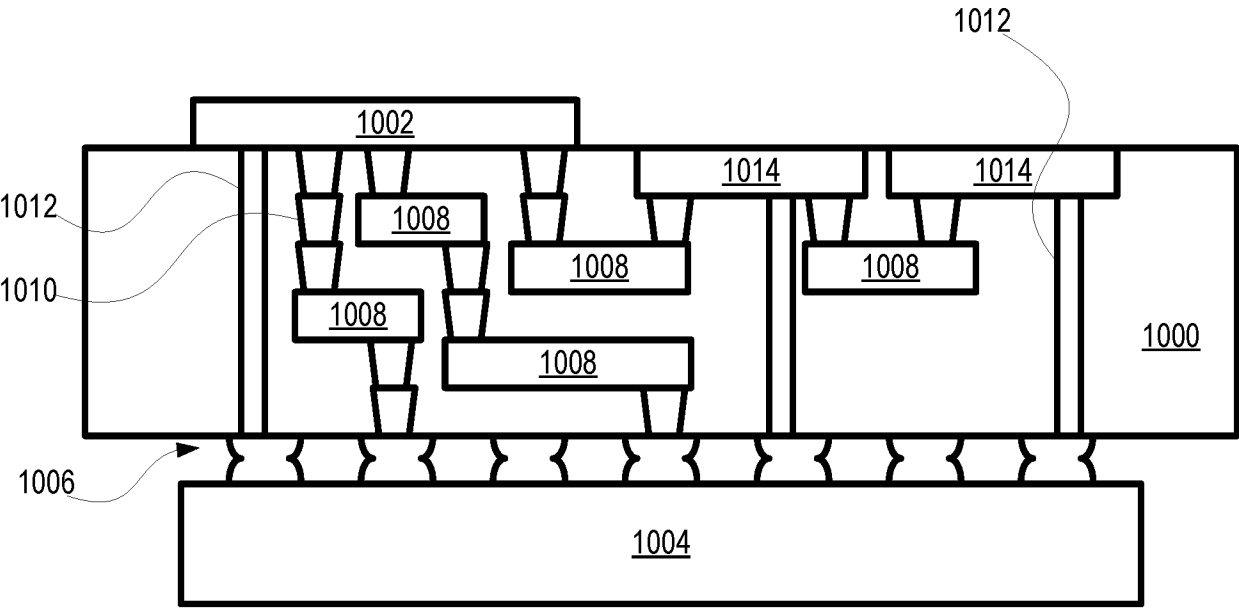


FIG. 9

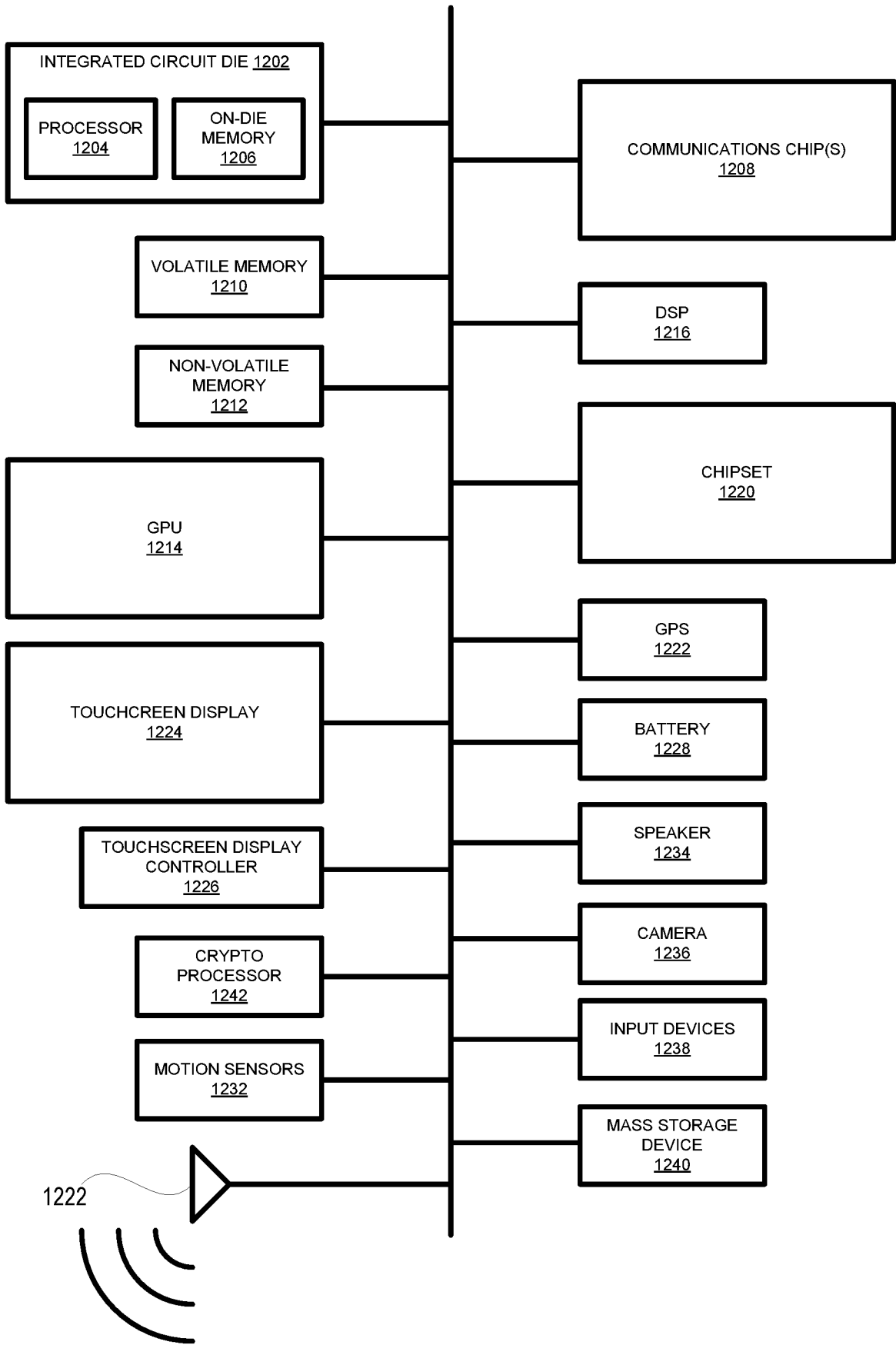


FIG. 10

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2017/025475**A. CLASSIFICATION OF SUBJECT MATTER****H03H 9/17(2006.01)i, H01L 21/205(2006.01)i, H01L 41/08(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H03H 9/17; H03H 9/56; H03H 3/02; H01L 41/02; H03H 9/54; H01L 21/205; H01L 41/08

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & keywords: acoustic, piezoelectric, void, porosity, filter

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2007-0285191 A1 (STUART M. JACOBSEN) 13 December 2007 See paragraphs [0002]-[0008], [0012], [0022]-[0036]; claims 1-4, 8-9; and figures 3-4.	1-25
A	US 2014-0125198 A1 (TEXAS INSTRUMENTS INCORPORATED) 08 May 2014 See paragraphs [0012]-[0018]; and figures 1-2.	1-25
A	JP 10-051255 A (KYOCERA CORP.) 20 February 1998 See paragraphs [0016]-[0033]; and figures 1-2.	1-25
A	US 2012-0056694 A1 (PANG WEI et al.) 08 March 2012 See paragraphs [0057]-[0070]; claims 1-4; and figures 1-2.	1-25
A	US 2007-0096851 A1 (TAKASHI UNO et al.) 03 May 2007 See paragraphs [0047]-[0073]; and figures 1-6.	1-25



Further documents are listed in the continuation of Box C.



See patent family annex.

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"I" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

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"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

22 December 2017 (22.12.2017)

Date of mailing of the international search report

22 December 2017 (22.12.2017)

Name and mailing address of the ISA/KR

International Application Division

Korean Intellectual Property Office

189 Cheongsa-ro, Seo-gu, Daejeon, 35208, Republic of Korea

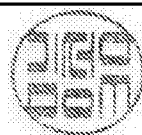


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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2017/025475

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