ABSTRACT
A signal is generated at the time of transfer of control by an electronic computer controlling a multiplicity of local equipment to control by a fail-safe apparatus if the phase time of display of traffic signals of one of the local equipments is in coincidence with the phase time of the fail-safe apparatus. This signal inhibits the control of the traffic signals by the local equipment, and the fail-safe apparatus controls the traffic signals. If the phase of display of traffic signals is not in coincidence with the phase of the fail-safe apparatus at the time of transfer of control, the signal is not generated, and the control of traffic signals is performed by the local equipment until the above described phases come into coincidence.

4 Claims, 5 Drawing Figures
TRAFFIC SIGNAL CONTROL APPARATUS

The present invention relates to traffic signal control apparatus, and, more particularly, to control apparatus for systematically controlling a plurality of local traffic signal equipments from a remote central control station or a central equipment.

In such a traffic signal control apparatus, control of traffic signals by an electronic computer provided in a central control station is transferred, if for any reason the computer should fail, to control by a fail-safe apparatus provided in the central station. At the time of transfer of control by the computer to control by the fail-safe apparatus, the systematic control will be distorted unless the fail-safe apparatus and the local traffic signal controllers in the local equipments are synchronized.

The object of the invention is to provide a traffic signal control apparatus for controlling a plurality of local traffic signals, wherein a fail-safe apparatus and local traffic signal controllers are synchronized at the time of transfer of the control by a computer to control by the fail-safe apparatus such that the transfer of control can be performed without distorting the display of traffic signals.

According to the invention, a signal is transmitted from the computer to the local equipment during normal operation of the computer. This signal, which will be described hereinafter as a hold signal, inhibits the control of the traffic signals by the local equipments and the traffic signals are controlled by the computer.

If the computer should fail, the hold signal from the computer is not transmitted to the local equipments, and the fail-safe apparatus or other signal generating means transmits the hold signal to the local equipments only when the phases of the fail-safe apparatus and the local equipments are in coincidence. In the fail-safe apparatus are set the times for providing right-of-way for a main street at respective intersection and the times for providing right-of-way for a cross street thereof, the times being counted by a clock or a time counter. The periods for providing right-of-way for the main street or the cross street by the fail-safe apparatus are called the phases of the fail-safe apparatus.

When the hold signal is not present at the time of transfer of control by the computer to control by the fail-safe apparatus, each local equipment advances a respective phase counter thereof by a signal generated each time the period of the phase of display of traffic signals has elapsed in each phase. The data of each period of the phases of display of traffic signals are pre-set in the local equipment. The phase counter switches the phase of display of the traffic signals each time the phase counter is advanced. The local controller clears a respective time counter thereof by the signal above described so that the time counter commences counting of the time of a succeeding phase of traffic signals when the traffic signals are switched by the phase counter. Thus the timing of each phase of the display of traffic signals is controlled in accordance with the phase periods or times pre-set in the local traffic signal equipment, if the phase of the fail-safe apparatus is not in coincidence with that of the local equipment at the time of transfer of control by the computer to the control by the fail-safe apparatus until both the phases coincide.

If the time counter in a respective local equipment has counted out the pre-set time of the phase at the time of transfer of control during the hold signal is present, the time counting of the time counter is stopped for a while, and at the time when the phase of the fail-safe apparatus is advanced, a signal is generated by a suitable means. This signal is supplied to the phase counter and to the time counter of the local equipment, to advance the phase counter as well as to commence time counting of the time counter, thereby the control of the local equipment is transferred to the control by the fail-safe apparatus.

Thus, the control by the computer is transferred to control by the fail-safe apparatus at a time when the phase of the fail-safe apparatus is advanced after the right-of-way period for main street or right-of-way period for cross street, both the periods being set in the fail-safe apparatus, and after a period of time has elapsed during which the phase of the fail-safe apparatus becomes coincident with the phase of the local equipment.

The other objects and features of the invention will be made apparent from the following detailed description of a preferred embodiment of the invention, as illustrated in the accompanying drawings:

In the Drawings:

FIG. 1 is a block diagram illustrating one of a large number of local equipments for controlling traffic signals at a respective intersection,

FIG. 2 is a wiring diagram of a part of the local equipment in FIG. 1,

FIG. 3 is a block diagram of the means for generating a hold signal utilized in the invention,

FIG. 4 is an explanatory drawing for explaining the operation of the registers in FIG. 3, and

FIG. 5 is a block diagram illustrating an embodiment of the hold signal generator provided in a central equipment.

In FIG. 1, 1 denotes a clock pulse generator which generates one pulse per second. These pulses will be described hereunder as "second pulses." 2 denotes an AND gate, 3 and 4 denote time-counters respectively, 5 denotes a diode AND matrix, 6 through 11 denote diodes constituting OR circuits in the matrix 5, 12 through 17 denote diodes constituting AND circuits in the matrix 5, 18 denotes a diode OR circuit, 19 denotes a (monostable) (multivibrator) (hereinunder will be described as a flip-flop) 20 and 21 denote inhibit circuits, 22 denotes a diode AND circuit, 23 denotes an OR circuit, 24 denotes a phase counter, 25 denotes a controller for traffic signal lights, 26 denotes a terminal for receiving hold signals from the central equipment, and 27 denotes a terminal for receiving hold signals from the central equipment.

Diodes 6 through 11 and 12 through 17 constitute a part of matrix 5 as illustrated in FIG. 2. As is well known, 30, 31 are resistances, 34, 35, 36, 37 are pin holes connected respectively to the output of a time counter, 32, 33 are diodes constituting AND circuits respectively together with the diodes 12 and 13, and the diodes 6, 7 constitute OR circuits respectively.

Referring again to FIG. 1, the outputs of the diodes 6 and 9 are connected to the reset input terminal of the flip-flop 19 as well as to the input terminal of the inhibit circuit 21. The respective outputs of the diodes 7, 8; 10, 11 is connected to the input terminal of the differentiation circuit 18, the output terminal of the differentiation circuit 18 is connected to the input terminal of
inhibit circuit 21. And the output terminal of inhibit circuit 21 is connected to the input terminal of the differentiation circuit 22. The phase advance signals are supplied to the OR circuit 23 through the terminal 26 from the central equipment. The output of the inhibit circuit 20 and the differentiation circuit 22 are also supplied to the OR circuit 23, and the output of the OR circuit 23 is supplied to the input of the phase counter 24 as well as to the clearance inputs of the counters, 3, 4 and also to the set input of the flip-flop 19. The signal lights controller 25 is controlled by the output of the phase counter 24.

The data of Green period (1G), and Yellow period (1Y) of the display of traffic signals for a main street, and the data of Green period (2G), and Yellow period (2Y) of the display of traffic signals for a cross street and the data of all Red period (1AR) and all Red period (2AR) of the display of the traffic signals for a main street and a cross street are set in the matrix 5. The AND gate 2 is open while the set output of the flip-flop 19 is supplied thereto, thereby the second pulses generated by the generator 1 are supplied to, and counted by, the counters 3, 4. The counters 3, 4 constitute one counter.

The phase counter 24 has output stages for 1G, 1Y, 1AR, 2G, 2Y and 2AR. When the output of the stage for 1G of the phase counter 24 is "1", the phase of display of the traffic signals is made 1G by the controller 25. Similarly, when the output of the stage for 1Y or 1AR, 2G, 2Y, 2AR of the counter 24 is 1, the phase of display of the traffic signals is made 1Y or 1AR, 2G, 2Y, 2AR, respectively. Hereinunder, the state that the output of the phase stage of counter 24 for 1G (or 1Y, 2G, 2Y,) is 1 will be described as the phase of the counter 24 is 1G (or 1Y, 1AR, 2G, 2Y, 2AR).

Now the operation of the control by the computer in the central equipment will be explained. While the local equipment is under control of the computer, the hold signal is generated by the central equipment and the hold signal is transmitted to the local equipment, and is supplied to the inhibit circuits 20, 21 through the terminal 27, thereby the circuits 20, 21 are inhibited. The hold signal can be obtained utilizing the output of the computer while the computer is operating normally. All the phase advance signals are generated by the computer and are supplied to the phase counter 24 through the OR circuit 23, whereby the phase counter 24 is advanced. The phase advance signals are also supplied to the counters 3, 4 through the OR circuit 23, thereby the counters 3, 4 are cleared. Further, the phase advance signals are supplied to the set-input of the flip-flop 19.

In a state that the inhibit circuits 20, 21 are inhibited by the hold signal, the diode 6 or 9 generates a termination signal when the count value of the counters 3, 4 reaches the phase period of 1G or 2G pre-set in the matrix 5 while the phase of the phase counter 24 is 1G or 2G. The termination signal is supplied to the inhibit circuit 21. However, the output of the inhibit circuit 21 does not become 1 since it is inhibited. Accordingly, the output of the OR circuit 23 does not become 1. The termination signal is also supplied to the set-reset-input of the flip-flop 19 through a line 28, thereby the flip-flop 19 is reset, and the set-output thereof becomes "0". Accordingly, the AND gate 2 is closed and the counters 3, 4 stop their time counting. When the phase advance signal is transmitted from the computer in this state, and supplied to the OR circuit 23 through the terminal 26, the output of the OR circuit 23 becomes 1, and advances the phase of the counter 24 and accordingly the phase of display of traffic signals to 1Y or 2Y, and, at the same time, the counters 3, 4 are cleared and the flip-flop 19 is set by the output 1 of the OR circuit 23. The AND gate 2 is open upon setting of the flip-flop 19, and thereby the counters 3, 4 commence the counting of time of 1Y or 2Y. Similarly, when the count value of the counters 3, 4 reaches the pre-set phase period of 1Y or 2Y while the phase of the phase counter 24 is 1Y or 2Y, the diode 7 or 10 in the matrix 5 generates a termination signal. This signal is supplied to the differentiation circuit 18, whereupon the output of the differentiation circuit 18 is supplied to the inhibit circuit 20.

However, since the inhibit circuit 20 is inhibited by the hold signal, the output of the inhibit circuit 20 does not become 1, and, accordingly, no signal is supplied to the phase counter 24. The phase counter 24 is advanced, by the advance signal which is transmitted later from the computer in the central equipment, to the next phase 1AR or 2AR. At the time of the advance of the counter 24 to the phase 1AR or 2AR, the advance signal from the computer is also supplied to the counters 3, 4. The counters 3, 4 are cleared by the signal and commence the counting of phase period of 1AR or 2AR. When the count value of the counters 3, 4 reaches the pre-set phase period of 1AR or 2AR, the diodes 8 or 11 generates a termination signal. The phase counter 24 is not advanced by this termination signal for the same reason as described with respect to the termination signal at the end of the phase 1Y or 2Y. As described above, the local equipment, even though it is operating, supplies no signal to the counter 24, and the counter 24 is controlled by the computer.

If the computer should fail for some reason, the computer ceases the transmission of the phase advance signals to the local equipment. At the same time, discrimination circuits provided in the central equipment discriminate whether the phase of the fail-safe apparatus are in coincidence with those of the local equipments, respectively. The phase of a local equipment is the same with the phase of display of traffic signals thereof.

The fail-safe apparatus comprises, corresponding to each local equipment, as illustrated in FIG. 3, two registers 41 and 42, a flip-flop 43, AND circuits 44 and 45 and an OR circuit 46. The fail-safe apparatus transmits signals for terminating the period of 1G and the period of 2G to the local equipment. The outputs of the registers 41 and 42 become high level alternately, as shown in FIG. 4. The output of the register 41 falls to a low level at the times t2 and t4 where 1G period is to be terminated, and the output of the register 42 falls to a low level at the times t3 and t5 where 2G period is to be terminated. Accordingly, the output of the register 41 is at a high level during the time from t2 to t3 and from t5 to t6, and the output of the register 42 is at a high level during the time from t2 to t3. The flip-flop 43 is set upon rising of the output of the register 42. In other words, the flip-flop 43 is reset upon falling of the output of the register 41, and is set upon falling of the output of the register 42. The set output of the flip-flop 43 is supplied to the AND circuit 44, and the reset output of the flip-flop 43 is supplied to the AND circuit 45. A signal is transmitted from the local equipment while the phase of display of the local signals is 1G or 2G, and is supplied to a respective another input of the AND circuits 44 and 45 through the respective terminals 47 and 48. Therefore, if the phase of display of the traffic signals is
The operations as described above can be summarized as follows.

When the computer ceases transmission of the phase advance signals, the fail-safe apparatus does not generate the hold signal if the phase of the fail-safe apparatus is not in coincidence with that of the display of the local traffic signals, thereby the hold signal is 0. In this case, the inhibit circuits 20 and 21 are not inhibited, and, when the count value by the counters 3, 4 during the phase of display is 1G or 2G, reaches, respectively, preset value in the matrix 5, the termination signal is generated in the local equipment, in other words, the output of the diode 6 or 9 becomes 1. This output 1 is supplied to the differentiation circuit 22 through the inhibit circuit 21, thereupon the differentiation output from the circuit 22 is supplied to the phase counter 24 through the OR circuit 23 and the phase counter 24 is advanced, and the phase of display of traffic signals is switched. The flip-flop 19 is reset by the output 1 of the diode 6 or 9, however, when the output of the OR circuit 23 becomes 1, this output clears the counters 3, 4 and, at the same time, sets the flip-flop 19. Thereby the AND gate 2 is open and the counters 3, 4 commence the counting of the succeeding phase period. Each time the count value of counters 3, 4 reaches the respective preset value of 1Y, 1AR; or 2Y, 2AR in the matrix 5, the respective output of the diode 7, 8, 10 or 11 becomes 1, and is supplied to the differentiation circuit 18, whereby the differentiation output is supplied to the phase counter 24 through the inhibit circuit 20 and the OR circuit 23, whereby the counter 24 is advanced, and the phase of display of traffic signals is switched. Each time the output of the OR circuit 23 becomes 1, the counters 3, 4 are cleared and commence the counting of the succeeding phase period. Thus the traffic signals are controlled in accordance with the pre-set phase times in the matrix 5.

Since the phase periods or cycle period pre-set in the matrix 5 differs from the phase periods or cycle period set in the fail-safe apparatus, as is well known, the phases of the fail-safe apparatus and the phase counter 24 comes into coincidence during the control of the traffic signals in accordance with the pre-set phase times in the matrix 5.

If the phase of the fail-safe apparatus is in coincidence with the phase of display of local traffic signals at the time the computer ceases transmission of the phase advance signals, or comes into coincidence with the phase of display of local traffic signals during the control by the local equipment, the hold signal is transmitted from the fail-safe apparatus, thereby the inhibit circuits 20 and 21 are inhibited. When the count value of the counters 3, 4 reaches the preset value of 1G or 2G in the matrix 5, output of the diode 6 or 9 becomes 1, whereby the flip-flop 19 is reset. Accordingly, the supply of second pulses to the counters 3, 4 ceases and the counters 3, 4 stop the counting. When the phase of the fail-safe apparatus is switched and the hold signal disappears, whereby the inhibit circuits 20, 21 are released, the phase counter 24 is advanced to the succeeding phase by the output 1 of the diode 6 or 9, and, at the same time, the counters 3, 4 are cleared and the flip-flop 19 is set. Upon the setting of the flip-flop 19, the counters 3, 4 commence the counting of the time of the succeeding phase. Since the hold signal is not supplied to the inhibit circuits 20 and 21 during the phases 1Y, 1AR, 2Y and 2AR of the display of the traffic sig-

The operating during the phase of display is 2G is similar to the operation as described above.

The phase 1G or 2G of the phase of display of the traffic signals is terminated, or advanced to the succeeding phase, upon extinction of the hold signal when the hold signal was present at the time the count value of the counters 3, 4 reaches the respective pre-set value of 1G or 2G.
nals, these phases are advanced respectively in accordance with the phase times pre-set in the matrix 5. After the phase 1G or 2G of the display is once terminated at the time of the switching of the phase of the fail-safe apparatus, the succeeding respective phase of 1G and 2G of the display is terminated at each time the phase of the fail-safe apparatus is switched.

Further, if the hold signal disappears, in the case the hold signal has been generated and transmitted to the local equipment before the count value of the counters 3, 4 reaches the pre-set value of the phase of 1G or 2G in the matrix 5, the phase counter 24 is advanced in accordance with the pre-set phase times in the matrix 5.

FIG. 5 is a block diagram illustrating an embodiment of a hold signal generating apparatus. 51 denotes an electronic computer, 52 denotes a flip-flop which is set by the output of the computer 51 when it is operating normally, 53 denotes a second pulse generator, 54 denotes a time counter for counting second pulses generated by the generator 53. The second pulse generator 53 may be a clock which generates one pulse per second. 57, 58, 59 and 60 respectively denote a register. Data of the time for starting the phases of 1G and 2G, or data of the time of terminating the phases of 2G and 1G, at a local equipment are respectively set in the registers 57 and 58, and data of the time for starting the phases 1G and 2G, or data for terminating phases 2G and 1G, at other local equipment are respectively set in the registers 59 and 60. A plurality of sets of the registers 57, 58; 59, 60 are provided in a central equipment, two sets of which being shown in FIG. 5. 61, 62, 63 and 64 denote respectively a coincidence circuit. Each output terminal of the registers 57, 58, 59 and 60 is connected to the respective one input terminal of the coincidence circuits 61, 62, 63 and 64, and the output terminal of the counter 54 is connected to each other input terminal of the coincidence circuits 61 through 64. A flip-flop 65 is set by the output of the circuit 61, and is reset by the output of the circuit 62. A flip-flop 66 is set by the output of the circuit 63, and is reset by the output of the circuit 64. Since both circuits following the flip-flops 65 and 66, respectively, are the same for respective local equipment, only the circuit following the flip-flop 65 will be explained hereunder. The set output terminal of the flip-flop 65 is connected to one input terminal of an AND circuit 67, and the reset output terminal of the flip-flop 65 is connected to one input terminal of an AND circuit 68. Signals transmitted from the local equipment of which data of the time for starting 1G and 2G are set in the registers 7, 8, respectively, are supplied to the other inputs of the AND circuits 67 and 68. Namely, the signal transmitted from the local equipment during the phase of display thereof is 1G, is supplied to the AND circuit 67, and the signal transmitted during the phase of display is 2G, is supplied to the AND circuit 68. The output terminals of the AND circuits 67 and 68 are connected to the input terminal of an OR circuit 69, and the output terminal of the OR circuit 69 is connected to one input terminal of an AND circuit 70. The output terminal of an inverter 71 of which input terminal is connected to the set output terminal of the flip-flop 52, is connected to the other input terminal of the AND circuit 70. The set output terminal of the flip-flop 52 and the output terminal of the AND circuit 70 are connected to the input terminal of an OR circuit 72. The output of the OR circuit 72 is transmitted to the local equipment, and is supplied to the inhibit circuits 20 and 21 in FIG. 1 through the terminal 27 as the hold signal.

When the computer 51 is operating normally, the computer 51 transmits phase advance signals to each local equipment, whereby the phase of display of each local equipment is advanced.

During the normal operation of the computer 51, the flip-flop 52 is set and the set output thereof is 1. Accordingly the output of the inverter 71 is 0, and the output of the AND circuit does not become 1. However, since the set output of the flip-flop 52 is 1, the output is transmitted to the local equipment as the hold signal.

Should the computer 51 fail, the phase advance signal is no more transmitted to the local equipment. Then the flip-flop 52 is reset, and the set output thereof becomes 0, and, accordingly, the output of the inverter 71 becomes 1. When the count value of the counter 54 reaches the value set in the register 57 or 58, the output of the coincidence circuit 61 or 62 appears. The output of the coincidence circuit 61 appears, for example, at the times $t_2$ and $t_3$ in FIG. 4, then the output of the coincidence circuit 62 appears at the times $t_4$ and $t_5$, whereby the flip-flop 65 is set during the periods from $t_2$ to $t_3$ and from $t_4$ to $t_5$, and is reset during the period from $t_3$ to $t_4$. If the phase of display of the local traffic signals becomes 1G while the flip-flop 65 is set, then the output of the AND circuit 67 becomes 1. Since the output of the inverter 71 is 1, the output of the AND circuit 70 becomes 1, and accordingly the output of the OR circuit 72 becomes 1 when the output of the AND circuit 67 becomes 1, and the hold signal is transmitted to the local equipment. Also, if the phase of display of the local traffic signals becomes 2G when the flip-flop 65 is reset, then the output of the AND circuit 68 becomes 1, and thereby the output of the OR circuit 22 becomes 1, and the hold signal is transmitted to the local equipment. If the phase of display of the local traffic signals does not become 1G or 2G, respectively, while the flip-flop 65 is set or reset, the hold signal is not transmitted to the local equipment.

Although the flip-flop 65 and the following circuits 67, 68, 69, 70 and 71 are provided in the central station in the embodiment illustrated in FIG. 5, the circuit 65 through 72 for generating the hold signal may be provided in the local equipment.

What is claimed is:

1. A traffic signal control apparatus for advancing the phase of traffic signals at an intersection by counting the time of display periods of the traffic signals by means of local traffic signal equipment at the intersection and a central equipment for controlling a plurality of local traffic signal equipments by generating control signals including control phase advance signals, comprising:

- first means, provided in the local traffic signal equipment, for counting the time of display periods of the traffic signals at the associated intersection, said first means generating a signal each time a count value corresponding to a pre-set value in each phase time of display;
- second means, provided in the local traffic signal equipment, for advancing the phase of the traffic signals at the associated intersection;
- third means for determining coincidence of the phase time of display of the local traffic signals controlled by said second means of the associated local equipment and the control phase time of display con-
trolled by the central equipment, said third means generating a signal upon coincidence; fourth means responsive to said third means for driving said second means to advance the phase of the traffic signals in accordance with the signal generated by said first means when said third means does not generate a coincidence signal and for driving said second means to advance the phase of the traffic signals in accordance with control phase advance signals from the central equipment when said third means generates a coincidence signal; and fifth means for discontinuing counting of said first means in the period between the generation of the signal by said first means and the driving of said second means.

2. A traffic signal control apparatus according to claim 1, wherein said fourth means includes gate circuit means for receiving signals from said first means and from said third means, said gate circuit means providing output signals in response to the signal supplied thereto, and circuit means for generating a signal in accordance with the output signals of said gate circuit means, said second means being driven by a signal generated from said circuit means when both said third means and said first means provide a signal, and a signal from said circuit means is extinguished.

3. A traffic signal control apparatus according to claim 1, wherein said third means is provided in the local traffic signal equipment.

4. A traffic signal control apparatus according to claim 1, wherein said first means includes preset means for storing a count value corresponding to each phase time of display, and counter means for counting the display time and for generating a signal each time the count value corresponds to a preset value.