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(54) **Title**: METHOD OF MAKING SUB-RESOLUTION PILLAR STRUCTURES USING UNDERCUTTING TECHNIQUE

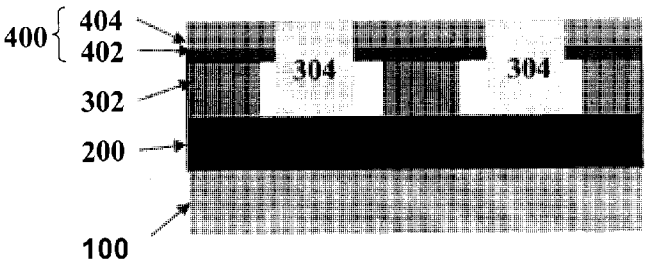

Figure 5B

(57) **Abstract**: A method of making a device includes forming an underlying mask layer over an underlying layer, forming a first mask layer over the underlying mask layer, patterning the first mask layer to form first mask features, undercutting the underlying mask layer to form underlying mask features using the first mask features as a mask, removing the first mask features, and patterning the underlying layer using at least the underlying mask features as a mask.

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METHOD OF MAKING SUB-RESOLUTION PILLAR STRUCTURES USING UNDERCUTTING TECHNIQUE

BACKGROUND OF THE INVENTION

[0001] The present application claims benefit of United States patent application 12/285,466, filed October 6, 2008, which is incorporated herein by reference in its entirety.

BACKGROUND OF THE INVENTION

[0002] The invention relates generally to a method for making a semiconductor device, for example, a nonvolatile memory array containing a diode steering element.

[0003] One prior art process using a hard mask stack shown in Figure 1A can be used to fabricate 45 nm and 80 nm features. The stack consists of a layer of organic hard mask 103, also known as an amorphous carbon advanced patterning film (APF), a layer of Dielectric Anti-Reflective Coating (DARC) 106, such as silicon oxynitride, on top of organic hard mask 103, and a Bottom Anti-Refection Coating (BARC) 109 layer, such as an organic BARC layer, on top of DARC layer 106. A photoresist 111 can be coated above the BARC layer. A device layer 110 can be etched using at least one or more layers of the stack as a mask.

SUMMARY OF THE EMBODIMENTS

[0004] One embodiment of the invention provides a method of making a device, including forming an underlying mask layer over an underlying layer, forming a first mask layer over the underlying mask layer, patterning the first mask layer to form first mask features, undercutting the underlying mask layer to form underlying mask features using the first mask features as a mask, removing the first mask features, and patterning the underlying layer using at least the underlying mask features as a mask.

[0005] Another embodiment of the invention provides a method of making a device, including forming an underlying mask layer over an underlying layer, forming a first mask layer over the underlying mask layer, patterning the first mask layer to form

first mask features, undercutting the underlying mask layer to form underlying mask features using the first mask features as a mask, forming filler features between the underlying mask features and over the underlying layer using the first mask features as a mask, wherein the filler features do not contact the underlying mask features, removing the first mask features, and patterning the underlying layer using at least a combination of the underlying mask features and filler features as a mask.

[0006] Another embodiment of this invention provides a method of making a device, including forming an underlying mask layer over an underlying layer, wherein the underlying layer comprises a resistivity switching storage element layer and a bottom hard mask layer over the resistivity storage element layer, forming a first mask layer over the underlying mask layer, patterning the first mask layer to form first mask features, undercutting the underlying mask layer to form underlying mask features using the first mask features as a mask, removing the first mask features, etching the bottom hard mask layer using at least the underlying mask features as a mask to form first openings, filling the first openings with an insulating material, removing the underlying mask features, removing the bottom hard mask layer to form second openings exposing top of the resistivity switching storage element layer, and filling the second openings with at least one semiconductor material to form semiconductor diodes having a substantially pillar shape in the second openings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0007] Figure 1A is a cross-sectional view illustrating a prior art hard mask configuration.

[0008] Figures 2A, 3A, and 4A are top views illustrating stages in formation of a device according to an embodiment of the present invention. Figures 2B, 3B, and 4B are cross-sectional views along the section line 1 of the structures shown in Figs. 2A, 3A, and 4A, respectively. Figures 2C, and 3C are cross-sectional views along the section line 2 of the same structures shown in Figs. 2A, and 3A, respectively.

[0009] Figures 5A, 6A, and 7A are top views illustrating stages in formation of a device according to a second embodiment of the present invention. Figures 5B, 6B,

and 7B are cross-sectional views along the section line 1 of the same structures shown in Figs. 5A, 6A, and 7A, respectively.

[0010] Figures 8A through 8D are top views illustrating stages in formation of a device according to another embodiment of the present invention. Figure 9 is a perspective view of a memory cell formed according to an embodiment of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0011] One embodiment of the invention provides a method of making a device, including forming an underlying mask layer over an underlying layer, forming a first mask layer over the underlying mask layer, patterning the first mask layer to form first mask features, undercutting the underlying mask layer to form underlying mask features using the first mask features as a mask, removing the first mask features, and patterning the underlying layer using at least the underlying mask features as a mask.

[0012] In some embodiments, the first mask layer comprises one or more hard mask layers. The method further includes forming a photoresist layer over the first mask layer, and patterning the photoresist layer to form a photoresist pattern. The step of patterning the first mask layer may use the photoresist pattern as a mask. Alternatively, the first mask layer can comprise one or more photoresist layers.

[0013] Referring to Figs. 2B and 2C, an underlying layer 200 is formed over a substrate 100. The substrate 100 can be any semiconductor substrate known in the art, such as monocrystalline silicon, IV-IV compounds such as silicon-germanium or silicon carbide, III-V compounds, II-VI compounds, epitaxial layers over such substrates, or any other semiconducting or non-semiconducting material, such as glass, plastic, metal or ceramic substrate. The substrate may include integrated circuits fabricated thereon, such as driver circuits and/or electrodes for a memory device. The underlying layer 200 can be selected from organic hard mask layer, an oxide hard mask layer, a device layer, or combinations thereof. In some embodiments, the underlying layer 200 comprises at least one semiconductor device layer. Any suitable semiconductor materials such as silicon, germanium, silicon

germanium, or other compound semiconductor materials, may be used. However, other device layers, including insulating layers, such as silicon oxide or silicon nitride layers, or conductive layers, such as aluminum, copper, tungsten, titanium, titanium nitride, and alloys thereof may also be used.

[0014] After an underlying mask layer 300 is formed over the underlying layer 200, a first mask layer (not shown) is formed over the underlying mask layer 300, which is then patterned to form first mask features 400. The underlying mask layer 300 can be partially exposed in openings 406 that are defined by the first mask features 400. In some embodiments, as shown in Figs. 2A (top view), 2B (cross-sectional view along the section line 1), and 2C (cross-sectional view along the section line 2), the first mask features 400 comprise sub-resolution features which contact with each other. For example, features may comprise circles or ovals which touch at least one adjacent neighbor (since they are below resolution of the particular lithography system). For example, features 400 may comprise circles arranged in a square or rectangular pattern where each circle contacts four adjacent neighbors.

[0015] The first mask features 400 can comprise one or more hard mask layers, such as a BARC layer, a DARC layer (for example silicon oxynitride), a titanium nitride layer, or a combination thereof. Preferably, as shown in Figs. 2A and 2B, the first mask features 400 can comprise a titanium nitride layer 402, and a DARC layer 404. The underlying mask layer 300 can comprise any suitable material that can be selectively etched using the first mask features 400 as a mask. For example, the underlying mask layer 300 may contain tungsten, while the first mask features 400 comprise titanium nitride. Layer 300 may comprise other materials, such as silicon oxide, an organic material or amorphous carbon (APF).

[0016] The underlying mask features 302 can be formed by undercut the underlying mask layer 300. In some embodiments, the step of undercutting can be a step of selectively wet etching the underlying mask layer 300 using the first mask features 400 as a mask. Optionally, a step of dry etching the underlying mask layer 300 using the first mask features 400 as a mask, may be conducted prior to the wet etching. The resulting structure after the undercutting step is shown in Figs. 3A (top view), 3B (cross-sectional view along the section line 1), and 3C (cross-sectional view along the

section line 2). The openings 306 formed during the step of the undercutting, as illustrated in Figs. 3B and 3C, partially expose the underlying layer 200 that is located underneath the first mask features 400.

[0017] The first mask features 400 can then be removed, resulting in a structure shown in Figs. 4A (top view), and 4B (cross-sectional view along the section line 1). The underlying mask features 302 can be used as a mask in a following step of etching the underlying layer 200. Features 302 may have a sublithographic size due to the undercutting.

[0018] Alternatively, as shown in Fig. 5A and 5B, prior to the step of removing the first mask features 400, filler features 304 can be formed between the underlying mask features 302 and over the underlying layer 200, using the first mask features 400 as a mask, in such a way that the filler features 304 do not contact the underlying mask features 302.

[0019] The step of forming the filler features 304 can comprise depositing a filler layer over the underlying layer 200 and over and between the first mask features 400, and planarizing, such as chemical mechanical polishing the filler layer using the top of the first mask features 400 as a polish stop. This results in a structure illustrated in Figs. 5A (top view), and 5B (cross-sectional view along the section line 1). The first mask features 400 (and optionally the upper portions of the filler features 304) can then be removed by etching or CMP methods, to form a structure illustrated in Figs. 6A (top view), and 6B (cross-sectional view along the section line 1). Alternatively, the steps of forming filler features 304 and removing the first mask features 400 comprises depositing a filler layer over the underlying layer 200 and over and between the first mask features 400, and chemical mechanical polishing the filler layer and the first mask features using the top of the underlying mask features 302 as a polish stop. In this embodiment, a plurality of cylindrical underlying mask features 302 and right angle parallelepiped shaped filler features 304 are formed. In the specific layout of Fig. 6A, each feature 302 is surrounded by four equidistant features 304 and vise-versa.

[0020] Turning to Fig. 7A (top view), and 7B (cross-sectional view along the section line 1), the underlying layer 200 can then be patterned using at least a combination of the underlying mask features 302 and the filler features 304 as a mask, forming an array of pillars 110. In this embodiment, a plurality of cylindrical pillars and right angle parallelepiped pillars are formed using respective features 302 and 304 as a mask. In the specific layout of Fig. 7A, each cylindrical pillar is surrounded by four equidistant parallelepiped pillars and vise-versa.

[0021] In some embodiments, the underlying layer 200 comprises at least one semiconductor layer, and the step of patterning the underlying layer 200 forms an array of semiconductor pillars 110. For example, layer 200 may comprise a p-type and n-type semiconductor layers to form a p-n diode pillar 110 diode. Alternatively, layer 200 may comprise p-type, intrinsic and n-type layers to form a p-i-n pillar 110 diode.

[0022] The diode 110 may be a steering element of a memory cell, for example, a memory cell 1 illustrated in Fig. 9, which further includes a storage element. The storage element may comprise a resistivity switching element. The resistivity switching element can be an antifuse dielectric, such as a metal oxide dielectric layer or another element, and the diode and the antifuse dielectric layer can be arranged in series (with the diode being above or below the dielectric). The storage element may be patterned together with the steering element or it may be formed over the steering element after the etching step. For example, the antifuse dielectric may be formed by oxidizing an upper portion of a semiconductor diode 110.

[0023] In some other embodiments, the underlying layer 200 comprises a resistivity switching storage element layer 118 and a bottom hard mask layer 208 over the resistivity storage element layer 118. A structure shown in Fig. 8A can be obtained, by etching the underlying layer 200 using at least the underlying mask features 302 (or the combination of the underlying mask features 302 and the filler features 304 in some embodiments) as a mask. Alternatively, the underlying layer 200 can be partially etched. For example, the step of etching the underlying layer 200 may use the top of the resistivity switching storage element layer 118 as a stop, therefore, only the bottom hard mask layer 208 is etched.

[0024] The resistivity switching element layer 118 can contain a metal-insulator-metal stack 200 that comprises a first electrically conductive layer 202, an insulating layer 204 over the first electrically conductive layer 202, and a second electrically conductive layer 206, as shown in Fig. 8A. Any suitable conductive material can be used for the first 202 and second 206 conductive layers, for example, tungsten, aluminum, copper, or alloys thereof. The insulating layer 204 can be an antifuse dielectric layer selected from a group consisting of hafnium oxide, aluminum oxide, titanium oxide, lanthanum oxide, tantalum oxide, ruthenium oxide, zirconium silicon oxide, aluminum silicon oxide, hafnium silicon oxide, hafnium aluminum oxide, hafnium silicon oxynitride, zirconium silicon aluminum oxide, hafnium aluminum silicon oxide, hafnium aluminum silicon oxynitride, zirconium silicon aluminum oxynitride, silicon oxide, silicon nitride, or a combination thereof. The bottom hard mask layer can comprise any suitable hard mask material, such as silicon oxide or silicon nitride. In a preferred embodiment, the bottom hard mask layer comprises an organic hard mask layer.

[0025] Tuning to Fig. 8B, the first openings 209, which are formed by the step of etching the underlying layer 200, can be filled by an insulating material 502. Any suitable insulating material can be used for the insulating layer 512, for example silicon oxide, silicon nitride, high-dielectric constant film, Si-C-O-H film, or a combination thereof.

[0026] The bottom hard mask layer 208 can then be removed, as shown in Fig. 8C, forming second openings 504 exposing top of the resistivity switching storage element layer 118. The second openings 504 can then be filled with at least one semiconductor material to form semiconductor diodes 110, as shown in Fig. 8D, having a substantially pillar shape. The diodes 110 may be a steering element of a memory cell, for example the memory cell 1 illustrated in Fig. 9.

[0027] The semiconductor diodes 110 may be formed by selectively growing the semiconductor material in the second openings 504, or by depositing the semiconductor material in the second openings 504 and over the insulating layer 502 and planarized by CMP or etchback. For a p-n diode, the p-type and the n-type layers may be deposited and/or selectively grown. For a p-i-n diode, the upper diode region,

such as the p-type region, may be formed by implanting suitable dopants into the upper portion of the intrinsic region.

[0028] The memory cell can be further located in a monolithic three dimensional array of memory cells. The memory cell can be a read / write memory cell or a rewritable memory cell. The memory cell type can be selected from at least one of antifuse, fuse, polysilicon memory effect cell, metal oxide memory, switchable complex metal oxide, carbon nanotube memory, graphene, amorphous or polycrystalline carbon switchable resistance material, phase change material memory, conductive bridge element, or switchable polymer memory. U.S. Application Numbers 11/864532 and 11/819,595, U.S. Published Application Numbers US 2007/0164309 A1 and US 2007/0072360 A1, and U.S. Patent Numbers 6,946,719, 6,952,030, 6,853,049, disclosing memory cells and methods of making and/or using thereof, are hereby incorporated by reference in their entirety.

[0029] In preferred embodiments, the memory cell includes a cylindrical semiconductor diode located in series with the storage element. The diode and the storage element are disposed between two electrodes, as illustrated in Figure 9. The diode and the storage element may have a shape other than cylindrical, such as the parallelepiped shape described above, if desired. For a detailed description of a the design of a memory cell comprising a diode and a metal oxide, see for example US Patent Application No. 11/125,939 filed on May 9, 2005 (which corresponds to US Published Application No. 2006/0250836 to Herner et al.), and US Patent Application No 11/395,995 filed on March 31, 2006 (which corresponds to US Patent Published Application No. 2006/0250837 to Herner et al.), each of which is hereby incorporated by reference. In the preferred embodiments of the invention, the storage element serves as the resistivity switching element and the diode as the steering element of the memory cell.

[0030] As a non-limiting example, Figure 9 illustrates the perspective view of a memory cell formed according to a preferred embodiment of the present invention. A bottom conductor 101 is formed of a conductive material, for example tungsten, and extends in a first direction. Barrier and adhesion layers, such as TiN layers, may be included in bottom conductor 101. The semiconductor diode 110 has a bottom

heavily doped n-type region 112; an intrinsic region 114, which is not intentionally doped; and a top heavily doped p-type region 116, though the orientation of this diode may be reversed. Such a diode, regardless of its orientation, will be referred to as a p-i-n diode or simply diode. The resistivity switching layer 118 is disposed on the diode, either on the p-type region 116 or below the n-region 112 of the diode 110. Top conductor 102 may be formed in the same manner and of the same materials as bottom conductor 101, and extends in a second direction different from the first direction. The semiconductor diode 110 is vertically disposed between bottom conductor 101 and top conductor 102. The diode can comprise any single crystal, polycrystalline, or amorphous semiconductor material, such as silicon, germanium, or silicon-germanium alloys.

[0031] The above described memory cell shown in Figure 9 may be located in a one memory level device. If desired, additional memory levels can be formed above the first memory level to form a monolithic three dimensional memory array. In some embodiments, conductors can be shared between memory levels; i.e. top conductor 102 shown in Figure 9 would serve as the bottom conductor of the next memory level. In other embodiments, an interlevel dielectric is formed above the first memory level, its surface planarized, and construction of a second memory level begins on this planarized interlevel dielectric, with no shared conductors.

[0032] A monolithic three dimensional memory array is one in which multiple memory levels are formed above a single substrate, such as a wafer, with no intervening substrates. The layers forming one memory level are deposited or grown directly over the layers of an existing level or levels. In contrast, stacked memories have been constructed by forming memory levels on separate substrates and adhering the memory levels atop each other, as in Leedy, US Patent No. 5,915,167, "Three dimensional structure memory." The substrates may be thinned or removed from the memory levels before bonding, but as the memory levels are initially formed over separate substrates, such memories are not true monolithic three dimensional memory arrays.

[0033] A monolithic three dimensional memory array formed above a substrate comprises at least a first memory level formed at a first height above the substrate and

a second memory level formed at a second height different from the first height. Three, four, eight, or indeed any number of memory levels can be formed above the substrate in such a multilevel array.

[0034] Based upon the teachings of this disclosure, it is expected that one of ordinary skill in the art will be readily able to practice the present invention. The descriptions of the various embodiments provided herein are believed to provide ample insight and details of the present invention to enable one of ordinary skill to practice the invention. Although certain supporting circuits and fabrication steps are not specifically described, such circuits and protocols are well known, and no particular advantage is afforded by specific variations of such steps in the context of practicing this invention. Moreover, it is believed that one of ordinary skill in the art, equipped with the teaching of this disclosure, will be able to carry out the invention without undue experimentation.

[0035] The foregoing details description has described only a few of the many possible implementations of the present invention. For this reason, this detailed description is intended by way of illustration, and not by way of limitations. Variations and modifications of the embodiments disclosed herein may be made based on the description set forth herein, without departing from the scope and spirit of the invention. It is only the following claims, including all equivalents, that are intended to define the scope of this invention.

WHAT IS CLAIMED IS:

1. A method of making a device, comprising:

forming an underlying mask layer over an underlying layer;

forming a first mask layer over the underlying mask layer;

patterning the first mask layer to form first mask features;

undercutting the underlying mask layer to form underlying mask features using the first mask features as a mask;

removing the first mask features; and

patterning the underlying layer using at least the underlying mask features as a mask.

2. The method of claim 1, wherein:

the method further comprises:

forming a photoresist layer over the first mask layer; and

patterning the photoresist layer to form a photoresist pattern; and

the step of patterning the first mask layer uses the photoresist pattern as a mask.

3. The method of claim 1, wherein undercutting the underlying mask layer comprises wet etching the underlying mask layer.

4. The method of claim 3, wherein undercutting the underlying mask layer further comprises dry etching the underlying mask layer using the first mask features as a mask, prior to the step of wet etching.

5. The method of claim 1, wherein:

the underlying mask layer comprises tungsten; and

the first mask layer comprises a BARC layer, a DARC layer, a titanium nitride layer, or a combination thereof.

6. The method of claim 1, wherein the first mask features comprise sub-resolution features which contact with each other.

7. The method of claim 1, wherein the underlying layer is selected from a group consisting of an organic hard mask layer, an oxide hard mask layer, a device layer, or combinations thereof.

8. The method of claim 7, wherein:
the device layer comprises at least one semiconductor layer; and
the step of patterning the device layer forms an array of semiconductor pillars.

9. The method of claim 8, wherein
each semiconductor pillar in the array of semiconductor pillars comprises a diode; and
the diode is a steering element of a memory cell and wherein the memory cell further comprises a storage element.

10. The method of claim 9, wherein the memory cell type is selected from at least one of antifuse, fuse, polysilicon memory effect cell, metal oxide memory, switchable complex metal oxide, carbon nanotube memory, graphene or polycrystalline carbon switchable resistance material, phase change material memory, conductive bridge element, or switchable polymer memory.

11. The method of claim 9, wherein the storage element comprises a resistivity switching element.

12. The method of claim 9, wherein the memory cell is a read / write memory cell or a rewritable memory cell.

13. The method of claim 9, wherein the memory cell is located in a monolithic three dimensional array of memory cells.

14. A method of making a device, comprising:
forming an underlying mask layer over an underlying layer;
forming a first mask layer over the underlying mask layer;
patterning the first mask layer to form first mask features;

undercutting the underlying mask layer to form underlying mask features using the first mask features as a mask;

forming filler features between the underlying mask features and over the underlying layer using the first mask features as a mask, wherein the filler features do not contact the underlying mask features;

removing the first mask features; and

patterning the underlying layer using at least a combination of the underlying mask features and filler features as a mask.

15. The method of claim 14, wherein:

the method further comprises:

forming a photoresist layer over the first mask layer; and

patterning the photoresist layer to form a photoresist pattern; and

the step of patterning the first mask layer uses the photoresist pattern as a mask.

16. The method of claim 14, wherein the step of forming the filler features comprises:

depositing a filler layer over the underlying layer and the first mask features, wherein the filler features do not contact the underlying mask features; and

chemical mechanical polishing the filler layer to expose top of the first mask features.

17. The method of claim 14, wherein the steps of forming filler features and removing the first mask features comprise:

depositing a filler layer over the underlying layer and the first mask features; and

chemical mechanical planarizing the filler layer and the first mask features to expose top of the underlying mask features.

18. The method of claim 14, wherein undercutting the underlying mask comprises wet etching the underlying mask layer.

19. The method of claim 18, wherein undercutting the underlying mask layer further comprises dry etching the underlying mask layer using the first mask features as a mask prior to the step of wet etching.

20. The method of claim 14, wherein the first mask layer comprises a BARC layer, a DARC layer, a titanium nitride layer, or a combination thereof.

21. A method of making a device, comprising:

forming an underlying mask layer over an underlying layer, wherein the underlying layer comprises a resistivity switching storage element layer and a bottom hard mask layer over the resistivity storage element layer;

forming a first mask layer over the underlying mask layer;

patterning the first mask layer to form first mask features;

undercutting the underlying mask layer to form underlying mask features using the first mask features as a mask;

removing the first mask features;

etching the bottom hard mask layer using at least the underlying mask features as a mask to form first openings;

filling the first openings with an insulating material;

removing the underlying mask features;

removing the bottom hard mask layer to form second openings exposing top of the resistivity switching storage element layer; and

filling the second openings with at least one semiconductor material to form semiconductor diodes having a substantially pillar shape in the second openings.

22. The method of claim 21, wherein:

the method further comprises:

forming a photoresist layer over the first mask layer; and

patterning the photoresist layer to form a photoresist pattern; and

the step of patterning the first mask layer uses the photoresist pattern as a mask.

23. The method of claim 21, wherein the resistivity switching element layer comprises a metal-insulator-metal stack.

24. The method of claim 21, wherein the bottom hard mask layer comprises an organic hard mask layer.

25. The method of claim 21, wherein undercutting the underlying mask layer comprises wet etching the underlying mask layer.

26. The method of claim 25, wherein undercutting the underlying mask layer further comprises dry etching the underlying mask layer using the first mask features as a mask prior to the step of wet etching.

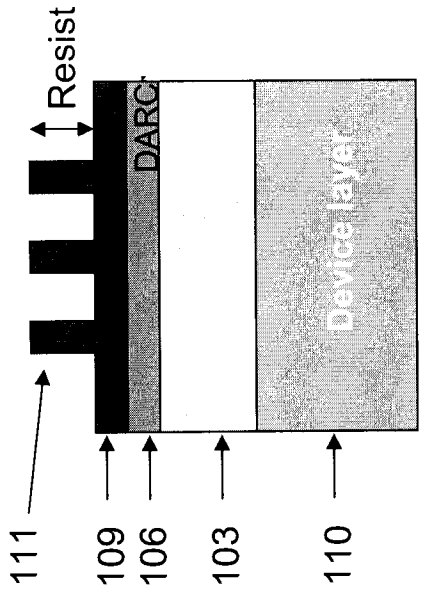


Figure 1A (Prior Art)

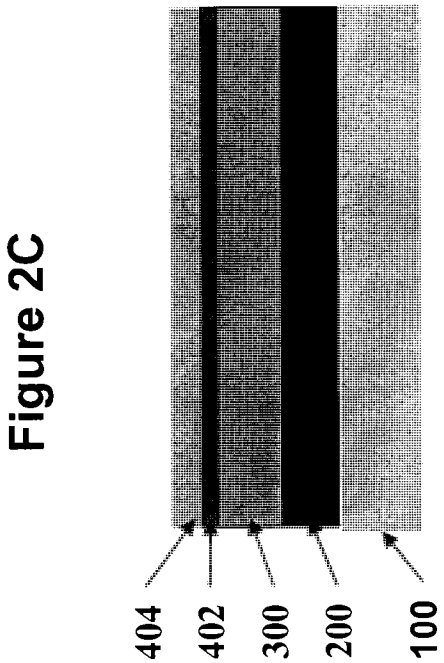


Figure 2C

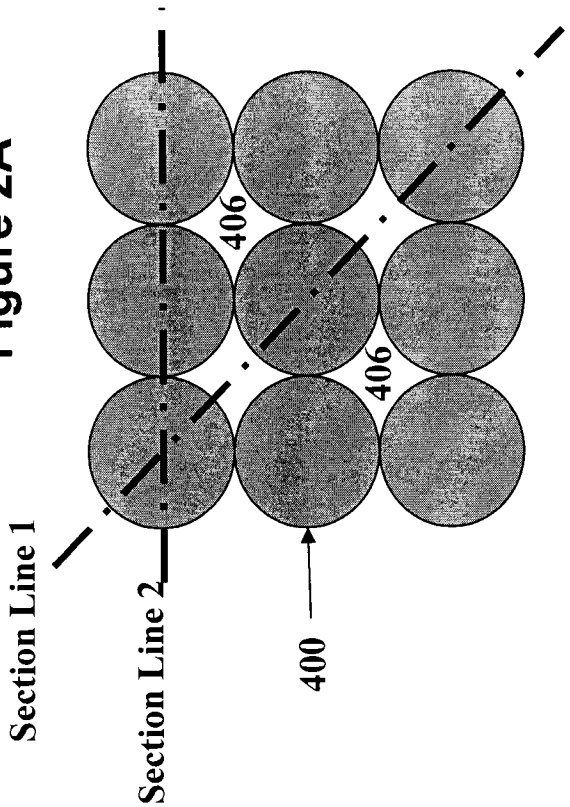


Figure 2A

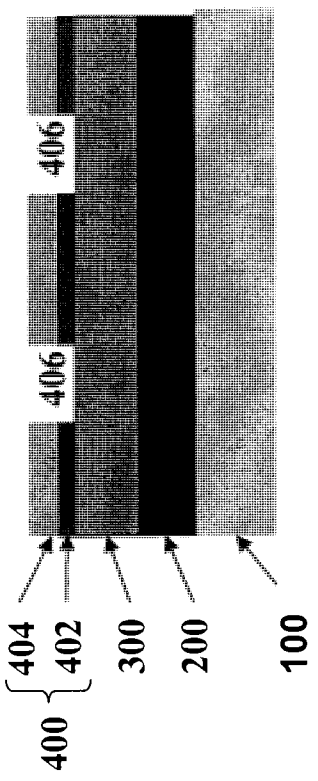


Figure 2B

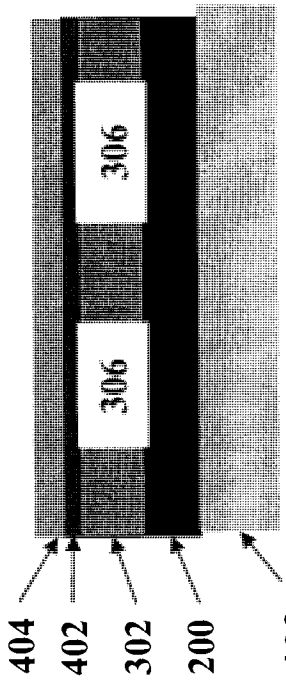


Figure 3C

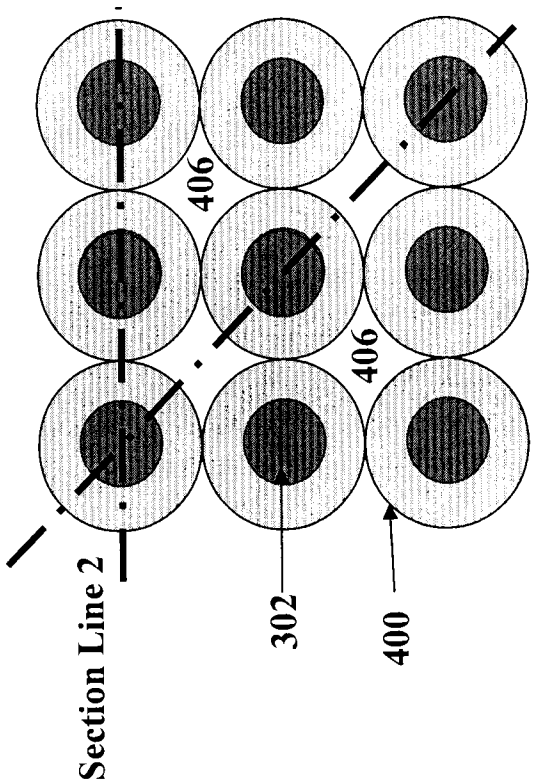


Figure 3A

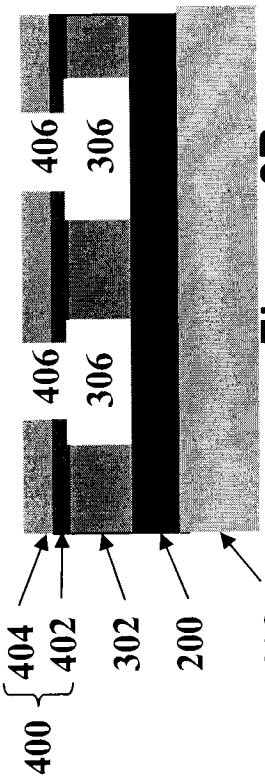


Figure 3B

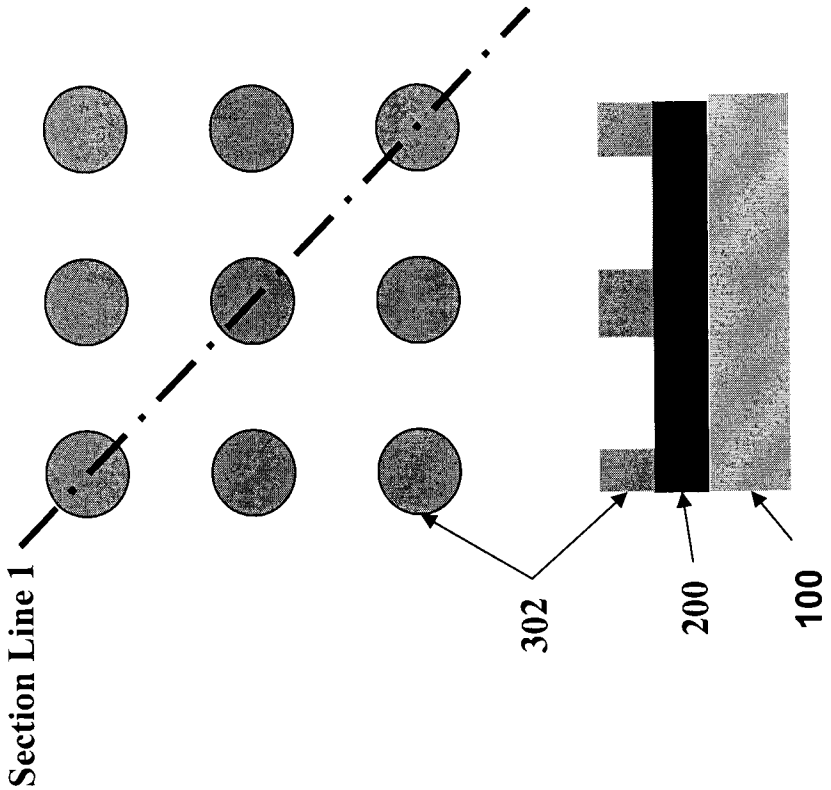
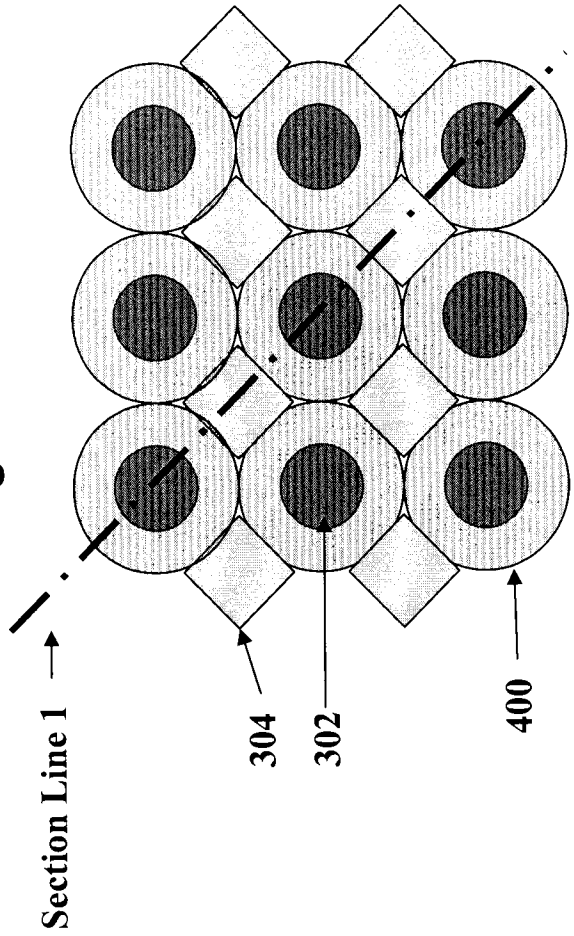


Figure 4A

Figure 4B

Figure 5A



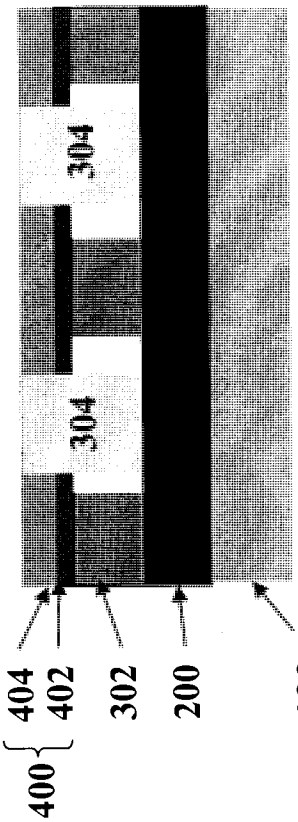


Figure 5B

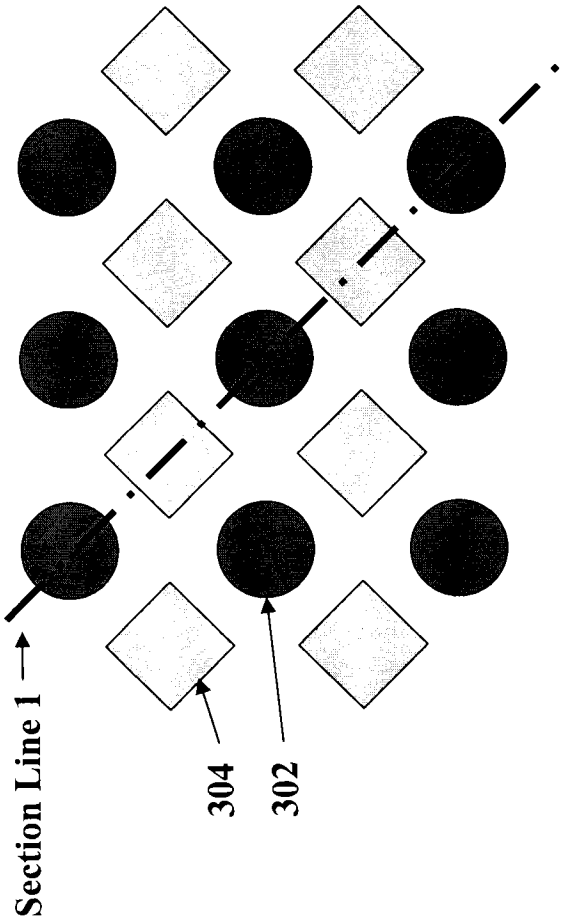


Figure 6A

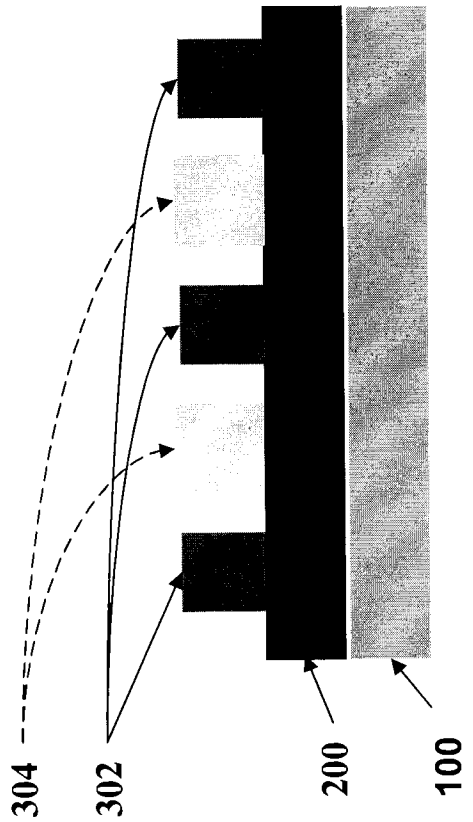


Figure 6B

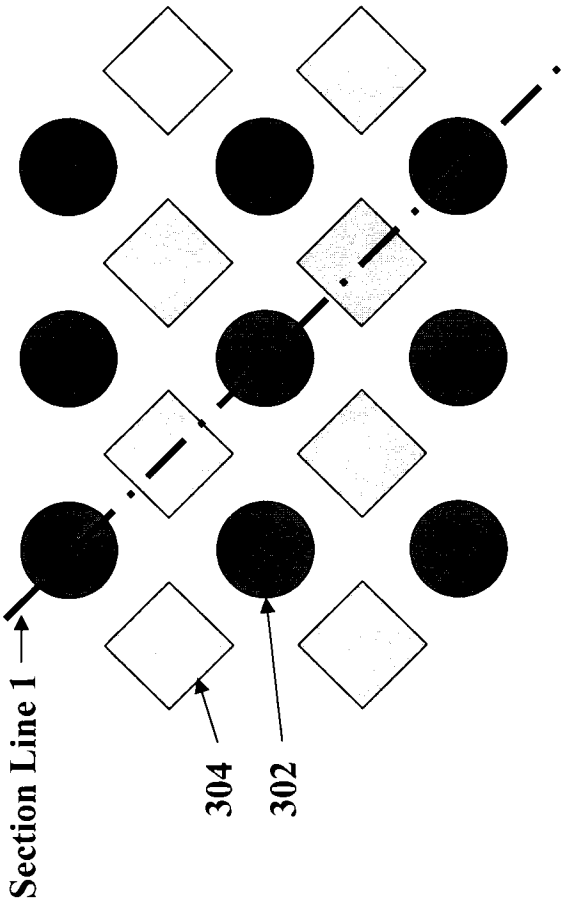


Figure 7A

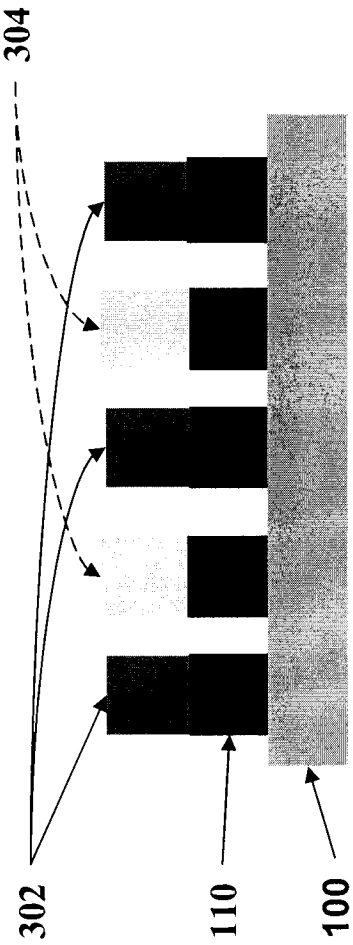


Figure 7B

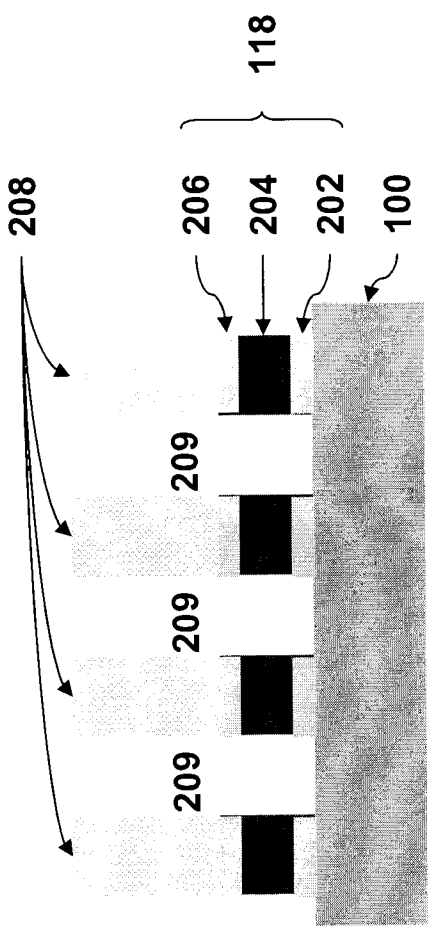


Figure 8A

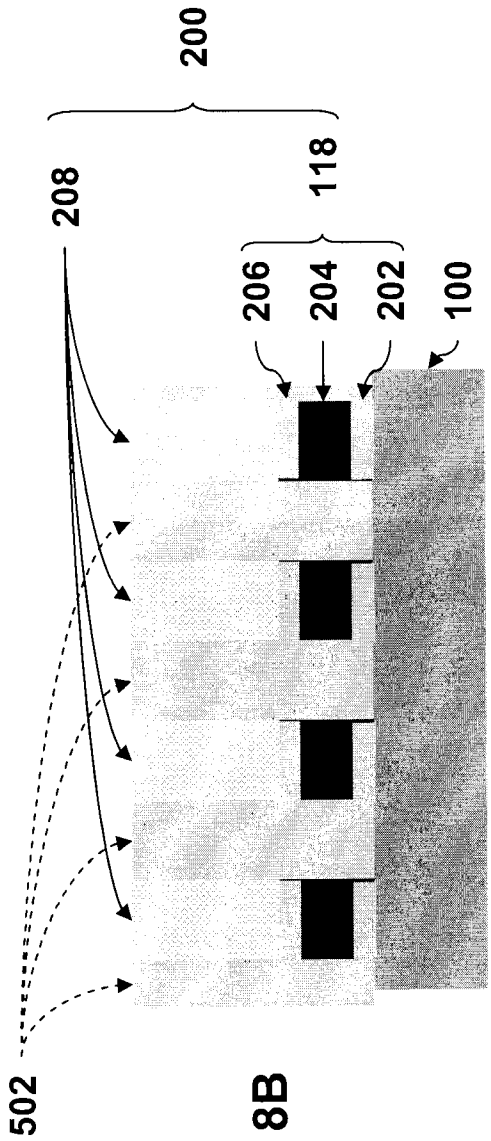


Figure 8B

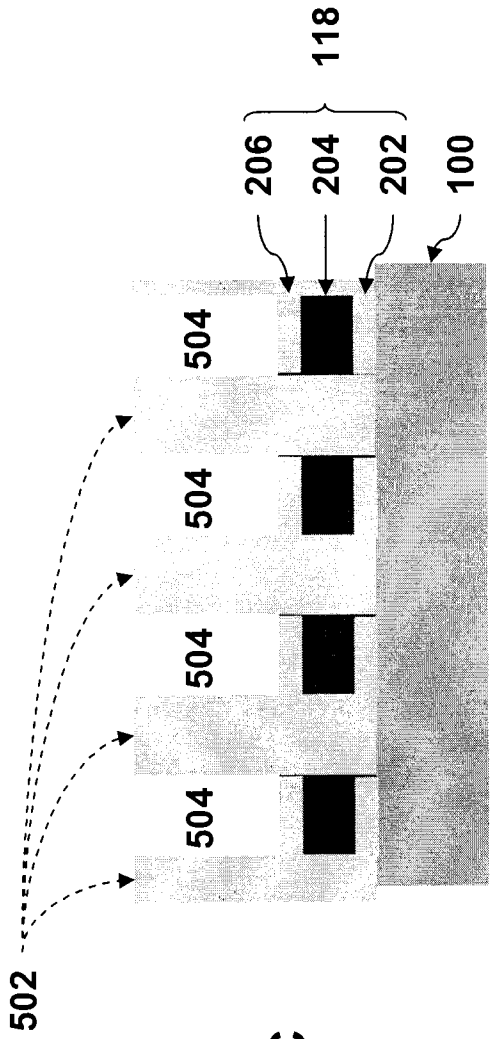


Figure 8C

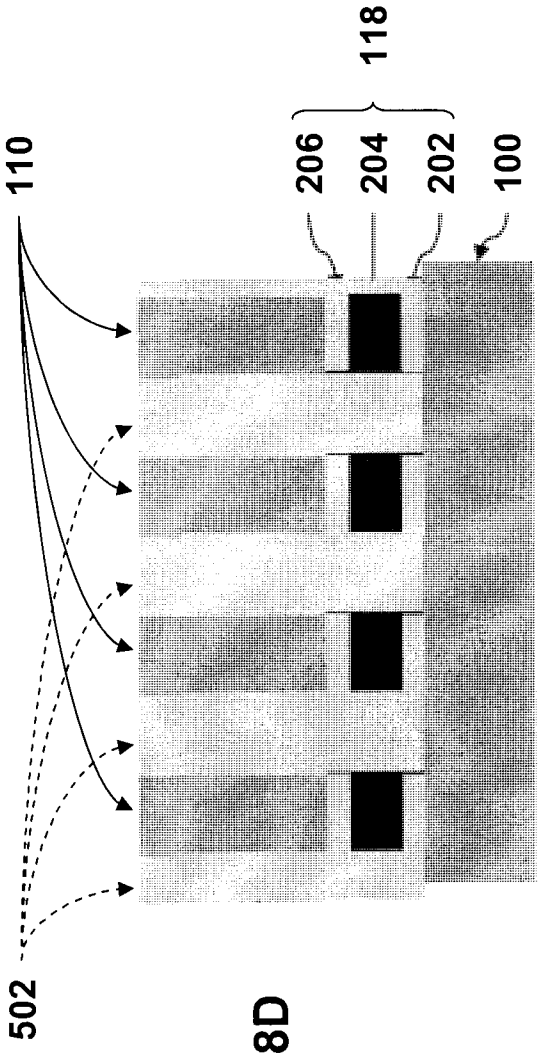


Figure 8D

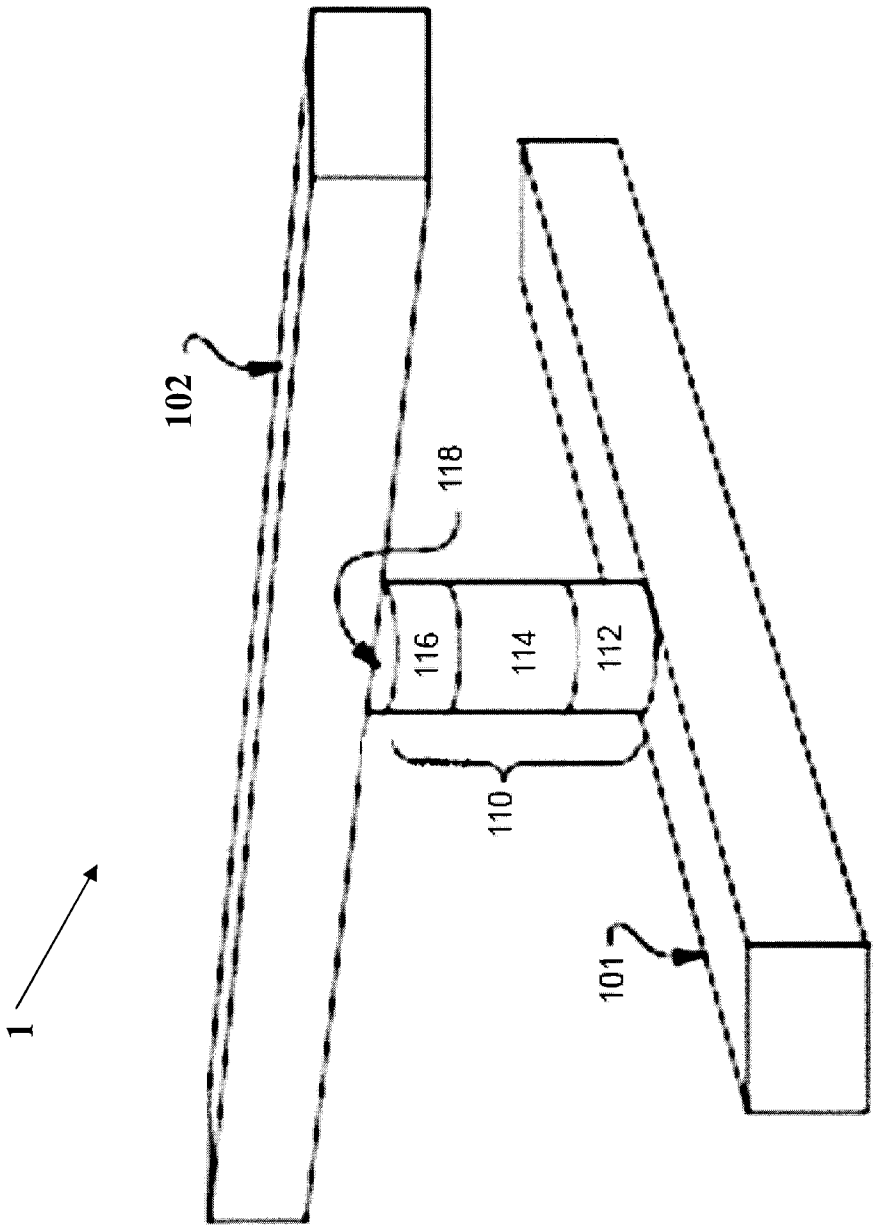


Figure 9

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2009/059188

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L21/027 H01L21/033

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2008/128867 A1 (LEE SANG-UK [KR]) 5 June 2008 (2008-06-05) paragraphs [0001], [0008], [0011] - [0018]; figures 5-10	1
X	WO 2007/103343 A (MICRON TECHNOLOGY INC [US]; ABATCHEV MIRZAFER K [US]; SUBRAMANIAN KRUP) 13 September 2007 (2007-09-13) paragraphs [0007] - [0019], [0034] - [0050], [0059], [0065], [0068] - [0071], [0077]; figures 2A-2C,3A,3B	1-6
X	US 2006/177977 A1 (CHAN PHILIP C H [CN] ET AL) 10 August 2006 (2006-08-10) paragraphs [0002], [0010] - [0013], [0017] - [0020], [0042] - [0050]; figures 2-5	1-6

-/--

[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
15 December 2009	04/03/2010

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Keller, Jan

Form PCT/ISA/210 (second sheet) (April 2005)

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2009/059188

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 6 096 659 A (GARDNER MARK I [US] ET AL) 1 August 2000 (2000-08-01) column 2, lines 9-35 column 3, line 1 - column 4, line 49 figures 2A-2D -----	1

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2009/059188

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

see additional sheet

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2. ☐ As all searchable claims could be searched without effort justifying an additional fees, this Authority did not invite payment of additional fees.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☒ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

1-6

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.

☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.

☐ No protest accompanied the payment of additional search fees.

FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

This International Searching Authority found multiple (groups of) inventions in this international application, as follows:

1. claims: 1-6

Method of making a multilayer mask system for patterning a layer comprising undercutting a first mask layer to increase resolution of the photoresist structures

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2. claims: 7-13

Method of patterning a device layer

---

3. claims: 14-20

Method of making a multilayer mask system comprising undercutting a first mask layer and forming filler features to increase resolution of the photoresist structures

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4. claims: 21-26

Method of forming select devices (diodes) for resistive switching storage elements and the according insulation in between the select devices

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/US2009/059188

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2008128867 A1	05-06-2008	CN 101197257 A	11-06-2008
WO 2007103343 A	13-09-2007	CN 101421824 A	29-04-2009
		EP 2002465 A1	17-12-2008
		JP 2009529784 T	20-08-2009
		KR 20080112281 A	24-12-2008
		US 2007212889 A1	13-09-2007
US 2006177977 A1	10-08-2006	NONE	
US 6096659 A	01-08-2000	NONE	