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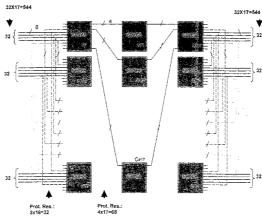
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(54) Title: THREE-STAGE NON-BLOCKING FAULT TOLERANT CROSS-CONNECT ARCHITECTURE



(57) Abstract: The invention concerns an electro and/or optical cross-connect core (E/OXC) in telecommunications, of the kind employing cross bars switch elements and/or selectors as building blocks and a three stage, SSNB, WSNB or RNB interconnecting architecture with suitable input and output cross connections, in order to provide a fault protection with protection ratio 1:N. According to the invention the elementary input and output matrices of the cross-connect core involve protection resources consisting of additional input/output channels; in that said additional protection channels are interconnected with the ordinary input/output channels of each elementary matrix; and in that the size of each of the matrices in the central stage is equal or smaller than the one required to provide a 1:N protection generated by each input/output matrix connected thereto. The cooperation among the elementary matrices to solve the fault of one of them can be controlled only by firmware and the size of the central stage can be determined only depending on he number of ordinary ports and of the chosen protection redundancy (1:N), both for input/output ports and for protection ports, so as to allow the undisturbed restoring of the connections interrupted by the fault and the matrix substitution, still without disturbs.



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THREE-STAGE NON-BLOCKING FAULT TOLERANT CROSS-CONNECT ARCHITECTURE

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This invention refers to an electro and/or optical cross connect core (E/OXC), which uses a three-stage architecture and which is able to ensure a fault protection with a protection ratio 1:N.

It is well-known that the next generation of Optical Transport Networks (OTN) have to provide global transport for circuit and packet switching services and particularly for IP services. OTN's will have to provide paths for light delivery and automatic routing and restoration thereof. To achieve that in an effective way, the Optical Transport Network needs to be flexible, reliable, reconfigurable, scalable and cost effective.

To provide flexibility and reconfigurability, optical cross connects (OXC's) have been developed an introduced in the OTN through which high capacity data streams are routed through the optical path layer. It is desirable that the OXC operations are independent of client signal (i.e. of signal bit rate and signal characteristics) and protocol.

Optical Cross-Connects have to be scalable and expandable, i.e. starting from a basic OXC size with a certain number of ports, it should be possible to easily reduce or expand the OXC size by reducing or increasing the number of boards.

Cost effectiveness requires a modular OXC implementation, i.e. all the boards constituting the OXC core have to be the same or of a few similar kinds.

Reliability implies that OTN provide some form of automatic protection and restoration of interrupted lightpaths in case of fault, with a minimal impact over the other concurring services. That has to be provided by the OXC architecture possibly even through other Network Elements (network topology, Routing Protocols etc.) which may concur in achieving reliability goals. The same reason implies that Fully Non-Blocking or Wide Sense Non-Blocking operation is required in all the possible OXC status.

A usual requirement for this aspect is that the OXC must provide full protection and restoration of the services under every single fault condition. In this context, single fault can be regarded as the minimum hardware or software element that can reliably monitored and substituted in its function (e.g. a PBA or a Module). Module replacement should be hitless too.

Most of the OXC implementations uses electronic or optical Cross-Bar elementary switch matrices as OXC internal building blocks and, in this context, fig. 1 in the annexed drawings shows a possible optical cross-connect architecture to which this invention can be applied. A comb 1 of channels having high capacity wavelength is transported on each input fibre 2. All of these optical signals are demultiplexed in 3 before entering the E/OXC 4. The cross-connect 4 is one of the basic elements in the architecture, since most characteristics of OXC's depend on its features.

When the implementations of optical cross-connect core use, as internal E/OXC building blocks, electronic or optical elementary switch matrices which are commercially available, such matrices are usually "square" (input and output array have the same length), presently with a size like 68x68 or smaller due to technological reasons. However, the invention applies also to rectangular matrices.

Conventional OXC design achieves strictly non blocking characteristic by using in its core (that is the central stage switch array) the well known three stage architecture fully connected. It is built by interconnecting a large number of smaller size switch elements, usually commercially available.

This design allows non-blocking feature because it is capable to route each of the N OXC core inputs in a NxN OXC, using the number of matrix elements effectively, at the cost of a reduction of the scalability characteristic.

This is due to the intricate nets linking each of central elementary modules to each of input/output stage module. Some solution have been proposed to relieve the scalability problem, but this circumstance has also prevented to find an acceptable I to N protection approach: it is in fact very difficult to imagine how a spare resource can be shared by different working OXC elements and used, in case of fault, unless incongruous (and fault prone) selection tree switch arrays are added. For this reason, no implementation of I to N protection is nowadays available, at the best of applicant's knowledge, and protection strategies offered for large Cross-Connects contemplate only 1+1 or 1:1 protection, as shown in Fig. 2.

The problem is now solved by the present invention, which provides a crossconnect core of new concept, utilising cross-bar switch elements as building blocks and a three-stage interconnection architecture with appropriate input/output linking, in order to provide a 1:N protection against single fault, with economic and reliability advantages.

More precisely, the invention refers to an electro and/or optical cross-connect core (E/OXC) in the telecommunications, of the kind employing as building blocks cross-bar switch elements and/or selectors and a three-stage interconnection architecture, with appropriate input and output cross-linkings, in order to ensure a 1:N protection against single faults, characterised in that input and output element matrices in the cross-connect core show protection resources consisting of additional input/output channels; in that said additional protection channels are interconnected to the usual input/output channels of each matrix element; and in that the size of each matrix of the central stage is equal or smaller than the one required to provide the 1:N protection load generated by each input/output matrix connected thereto.

In this cross-connect core the cooperation among the elementary matrices, in order to solve the fault of one of them, is exclusively controlled by firmware and the size of the central stage is selected only depending on the number of common ports and of the selected protection ratio (1:N), both for input/output ports and for protection ports, in order to allow undisturbed restoring of connections interrupted because of the fault and the matrix replacement with no disturb.

The invention is now illustrated more in depth, by way of example, for an optical, SSNB (Strict Sense Non Blocking) type cross-connect according to Clos' theorema, with reference to the enclosed drawings, wherein:

- Fig. 1 shows an optical cross-connect architecture (E/OXC), which has already been described above, to which the inventive cross-connect core is applied;
- Fig. 2 shows a connection architecture having 1:1 protection according to the prior art;
- Fig. 3 shows a 20x20 cross-connect architecture, having protection ratio 1:4 according to this invention;
- Fig. 4 shows a possible synthesis of the 8x10 input matrices used in Fig. 3, by using smaller rectangular matrices, and a selector; and

Fig. 5 shows the application of the invention to a cross-connect architecture with 544x544 ports, having a 1:16 protection ratio, due to the use of commercial matrix elements (68x68 instead of 64x64).

As it has been set forth above, the invention consists in: using Input/Output elementary matrices having an amount of protection resource (that is: extra Input/Output channels) and in distributing this resource so that the Input/Output channels of each elementary matrix are interconnected with the protection channels of the other Input/Output elementary matrices; rearranging the interconnections among elementary matrices, in order to cope with the fault of one of them is performed by the Cross-connect firmware, with no extra switch element other than the ones contained in the elementary matrices required to actuate protection; the size of each central core elementary matrix shall be equal smaller to that required for carrying the 1:N protection ratio generated by each Input/Output matrix connected to it; so for example, if the I/O stages connected to the central elementary matrix cover M traffic ports with 1:N protection, so central elementary switch size should be smaller than $2*M/N \times 2*M/N$ in order to satisfy Clos' condition, while in WSNB case (Wide Sense Non Blocking) the maximum size is 1.5M/Nx1.5M/N and in RNB case (Rearrangeable Non Blocking) the maximum size is M/NxM/N; all of this in order to allow an undisturbed restoring of the connections interrupted by the fault and the module replacement.

To illustrate the invention and its cost benefits, consider its application, which is shown in Fig. 3, to a 20x20 cross-connect with 1:4 protection, then comparing the same to the 20x20 cross-connect having protection 1:1, shown in Fig. 2. In Fig. 3 protection inputs/outputs have been drawn in dashed line, in order to make it clear how they are distributed to protect the Cross-Connect inputs/outputs.

As a general rule, the number of inputs/outputs of the lateral stages in the 1:N protected Cross-Connect must be doubled with respect to the non-protected one but the core size must be increased only by 1:N, due to the capacity added for protection purposes.

This is because input/output stages are not used in they full connectivity capability, but only for that required by single fault protection as it is shown in Fig. 4, where an assembly of smaller rectangular matrices 5 and a selector 6 are used. If

purposely built elementary matrices are available and can be assembled, consisting of smaller crossbar matrices and selection tree matrices accordingly to Fig. 4, substantially reduction of conventional cost is obtained, which are determined depending on the number of elementary switchers. However, the implementation choice is a matter to be decided in the specific design process putting into the balance the higher flexibility offered by full crossbar matrices when scalability is to be taken into account and the available switch elements sizes and cost. Furthermore, the cost of elementary switch matrices is determined mainly by market criteria rather than by the only technological complexity.

It is easy to see that the 1:N protected architecture is tolerant against every single fault with a single point fault at level of elementary switch matrix.

To show this fact, it can be observed that, should any input/output matrix fail, its task may be taken over by an equivalent number of protection channels, connected to its inputs/outputs, while the loss of an elementary matrix of the central core implies a connectivity loss equivalent to that required by the protection channels while normal traffic can be still satisfied.

In every case, the connections torn down by the single fault may be restored without affecting the others using the remaining protection resources; subsequent board substitution to restore the OXC full capability is hitless.

The advangages of using the proposed 1:N protection scheme rely on the related Hardware simplification (that is recurring cost reduction and higher reliability) at expense of a slightly more complex Firmware (nonrecurring cost).

A rough measure of the hardware simplification may be obtained by considering the number of single elementary switches, needed in the two alternative protection solutions.

Conventional 20X20, 1:1 protected system: (10x4x8 + 4x10x10)x2 = 1440Inventive 20X20, 1:4 protected system: (10x8x10 + 5x10x10) = 1300 with a saving in conventional costs around 7%

Inventive 20X20, 1:4 protected system accordingly to Fig. 4: $(10(5\times10 + 1\times4) + 5\times10\times10) = 1040$, with a saving of 38%.

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Using integrated crossbar switch arrays (usually manufactured in "square" format; we should employ for instance 10x10 and 8x8 elementary matrices); the advantages becomes apparent:

20X20, 1:1 protected: (10x8x8 + 4x10x10)x2 = 2080

20X20, 1:4 protected: (10x10x10+5x10x10) = 1500

Saving in conventional cost: 28%.

This situation becomes even more favourable when it is considered that many vendors offer matrices with input/output size equal to a power of two plus a small amount (e.g. 68x68, 34x34) for ancillary purposes.

This fact is better exposed in Fig. 5 which shows an application of this invention over a 544x544 Cross-Connected system with 1:16 protection, using 68x68 elementary matrices.

The conventional cost for the 1:1 protected, 544X544 Cross-Connect is:

 $(48\times68\times68)\times2=443904$, while the 1:16 protected Cross-Connect 544x544 shown in Fig. 5 core is: $51\times68\times68=235824$ with a savings of 47%.

CLAIMS

- 1. Electro and/or optical cross-connect core (E/OXC) in telecommunications, of the kind employing cross bars switch elements and/or selectors as building blocks and a three stage, SSNB, WSNB or RNB interconnecting architecture with suitable input and output cross connections, in order to provide a fault protection with protection ratio 1:N, characterised in that the elementary input and output matrices of the cross-connect core involve protection resources consisting of additional input/output channels; in that said additional protection channels are interconnected with the ordinary input/output channels of each elementary matrix; and in that the size of each of the matrices in the central stage is equal or smaller than the one required to provide a 1:N protection generated by each input/output matrix connected thereto.
- 2. Cross-connect core as set forth in claim 1., wherein the cooperation among the elementary matrices to solve the fault of one of them is controlled only by firmware.
- 3. Cross-connect core as set forth in claims 1. and 2., wherein the size of the central stage is determined only depending on the number of ordinary ports and of the chosen protection redundancy (1:N), both for input/output ports and for protection ports, so as to allow the undisturbed restoring of the connections interrupted by the fault and the matrix substitution, still without disturbs.
- 4. Architecture to provide the elementary matrices to be used in input and output stages of the cross-connect core as set forth in claims 1. and 2., characterised in that it employs smaller elementary matrices, joined to a selection tree.

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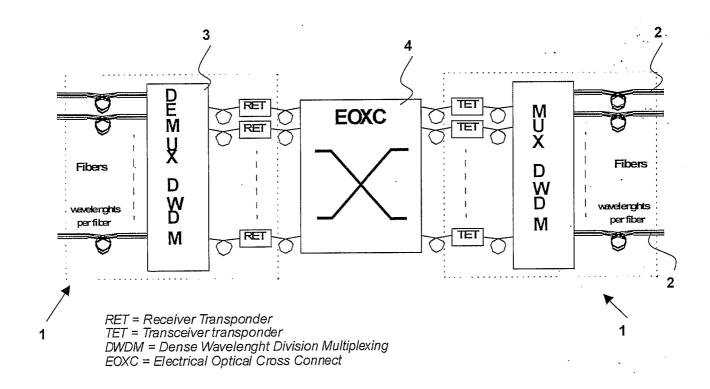


Fig. 1

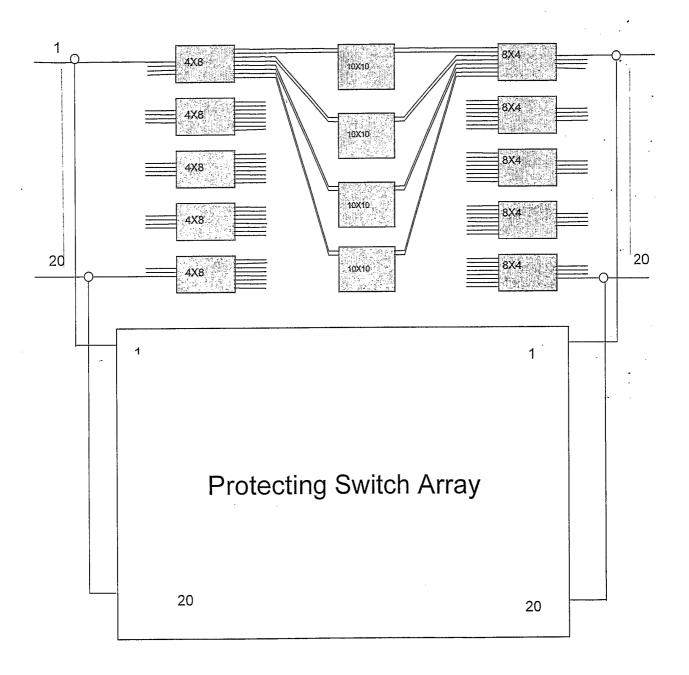


Fig. 2

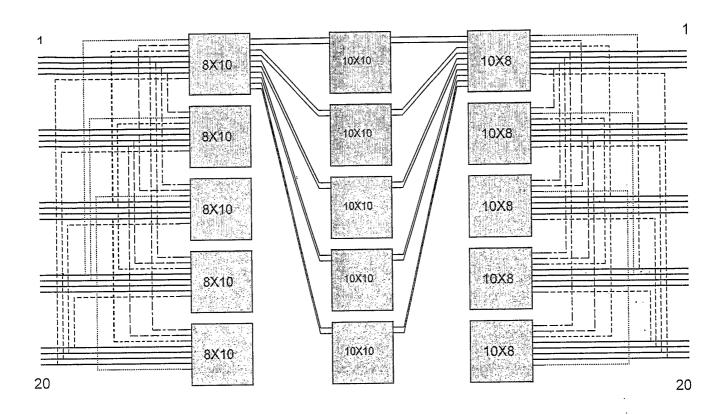


Fig.3

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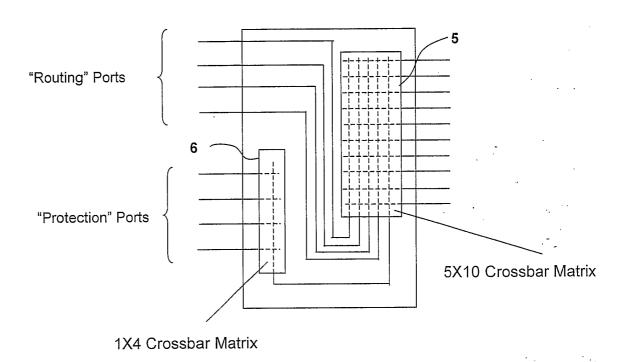


Fig. 4

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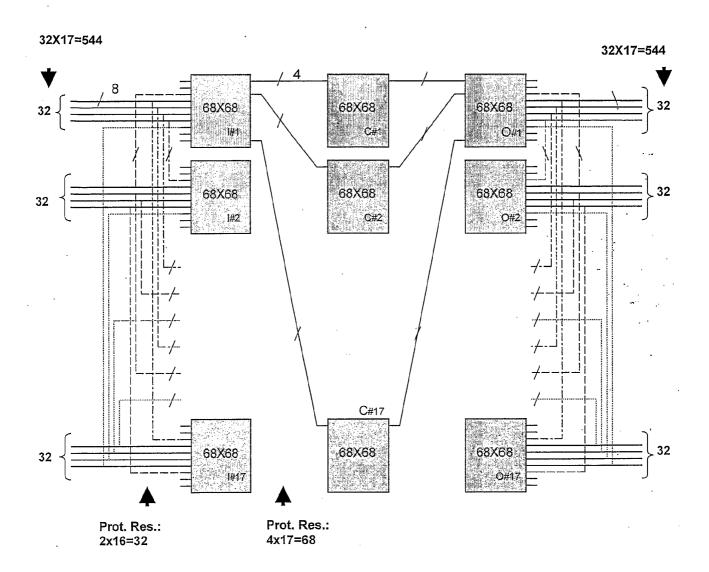


Fig. 5

INTERNATIONAL SEARCH REPORT

In ational Application No
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A. CLASSIFICATION OF SUBJECT MATTER IPC 7 H04L12/56 H04Q11/00 H04Q3/68 According to International Patent Classification (IPC) or to both national classification and IPC **B. FIELDS SEARCHED** Minimum documentation searched (classification system followed by classification symbols) IPC 7 H04L H04Q Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched Electronic data base consulted during the international search (name of data base and, where practical, search terms used) EPO-Internal, WPI Data, PAJ C. DOCUMENTS CONSIDERED TO BE RELEVANT Citation of document, with indication, where appropriate, of the relevant passages Relevant to claim No. χ US 5 229 990 A (TERASLINNA KARI T) 1-4 20 July 1993 (1993-07-20) column 13, line 19 - line 37; figures 1,2 DE 198 05 001 A (BOSCH GMBH ROBERT) A 1-4 12 August 1999 (1999-08-12) the whole document US 4 983 961 A (BRUENLE SIEGFRIED ET AL) 1 - 4A 8 January 1991 (1991-01-08) column 1, line 41 -column 2, line 37 Further documents are listed in the continuation of box C. X Patent family members are listed in annex. χ Special categories of cited documents: "T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the "A" document defining the general state of the art which is not considered to be of particular relevance "E" earlier document but published on or after the international "X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone filing date "L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified) "Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such docu-ments, such combination being obvious to a person skilled in the art. "O" document referring to an oral disclosure, use, exhibition or other means document published prior to the international filing date but later than the priority date claimed "&" document member of the same patent family Date of the actual completion of the international search Date of mailing of the international search report 3 May 2002 15/05/2002 Name and mailing address of the ISA Authorized officer European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016 Meurisse, W

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INTERNATIONAL SEARCH REPORT

Information on patent family members

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