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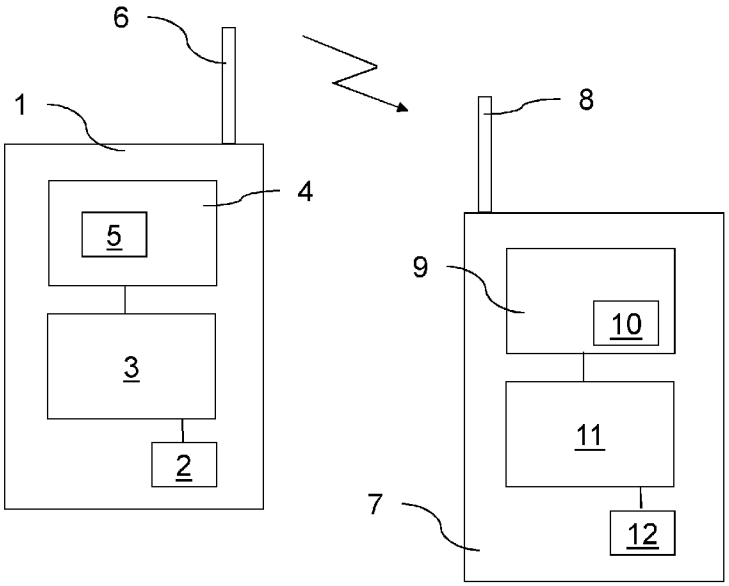

Figure 1

(57) Abstract: A radio transmitter (4) comprises an encoder (5) that receives one or more variable message bits,and encodes each message bit that has a first value as a predetermined first binary chip sequence and encodes each message bit that has the opposite value as a predetermined second binary chip sequence. The radio transmitter (4) transmits data packets, each comprising (i) a predetermined synchronisation portion, comprising one or more instances of the first binary chip sequence, and (ii) a variable data portion, comprising one or more encoded message bits output by the encoder. A radio receiver (9) receives such data packets. It uses the synchronisation portion of a received data packet to perform a frequency and/or timing synchronisation operation, and then decodes message bits from the data portion of the data packet.

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Radio communication

This invention relates to radio transmitters and receivers for communicating binary data.

Various radio communication systems are known for transmitting binary message data. Examples include Bluetooth™ and Bluetooth Low Energy™. It is important for a radio receiver to determine timing synchronisation quickly and accurately from a received data packet, in order to be able to decode the message data reliably. It is known to include a predetermined synchronisation sequence, known in advance to both the transmitter and the receiver, near the beginning of each data packet. The receiver can use this to perform operations such as frequency synchronisation, phase synchronisation, symbol timing estimation, and Automatic Gain Control (AGC) training, before decoding the payload message data.

When a received radio signal is weak (e.g. due to there being considerable distance between the transmitter and the receiver), it can be harder for the receiver to obtain an accurate synchronisation. Trying to mitigate this can lead to significant additional complexity in the radio receiver. The present invention seeks to provide a novel approach that facilitates a particularly efficient radio receiver design with good performance at low signal levels.

From a first aspect, the invention provides a radio transmitter comprising an encoder configured to receive one or more variable message bits and to encode each message bit that has a first value as a predetermined first binary chip sequence and to encode each message bit that has the opposite value as a predetermined second binary chip sequence, wherein the radio transmitter is configured to transmit data packets, each comprising (i) a predetermined synchronisation portion, comprising one or more instances of the first binary chip sequence, and (ii) a variable data portion, comprising one or more encoded message bits output by the encoder.

From a second aspect, the invention provides a radio receiver configured to:

receive data packets, each comprising a predetermined synchronisation portion, comprising one or more instances of a predetermined first binary chip sequence, and a variable data portion, comprising one or more encoded message bits, wherein each message bit that has a first value is encoded as the first binary chip sequence and each message bit that has the opposite value is encoded as a predetermined second binary chip sequence;

use the synchronisation portion of a received data packet to perform a frequency and/or timing synchronisation operation, before decoding the data portion of the data packet; and

decode message bits from the data portion of the data packet.

From a third aspect, the invention provides a radio communication system comprising a radio transmitter and a radio receiver,

wherein the radio transmitter:

comprises an encoder configured to receive one or more variable message bits and to encode each message bit that has a first value as a predetermined first binary chip sequence and to encode each message bit that has the opposite value as a predetermined second binary chip sequence; and

is configured to transmit data packets, each comprising (i) a predetermined synchronisation portion, comprising one or more instances of the first binary chip sequence, and (ii) a variable data portion, comprising one or more encoded message bits output by the encoder,

and wherein the radio receiver is configured to:

receive the data packets transmitted by the radio transmitter;

use the synchronisation portion of a received data packet to perform a frequency and/or timing synchronisation operation, before decoding the data portion of the data packet; and

decode the message bits from the data portion of the data packet.

From a fourth aspect, the invention provides a method of radio communication, comprising:

transmitting a data packet by radio, the data packet comprising (i) a predetermined synchronisation portion, comprising one or more instances of a first binary chip sequence, and (ii) a data portion, comprising one or more encoded message bits, wherein each message bit that has a first value is encoded as a

predetermined first binary chip sequence, and each message bit that has the opposite value is encoded as a predetermined second binary chip sequence,

receiving the data packet;

using the synchronisation portion of the received data packet to perform a frequency and/or timing synchronisation operation; and

decoding the message bits from the data portion of the received data packet.

Thus it will be seen that the same binary chip sequence is used both for synchronisation and for data encoding. This allows for a particularly efficient radio receiver design, because most of the circuitry in the receiver can be shared for both purposes. In particular, the receiver may use a fixed-coefficient correlator for both operations, as explained in more detail below.

In some embodiments, the synchronisation portion and the variable data portion are modulated on a radio carrier wave using frequency-shift-keying (FSK); preferably Gaussian FSK (GFSK); more preferably 2-level GFSK. Where GFSK modulation is used, a modulation index of approximately 0.5 is preferred (preferably within around 20% of 0.5, or more preferably within around 10% of 0.5, such as between around 0.45 and around 0.55). In some embodiments, the radio receiver may be configured to demodulate the received data portion using a differential-binary-phase-shift-keying (DBPSK) demodulator. This is possible because, for suitable first and second binary chip sequences, the transmitted signal, modulated using GFSK, can have qualities of a DBPSK signal. In particular, for suitable sequences, the receiver is able to decode data based on phase differences between portions of successive sequences in the data portion, as is explained in more detail below.

The frequency of the carrier wave may change between successive data packets according to a predetermined frequency-hopping sequence. The radio transmitter and/or receiver may be configured to communicate using a physical layer, and optionally other layers, as defined in a Bluetooth™ specification, such as the Bluetooth™ Low Energy™ Physical Layer Specification section of the Bluetooth™ Core Specification 4.0, published 30 June 2010, or any later version.

The first binary chip sequence may be of any length, but is preferably an even number of bits long, greater or equal to four, It may, for instance, be 4, 8, 16, 24, 32, 48, 64 or

more bits long. In some preferred embodiments it is 16 bits long. The same applies for the second binary chip sequence. The first and second binary chip sequences are preferably the same length as each other.

The first binary chip sequence is preferably phase neutral, when modulated using GFSK; i.e. it is such that the phase of the carrier signal, modulated with the first binary chip sequence, is substantially the same at the start and end of the first binary chip sequence. The second binary chip sequence is preferably also phase neutral. This is advantageous as it allows the radio receiver to identify the first and second binary chip sequences in the data portion more easily, because a constant phase can be assumed to be present at the end of each chip sequence. It can also enable better automatic frequency control on the receiver.

The first binary chip sequence preferably consists of an equal number of zero bits and one bits. The second binary chip sequence preferably also consists of an equal number of zero bits and one bits. This is advantageous as it means that, when using GFSK modulation, any modulation errors automatically cancel out over a sequence, and thus do not need to be estimated or tracked in the receiver.

The second binary chip sequence is preferably equal to the first binary chip sequence except at a number of predetermined bit positions, where it differs. This number is preferably less than half the length of the first binary chip sequence. It is preferably an even number. In some preferred embodiments, the first and second binary chip sequences differ at exactly two bit positions, which are preferably the first and last bit positions. This can allow for the efficient use of a correlator in the radio receiver, as explained in more detail below.

The second binary chip sequence preferably differs from the first binary chip sequence in at least the first and last bit positions. In particularly preferred embodiments, the first and second chip sequences are identical to each other except for the first and last bit positions, at which they differ. The first chip sequence preferably has different binary values in its first and last bit positions (and hence, so does the second sequence, in embodiments in which they differ in the first and last positions). This ensures that the last chip of a sequence in the data portion will have a different value from the first chip in the immediately following sequence whenever the two message bits are the same

as each other (two '1' message bits, or two '0' message bits), and will have the same value whenever the two message bits are different (message bits '1 0', or '0 1'). When using GFSK modulation with a modulation index of approximately 0.5, this gives rise to a phase shift of approximately 0 or approximately π between the middle sections of adjacent sequences (i.e. for the whole sequence except for the first and last bit positions). This is because every '1' bit in the sequence results in a π / 2 positive phase shift, while every '0' results in a π / 2 negative phase shift. The presence or absence of a phase shift between adjacent sequences is determined by the value of the underlying message bits. This allows the radio receiver to decode the message bits simply by determining the phase shifts between successive chip sequences in the data portion of a received packet. No phase shift indicates a repetition of the same message bit, while a phase shift indicates a change of message bit. The radio receiver can use this differential information to decode the underlying message data. It can determine whether the very first message bit should be decoded as a '0' or a '1' based on whether there is a phase change between the first message chip sequence and the last chip sequence of the synchronisation portion. Alternatively, in some embodiments, the message data may already be differentially encoded before it is transmitted by the radio transmitter; in this case, the original data can be determined directly using a differential decoder on the radio receiver.

If the GFSK modulation index is not precisely 0.5, the same approach can still be used, but the phase shift will either be approximately 0 or a value further removed from π (depending on how far the modulation index is away from 0.5).

The first binary chip sequence is preferably such that it has maximum autocorrelation performance, over the set of all possible sequences of a given length, subject to the constraints that the sequence must have an equal number of zero bits and one bits, and that it must have first and last bits that differ in value from each other. This allows the receiver to perform reliable synchronisation timing, by applying a correlation operation to the received synchronisation portion, and also to decode the message bits reliably. Sequences that are do not have this property may nevertheless still be useful. In some embodiments, any sequence having an autocorrelation quality of less than 0.3, or preferably less than 0.28, or more preferably less than 0.26, may be used as the first binary chip sequence, potentially subject to any one or more of the additional constraints mentioned elsewhere herein, where the autocorrelation quality

for a sequence is determined as the ratio of the maximum sidelobe amplitude to the zero-lag peak amplitude, when the sequence is correlated with a pulse train of four sequence-repetitions.

The 16-chip sequence [0 0 0 1 1 0 1 0 1 1 0 0 1 0 1 1], its bitwise complement, the reversed sequence, and the reversed bitwise complement, have been found to provide particularly good performance when used as the first binary chip sequence. Particularly preferred embodiments use one of these sequences. The second binary chip sequence may then be the first chip sequence with the first and last bits flipped; i.e. [1 0 0 1 1 0 1 0 1 1 0 0 1 0 1 0], its bitwise complement, the reversed sequence, or the reversed bitwise complement (respectively).

The predetermined synchronisation portion of the data packets preferably comprises between one or two and around 30 instances of the first binary chip sequence; more preferably between around five and around 30 instances. In some embodiments, it comprises exactly or approximately 15 instances. This is considered to be a particularly good trade-off between (i) having sufficient instances to allow for reliable synchronisation, and to enable any drift correction in the receiver to settle before the data portion arrives, and (ii) keeping the data packets as short as possible to reduce power consumption in the transmitter. The sequences instances in the synchronisation portion preferably follow one immediately after another, without any gaps. The data portion preferably follows after the synchronisation portion without any gap. The receiver is preferable configured to perform drift tracking on at least the synchronisation portion. By including the synchronisation portion and the data portion in the same data packet, with substantially no gap between them, there is no loss of phase information between the two portions, allowing for particularly efficient drift tracking across the whole data packet.

The radio receiver preferably comprises a correlator. The receiver is preferably configured to use the correlator when performing the frequency and/or timing synchronisation operation. The receiver may use the correlator output for frequency ramp tracking; e.g. as part of an Automatic Frequency Control (AFC) loop. The correlator is preferably a fixed-coefficient correlator. This is desirable as it can be implemented in silicon with a relatively small number of gates. Reusing the same correlator for synchronisation and for data correlation leads to a small receiver footprint

and reduced complexity. The correlator may be configured to correlate a received signal with the first binary chip sequence and/or with a sub-sequence thereof. In some embodiments, it may be configured to correlate a received signal with a combination of two or more copies of the first binary chip sequences, when processing the synchronisation portion; for example, it may be a 32-bit correlator and may be configured to correlate the received synchronisation portion with a 32-bit pattern consisting of two copies of a 16-bit first binary chip sequence, one after the other. Such a 32-bit correlator may be simulated by applying suitable processing to the output of a 16-bit correlator. Such a multiple-length correlator is preferably configured to revert to correlating the received signal against a single instance of the first binary chip sequence, or a sub-sequence thereof, when processing the data portion of the received signal.

The correlator is preferably arranged to be able to correlate a received signal with a sub-sequence of the first binary chip sequence. It may be switchable between two modes: a first mode in which is correlates against the complete first binary chip sequence, and a second mode in which it correlates against a sub-sequence of the first binary chip sequence. The sub-sequence is preferably defined by the bit positions at which the first and second binary chip sequences have the same values. The sub-sequence is preferably a contiguous sequence of bits from the first binary chip sequence. For example, where the first chip sequence is a 16-bit sequence, and the second chip sequence differs only at the first and last bit positions, the correlator may be able to correlate against just the middle 14 bits of the sequences when in the first mode. The radio receiver may use the first mode when processing the synchronisation portion of a received data packet, and may switch the correlator to the second mode when decoding message bits from the data portion.

This idea is novel in its own right and, from a further aspect, the invention provides a radio receiver comprising a fixed-coefficient correlator that is switchable between a first mode in which it is configured to correlate a received signal against a binary chip sequence, and a second mode in which it is configured to correlate a received signal against a shorter sub-sequence from the binary chip sequence, wherein the correlator is configured, when in the second mode, to output a signal representative of a phase shift between two successive occurrences of the sub-sequence in a received signal. The radio receiver may be configured to use the output from the correlator to decode

message data from a received signal. Features of the earlier aspects and embodiments may be features of embodiments of this aspect also.

The correlator is preferably configured to output amplitude information. The radio receiver may use this amplitude information to perform symbol timing synchronisation. The correlator is preferably also configured to output phase information. The radio receiver is preferably configured to use this phase information to perform an initial frequency synchronisation. The radio receiver may also be configured to use this information to perform on-going frequency drift tracking, and to apply appropriate adjustment or compensation if the frequency drifts. This is particularly straightforward when, as in preferred embodiments, the binary chip sequences are phase neutral, since the phase should always return to zero after each sequence, unless there is frequency drift.

The radio receiver is preferably arranged to use the correlator to determine whether a sub-sequence in the data portion of a received data packet has an approximately 0 or an approximately π phase change relative to the immediately-preceding sub-sequence in the data portion. The correlator preferably outputs a signal representative of this phase change, suitable for the radio receiver to use to determine the message bits.

Alternatively, in embodiments of any of the aspects herein, the receiver may comprise a fixed-coefficient correlator that correlates a received signal against a shorter sub-sequence for both the data portion and the synchronisation portion. The correlator may be configured to ignore all those bit positions at which the first binary chip sequence differs from the second binary chip sequence, and instead to correlate on those positions at which they agree. This may result in lower synchronisation performance, but it would reduce the size and complexity of the receiver. Such a correlator preferably determines whether a sub-sequence in the data portion has an approximately 0 or π phase change relative to the preceding sub-sequence in the data portion, and outputs a signal representative of this phase change, which the radio receiver may use to determine the message bits.

The data portion of the data packet may comprise any appropriate information, such as any one or more of: address information, a data payload, error-correction

information, etc. Data packets may be sent and received on a predetermined schedule, or erratically.

In some embodiments of the invention, the synchronisation portion, and a '1' bit (or equivalently a '0' bit) in the data portion, preferably uses any 16-bit pattern taken from the table below (or the bitwise complement and/or back-to-front reflection of one of the entries). The opposite bit value in the data portion may be represented as the same sequence but with the first and last bit values flipped.

The table presents possible 16-bit sequences in decreasing order to autocorrelation quality, where the quality value shown for a sequence is the ratio of the maximum sidelobe amplitude to the zero-lag peak amplitude, when the sequence is correlated with a pulse train of four sequence-repetitions (determined by simulation). The sequences towards the top of the table are preferred, but any of these sequences, or others, may still advantageously be used with embodiments of the invention.

Pattern (for 16-bit correlator)	Quality
[0 0 0 1 1 0 1 0 1 1 0 0 1 0 1 1]	0.250266
[0 1 0 1 1 0 0 0 1 1 0 1 0 0 1 1]	0.250924
[0 1 1 0 0 1 0 1 1 0 0 0 1 1 0 1]	0.251075
[1 0 0 1 1 0 1 0 0 1 1 1 0 0 1 0]	0.252291
[1 0 1 0 0 1 1 1 0 0 1 0 1 1 0 0]	0.252481
[1 1 0 1 0 0 1 1 0 1 0 1 1 0 0 0]	0.252488
[1 1 0 1 0 1 1 0 0 0 1 1 0 1 0 0]	0.252488
[1 1 1 0 0 1 0 1 0 0 1 1 0 1 0 0]	0.252488
[1 1 0 0 0 1 1 0 1 0 1 1 0 0 1 0]	0.252821
[1 1 0 0 1 0 1 1 0 0 0 1 1 0 1 0]	0.252821
[0 0 1 0 1 1 0 0 1 0 1 0 0 1 1 1]	0.253584
[0 0 0 1 1 0 1 0 1 1 1 0 1 0 0 1]	0.253801
[0 0 0 1 0 1 0 0 1 1 1 0 1 1 0 1]	0.253849
[0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1]	0.254011

In some embodiments, a receiver may perform a 32-bit correlation operation on the synchronisation portion of a received data packet by correlating with two copies of the 16-bit first binary chip sequence placed one after the other. Such a correlator will match pairs of instances of the repeated 16-bit sequence that occur in the

synchronisation portion. The 16-bit sequences that provide optimal autocorrelation in simulations of such embodiments have been found to be different from those where a 16-bit correlator is used. They are presented in the table below.

Where a 32-bit correlation operation is performed, the synchronisation portion, and a '1' bit (or equivalently a '0' bit) in the data portion, may be represented by any 16-bit pattern taken from the table below (or the bitwise complement and/or back-to-front reflection of one of the entries). The opposite bit value in the data portion may be represented as the same sequence but with the first and last bit values flipped. The quality value is based on the same definition given above.

Pattern (for 32-bit correlator)	Quality
[1 0 0 0 1 1 0 1 0 1 1 1 0 1 0 0]	0.232281
[1 1 0 1 0 0 0 1 0 1 0 0 1 1 1 0]	0.232607
[1 1 0 0 1 0 1 1 0 0 0 1 1 0 1 0]	0.246238
[1 0 1 0 0 1 1 1 0 0 1 0 1 1 0 0]	0.248749
[0 1 0 1 1 0 0 0 1 1 0 1 0 0 1 1]	0.250661
[0 1 1 0 0 1 0 1 1 0 0 0 1 1 0 1]	0.250678
[0 0 0 1 1 0 1 0 1 1 0 0 1 0 1 1]	0.251603
[0 1 0 0 1 1 0 1 0 1 1 0 0 0 1 1]	0.252833
[1 1 0 1 0 0 1 1 0 1 0 1 1 0 0 0]	0.252869
[0 0 1 0 1 1 0 0 1 0 1 0 0 1 1 1]	0.253260
[0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1]	0.253473
[0 0 1 1 1 0 0 1 0 1 0 0 1 1 0 1]	0.254259
[0 0 1 1 0 1 0 0 1 1 1 0 0 1 0 1]	0.254626
[1 0 0 0 1 1 0 1 0 1 1 1 0 1 0 0]	0.232281

The radio transmitter may be wholly or substantially implemented as an integrated circuit. It may comprise, or be configured to communicate with, a microcontroller or other processor. It may be configured to receive message data from the microcontroller, processor, or other logic device, and to transmit the message data by radio. The radio receiver may be wholly or substantially implemented as an integrated circuit. It may comprise, or be configured to communicate with, a microcontroller or other processor. It may be configured to decode message data from one or more received data packets, and to output the message data to the microcontroller, processor, or other logic device. In some embodiments, the radio transmitter

comprises, or is communicably connected to, an input source such as a button, keyboard, touchscreen or other sensor. In some embodiments, the radio receiver comprises, or is communicably connected to, an output such as a display, loudspeaker or indicator light.

Features of any aspect or embodiment described herein may, wherever appropriate, be applied to any other aspect or embodiment described herein. Where reference is made to different embodiments or sets of embodiments, it should be understood that these are not necessarily distinct but may overlap.

Certain preferred embodiments of the invention will now be described, by way of example only, with reference to the accompanying drawings, in which:

Figure 1 is a schematic drawing of a radio communication system embodying the invention;

Figure 2 is a diagram of a data packet that may be transmitted and received by the radio communication system;

Figure 3 is a schematic drawing of part of a radio transmitter embodying the invention;

Figure 4 is a plot of phase against time for two different chip sequences;

Figure 5 is schematic drawing of part of a radio receiver embodying the invention; and

Figure 6 is a state diagram for this radio receiver.

Figure 1 shows a wireless heart-rate monitor 1 which is in communication with a mobile telephone 7. Both devices embody the present invention.

The wireless heart-rate monitor 1 has a heart-rate sensor 2 which is connected to a microprocessor 3 (such as an ARM™ Cortex M-series). The microprocessor 3 is connected to a radio transmitter 4. The radio transmitter 4 includes an encoder 5 (among other components). Other conventional components, such as memory, a battery, etc. are also present, but are omitted from the drawing for the sake of simplicity. The microprocessor 3 and radio transmitter 4 may be integrated on a single silicon chip. The monitor 1 has a radio antenna 6, which may be integrated on such a chip or external to it.

The mobile telephone 7 has, among other conventional components (not shown), an antenna 8, suitable for receiving short-range radio communications from wireless-personal-area-network devices, which is connected to a radio receiver 9. The radio receiver 9 includes a fixed-coefficient correlator 10 (among other components). The radio receiver 9 is connected to a microprocessor 11 (such as an ARM™ Cortex M-series), which can output data for display on a screen 12, possibly via other components, such as a further microprocessor (not shown) running an operating system and appropriate software applications.

In use, the wireless heart-rate monitor 1 receives periodic heart-rate readings for a human user from the heart-rate sensor 2. The microprocessor 3 processes the readings into a suitable format for transmission, and sends the message data to the radio transmitter 4. In some embodiments, the message data may already be differentially encoded, in order to improve the efficiency of the decoding operation on the radio receiver 9. The radio transmitter 4 determines whether the message data can fit within a single data packet, or if it must be split across two or more data packets. In either case, the radio transmitter 4 assembles the message data into a data portion, along with any other relevant data. The encoder 5 in the radio transmitter 4 encodes the data portion, containing the message data, to create a payload in which each '1' bit is represented by the 16-bit sequence [0 0 0 1 1 0 1 0 1 1 0 0 1 0 1 1] and each '0' bit is represented by the sequence [1 0 0 1 1 0 1 0 1 1 0 0 1 0 1 0] (or vice versa). It prepends a synchronisation word to the payload, consisting of 15 repetitions of the first sequence, [0 0 0 1 1 0 1 0 1 1 0 0 1 0 1 1]. A fixed preamble (e.g. of 8 chips) may be included before the synchronisation word.

The radio transmitter 4 then transmits the encoded data packet from the antenna 6, modulated on a radio-frequency carrier (e.g. at around 2.4 GHz), using two-level GFSK with a modulation index of 0.5. The data packet may contain additional elements, such as a preamble, if appropriate.

Figure 2 shows an exemplary data packet structure, which includes a fixed preamble, a synchronisation portion (sync word), and a data portion. The data portion contains an access address, message bits, and a cyclic-redundancy check (CRC).

The mobile telephone 7 receives the radio data packet at the antenna 8. The radio receiver 9 processes the GFSK signal using the correlator 10. The receiver 9 first correlates the received signal with the first 16-bit sequence [0 0 0 1 1 0 1 0 1 1 0 0 1 0 1 1], in order to determine frequency and/or timing synchronisation information from the synchronisation portion.

The radio receiver 9 then reconfigures the correlator 10 to correlate the received data portion with the 14-bit sub-sequence [0 0 1 1 0 1 0 1 1 0 0 1 0 1], which is the shared, middle 14 bits contained in each of the two 16-bit sequences. It processes I and Q components separately in order to determine the phase shift between successive appearances of the sub-sequence in the data portion. The radio receiver 9 decodes the message data from the phase shift information by using an initial phase reference from the synchronisation portion (which corresponds to an initial decoded bit value of '1', for instance) to decode any sequence that shifts in phase by approximately 180 degrees as having the opposite value to the immediately preceding decoded message bit, and any sequence that has approximately zero degrees of phase shift as having the same value as the immediately preceding decoded message bit.

The radio receiver 9 performs on-going drift tracking while processing the data packet, based on phase information output by the correlator 10.

The radio receiver 9 can then extract the message from the decoded data, check the CRC, and perform any other appropriate operations. It then passes the decoded message data to the microprocessor 11 for processing. The microprocessor 11 may process it in any appropriate way. In some embodiments, heart-rate information may be displayed graphically on the display screen 12 for the user to see.

The wireless heart-rate monitor 1 and mobile telephone 7 may be configured so that heart-rate message data is transferred from the wireless heart-rate monitor 1 to the mobile telephone 7 substantially according to the Bluetooth Low Energy (BTLE)™ core specification version 4.0, with the exception of the physical layer. The wireless heart-rate monitor 1 and mobile telephone 7 may be equipped for two-way radio communication, using corresponding components for radio transmission in the opposite direction, although this is not essential.

Figure 3 shows greater detail of elements within a radio transmitter embodying the invention. This could be the same radio transmitter 4 as described above, or it could be a different radio transmitter.

This radio transmitter first differentially encodes the data bits using a differential encoder unit 13. Each differentially encoded bit is then represented by one of two quasi-antipodal chip sequences, by an up-chipping unit 14. Each of the chips in a sequence is then feed through a GFSK filter 15 and is transmitted as a GFSK modulated signal.

Figure 4 illustrates two possible quasi-antipodal chip sequences 16, 17 that could be used by the up-chipping unit 14. The two chip sequences are the same length and differ only in the first and last chips. When, as is preferred, the modulation index is h=0.5 nominally, the phase difference between the two signals will be π everywhere except for the very first chip and the very last chip in the sequences, as can be seen from Figure 4, which shows the first five chips of both sequences 16, 17, as well as the final chip (the remaining chips are omitted for conciseness).

Figure 5 shows detail of a digital baseband processing stage of a radio receiver embodying the invention. This could be the same radio receiver 9 as described above, or it could be a different radio receiver.

Steps such as filtering and residual frequency offset tracking are not shown for reasons of conciseness.

The design of the radio receiver aims to optimize sensitivity while tolerating realistic channel conditions (carrier frequency offset, carrier drift, fading, etc.). It uses correlation for timing synchronization and detection.

Complex-valued baseband samples are shown entering from the left side of Figure 5. These are passed to a CORDIC unit 18, and from there to a despreader unit 19. The despreader unit 19 performs a cross correlation between an incoming chip sequence containing data and a stored replica of this chip sequence. The output of the despreader unit 19 conveys the phase difference between the two different chip sequences. This is passed to a second CORDIC unit 20, and then on to a DBPSK

decoder unit 21. The incoming samples are also passed to a synchronisation unit 22 which performs timing synchronization and initial carrier frequency offset estimation.

Figure 5 contains the following abbreviations:

n = chip index;

m = symbol index;

z(n) = complex baseband samples;

z'(n) = carrier-frequency offset (CFO) compensated z(n); and

p(k) = complex values representing the chip sequence.

The synchronization is built around a particular kind of correlator. The correlator is a data-aided joint timing and frequency estimator which exploits knowledge of the data in the received symbols to cancel the effect of the modulation on the estimate of a conventional delay-and-correlate type of carrier frequency offset estimator. The principle behind the synchronisation is described in WO 2014/167318, by the present applicant, the entire contents of which are hereby incorporated by reference.

The performance of the radio receiver of Figure 5, assuming ideal synchronisation, can be analysed as follows.

For discriminator detection of FSK signalling with a modulation index of h=0.5, it is expected that $E_b/N_0 \approx 12$dB for a bit error rate (BER) =0.001. When cross-correlating directly on I and Q, the underlying theory for BER in additive white Gaussian noise (AWGN) is expected to follow that for non-coherent detection of correlated binary signalling. For a modulation index=0.5, $E_b/N_0 \approx 14.5$dB for a bit error rate (BER) =0.001.

Discriminator detection will normally outperform non-coherent detection of correlated binary signalling for this modulation index. However, by correlating after the discriminator, the discriminator is here operating below the FM "threshold"—a region where detector performance deteriorates rapidly.

For differential detection of DBPSK, the $E_b/N_0 \approx 8$dB for a bit error rate (BER) =0.001. This is 6.5dB less compared to orthogonal detection and about 4dB less than the case for discriminator detection of a GFSK signal given modulation index=0.5 Thus,

utilizing DBPSK signalling on symbols made of GFSK modulated chips gives an inherent gain of 4dB on the link budget. This is a very significant benefit of the present approach. This gain adds on top of the usual DSSS processing gain.

The "joint timing & freq. offset sync" synchronisation unit 22 in Figure 5 carries out the following cross correlation for every incoming baseband sample $z_n = I(n) + jQ(n)$:

$$\Delta\hat{f} = \frac{1}{2\pi DT}\arg\left\{\sum_{i=0}^{L-1}\left[z_{n-i}z_{n-i-D}^{*}\right]d_i\right\},$$

where L is the number of samples representing an up-sampled "sync word" (such as the 16-bit sequence specified above); where D is a lag which is decided at design time; and where T is the sample period.

The coefficients are given as $d_i = p_i^{*} p_{i+D}$ where *p* are the samples constituting the up-sampled and modulated sync word bits. The correlator should be sampled at the right point in time for the frequency offset estimate to be valid, and this time instant is when a "peak" is observed in the value of M_n given by:

$$M_n = \frac{|C_n|}{P_n}, \text{ where } C_n = \sum_{i=0}^{L-1}\left[z_{n-i}z_{n-i-D}^{*}\right]d_i \text{ and } P_n = \sum_{i=0}^{L-1}\left|z_{n-i-D}\right|^2.$$

A valid peak in M_n is determined against a programmable threshold. A successful synchronisation event is defined by the observation of a few valid peaks spaced apart in time by amounts corresponding to the "sync word" length, plus or minus a value, Δ, to account for noise. This synchronization event furthermore defines the strobe time to be used for subsequent detection of the data symbols.

The coefficients $d_i = p_i^{*} p_{i+D}$ are calculated at design time.

The DBPSK detection is implemented as follows.

The received sequence of complex baseband samples *z(n)* that represents a sequence of GFSK-modulated chips is processed by the digital-baseband-correlator

despreader unit 19. The chip sequence constitutes one symbol with period T_s. Assuming a constant envelope *A*:

$$z(n) = Ae^{j\varphi(n)}, \text{ where } \varphi(n) = \varphi_0 + \omega_{cfo}n + \varphi_m(n).$$

Here, φ_0 represents a constant phase offset between the transmitter and the receiver, while ω_{cfo} represents a negligible carrier frequency offset (a non-zero carrier frequency offset will result in a constellation rotation between symbols; unless this offset is kept sufficiently small after carrier-frequency offset estimation and compensation, the bit error rate will increase). The differential phase modulation is embedded in $\varphi_m(n)$ which represents the phase relative to the previous symbol, and will take on values in {0, π}.

The message data bits are determined in the decoder unit 21 by observing the phase shift of $\varphi_m(n)$ between consecutive received symbols. The radio transmitter applies the same phase shift to all chips in a symbol, depending on the data to be transmitted. Each bit of the message data may therefore be differentially decoded, with no phase shift implying a '0' and a phase shift of π implying a '1' (or vice versa, depending on how the differential encoding is implemented in the radio transmitter).

In order to correlate *N* values of *z(n)* with a set of *N* complex coefficients representing *N* GFSM modulated chips (assuming no oversampling for now, for simplicity), the coefficients *p(k)* can be written as:

$$p(k) = e^{j\theta_k}.$$

Assuming, for simplicity, that $\omega_{cfo} = 0$, the complex-valued correlator output at time *t* is then given by:

$$\begin{aligned} C(t) &= \sum_{k=0}^{N-1} z(n-k)p^*(k) \\ &= A\sum_{k=0}^{N-1} e^{j\varphi(n-k)}e^{-j\theta_k} \\ &= A\sum_{k=0}^{N-1} e^{j(\varphi_0+\varphi_m(n-k)-\theta_k)} \\ &= A\sum_{k=0}^{N-1} e^{j(\varphi_0+q\pi)}, \text{ q} \in \{0,1\}, \text{ when timing synchronized } \varphi_m(n-k)-\theta_k \in \{0,\pi\} \\ &= ANe^{j(\varphi_0+q\pi)}, \end{aligned}$$

where $angle\big(C(t)\big) = \varphi_0 + q\pi$.

Thus the angular difference between $C(t)$ and $C(t+T_s)$ will be 0 or π. Note that φ_0 disappears.

If the angular difference is greater than π/2 or less than -π/2 the detector will output a '1'; otherwise it will output a '0'.

For coherent detection, φ_0 would need to be estimated.

Symbol timing synchronization or tracking can be done by detecting the time when a "peak value" is observed on $|C(t)|$.

The residual carrier frequency offset ω_{cfo} is a consequence of carrier-frequency drift and initial carrier frequency offset estimation error, and can be tracked by looking at the angular difference between $C(t)$ and $C(t+T_s)$. Thus ω_{cfo} can be estimated as:

$$\widehat{\omega_{cfo}} = \frac{angle\big(C(t+T_s)\big) - angle\big(C(t)\big)}{T_s},$$

after subtracting the known phase shift (after decision) due to the modulation. The residual carrier frequency offset $\widehat{F_{cfo}}$ in [Hz] is then calculated as $\widehat{F_{cfo}} = \widehat{\omega_{cfo}}\frac{1}{2\pi}$ [Hz].

Figure 6 shows a finite state machine (FSM) that can orchestrate the synchronization process and data reception in a radio receiver as illustrated in Figure 5.

The state of this FSM is given by the variable *syncstate*. At time t=0 the FSM starts out in *syncstate*=0. In this state the FSM is to the right side of the dashed line in Figure 6, and is looking for "peaks" in the value of M_n computed by the synchronisation unit 22. For each "peak", the $\Delta\hat{f}$ value is recorded in a vector element cfoVec[MnCnt], and the "peak" counter MnCnt is incremented by one. When a sufficient minimum number *min* of such peaks with a certain distance *dist* between each peak has been observed, initial timing and carrier frequency offset synchronization is achieved and *syncstate* is incremented by one.

The average time of the "peaks" as measured by a counter (which counts modulo the number of samples per symbol) defines the subsequent symbol boundaries (strobe timing). Additionally, an initial carrier frequency offset estimate is computed as the average of the elements in the vector cfoVec. This value, $\widehat{\omega_{cfo}}$, is then passed to the CORDIC unit 18.

Now, with *syncstate*>0, the FSM enters the left side of the dashed line in Figure 6, for receiving the payload. In this state, the message data bits are determined in the decoder unit 21 by observing the phase shift of $\varphi_m(n)$ between consecutive received symbols, as described above. Additionally, the residual carrier frequency offset (CFO) is tracked and ω_{CFO} is computed, as described above. In turn, this value is used to update (by being added to) the value $\widehat{\omega_{cfo}}$ in the CORDIC unit 18.

Claims

1. A radio transmitter comprising an encoder configured to receive one or more variable message bits and to encode each message bit that has a first value as a predetermined first binary chip sequence and to encode each message bit that has the opposite value as a predetermined second binary chip sequence, wherein the radio transmitter is configured to transmit data packets, each comprising (i) a predetermined synchronisation portion, comprising one or more instances of the first binary chip sequence, and (ii) a variable data portion, comprising one or more encoded message bits output by the encoder.

2. A radio transmitter as claimed in claim 1, configured to modulate the synchronisation portion and the variable data portion on a radio carrier wave using Gaussian frequency-shift-keying (GFSK).

3. A radio transmitter as claimed in claim 2, wherein the GFSK modulation has a modulation index of approximately 0.5.

4. A radio transmitter as claimed in any preceding claim, wherein one or each of the first and second binary chip sequences is an even number of bits long, greater than or equal to four.

5. A radio transmitter as claimed in any preceding claim, wherein the first binary chip sequence is such that it is phase neutral when modulated using GFSK.

6. A radio transmitter as claimed in any preceding claim, wherein one or each of the first and second binary chip sequences consists of an equal number of zero bits and one bits.

7. A radio transmitter as claimed in any preceding claim, wherein the second binary chip sequence is identical to the first binary chip sequence except at its first and last bit positions, at which it differs.

8. A radio transmitter as claimed in any preceding claim, wherein the first and last bits of the first binary chip sequence differ from each other.

9. A radio transmitter as claimed in any preceding claim, wherein the first binary chip sequence has maximum autocorrelation performance, over the set of all possible binary sequences of the same length as the first binary chip sequence, subject to the constraints that the sequence must have an equal number of zero bits and one bits, and that it must have first and last bits that differ in value from each other.

10. A radio transmitter as claimed in any preceding claim, wherein the first binary chip sequence has an autocorrelation quality of less than 0.26, determined as the ratio of the maximum sidelobe amplitude to the zero-lag peak amplitude when the sequence is correlated with a pulse train of four sequence-repetitions.

11. A radio transmitter as claimed in any preceding claim, wherein the first binary chip sequence is the 16-bit sequence [0 0 0 1 1 0 1 0 1 1 0 0 1 0 1 1], or its reverse, or its bitwise complement, or its reversed bitwise complement.

12. A radio transmitter as claimed in any preceding claim, wherein the predetermined synchronisation portion of the data packets comprises between two and around 30 instances of the first binary chip sequence.

13. A radio transmitter as claimed in any preceding claim, wherein the data portions of the data packets follow after the synchronisation portions without any gap.

14. A radio receiver configured to:

receive data packets, each comprising a predetermined synchronisation portion, comprising one or more instances of a predetermined first binary chip sequence, and a variable data portion, comprising one or more encoded message bits, wherein each message bit that has a first value is encoded as the first binary chip sequence and each message bit that has the opposite value is encoded as a predetermined second binary chip sequence;

use the synchronisation portion of a received data packet to perform a frequency and/or timing synchronisation operation, before decoding the data portion of the data packet; and

decode message bits from the data portion of the data packet.

15. A radio receiver as claimed in claim 14, configured to demodulate the data portion of a received data packet using a differential-binary-phase-shift-keying (DBPSK) demodulator.

16. A radio receiver as claimed in claim 14 or 15, comprising a correlator, and configured to use the correlator for performing the frequency and/or timing synchronisation operation.

17. A radio receiver as claimed in claim 16, wherein the correlator is a fixed-coefficient correlator.

18. A radio receiver as claimed in any of claims 14 to 17, comprising a correlator that is switchable between two modes: a first mode in which it correlates against the complete first binary chip sequence, and a second mode in which it correlates against a sub-sequence of the first binary chip sequence.

19. A radio receiver as claimed in claim 18, configured to use the correlator in the first mode for processing the synchronisation portion of a received data packet, and to switch the correlator to the second mode for decoding message bits from the data portion.

20. A radio receiver as claimed in claim 18 or 19, wherein the sub-sequence is defined by the bit positions in the first binary chip sequence at which the first and second binary chip sequences have the same values as each other.

21. A radio receiver as claimed in any of claims 18 to 20, wherein the sub-sequence consists of all the bits of the first binary chip sequence except for the first and last bits.

22. A radio receiver as claimed in any of claims 16 to 21, wherein the correlator is configured to output amplitude information and the radio receiver is configured to use this amplitude information to perform symbol timing synchronisation.

23. A radio receiver as claimed in any of claims 16 to 22, wherein the correlator is configured to output phase information and the radio receiver is configured to use this phase information to perform an initial frequency synchronisation.

24. A radio receiver as claimed in any of claims 16 to 23, configured to use phase information from the correlator to perform on-going frequency drift tracking, and to apply appropriate adjustment or compensation if the frequency of a received signal drifts.

25 A radio receiver as claimed in any of claims 16 to 24, configured to use the correlator to determine whether a sub-sequence in the data portion of a received data packet has an approximately 0 or an approximately π phase change relative to the immediately-preceding sub-sequence in the data portion, and to use a signal representative of this phase change from the correlator to determine the message bits.

26. A radio communication system comprising a radio transmitter and a radio receiver,

wherein the radio transmitter:

comprises an encoder configured to receive one or more variable message bits and to encode each message bit that has a first value as a predetermined first binary chip sequence and to encode each message bit that has the opposite value as a predetermined second binary chip sequence; and

is configured to transmit data packets, each comprising (i) a predetermined synchronisation portion, comprising one or more instances of the first binary chip sequence, and (ii) a variable data portion, comprising one or more encoded message bits output by the encoder,

and wherein the radio receiver is configured to:

receive the data packets transmitted by the radio transmitter;

use the synchronisation portion of a received data packet to perform a frequency and/or timing synchronisation operation, before decoding the data portion of the data packet; and

decode the message bits from the data portion of the data packet.

27. A method of radio communication, comprising:

transmitting a data packet by radio, the data packet comprising (i) a predetermined synchronisation portion, comprising one or more instances of a first binary chip sequence, and (ii) a data portion, comprising one or more encoded message bits, wherein each message bit that has a first value is encoded as a predetermined first binary chip sequence, and each message bit that has the opposite value is encoded as a predetermined second binary chip sequence,

receiving the data packet;

using the synchronisation portion of the received data packet to perform a frequency and/or timing synchronisation operation; and

decoding the message bits from the data portion of the received data packet.

28. A radio receiver comprising a fixed-coefficient correlator that is switchable between a first mode in which it is configured to correlate a received signal against a binary chip sequence, and a second mode in which it is configured to correlate a received signal against a shorter sub-sequence from the binary chip sequence, wherein the correlator is configured, when in the second mode, to output a signal representative of a phase shift between two successive occurrences of the sub-sequence in a received signal.

29. A radio receiver as claimed in claim 28, configured to use the signal representative of a phase shift between two successive occurrences of the sub-sequence in a received signal to decode message data from a data portion of a received data packet.

30. A radio receiver as claimed in claim 28 or 29, configured to demodulate the data portion of a received data packet using a differential-binary-phase-shift-keying (DBPSK) demodulator.

31. A radio receiver as claimed in any of claims 28 to 30, configured to use the correlator for performing a frequency and/or timing synchronisation operation.

32. A radio receiver as claimed in any of claims 28 to 31, configured to use the correlator in the first mode for processing a synchronisation portion of a received data packet, and to switch the correlator to the second mode for decoding message bits from a data portion of the data packet.

33. A radio receiver as claimed in any of claims 28 to 32, wherein the sub-sequence consists of all the bits of the binary chip sequence except for the first and last bits.

34. A radio receiver as claimed in any of claims 28 to 33, wherein the correlator is configured to output amplitude information and the radio receiver is configured to use this amplitude information to perform symbol timing synchronisation.

35. A radio receiver as claimed in any of claims 28 to 34, wherein the correlator is configured to output phase information and the radio receiver is configured to use this phase information to perform an initial frequency synchronisation.

36. A radio receiver as claimed in any of claims 28 to 35, configured to use phase information from the correlator to perform on-going frequency drift tracking, and to apply appropriate adjustment or compensation if the frequency of a received signal drifts.

37 A radio receiver as claimed in any of claims 28 to 36, configured to use the correlator to determine whether a sub-sequence in the data portion of a received data packet has an approximately 0 or an approximately π phase change relative to the immediately-preceding sub-sequence in the data portion, and to use a signal representative of this phase change from the correlator to determine the message bits.

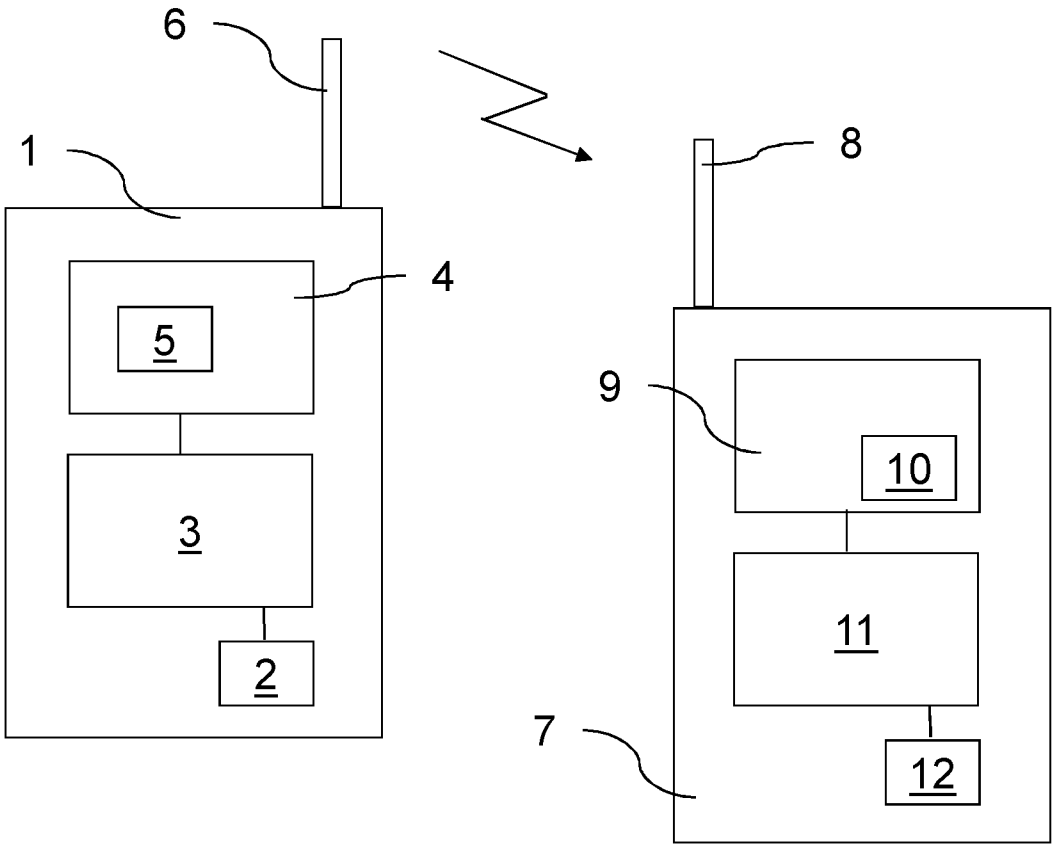


Figure 1

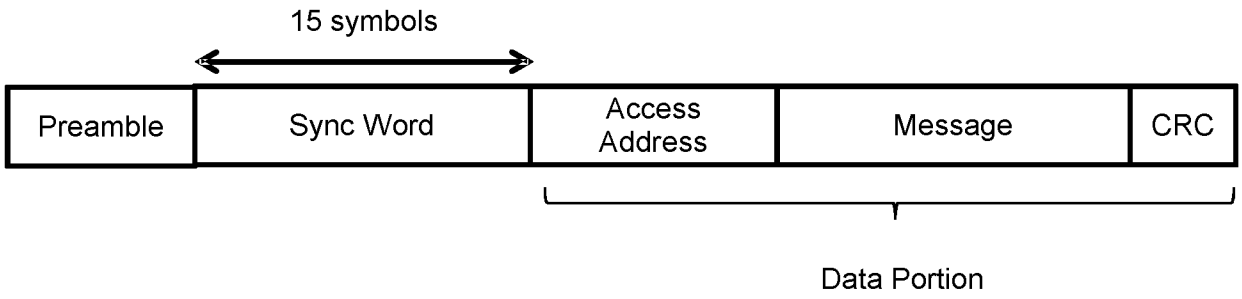


Figure 2

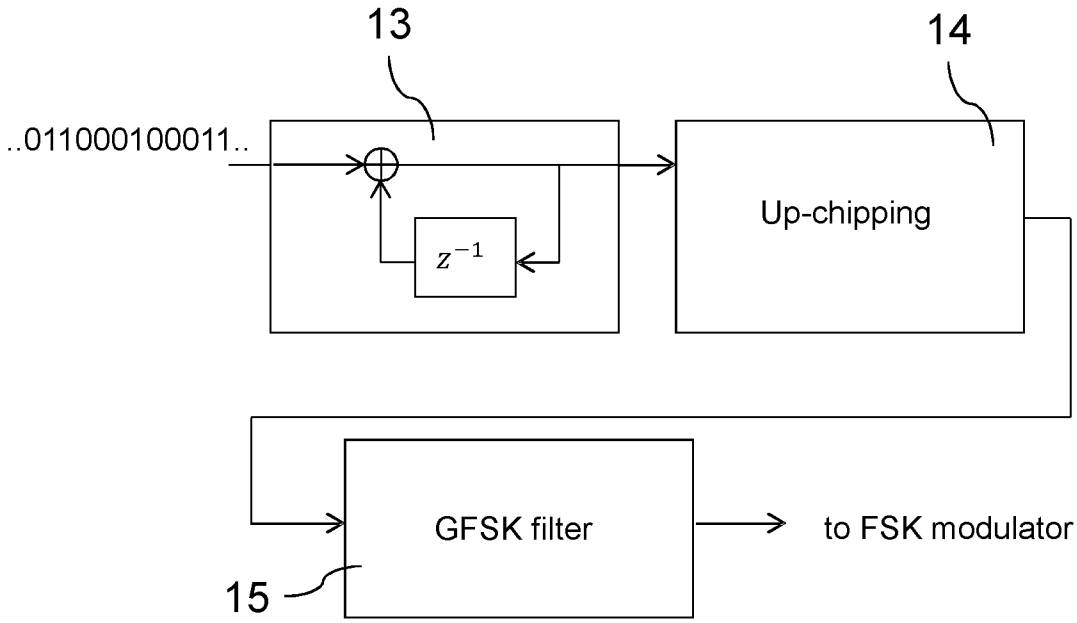


Figure 3

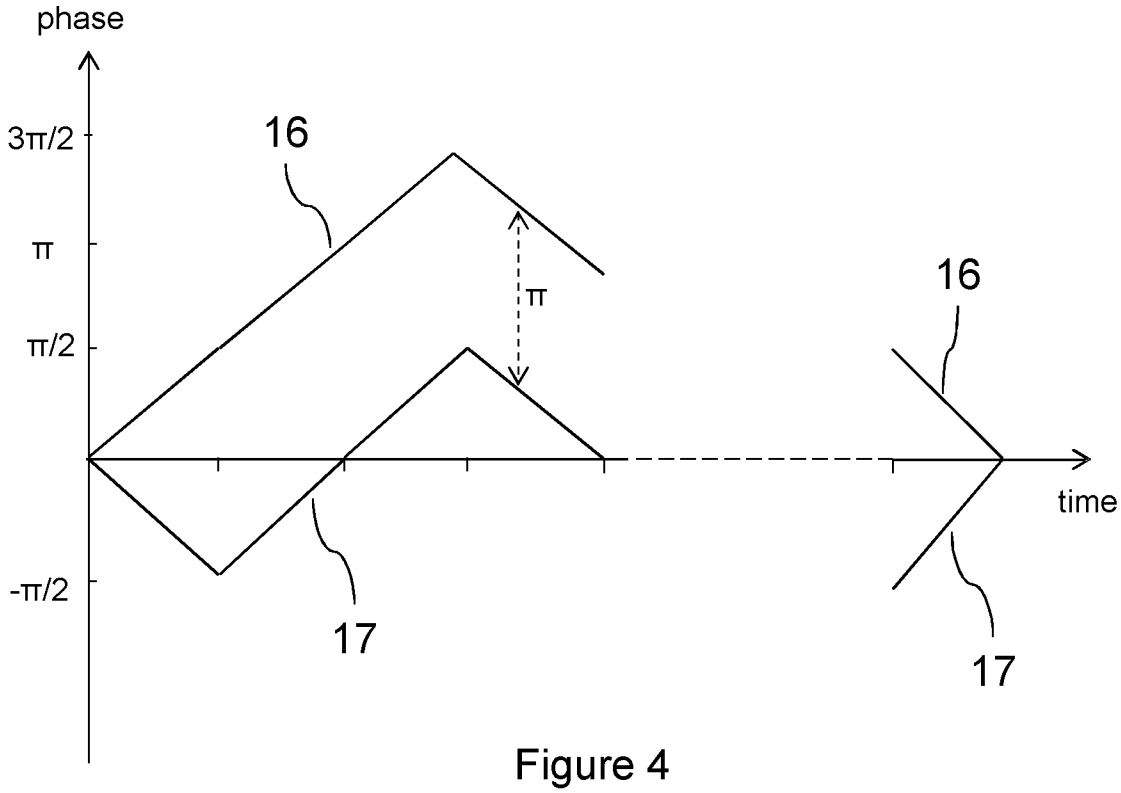
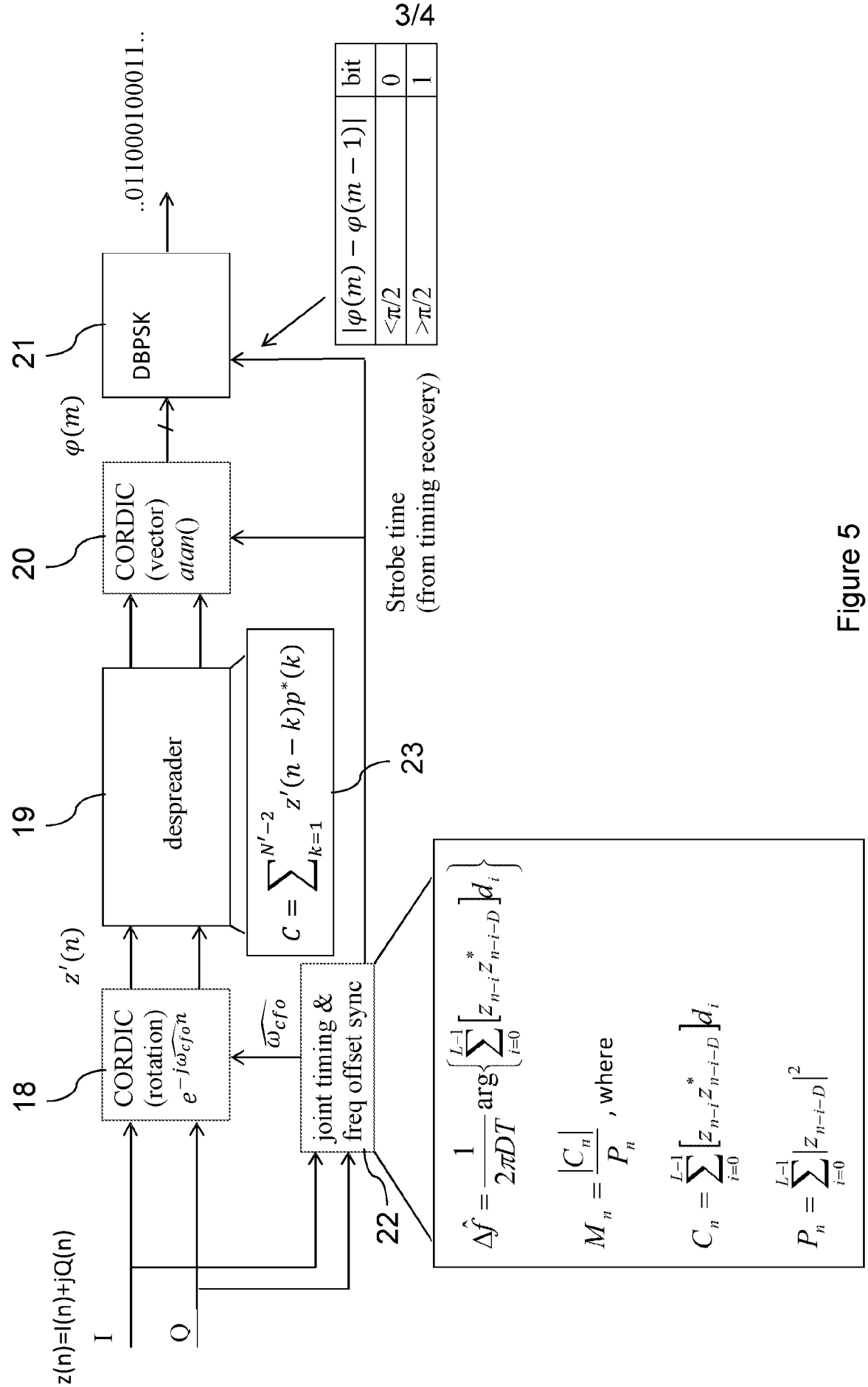


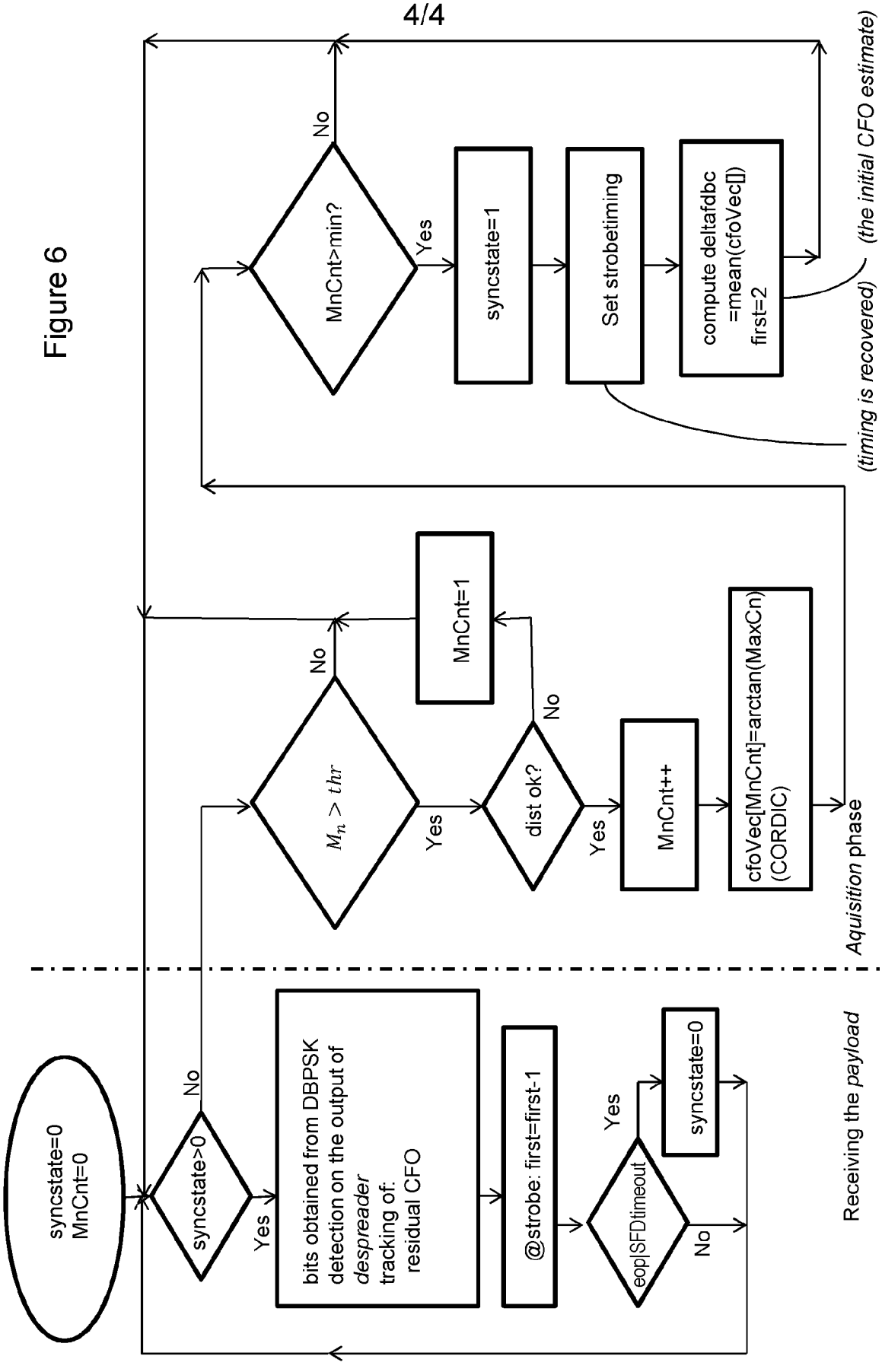
Figure 4



$\lvert\varphi(m)-\varphi(m-1)\rvert$	bit
$<\pi/2$	0
$>\pi/2$	1

Figure 5

Figure 6


syncstate=0
MnCnt=0
syncstate>0
No
Yes
bits obtained from DBPSK detection on the output of *despreader* tracking of: residual CFO
@strobe: first=first-1
eop|SFDtimeout
Yes
No
syncstate=0
Receiving the *payload*
$M_n > thr$
No
Yes
MnCnt=1
dist ok?
No
Yes
MnCnt++
cfoVec[MnCnt]=arctan(MaxCn) (CORDIC)
Aquisition phase
MnCnt>min?
No
Yes
syncstate=1
Set strobetiming
compute deltafdbc =mean(cfoVec[]) first=2
(timing is recovered)
(the initial CFO estimate)

INTERNATIONAL SEARCH REPORT

International application No
PCT/GB2015/051669

A. CLASSIFICATION OF SUBJECT MATTER
INV. H04J13/00 H04J13/10 H04L27/22 H04L27/18 H04L27/20
H04L7/00 H04B1/7073
ADD.
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H04J H04L H04B

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal, WPI Data, COMPENDEX, INSPEC

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	SUST M K: "Performance of digital matched filters in a direct sequence spread spectrum receiver", 19881023; 19881023 - 19881026, 23 October 1988 (1988-10-23), pages 961-967, XP010072053,	1-4, 12-14, 26,27
A	the whole document	5,15

Y	US 4 943 974 A (MOTAMEDI MASOUD [US]) 24 July 1990 (1990-07-24)	1-4, 12-14, 26,27
A	column 6, line 3 - line 27	5,15

Y	US 2014/086125 A1 (POLO ANGEL [US] ET AL) 27 March 2014 (2014-03-27) paragraph [0056] - paragraph [0058]	2,3

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
21 August 2015	09/11/2015

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Giglietto, Massimo

INTERNATIONAL SEARCH REPORT

International application No.
PCT/GB2015/051669

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

see additional sheet

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2. ☐ As all searchable claims could be searched without effort justifying an additional fees, this Authority did not invite payment of additional fees.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☒ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

1-5, 12-15, 26, 27

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.

☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.

☐ No protest accompanied the payment of additional search fees.

FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

This International Searching Authority found multiple (groups of) inventions in this international application, as follows:

1. claims: 1-5, 12-15, 26, 27

   a transmitter apparatus, a receiver apparatus, a system and communication method, respectively, the transmitter comprising an encoder configured to receive one or more variable message bits and to encode each message bit that has a first value as a predetermined first binary chip sequence and to encode each message bit that has the opposite value as a predetermined second binary chip sequence, wherein the radio transmitter is configured to transmit data packets, each comprising (i) a predetermined synchronisation portion, comprising one or more instances of the first binary chip sequence, and (ii) a variable data portion, comprising one or more encoded message bits output by the encoder.

   ---

2. claim: 6

   a radio transmitter wherein one or each of the first and second binary chip sequences consists of an equal number of zero bits and one bits.

   ---

3. claim: 7

   a radio transmitter wherein the second binary chip sequence is identical to the first binary chip sequence except at its first and last bit positions, at which it differs

   ---

4. claim: 8

   a radio transmitter wherein the first and last bits of the first binary chip sequence differ from each other.

   ---

5. claims: 9-11

   a radio transmitter wherein the first binary chip sequence has maximum autocorrelation performance, over the set of all possible binary sequences of the same length as the first binary chip sequence, subject to the constraints that the sequence must have an equal number of zero bits and one bits, and that it must have first and last bits that differ in value from each other

   ---

6. claims: 16-25, 28-37

   A radio receiver comprising a fixed-coefficient correlator that is switchable between a first mode in which it is

configured to correlate a received signal against a binary chip sequence, and a second mode in which it is configured to correlate a received signal against a shorter sub-sequence from the binary chip sequence, wherein the correlator is configured, when in the second mode, to output a signal representative of a phase shift between two successive occurrences of the sub-sequence in a received signal.

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/GB2015/051669

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 4943974 A	24-07-1990	NONE	
US 2014086125 A1	27-03-2014	NONE	