



(51) International Patent Classification:
H01L 29/78 (2006.01) *H01L 21/336* (2006.01)

(21) International Application Number:
PCT/CN2010/079412

(22) International Filing Date:
3 December 2010 (03.12.2010)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
200910188704.5 3 December 2009 (03.12.2009) CN

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(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PE, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:

— with international search report (Art. 21(3))

(54) Title: N TYPE LATERAL DOUBLE DIFFUSED METAL OXIDE SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREOF

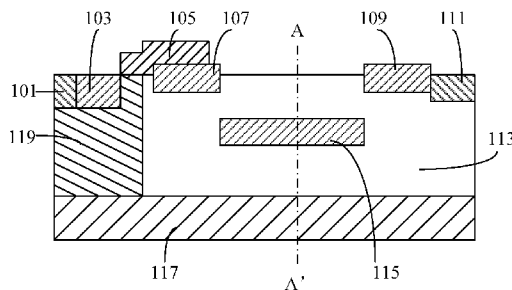


Figure 1

(57) Abstract: An N type lateral double diffused metal oxide semiconductor (NLD MOS) device comprises a floating P type structure (115), a first field oxide region (107), a second field oxide region (109) and an N type drift region (113), wherein the first field oxide region (107) and the second field oxide region (109) are disposed on the N type drift region (113); the floating P type structure (115) is located in the middle portion of the N type drift region (113); the first field oxide region (107) and the second field oxide region (109) are not connected together; and width of active region between the first field oxide region (107) and the second field oxide region (109) matches with length of the injected floating P type structure (115). By employing the construction of the NLD MOS, not only the breakdown voltage of semiconductor device can be raised, but also on-resistance can be effectively lowered. Meanwhile, the requirements of high-energy injection are lowered and the limitation to processing machine is decreased, making the manufacturing easier to be carried out.



N TYPE LATERAL DOUBLE DIFFUSED METAL OXIDE SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREOF

FIELD OF THE INVENTION

[0001] The present invention relates to an N type Lateral Double-diffused Metal Oxide Semiconductor (NLDMOS) device, in particular, relates to a NLDMOS having a relatively high breakdown voltage and a relatively low on-resistance and a method of manufacturing the same.

BACKGROUND

[0002] With continuous increase of operational voltage of semiconductor devices, Super Junction has been introduced in order to obtain a higher withstand voltage and a lower on-resistance. For example, with respect to an N type Lateral Double-diffused Metal Oxide Semiconductor (NLDMOS), an N type drift region with a relatively high concentration is firstly formed in order to obtain a relatively low on-resistance. Since a drift region with a relatively high concentration makes the breakdown value of device relatively low, a certain P type region is formed in the N type drift region meanwhile. The P type region is generally distributed in stripe along the channel direction in the surface of the drift region. By achieving an electrical charge balance between N type impurities in the drift region and P type impurities introduced, the depletion of drift region is enhanced and the breakdown voltage of device is improved. However, the P type region is injected into the surface of the drift region by low energy, electrical current can merely flow through the drift region underneath. Moreover, in order to deplete the whole drift region in longitudinal direction, the junction depth of the P type region should not be too shallow. Therefore, the P type region must be formed through a certain thermal drive-in process, such that impurity concentration in the N type drift region will decrease under effect of the P type impurity, thus increasing the on-resistance. Besides, the P type region formed through a thermal process increases in size due to lateral diffusion, which reducing flow path of electrical current and increasing the on-resistance again.

SUMMARY OF THE INVENTION

[0003] In view of above, it is necessary to provide a NLDMOS device that can increase

breakdown voltage and reduce on-resistance, which addresses the issue of relatively large on-resistance and relatively low breakdown voltage of NLD MOS device.

[0004] Furthermore, it is also necessary to provide a method of manufacturing a NLD MOS device that increases breakdown voltage and reduces on-resistance.

5 [0005] A NLD MOS device comprises a floating P type structure, a first field oxide region, a second field oxide region and a N type drift region, wherein the first field oxide region and the second field oxide region are disposed on the N type drift region, wherein the floating P type structure is located in the middle portion of the N type drift region along the channel direction of the N type drift region, the width of an active region between the
10 first field oxide region and the second field oxide region is no less than the length of the floating P type structure.

[0006] Preferably, a plurality of floating P type structures are provided in the N type drift region.

15 [0007] Preferably, the floating P type structure is in a stripe shape and the cross section of the floating P type structure is in a rectangular shape.

[0008] Preferably, the cross section of the floating P type structure is in a circular shape.

[0009] Preferably, the length of the first field oxide region is different from that of the second field oxide region.

20 [0010] A method of manufacturing a NLD MOS device comprising a floating P type structure, a first field oxide region, a second field oxide region and a N type drift region, wherein the first field oxide region and the second field oxide region are disposed on the N type drift region, the method comprises the following five steps of:

[0011] step 1): forming an epitaxial layer on a buried oxide layer by epitaxial manufacturing process;

25 [0012] step 2): performing well injection by MOS process to form the N type drift region;

[0013] step 3): growing the first field oxide region and the second field oxide region, an active region located between the first field oxide region and the second field oxide region, wherein the size of the active region matches with the length of the floating P type

structure to be injected;

[0014] step 4): performing injection for a source region, a gate region and a drain region; and

5 [0015] step 5): injecting a floating P type structure into the middle portion of the N type drift region through the active region between the first field oxide region and the second field oxide region.

[0016] Preferably, the injection energy of the floating P type structure is 200Kev~2000Kev.

10 [0017] By using the above construction, the breakdown voltage of a NLDMOS device can be increased and on-resistance thereof can be reduced, the requirement on thickness of photoresist during manufacturing process and the requirement of high energy injection machine are lowered.

BRIEF DESCRIPTION OF THE DRAWINGS

15 [0018] FIG. 1 is a schematic structural view of a NLDMOS device according to an embodiment of the invention.

[0019] FIG. 2 is a schematic sectional view taken along A-A' direction of Fig. 1.

DETAILED DESCRIPTION OF THE INVENTION

20 [0020] Fig. 1 illustrates a schematic structural view of a NLDMOS device according to the invention. The NLDMOS device includes a substrate lead-out 101, an source region lead-out 103, a gate lead-out 105, a first field oxide region 107, a second field oxide region 109, a drain end lead-out 111, a N type drift region 113 made by high voltage N well, a floating P type structure (floating P structure) 115, a buried oxide layer 117 and a substrate 119 made by high voltage P well, wherein the N type drift region 113 is located on the buried oxide layer 117, the substrate 119 adjacent to the N type drift region 113 is located on the buried oxide layer 117, and the floating P type structure 115 is disposed within the N
25 type drift region 113.

[0021] By adjusting concentrations of impurities in various parts, the range of breakdown voltage of the above NLDMOS device can reach 100V~1000V.

[0022] The floating P type structure 115 is located in the middle portion of the N type drift region 113 along the channel direction of the N type drift region 113 and the number thereof is not limited to one, i.e., there can be two and more floating P type structures 115 (as shown in Fig. 2). The floating P type structure 115 is of a stripe shape in layout and the cross section of the floating P type structure is in a rectangular shape. The floating P type structure 115 is injected into the middle portion of the N type drift region 113 by high energy. The injection energy is 200Kev~2000Kev and can be suitably adjusted according to the impurity distribution of the N type drift region 113 and the thickness of the epitaxial process. The dose of the floating P type structure 115 is required to achieve an electrical charge balance with the N type drift region 113. The floating P type structure 115 located in the middle portion of the N type drift region 113 can deplete N type impurities in the lateral direction and the longitudinal direction, thus facilitating the depletion of the N type drift region 113, increasing breakdown voltage of the device and reducing on-resistance. Moreover, electrical current can flow along channels in the N type drift region 113 above and under the floating P type structure 115, and the path through which electrical current flows is relative large. By employing the above construction, the impurity concentration of the drift region can be suitably increased so as to further reduce resistance.

[0023] The cross section of the floating P type structure 115 is not limited to rectangle, other shapes are also possible, such as circle, as long as these shapes are advantageous to the depletion of the N type drift region.

[0024] The first field oxide region 107 and the second field oxide region 109 are disposed on the N type drift region 113 to face each other. The first field oxide region 107 and the second field oxide region 109 do not completely cover the N type drift region 113. Therefore, the region between the first field oxide region 107 and the second field oxide region 109 remains to be an active region. The width of the active region between the first field oxide region 107 and the second field oxide region 109 matches with the length of the injected floating P type structure 115. The length of the first field oxide region 107 can be different from that of the second field oxide region 109.

[0025] Conventionally, the whole drift region of a NLDMOS device with a breakdown voltage which is above 100V is covered by a field oxide region. Since the floating P type structure 115 has to be injected into a middle portion of the N type drift region, a very high

injection energy is necessary, thus requiring that the injection machine must realize a high energy injection and that the photoresist is thick enough so as to block the floating P type structure 115 from being injected into other regions. In the embodiment, the active region made between the first field oxide region 107 and the second field oxide region 109 has a relatively thin oxide layer, thus facilitating the injection of the floating P type structure 115 and reducing the requirements on the energy of injection machine and the thickness of photoresist, such that a floating P type structure 115 can be formed with a smaller width and spacing and the injection peak value of the floating P type structure 115 is deeper, making it easier to realize in manufacturing.

10 [0026] According to an embodiment of the invention, a method of manufacturing the above-described NLDMOS device includes the following steps of:

[0027] step 1): forming an epitaxial layer on a buried oxide layer by conventional epitaxial manufacturing process;

15 [0028] step 2): performing well injection by conventional MOS process to form the N type drift region;

[0029] step 3): forming the first field oxide region and the second field oxide region by growth, the active region located between the first field oxide region and the second field oxide region, wherein the size of the active region matches with the length of a floating P type structure to be injected;

20 [0030] step 4): performing injection for a source region, a gate region and a drain region; and

[0031] step 5): injecting a floating P type structure into the middle portion of the N type drift region through the active region between the first field oxide region and the second field oxide region.

25 [0032] Since the device according to the embodiment of the invention is made on a silicon-on-insulator (SOI) wafer, there is a buried oxide layer. It is appreciated by those skilled in the art that the use of the SOI wafer intends to enhance isolation effect of the device and should not be construed as limiting the invention.

30 [0033] The five steps described above are only main steps required, and it is apparent that those skilled in the art are familiar with well known details that have not been

mentioned.

[0034] In the embodiment of the invention, the injection of the floating P type structure 115 is performed after the injection for the source region and a drain region, so that the floating P type structure 115 is subject to less thermal process, thus avoiding the reduction of N type impurity concentration caused by diffusion of P type impurity and the increase of on-resistance caused by increase in size of the floating P type structure 115, etc.

[0035] Described above are only several embodiments of the invention, which are described in a relatively specific and detailed manner. However, they should not be construed as limiting the scope of the invention. It is noted that many variations and modifications can be made by those with ordinary skills in the art under the premise that they do not depart the concept of the invention, which all fall within the scope of protection of the invention. Therefore, the scope of protection of the invention is defined by the appended claims.

CLAIMS

1. An NLDMOS device, comprising a floating P type structure, a first field oxide region, a second field oxide region and a N type drift region, wherein the first field oxide region and the second field oxide region are disposed on the N type drift region, wherein
5 the floating P type structure is located in the middle portion of the N type drift region along the channel direction of the N type drift region, and wherein the width of active region between the first field oxide region and the second field oxide region is no less than the length of the floating P type structure.

10 2. The NLDMOS device according to claim 1, wherein the number of the floating P type structure is no less than two.

3. The NLDMOS device according to claim 1, wherein the floating P type structure is in a stripe shape and the cross section of the floating P type structure is in a
15 rectangular shape.

4. The NLDMOS device according to claim 1, wherein the cross section of the floating P type structure is in a circular shape.

20 5. The NLDMOS device according to claim 1, wherein the length of the first field oxide region is different from that of the second field oxide region.

6. A method of manufacturing NLDMOS device comprising a floating P type structure, a first field oxide region, a second field oxide region and a N type drift region,
25 wherein the first field oxide region and the second field oxide region are disposed on the N type drift region, wherein the method comprises:

step 1): forming an epitaxial layer on a buried oxide layer by epitaxial manufacturing process;

step 2): performing well injection by MOS process to form the N type drift region;

step 3): growing the first field oxide region and the second field oxide region, an active region located between the first field oxide region and the second field oxide region, wherein size of the active region matches with length of the floating P type structure to be injected;

step 4): performing injection for a source region, a gate region and a drain region; and

step 5): injecting the floating P type structure into the middle portion of the N type drift region through the active region between the first field oxide region and the second field oxide region.

7. The method of manufacturing NLD MOS device according to claim 6, wherein the injection energy of the floating P type structure is 200Kev~2000Kev.

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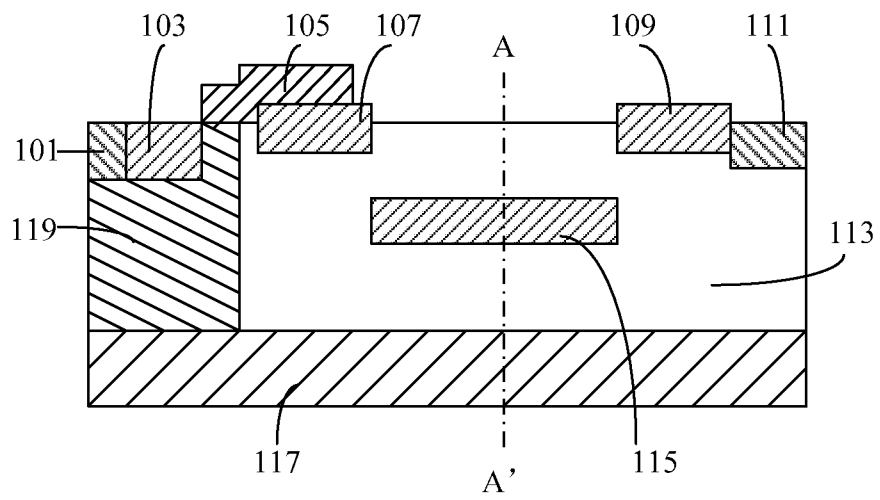


Figure 1

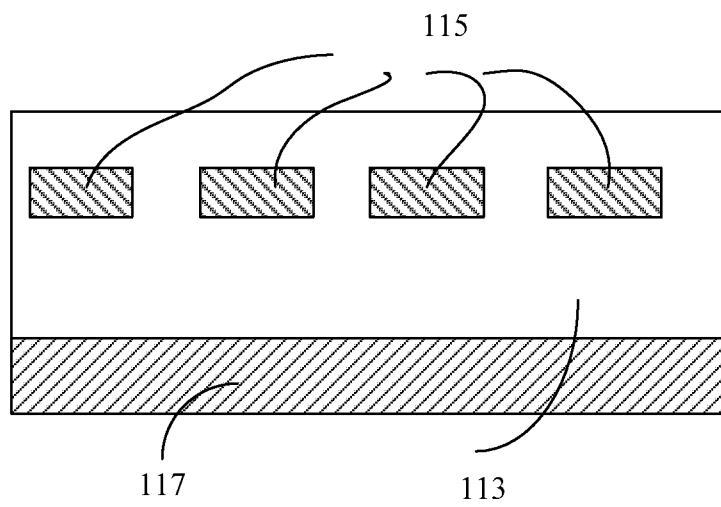


Figure 2

INTERNATIONAL SEARCH REPORT

International application No.

PCT/CN2010/079412

A. CLASSIFICATION OF SUBJECT MATTER

See extra sheet

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC: H01L21/-, H01L27/-, H01L29/-

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

WPI, EPODOC, CNKI, CNABS: float+, drift, field, oxide, active, breakdown, voltage, on-resistance

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	CN101488526A (UNIV SOUTHEAST) 22 Jul. 2009(22. 07. 2009) pages 3-5 and figs. 1-3	1-7
Y	JP2001274414 A (TOSHIBA KK) 05 Oct. 2001(05. 10. 2001) abstract and figs. 1 and 4	1-7
A	CN101593774A (SUZHOU POWERON IC DESIGN CO LT) 02 Dec. 2009(02. 12. 2009) the whole document	1-7
A	US6274904B1 (TIHANYI) 14 Aug. 2001(14. 08. 2001) the whole document	1-7
A	US2007/0272978A1 (MAUDER et al.) 29 Nov. 2007(29. 11. 2007) the whole document	1-7
A	US2006/0267044A1 (YANG) 30 Nov. 2006(30. 11. 2006) the whole document	1-7

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:	"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A" document defining the general state of the art which is not considered to be of particular relevance	"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
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"L" document which may throw doubts on priority claim (S) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&" document member of the same patent family
"O" document referring to an oral disclosure, use, exhibition or other means	
"P" document published prior to the international filing date but later than the priority date claimed	

Date of the actual completion of the international search 18 Feb. 2011 (18. 02. 2011)	Date of mailing of the international search report 17 Mar. 2011 (17.03.2011)
Name and mailing address of the ISA/CN The State Intellectual Property Office, the P.R.China 6 Xitucheng Rd., Jimen Bridge, Haidian District, Beijing, China 100088 Facsimile No. 86-10-62019451	Authorized officer LUO, Sufang Telephone No. (86-10)62411026

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
PCT/CN2010/079412

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INTERNATIONAL SEARCH REPORT

International application No.

PCT/CN2010/079412

CLASSIFICATION OF SUBJECT MATTER

H01L 29/78 (2006. 01) i

H01L 21/336 (2006. 01) i