

[54] **COMBINATION MONOSTABLE AND ASTABLE INDUCTOR DRIVER**

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[58] Field of Search **317/154, DIG. 4, 148.5**

[56] **References Cited**

UNITED STATES PATENTS

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[57] **ABSTRACT**

A driver is disclosed that is particularly adapted to deliver excitation to solenoids characterized by a high ratio of pull-in current to holding current. In order to minimize the continuous current rating of a solenoid required in a given application, the solenoid is pulsed with holding current after pull-in is effected. The driver employs solid state timing circuitry having monostable and astable modes of operation controlled by capacitors provided with independent charging and discharging circuits. After the initial, monostable mode in which the driving excitation is uninterrupted, the timing circuitry automatically goes into the astable mode to pulse the solenoid in accordance with a predetermined duty cycle which may be set at either less than or greater than fifty percent throughout a wide range as required.

8 Claims, 5 Drawing Figures

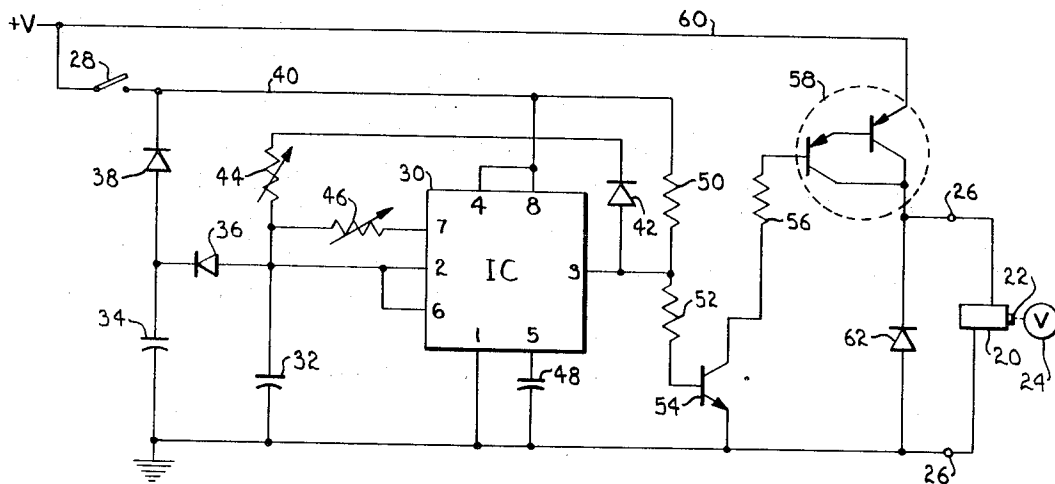


Fig. 1.

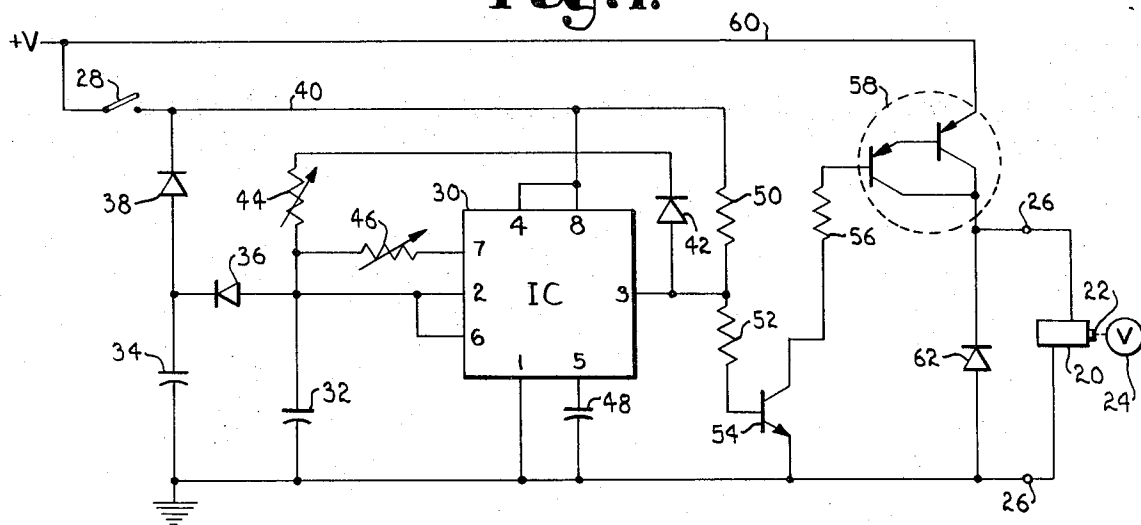


Fig. 2.

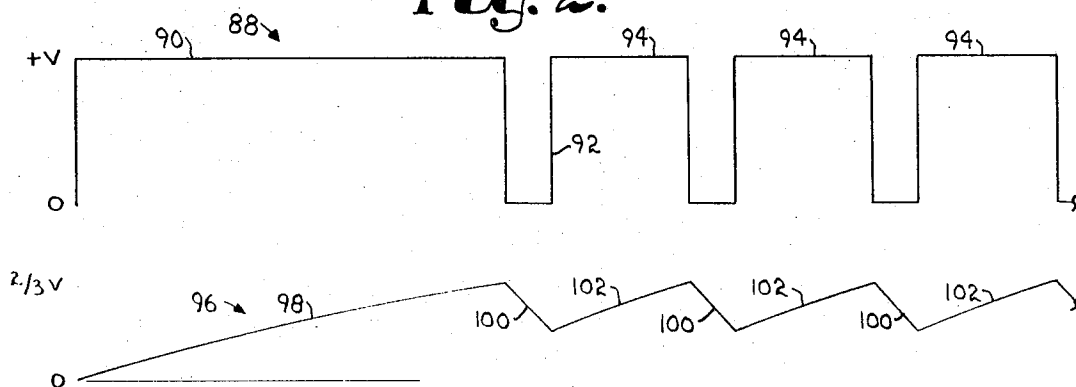
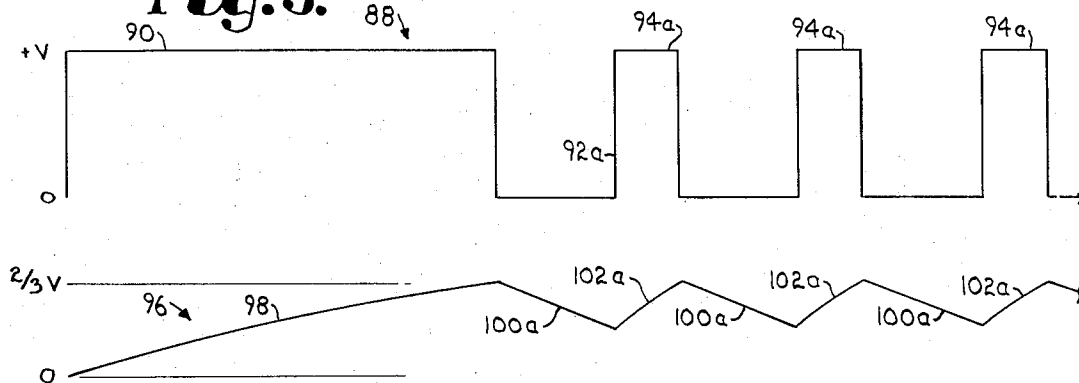
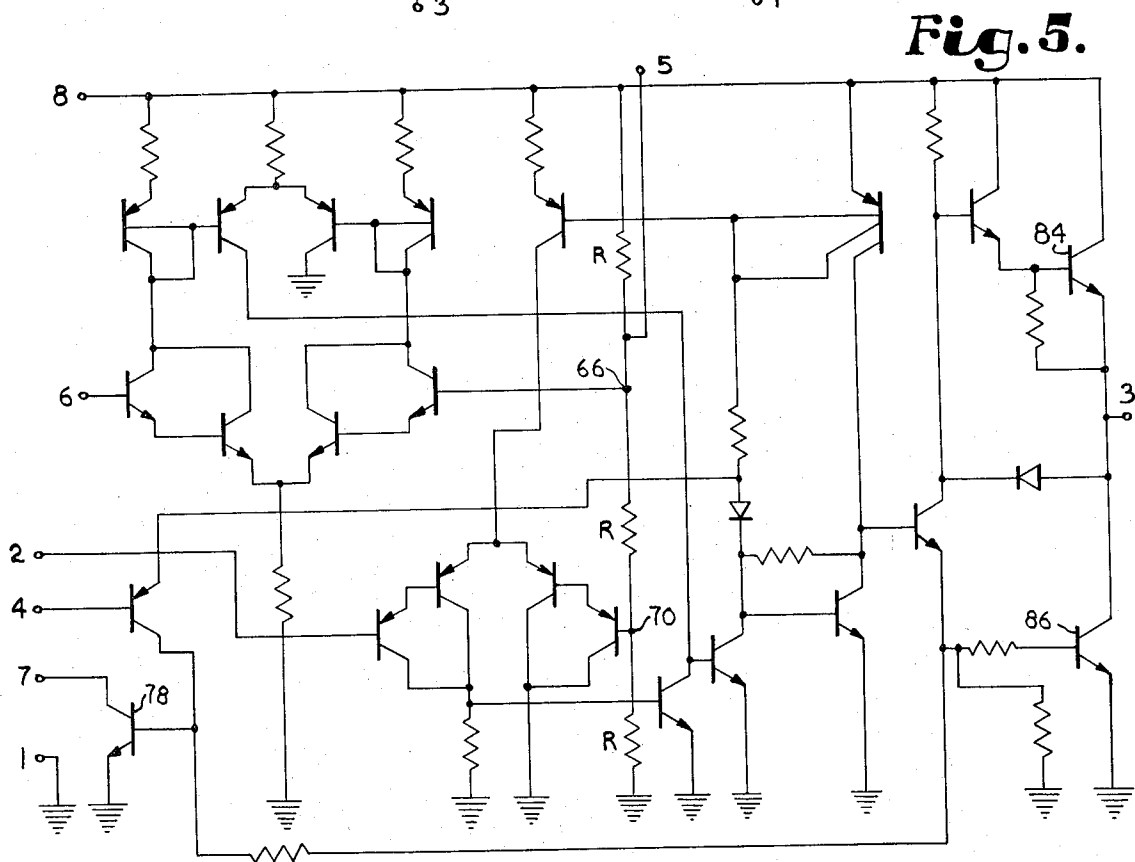
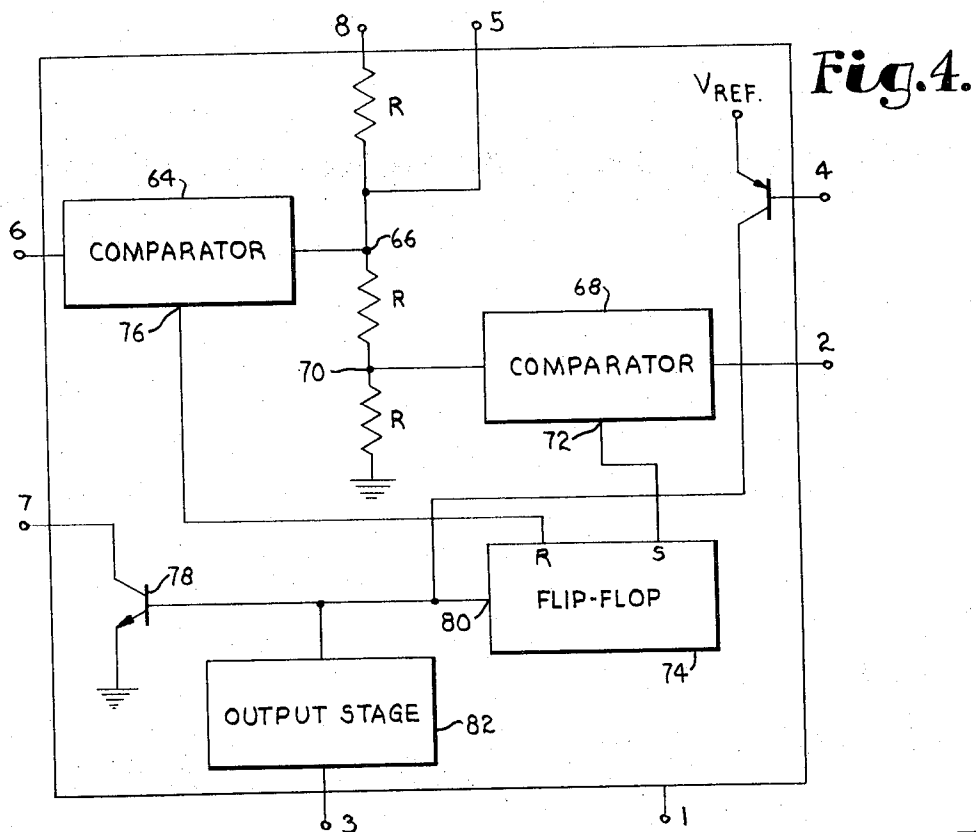


Fig. 3.





COMBINATION MONOSTABLE AND ASTABLE INDUCTOR DRIVER

This invention relates to driver apparatus for delivering electrical excitation which is uninterrupted during an initial period followed by intermittent delivery at a predetermined duty cycle and, in particular, to a driver which is uniquely adapted for solenoid control applications.

Solenoids are inherently characterized by a high ratio of pull-in current to drop-out current due to air gap changes in the magnetic circuit occurring with armature movement. Accordingly, once the armature completes its stroke, the excitation requirements of the solenoid coil decrease significantly, thereby making it possible to realize a substantial power saving by reducing the drive. The alternative is to select a solenoid having a continuous current rating that is sufficiently high to permit operation at the pull-in current level at all times. However, besides consuming considerably more power, this requires that a more expensive, heavier-duty solenoid coil be utilized than is really necessary for the particular control application.

In an effort to take advantage of a reduced continuous current rating, mechanical switches operated by the solenoid armatures have been employed to switch the operating potential on a DC solenoid to a lower level once the armature completes its stroke. Mechanical latches have also been utilized. However, these approaches all suffer from the disadvantage that mechanical parts subject to wear and ultimate failure must be employed, thereby increasing the cost of the solenoid device both initially and from the standpoint of continuing servicing and maintenance. Furthermore, the problem is enhanced in the case of armature-operated switches due to contact wear inherent in switching an inductive load.

It is, therefore, an important object of the present invention to provide a driver for solenoids that is devoid of mechanical parts and yet capable of reducing the excitation to the solenoid coil following pull-in, in order to minimize the required continuous current rating of the solenoid.

As a corollary to the foregoing object, it is an important aim of this invention to provide a driver as aforesaid which is not subject to the disadvantages inherent in mechanical arrangements for reducing the solenoid drive discussed hereinabove, and which has a normal expected operating life exceeding that of the solenoids it supplies.

It is another important object of this invention to provide a driver as aforesaid which supplies uninterrupted excitation to the solenoid during an initial period at the outset of a timing program commencing with energization of the solenoid coil, followed by intermittent delivery of excitation to the coil after pull-in is completed.

Still another important object of the invention is to provide a driver as aforesaid where the duty cycle after pull-in may be varied over a wide range, including both less than and greater than 50 percent, in order to meet the holding current requirements of the solenoid coil but be purposely limited to preclude unnecessary power consumption.

Furthermore, it is an important object of the present invention to provide driver apparatus, particularly for inductive loads, capable of delivering electrical excitation which is uninterrupted during an initial period fol-

lowed by intermittent delivery at a predetermined duty cycle, wherein the pulse width and spacing during such duty cycle is variable over a wide range to accommodate the particular application.

Additionally, it is an important object of this invention to provide such apparatus wherein control circuitry is employed having monostable and astable modes of operation, and wherein the control circuitry upon activation initially operates in the monostable mode followed by continuous operation in the astable mode.

Yet another important object of the invention is to provide such apparatus having control circuitry as aforesaid wherein, in the astable mode, the output of the circuitry is cycled between first and second voltage levels in accordance with a desired pulse width and spacing of the excitation to be supplied to the external load.

A further and important object is to provide such control circuitry incorporating capacitors with independent charging and discharging circuits wherein the charge and discharge times are employed to govern the duration of the monostable mode and the pulse width and spacing of the output in the astable mode.

In the drawings:

FIG. 1 is an electrical schematic diagram illustrating the driver apparatus of the present invention;

FIG. 2 is a timing diagram showing wave forms that illustrate the operation of the apparatus in applications requiring greater than a 50 percent duty cycle following the initial period of excitation;

FIG. 3 is a timing diagram similar to FIG. 2 but illustrating a duty cycle of less than 50 percent;

FIG. 4 is a block diagram illustrating the functional sections of the integrated circuit timer; and

FIG. 5 is an electrical schematic diagram showing the equivalent circuit for the integrated circuit timer.

Referring initially to FIG. 1, the driver apparatus of the present invention is shown connected to a solenoid 20 having an armature 22 mechanically coupled to a valve 24. In the application illustrated in FIG. 1, the solenoid 20 is being utilized to control the opening and closing of the valve 24 in conjunction with operation of any of various types of equipment, such as the hydraulic valves associated with heavy-duty construction equipment. In such applications the solenoid 20 would be operated from battery potential (typically 12 volts) as represented by the +V notation. The solenoid coil is connected to the supply terminals 26 of the driver, and the latter is activated by closing an on-off switch 28.

An integrated circuit timer 30 is employed in the preferred embodiment of the driver illustrated herein, and has a number of terminals designated by the numerals 1 through 8. Terminal 1 is a ground connection as illustrated by the ground symbol. Terminal 2 is a trigger input, 3 is the output terminal of the timer 30, terminal 4 is a reset, terminal 5 is a control voltage input, terminal 6 is a threshold input, terminal 7 executes a discharge function, and terminal 8 is connected to the supply voltage. The particular integrated circuit illustrated herein is manufactured by Signetics, a subsidiary of Corning Glass Works, of Sunnyvale, Calif., and is currently available under the designation NE/SE 555. Other equivalent integrated circuits may be employed or discrete components may be substituted if desired. The nature of the integrated circuit 30 will be discussed in detail hereinbelow with reference to FIGS. 4 and 5.

In addition to the integrated circuit 30, the driver has a number of additional components which cooperate with the circuit 30 to execute the various control functions of the present invention. It should be noted that the trigger input 2 and the threshold input 6 are interconnected, a capacitor 32 being connected between such terminals and ground. A second capacitor 34 is in parallel with the capacitor 32 through an isolation diode 36 poled to conduct positive current in the direction of the capacitor 34. A reset diode 38 extends from the upper plate of the capacitor 34 to a lead 40 which is at the level of the +V supply when switch 28 is closed.

The capacitor 32 is charged and discharged through independent circuits, the charging circuit being traceable from the output terminal 3 to the capacitor 32 via a diode 42 and a series-connected variable resistor 44. This also serves as the charging circuit for the capacitor 34 through the diode 36. The discharging circuit from capacitor 32 is through a variable resistor 46 to the discharge terminal 7 of the integrated circuit 30. Terminals 4 and 8 are tied to the lead 40, and a noise bypass capacitor 48 is connected between terminal 5 and ground.

The control circuitry comprising the integrated circuit 30 and its associated external components delivers a control signal at the output terminal 3 in the nature of a bilevel output which may be considered either "high" or "low." These are analogous to logic levels with the high level being at the positive supply voltage (+V). A voltage divider consisting of resistors 50 and 52 delivers the output signal to the base of an NPN switching transistor 54 having a grounded emitter. The collector of transistor 54 is connected by a coupling resistor 56 to a Darlington amplifier 58 which serves as a switch between the +V lead 60 and the upper supply terminal 26. A diode 62 is connected across the supply terminals 26 and poled in opposition to the supply voltage to provide transient suppression during switching of the solenoid 20.

Referring to FIG. 4, the integrated circuit timer 30 is revealed in block diagram form. A voltage divider comprising three series connected resistors R of equal value is connected between the supply terminal 8 and ground. A first voltage comparator 64 has a pair of inputs connected to the threshold input 6 and the junction 66 between the upper and center resistors R as they appear in the illustration. A second voltage comparator 68 has a pair of inputs respectively connected to the trigger input 2 and the junction point 70 between the center and lower resistors R. The output 72 of the comparator 68 is connected to the set input S of a flip-flop 74, the output 76 of the comparator 64 being connected to the reset input R of the flip-flop 74.

An NPN transistor 78 is nonconductive when the capacitors 32 and 34 are charging, but is rendered conductive by the output 80 of the flip-flop 74 to discharge the capacitor 32 during astable operation, as will be discussed. The output stage 82 of the timer 30 is responsive to the flip-flop output 80 and delivers the bilevel control signal at terminal 3.

FIG. 5 is an equivalent circuit of the timer 30 shown in block diagram form in FIG. 4. The three resistors R forming the voltage divider are also identified by the letter R in FIG. 5. When the transistor 78 (connected between discharge terminal 7 and ground) is nonconducting during charging of the capacitors 32 and 34, a

transistor 84 connected to output terminal 3 is conducting while a second transistor 86 is in the nonconductive state. Both of the transistors 84 and 86 are of the NPN type, the collector of transistor 84 being connected to the supply terminal 8 while its emitter is directly connected to the output terminal 3. The transistor 86 has its emitter-collector circuit connected between terminal 3 and ground with the emitter being grounded. Accordingly, under the conditions just described with transistor 84 on and transistor 86 off, output terminal 3 is at the high or +V voltage level. Conversely, reversal of the states of these two transistors places output terminal 3 at the low level (ground potential); at this time the transistor 78 is conducting and the capacitor 32 is discharging.

The control circuitry of the present invention has monostable and astable modes of operation as illustrated by the timing diagrams in FIGS. 2 and 3. Referring to FIG. 2, the wave form 88 represents the output signal occurring at the output terminal 3 of timer 30. As discussed above, the signal is either at the high level or the low level indicated by +V and 0 respectively. The wave form 88 is also representative of a timing program having an uninterrupted initial period 90 followed by intermittent delivery of high level voltage commencing on the positive excursion 92 of the first pulse 94 after the long initial period 90. A series of three such pulses 94 is illustrated, it being understood that the pulses 94 continue indefinitely as long as the solenoid 20 is in operation.

A second wave form 96 is illustrated in FIG. 2 correlated in time with the wave form 88. Wave form 96 represents the voltage at the interconnected terminals 2 and 6 of the timer 30. Starting from 0, initial charging of the capacitors 32 and 34 occurs along a ramp 98 coinciding with the long initial period 90. The end of the ramp 98 is at a voltage level equal to $\frac{2}{3}$ of the supply voltage V. Capacitor discharge is illustrated by the abrupt negative excursions 100, each being followed by a short charging ramp 102. The lower limit of each negative excursion 100 is at a voltage level equal to $\frac{1}{3}$ of the supply voltage.

The operation illustrated in FIG. 3 is similar to FIG. 2 except that the duty cycle of the driver during the astable mode of operation is less than 50 percent, whereas a duty cycle significantly over 50 percent is illustrated in FIG. 2. The same reference numerals are used with the addition of the *a* notation.

OPERATION

The capacitance of capacitor 34 is much larger than that of capacitor 32 in order to assure that the duration of the initial period 90 will be sufficiently long to fulfill the pull-in current requirements of the solenoid 20, irrespective of the value of the resistor 44. Upon closure of the switch 28, the control circuitry is activated and the parallel capacitors 32 and 34 begin charging via the charging circuit from output terminal 3 through diode 42 and resistor 44. At this time, the transistor 78 (FIGS. 4 and 5) is nonconductive and the output terminal 3 is at the high level. Accordingly, there is no conduction of current through the resistor 46 to the discharge terminal 7.

Charging continues as shown by the ramp 98 (FIGS. 2 and 3) until such time that the voltage developed across capacitors 32 and 34 reaches $\frac{2}{3}$ V. This is sensed by comparator 64 since one of its inputs is connected

to terminal 6 and its other input is connected to the junction 66, the latter being maintained at the $\frac{2}{3}$ V level by the voltage divider action of the three resistors R. When a voltage differential ceases to exist at the two inputs to the comparator 64, it delivers an output at the high level to the reset input R of the flip-flop 74. This causes the output 80 of the flip-flop 74 to go from the low to the high level, thereby gating the transistor 78 and commencing the discharge of capacitor 32. It should be noted that the diode 36 precludes any significant discharge of capacitor 34 so that the latter has little affect on subsequent operation of the circuitry. Also at this time, the output stage 82 of the integrated circuit timer 30 causes the output terminal 3 to go to the low level (terminal 3 is effectively shunted to ground by the conduction of transistor 86 shown in FIG. 5).

In FIG. 2 the discharge of the capacitor 32 is illustrated by the ramp 100. Since the comparator 68 has its inputs connected to the junction point 70 and terminal 2, it senses the absence of a differential voltage at the time that the voltage across capacitor 32 falls to the $\frac{2}{3}$ V level. Accordingly, the flip-flop 74 is set at this time to again place transistor 78 in the nonconducting state and cause the output at terminal 3 to go to the high level. Charging now begins again, but this time only the capacitor 32 is charged through the resistor 44. Charging is illustrated by the shorter ramp 102 beginning in coincidence with the leading excursion 92 of the first pulse 94.

The control signal depicted by the wave forms 88 in FIGS. 2 and 3 renders switching transistor 54 conductive when the control signal is at the high level, and nonconductive when the control signal is at the low level. Accordingly, transistor 54 and the succeeding Darlington amplifier stage 58 constitute an electrically responsive, bistate switch which controls delivery of supply voltage to the upper supply terminal 26 in accordance with the level of the control signal appearing at output terminal 3 of the timer 30. During the initial period 90, excitation of the solenoid coil was uninterrupted but now, as the circuitry begins its astable mode of operation, power to the solenoid 20 is cycled on and off in accordance with the frequency of the control signal. Both pulse width and pulse spacing at the supply terminals 26 may be independently controlled by the variable resistors 44 and 46 to conform the duty cycle to the holding current requirements of the solenoid. Thus, the required continuous current rating of the solenoid is minimized and power is conserved.

During the monostable mode of operation when both of the capacitors 32 and 34 are charging, the time constant is a function of the value of resistor 44 multiplied by the sum of the capacities of capacitors 32 and 34. As mentioned hereinabove, the value of capacitor 34 would be selected so as to be much greater than the value of capacitor 32, thereby minimizing the effect of capacitor 32 on the period 90. During the subsequent astable mode of operation, however, the time constant is a function of the product of the ohmic value of resistor 44 and the capacitance of capacitor 32 alone. Then, during discharge, the time constant is a function of the product of the ohmic value of resistor 46 and the capacitance of capacitor 32. Accordingly, during the astable mode, the charge time and the discharge time are entirely independent of each other so that the duty cycle is theoretically variable over an unlimited range. This enables the driver to accommodate a variety of

load requirements as exemplified by a comparison of the pulse width and spacing in FIGS. 2 and 3. In FIG. 2 the duty cycle well over 50 percent, while in FIG. 3 the duty cycle is less than 50 percent.

When the switch 28 is reopened, the diode 38 allows the larger capacitor 34 to discharge so that the driver is rapidly reset in readiness for a subsequent closure of switch 28. It should be understood that, although the resistors 44 and 46 are illustrated as variable, this is done to demonstrate the independent setting of variables in the present invention, thus in practice both resistors may be fixed at values determined by a particular application.

Having thus described the invention, what is claimed as new and desired to be secured by Letters Patent is:

1. In actuator apparatus employing a solenoid characterized by a relatively high ratio of required pull-in current to required holding current, a driver for operating said solenoid comprising:

supply terminal means connected to said solenoid for supplying the latter with operating potential;

electrically responsive, bistate switching means connected with said terminal means for applying said potential thereto when said switching means is in a first operational state, and for interrupting application of said potential to said terminal means when said switching means is in a second, normal operational state; and

control means coupled with said switching means for delivering an electrical control signal thereto in accordance with a timing program selected to provide the pull-in current requirements of said solenoid and hold the solenoid following pull-in,

said control means upon activation thereof causing said switching means to initially assume said first state for a predetermined, uninterrupted time period at the outset of said program corresponding to said pull-in requirements, and thereafter cycling said switching means between said first and second states to provide a pulse width and spacing at said terminal means which supplies sufficient holding current to the solenoid,

said control signal having first and second levels and said control means delivering said signal at said first level during said time period at the outset of said program and thereafter cycling said signal between said first and second levels to cause said switching means to assume said first and second states thereof respectively in response to said first and second levels of the signal,

said control means including first capacitor means, charging and discharging circuit means connected with said first capacitor means, operating means responsive to predetermined minimum and maximum voltages developed across said first capacitor means for causing the latter to charge via said circuit means when the voltage across said first capacitor means falls to said minimum, and to discharge via said circuit means when said voltage rises to said maximum, and output means for delivering said control signal at said first level during charging of the first capacitor means and at said second level during discharge thereof, whereby said first capacitor means, charging and discharging circuit means, and operating means control said pulse width and spacing at said terminal means to provide a prede-

terminated duty cycle following said uninterrupted time period at the outset of said program, said control means being provided with second capacitor means of substantial capacitance, and means electrically connecting said second capacitor means with said circuit means during charging operation thereof but electrically isolating said second capacitor means therefrom during discharging operation of said circuit means, whereby upon said activation of the control means both the first and second capacitor means charge over a time duration terminating when said voltage reaches said maximum, said time duration defining said uninterrupted time period at the outset of said program.

2. Driver apparatus for delivering electrical excitation which is uninterrupted during an initial period followed by intermittent delivery at a predetermined duty cycle, said apparatus comprising:

supply terminal means for delivering said excitation to an external load connected thereto;

electrically responsive, bistate switching means connected with said terminal means for applying said excitation thereto when said switching means is in a first operational state, and for interrupting application of said excitation to said terminal means when said switching means is in a second, normal operational state; and

control circuitry coupled with said switching means and having first and second electrical output levels causing said switching means to assume said first and second states thereof respectively,

said control circuitry having monostable and astable modes of operation and, upon activation thereof, initially operating in said monostable mode followed by continuous operation in said astable mode,

said control circuitry in said monostable mode delivering an output signal at said first level for said initial period and, in said astable mode, cycling said output signal between said first and second levels in accordance with a pulse width and spacing corresponding to said predetermined duty cycle, whereby said uninterrupted and then intermittent excitation is available at said terminal means,

said control circuitry including first capacitor means, charging and discharging circuit means connected with said first capacitor means, operating means responsive to predetermined minimum and maximum voltages developed across said first capacitor means for causing the latter to charge via said circuit means when the voltage across said first capacitor means falls to said minimum, and to discharge via said circuit means when said voltage rises to said maximum, and output means for delivering said output signal at said first level during charging of the first capacitor means and at said second level during discharge thereof, whereby said first capacitor means, charging and discharging circuit means, and operating means establish said duty cycle,

said control circuitry being provided with second capacitor means of substantial capacitance, and means electrically connecting said second capacitor means with said circuit means during charging operation thereof but electrically isolating said second capacitor means therefrom during discharging operation of said circuit means, whereby upon said activation of the control circuitry both the first and second capacitor means charge over a time duration terminating when said voltage reaches said maximum, said time duration defining said initial period occurring during said monostable mode of operation.

3. The apparatus as claimed in claim 2 wherein said operating means includes comparator means connected with said first and second capacitor means for detecting the occurrence of said minimum and maximum voltages.

4. The apparatus as claimed in claim 2, wherein said circuit means has independent charging and discharging circuits operably coupled with said first capacitor means, and means in said independent circuits for varying the duration of said output signal at said first and second levels in said astable mode, whereby said duty cycle may be set at either less than or greater than 50 percent.

5. The apparatus as claimed in claim 4, wherein said charging circuit is connected with said output means for applying said output signal to said first and second capacitor means when the signal is at said first level, there being means electrically isolating said charging circuit from said output means when said output signal is at its second level, whereby to maintain said charging circuit completely independent from said discharging circuit.

6. The apparatus as claimed in claim 1, wherein said operating means includes comparator means connected with said first and second capacitor means for detecting the occurrence of said minimum and maximum voltages.

7. The apparatus as claimed in claim 1, wherein said circuit means has independent charging and discharging circuits operably coupled with said first capacitor means, and means in said independent circuits for varying the duration of said control signal at said first and second levels following said time period at the outset of said program, whereby to control said pulse width and spacing at said terminal means to provide a duty cycle either less than or greater than 50 percent.

8. The apparatus as claimed in claim 7, wherein said charging circuit is connected with said output means for applying said control signal to said first and second capacitor means when the signal is at said first level, there being means electrically isolating said charging circuit from said output means when said control signal is at its second level, whereby to maintain said charging circuit completely independent from said discharging circuit.

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