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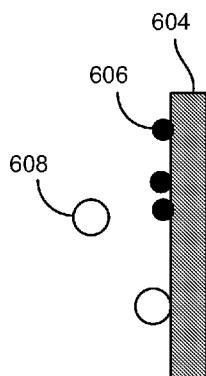


FIG. 6B

(57) Abstract: Development of resists are useful, for example, to form a patterning mask in the context of high-resolution patterning. Development can be accomplished using an organic vapor such as a carboxylic acid. In some implementations, the organic vapor is trifluoroacetic acid. In some implementations, the organic vapor is hexafluoro-acetylacetone. A metal-containing resist film such as an EUV-sensitive organo-metal oxide may be deposited on a semiconductor substrate using a dry or wet deposition technique. The metal-containing resist film on the semiconductor substrate may be developed using the organic vapor, or residue of metal-containing resist material formed on surfaces of a process chamber may be removed using the organic vapor.



## PHOTORESIST DEVELOPMENT WITH ORGANIC VAPOR

### INCORPORATION BY REFERENCE

[0001] A PCT Request Form is filed concurrently with this specification as part of the present application. Each application that the present application claims benefit of or priority to as  
5 identified in the concurrently filed PCT Request Form is incorporated by reference herein in its entirety and for all purposes.

### BACKGROUND

[0002] The fabrication of semiconductor devices, such as integrated circuits, is a multi-step process involving photolithography. In general, the process includes the deposition of material on  
10 a wafer, and patterning the material through lithographic techniques to form structural features (e.g., transistors and circuitry) of the semiconductor device. The steps of a typical photolithography process known in the art include: preparing the substrate; applying a photoresist, such as by spin coating; exposing the photoresist to light in a desired pattern, causing the exposed areas of the photoresist to become more or less soluble in a developer solution; developing by applying a  
15 developer solution to remove either the exposed or the unexposed areas of the photoresist; and subsequent processing to create features on the areas of the substrate from which the photoresist has been removed, such as by etching or material deposition.

[0003] The evolution of semiconductor design has created the need, and has been driven by the ability, to create ever smaller features on semiconductor substrate materials. This progression of  
20 technology has been characterized in “Moore’s Law” as a doubling of the density of transistors in dense integrated circuits every two years. Indeed, chip design and manufacturing has progressed such that modern microprocessors may contain billions of transistors and other circuit features on a single chip. Individual features on such chips may be on the order of 22 nanometers (nm) or smaller, in some cases less than 10 nm.

[0004] One challenge in manufacturing devices having such small features is the ability to  
25 reliably and reproducibly create photolithographic masks having sufficient resolution. Current photolithography processes typically use 193 nm ultraviolet (UV) light to expose a photoresist. The fact that the light has a wavelength significantly greater than the desired size of the features to be produced on the semiconductor substrate creates inherent issues. Achieving feature sizes  
30 smaller than the wavelength of the light requires use of complex resolution enhancement techniques, such as multipatterning. Thus, there is significant interest and research effort in

developing photolithographic techniques using shorter wavelength light, such as extreme ultraviolet radiation (EUV), having a wavelength of from 10 nm to 15 nm, e.g., 13.5 nm.

[0005] EUV photolithographic processes can present challenges, however, including low power output and loss of light during patterning. Traditional organic chemically amplified resists (CAR) similar to those used in 193 nm UV lithography have potential drawbacks when used in EUV lithography, particularly as they have low absorption coefficients in EUV region and the diffusion of photo-activated chemical species can result in blur or line edge roughness. Furthermore, in order to provide the etch resistance required to pattern underlying device layers, small features patterned in conventional CAR materials can result in high aspect ratios at risk of pattern collapse. Accordingly, there remains a need for improved EUV photoresist materials, having such properties as decreased thickness, greater absorbance, and greater etch resistance.

[0006] The background description provided herein is for the purpose of generally presenting the context of the present technology. Work of the presently named inventors, to the extent it is described in this background section, as well as aspects of the description that may not otherwise qualify as prior art at the time of filing, are neither expressly nor impliedly admitted as prior art against the present technology.

#### SUMMARY

[0007] Provided herein is a method of developing a photopatterned metal-containing resist. The method includes providing in a process chamber a photopatterned metal-containing resist on a surface of a semiconductor substrate, and dry developing the photopatterned metal-containing resist by selectively removing a portion of the resist by exposure to a development chemistry comprising an organic vapor to form a resist mask.

[0008] In some implementations, the organic vapor comprises a carboxylic acid. In some implementations, the organic vapor comprises trifluoroacetic acid. In some implementations, the organic vapor comprises trifluoroacetic acid anhydride, acetic acid anhydride, trichloroacetic acid, mono-fluoroacetic acid, di-fluoroacetic acid, chloro-difluoro-acetic acid, thioacetic acid, or thioglycolic acid. In some implementations, the organic vapor comprises hexafluoro-acetylacetone. In some implementations, the development chemistry comprises a mixture in a vapor phase of a halogenated carboxylic acid and a hydrogen halide. In some implementations, dry developing the photopatterned metal-containing resist comprises reacting the organic vapor with the photopatterned metal-containing resist to form a volatile compound at a temperature less than about 200°C. In some implementations, dry developing the photopatterned metal-containing resist comprises exposure to at least the organic vapor in a plasma-free thermal process. In some

implementations, the photopatterned metal-containing resist is a photopatterned metal-containing EUV resist, where the photopatterned metal-containing EUV resist is an organo-metal oxide or organo-metal-containing film. In some implementations, dry developing the photopatterned metal-containing resist comprises selectively removing an EUV-unexposed portion of the resist  
5 relative to an EUV-exposed portion with the development chemistry to form the resist mask.

**[0009]** Also provided herein is a method of removing residue from one or more surfaces of a process chamber. The method includes depositing in a process chamber, a metal-containing resist material on a surface of a semiconductor substrate, where a portion of the metal-containing resist material forms a residue on one or more surfaces of the process chamber, and introducing a dry  
10 etchant comprising an organic vapor into the process chamber, where the dry etchant at least partially removes the residue on the one or more surfaces of the process chamber.

**[0010]** In some implementations, the organic vapor comprises a carboxylic acid. In some implementations, the organic vapor comprises trifluoroacetic acid. In some implementations, the organic vapor comprises trifluoroacetic acid anhydride, acetic acid anhydride, trichloroacetic acid, mono-fluoroacetic acid, di-fluoroacetic acid, chloro-difluoro-acetic acid, thioacetic acid, or thioglycolic acid. In some implementations, the organic vapor comprises hexafluoroacetylacetone. In some implementations, the dry etchant comprises a mixture in a vapor phase of a halogenated carboxylic acid and a hydrogen halide. In some implementations, at least partial removal of the residue comprises reacting the organic vapor with the metal-containing resist  
15 material to form a volatile compound at a temperature less than about 200°C. In some implementations, at least partial removal of the residue comprises exposure to at least the organic vapor in a plasma-free thermal process. In some implementations, the metal-containing resist material is an organo-metal oxide or organo-metal-containing film. In some implementations, the method further includes purging the process chamber after introducing the dry etchant to remove residual dry etchant from the process chamber, and conditioning the one or more surfaces of the process chamber by forming a protective coating of the metal-containing resist material on the one  
20 or more surfaces of the process chamber.

### BRIEF DESCRIPTION OF DRAWINGS

**[0011]** Figure 1 presents a flow diagram of an example method for depositing and developing a photoresist according to some implementations.  
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**[0012]** Figure 2 presents a flow diagram of an example method of dry developing a metal-containing resist according to some implementations.

[0013] Figures 3A–3C show cross-sectional schematic illustrations of various processing stages of dry development according to some implementations.

[0014] Figure 4A shows cross-sectional schematic illustrations of dry development without applying inert gas plasma according to some implementations.

5 [0015] Figure 4B shows cross-sectional schematic illustrations of dry development cycling inert gas plasma for descumming according to some implementations.

[0016] Figure 5 presents a flow diagram of an example method of dry chamber cleaning according to some implementations.

10 [0017] Figures 6A–6D show cross-sectional schematic illustrations of various processing stages of dry chamber cleaning according to some implementations.

[0018] Figure 7 depicts a schematic illustration of an example process station that is suitable for performing dry development, clean, rework, descum, and smoothing operations according to some implementations.

15 [0019] Figure 8 depicts a schematic illustration of an example multi-station processing tool suitable for implementation of various dry development, clean, rework, descum, and smoothing operations described herein.

[0020] Figure 9 shows a cross-sectional schematic view of an example inductively-coupled plasma apparatus for implementing certain implementations and operations described herein.

20 [0021] Figure 10 depicts a semiconductor process cluster tool architecture with vacuum-integrated deposition and patterning modules that interface with a vacuum transfer module, suitable for implementations of processes described herein.

[0022] Figure 11A depicts a cross-sectional schematic view of an example of a dry deposition apparatus according to some implementations.

25 [0023] Figure 11B depicts a detailed side section and plan views of a portion of a top plate, substrate, and edge ring of a dry deposition apparatus according to some implementations.

#### DETAILED DESCRIPTION

[0024] This disclosure relates generally to the field of semiconductor processing. In particular aspects, the disclosure is directed to processes and apparatuses for development of photoresists (e.g., EUV-sensitive metal and/or metal oxide-containing photoresists) using organic vapors such  
30 as organic acids, for example to form a patterning mask in the context of EUV patterning or other wavelength patterning. While discussion below may be focused on EUV photoresists, it will be

apparent that the photoresists discussed herein may also be appropriate for use with other wavelengths of radiation, and the techniques and apparatuses discussed herein are not limited solely to EUV photoresist manufacturing.

**[0025]** Reference is made herein in detail to specific embodiments of the disclosure. Examples of the specific embodiments are illustrated in the accompanying drawings. While the disclosure will be described in conjunction with these specific embodiments, it will be understood that it is not intended to limit the disclosure to such specific embodiments. On the contrary, it is intended to cover alternatives, modifications, and equivalents as may be included within the spirit and scope of the disclosure. In the following description, numerous specific details are set forth in order to provide a thorough understanding of the present disclosure. The present disclosure may be practiced without some or all of these specific details. In other instances, well known process operations have not been described in detail so as to not unnecessarily obscure the present disclosure.

## 15 Introduction

**[0026]** Patterning of thin films in semiconductor processing is often an important step in the fabrication of semiconductors. Patterning involves lithography. In conventional photolithography, such as 193 nm photolithography, patterns are printed by emitting photons from a photon source onto a mask and printing the pattern onto a photosensitive photoresist, thereby causing a chemical reaction in the photoresist that, after development, removes certain portions of the photoresist to form the pattern.

**[0027]** Advanced technology nodes (as defined by the International Technology Roadmap for Semiconductors) include nodes 22 nm, 16 nm, and beyond. In the 16 nm node, for example, the width of a typical via or line in a Damascene structure is typically no greater than about 30 nm. Scaling of features on advanced semiconductor integrated circuits (ICs) and other devices is driving lithography to improve resolution.

**[0028]** Extreme ultraviolet (EUV) lithography can extend lithography technology by moving to smaller imaging source wavelengths than would be achievable with conventional photolithography methods. EUV light sources at approximately 10–20 nm, or 11–14 nm wavelength, for example 13.5 nm wavelength, can be used for leading-edge lithography tools, also referred to as scanners. The EUV radiation is strongly absorbed in a wide range of solid and fluid materials including quartz and water vapor, and so operates in a vacuum.

[0029] EUV lithography makes use of EUV resists that are patterned to form masks for use in etching underlying layers. EUV resists may be polymer-based chemically amplified resists (CARs) produced by liquid-based spin-on techniques. An alternative to CARs is directly photopatternable metal oxide-containing films, such as those available from Inpria, Corvallis, OR, and described, for example, in US Patent Publications US 2017/0102612, US 2016/021660 and 5 US 2016/0116839, incorporated by reference herein at least for their disclosure of photopatternable metal oxide-containing films. Such films may be produced by spin-on techniques or dry vapor-deposited. The metal oxide-containing film can be patterned directly (i.e., without the use of a separate photoresist) by EUV exposure in a vacuum ambient providing sub-10 30 nm patterning resolution, for example as described in US Patent 9,996,004, issued June 12, 2018 and titled EUV PHOTOPATTERNING OF VAPOR-DEPOSITED METAL OXIDE-CONTAINING HARDMASKS, and/or in International Patent Application No. PCT/US2019/31618, filed May 9, 2019, and titled METHODS FOR MAKING EUV PATTERNABLE HARD MASKS, the disclosures of which at least relating to the composition, 15 deposition, and patterning of directly photopatternable metal oxide films to form EUV resist masks is incorporated by reference herein. Generally, the patterning involves exposure of the EUV resist with EUV radiation to form a photo pattern in the resist, followed by development to remove a portion of the resist according to the photo pattern to form the mask.

[0030] It should also be understood that the while present disclosure relates to lithographic patterning techniques and materials exemplified by EUV lithography, it is also applicable to other 20 next generation lithographic techniques. In addition to EUV, which includes the standard 13.5 nm EUV wavelength currently in use and development, the radiation sources most relevant to such lithography are DUV (deep-UV), which generally refers to use of 248 nm or 193 nm excimer laser sources, X-ray, which formally includes EUV at the lower energy range of the X-ray range, as 25 well as e-beam, which can cover a wide energy range. The specific methods may depend on the particular materials and applications used in the semiconductor substrate and ultimate semiconducting device. Thus, the methods described in this application are merely exemplary of the methods and materials that may be used in present technology.

[0031] Directly photopatternable EUV resists may be composed of or contain metals and/or 30 metal oxides mixed within organic components. The metals/metal oxides are highly promising in that they can enhance the EUV photon adsorption and generate secondary electrons and/or show increased etch selectivity to an underlying film stack and device layers. To date, these resists have been developed using a wet (solvent) approach, which requires the wafer to move to the track,

where it is exposed to developing solvent, dried and baked. Wet development does not only limit productivity but can also lead to line collapse due to surface tension effects and/or delamination.

[0032] Dry development techniques have been proposed to overcome these issues by eliminating substrate delamination and interface failures. Dry development can improve performance at narrower linewidths (e.g., prevent line collapse due to surface tension and delamination seen in wet development) and potentially enhance throughput (e.g., by avoiding need for wet development tracks). Other advantages may include eliminating the use of organic solvent developers, reduced sensitivity to underlayer adhesion, and a lack of solubility-based limitations. Dry development can also provide more tunability and give further critical dimension (CD) control and scum removal.

[0033] Dry development has its own challenges, including etch selectivity between unexposed and EUV exposed resist material which can lead to a higher dose to size requirement for effective resist exposure when compared to wet development. Suboptimal selectivity can also cause PR corner rounding due to lower contrast at feature edges which may increase line CD variation in the following transfer etch step.

#### Dry Removal of Metal-Containing Resist

[0034] According to various aspects of the present disclosure, a photopatterned metal-containing photoresist is developed by exposure to vapors of organic acids or other vapor phase precursors. An EUV-sensitive metal or metal oxide-containing film, e.g., an organotin oxide, is disposed on a semiconductor substrate. The EUV-sensitive metal or metal oxide-containing film is patterned directly by EUV exposure in vacuum ambient. A pattern is then developed to form a resist mask using a development chemistry. In some implementations, the development chemistry is a dry development chemistry. In some implementations, the dry development chemistry includes an organic vapor such as trifluoroacetic acid. Such dry development techniques may be done while using either a gentle plasma (high pressure, low power) or non-plasma thermal process while flowing an organic vapor. Additionally or alternatively, the present disclosure provides for dry chamber clean of EUV resist material or metal-containing resist material from internal surfaces of a process chamber by exposure to organic acids or other vapor phase precursors. In some implementations, the organic vapor is trifluoroacetic acid. The dry clean may be a non-plasma thermal-based clean operation. The dry chamber clean may be performed in any process chamber used in deposition, bevel edge and/or backside clean, bake, development, or etch operation.

[0035] Various implementations of the present disclosure may include combining all dry operations by vapor deposition, EUV lithographic patterning, and dry development. Various other implementations include a combination of wet and dry processing operations, for example, spin-on EUV photoresists (wet process) may be combined with dry development or other wet or dry processes as described herein. Also described are various post-deposition (or post-application) processes such as bevel and backside cleaning, chamber cleaning, descum, smoothing, curing to modify and enhance film characteristics, and photoresist rework processing.

[0036] Figure 1 presents a flow diagram of an example method for depositing and developing a photoresist according to some implementations. The operations of a process 100 may be performed in different orders and/or with different, fewer, or additional operations. Aspects of the process 100 may be described with reference to Figures 2, 3A–3C, 4A–4B, 5, and 6A–6D. One or more operations of the process 100 may be performed using an apparatus described in any one of Figures 7–11B. In some implementations, the operations of the process 100 may be implemented, at least in part, according to software stored in one or more non-transitory computer readable media. In some implementations, dry chamber clean may be performed after deposition, backside and bevel edge clean, post application bake, post exposure bake, or dry development.

[0037] At block 102 of the process 100, a layer of photoresist is deposited. This may be either a dry deposition process such as a vapor deposition process or a wet process such as a spin-on deposition process.

[0038] The photoresist may be a metal-containing EUV resist. An EUV-sensitive metal or metal oxide-containing film may be deposited on a semiconductor substrate by any suitable technique, including wet (e.g., spin-on) or dry (e.g., CVD) deposition techniques. For example, described processes have been demonstrated for EUV photoresist compositions based on organotin oxides, being applicable to both commercially spin-coatable formulations (e.g., such as are available from Inpria Corp, Corvallis, OR) and formulations applied using dry vacuum deposition techniques, further described below.

[0039] Semiconductor substrates may include any material construct suitable for photolithographic processing, particularly for the production of integrated circuits and other semiconducting devices. In some implementations, semiconductor substrates are silicon wafers. Semiconductor substrates may be silicon wafers upon which features have been created ("underlying features"), having an irregular surface topography. As referred to herein, the "surface" is a surface onto which a film of the present disclosure is to be deposited or that is to be exposed to EUV during processing. Underlying features may include regions in which material

has been removed (e.g., by etching) or regions in which materials have been added (e.g., by deposition) during processing prior to conducting a method of this disclosure. Such prior processing may include methods of this disclosure or other processing methods in an iterative process by which two or more layers of features are formed on the substrate.

5 **[0040]** EUV-sensitive thin films may be deposited on the semiconductor substrate, such films being operable as resists for subsequent EUV lithography and processing. Such EUV-sensitive thin films comprise materials which, upon exposure to EUV, undergo changes, such as the loss of bulky pendant substituents bonded to metal atoms in low density M-OH rich materials, allowing their crosslinking to denser M-O-M bonded metal oxide materials. Through EUV patterning, areas  
10 of the film are created that have altered physical or chemical properties relative to unexposed areas. These properties may be exploited in subsequent processing, such as to dissolve either unexposed or exposed areas, or to selectively deposit materials on either the exposed or unexposed areas. In some implementations, the unexposed film has a more hydrophobic surface than the exposed film under the conditions at which such subsequent processing is performed. For example, the removal  
15 of material may be performed by leveraging differences in chemical composition, density and cross-linking of the film. Removal may be by wet processing or dry processing, as further described below.

**[0041]** The thin films are, in various implementations, organometallic materials, for example organotin materials comprising tin oxide, or other metal oxide materials/moieties. The  
20 organometallic compounds may be made in a vapor phase reaction of an organometallic precursor with a counter reactant. In various implementations, the organometallic compounds are formed through mixing specific combinations of organometallic precursors having bulky alkyl groups or fluoroalkyl groups with counter-reactants and polymerizing the mixture in the vapor phase to produce a low-density, EUV-sensitive material that deposits onto the semiconductor substrate.

25 **[0042]** In various implementations, organometallic precursors comprise at least one alkyl group on each metal atom that can survive the vapor-phase reaction, while other ligands or ions coordinated to the metal atom can be replaced by the counter-reactants. Organometallic precursors include those of the formula:



30 (Formula 1)

**[0043]** wherein: M is an element with a high patterning radiation-absorption cross-section; R is alkyl, such as  $C_nH_{2n+1}$ , preferably wherein  $n = 1-6$ ; L is a ligand, ion or other moiety which is

reactive with the counter-reactant;  $a \geq 1$ ;  $b \geq 1$ ; and  $c \geq 1$ . In various implementations, M has an atomic absorption cross section equal to or greater than  $1 \times 10^7 \text{ cm}^2/\text{mol}$ . M may be, for example, selected from the group consisting of tin, hafnium, tellurium, bismuth, indium, antimony, iodine, germanium, and combinations thereof. In some implementations, M is tin. R may be fluorinated, e.g., having the formula  $\text{C}_n\text{F}_x\text{H}_{(2n+1)}$ . In various implementations, R has at least one beta-hydrogen or beta-fluorine. For example, R may be selected from the group consisting of methyl, ethyl, i-propyl, n-propyl, t-butyl, i-butyl, n-butyl, sec-butyl, n-pentyl, i-pentyl, t-pentyl, sec-pentyl, and mixtures thereof. L may be any moiety readily displaced by a counter-reactant to generate an M-OH moiety, such as a moiety selected from the group consisting of amines (such as dialkylamino, monoalkylamino), alkoxy, carboxylates, halogens, and mixtures thereof.

**[0044]** Organometallic precursors may be any of a wide variety of candidate metal-organic precursors. For example, where M is tin, such precursors include t-butyl tris(dimethylamino) tin, i-butyl tris(dimethylamino) tin, n-butyl tris(dimethylamino) tin, sec-butyl tris(dimethylamino) tin, i-propyl(tris)dimethylamino tin, n-propyl tris(dimethylamino) tin, ethyl tris(dimethylamino) tin and analogous alkyl(tris)(t-butoxy) tin compounds such as t-butyl tris(t-butoxy) tin. In some implementations, the organometallic precursors are partially fluorinated.

**[0045]** Counter-reactants have the ability to replace the reactive moieties, ligands or ions (e.g., L in Formula 1, above) so as to link at least two metal atoms via chemical bonding. Counter-reactants can include water, peroxides (e.g., hydrogen peroxide), di- or polyhydroxy alcohols, fluorinated di- or polyhydroxy alcohols, fluorinated glycols, and other sources of hydroxyl moieties. In various implementations, a counter-reactant reacts with the organometallic precursor by forming oxygen bridges between neighboring metal atoms. Other potential counter-reactants include hydrogen sulfide and hydrogen disulfide, which can crosslink metal atoms via sulfur bridges.

**[0046]** The thin films may include optional materials in addition to an organometallic precursor and counter-reactants to modify the chemical or physical properties of the film, such as to modify the sensitivity of the film to EUV or enhancing etch resistance. Such optional materials may be introduced, such as by doping during vapor phase formation prior to deposition on the semiconductor substrate, after deposition of the thin film, or both. In some implementations, a gentle remote  $\text{H}_2$  plasma may be introduced so as to replace some Sn-L bonds with Sn-H, which can increase reactivity of the resist under EUV.

**[0047]** In various implementations, the EUV-patternable films are made and deposited on the semiconductor substrate using vapor deposition equipment and processes among those known

in the art. In such processes, the polymerized organometallic material is formed in vapor phase or *in situ* on the surface of the semiconductor substrate. Suitable processes include, for example, chemical vapor deposition (CVD), atomic layer deposition (ALD), and ALD with a CVD component, such as a discontinuous, ALD-like process in which metal precursors and counter-  
5 reactants are separated in either time or space.

**[0048]** In general, methods comprise mixing a vapor stream of an organometallic precursor with a vapor stream of a counter-reactant so as to form a polymerized organometallic material, and depositing the organometallic material onto the surface of the semiconductor substrate. In some implementations, more than one organometallic precursor is included in the vapor stream. In some  
10 implementations, more than one counter-reactant is included in the vapor stream. As will be understood by one of ordinary skill in the art, the mixing and depositing aspects of the process may be concurrent, in a substantially continuous process.

**[0049]** In an example continuous CVD process, two or more gas streams, in separate inlet paths, of organometallic precursor and source of counter-reactant are introduced to the deposition  
15 chamber of a CVD apparatus, where they mix and react in the gas phase, to form agglomerated polymeric materials (e.g., via metal-oxygen-metal bond formation). The streams may be introduced, for example, using separate injection inlets or a dual-plenum showerhead. The apparatus is configured so that the streams of organometallic precursor and counter-reactant are mixed in the chamber, allowing the organometallic precursor and counter-reactant to react to form  
20 a polymerized organometallic material. Without limiting the mechanism, function, or utility of present technology, it is believed that the product from such vapor-phase reaction becomes heavier in molecular weight as metal atoms are crosslinked by counter-reactants, and is then condensed or otherwise deposited onto the semiconductor substrate. In various implementations, the steric hindrance of the bulky alkyl groups prevents the formation of densely packed network and  
25 produces smooth, amorphous, low-density films.

**[0050]** The CVD process is generally conducted at reduced pressures, such as from 10 milli Torr to 10 Torr. In some implementations, the process is conducted at from 0.5 to 2 Torr. In some implementations, the temperature of the semiconductor substrate is at or below the temperature of the reactant streams. For example, the substrate temperature may be from 0°C to 250°C, or from  
30 ambient temperature (e.g., 23°C) to 150°C. In various processes, deposition of the polymerized organometallic material on the substrate occurs at rates inversely proportional to surface temperature.

[0051] In some implementations, the EUV-patternable films are made and deposited on the semiconductor substrate using wet deposition equipment and processes among those known in the art. For example, the organometallic material is formed by spin-coating on the surface of the semiconductor substrate.

5 [0052] The thickness of the EUV-patternable film formed on the surface of the semiconductor substrate may vary according to the surface characteristics, materials used, and processing conditions. In various implementations, the film thickness may range from 0.5 nm to 100 nm, and may be a sufficient thickness to absorb most of the EUV light under the conditions of EUV  
10 patterning. The EUV-patternable film may be able to accommodate absorption equal to or greater than 30%, thereby having significantly fewer EUV photons available towards the bottom of the EUV-patternable film. Higher EUV absorption leads to more cross-linking and densification near the top of an EUV-exposed film compared to the bottom of the EUV-exposed film. Though insufficient cross-linking may cause the resist to be more prone to liftoff or collapse in wet development, such as risk is not as present in dry development. An all-dry lithography approach  
15 may facilitate more efficient utilization of EUV photons by more opaque resist films. Though efficient utilization of EUV photons may occur with EUV-patternable films having higher overall absorption, it will be understood that in some instances, the EUV-patternable film may be less than about 30%. For comparison, the maximum overall absorption of most other resist films is less than 30% (e.g., 10% or less, or 5% or less) so that the resist material at the bottom of the resist  
20 film is sufficiently exposed. In some implementations, the film thickness is from 10 nm to 40 nm or from 10 nm to 20 nm. Without limiting the mechanism, function, or utility of the present disclosure, the processes of the present disclosure have few restrictions on the surface adhesion properties of the substrate, and therefore can be applied to a wide variety of substrates. Moreover, as discussed above, the deposited films may closely conform to surface features, providing  
25 advantages in forming masks over substrates, such as substrates having underlying features, without "filling in" or otherwise planarizing such features.

[0053] In addition to depositing a metal-containing EUV resist thin film on a semiconductor substrate at block 102 of the process 100, some metal-containing EUV resist material may form as a residue on internal surfaces of the process chamber. The internal surfaces may include  
30 chamber walls, floors, and ceilings of the process chamber. Other internal surfaces may include a showerhead, nozzles, and substrate support surfaces. The metal-containing EUV resist material may form as a result of dry deposition processes, such as CVD or ALD processes. A thickness of the residue of the metal-containing EUV resist material may increase over time as a result of additional processing (e.g., deposition) operations being performed in the process chamber. The

residue is prone to flake off, shed particles, or peel from the internal surfaces of the process chamber to cause contamination in downstream processes.

**[0054]** At block 150 of the process 100, a dry chamber clean is performed after deposition of the metal-containing EUV resist thin film at block 102 of the process 100. This allows for deposition and dry cleaning to be performed in the same process chamber. However, it will be understood that the dry chamber clean may be performed in a different process chamber than the deposition operation in some implementations. In fact, the dry chamber clean may be performed subsequent to a bevel edge and/or backside clean, bake, development, or etch operation, since residue may also form inside chambers where any of these operations are performed, which may or may not be the same as the deposition chamber.

**[0055]** The dry-deposited EUV resist materials being removed are generally composed of Sn, O, and C, but the same clean approaches can be extended to films of other metal oxide resists and materials. In addition, this approach can be used for film strip and photoresist rework.

**[0056]** At block 104, an optional cleaning process is performed to clean a backside and/or bevel edge of the semiconductor substrate. The backside and/or bevel edge clean may non-selectively etch EUV resist film to equally remove film with various levels of oxidation or crosslinking on the substrate backside and bevel edge. During application of the EUV-patternable film, either by wet deposition processing or dry deposition processing, there may be some unintended deposition of resist material on the substrate bevel edge and/or backside. The unintended deposition may lead to undesirable particles later moving to a top surface of the semiconductor substrate and becoming particle defects. Moreover, this bevel edge and backside deposition can cause downstream processing problems, including contamination of the patterning (scanner) and development tools. Conventionally, removal of this bevel edge and backside deposition is done by wet cleaning techniques. For spin-coated photoresist material, this process is called edge bead removal (EBR) and is performed by directing a stream of solvent from above and below the bevel edge while the substrate is spinning. The same process can be applied to soluble organotin oxide-based resists deposited by vapor deposition techniques.

**[0057]** The substrate bevel edge and/or backside clean may also be a dry clean process. In some implementations, the dry clean process involves a vapor and/or plasma having one or more of the following gases: HBr, HCl, BCl<sub>3</sub>, SOCl<sub>2</sub>, Cl<sub>2</sub>, BBr<sub>3</sub>, H<sub>2</sub>, O<sub>2</sub>, PCl<sub>3</sub>, CH<sub>4</sub>, methanol, ammonia, formic acid, NF<sub>3</sub>, HF. In some implementations, the dry clean process may use the same chemistries as a dry development process described herein. For example, the bevel edge and/or backside clean may use an organic acid such as trifluoroacetic acid or other organic vapor. For the bevel edge

and/or backside clean process, the vapor and/or the plasma has to be limited to a specific region of the substrate to ensure that only the backside and the bevel are removed, without any film degradation on a frontside of the substrate.

5 [0058] Process conditions may be optimized for bevel edge and/or backside clean. In some implementations, higher temperature, higher pressure, and/or higher reactant flow may lead to increased etch rate. Suitable process conditions for a dry bevel edge and backside clean may be: reactant flow of 100–10000 sccm (e.g., 500 sccm HCl, HBr, HI, or H<sub>2</sub> and Cl<sub>2</sub> or Br<sub>2</sub>, BCl<sub>3</sub> or H<sub>2</sub>, or other halogen-containing compound), temperature of 20 to 140°C (e.g., 80°C), pressure of 20–1000 mTorr (e.g., 100 mTorr) or pressure of 50–765 Torr (e.g., 760 Torr), plasma power of 0 to 10 500 W at high frequency (e.g., 13.56 MHz), and for a time of about 10 to 20 seconds, dependent on the photoresist film and composition and properties. Bevel and/or backside clean may be accomplished using a Coronus® tool available from Lam Research Corporation, Fremont, CA, though a wider range of process conditions may be used according to the capabilities of the processing reactor.

15 [0059] Bevel edge and/or backside clean may alternatively be extended to a full photoresist removal or photoresist “rework” in which an applied EUV photoresist is removed and the semiconductor substrate prepared for photoresist reapplication, such as when the original photoresist is damaged or otherwise defective. Photoresist rework should be accomplished without damaging the underlying semiconductor substrate, so an oxygen-based etch should be 20 avoided. Instead, organic vapor chemistries or variants of halogen-containing chemistries as described herein may be used. It will be understood that the photoresist rework operation may be applied at any stage during the process 100. Thus, the photoresist rework operation may be applied after deposition, after bevel edge and/or backside clean, after PAB treatment, after EUV exposure, after PEB treatment, after development, or after hard bake. In some implementations, the 25 photoresist rework may be performed for non-selective removal of exposed and unexposed regions of the photoresist but selective to an underlayer.

[0060] In some implementations, the photoresist rework process involves a vapor and/or plasma having one or more of the following gases: HBr, HCl, HI, BCl<sub>3</sub>, Cl<sub>2</sub>, BBr<sub>3</sub>, H<sub>2</sub>, PCl<sub>3</sub>, CH<sub>4</sub>, methanol, ammonia, formic acid, NF<sub>3</sub>, HF. In some implementations, the photoresist rework may 30 use the same chemistries as a dry development process described herein. For example, the photoresist rework may use an organic acid such as trifluoroacetic acid or other organic vapor.

[0061] Process conditions may be optimized for the photoresist rework. In some implementations, higher temperature, higher pressure, and/or higher reactant flow may lead to

increased etch rate. Suitable process conditions for a photoresist rework may be: reactant flow of 100–500 sccm (e.g., 500 sccm HCl, HBr, HI, BCl<sub>3</sub> or H<sub>2</sub> and Cl<sub>2</sub> or Br<sub>2</sub>), temperature of 20 to 140°C (e.g., 80°C), pressure of 20–1000 mTorr (e.g., 300 mTorr) or pressure of 50–765 Torr (e.g., 760 Torr), plasma power of 0 to 800 W (e.g., 500 W) at high frequency (e.g., 13.56 MHz), wafer bias of 0 to 200 V<sub>b</sub> (a higher bias may be used with harder underlying substrate materials) and for a time of about 20 seconds to 3 minutes, sufficient to completely remove the EUV photoresist, dependent on the photoresist film and composition and properties. It should be understood that while these conditions are suitable for some processing reactors, e.g., a Kiyoo etch tool available from Lam Research Corporation, Fremont, CA, a wider range of process conditions may be used according to the capabilities of the processing reactor.

**[0062]** At block 150 of the process 100, a dry chamber clean operation may be performed after a bevel edge and/or backside clean at block 104 of the process 100. This allows for bevel edge and/or backside clean and dry chamber clean to be performed in the same process chamber. However, it will be understood that the dry chamber clean may be performed in a different process chamber than the bevel edge and/or backside clean in some implementations.

**[0063]** At block 106 of the process 100, an optional post-application bake (PAB) is performed after deposition of the metal-containing EUV resist film and prior to EUV exposure. The PAB treatment may involve a combination of thermal treatment, chemical exposure, and moisture to increase the EUV sensitivity of the metal-containing EUV resist film, reducing the EUV dose to develop a pattern in the metal-containing EUV resist film. The PAB treatment temperature may be tuned and optimized for increasing the sensitivity of the metal-containing EUV resist film. For example, the treatment temperature may be between about 90°C and about 200°C or between about 150°C and about 190°C. In some implementations, the PAB treatment may be conducted with a pressure between atmospheric and vacuum, and a treatment duration of about 1 to 15 minutes, for example about 2 minutes. In some implementations, the PAB treatment is conducted at a temperature between about 100°C to 230°C for about 1 minute to 2 minutes.

**[0064]** At block 150 of the process 100, a dry chamber clean operation may be performed after the PAB treatment at block 106 of the process 100. This allows for bake and dry chamber clean to be performed in the same process chamber. However, it will be understood that the dry chamber clean may be performed in a different process chamber than the PAB treatment in some implementations.

**[0065]** At block 108 of the process 100, the metal-containing EUV resist film is exposed to EUV radiation to develop a pattern. Generally speaking, the EUV exposure causes a change in the

chemical composition and cross-linking in the metal-containing EUV resist film, creating a contrast in etch selectivity that can be exploited for subsequent development.

**[0066]** The metal-containing EUV resist film may then be patterned by exposing a region of the film to EUV light, typically under relatively high vacuum. EUV devices and imaging methods among those useful herein include methods known in the art. In particular, as discussed above, 5 exposed areas of the film are created through EUV patterning that have altered physical or chemical properties relative to unexposed areas. For example, in exposed areas, metal-carbon bond cleavage may occur, as through a beta-hydride elimination, leaving behind reactive and accessible metal hydride functionality that can be converted to hydroxide and cross-linked metal 10 oxide moieties via metal-oxygen bridges during a subsequent post-exposure bake (PEB) step. This process can be used to create chemical contrast for development as a negative tone resist. In general, a greater number of beta-H in the alkyl group results in a more sensitive film. This can also be explained as weaker Sn-C bonding with more branching. Following exposure, the metal-containing EUV resist film may be baked, so as to cause additional cross-linking of the metal oxide 15 film. The difference in properties between exposed and unexposed areas may be exploited in subsequent processing, such as to dissolve unexposed areas or to deposit materials on the exposed areas. For example the pattern can be developed using a dry method to form a metal oxide-containing mask.

**[0067]** In particular, in various implementations, the hydrocarbyl-terminated tin oxide present 20 on the surface is converted to hydrogen-terminated tin oxide in the exposed region(s) of an imaging layer, particularly when the exposure is performed in a vacuum using EUV. However, removing exposed imaging layers from vacuum into air, or the controlled introduction of oxygen, ozone, H<sub>2</sub>O<sub>2</sub>, or water, can result in the oxidation of surface Sn-H into Sn-OH. The difference in properties between exposed and unexposed regions may be exploited in subsequent processing, 25 such as by reacting the irradiated region, the unirradiated region, or both, with one or more reagents to selectively add material to or remove material from the imaging layer.

**[0068]** Without limiting the mechanism, function or utility of present technology, EUV exposure, for example, at doses of from 10 mJ/cm<sup>2</sup> to 100 mJ/cm<sup>2</sup> results in the cleavage of Sn-C bonds resulting in loss of the alkyl substituent, alleviating steric hindrance and allowing the low- 30 density film to collapse. In addition, reactive metal-H bond generated in the beta-hydride elimination reactions can react with neighboring active groups such as hydroxyls in the film, leading to further cross-linking and densification, and creating chemical contrast between exposed and unexposed region(s).

[0069] Following exposure of the metal-containing EUV resist film to EUV light, a photopatterned metal-containing EUV resist is provided. The photopatterned metal-containing EUV resist includes EUV-exposed and unexposed regions.

[0070] At block 110 of the process 100, an optional post-exposure bake (PEB) is performed to further increase contrast in etch selectivity of the photopatterned metal-containing EUV resist. The photopatterned metal-containing EUV resist can be thermally treated in the presence of various chemical species to facilitate cross-linking of the EUV-exposed regions or simply baked on a hot plate in ambient air, for example between 100°C and 250°C for between one and five minutes (e.g., 190°C for two minutes).

[0071] In various implementations, a bake strategy involves careful control of the bake ambient, introduction of reactive gases, and/or careful control of the ramping rate of the bake temperature. Examples of useful reactive gases include e.g., air, H<sub>2</sub>O, H<sub>2</sub>O<sub>2</sub> vapor, CO<sub>2</sub>, CO, O<sub>2</sub>, O<sub>3</sub>, CH<sub>4</sub>, CH<sub>3</sub>OH, N<sub>2</sub>, H<sub>2</sub>, NH<sub>3</sub>, N<sub>2</sub>O, NO, alcohol, acetyl acetone, formic acid, Ar, He, or their mixtures. The PEB treatment is designed to (1) drive complete evaporation of organic fragments that are generated during EUV exposure and (2) oxidize any Sn-H, Sn-Sn, or Sn radical species generated by EUV exposure into metal hydroxide, and (3) facilitate cross-linking between neighboring Sn-OH groups to form a more densely crosslinked SnO<sub>2</sub>-like network. The bake temperature is carefully selected to achieve optimal EUV lithographic performance. Too low a PEB temperature would lead to insufficient cross-linking, and consequently less chemical contrast for development at a given dose. Too high a PEB temperature would also have detrimental impacts, including severe oxidation and film shrinkage in the unexposed region (the region that is removed by development of the patterned film to form the mask in this example), as well as, undesired interdiffusion at the interface between the photopatterned metal-containing EUV resist and an underlayer, both of which can contribute to loss of chemical contrast and an increase in defect density due to insoluble scum. The PEB treatment temperature may be between about 100°C and about 300°C, between about 170°C and about 290°C, or between about 200°C and about 240°C. In some implementations, the PEB treatment may be conducted with a pressure between atmospheric and vacuum, and a treatment duration of about 1 to 15 minutes, for example about 2 minutes. In some implementations, PEB thermal treatment may be repeated to further increase etch selectivity.

[0072] At block 150 of the process 100, a dry chamber clean operation may be performed after the PEB treatment at block 110 of the process 100. This allows for bake and dry chamber clean to be performed in the same process chamber. However, it will be understood that the dry chamber

clean may be performed in a different process chamber than the PEB treatment in some implementations.

**[0073]** At block 112 of the process 100, the photopatterned metal-containing EUV resist is developed to form a resist mask. In various implementations, the exposed regions are removed (positive tone) or the unexposed regions are removed (negative tone). In some implementations, development may include selective deposition on either the exposed or unexposed regions of the photopatterned metal-containing EUV resist, followed by an etching operation. In some implementations, development may be done with exposure to one or more organic vapors (e.g., trifluoroacetic acid). The development may be done without striking a plasma in some implementations. Or, development may be done with flows of one or more organic vapors (e.g., trifluoroacetic acid) activated in a remote plasma source or activated by exposure to remote UV radiation. The photoresist for development may include an element selected from the group consisting of: tin, hafnium, tellurium, bismuth, indium, antimony, iodine, and germanium. The element may have a high patterning radiation-absorption cross-section. In some implementations, the element may have a high EUV-absorption cross-section. In some implementations, the metal-containing EUV resist may have an overall absorption greater than 30%. In an all-dry lithography process, this provides more efficient utilization of EUV photons, enabling development of thicker and more EUV-opaque resists.

**[0074]** Examples of processes for development involve an organotin oxide-containing EUV-sensitive photoresist thin film (e.g., 10–30 nm thick, such as 20 nm), subjected to a EUV exposure dose and post-exposure bake, and then developed. The photoresist film may be, for example, deposited based on a gas phase reaction of an organotin precursor such as isopropyl(tris)(dimethylamino)tin and water vapor, or may be a spin-on film comprising tin clusters in an organic matrix.

**[0075]** At block 150 of the process 100, a dry chamber clean may be performed after dry development at block 112 of the process 100. This allows for dry development and dry chamber clean to be performed in the same process chamber. However, it will be understood that the dry chamber clean may be performed in a different process chamber than the dry development in some implementations. Moreover, it will be understood that the dry chamber clean may be performed in the same or different process chamber than an etch operation. The etch operation may be applied to etch a substrate underlayer of the semiconductor substrate.

**[0076]** At block 114 of the process 100, the semiconductor substrate optionally undergoes a hard bake. During the hard bake, the semiconductor substrate is subjected to an elevated temperature.

For example, the semiconductor substrate may be subjected to an elevated temperature equal to or greater than about 50°C, between about 100°C and about 300°C, or between about 170°C and about 290°C. The hard bake may drive out remaining solvents or etch gas from development.

[0077] Figure 2 presents a flow diagram of an example method of dry developing a metal-containing resist according to some implementations. The operations of a process 200 may be performed in different orders and/or with different, fewer, or additional operations. Aspects of the process 200 may be described with reference to Figures 3A–3C and Figures 4A–4B. One or more operations of the process 200 may be performed using an apparatus described in any one of Figures 7–11B. In some implementations, the operations of the process 200 may be implemented, at least in part, according to software stored in one or more non-transitory computer readable media.

[0078] At block 202 of the process 200, a photopatterned metal-containing resist is provided on a surface of a semiconductor substrate in a process chamber. A metal-containing resist may be deposited on the surface of the semiconductor substrate. The metal-containing resist may be exposed to UV radiation (e.g., EUV radiation) by a scanner or EUV lithography tool to form the photopatterned metal-containing resist. In some implementations, the photopatterned metal-containing resist is a photopatterned metal-containing EUV resist. For example, the photopatterned metal-containing EUV resist is an organo-metal oxide or organo-metal-containing film. The semiconductor substrate may be provided in the process chamber after processing in the scanner and/or PEB treatment chamber.

[0079] At block 204 of the process 200, the photopatterned metal-containing resist is dry developed to selectively remove a portion of the resist by exposure to a development chemistry comprising an organic vapor to form a resist mask. Dry developing the photopatterned metal-containing resist includes selectively removing an EUV-unexposed portion of the resist relative to an EUV-exposed portion with the development chemistry to form the resist mask. Typically, development occurs using a wet development chemistry. Wet development using a solvent produces an undesirable waste stream. Wet development generally involves moisture and/or oxygen, which more easily leads to scum formation. Wet development is limited by solubility and cluster size, whereas dry development is not limited by solubility and cluster size. Wet development is more prone to pattern collapse and delamination issues that dry development avoids. Development in the present disclosure occurs in the vapor phase using a dry development chemistry instead of wet development chemistry.

[0080] Development using dry development chemistry ordinarily involves vapors of halogens such as a vapor of boron trichloride (BCl<sub>3</sub>), hydrogen gas (H<sub>2</sub>) mixed with chlorine gas (Cl<sub>2</sub>) or

bromine gas ( $\text{Br}_2$ ), or a vapor of a hydrogen halide such as hydrogen bromide ( $\text{HBr}$ ), hydrogen chloride ( $\text{HCl}$ ), or hydrogen fluoride ( $\text{HF}$ ). However, such vapors may leave a residue or scum after development. The residue may include residual etch byproduct adsorbed onto the surface of the semiconductor substrate or even onto chamber walls. For example, the vapors of halogens  
5 may react with moisture or oxygen to forming residual etch byproducts that are difficult to remove. In some instances, the residual etch byproduct includes bromides that are sticky and resistant to removal. Buildup of residual etch byproducts can lead to process drift, resulting in hazard precautions in the process chamber. Moreover, residue adsorbed on the semiconductor substrate has the potential to desorb off the semiconductor substrate and contaminate downstream  
10 processing tools. In some cases, the residue may include high metal concentrations or clusters of metal oxide that can contaminate downstream processing tools. And because the residual etch byproduct is difficult to remove and not readily volatile, a separate plasma step or separate chamber with plasma capability may be necessary. Otherwise, high temperature swings are performed to cause the residue to volatilize, which is often undesirable for the semiconductor  
15 substrate and process chamber.

**[0081]** The development chemistry of the present disclosure is an organic vapor. The organic vapor may be an organic acid. In some implementations, the organic acid includes a carboxylic acid. In some implementations, the organic acid includes trifluoroacetic acid ( $\text{CF}_3\text{COOH}$ ). The organic vapor may be halogenated or at least fluorinated. In some implementations, the organic  
20 vapor includes hexafluoro-acetylacetone ( $\text{CF}_3\text{CCH}_2\text{CCF}_3$ ). In some implementations, the organic vapor includes trifluoroacetic acid anhydride ( $(\text{CF}_3\text{CO})_2\text{O}$ ), acetic acid anhydride ( $(\text{CH}_3\text{CO})_2\text{O}$ ), trichloroacetic acid ( $\text{CCl}_3\text{COOH}$ ), mono-fluoroacetic acid ( $\text{CFH}_2\text{COOH}$ ), di-fluoroacetic acid ( $\text{CF}_2\text{HCOOH}$ ), a mixed halide acetic acid such as chloro-difluoro-acetic acid, a sulfur-containing analogue of acetic acid, thioacetic acid ( $\text{CH}_3\text{COSH}$ ), or thioglycolic acid ( $\text{HSCH}_2\text{CO}_2\text{H}$ ). In some  
25 implementations, the development chemistry includes a mixture of a carboxylic acid and a hydrogen halide in a vapor phase. For example, the development chemistry includes a mixture of acetic acid or formic acid with hydrogen chloride or hydrogen bromide. In some implementations, the organic vapor may be flowed with or without inert/carrier gas such as helium ( $\text{He}$ ), neon ( $\text{Ne}$ ), argon ( $\text{Ar}$ ), xenon ( $\text{Xe}$ ), and nitrogen ( $\text{N}_2$ ).

30 **[0082]** The organic vapor may react with the metal-containing resist to form byproducts that are more volatile than the etch byproducts formed from vapors of halogens. By way of an example, it is possible that etch byproducts of tin bromides may have a boiling point equal to or greater than about  $200^\circ\text{C}$ . However, etch byproducts of tin fluoroacetates may be less than about  $200^\circ\text{C}$ . For example, hexatin(II)-di- $\mu$ -oxy-octakis- $\mu$ -trifluoroacetate (1F) is volatile at  $191^\circ\text{C}$  at 1 Torr and

tin(IV) tetrakis(trifluoroacetate) (2F) is volatile at 84°C at 1 Torr. Both 1F and 2F provide high thermal stability and volatility. Etch byproducts formed from organic vapors reacting with metal-containing resist may have excellent volatility. In particular, etch byproducts formed from trifluoroacetic acid reacting with EUV-unexposed organometallic resist may have excellent  
5 volatility. Without being limited by any theory, trifluoroacetic acid or other fluorinated derivatives of organic acids may increase the volatility of etch byproducts with their electron-drawing effect. Trifluoroacetic acids or other fluorinated derivatives of organic acids may be strong organic acids.

**[0083]** The organic vapor of the present disclosure may be a strong organic acid. As used herein, a strong organic acid may have a pK<sub>a</sub> value that is equal to or less than about 3.8. The strength of  
10 the organic acid may be increased by halogenation. In some implementations, the strength of the organic acid may be significantly increased by fluorination. For example, though formic acid or acetic acid may etch metal-containing resist materials such as organometallic resist materials, trifluoroacetic acid can more effectively etch such metal-containing resist materials. Whereas less  
15 strong organic acids (e.g., acetic acid) may be assisted by plasma for selective removal of metal-containing resist materials, stronger organic acids may selectively remove the metal-containing resist materials without the assistance of plasma. Accordingly, dry development of the metal-containing resist may be performed without the assistance of plasma in the present disclosure. However, as described below, plasma may optionally be employed in a desorption, descumming,  
20 or smoothing operation after dry development. This plasma-based desorption, descumming, or smoothing operation may be unnecessary where the etch byproducts of the organic vapors are volatilized.

**[0084]** Organic vapors of the present disclosure may perform dry development in a plasma-free thermal process. This means that dry development may be performed in a process chamber without plasma capability. In some implementations, dry development may be performed without  
25 a subsequent plasma-based descumming or smoothing operation. By eliminating plasma exposure, this avoids plasma damage to the semiconductor substrate and can significantly reduce cost and increase throughput. Furthermore, internal surfaces of the process chamber may be made of a material that does not have to be resistant to plasma as well as resistant to vapors of halogens such as hydrogen halides. Chamber walls, ceilings, and surfaces of chamber components such as  
30 showerheads may be vulnerable to corrosion in the presence of moisture and vapors of halogens. As a result, the internal surfaces of the process chamber are typically composed of materials that are stable in plasma, vapors of halogens, and water vapor. However, for dry development chemistries of the present disclosure such as trifluoroacetic acid, internal surfaces of the process chamber in the present disclosure may be composed of materials that do not necessarily meet the

aforementioned requirements. In some implementations, chamber walls of the process chamber may include aluminum oxide, anodized aluminum, or plastic.

**[0085]** By applying a plasma-free thermal approach, productivity can be significantly improved as multiple wafers can be batch developed, at the same time in a low-cost thermal vacuum chamber/oven. However, in some implementations, the thermal dry development process may be followed by exposure to plasma. Subsequent exposure to plasma may occur for desorption, descumming, smoothing, or other processing operations.

**[0086]** Dry development of the photopatterned metal-containing resist may be combined with other dry processing operations such as dry deposition (e.g., CVD) of the metal-containing resist.

In some implementations, processing of the semiconductor substrate may combine all dry steps including film formation by vapor deposition, EUV lithographic patterning, and dry development. Bake operations, bevel edge and/or backside clean operations, and chamber clean operations may also be dry operations. Such processing operations may avoid material and productivity costs associated with wet processing operations such as wet development. Furthermore, dry processing can provide more tunability and add further critical dimension (CD) control and possible scum removal. In general, wet processing involves moisture and/or oxygen, which more easily leads to scum formation. Wet development is limited by solubility and cluster size, whereas dry development is not limited by solubility and cluster size. Wet development is more prone to pattern collapse and delamination issues that dry development avoids. In addition, employing all-dry processing operations may facilitate integration within an interconnected vacuum processing chamber without exposure to and contamination by ambient air or trace contaminants contained therein. For example, the PEB thermal treatment during which exposed regions undergo further crosslinking may be conducted in the same chamber as development, though it will be understood that the PEB thermal treatment may be performed in another chamber.

**[0087]** In some implementations, dry development can be done by using a thermal process while flowing the organic vapor such as trifluoroacetic acid. For example, dry development can be carried out in a thermal processing chamber. In some implementations, the organic vapor such as trifluoroacetic acid is able to quickly remove the unexposed portions of the photopatterned metal-containing resist relative to the exposed portions of the photopatterned metal-containing resist, leaving behind a pattern of exposed film that can be transferred to underlying layers of the semiconductor substrate by an etch process.

**[0088]** In some implementations, the semiconductor substrate may be exposed to dry development chemistry such as a strong organic acid in a thermal processing chamber such as an

oven. The thermal processing chamber may include a development chemistry line for delivery of the organic vapor into the thermal processing chamber. In some implementations, the thermal processing chamber may include one or more heating elements for temperature control, such as heating elements coupled to a heating assembly facing the semiconductor substrate in the process chamber for substrate temperature control. In some implementations, the one or more heating elements may be one or more LEDs. The one or more heaters may heat the semiconductor substrate to an elevated temperature during dry development to promote volatilization of etch byproducts.

**[0089]** In thermal dry development processes, the photopatterned metal-containing resist is exposed to development chemistry that is optimized for etch selectivity between exposed and unexposed regions. Generally, lower temperatures may increase contrast in etch selectivity while higher temperatures may decrease contrast in etch selectivity. Higher temperatures may increase volatilization of etch byproducts to limit residue formation on the semiconductor substrate. In some implementations, a temperature may be less than about 200°C, between about 20°C and about 190°C, between about 40°C and about 120°C, or between about 50°C and about 100°C. Reacting the photopatterned metal-containing resist with the organic vapor forms a volatile compound at a temperature less than about 200°C.

**[0090]** Chamber pressure may be tuned, where chamber pressure may influence etch selectivity between exposed and unexposed regions during thermal dry development. In some implementations, chamber pressure may be relatively low and accompanied without dilution, where the chamber pressure may be between about 0.1 mTorr and about 1000 mTorr, between about 0.2 mTorr and about 300 mTorr, or between about 0.5 mTorr and about 100 mTorr. In some implementations, the chamber pressure may be between about 20 mTorr and about 2000 mTorr, or between about 20 mTorr and about 1000 mTorr, such as about 300 mTorr. In some implementations, the chamber pressure may be relatively high with high flow and accompanied by dilution, where the chamber pressure may be between about 100 Torr and about 765 Torr or between about 200 Torr and about 760 Torr.

**[0091]** Gas flow rate of the dry development chemistry may be tuned, where gas flow may influence etch selectivity between exposed and unexposed regions during thermal dry development. In some implementations, gas flow may be between about 0.5 SLM and about 30 SLM, between about 1 SLM and about 20 SLM, or between about 2 SLM and about 15 SLM. The gas flow rate may include a total flow rate of gases flowed, including the organic vapor and carrier gas such as nitrogen, argon, etc. The organic vapor flow rate may only be a fraction of the total

flow rate, where the organic vapor flow rate may be between about 0.01 SLM and about 1 SLM. In instances with high flow, organic vapor flow may be between about 1 SLM and about 10 SLM.

[0092] Duration of exposure may be tuned in the thermal dry development process. The duration of exposure may depend on how much resist is desired to be removed, development chemistry, amount of crosslinking in the resist, and composition and properties of the resist, among other factors. In some implementations, duration of exposure may be between about 5 seconds and about 5 minutes, between about 10 seconds and about 3 minutes, or between about 10 seconds and about 1 minute.

[0093] In some implementations, the photopatterned metal-containing resist is developed in a plasma-free thermal approach. In alternative implementations, the photopatterned metal-containing resist is developed in a plasma development process. The photopatterned metal-containing resist is exposed to development chemistry including radicals/ions of one or more gases. The one or more gases may include an organic vapor such as trifluoroacetic acid. A process chamber for processing the semiconductor substrate for dry development may be a plasma-generating chamber or coupled to a plasma-generating chamber remote from the process chamber. The plasma-generating chamber may be an inductively-coupled plasma (ICP) reactor, transformer-coupled plasma (TCP) reactor, or capacitively-coupled plasma (CCP) reactor, employing equipment and techniques among those known in the art. An electromagnetic field acts on the one or more gases to produce a plasma in the plasma-generating chamber. Ions and/or radicals from the remote plasma may interact with the photopatterned metal-containing resist. The ions and/or radicals may include ions and/or radicals of an organic acid such as trifluoroacetic acid. In some implementations, a vacuum line is coupled to the process chamber for pressure control, and a development chemistry line may be coupled to the plasma-generating chamber for delivery of the one or more gases into the plasma-generating chamber. The process chamber may include one or more heaters for temperature control, such as heaters coupled to a heating assembly facing the substrate for substrate temperature control. In some implementations, development of the photopatterned metal-containing resist is exposed to conditions optimized for generating a gentle plasma characterized by high pressure and low power. In some implementations, RF power levels may be tuned, where RF power may be equal to or less than about 1000 W, equal to or less than about 800 W, or equal to or less than about 500 W.

[0094] In addition or in the alternative to plasma activation, activation of the one or more gases in a dry development process may occur by photoactivation. In some implementations, the photoactivation may be achieved by exposure to ultraviolet (UV) radiation. For example, the

process chamber may include a lamp such as a UV lamp configured to generate UV radiation. Exposing the one or more gases to UV radiation may generate radicals of the one or more gases that can be used in dry development of the photopatterned metal-containing resist. Exposure of the one or more gases to UV radiation may occur in a manner without exposing the photopatterned metal-containing resist to UV radiation. In other words, the photopatterned metal-containing resist is out-of-sight with respect to the UV lamp.

[0095] It will be understood that the aforementioned methods of thermal development, plasma development, and photoactivation development may be combined together. Such development methods may be applied simultaneously or sequentially. The one or more development methods may be applied while flowing dry development chemistry in the vapor phase. The development can result in a positive or a negative tone, in which the dry development chemistry selectively removes either the unexposed or the exposed material, leaving behind the exposed or unexposed counterpart as a mask.

[0096] As described above, etch selectivity during dry development is tunable by controlling process conditions such as temperature, pressure, gas flow, gas composition, and plasma power, among other tunable process conditions. Tuning etch selectivity in a single step or multiple steps may achieve desired patterned characteristics. In some implementations, etch selectivity during dry development is tuned across one or more steps to influence resist profile. More specifically, the amount of taper or a re-entrant angle in the resist profile can be controlled by applying dry development chemistry of different etch selectivity over one or more steps. Descumming, photoresist reworking, curing, smoothing, and cleaning operations may also be tuned according to a tunable etch selectivity.

[0097] Figures 3A–3C show cross-sectional schematic illustrations of various processing stages of dry development according to some implementations. The example shown in Figures 3A–3C illustrates negative tone dry development. As shown in Figure 3A, a wafer 300 includes a substrate 302 and a substrate layer 304 to be etched. In some implementations, the substrate layer 304 includes an ashable hard mask such as spin-on carbon (SoC) or other material, e.g., silicon, silicon oxide, silicon nitride, silicon carbide, etc. In some implementations, the substrate layer 304 may be a layer stack disposed on the substrate 302. The wafer 300 further includes a photopatterned metal-containing EUV resist film 306. For example, the photopatterned metal-containing EUV resist film 306 may be an organo-metal-containing layer disposed on the substrate layer 304 to be etched. The photopatterned metal-containing EUV resist film 306 may have a thickness between about 5 nm and about 50 nm or between about 10 nm and about 30 nm. The photopatterned metal-

containing EUV resist film 306 may be provided in a process chamber after photopatterning in an EUV scanner and/or after a PEB treatment as described above. The photopatterned metal-containing EUV resist film 306 includes non-EUV exposed regions 306a and EUV exposed regions 306b. As shown in Figure 3B, the non-EUV exposed regions 306a of the photopatterned metal-containing EUV resist film 306 can be removed in a dry development process by exposure to flows of dry development chemistry without striking a plasma. The dry development chemistry may include an organic vapor such as an organic acid. The organic acid may include a halogenated or fluorinated carboxylic acid. Examples of organic acids include but are not limited to trifluoroacetic acid, hexafluoro-acetylacetone, trichloroacetic acid, mono-fluoroacetic acid, and difluoroacetic acid. Other examples of organic acids include a mixed halide acetic acid such as chloro-difluoro-acetic acid, a sulfur-containing analogue of acetic acid, thioacetic acid, and thioglycolic acid. A resist mask 308 is formed after development by removal of the non-EUV exposed regions 306a. Thereafter, the substrate layer 304 to be etched may be etched using the resist mask 308 to provide the structure depicted in Figure 3C.

**[0098]** An organo-metal-oxide film may have a tetrahedrally coordinated structure. Exposed regions have higher levels of Sn-O-Sn crosslinking, resulting in higher density and lower/slower reactivity with halogenated carboxylic acids. Unexposed regions exhibit lower density due to the presence of bulky alkyl substituents which block the close approach and condensation of Sn-OH moieties. In unexposed regions, an acid such as trifluoroacetic acid more readily protonates more “basic” and accessible oxygen lone pairs characteristic of more tetrahedral-coordinated organotin oxide hydroxides. Volatile byproducts of trifluoroacetates are generated and removed from the unexposed regions. Without being limited by any theory, trifluoroacetic acid may selectively protonate an oxygen lone pair to form a volatile byproduct. When the alkyl group is iso-propyl, at typical EUV patterning doses, at least 2 out of every 3 isopropyl substituents are removed, such that after a PEB step exposed areas condense to form a higher density more SnO<sub>2</sub> like material exhibiting lower reactivity with trifluoroacetic acid due to adoption of a more hexacoordinate tin structure in which oxygen atoms are less accessible, resulting in much slower reactivity with trifluoroacetic acid.

**[0099]** In some instances, there may be residue or scum remaining after development. Residue may result from slower etching components in less homogeneous EUV resist formulations, including those applied by spin-coating techniques. Such scum may contain high metal concentrations, which may be problematic during subsequent pattern transfer.

[0100] Additionally or alternatively, roughness may form after development on sidewalls of etched features in a developed pattern. Some of this may be attributed to stochastics or non-optimal Gaussian distribution of the light resulting in partially or fully exposed material in areas where the resist should remain unexposed or vice versa.

5 [0101] In some implementations, dry development may be accompanied by a descum/smoothing operation. In some implementations, a descumming and smoothing operation may be an inert gas plasma desorption operation. For example, the inert gas plasma desorption operation may be a helium plasma desorption operation. The inert gas plasma desorption operation may be performed after dry development or cycled with dry development.

10 [0102] Figure 4A shows cross-sectional schematic illustrations of dry development without applying inert gas plasma according to some implementations. A photopatterned metal-containing EUV resist film includes exposed and unexposed regions. As shown in Figure 4A, particles or clusters of metal oxide (e.g.,  $\text{SnO}_x$ ) may occupy the unexposed regions. As dry development proceeds, the clusters of metal oxide become more concentrated. Clusters of metal oxide are  
15 generally difficult to remove. Development may be selective for removal of organic material. After removal of the unexposed regions, the clusters of metal oxide may remain on a surface of the substrate as scum. Clusters of metal oxide that remain on sidewalls of the exposed regions may lead to roughness.

[0103] Figure 4B shows cross-sectional schematic illustrations of dry development cycling inert  
20 gas plasma for descumming according to some implementations. A first phase involves dry development to remove a substantial portion of the unexposed regions of the photopatterned metal-containing EUV resist film. The dry development chemistry may include, for example, an organic acid and/or hydrogen halide. A substantial portion may represent at least more than 70 volume % of the unexposed regions, more than 80 volume % of the unexposed regions, or more than 90  
25 volume % of the unexposed regions. Clusters of metal oxide concentrate at a surface of the remaining unexposed regions of the EUV resist film. A second phase involves applying an inert gas plasma like helium plasma with low power and high ion energy for a short duration. The helium plasma removes the clusters of metal oxides. In addition, the helium plasma removes clusters from sidewalls and smooths the sidewalls. Helium plasma treatment may also serve to  
30 help harden or cure the patterned EUV resist film to form a denser metal oxide like hard mask. After the helium plasma treatment, a less selective dry etch step can be employed to remove any residue remaining in unexposed regions of the EUV resist film.

[0104] In some implementations, dry development may cycle with helium plasma treatment across one or more cycles until the unexposed regions of the EUV resist film are removed. The helium plasma descum/smoothing may be cycled with dry development, as described above, for enhanced results. In this way, most of the organic component of the unexposed regions, for example, of the pattern is removed by the dry development, then a short helium plasma operation can remove some of the concentrated metal at the surface, opening up access to the remaining underlying organic material, that can then be removed in a subsequent dry development operation/cycle. Another cycle of helium plasma may be used to remove any remaining metal to leave a clean and smooth feature surface. The cycling can be continued until all or substantially all the scum and roughness residue is removed to leave a clean and smooth feature surface.

[0105] Process conditions for a descumming and smoothing operations may be controlled during or after development. In some implementations, reactant flow may be between about 50 sccm and about 1000 sccm or between about 100 sccm and about 500 sccm, such as about 500 sccm He. In some implementations, a temperature may be between about -60°C and about 120°C, between about -20°C and about 60°C, or between about 20°C and about 40°C, such as about 20°C. In some implementations, chamber pressure may be between about 1 mTorr and about 300 mTorr, between about 5 mTorr and about 100 mTorr, between about 5 mTorr and about 20 mTorr, such as about 10 mTorr. The plasma power may be relatively low with high ion energy. In some implementations, plasma power may be between about 50 W and about 1000 W, between about 100 W and about 500 W, or between about 100 W and about 300 W, such as about 300 W. In some implementations, the wafer bias is between about 10 V and about 500 V, between about 50 V and about 300 V, such as about 200 V. The plasma may be generated using a high RF frequency. In some implementations, the RF frequency is 13.56 MHz. The duration of exposure to inert gas plasma may be relatively short so as to avoid excess exposure to UV radiation during plasma exposure. In some implementations, the duration of exposure is between about 0.5 seconds and about 5 seconds, between about 1 second and about 3 seconds, such as about 2 seconds.

[0106] The inert gas plasma treatment for descumming and cleaning of the unexposed resist residue can have the collateral benefit of curing the exposed resist to harden it, thereby enhancing its hard mask function in subsequent operations to etch the underlying substrate. This resist hardening is achieved by exposure of the EUV exposed resist to UV radiation generated by the inert gas plasma, which may be continued after the descum/smoothing is complete with the bias turned off. The inert gas plasma curing may alternatively be performed if no descum/smoothing is needed or performed.

[0107] Not only can organic vapors of the present disclosure be employed in dry development processes, organic vapors such as trifluoroacetic acid may be employed in dry chamber clean or other processing operations for dry removal of metal-containing resist.

[0108] Figure 5 presents a flow diagram of an example method of dry chamber cleaning according to some implementations. Dry chamber clean may be performed after deposition, bevel and/or backside clean, bake, development, or etch. In some implementations, dry chamber clean may be performed after deposition of resist material and in the same process chamber as deposition of the resist material. The operations of a process 500 may be performed in different orders and/or with different, fewer, or additional operations. Aspects of the process 500 may be described with reference to Figures 6A–6D. One or more operations of the process 200 may be performed using an apparatus described in any one of Figures 7–11B. In some implementations, the operations of the process 500 may be implemented, at least in part, according to software stored in one or more non-transitory computer readable media.

[0109] At block 502 of the process 500, a metal-containing resist material is deposited on a surface of a semiconductor substrate in a process chamber, where a portion of the metal-containing resist material forms a residue on one or more surfaces of the process chamber. The composition and deposition of such metal-containing resist material may be described, for example, in International Patent Application No. PCT/US2019/31618, filed May 9, 2019, incorporated by reference herein for the disclosure of the methods and materials applicable to the present disclosure. Methods include those where polymerized organometallic materials are produced in the vapor phase and deposited on the semiconductor substrate. In some implementations, the metal-containing resist material is a metal oxide-containing EUV resist material. For example, an element in the metal-containing resist material is selected from a group consisting of: tin, hafnium, tellurium, bismuth, indium, antimony, iodine, germanium, and combinations thereof. In some implementations, the metal-containing resist material includes organo-metal oxides such as organotin oxides.

[0110] In some implementations, the process chamber in which the semiconductor substrate is provided may be a dry deposition chamber. In other implementations, the process chamber in which the semiconductor substrate is provided in may be a bevel edge and/or backside clean chamber, PAB treatment chamber, PEB treatment chamber, development chamber, or etch chamber. Any of the foregoing chambers may accumulate metal-containing resist material on internal surfaces over time. As more and more semiconductor substrates are processed in a process chamber, unintended metal-containing resist material may grow on the internal surfaces as residue.

Periodic cleaning is needed to remove the unintended deposits of the metal-containing resist material. The cleaning may be performed “*in situ*,” where the dry chamber clean is performed in the same process chamber where unintended metal-containing resist material formed.

5 [0111] The residue may be formed on one or more surfaces of the process chamber, where the one or more surfaces may include one or more of chamber walls, ceilings, floors, showerhead surfaces, nozzle surfaces, and substrate support surfaces. In some implementations, the residue may form as a result of dry deposition processes such as CVD or ALD processes. A thickness of the residue on the one or more surfaces may increase over time as a result of additional processing (e.g., deposition) operations being performed in the process chamber. In some implementations, 10 an average thickness of the residue is equal to or greater than about 2 nm, equal to or greater than about 3 nm, equal to or greater than about 5 nm, or equal to or greater than about 10 nm. The metal-containing resist material is prone to flake off, shed particles, or peel from the one or more surfaces to contaminate subsequent semiconductor substrates during processing.

[0112] Figure 6A shows a cross-sectional schematic illustration of a metal-containing EUV resist material 602 formed on chamber walls 604 of a process chamber. The metal-containing EUV resist material 602 may include particles or clusters of metal oxide 606. Particles or clusters of metal oxide 606 may be difficult to remove. In some implementations, the metal-containing EUV resist material 602 is formed by vapor deposition methods such as CVD or ALD. Over time, the metal-containing EUV resist material 602 may accumulate in thickness on the chamber walls 15 604 of the process chamber. The metal-containing EUV resist material 602 may be an organotin oxide. The particles or clusters of metal oxide 606 may include tin oxide. 20

[0113] Returning to Figure 5, at block 504 of the process 500, a dry etchant comprising an organic vapor is introduced into the process chamber, where the dry etchant at least partially removes the residue on the one or more surfaces of the process chamber. In some implementations, 25 the organic vapor is an organic acid. The organic acid may be a strong organic acid having a pK<sub>a</sub> that is equal to or less than about 3.8. In some implementations, the organic acid includes a carboxylic acid. In some implementations, the organic acid includes trifluoroacetic acid. The organic vapor may be halogenated or at least fluorinated. In some implementations, the organic vapor includes hexafluoro-acetylacetone. In some implementations, the organic vapor includes 30 trifluoroacetic acid anhydride, acetic acid anhydride, trichloroacetic acid, mono-fluoroacetic acid, di-fluoroacetic acid, a mixed halide acetic acid such as chloro-difluoro-acetic acid, a sulfur-containing analogue of acetic acid, thioacetic acid, or thioglycolic acid. In some implementations, the dry etchant includes a mixture of a carboxylic acid and a hydrogen halide in a vapor phase.

For example, the dry etchant includes a mixture of acetic acid or formic acid with hydrogen chloride or hydrogen bromide. In some implementations, the organic vapor may be flowed with or without inert/carrier gas such as helium, neon, argon, xenon, and nitrogen.

5 [0114] In some implementations, at least partial removal of the residue includes reacting the organic vapor with the metal-containing resist material to form a volatile compound at a temperature less than about 200°C. In some implementations, at least partial removal includes substantial removal of the residue, where “substantial removal” refers to sufficient removal of the residue so that at least some of the one or more surfaces are exposed following removal.

10 [0115] In some implementations, the process chamber may be prepared with desired conditions for dry chamber cleaning prior to introducing the dry etchant. Preparation of the process chamber may achieve certain pressure conditions, levels of loose particles or film impurities, moisture levels, temperature conditions, or protection of surfaces or components (e.g., substrate support) in the process chamber from the dry etchant. In some implementations, preparing the process chamber may include purging and/or pumping the process chamber to remove unwanted particles.  
15 A purge gas may be flowed into the process chamber to facilitate removal of unwanted particles in the process chamber. A purge of metal organic precursor may be useful to avoid undesired byproducts and ensure sufficient removal of metal organic precursor before dry chamber cleaning.

20 [0116] In some implementations, chamber walls and other components may be heated to release unreacted precursor. The heat may additionally or alternatively facilitate removal of moisture in the process chamber. Without being limited by any theory, the presence of moisture can slow down the reaction between the dry etchant and the metal-containing resist material for removal of the metal-containing resist material. In addition, the increased temperature in the process chamber promotes a higher etch rate for removal of the metal-containing resist material. One or more heaters in the process chamber may heat the one or more surfaces to an elevated temperature. In  
25 some implementations, the elevated temperature may be between about 20°C and about 180°C, between about 40°C and about 160°C, or between about 80°C and about 140°C.

30 [0117] In some implementations, preparing the process chamber may include providing a dummy substrate on a substrate support in the process chamber. Thus, the semiconductor substrate having the metal-containing resist material deposited thereon may be transferred out of the process chamber prior to dry chamber cleaning. That way, the semiconductor substrate is not exposed to the dry etchant when removing the residue of the metal-containing resist material from the one or more surfaces of the process chamber. The dummy substrate may be provided on the substrate support to protect the substrate support (e.g., electrostatic chuck) from exposure to the dry etchant

during dry chamber cleaning. Alternatively, protection of the substrate support may occur by providing a protective cover over the substrate support during dry chamber cleaning.

[0118] The dry etchant may be introduced through a showerhead or separate chamber inlet coupled to the process chamber. The dry etchant may flow into the process chamber to react with the residue of the metal-containing resist material and form volatile products. Without being limited by any theory, an organo-metal-oxide resist material may have a tetrahedrally coordinated structure, and an organic vapor such as trifluoroacetic acid may protonate an oxygen lone pair to form a volatile byproduct. After volatile byproducts are formed, the process chamber may be pumped and purged to remove the volatile byproducts. Furthermore, the process chamber may be pumped and purged to remove residual dry etchant. Such residual dry etchant may cause undesired etching of subsequent semiconductor substrates.

[0119] The dry chamber clean may be optimized for low etch selectivity or high etch rate of resist material deposited in the process chamber. That way, unwanted resist material may be quickly and efficiently removed. In some implementations, higher temperatures and/or higher pressures may result in lower etch selectivity of the dry etchant and increase the etch rate. For instance, the resist material may be removed with an etch rate of up to 1 nm/s. During exposure to the dry etchant, the residue of the metal-containing resist material on the one or more surfaces may be subjected to an elevated temperature. The elevated temperature may be between about 20°C and about 180°C, between about 40°C and about 160°C, or between about 80°C and about 140°C. In some implementations, reacting the residue of the metal-containing resist material with the organic vapor forms a volatile compound at a temperature less than about 200°C. During exposure to the dry etchant, the pressure in the process chamber may be high. In some implementations, a chamber pressure is between about 0.01 Torr and 765 Torr, between about 0.1 Torr and 100 Torr, or between about 0.1 Torr and about 6 Torr. In some implementations, the chamber pressure is cycled between high and low pressures during exposure to the dry etchant. Organic vapor flow rate may also be tuned to control etch selectivity. In some implementations, an organic vapor flow rate is between about 0.05 SLM and about 10 SLM or between about 0.1 SLM and about 5 SLM.

[0120] As discussed above with respect to dry development, dry chamber clean is performed using an organic vapor such as an organic acid instead of vapors of halogens. Vapors of halogens such as vapors of hydrogen halides are prone to leave residual etch byproducts after removal of metal-containing resist material. However, an organic vapor such as trifluoroacetic acid form more volatile etch byproducts that are less difficult to remove from the process chamber. Organic vapors

such as trifluoroacetic acid may be used in dry chamber cleaning in a plasma-free thermal process. In other words, the residue of the metal-containing resist material is removed without striking a plasma. Residual carbon, contaminants, or other remaining materials may or may not be removed by exposure to plasma. In some implementations, introduction of the dry etchant may be followed  
5 by exposing the one or more surfaces to an oxidizing gas such as oxygen (O<sub>2</sub>), ozone (O<sub>3</sub>), carbon dioxide (CO<sub>2</sub>), or carbon monoxide (CO).

[0121] Due to the ability to clean as-deposited films (non-exposed or non-crosslinked) thermally, without the need for use of plasma, the approach described herein can also clean downstream and upstream components of the tool, beyond the process chamber (e.g., the exhaust  
10 lines going from the process chamber to the vacuum pump). More generally, this dry clean method can be used to clean other parts and components contaminated having a similar composition of a metal that has volatile byproducts with organic vapors.

[0122] In some implementations, interior surfaces of the process chamber may be compatible with the organic vapor of the present disclosure. Rather than having the interior surfaces of the  
15 process chamber resistant to plasma as well as resistant to vapors of halogens such as hydrogen halides, the interior surfaces may include any materials that are simply resistant to the organic vapor of the present disclosure. In some implementations, chamber walls of the process chamber may include aluminum oxide, anodized aluminum, or plastic.

[0123] In some implementations, the process chamber may include chamber parts temperature control coupled to the one or more surfaces (e.g., chamber walls) to control temperature. In some  
20 implementations, the process chamber may include gas inlets other than the showerhead for delivery of the dry etchant. The gas inlets may be positioned in regions of the process chamber with a higher concentration of the metal-containing resist material. The gas inlets may be positioned in regions of the process chamber where dry etchant is less likely to reach through  
25 delivery via a showerhead. In some implementations, the gas inlets may be positioned below the substrate support, positioned in the walls of the process chamber, and/or positioned close to an exhaust of the process chamber. Multiple gas inlets may be used for delivery of the dry etchant into the process chamber. This can ensure the dry clean of the entire process chamber. In various implementations, the dry etchant is delivered into the process chamber through one or more gas  
30 inlets separate from the showerhead, and deposition gases may be delivered into the process chamber through the showerhead. In some implementations, the showerhead may supply separate gases by keeping the gases largely segregated within the showerhead. The showerhead may include multiple plenum volumes. Multiple exhaust lines may be used to ensure separation of

gases downstream from the process chamber. A switch may be operably coupled to the multiple exhaust lines so as to permit separation of dry etchant chemistry from deposition gases/precursors.

[0124] To protect the showerhead, a pressure differential may be used to prevent the dry etchant from entering the showerhead (e.g., backflow). In some implementations, the dry etchant may clean internal surfaces of the showerhead by flowing the dry etchant through the showerhead. However, residual organic vapors or moisture may be retained inside channels of the showerhead. In some implementations, the showerhead may be made out of a transparent material and heated with a suitable light source. For example, an irradiation source tuned to the appropriate wavelength (e.g., IR or blue wavelength) can directly heat the residual organic vapors and/or moisture to remove the residual organic vapors and/or moisture. Alternatively, the residual organic vapors and/or moisture may be removed by gas purging.

[0125] Figure 6B shows a cross-sectional schematic illustration of the chamber walls 604 after a dry etchant removes the metal-containing EUV resist material 602 from the chamber walls 604. The dry etchant may include an organic vapor such as an organic acid, where the organic acid may include trifluoroacetic acid. The chamber walls 604 may be heated to an elevated temperature to promote low etch selectivity. The process chamber may be increased to a high pressure to promote low etch selectivity. Removal of the metal-containing EUV resist material 602 may occur without using plasma. Residual particles or clusters of metal oxide 606 may remain on the chamber walls 604 after exposure to the dry etchant. In addition, residual dry etchant 608 may remain in the process chamber.

[0126] Returning to Figure 5, at block 506 of the process 500, the process chamber is optionally purged to remove residual dry etchant from the process chamber. The purge operation may involve flowing a purge gas into the process chamber or a combination of flowing a purge gas and pumping the process chamber to a desired chamber pressure. The purge gas may be an inert gas and/or a reactive gas. The reactive gas may react with residual dry etchant to facilitate ease of removal. The reactive gas may be, for example, a tin-based precursor such as an organotin precursor. The inert gas may be argon, helium, xenon, or nitrogen. The chamber pressure may be between about 0.1 Torr and about 6 Torr.

[0127] In some implementations, the purge operation may proceed at a high temperature. The high temperature may facilitate removal of organic vapors from the process chamber. In one example, one or more heaters coupled to the one or more surfaces of the process chamber may heat the process chamber to the high temperature. In another example, one or more IR sources or LEDs may be installed in the process chamber to heat the process chamber to the high temperature.

The high temperature may be between about 20°C and about 180°C or between about 80°C and about 140°C.

[0128] In some implementations, a direct or remote plasma-based treatment is useful to accelerate the removal of residual dry etchant, where the residual dry etchant may cover internal surfaces of the process chamber following dry chamber clean. In other implementations, a non-plasma treatment may be useful to accelerate the removal of residual dry etchant. Oxidizing gas may be introduced to oxidize residual dry etchant. Thus, the non-plasma treatment may include delivering a flow of ozone and/or oxygen gas.

[0129] Figure 6C shows a cross-sectional schematic illustration of the chamber walls 604 after removal of residual dry etchant 608 from the process chamber. Pumping/purging operations may be performed to exhaust the residual dry etchant 608 from the process chamber. In some implementations, the chamber walls 604 or other components of the process chamber may be heated to promote release of the residual dry etchant 608. In some implementations, direct or remote plasma-based treatments may be applied to remove the residual dry etchant 608, where such plasma-based treatments may include a fluorine-based plasma process, oxygen-based plasma process, or combinations thereof. In some other implementations, a non-plasma treatment may be applied to remove the residual dry etchant 608. Particles or clusters of metal oxide 606 may remain on the chamber walls 604.

[0130] Returning to Figure 5, at block 508 of the process 500, the one or more surfaces of the process chamber are optionally conditioned by forming a protective coating of the metal-containing resist material on the one or more surfaces of the process chamber. An average thickness of the protective coating may be less than an average thickness of the residue of the metal-containing resist material. In some implementations, the average thickness of the protective coating is equal to or greater than about 1 nm, equal to or greater than about 2 nm, equal to or greater than about 3 nm, or between about 1 nm and about 5 nm. Alternatively, the one or more surfaces are optionally conditioned by forming a protective coating made of different materials than the metal-containing resist material. Such a protective coating may be a variation of organotin oxide. After exposure to the dry etchant, the one or more surfaces are left exposed. Exposed surfaces in the process chamber may be vulnerable to attack especially by halogen-based species. The conditioning operation may provide protection of the one or more surfaces. Additionally, the conditioning operation may cover residual particles or clusters of metal oxide stuck on the one or more surfaces. That way, the particles or clusters of metal oxide are less likely to contaminate wafers during subsequent processing.

[0131] Conditioning the one or more surfaces of the process chamber may occur by a vapor-based deposition technique such as a CVD or ALD technique. Organometallic materials are produced in the vapor phase and deposited on the one or more surfaces of the process chamber. The organometallic materials may be, for example, deposited based on a gas phase reaction of an organotin precursor such as isopropyl(tris)(dimethylamino)tin and water vapor. The flow of water vapor may be relatively low. During conditioning, the substrate support may be protected or covered by a dummy wafer or other protective covering. The protective coating may be formed on chamber walls, floors, ceilings, or chamber components such as gas inlets, showerheads, and exhaust lines. After deposition of the protective coating of the metal-containing resist material, pumping/purging operations may follow to remove excess precursor and/or counter-reactant. Conditioning the one or more surfaces of the process chamber can trap residual particles of metal oxide and limit particle contamination.

[0132] Figure 6D shows a cross-sectional schematic illustration of a metal-containing resist material 610 formed on the chamber walls 604 of the process chamber. The metal-containing EUV resist material 610 may be re-deposited in a conditioning operation to protect the chamber walls 604 and trap the particles or clusters of metal oxide 606 from contaminating wafers during processing. This may also be referred to as chamber seasoning. The metal-containing EUV resist material 610 is formed by a vapor deposition method such as CVD or ALD. In some implementations, the metal-containing EUV resist material 610 may be an organotin oxide. By conditioning/seasoning the chamber walls 604 and other internal surfaces of the process chamber, undesirable first wafer effects are mitigated when re-initiating deposition operations on semiconductor substrates.

[0133] While this disclosure frequently refers to the removal of EUV-sensitive films that have been exposed and/or developed, the removal processes described can be extended to EUV films of similar composition (e.g., other  $MO_xR_y$ -based films), for example, other films containing a metal oxide, in which the metal can form volatile byproducts with organic vapors, including unexposed EUV resist films. In some implementations, films other than EUV resists can be removed by this method, for example hard masks, UV resists or films of similar composition having other applications; in this respect, the described removal process relates to the film's chemical composition, as opposed to its function.

Apparatus

[0134] An apparatus of the present disclosure is configured for dry removal of EUV resist. The apparatus may be configured to perform dry development or dry chamber clean. The apparatus may be configured for other processing operations such as deposition, bevel and backside cleaning, 5 post-application baking, EUV scanning, post-exposure baking, photoresist reworking, descum, smoothing, curing, and other operations. In some implementations, the apparatus is configured to perform all dry operations. In some implementations, the apparatus is configured to perform a combination of wet and dry operations. The apparatus may include a single wafer chamber or multiple stations in the same process chamber. With multiple stations in the same process 10 chamber, various processing operations such as those described in the present disclosure may be performed in different stations in the same process chamber. In one example, PEB thermal treatment may be performed in one station and development in another station.

[0135] The apparatus configured for dry removal of EUV resist includes a process chamber with a substrate support. The apparatus may include a dry etch line coupled to the process chamber for 15 delivery of etch gas. In some implementations, the etch gas includes an organic vapor such as trifluoroacetic acid. The apparatus may include one or more heaters for temperature control. Such heaters may be provided in the process chamber and/or in the substrate support. In some implementations, there may be multiple gas inlets positioned within the process chamber to flow etch gas near regions where unintended EUV resist tend to form. The apparatus may further 20 include one or more sensors for sensing particle count, wafer count, thickness count, or other parameters for triggering the dry chamber clean and/or endpoint of the dry chamber clean.

[0136] In some implementations, the process chamber is made of an inexpensive material such as plastic. In some other implementations, the process chamber is made of a metal such as anodized aluminum or a ceramic such as aluminum oxide.

25 [0137] Figure 7 depicts a schematic illustration of an example process station that is suitable for performing dry development, clean, rework, descum, and smoothing operations according to some implementations. A plurality of process stations 700 may be included in a common low-pressure process tool environment. For example, Figure 8 depicts an implementation of a multi-station processing tool 800, such as a VECTOR® processing tool available from Lam Research 30 Corporation, Fremont, CA. In some implementations, one or more hardware parameters of the process tool 800 including those discussed in detail below may be adjusted programmatically by one or more computer controllers 850.

[0138] A process station may be configured as a module in a cluster tool. Figure 10 depicts a semiconductor process cluster tool architecture with vacuum-integrated deposition and patterning modules suitable for implementation of the implementations described herein. Such a cluster process tool architecture can include resist deposition, resist exposure (EUV scanner), resist development and etch modules, as described above and further below with reference to Figures 9 and 10.

[0139] In some implementations, certain of the processing functions can be performed consecutively in the same module, for example dry development and etch or dry deposition and dry chamber clean. And implementations of this disclosure are directed to methods and apparatus for receiving a wafer, including an EUV resist thin film layer disposed on a layer or layer stack to be etched, to a dry development/etch chamber following photopatterning in an EUV scanner; dry developing photopatterned EUV resist thin film layer; and then etching the underlying layer using the patterned EUV resist as a mask, as described herein.

[0140] Returning to Figure 7, process station 700 fluidly communicates with reactant delivery system 701 for delivering process gases to a distribution showerhead 706. Reactant delivery system 701 optionally includes a mixing vessel 704 for blending and/or conditioning process gases, for delivery to showerhead 706. One or more mixing vessel inlet valves 720 may control introduction of process gases to mixing vessel 704. Where plasma exposure is used, plasma may also be delivered to the showerhead 706 or may be generated in the process station 700. As noted above, in at least some implementations, non-plasma thermal exposure is favored.

[0141] Figure 7 includes an optional vaporization point 703 for vaporizing liquid reactant to be supplied to the mixing vessel 704. In some implementations, a liquid flow controller (LFC) upstream of vaporization point 703 may be provided for controlling a mass flow of liquid for vaporization and delivery to process station 700. For example, the LFC may include a thermal mass flow meter (MFM) located downstream of the LFC. A plunger valve of the LFC may then be adjusted responsive to feedback control signals provided by a proportional-integral-derivative (PID) controller in electrical communication with the MFM.

[0142] Showerhead 706 distributes process gases toward substrate 712. In the implementation shown in Figure 7, the substrate 712 is located beneath showerhead 706 and is shown resting on a pedestal 708. Showerhead 706 may have any suitable shape, and may have any suitable number and arrangement of ports for distributing process gases to substrate 712.

[0143] In some implementations, pedestal 708 may be raised or lowered to expose substrate 712 to a volume 707 between the substrate 712 and the showerhead 706. It will be appreciated that, in

some implementations, pedestal height may be adjusted programmatically by a suitable computer controller 750. In some implementations, the showerhead 706 may have multiple plenum volumes with multiple temperature controls.

5 [0144] In some implementations, pedestal 708 may be temperature controlled via heater 710. In some implementations, the pedestal 708 may be heated to a temperature of greater than 0°C and up to 300°C or more, for example 40°C to 160°C, such as about 80°C to 140°C, during non-plasma thermal exposure of a photopatterned resist to organic vapor development chemistry, such as trifluoroacetic acid, as described in disclosed implementations. In some implementations, the heater 710 of the pedestal 708 may include a plurality of independently controllable temperature control zones.

10 [0145] Further, in some implementations, pressure control for process station 700 may be provided by a butterfly valve 718. As shown in the implementation of Figure 7, butterfly valve 718 throttles a vacuum provided by a downstream vacuum pump (not shown). However, in some implementations, pressure control of process station 700 may also be adjusted by varying a flow rate of one or more gases introduced to the process station 700.

15 [0146] In some implementations, a position of showerhead 706 may be adjusted relative to pedestal 708 to vary a volume 707 between the substrate 712 and the showerhead 706. Further, it will be appreciated that a vertical position of pedestal 708 and/or showerhead 706 may be varied by any suitable mechanism within the scope of the present disclosure. In some implementations, pedestal 708 may include a rotational axis for rotating an orientation of substrate 712. It will be appreciated that, in some implementations, one or more of these example adjustments may be performed programmatically by one or more suitable computer controllers.

20 [0147] Where plasma may be used, for example in descumming or smoothing operations, showerhead 706 and pedestal 708 electrically communicate with a radio frequency (RF) power supply 714 and matching network 716 for powering a plasma. In some implementations, the plasma energy may be controlled by controlling one or more of a process station pressure, a gas concentration, an RF source power, an RF source frequency, and a plasma power pulse timing. For example, RF power supply 714 and matching network 716 may be operated at any suitable power to form a plasma having a desired composition of radical species. Examples of suitable powers are up to about 500 W.

30 [0148] In some implementations, instructions for a controller 750 may be provided via input/output control (IOC) sequencing instructions. In one example, the instructions for setting conditions for a process phase may be included in a corresponding recipe phase of a process recipe.

In some cases, process recipe phases may be sequentially arranged, so that all instructions for a process phase are executed concurrently with that process phase. In some implementations, instructions for setting one or more reactor parameters may be included in a recipe phase. For example, a recipe phase may include instructions for setting a flow rate of a dry development chemistry reactant gas, such as trifluoroacetic acid, and time delay instructions for the recipe phase. In some implementations, the controller 750 may include any of the features described below with respect to system controller 850 of Figure 8.

[0149] As described above, one or more process stations may be included in a multi-station processing tool. Figure 8 shows a schematic view of an implementation of a multi-station processing tool 800 with an inbound load lock 802 and an outbound load lock 804, either or both of which may include a remote plasma source. A robot 806 at atmospheric pressure is configured to move wafers from a cassette loaded through a pod 808 into inbound load lock 802 via an atmospheric port 810. A wafer is placed by the robot 806 on a pedestal 812 in the inbound load lock 802, the atmospheric port 810 is closed, and the load lock is pumped down. Where the inbound load lock 802 includes a remote plasma source, the wafer may be exposed to a remote plasma treatment to treat the substrate surface in the load lock prior to being introduced into a processing chamber 814. Further, the wafer also may be heated in the inbound load lock 802 as well, for example, to remove moisture and adsorbed gases. Next, a chamber transport port 816 to processing chamber 814 is opened, and another robot (not shown) places the wafer into the reactor on a pedestal of a first station shown in the reactor for processing. While the implementation depicted in Figure 8 includes load locks, it will be appreciated that, in some implementations, direct entry of a wafer into a process station may be provided.

[0150] The depicted processing chamber 814 includes four process stations, numbered from 1 to 4 in the implementation shown in Figure 8. Each station has a heated pedestal (shown at 818 for station 1), and gas line inlets. It will be appreciated that in some implementations, each process station may have different or multiple purposes. For example, in some implementations, a process station may be switchable between dry development and etch process modes. Additionally or alternatively, in some implementations, processing chamber 814 may include one or more matched pairs of dry development and etch process stations. While the depicted processing chamber 814 includes four stations, it will be understood that a processing chamber according to the present disclosure may have any suitable number of stations. For example, in some implementations, a processing chamber may have five or more stations, while in other implementations a processing chamber may have three or fewer stations.

[0151] Figure 8 depicts an implementation of a wafer handling system 890 for transferring wafers within processing chamber 814. In some implementations, wafer handling system 890 may transfer wafers between various process stations and/or between a process station and a load lock. It will be appreciated that any suitable wafer handling system may be employed. Non-limiting examples include wafer carousels and wafer handling robots. Figure 8 also depicts an implementation of a system controller 850 employed to control process conditions and hardware states of process tool 800. System controller 850 may include one or more memory devices 856, one or more mass storage devices 854, and one or more processors 852. Processor 852 may include a CPU or computer, analog, and/or digital input/output connections, stepper motor controller boards, etc.

[0152] In some implementations, system controller 850 controls all of the activities of process tool 800. System controller 850 executes system control software 858 stored in mass storage device 854, loaded into memory device 856, and executed on processor 852. Alternatively, the control logic may be hard coded in the controller 850. Applications Specific Integrated Circuits, Programmable Logic Devices (e.g., field-programmable gate arrays, or FPGAs) and the like may be used for these purposes. In the following discussion, wherever “software” or “code” is used, functionally comparable hard coded logic may be used in its place. System control software 858 may include instructions for controlling the timing, mixture of gases, gas flow rates, chamber and/or station pressure, chamber and/or station temperature, wafer temperature, target power levels, RF power levels, substrate pedestal, chuck and/or susceptor position, and other parameters of a particular process performed by process tool 800. System control software 858 may be configured in any suitable way. For example, various process tool component subroutines or control objects may be written to control operation of the process tool components used to carry out various process tool processes. System control software 858 may be coded in any suitable computer readable programming language.

[0153] In some implementations, system control software 858 may include input/output control (IOC) sequencing instructions for controlling the various parameters described above. Other computer software and/or programs stored on mass storage device 854 and/or memory device 856 associated with system controller 850 may be employed in some implementations. Examples of programs or sections of programs for this purpose include a substrate positioning program, a process gas control program, a pressure control program, a heater control program, and a plasma control program.

[0154] A substrate positioning program may include program code for process tool components that are used to load the substrate onto pedestal 818 and to control the spacing between the substrate and other parts of process tool 800.

5 [0155] A process gas control program may include code for controlling organic vapor composition (e.g., trifluoroacetic acid as described herein) and flow rates and optionally for flowing gas into one or more process stations prior to deposition in order to stabilize the pressure in the process station. A pressure control program may include code for controlling the pressure in the process station by regulating, for example, a throttle valve in the exhaust system of the process station, a gas flow into the process station, etc.

10 [0156] A heater control program may include code for controlling the current to a heating unit that is used to heat the substrate. Alternatively, the heater control program may control delivery of a heat transfer gas (such as helium) to the substrate.

[0157] A plasma control program may include code for setting RF power levels applied to the process electrodes in one or more process stations in accordance with the implementations herein.

15 [0158] A pressure control program may include code for maintaining the pressure in the reaction chamber in accordance with the implementations herein.

[0159] In some implementations, there may be a user interface associated with system controller 850. The user interface may include a display screen, graphical software displays of the apparatus and/or process conditions, and user input devices such as pointing devices, keyboards,  
20 touch screens, microphones, etc.

[0160] In some implementations, parameters adjusted by system controller 850 may relate to process conditions. Non-limiting examples include process gas composition and flow rates, temperature, pressure, plasma conditions (such as RF bias power levels), etc. These parameters may be provided to the user in the form of a recipe, which may be entered utilizing the user  
25 interface.

[0161] Signals for monitoring the process may be provided by analog and/or digital input connections of system controller 850 from various process tool sensors. The signals for controlling the process may be output on the analog and digital output connections of process tool 800. Non-limiting examples of process tool sensors that may be monitored include mass flow controllers,  
30 pressure sensors (such as manometers), thermocouples, etc. Appropriately programmed feedback and control algorithms may be used with data from these sensors to maintain process conditions.

[0162] System controller 850 may provide program instructions for implementing the above-described deposition processes. The program instructions may control a variety of process parameters, such as DC power level, RF bias power level, pressure, temperature, etc. The instructions may control the parameters to operate development, clean, and/or etch processes according to various implementations described herein.

[0163] The system controller 850 will typically include one or more memory devices and one or more processors configured to execute the instructions so that the apparatus will perform a method in accordance with disclosed implementations. Machine-readable media containing instructions for controlling process operations in accordance with disclosed implementations may be coupled to the system controller 850.

[0164] In some implementations, the system controller 850 is part of a system, which may be part of the above-described examples. Such systems can include semiconductor processing equipment, including a processing tool or tools, chamber or chambers, a platform or platforms for processing, and/or specific processing components (a wafer pedestal, a gas flow system, etc.). These systems may be integrated with electronics for controlling their operation before, during, and after processing of a semiconductor wafer or substrate. The electronics may be referred to as the “controller,” which may control various components or subparts of the system or systems. The system controller 850, depending on the processing conditions and/or the type of system, may be programmed to control any of the processes disclosed herein, including the delivery of processing gases, temperature settings (e.g., heating and/or cooling), pressure settings, vacuum settings, power settings, radio frequency (RF) generator settings, RF matching circuit settings, frequency settings, flow rate settings, fluid delivery settings, positional and operation settings, wafer transfers into and out of a tool and other transfer tools and/or load locks connected to or interfaced with a specific system.

[0165] Broadly speaking, the system controller 850 may be defined as electronics having various integrated circuits, logic, memory, and/or software that receive instructions, issue instructions, control operation, enable cleaning operations, enable endpoint measurements, and the like. The integrated circuits may include chips in the form of firmware that store program instructions, digital signal processors (DSPs), chips defined as application specific integrated circuits (ASICs), and/or one or more microprocessors, or microcontrollers that execute program instructions (e.g., software). Program instructions may be instructions communicated to the system controller 850 in the form of various individual settings (or program files), defining operational parameters for carrying out a particular process on or for a semiconductor wafer or to a system. The operational

parameters may, in some implementations, be part of a recipe defined by process engineers to accomplish one or more processing steps during the fabrication of one or more layers, materials, metals, oxides, silicon, silicon dioxide, surfaces, circuits, and/or dies of a wafer.

5 [0166] The system controller 850, in some implementations, may be a part of or coupled to a computer that is integrated with, coupled to the system, otherwise networked to the system, or a combination thereof. For example, the system controller 850 may be in the “cloud” or all or a part of a fab host computer system, which can allow for remote access of the wafer processing. The computer may enable remote access to the system to monitor current progress of fabrication operations, examine a history of past fabrication operations, examine trends or performance  
10 metrics from a plurality of fabrication operations, to change parameters of current processing, to set processing steps to follow a current processing, or to start a new process. In some examples, a remote computer (e.g. a server) can provide process recipes to a system over a network, which may include a local network or the Internet. The remote computer may include a user interface that enables entry or programming of parameters and/or settings, which are then communicated to  
15 the system from the remote computer. In some examples, the system controller 850 receives instructions in the form of data, which specify parameters for each of the processing steps to be performed during one or more operations. It should be understood that the parameters may be specific to the type of process to be performed and the type of tool that the system controller 850 is configured to interface with or control. Thus as described above, the system controller 850 may  
20 be distributed, such as by including one or more discrete controllers that are networked together and working towards a common purpose, such as the processes and controls described herein. An example of a distributed controller for such purposes would be one or more integrated circuits on a chamber in communication with one or more integrated circuits located remotely (such as at the platform level or as part of a remote computer) that combine to control a process on the chamber.

25 [0167] Without limitation, example systems may include a plasma etch chamber or module, a deposition chamber or module, a spin-rinse chamber or module, a metal plating chamber or module, a clean chamber or module, a bevel edge etch chamber or module, a physical vapor deposition (PVD) chamber or module, a chemical vapor deposition (CVD) chamber or module, an ALD chamber or module, an atomic layer etch (ALE) chamber or module, an ion implantation  
30 chamber or module, a track chamber or module, an EUV lithography chamber (scanner) or module, a development chamber or module, and any other semiconductor processing systems that may be associated or used in the fabrication and/or manufacturing of semiconductor wafers.

[0168] As noted above, depending on the process step or steps to be performed by the tool, the system controller 850 might communicate with one or more of other tool circuits or modules, other tool components, cluster tools, other tool interfaces, adjacent tools, neighboring tools, tools located throughout a factory, a main computer, another controller, or tools used in material transport that bring containers of wafers to and from tool locations and/or load ports in a semiconductor manufacturing factory.

[0169] ICP reactors which, in certain implementations, may be suitable for etch operations suitable for implementation of some implementations, are now described. Although ICP reactors are described herein, in some implementations, it should be understood that capacitively coupled plasma reactors may also be used.

[0170] Figure 9 schematically shows a cross-sectional view of an inductively coupled plasma apparatus 900 appropriate for implementing certain implementations or aspects of implementations such as dry development, clean, and/or etch, an example of which is a Kiyoo® reactor, produced by Lam Research Corp. of Fremont, CA. In other implementations, other tools or tool types having the functionality to conduct the dry development, clean, and/or etch processes described herein may be used for implementation.

[0171] The inductively coupled plasma apparatus 900 includes an overall process chamber 924 structurally defined by chamber walls 901 and a window 911. The chamber walls 901 may be fabricated from stainless steel, aluminum, or plastic. The window 911 may be fabricated from quartz or other dielectric material. An optional internal plasma grid 950 divides the overall process chamber into an upper sub-chamber 902 and a lower sub chamber 903. In most implementations, plasma grid 950 may be removed, thereby utilizing a chamber space made of sub chambers 902 and 903. A chuck 917 is positioned within the lower sub-chamber 903 near the bottom inner surface. The chuck 917 is configured to receive and hold a semiconductor wafer 919 upon which the etching and deposition processes are performed. The chuck 917 can be an electrostatic chuck for supporting the wafer 919 when present. In some implementations, an edge ring (not shown) surrounds chuck 917, and has an upper surface that is approximately planar with a top surface of the wafer 919, when present over chuck 917. The chuck 917 also includes electrostatic electrodes for chucking and dechucking the wafer 919. A filter and DC clamp power supply (not shown) may be provided for this purpose. Other control systems for lifting the wafer 919 off the chuck 917 can also be provided. The chuck 917 can be electrically charged using an RF power supply 923. The RF power supply 923 is connected to matching circuitry 921 through a connection 927. The matching circuitry 921 is connected to the chuck 917 through a connection 925. In this

manner, the RF power supply 923 is connected to the chuck 917. In various implementations, a bias power of the electrostatic chuck may be set at about 50 V or may be set at a different bias power depending on the process performed in accordance with disclosed implementations. For example, the bias power may be between about 20 V and about 100 V, or between about 30 V and about 150 V.

[0172] Elements for plasma generation include a coil 933 is positioned above window 911. In some implementations, a coil is not used in disclosed implementations. The coil 933 is fabricated from an electrically conductive material and includes at least one complete turn. The example of a coil 933 shown in Figure 9 includes three turns. The cross sections of coil 933 are shown with symbols, and coils having an “X” extend rotationally into the page, while coils having a “●” extend rotationally out of the page. Elements for plasma generation also include an RF power supply 941 configured to supply RF power to the coil 933. In general, the RF power supply 941 is connected to matching circuitry 939 through a connection 945. The matching circuitry 939 is connected to the coil 933 through a connection 943. In this manner, the RF power supply 941 is connected to the coil 933. An optional Faraday shield 949 is positioned between the coil 933 and the window 911. The Faraday shield 949 may be maintained in a spaced apart relationship relative to the coil 933. In some implementations, the Faraday shield 949 is disposed immediately above the window 911. In some implementations, the Faraday shield 949 is between the window 911 and the chuck 917. In some implementations, the Faraday shield 949 is not maintained in a spaced apart relationship relative to the coil 933. For example, the Faraday shield 949 may be directly below the window 911 without a gap. The coil 933, the Faraday shield 949, and the window 911 are each configured to be substantially parallel to one another. The Faraday shield 949 may prevent metal or other species from depositing on the window 911 of the process chamber 924.

[0173] Process gases may be flowed into the process chamber through one or more main gas flow inlets 960 positioned in the upper sub-chamber 902 and/or through one or more side gas flow inlets 970. Likewise, though not explicitly shown, similar gas flow inlets may be used to supply process gases to a capacitively coupled plasma processing chamber. A vacuum pump, e.g., a one or two stage mechanical dry pump and/or turbomolecular pump 940, may be used to draw process gases out of the process chamber 924 and to maintain a pressure within the process chamber 924. For example, the vacuum pump may be used to evacuate the lower sub-chamber 903 during a purge operation. A valve-controlled conduit may be used to fluidically connect the vacuum pump to the process chamber 924 so as to selectively control application of the vacuum environment provided by the vacuum pump. This may be done employing a closed loop-controlled flow restriction device, such as a throttle valve (not shown) or a pendulum valve (not shown), during

operational plasma processing. Likewise, a vacuum pump and valve controlled fluidic connection to the capacitively coupled plasma processing chamber may also be employed.

5 [0174] During operation of the apparatus 900, one or more process gases may be supplied through the gas flow inlets 960 and/or 970. In certain implementations, process gas may be supplied only through the main gas flow inlet 960, or only through the side gas flow inlet 970. In some cases, the gas flow inlets shown in the figure may be replaced by more complex gas flow inlets, one or more showerheads, for example. The Faraday shield 949 and/or optional grid 950 may include internal channels and holes that allow delivery of process gases to the process chamber 924. Either or both of Faraday shield 949 and optional grid 950 may serve as a showerhead for delivery of process gases. In some implementations, a liquid vaporization and delivery system may be situated upstream of the process chamber 924, such that once a liquid reactant or precursor is vaporized, the vaporized reactant or precursor is introduced into the process chamber 924 via a gas flow inlet 960 and/or 970.

10 [0175] Radio frequency power is supplied from the RF power supply 941 to the coil 933 to cause an RF current to flow through the coil 933. The RF current flowing through the coil 933 generates an electromagnetic field about the coil 933. The electromagnetic field generates an inductive current within the upper sub-chamber 902. The physical and chemical interactions of various generated ions and radicals with the wafer 919 etch features of and selectively deposit layers on the wafer 919.

15 [0176] If the plasma grid 950 is used such that there is both an upper sub-chamber 902 and a lower sub-chamber 903, the inductive current acts on the gas present in the upper sub-chamber 902 to generate an electron-ion plasma in the upper sub-chamber 902. The optional internal plasma grid 950 limits the amount of hot electrons in the lower sub-chamber 903. In some implementations, the apparatus 900 is designed and operated such that the plasma present in the lower sub-chamber 903 is an ion-ion plasma.

20 [0177] Both the upper electron-ion plasma and the lower ion-ion plasma may contain positive and negative ions, though the ion-ion plasma will have a greater ratio of negative ions to positive ions. Volatile etching and/or deposition byproducts may be removed from the lower sub-chamber 903 through port 922. The chuck 917 disclosed herein may operate at elevated temperatures ranging between about 10°C and about 250°C. The temperature will depend on the process operation and specific recipe.

25 [0178] Apparatus 900 may be coupled to facilities (not shown) when installed in a clean room or a fabrication facility. Facilities include plumbing that provide processing gases, vacuum,

temperature control, and environmental particle control. These facilities are coupled to apparatus 900, when installed in the target fabrication facility. Additionally, apparatus 900 may be coupled to a transfer chamber that allows robotics to transfer semiconductor wafers into and out of apparatus 900 using typical automation.

5 [0179] In some implementations, a system controller 930 (which may include one or more physical or logical controllers) controls some or all of the operations of a process chamber 924. The system controller 930 may include one or more memory devices and one or more processors. In some implementations, the apparatus 900 includes a switching system for controlling flow rates and durations when disclosed implementations are performed. In some implementations, the  
10 apparatus 900 may have a switching time of up to about 500 ms, or up to about 750 ms. Switching time may depend on the flow chemistry, recipe chosen, reactor architecture, and other factors.

[0180] In some implementations, the system controller 930 is part of a system, which may be part of the above-described examples. Such systems can include semiconductor processing equipment, including a processing tool or tools, chamber or chambers, a platform or platforms for  
15 processing, and/or specific processing components (a wafer pedestal, a gas flow system, etc.). These systems may be integrated with electronics for controlling their operation before, during, and after processing of a semiconductor wafer or substrate. The electronics may be integrated into the system controller 930, which may control various components or subparts of the system or systems. The system controller 930, depending on the processing parameters and/or the type of  
20 system, may be programmed to control any of the processes disclosed herein, including the delivery of processing gases, temperature settings (e.g., heating and/or cooling), pressure settings, vacuum settings, power settings, radio frequency (RF) generator settings, RF matching circuit settings, frequency settings, flow rate settings, fluid delivery settings, positional and operation settings, wafer transfers into and out of a tool and other transfer tools and/or load locks connected  
25 to or interfaced with a specific system.

[0181] Broadly speaking, the system controller 930 may be defined as electronics having various integrated circuits, logic, memory, and/or software that receive instructions, issue instructions, control operation, enable cleaning operations, enable endpoint measurements, and the like. The integrated circuits may include chips in the form of firmware that store program instructions,  
30 digital signal processors (DSPs), chips defined as application specific integrated circuits (ASICs), and/or one or more microprocessors, or microcontrollers that execute program instructions (e.g., software). Program instructions may be instructions communicated to the controller in the form of various individual settings (or program files), defining operational parameters for carrying out

a particular process on or for a semiconductor wafer or to a system. The operational parameters may, in some implementations, be part of a recipe defined by process engineers to accomplish one or more processing steps during the fabrication or removal of one or more layers, materials, metals, oxides, silicon, silicon dioxide, surfaces, circuits, and/or dies of a wafer.

5 [0182] The system controller 930, in some implementations, may be a part of or coupled to a computer that is integrated with, coupled to the system, otherwise networked to the system, or a combination thereof. For example, the controller may be in the “cloud” or all or a part of a fab host computer system, which can allow for remote access of the wafer processing. The computer may enable remote access to the system to monitor current progress of fabrication operations,  
10 examine a history of past fabrication operations, examine trends or performance metrics from a plurality of fabrication operations, to change parameters of current processing, to set processing steps to follow a current processing, or to start a new process. In some examples, a remote computer (e.g. a server) can provide process recipes to a system over a network, which may include a local network or the Internet. The remote computer may include a user interface that enables  
15 entry or programming of parameters and/or settings, which are then communicated to the system from the remote computer. In some examples, the system controller 930 receives instructions in the form of data, which specify parameters for each of the processing steps to be performed during one or more operations. It should be understood that the parameters may be specific to the type of process to be performed and the type of tool that the controller is configured to interface with or  
20 control. Thus as described above, the system controller 930 may be distributed, such as by including one or more discrete controllers that are networked together and working towards a common purpose, such as the processes and controls described herein. An example of a distributed controller for such purposes would be one or more integrated circuits on a chamber in communication with one or more integrated circuits located remotely (such as at the platform level  
25 or as part of a remote computer) that combine to control a process on the chamber.

[0183] Without limitation, example systems may include a plasma etch chamber or module, a deposition chamber or module, a spin-rinse chamber or module, a metal plating chamber or module, a clean chamber or module, a bevel edge etch chamber or module, a physical vapor deposition (PVD) chamber or module, a chemical vapor deposition (CVD) chamber or module, an  
30 ALD chamber or module, an ALE chamber or module, an ion implantation chamber or module, a track chamber or module, an EUV lithography chamber (scanner) or module, a dry development chamber or module, and any other semiconductor processing systems that may be associated or used in the fabrication and/or manufacturing of semiconductor wafers.

[0184] As noted above, depending on the process step or steps to be performed by the tool, the controller might communicate with one or more of other tool circuits or modules, other tool components, cluster tools, other tool interfaces, adjacent tools, neighboring tools, tools located throughout a factory, a main computer, another controller, or tools used in material transport that bring containers of wafers to and from tool locations and/or load ports in a semiconductor manufacturing factory.

[0185] EUVL patterning may be conducted using any suitable tool, often referred to as a scanner, for example the TWINSCAN NXE: 3300B® platform supplied by ASML of Veldhoven, NL). The EUVL patterning tool may be a standalone device from which the substrate is moved into and out of for deposition and etching as described herein. Or, as described below, the EUVL patterning tool may be a module on a larger multi-component tool. Figure 10 depicts a semiconductor process cluster tool architecture with vacuum-integrated deposition, EUV patterning and dry development/etch modules that interface with a vacuum transfer module, suitable for implementation of the processes described herein. While the processes may be conducted without such vacuum integrated apparatus, such apparatus may be advantageous in some implementations.

[0186] Figure 10 depicts a semiconductor process cluster tool architecture with vacuum-integrated deposition and patterning modules that interface with a vacuum transfer module, suitable for implementations of processes described herein. The arrangement of transfer modules to “transfer” wafers among multiple storage facilities and processing modules may be referred to as a “cluster tool architecture” system. Deposition and patterning modules are vacuum-integrated, in accordance with the requirements of a particular process. Other modules, such as for etch, may also be included on the cluster.

[0187] A vacuum transport module (VTM) 1038 interfaces with four processing modules 1020a–1020d, which may be individually optimized to perform various fabrication processes. By way of example, processing modules 1020a–1020d may be implemented to perform deposition, evaporation, ELD, dry development, clean, etch, strip, and/or other semiconductor processes. For example, module 1020a may be an ALD reactor that may be operated to perform in a non-plasma, thermal atomic layer depositions as described herein, such as Vector tool, available from Lam Research Corporation, Fremont, CA. And module 1020b may be a PECVD tool, such as the Lam Vector®. It should be understood that the figure is not necessarily drawn to scale.

[0188] Airlocks 1042 and 1046, also known as a loadlocks or transfer modules, interface with the VTM 1038 and a patterning module 1040. For example, as noted above, a suitable patterning

module may be the TWINSCAN NXE: 3300B® platform supplied by ASML of Veldhoven, NL). This tool architecture allows for work pieces, such as semiconductor substrates or wafers, to be transferred under vacuum so as not to react before exposure. Integration of the deposition modules with the lithography tool is facilitated by the fact that EUVL also requires a greatly reduced  
5 pressure given the strong optical absorption of the incident photons by ambient gases such as H<sub>2</sub>O, O<sub>2</sub>, etc.

[0189] As noted above, this integrated architecture is just one possible implementation of a tool for implementation of the described processes. The processes may also be implemented with a more conventional stand-alone EUVL scanner and a deposition reactor, such as a Lam Vector tool,  
10 either stand alone or integrated in a cluster architecture with other tools, such as etch, strip etc. (e.g., Lam Kiyō or Gamma tools), as modules, for example as described with reference to Figure 10 but without the integrated patterning module.

[0190] Airlock 1042 may be an “outgoing” loadlock, referring to the transfer of a substrate out from the VTM 1038 serving a deposition module 1020a to the patterning module 1040, and airlock  
15 1046 may be an “ingoing” loadlock, referring to the transfer of a substrate from the patterning module 1040 back in to the VTM 1038. The ingoing loadlock 1046 may also provide an interface to the exterior of the tool for access and egress of substrates. Each process module has a facet that interfaces the module to VTM 1038. For example, deposition process module 1020a has facet 1036. Inside each facet, sensors, for example, sensors 1–18 as shown, are used to detect the passing  
20 of wafer 1026 when moved between respective stations. Patterning module 1040 and airlocks 1042 and 1046 may be similarly equipped with additional facets and sensors, not shown.

[0191] Main VTM robot 1022 transfers wafer 1026 between modules, including airlocks 1042 and 1046. In one implementation, robot 1022 has one arm, and in another implementation, robot 1022 has two arms, where each arm has an end effector 1024 to pick wafers such as wafer 1026  
25 for transport. Front-end robot 1044, in is used to transfer wafers 1026 from outgoing airlock 1042 into the patterning module 1040, from the patterning module 1040 into ingoing airlock 1046. Front-end robot 1044 may also transport wafers 1026 between the ingoing loadlock and the exterior of the tool for access and egress of substrates. Because ingoing airlock module 1046 has the ability to match the environment between atmospheric and vacuum, the wafer 1026 is able to  
30 move between the two pressure environments without being damaged.

[0192] It should be noted that an EUVL tool typically operates at a higher vacuum than a deposition tool. If this is the case, it is desirable to increase the vacuum environment of the

substrate during the transfer between the deposition to the EUVL tool to allow the substrate to degas prior to entry into the patterning tool. Outgoing airlock 1042 may provide this function by holding the transferred wafers at a lower pressure, no higher than the pressure in the patterning module 1040, for a period of time and exhausting any off-gassing, so that the optics of the patterning module 1040 are not contaminated by off-gassing from the substrate. A suitable pressure for the outgoing, off-gassing airlock is no more than 1E-8 Torr.

**[0193]** In some implementations, a system controller 1050 (which may include one or more physical or logical controllers) controls some or all of the operations of the cluster tool and/or its separate modules. It should be noted that the controller can be local to the cluster architecture, or can be located external to the cluster architecture in the manufacturing floor, or in a remote location and connected to the cluster architecture via a network. The system controller 1050 may include one or more memory devices and one or more processors. The processor may include a central processing unit (CPU) or computer, analog and/or digital input/output connections, stepper motor controller boards, and other like components. Instructions for implementing appropriate control operations are executed on the processor. These instructions may be stored on the memory devices associated with the controller or they may be provided over a network. In certain implementations, the system controller executes system control software.

**[0194]** The system control software may include instructions for controlling the timing of application and/or magnitude of any aspect of tool or module operation. System control software may be configured in any suitable way. For example, various process tool component subroutines or control objects may be written to control operations of the process tool components necessary to carry out various process tool processes. System control software may be coded in any suitable compute readable programming language. In some implementations, system control software includes input/output control (IOC) sequencing instructions for controlling the various parameters described above. For example, each phase of a semiconductor fabrication process may include one or more instructions for execution by the system controller. The instructions for setting process conditions for condensation, deposition, evaporation, patterning and/or etching phase may be included in a corresponding recipe phase, for example.

**[0195]** In various implementations, an apparatus for forming a negative pattern mask is provided. The apparatus may include a processing chamber for patterning, deposition and etch, and a controller including instructions for forming a negative pattern mask. The instructions may include code for, in the processing chamber, patterning a feature in a chemically amplified (CAR) resist on a semiconductor substrate by EUV exposure to expose a surface of the substrate,

developing the photopatterned resist, and etching the underlying layer or layer stack using the patterned resist as a mask. Development may be performed using an organic vapor such as an organic acid.

[0196] It should be noted that the computer controlling the wafer movement can be local to the cluster architecture, or can be located external to the cluster architecture in the manufacturing floor, or in a remote location and connected to the cluster architecture via a network. A controller as described above with respect to any of Figures 7, 8, or 9 may be implemented with the tool in Figure 10.

[0197] Figure 11A shows an example of a deposition chamber for vapor-based deposition of metal-containing resist material according to some implementations. As can be seen, an apparatus 1100 is depicted that has a process chamber 1102 that includes a lid 1108. The process chamber 1102 may include a wafer transfer passage 1104 through one of the walls of the process chamber 1102 that is sized to allow a substrate 1122 to be passed therethrough and into the interior of the process chamber 1102, where the substrate 1122 may be placed on a wafer support 1124. The wafer transfer passage 1104 may have a gate valve 1106 or similar door mechanism that may be operated to seal or unseal the wafer transfer passage 1104, thereby allowing the environment within the process chamber 1102 to be isolated from the environment on the other side of the gate valve 1106. For example, the process chamber 1102 may be provided substrates 1122 via a wafer handling robot that is located in an adjoining transfer chamber. Such a transfer chamber may, for example, have multiple process chambers 1102 arranged around its periphery, with each such process chamber 1102 connected with the transfer chamber via a corresponding gate valve 1106.

[0198] The wafer support 1124 may, for example, include an electrostatic chuck (ESC) 1126, which may be used to provide a wafer support surface for supporting the substrate 1122. The ESC 1126 may include, for example, a base plate 1134 that is bonded to a top plate 1128 that is placed atop the base plate 1134. The top plate 1128 may, for example, be made of a ceramic material and may have embedded within it several other components. In the depicted example, the top plate 1128 has two separate electrical systems embedded within it. One such system is an electrostatic clamping electrode system, which may have one or more clamping electrodes 1132 that may be used to generate an electric charge within the substrate 1122 that causes the substrate 1122 to be drawn against the wafer support surface of the top plate 1128. In the implementation of Figure 11A, there are two clamping electrodes 1132 that provide a bi-polar electrostatic clamping system, although some implementations may use only a single clamping electrode 1132 to provide a mono-polar electrostatic clamping system.

[0199] The other system is a thermal control system that may be used to control the temperature of the substrate 1122 during processing conditions. In Figure 11A, the thermal control system is a multi-zone thermal control system featuring four annular resistance heater traces 1130a, 1130b, 1130c, and 1130d that are concentric with one another and positioned beneath the clamping electrodes 1132. The center resistance heater traces 1130a may, in some implementations, fill a generally circular area, and each resistance heater trace 1130a/b/c/d may follow a generally serpentine or otherwise meandering path within a corresponding annular region. Each resistance heater trace 1130a/b/c/d may be individually controlled to provide a variety of radial heating profiles in the top plate 1128; such a four-zone heating system may, for example, be controlled to maintain the substrate 1122 so as to have a temperature uniformity of  $\pm 0.5^{\circ}\text{C}$  in some cases. While the apparatus 1100 of Figure 11A features a four-zone heating system in the ESC 1126, other implementations may use single-zone or multi-zone heating systems having more or fewer than four zones.

[0200] In some implementations, of, for example, temperature control mechanisms discussed above, heat pumps may be used instead of resistance heating traces. For example, in some implementations, the resistance heater traces may be replaced by, or augmented by, Peltier junctions or other, similar devices that may be controlled to “pump” heat from one side thereof to another. Such mechanisms may be used, for example, to draw heat from the top plate 1128 (and thus the substrate 1122) and direct it into the base plate 1134 and the heat exchange passages 1136, thereby allowing the substrate 1122 to be cooled more rapidly and more effectively, if desired.

[0201] The ESC 1126 may also include, for example, a base plate 1134 that may be used to provide structural support to the underside of the top plate 1128 and which may also act as a heat dispersion system. For example, the base plate 1134 may include one or more heat exchange passages 1136 that are arranged in a generally distributed fashion throughout the base plate 1134, e.g., the heat exchange passages 1136 may follow a serpentine, circular switchback, or spiral pattern around the center of the base plate 1134. A heat exchange medium, e.g., water or inert fluorinated liquid, may be circulated through the heat exchange passages 1136 during use. The flow rate and temperature of the heat exchange medium may be externally controlled so as to result in a particular heating or cooling behavior in the base plate 1134.

[0202] The ESC 1126 may, for example, be supported by a wafer support housing 1142 that is connected with, and supported by, a wafer support column 1144. The wafer support column 1144 may, for example, have a routing passage 1148 other pass-throughs for routing cabling, fluid flow conduits, and other equipment to the underside of the base plate 1134 and/or the top plate 1128.

For example, while not shown in Figure 11A, cabling for providing electrical power to the resistance heater traces 1130a/b/c/d may be routed through the routing passage 1148, as may cabling for providing electrical power to the clamping electrodes 1132. Other cables, e.g., cables for temperature sensors, may also be routed through the routing passage 1148 to locations in the interior of the wafer support 1124. In implementations with a temperature-controllable base plate 1134, conduits for conveying heat exchange medium to and from the base plate 1134 may also be routed through the routing passage 1148. To avoid undue clutter, such cables and conduits are not depicted in Figure 11A, but it is to be understood that they would, nonetheless, be present.

[0203] The apparatus 1100 of Figure 11A also includes a wafer support z-actuator 1146 that may provide movable support to the wafer support column 1144. The wafer support z-actuator 1146 may be actuated to cause the wafer support column 1144, and the wafer support 1124 supported thereby, to move up or down vertically, e.g., by up to several inches, within a reaction space 1120 of the process chamber 1102. In doing so, a gap distance X between the substrate 1122 and the underside of the showerhead 1110 may be tuned depending on various process conditions.

[0204] The wafer support 1124 may also include, in some implementations, one or more edge rings that may be used to control and/or fine-tune various process conditions. In Figure 11A, an upper edge ring 1138 is provided that lies on top of, for example, lower edge rings 1140a and 1140b, which, in turn, are supported by the wafer support housing 1142 and a third lower edge ring 1140c. The upper edge ring 1138 may, for example, be generally subjected to the same processing environment as the substrate 1122, whereas the lower edge rings 1140a/b/c may generally be shielded from the processing environment. Due to the increased exposure of the upper edge ring 1138, the upper edge ring 1138 may have a limited lifespan and may require more frequent replacement or cleaning as compared with the lower edge rings 1140a/b/c.

[0205] The apparatus 1100 may also include a system for removing process gases from the process chamber 1102 during and after processing concludes. For example, the process chamber 1102 may include an annular plenum 1156 that encircles the wafer support column 1144. The annular plenum 1156 may, in turn, be fluidically connected with a vacuum foreline 1152 that may be connected with a vacuum pump, e.g., such as may be located beneath a subfloor below the apparatus 1100. A regulator valve 1154 may be provided in between the vacuum foreline 1152 and the process chamber 1102 and actuated to control the flow into the vacuum foreline 1152. In some implementations, a baffle 1150, e.g., an annular plate or other structure that may serve to make the flow into the annular plenum 1156 more evenly distributed about the circumference of

the wafer support column 1144, may be provided to reduce the chances of flow non-uniformities developing in reactants flowed across the substrate 1122.

[0206] The showerhead 1110, as shown, is a dual-plenum showerhead 1110 and includes a first plenum 1112 that is provided process gas via a first inlet 1116 and a second plenum 1114 that is provided process gas via a second inlet 1118. Generally, two plenums can be employed to maintain separation between the precursor(s) and the counter-reactant(s) prior to release of the precursor and the counter-reactant. The showerhead 1110 may, in some implementations, have more than two plenums. In some instances, a single plenum is used to deliver the precursor(s) into the reaction space 1120 of the processing chamber 1102. Each plenum may have a corresponding set of gas distribution ports that fluidically connect the respective plenum with the reaction space 1120 through the faceplate of the showerhead 1110 (the faceplate being the portion of the showerhead 1110 that is interposed between the lowermost plenum and the reaction space 1120).

[0207] The first inlet 1116 and the second inlet 1118 of the showerhead 1110 may be provided processing gases via a gas supply system, which may be configured to provide one or more precursor(s) and/or counter-reactant(s), as discussed herein. The depicted apparatus 1100 is configured to provide multiple precursors and multiple counter-reactants. For example, a first valve manifold 1168a may be configured to provide precursor(s) to the first inlet 1116, while a second valve manifold 1168b may be configured to provide other precursor(s) or other counter-reactants to the second inlet 1118.

[0208] A first valve manifold 1168a may be configured to provide one or more precursor(s) to the first inlet 1116, while a second valve manifold 1168b may be configured to provide other precursor(s) or other reactant to the second inlet 1118. In this example, the first valve manifold 1168a, for example, includes multiple valves A1–A5. Valve A2 may, for example, be a three-way valve that has one port fluidically connected with a first vaporizer 1172a, another port fluidically connected with a bypass line 1170a, and a third port fluidically connected with a port on another 3-way valve A3. Similarly, valve A4 may be another three-way valve that has one port fluidically connected with a second vaporizer 1172b, another port fluidically connected with the bypass line 1170a, and a third port fluidically connected with a port on another 3-way valve A5. One of the other ports on valve A5 may be fluidically connected with the first inlet 1116 while the remaining port on valve A5 may be fluidically connected with one of the remaining ports on the valve A3. The remaining port on the valve A3 may, in turn, be fluidically connected with the valve A1 which may be fluidically interposed between the valve A3 and a purge gas source 1174, e.g., nitrogen,

argon, or other suitably inert gas (with respect to precursor(s) and/or counter-reactant(s)). In some implementations, only the first valve manifold is employed.

[0209] For the purposes of this disclosure, the term “fluidically connected” is used with respect to volumes, plenums, holes, etc., that may be connected with one another in order to form a fluidic connection, similar to how the term “electrically connected” is used with respect to components that are connected together to form an electric connection. The term “fluidically interposed,” if used, may be used to refer to a component, volume, plenum, or hole that is fluidically connected with at least two other components, volumes, plenums, or holes such that fluid flowing from one of those other components, volumes, plenums, or holes to the other or another of those components, volumes, plenums, or holes would first flow through the “fluidically interposed” component before reaching that other or another of those components, volumes, plenums, or holes. For example, if a pump is fluidically interposed between a reservoir and an outlet, fluid that flowed from the reservoir to the outlet would first flow through the pump before reaching the outlet.

[0210] The first valve manifold 1168a may, for example, be controllable to cause vapors from one or both of the vaporizers 1172a and 1172b to be flowed either to the process chamber 1102 or through the first bypass line 1170a and into the vacuum foreline 1152. The first valve manifold 1168a may also be controllable to cause a purge gas to be flowed from the purge gas source 1174 and into the first inlet 1116.

[0211] For example, to flow vapor from the first vaporizer 1172a into the reaction space 1120, the valve A2 may be actuated to cause the vapor from the first vaporizer 1172a to first flow into the first bypass line 1170a. This flow may be maintained for a period of time sufficient to allow the flow of the vapor to reach steady state flow conditions. After sufficient time has passed (or after a flow meter, if used, indicates that the flow rate is stable), valves A2, A3, and A5 may be actuated to cause the vapor flow from the first vaporizer 1172a to be directed to the first inlet. Similar operations with valves A4 and A5 may be performed to deliver vapor from the second vaporizer 1172b to the first inlet 1116. In some instances, it may be desirable to purge one of the vapors from the first plenum 1112 by actuating the valves A1, A3, and A5 so as to cause the purge gas from the purge gas source 1174 to be flowed into the first inlet 1116. In some additional implementations, it may be desirable to simultaneously flow vapor from one of the vaporizers 1172a or 1172b in tandem with flowing gas from the purge gas into the first inlet 1116. Such implementations may be used to dilute the concentration of the reactant(s) contained in such vapor(s).

[0212] It will be appreciated that the second valve manifold 1168b may be controlled in a similar manner, e.g., by controlling valves B1–B5, to provide vapors from vaporizers 1172c and 1172d to the second inlet 1118 or to the second bypass line 1170b. It will be further appreciated that different manifold arrangements may be utilized as well, including a single unitary manifold that includes valves for controlling flow of the precursor(s), counter-reactant(s), or other reactants to the first inlet 1116 and the second inlet 1118.

[0213] As mentioned earlier, some apparatuses 1100 may feature a lesser number of vapor sources, e.g., only two vaporizers 1172, in which case the valve manifold(s) 1168 may be modified to have a lesser number of valves, e.g., only valves A1–A3.]

[0214] As discussed above, apparatuses such as apparatus 1100, which may be used to provide for dry deposition of films, may be configured to maintain particular temperature profiles within the process chamber 1102. In particular, such apparatuses 1100 may be configured to maintain the substrate 1122 at a lower temperature, e.g., at least 25°C to 50°C lower, than most of the equipment of the apparatus 1100 that comes into direct contact with the precursor(s) and/or counter-reactant(s). Additionally, the temperature of the equipment of the apparatus 1100 that comes into direct contact with the precursor(s) and/or counter-reactant(s) may be kept to an elevated level that is sufficiently high that condensation of the vaporized reactants on the surfaces of such equipment is discouraged. At the same time, the substrate 1122 temperature may be controlled to a level that promotes condensation, or at least deposition, of the reactants on the substrate 1122.

[0215] To provide for such temperature control, various heating systems may be included in the apparatus 1100. For example, the process chamber 1102 may have receptacles for receiving cartridge heaters 1158, e.g., for a process chamber 1102 that has a generally cylindrical interior volume but a square or rectangular external shape, vertical holes for receiving cartridge heaters 1158 may be bored into the four corners of the chamber 1102 housing. In some implementations, the showerhead 1110 may be covered with heater blankets 1160, which may be used to apply heat across the exposed upper surface of the showerhead 1110 to keep the showerhead temperature elevated. It may also be beneficial to heat various gas lines that are used to conduct the vaporized reactants from the vaporizers 1172 to the showerhead 1110. For example, resistive heater tape may be wound around such gas lines and used to heat them to an elevated temperature. As shown in Figure 11A, all of the gas lines that potentially have precursor(s) and/or counter-reactant(s) flowing through them are shown as being heated, including the bypass lines 1170. The only exceptions are the gas lines from the valve manifolds 1168 to the first inlet 1116 and the second

inlet 1118, which may be quite short and may be indirectly heated by the showerhead 1110. Of course, even these gas lines may be actively heated, if desired. In some implementations, heaters may be provided proximate to the gate valve 1106 to provide heat to the gate valve as well.

5 [0216] The various operational systems of the apparatus 1100 may be controlled by a controller 1184, which may include one or more processors 1186 and one or more memory devices 1188 that are operatively connected with each other and that are communicatively connected with various systems and subsystems of the apparatus 1100 so as to provide for control functionality for those systems. For example, the controller 1184 may be configured to control the valves A1–A5 and B1–B5, the various heaters 1158, 1160, the vaporizers 1172, the regulator valve 1154, the gate valve 1106, the wafer support z-actuator, and so forth.

10 [0217] Another feature that the apparatus 1100 may include is shown in Figure 11B, which depicts a close-up side cross-sectional and plan views of a portion of the substrate 1122, top plate 1128, and upper edge ring 1138 of Figure 11A. As can be seen, in some implementations, the substrate 1122 may be elevated off of most of the top plate 1128 by a plurality of small mesas 15 1176, which may be shallow bosses that protrude from the nominal upper surface of the top plate 1128 by a small distance so as to provide for a backside gap 1178 between the underside of the substrate 1122 and the majority of the top plate 1128. A circumferential wall feature 1177 may be provided at the periphery of the top plate 1128. The circumferential wall feature 1177 may extend around the entire perimeter of the top plate 1128 and be of nominally the same height as the mesas 20 1176. During processing operations, a generally inert gas, such as helium, may be flowed into the backside gap 1178 via one or more gas ports 1182. This gas may then flow radially outward before encountering the circumferential wall feature 1177, which way then restrict such radially outward flow and cause a higher-pressure region of the gas to be trapped between the substrate 1122 and the top plate 1128. The inert gas that leaks past the circumferential wall 1177 may eventually flow 25 out through a radial gap 1180 between the outer edge of the substrate 1122 and a portion of the upper edge ring 1138. Such gas may serve to protect the underside of the substrate from undesirably being affected by the processing operations being performed by acting to prevent the gases released by the showerhead 1110 from reaching the underside of the substrate 1122. At the same time, the gas released into the backside gap 1178 region may also act to increase thermal 30 coupling between the substrate 1122 and the top plate 1128, thereby allowing the top plate 1128 to more effectively heat or cool the substrate 1122. Due to the higher pressure provided by the circumferential wall, the gas that is within the backside gap 1178 region may also be at a higher density than gas in the remainder of the chamber, and may thus provide more effective thermal coupling between the substrate 1122 and the top plate 1128.

[0218] The controller 1184 may be configured, e.g., via execution of computer-executable instructions, to cause the apparatus 1100 to perform various operations consistent with the disclosure provided above.

[0219] Once the metal-containing resist film has been deposited on the substrate 1122, the substrate 1122 may, as noted above, be transferred to one or more subsequent process chambers or tool for additional operations (e.g., any described herein). Further deposition apparatuses are described in International Patent Application No. PCT/US2020/038968, filed June 22, 2020, titled “APPARATUS FOR PHOTORESIST DRY DEPOSITION,” which is herein incorporated by reference in its entirety.

10

### Conclusion

[0220] Process and apparatus for dry development of metal and/or metal oxide photoresists, for example to form a patterning mask in the context of EUV patterning is disclosed.

[0221] It is understood that the examples and implementations described herein are for illustrative purposes only and that various modifications or changes in light thereof will be suggested to persons skilled in the art. Although various details have been omitted for clarity’s sake, various design alternatives may be implemented. Therefore, the present examples are to be considered as illustrative and not restrictive, and the disclosure is not to be limited to the details given herein, but may be modified within the scope of the disclosure.

20

**CLAIMS**

1. A method comprising:  
providing in a process chamber a photopatterned metal-containing resist on a surface of a  
5 semiconductor substrate; and  
dry developing the photopatterned metal-containing resist by selectively removing a  
portion of the photopatterned metal-containing resist by exposure to a development chemistry  
comprising an organic vapor to form a resist mask.
2. The method of claim 1, wherein the organic vapor comprises a carboxylic acid.
- 10 3. The method of claim 2, wherein the organic vapor comprises trifluoroacetic acid.
4. The method of claim 1, wherein the organic vapor comprises trifluoroacetic acid  
anhydride, acetic acid anhydride, trichloroacetic acid, mono-fluoroacetic acid, di-fluoroacetic  
acid, chloro-difluoro-acetic acid, thioacetic acid, or thioglycolic acid.
5. The method of claim 1, wherein the organic vapor comprises hexafluoro-acetylacetone.
- 15 6. The method of any one of claims 1-5, wherein the development chemistry comprises a  
mixture in a vapor phase of a halogenated carboxylic acid and a hydrogen halide.
7. The method of any one of claims 1-5, wherein dry developing the photopatterned metal-  
containing resist comprises reacting the organic vapor with the photopatterned metal-containing  
resist to form a volatile compound at a temperature less than about 200°C.
- 20 8. The method of any one of claims 1-5, wherein dry developing the photopatterned metal-  
containing resist comprises exposure to at least the organic vapor in a plasma-free thermal  
process.
9. The method of any one of claims 1-5, wherein the photopatterned metal-containing resist  
is a photopatterned metal-containing EUV resist, wherein the photopatterned metal-containing  
25 EUV resist is an organo-metal oxide or organo-metal-containing film.
10. The method of any one of claims 1-5, wherein dry developing the photopatterned metal-  
containing resist comprises selectively removing an EUV-unexposed portion of the

photopatterned metal-containing resist relative to an EUV-exposed portion with the development chemistry to form the resist mask.

11. A method comprising:

depositing in a process chamber, a metal-containing resist material on a surface of a  
5 semiconductor substrate, wherein a portion of the metal-containing resist material forms a  
residue on one or more surfaces of the process chamber; and

introducing a dry etchant comprising an organic vapor into the process chamber, wherein  
the dry etchant at least partially removes the residue on the one or more surfaces of the process  
chamber.

10 12. The method of claim 11, wherein the organic vapor comprises a carboxylic acid.

13. The method of claim 12, wherein the organic vapor comprises trifluoroacetic acid.

14. The method of claim 11, wherein the organic vapor comprises trifluoroacetic acid  
anhydride, acetic acid anhydride, trichloroacetic acid, mono-fluoroacetic acid, di-fluoroacetic  
acid, chloro-difluoro-acetic acid, thioacetic acid, or thioglycolic acid.

15 15. The method of claim 11, wherein the organic vapor comprises hexafluoro-acetylacetone.

16. The method of any one of claims 11-15, wherein the dry etchant comprises a mixture in a  
vapor phase of a halogenated carboxylic acid and a hydrogen halide.

17. The method of any one of claims 11-15, wherein at least partial removal of the residue  
comprises reacting the organic vapor with the metal-containing resist material to form a volatile  
20 compound at a temperature less than about 200°C.

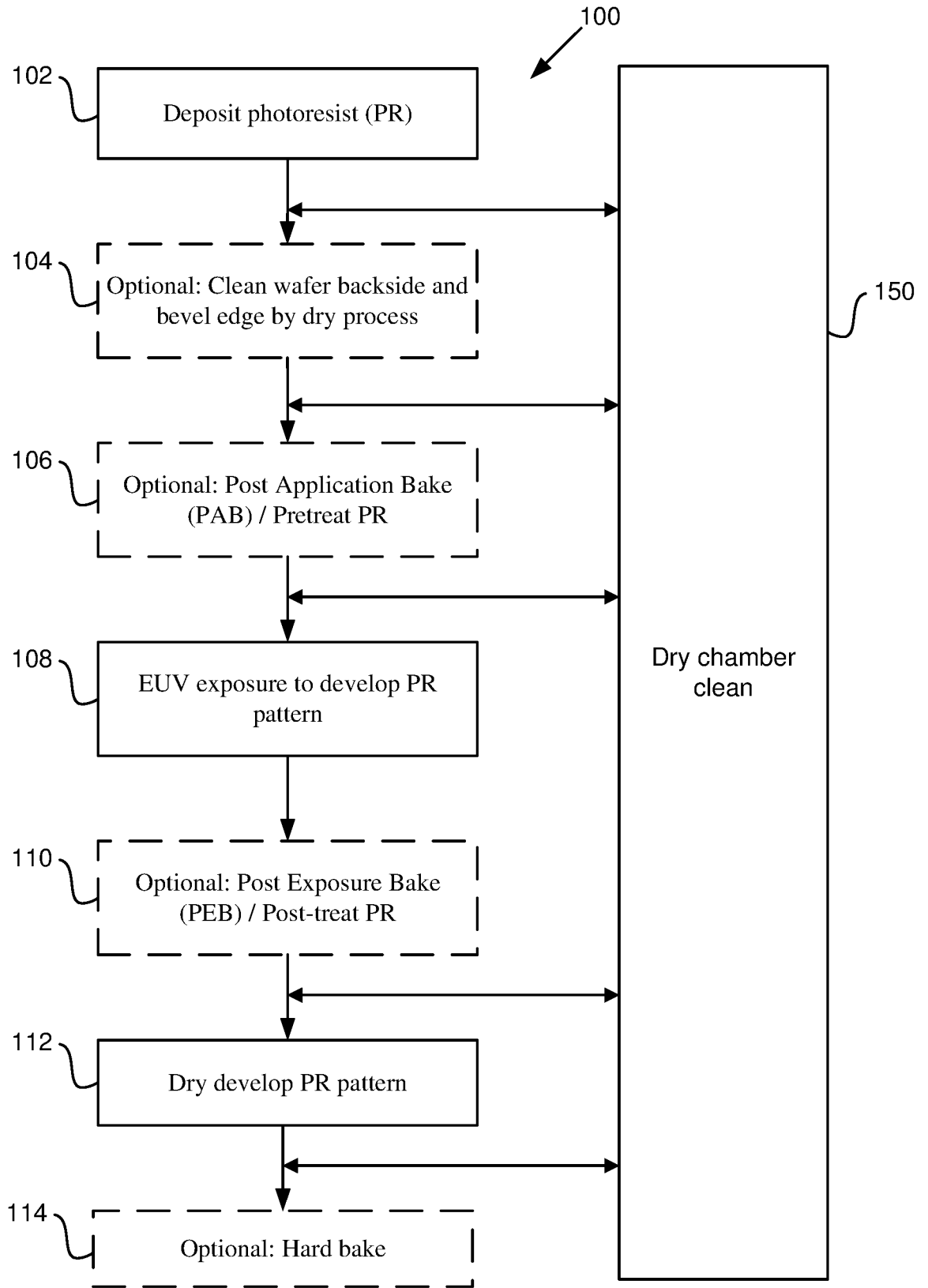
18. The method of any one of claims 11-15, wherein at least partial removal of the residue  
comprises exposure to at least the organic vapor in a plasma-free thermal process.

19. The method of any one of claims 11-15, wherein the metal-containing resist material is  
an organo-metal oxide or organo-metal-containing film.

25 20. The method of any one of claims 11-15, further comprising:

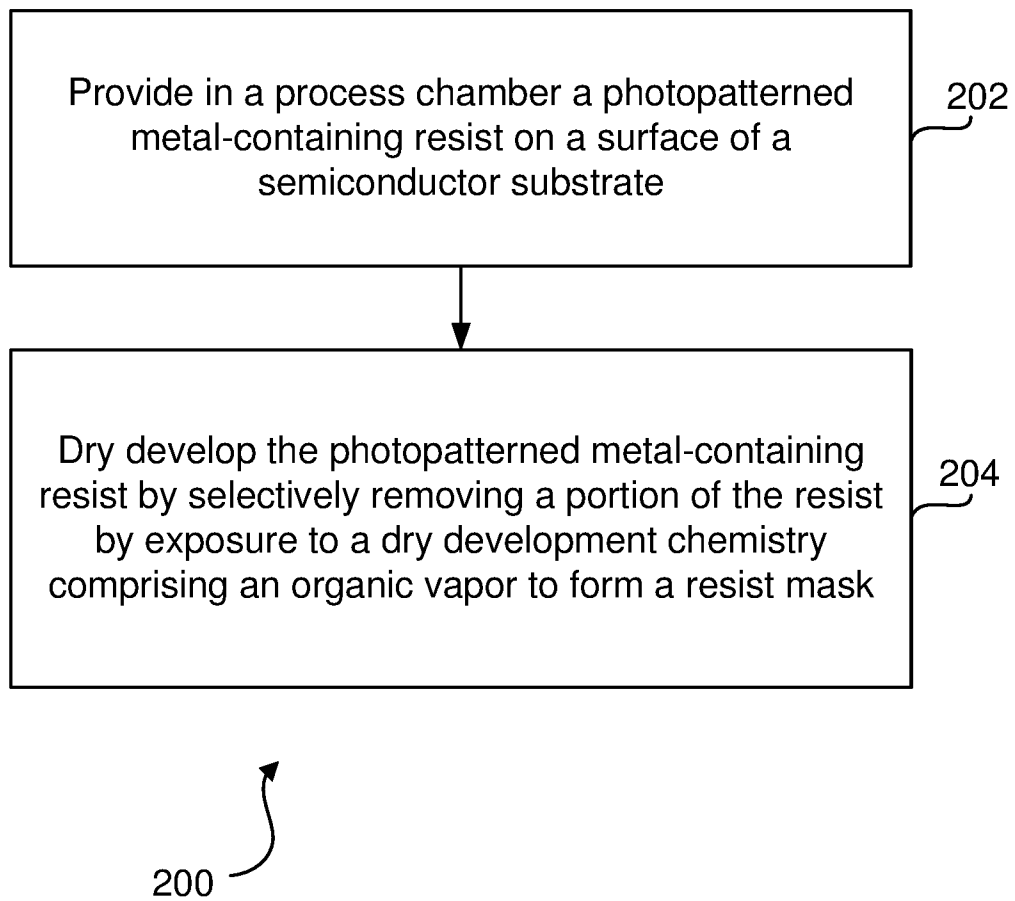
purging the process chamber after introducing the dry etchant to remove residual dry  
etchant from the process chamber; and

conditioning the one or more surfaces of the process chamber by forming a protective coating of the metal-containing resist material on the one or more surfaces of the process chamber.

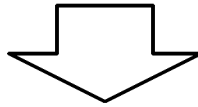
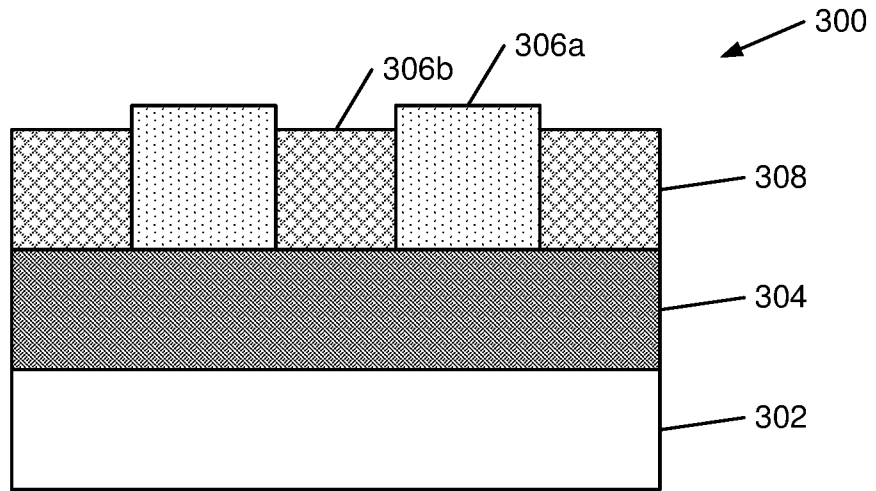


**FIG. 1**

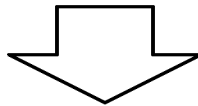
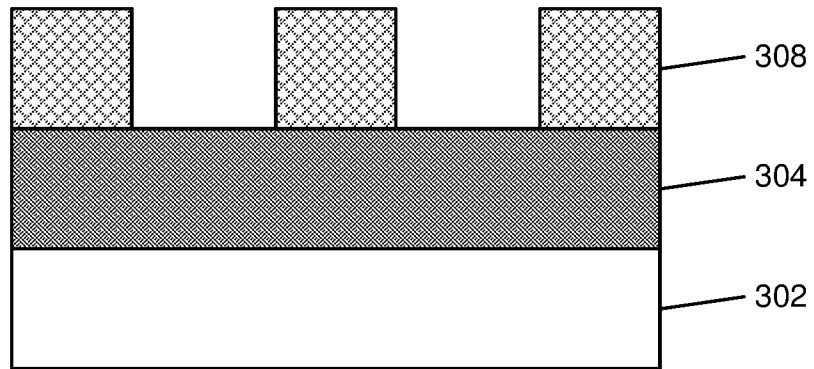
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**FIG. 2**

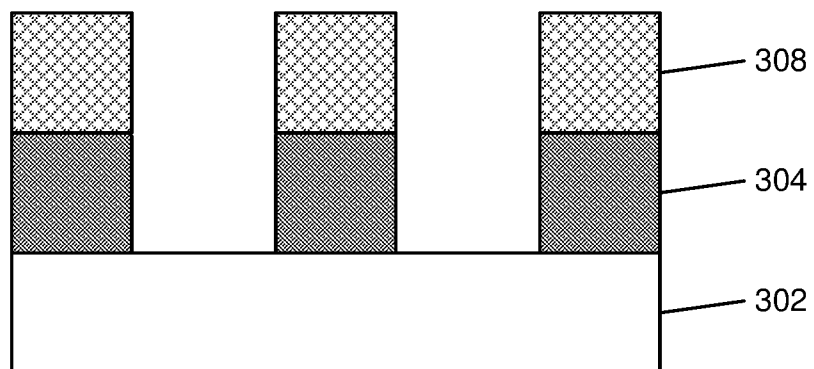
**FIG. 3A**

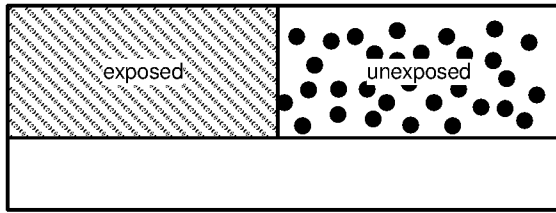


**FIG. 3B**

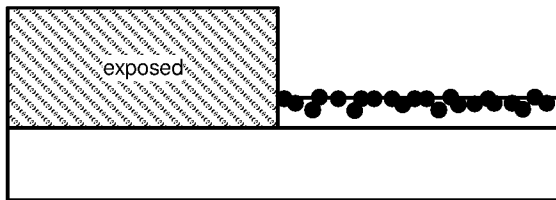


**FIG. 3C**

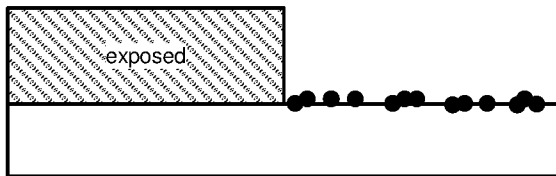




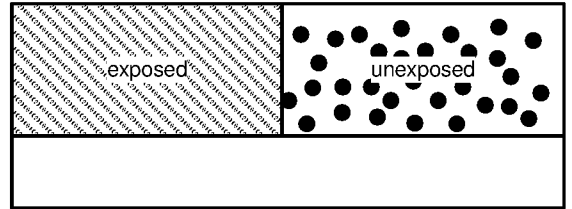
↓  
Dry  
development



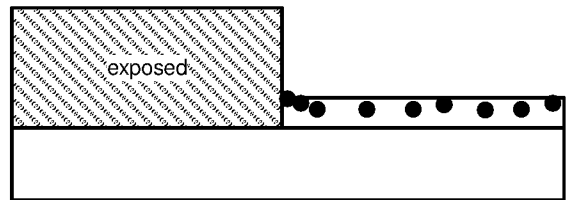
↓  
Dry  
development



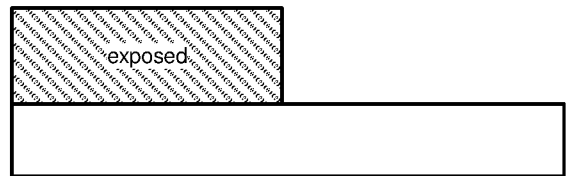
**FIG. 4A**



↓  
Dry  
development

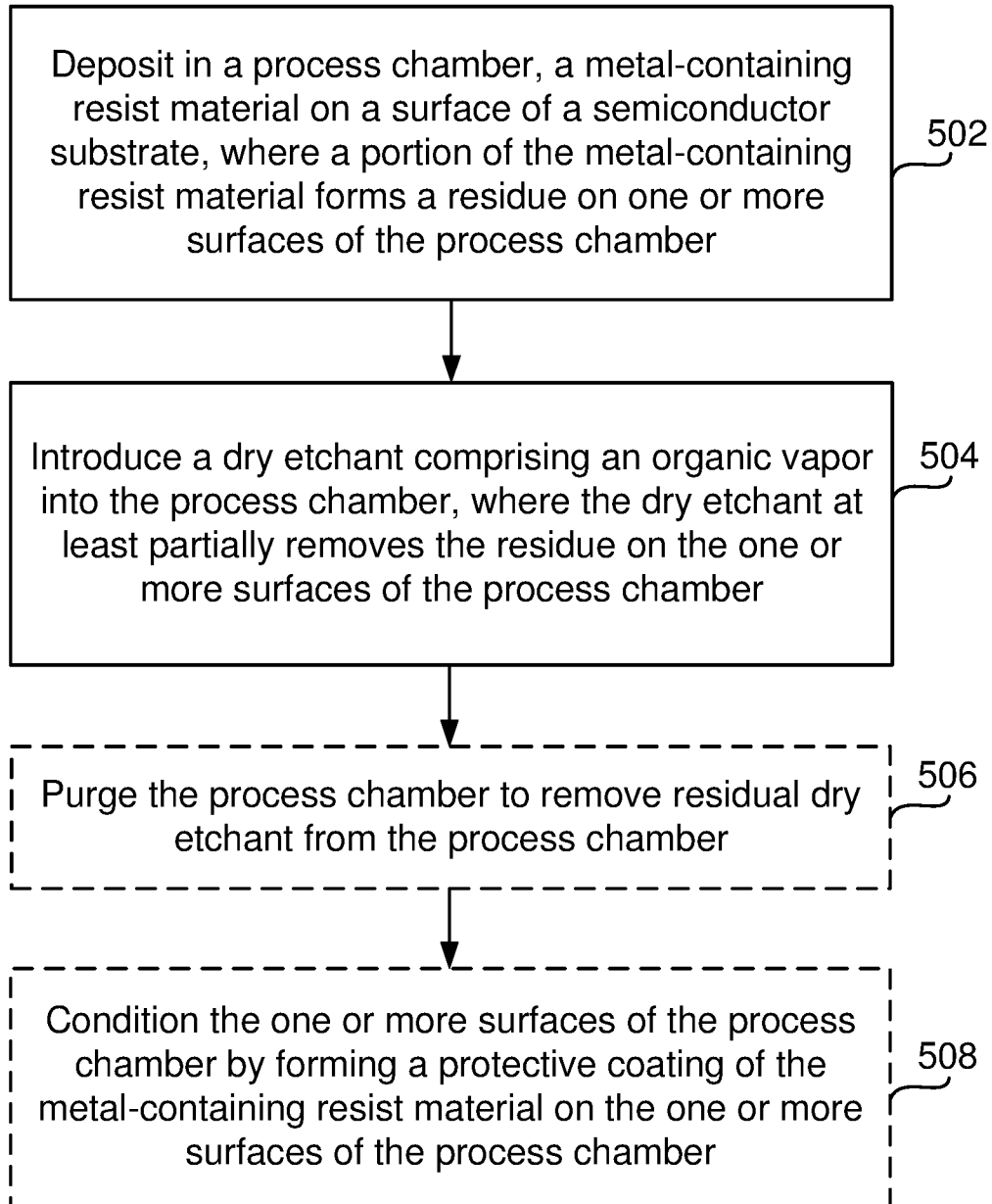


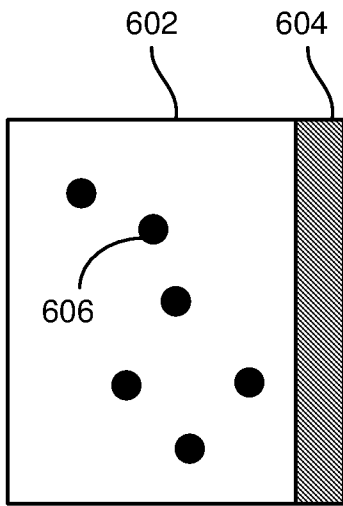
↓  
Helium  
desorption



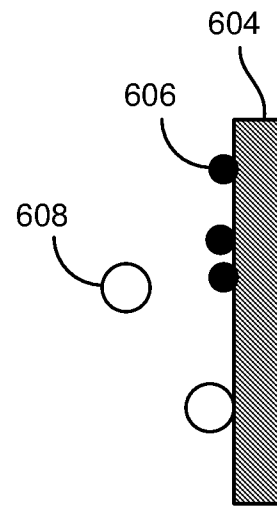
**FIG. 4B**

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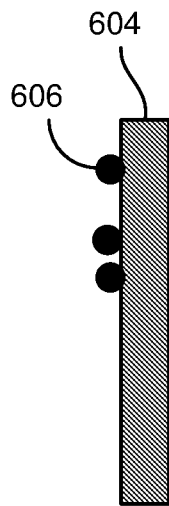
**FIG. 5**



**FIG. 6A**



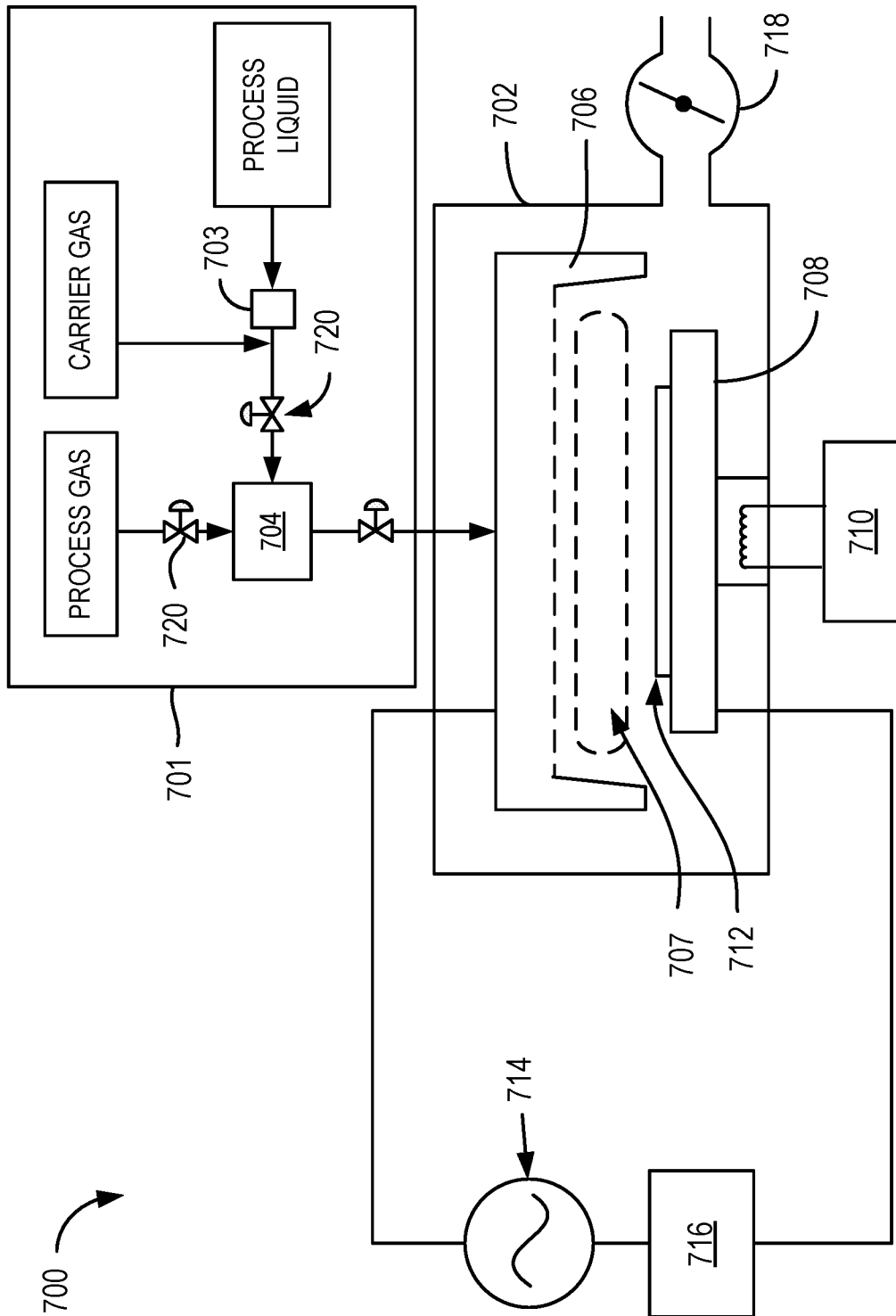
**FIG. 6B**



**FIG. 6C**

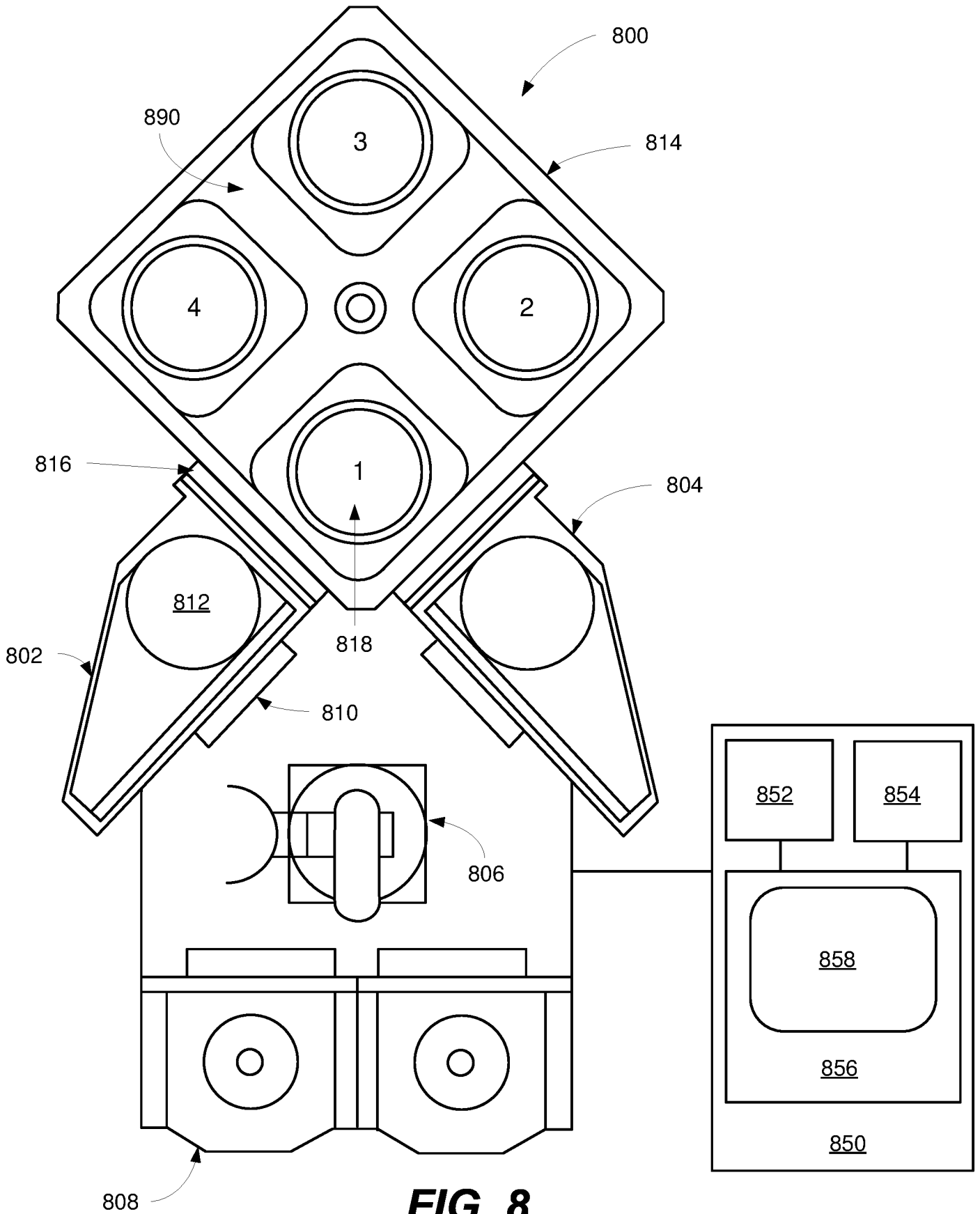


**FIG. 6D**

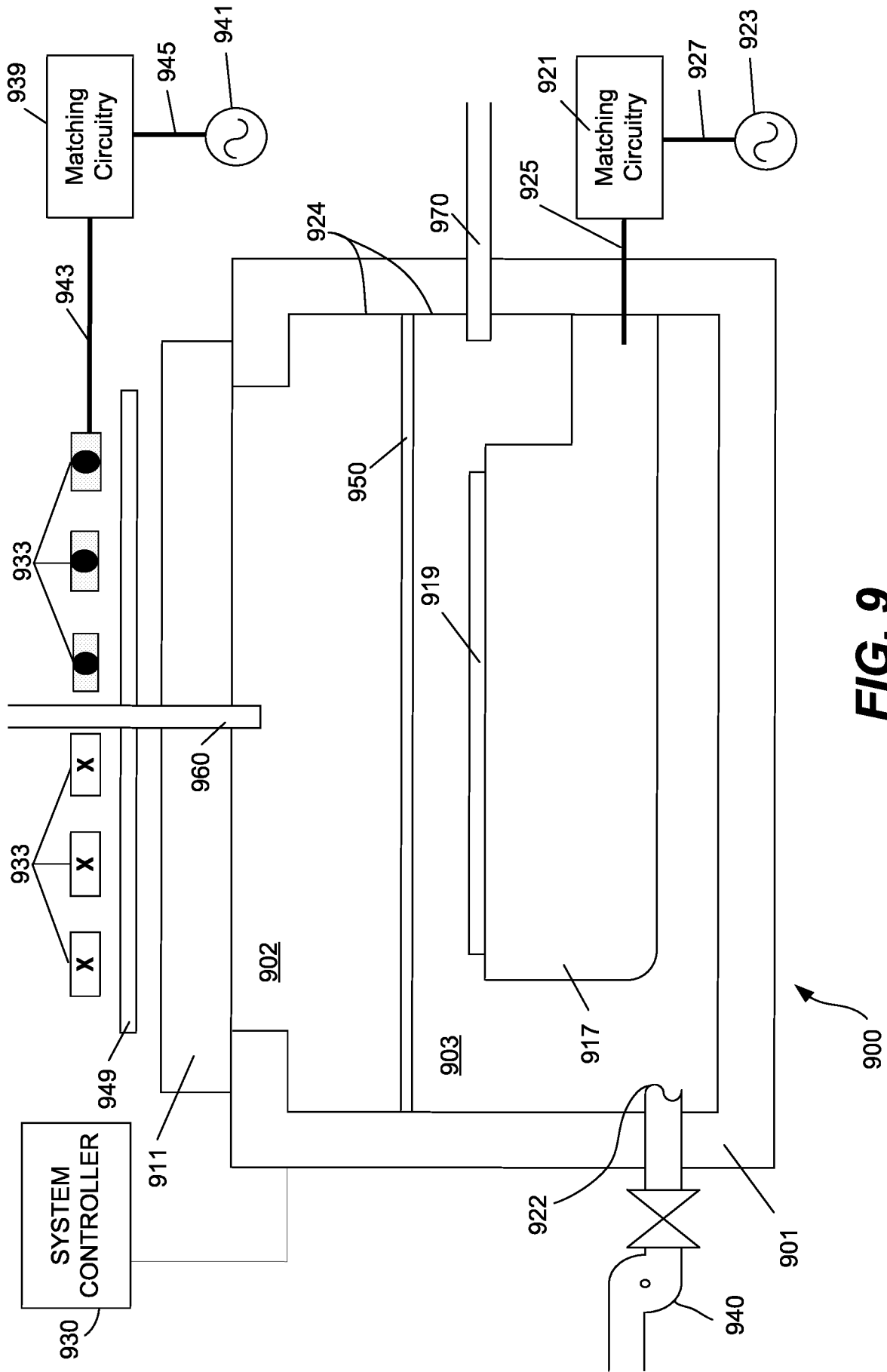


**FIG. 7**

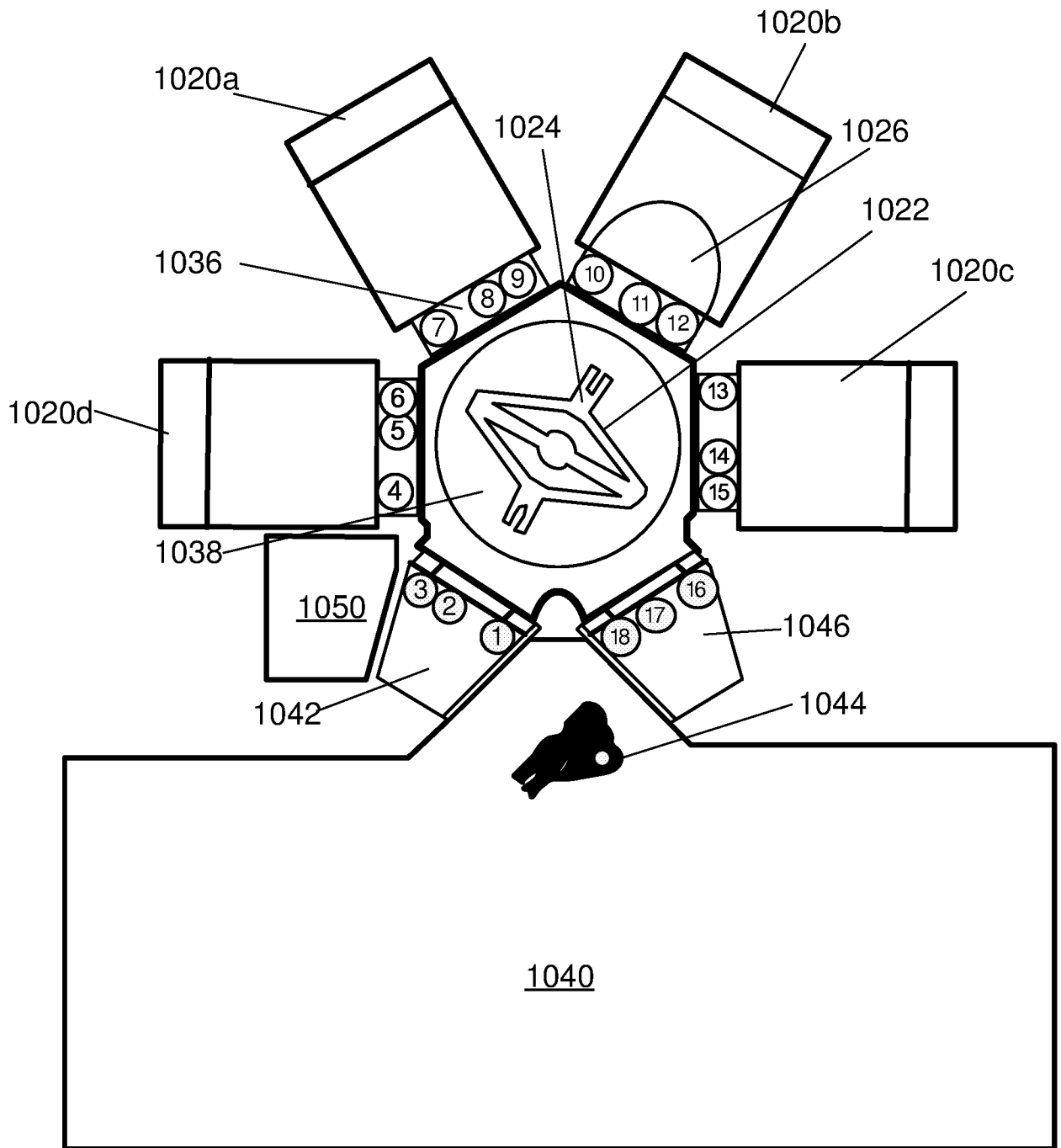
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**FIG. 8**



**FIG. 9**



**FIG. 10**

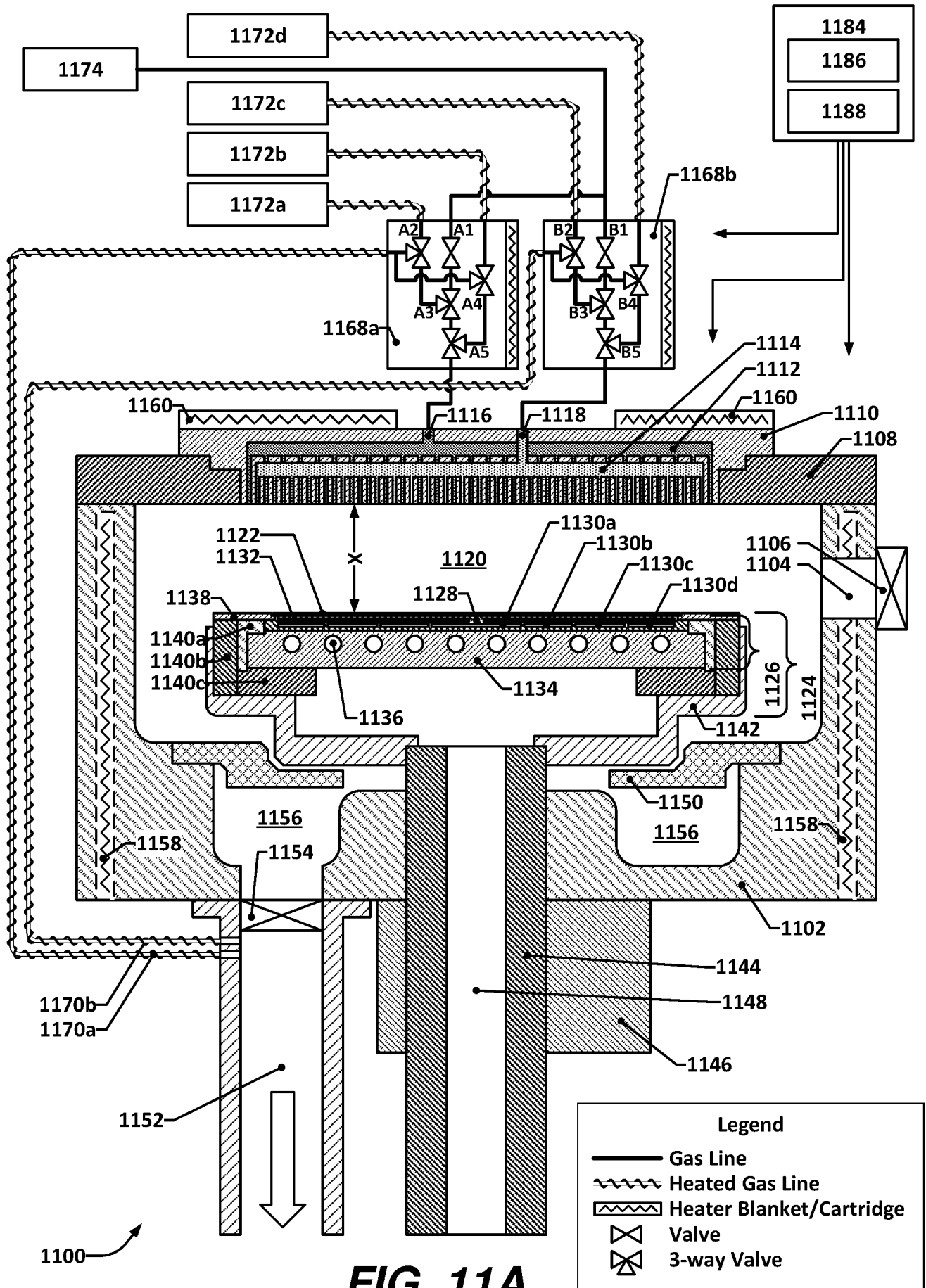


FIG. 11A

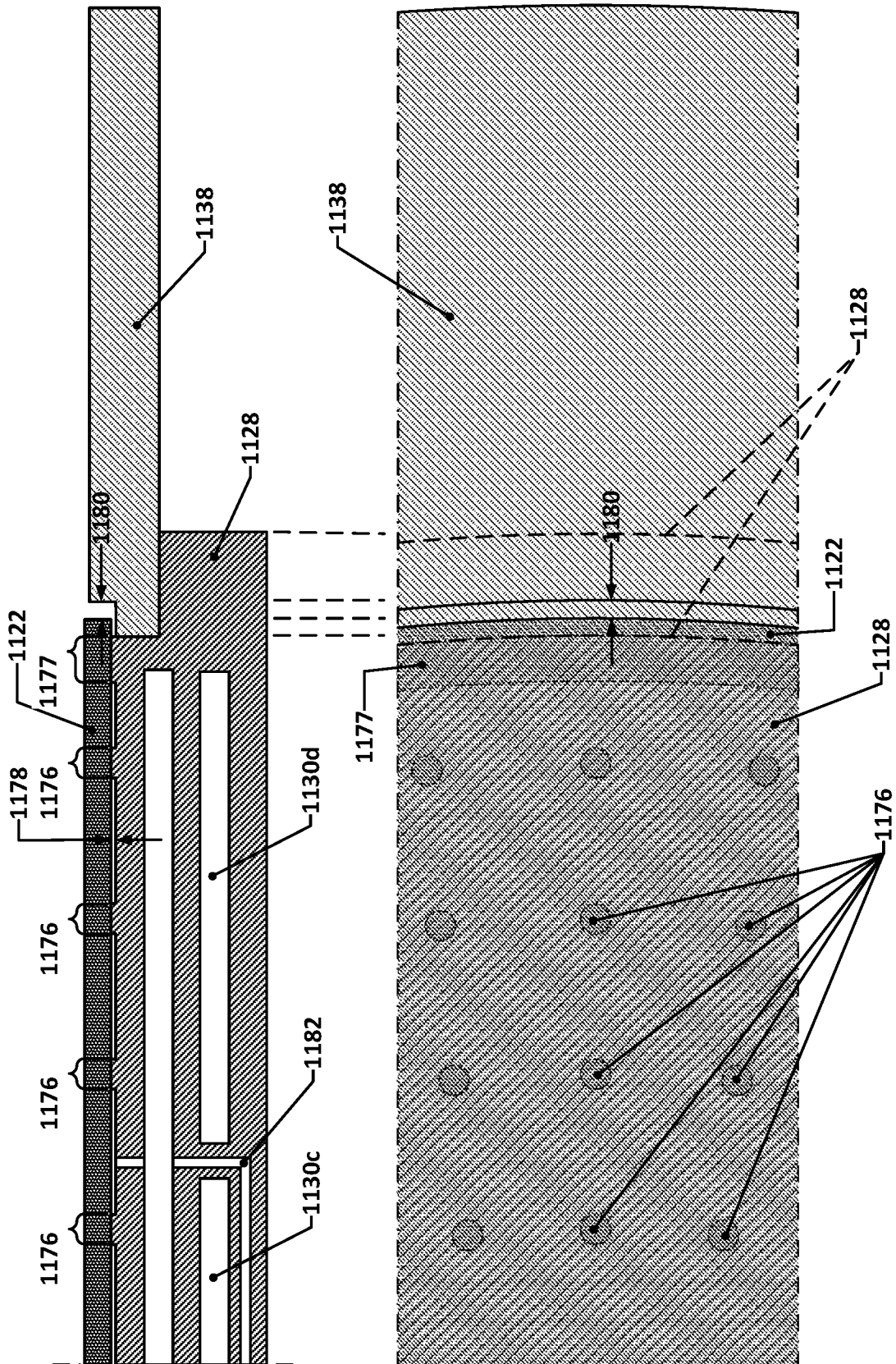


FIG. 11B

## INTERNATIONAL SEARCH REPORT

International application No.

PCT/US2021/061751

<b>A. CLASSIFICATION OF SUBJECT MATTER</b>		
G03F 7/36(2006.01)i; G03F 7/16(2006.01)i; G03F 7/004(2006.01)i; C09K 13/06(2006.01)i; C09K 13/08(2006.01)i		
According to International Patent Classification (IPC) or to both national classification and IPC		
<b>B. FIELDS SEARCHED</b>		
Minimum documentation searched (classification system followed by classification symbols) G03F 7/36(2006.01); C23C 14/56(2006.01); G03F 1/76(2012.01); G03F 7/004(2006.01); G03F 7/20(2006.01); G03F 7/32(2006.01); G03F 7/42(2006.01); H01L 21/02(2006.01); H01L 21/027(2006.01); H01L 21/67(2006.01)		
Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched Korean utility models and applications for utility models Japanese utility models and applications for utility models		
Electronic data base consulted during the international search (name of data base and, where practicable, search terms used) eKOMPASS(KIPO internal) & Keywords: metal-containing resist, dry developing, organic vapor, dry etchant, chamber		
<b>C. DOCUMENTS CONSIDERED TO BE RELEVANT</b>		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X A	WO 2019-217749 A1 (LAM RESEARCH CORPORATION) 14 November 2019 (2019-11-14) paragraphs [0014]-[0033] and figures 1-2	1,7-10 2-6,11-20
A	US 2018-0323064 A1 (SEMES CO., LTD.) 08 November 2018 (2018-11-08) claim 1	1-20
A	US 2020-0089104 A1 (LAM RESEARCH CORPORATION) 19 March 2020 (2020-03-19) the entire document	1-20
A	US 2020-0326627 A1 (INPRIA CORPORATION) 15 October 2020 (2020-10-15) the entire document	1-20
A	WO 2018-004646 A1 (INTEL CORPORATION) 04 January 2018 (2018-01-04) the entire document	1-20
<input type="checkbox"/> Further documents are listed in the continuation of Box C. <input checked="" type="checkbox"/> See patent family annex.		
* Special categories of cited documents: "A" document defining the general state of the art which is not considered to be of particular relevance "D" document cited by the applicant in the international application "E" earlier application or patent but published on or after the international filing date "L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified) "O" document referring to an oral disclosure, use, exhibition or other means "P" document published prior to the international filing date but later than the priority date claimed "T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention "X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone "Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art "&" document member of the same patent family		
Date of the actual completion of the international search <b>24 March 2022</b>		Date of mailing of the international search report <b>24 March 2022</b>
Name and mailing address of the ISA/KR <b>Korean Intellectual Property Office 189 Cheongsa-ro, Seo-gu, Daejeon 35208, Republic of Korea</b> Facsimile No. +82-42-481-8578		Authorized officer <b>HEO, Joo Hyung</b> Telephone No. +82-42-481-5373

**INTERNATIONAL SEARCH REPORT**  
**Information on patent family members**

International application No.

**PCT/US2021/061751**

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				WO	2020-210660	A1	15 October 2020
WO	2018-004646	A1	04 January 2018	None			