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**(71) Applicant: MEDIATEK INC.** [CN/CN]; No. 1, Dusing 1st Rd., Hsinchu Science Park, Hsinchu City, Taiwan 30078 (CN).

**(72) Inventors: HU, Shengquan**; 2840 Junction Ave, San Jose, California 95134 (US). **LIU, Jianhan**; 2840 Junction Ave, San Jose, California 95134 (US). **PARE JR., Thomas Edward**; 2840 Junction Ave, San Jose, California 95134 (US).

**(74) Agent: BEIJING SANYOU INTELLECTUAL PROPERTY AGENCY LTD.**; 16th Fl., Block A, Corporate Square, No.35 Jinrong Street, Xicheng District, Beijing 100033 (CN).



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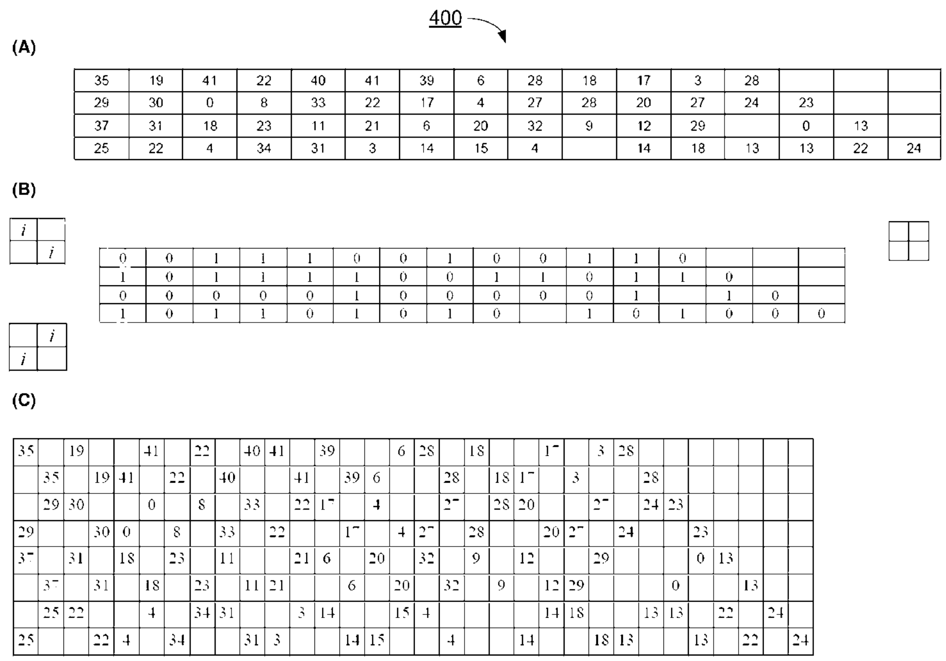


FIG. 4


**(57) Abstract:** Techniques pertaining to low-density parity-check (LDPC) encoding enhancement for next-generation wireless local area network (WLAN) systems in wireless communications are described. An apparatus (e.g., a station (STA) ) encodes a plurality of bits with an enlarged codeword length. The apparatus then communicates with the encoded plurality of bits in a wireless communication system.


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# LDPC ENCODING ENHANCEMENT FOR NEXT-GENERATION WLAN SYSTEMS

## CROSS REFERENCE TO RELATED PATENT APPLICATION

**[0001]** The present disclosure is part of a non-provisional patent application claiming the priority benefit of U.S. Provisional Patent Application No. 63/507,124, filed 09 June 2023, the content of which herein being incorporated by reference in its entirety.

## TECHNICAL FIELD

**[0002]** The present disclosure is generally related to wireless communications and, more particularly, to low-density parity-check (LDPC) encoding enhancement for next-generation wireless local area network (WLAN) systems in wireless communications.

## BACKGROUND

**[0003]** Unless otherwise indicated herein, approaches described in this section are not prior art to the claims listed below and are not admitted as prior art by inclusion in this section.

**[0004]** In wireless communications, LDPC encoding has been used in both cellular communications (e.g., 5$^{th}$ Generation (5G)/New Radio (NR)) in accordance with the 3$^{rd}$ Generation Partnership Project (3GPP) standards as well as Wi-Fi (or WiFi) and WLAN systems in accordance with the Institute of Electrical and Electronics Engineers (IEEE) 802.11 standards. In IEEE 802.11n/ac/ax/be, the highest coding rate is 5/6 and the codeword length is up to 1944 bits. However, to enhance system performance and coverage range, higher LDPC coding rates and increased codeword lengths may be necessary but have yet to be defined. Therefore, there is a need for a solution of LDPC encoding enhancement for next-generation WLAN systems.

## SUMMARY

**[0005]** The following summary is illustrative only and is not intended to be limiting in any way. That is, the following summary is provided to introduce concepts, highlights, benefits and advantages of the novel and non-obvious techniques described herein. Select implementations are further described below in the detailed description. Thus, the following summary is not intended to identify essential features of the claimed subject matter, nor is it intended for use in determining the scope of the claimed subject matter.

**[0006]** An objective of the present disclosure is to provide schemes, concepts, designs, techniques, methods and apparatuses pertaining to LDPC encoding enhancement for next-generation WLAN systems in wireless communications. It is believed that implementations of various schemes proposed herein may extend the LDPC coding rate up to 7/8 and 11/12 and increase the codeword length by two times to 2592 bits (= 2*1296) or 3888 bits (= 2*1944), or by three times to 3888 bits (= 3*1296) or 5832 bits (= 3*1944), or by four times to 5184 bits (= 4*1296) or 7776 bits (= 4*1944).

**[0007]** In one aspect, a method may involve encoding a plurality of bits with an enlarged codeword length. The method may also involve communicating with the encoded plurality of bits in a wireless communication system.

**[0008]** In another aspect, an apparatus may include a transceiver configured to communicate wirelessly and a processor coupled to the transceiver. The processor may encode a plurality of bits with an enlarged codeword length. The processor may also communicate with the encoded plurality of bits in a wireless communication system.

**[0009]** It is noteworthy that, although description provided herein may be in the context of certain radio access technologies, networks and network topologies such as, Wi-Fi, the proposed concepts, schemes and any variation(s)/derivative(s) thereof may be implemented in, for and by other types of radio access technologies, networks and network topologies such as, for example and without limitation, Bluetooth, ZigBee, 5th Generation (5G)/New Radio (NR), Long-Term Evolution (LTE), LTE-Advanced, LTE-Advanced Pro, Internet-of-Things (IoT), Industrial IoT (IIoT) and narrowband IoT (NB-IoT). Thus, the scope of the present disclosure is not limited to the examples described herein.

## BRIEF DESCRIPTION OF THE DRAWINGS

**[0010]** The accompanying drawings are included to provide a further understanding of the disclosure and are incorporated in and constitute a part of the present disclosure. The drawings illustrate implementations of the disclosure and, together with the description, serve to explain the principles of the disclosure. It is appreciable that the drawings are not necessarily in scale as some components may be shown to be out of proportion than the size in actual implementation to clearly illustrate the concept of the present disclosure.

**[0011]** FIG. 1 is a diagram of an example network environment in which various solutions and schemes in accordance with the present disclosure may be implemented.

**[0012]** FIG. 2 is a diagram of an example design under a proposed scheme in accordance with the present disclosure.

**[0013]** FIG. 3 is a diagram of an example design under a proposed scheme in accordance with the present disclosure.

**[0014]** FIG. 4 is a diagram of an example scenario under a proposed scheme in accordance with the present disclosure.

**[0015]** FIG. 5 is a diagram of an example design under a proposed scheme in accordance with the present disclosure.

**[0016]** FIG. 6 is a diagram of an example design under a proposed scheme in accordance with the present disclosure.

**[0017]** FIG. 7 is a diagram of an example design under a proposed scheme in accordance with the present disclosure.

**[0018]** FIG. 8 is a diagram of an example design under a proposed scheme in accordance with the present disclosure.

**[0019]** FIG. 9 is a diagram of an example design under a proposed scheme in accordance with the present disclosure.

**[0020]** FIG. 10 is a diagram of an example design under a proposed scheme in accordance with the present disclosure.

**[0021]** FIG. 11 is a diagram of an example design under a proposed scheme in accordance with the present disclosure.

**[0022]** FIG. 12 is a block diagram of an example communication system in accordance with an implementation of the present disclosure.

**[0023]** FIG. 13 is a flowchart of an example process in accordance with an implementation of the present disclosure.

## DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

**[0024]** Detailed embodiments and implementations of the claimed subject matters are disclosed herein. However, it shall be understood that the disclosed embodiments and implementations are merely illustrative of the claimed subject matters which may be embodied in various forms. The present disclosure may, however, be embodied in many different forms and should not be construed as limited to the exemplary embodiments and implementations set forth herein. Rather, these exemplary embodiments and implementations are provided so that description of the present disclosure is thorough and complete and will fully convey the scope of the present disclosure to those skilled in the art. In the description below, details of well-known features and techniques may be omitted to avoid unnecessarily obscuring the presented embodiments and implementations.

***Overview***

**[0025]** Implementations in accordance with the present disclosure relate to various techniques, methods, schemes and/or solutions pertaining to LDPC encoding enhancement for next-generation WLAN systems in wireless communications. According to the present disclosure, a number of possible solutions may be implemented separately or jointly. That is, although these possible solutions may be described below separately, two or more of these possible solutions may be implemented in one combination or another.

**[0026]** FIG. 1 illustrates an example network environment 100 in which various solutions and schemes in accordance with the present disclosure may be implemented. FIG. 2 ~ FIG. 13 illustrate examples of implementation of various proposed schemes in network environment 100 in accordance with the present disclosure. The following description of various proposed schemes is provided with reference to FIG. 1 ~ FIG. 13.

**[0027]** Referring to part (A) of FIG. 1, network environment 100 may involve at least a station (STA) 110 communicating wirelessly with a STA 120. Either of STA 110 and STA 120 may be an access point (AP) STA or, alternatively, either of STA 110 and STA 120 may function as a non-AP STA. In some cases, STA 110 and STA 120 may be associated with a basic service set (BSS) in accordance with one or more IEEE 802.11 standards (e.g., IEEE 802.11be and future-developed standards). Each of STA 110 and STA 120 may be configured to communicate with each other by utilizing the LDPC encoding enhancement for next-generation WLAN systems in wireless communications in accordance with various proposed schemes described below. It is noteworthy that, while the various proposed schemes may be individually or separately described below, in actual implementations some or all of the proposed schemes may be utilized or otherwise implemented jointly. Of course, each of the proposed schemes may be utilized or otherwise implemented individually or separately.

**[0028]** Under current IEEE 802.11 specifications such as IEEE 802.11n/ac/ax/be, the LDPC coding rate (R) may be 1/2, 2/3, 3/4 or 5/6. As for the codeword (K = L * R), L may be 648, 1296 or 1944. Correspondingly, the parity matrix (Z) may be 27, 54 or 81. Referring to part (B) of FIG. 1, with a coding rate = k / n, the number of rows may be n – k, the number of columns of information bits may be k and the number of columns of parity bits may be n – k, corresponding to the following parameters: a codeword length = n, information part = k, and parity part = n – k. For instance, with R = 3/4 and Z = 81, the codeword length = n = 24 * Z, the number of columns of information part = k = 18 * Z, and the number of columns of parity part = n – k = 6 * Z.

**[0029]** FIG. 2 illustrates an example design 200 under a proposed scheme in accordance with the present disclosure. Design 200 may pertain to a parity check matrix for an LDPC coding rate of R = 7/8. Under the proposed scheme, the coding rate R = 7/8 parity check matrix may be generated using a coding rate of R = 3/4 LDPC parity check matrix by performing a modulo-2 addition between rows 1 and 4, between rows 2 and 5, and between rows 3 and 6.

**[0030]** FIG. 3 illustrates an example design 300 under a proposed scheme in accordance with the present disclosure. Design 300 may pertain to a parity check matrix for an LDPC coding rate of R = 11/12. Under the proposed scheme, the coding rate R = 11/12 parity check matrix may be generated using a coding rate of

R = 5/6 LDPC parity check matrix by performing a modulo-2 addition between rows 1 and 3, and between rows 2 and 4.

**[0031]** FIG. 4 illustrates an example scenario 400 under a proposed scheme in accordance with the present disclosure. Scenario 400 may pertain to enlargement of LDPC codeword length by using a lifting matrix. As defined in IEEE 802.11ad, the coding rate may be 1/2, 5/8, 3/4 or 13/16, and, for the parity matrix, Z = 42 and H = 336 * 672, 252 * 672, 168 * 672 or 126 * 672, respectively. As defined in IEEE 802.11ay, the coding rate may be 1/2, 5/8, 3/4, 13/16, 7/8, 2/3 or 5/6, and for the parity matrix, Z = 42 for a code length = 672 and H = 336 * 672, 252 * 672, 168 * 672, 126 * 672, 2Z * 2Z with a lifting matrix, respectively, with the code length = 2 * 672 = 1344. Under the proposed scheme, a lifting matrix similar to that defined in IEEE 802.11ay may be utilized to increase the LDPC codeword length.

**[0032]** Referring to part (A) of FIG. 4, with an original code rate R = 3/4 LDPC parity check matrix, Z = 42 with 168 rows x 672 columns. Part (B) of FIG. 4 shows a lifting matrix for code rate of 3/4. Part (C) of FIG. 4 shows an LDPC code matrix for code rate of 3/4 resulting from applying the lifting matrix of part (B) of FIG. 4 to the original LDPC parity check matrix of part (A) of FIG. 4. The resultant matrix may have 2 * 168 rows x 2 * 672 column = 336 rows x 1344 columns.

**[0033]** In legacy Wi-Fi systems in accordance with IEEE 802.11n/ac/ax/be, there are three types of codeword length, namely: n = 648, 1296 or 1944. Submatrix size Z = 27 is used for n = 648, Z = 54 for n = 1296, and Z = 81 for n = 1944. Under the various proposed schemes in accordance with the present disclosure, LDPC codeword length may be increased (e.g., for IEEE 802.11bn and/or Ultra-High Reliability (UHR) communications) may be achieved by a one-step lifting. Under the proposed schemes, the codeword length n = 1296 and 1944 may be increased or otherwise enlarged to n = 2 * 1296 = 2592, n = 2 * 1944 = 3888, n = 3 * 1296, n = 3 * 1944, n = 4 * 1296, and n = 4 * 1944. To increase or enlarge the codeword length two times (2x) by applying a lifting matrix, each element in the lifting matrix acting on a Z x Z submatrix may create a submatrix of size 2Z x 2Z (e.g., 2Z x 2Z = 2 * 54 x 2 * 54 for codeword length n = 2 * 1296, and 2Z x 2Z = 2 * 81 x 2 * 81 for codeword length n = 2 * 1944). To increase or enlarge the codeword length three times (3x) by applying a lifting matrix, each element in the lifting matrix acting on a Z x Z submatrix may create a submatrix of size 3Z x 3Z (e.g., 3Z x 3Z = 3 * 54 x 3 * 54 for codeword length n = 3 * 1296, and 3Z x 3Z = 3 * 81 x 3 * 81 for codeword length n = 3 * 1944). To increase or enlarge the codeword length four times (4x) by applying a lifting matrix, each element in the lifting matrix acting on a Z x Z submatrix may create a submatrix of size 4Z x 4Z (e.g., 4Z x 4Z = 4 * 54 x 4 * 54 for codeword length n = 4 * 1296, and 4Z x 4Z = 4 * 81 x 4 * 81 for codeword length n = 4 * 1944).

**[0034]** FIG. 5 illustrates an example design 500 under a proposed scheme in accordance with the present disclosure. Design 500 may pertain to increasing LDPC codeword length by one-step lifting (e.g., for IEEE 802.11bn/UHR). Under the proposed scheme, a non-blank ("0") element in a lifting matrix may act on a Z x Z cyclic permutation matrix Pi in the LDPC parity check matrix to cause or result in enlargement. Referring to part (A) of FIG. 5, a non-blank "0" element in the lifting matrix may act on a Z x Z cyclic permutation matrix Pi in the LDPC parity check matrix to cause or result in a 2Z x 2Z submatrix for two times (2x) enlargement of the codeword length, with "i" denoting the value of an original element of the Z x Z cyclic permutation matrix Pi which is duplicated and disposed along a diagonal line from an upper-left corner to a lower-right corner of the 2Z x 2Z submatrix. Referring to part (B) of FIG. 5, a non-blank "0" element in the lifting matrix may act on a Z x Z cyclic permutation matrix Pi in the LDPC parity check matrix to cause or result in a 3Z x 3Z submatrix for three times (3x) enlargement of the codeword length, with "i" denoting the value of an original element of the Z x Z cyclic permutation matrix Pi which is duplicated and disposed along a diagonal line from an upper-left corner to a lower-right corner of the 3Z x 3Z submatrix. Referring to part

(C) of FIG. 5, a non-blank "0" element in the lifting matrix may act on a Z x Z cyclic permutation matrix Pi in the LDPC parity check matrix to cause or result in a 4Z x 4Z submatrix for four times (4x) enlargement of the codeword length, with "i" denoting the value of an original element of the Z x Z cyclic permutation matrix Pi which is duplicated and disposed along a diagonal line from an upper-left corner to a lower-right corner of the 4Z x 4Z submatrix.

**[0035]** FIG. 6 illustrates an example design 600 under a proposed scheme in accordance with the present disclosure. Design 600 may pertain to increasing LDPC codeword length by one-step lifting (e.g., for IEEE 802.11bn/UHR). Under the proposed scheme, a non-blank ("1") element in a lifting matrix may act on a Z x Z cyclic permutation matrix Pi in the LDPC parity check matrix to cause or result in enlargement. Referring to part (A) of FIG. 6, a non-blank "1" element in the lifting matrix may act on a Z x Z cyclic permutation matrix Pi in the LDPC parity check matrix to cause or result in a 2Z x 2Z submatrix for two times (2x) enlargement of the codeword length, with "i" denoting the value of an original element of the Z x Z cyclic permutation matrix Pi which is duplicated and disposed along a diagonal line from an upper-right corner to a lower-left corner of the 2Z x 2Z submatrix. Referring to part (B) of FIG. 6, a non-blank "1" element in the lifting matrix may act on a Z x Z cyclic permutation matrix Pi in the LDPC parity check matrix to cause or result in a 3Z x 3Z submatrix for three times (3x) enlargement of the codeword length, with "i" denoting the value of an original element of the Z x Z cyclic permutation matrix Pi which is duplicated and disposed along a diagonal line from an upper-right corner to a lower-left corner of the 3Z x 3Z submatrix. Referring to part (C) of FIG. 6, a non-blank "1" element in the lifting matrix may act on a Z x Z cyclic permutation matrix Pi in the LDPC parity check matrix to cause or result in a 4Z x 4Z submatrix for four times (4x) enlargement of the codeword length, with "i" denoting the value of an original element of the Z x Z cyclic permutation matrix Pi which is duplicated and disposed along a diagonal line from an upper-right corner to a lower-left corner of the 4Z x 4Z submatrix.

**[0036]** FIG. 7 illustrates an example design 700 under a proposed scheme in accordance with the present disclosure. Design 700 may pertain to increasing LDPC codeword length by one-step lifting (e.g., for IEEE 802.11bn/UHR). Under the proposed scheme, a blank (" ") element in a lifting matrix may act on a Z x Z cyclic permutation matrix Pi in the LDPC parity check matrix to cause or result in enlargement. Referring to part (A) of FIG. 7, a blank element in the lifting matrix may act on a Z x Z cyclic permutation matrix Pi in the LDPC parity check matrix to cause or result in a 2Z x 2Z zero-matrix for two times (2x) enlargement of the codeword length. Referring to part (B) of FIG. 7, a blank element in the lifting matrix may act on a Z x Z cyclic permutation matrix Pi in the LDPC parity check matrix to cause or result in a 3Z x 3Z zero-matrix for three times (3x) enlargement of the codeword length. Referring to part (C) of FIG. 7, a blank element in the lifting matrix may act on a Z x Z cyclic permutation matrix Pi in the LDPC parity check matrix to cause or result in a 4Z x 4Z zero-matrix for four times (4x) enlargement of the codeword length.

**[0037]** Under the various proposed schemes in accordance with the present disclosure, LDPC codeword length may be increased (e.g., for IEEE 802.11bn and/or UHR communications) may be achieved by a two-step lifting. Under the proposed schemes, for codeword length n = 4 * 1296 and 4 * 1944, a one-step lifting matrix or a two-step lifting matrix may be applied to increase or otherwise enlarge the codeword length. For the two-step lifting matrix, a first-step lifting matrix and a second-step lifting matrix may be applied, and the first-step lifting matrix and the second-step lifting matrix may be the same or different. For instance, for n = 4 * 1944, in a first step each element in the first-step lifting matrix (M1) acting on a Z x Z submatrix may create a submatrix of size Z1 x Z1 = 2 * Z x 2 * Z = 2 * 81 x 2 * 81, and the first-step lifting matrix M1 may be applied on an LDPC parity check matrix H1. Then, in a second step a second-step lifting matrix (M2) may be applied on H1, and each element in the second-step matrix M1 acting on the Z1 x Z1 submatrix may create a submatrix of size Z2 x Z2 = 2 * Z1 x 2 * Z1 = 2 * 2 * 81 x 2 * 2 * 81 = 4 * 81 x 4 * 81, and the final LDPC parity check matrix H2 may result by applying the second-step lifting matrix M2 on top of H1. Here, M1 = M2 or M1 != M2.

**[0038]** FIG. 8 illustrates an example design 800 under a proposed scheme in accordance with the present disclosure. Design 800 may pertain to an example of a lifting matrix design for Z = 54, R = 1/2. Part (A) of FIG. 8 shows an original parity check matrix for Z = 54 may have a code rate R = 1/2. Part (B) of FIG. 8 shows an example lifting matrix under the proposed scheme for Z = 54 and R = 1/2.

**[0039]** FIG. 9 illustrates an example design 900 under a proposed scheme in accordance with the present disclosure. Design 900 may pertain to an example of a lifting matrix design for Z = 81, R = 1/2. Part (A) of FIG. 9 shows an original parity check matrix for Z = 81 may have a code rate R = 1/2. Part (B) of FIG. 9 shows an example lifting matrix under the proposed scheme for Z = 81 and R = 1/2.

**[0040]** FIG. 10 illustrates an example design 1000 under a proposed scheme in accordance with the present disclosure. Design 1000 may pertain to an example of a lifting matrix design for Z = 54, R = 3/4. Part (A) of FIG. 10 shows an original parity check matrix for Z = 54 may have a code rate R = 3/4. Part (B) of FIG. 10 shows an example lifting matrix under the proposed scheme for Z = 54 and R = 3/4.

**[0041]** FIG. 11 illustrates an example design 1100 under a proposed scheme in accordance with the present disclosure. Design 1100 may pertain to an example of a lifting matrix design for Z = 81, R = 3/4. Part (A) of FIG. 11 shows an original parity check matrix for Z = 81 may have a code rate R = 3/4. Part (B) of FIG. 11 shows an example lifting matrix under the proposed scheme for Z = 81 and R = 3/4.

***Illustrative Implementations***

**[0042]** FIG. 12 illustrates an example system 1200 having at least an example apparatus 1210 and an example apparatus 1220 in accordance with an implementation of the present disclosure. Each of apparatus 1210 and apparatus 1220 may perform various functions to implement schemes, techniques, processes and methods described herein pertaining to LDPC encoding enhancement for next-generation WLAN systems in wireless communications including the various schemes described above with respect to various proposed designs, concepts, schemes, systems and methods described above as well as processes described below. For instance, apparatus 1210 may be implemented in STA 110 and apparatus 1220 may be implemented in STA 120, or vice versa.

**[0043]** Each of apparatus 1210 and apparatus 1220 may be a part of an electronic apparatus, which may be a non-AP STA or an AP STA, such as a portable or mobile apparatus, a wearable apparatus, a wireless communication apparatus or a computing apparatus. When implemented in a STA, each of apparatus 1210 and apparatus 1220 may be implemented in a smartphone, a smart watch, a personal digital assistant, a digital camera, or a computing equipment such as a tablet computer, a laptop computer or a notebook computer. Each of apparatus 1210 and apparatus 1220 may also be a part of a machine type apparatus, which may be an IoT apparatus such as an immobile or a stationary apparatus, a home apparatus, a wire communication apparatus or a computing apparatus. For instance, each of apparatus 1210 and apparatus 1220 may be implemented in a smart thermostat, a smart fridge, a smart door lock, a wireless speaker or a home control center. When implemented in or as a network apparatus, apparatus 1210 and/or apparatus 1220 may be implemented in a network node, such as an AP in a WLAN.

**[0044]** In some implementations, each of apparatus 1210 and apparatus 1220 may be implemented in the form of one or more integrated-circuit (IC) chips such as, for example and without limitation, one or more single-core processors, one or more multi-core processors, one or more reduced-instruction set computing (RISC) processors, or one or more complex-instruction-set-computing (CISC) processors. In the various schemes described above, each of apparatus 1210 and apparatus 1220 may be implemented in or as a STA or an AP. Each of apparatus 1210 and apparatus 1220 may include at least some of those components shown in FIG. 12 such as a processor 1212 and a processor 1222, respectively, for example. Each of apparatus 1210 and apparatus 1220 may further include one or more other components not pertinent to the proposed scheme of the present disclosure (e.g., internal power supply, display device and/or user interface device), and, thus, such component(s) of apparatus 1210 and apparatus 1220 are neither shown in FIG. 12 nor described below in the interest of simplicity and brevity.

**[0045]** In one aspect, each of processor 1212 and processor 1222 may be implemented in the form of one or more single-core processors, one or more multi-core processors, one or more RISC processors or one or more CISC processors. That is, even though a singular term "a processor" is used herein to refer to processor 1212 and processor 1222, each of processor 1212 and processor 1222 may include multiple processors in some implementations and a single processor in other implementations in accordance with the present disclosure. In another aspect, each of processor 1212 and processor 1222 may be implemented in the form of hardware (and, optionally, firmware) with electronic components including, for example and without limitation, one or more transistors, one or more diodes, one or more capacitors, one or more resistors, one or more inductors, one or more memristors and/or one or more varactors that are configured and arranged to achieve specific purposes in accordance with the present disclosure. In other words, in at least some implementations, each of processor 1212 and processor 1222 is a special-purpose machine specifically designed, arranged and configured to perform specific tasks including those pertaining to LDPC encoding enhancement for next-generation WLAN systems in wireless communications in accordance with various implementations of the present disclosure.

**[0046]** In some implementations, apparatus 1210 may also include a transceiver 1216 coupled to processor 1212. Transceiver 1216 may include a transmitter capable of wirelessly transmitting and a receiver capable of wirelessly receiving data. In some implementations, apparatus 1220 may also include a transceiver 1226 coupled to processor 1222. Transceiver 1226 may include a transmitter capable of wirelessly transmitting and a receiver capable of wirelessly receiving data. It is noteworthy that, although transceiver 1216 and transceiver 1226 are illustrated as being external to and separate from processor 1212 and processor 1222, respectively, in some implementations, transceiver 1216 may be an integral part of processor 1212 as a system on chip (SoC), and transceiver 1226 may be an integral part of processor 1222 as a SoC.

**[0047]** In some implementations, apparatus 1210 may further include a memory 1214 coupled to processor 1212 and capable of being accessed by processor 1212 and storing data therein. In some implementations, apparatus 1220 may further include a memory 1224 coupled to processor 1222 and capable of being accessed by processor 1222 and storing data therein. Each of memory 1214 and memory 1224 may include a type of random-access memory (RAM) such as dynamic RAM (DRAM), static RAM (SRAM), thyristor RAM (T-RAM) and/or zero-capacitor RAM (Z-RAM). Alternatively, or additionally, each of memory 1214 and memory 1224 may include a type of read-only memory (ROM) such as mask ROM, programmable ROM (PROM), erasable programmable ROM (EPROM) and/or electrically erasable programmable ROM (EEPROM). Alternatively, or additionally, each of memory 1214 and memory 1224 may include a type of non-volatile random-access memory (NVRAM) such as flash memory, solid-state memory, ferroelectric RAM (FeRAM), magnetoresistive RAM (MRAM) and/or phase-change memory.

**[0048]** Each of apparatus 1210 and apparatus 1220 may be a communication entity capable of communicating with each other using various proposed schemes in accordance with the present disclosure. For illustrative purposes and without limitation, a description of capabilities of apparatus 1210, as STA 110, and apparatus 1220, as STA 120, is provided below in the context of example process 1300. It is noteworthy that, although a detailed description of capabilities, functionalities and/or technical features of apparatus 1220 is provided below, the same may be applied to apparatus 1210 although a detailed description thereof is not provided solely in the interest of brevity. It is also noteworthy that, although the example implementations described below are provided in the context of WLAN, the same may be implemented in other types of networks.

***Illustrative Processes***

**[0049]** FIG. 13 illustrates an example process 1300 in accordance with an implementation of the present disclosure. Process 1300 may represent an aspect of implementing various proposed designs, concepts, schemes, systems and methods described above. More specifically, process 1300 may represent an aspect of the proposed concepts and schemes pertaining to LDPC encoding enhancement for next-generation WLAN systems in wireless communications in accordance with the present disclosure. Process 1300 may include one or more operations, actions, or functions as illustrated by one or more of blocks 1310 and 1320. Although illustrated as discrete blocks, various blocks of process 1300 may be divided into additional blocks, combined into fewer blocks, or eliminated, depending on the desired implementation. Moreover, the blocks/sub-blocks of process 1300 may be executed in the order shown in FIG. 13 or, alternatively, in a different order. Furthermore, one or more of the blocks/sub-blocks of process 1300 may be executed repeatedly or iteratively. Process 1300 may be implemented by or in apparatus 1210 and apparatus 1220 as well as any variations thereof. Solely for illustrative purposes and without limiting the scope, process 1300 is described below in the context of apparatus 1210 implemented in or as STA 110 functioning as a non-AP STA or an AP STA and apparatus 1220 implemented in or as STA 120 functioning as an AP STA or a non-AP STA of a wireless network such as a WLAN in network environment 100 in accordance with one or more of IEEE 802.11 standards. Process 1300 may begin at block 1310.

**[0050]** At 1310, process 1300 may involve processor 1212 of apparatus 1210 encoding a plurality of bits with an enlarged codeword length. Process 1300 may proceed from 1310 to 1320.

**[0051]** At 1320, process 1300 may involve processor 1212 communicating, via transceiver 1216, with the encoded plurality of bits in a wireless communication system (e.g., by transmitting the encoded bits to apparatus 1220).

**[0052]** In some implementations, in encoding, process 1300 may involve processor 1212 increasing a codeword length n by two times (2x) such that: (a) for n = 1296, the enlarged codeword length = 2 * 1296 = 2595, and (b) for n = 1944, the enlarged codeword length = 2 * 1944 = 3888. In some implementations, in encoding, process 1300 may further involve processor 1212 applying a lifting matrix such that each element in the lifting matrix acting on a Z x Z cyclic permutation matrix in an LDPC parity check matrix creates a submatrix of size 2Z x 2Z such that: (1) for n = 1296, 2Z x 2Z = 2 * 54 x 2 * 54, and (2) for n = 1944, 2Z x 2Z = 2 * 81 x 2 * 81. In some implementations, in applying the lifting matrix, process 1300 may involve processor 1212 applying the lifting matrix in a one-step lifting such that: (i) a non-blank element "0" in the lifting matrix acting on the Z x Z cyclic permutation matrix creates the 2Z x 2Z submatrix with a value of an original element of the Z x Z cyclic permutation matrix disposed along a diagonal line from an upper-left corner to a lower-right corner of the 2Z x 2Z submatrix, (ii) a non-blank element "1" in the lifting matrix acting on the Z x Z cyclic permutation matrix creates the 2Z x 2Z submatrix with the value of the original element of the Z x Z cyclic permutation matrix disposed along another diagonal line from an upper-right corner to a lower-left corner of the 2Z x 2Z submatrix, and (iii) a blank element in the lifting matrix acting on the Z x Z cyclic permutation matrix creates a 2Z x 2Z zero-matrix.

**[0053]** In some implementations, in encoding, process 1300 may involve processor 1212 increasing a codeword length n by three times (3x) such that: (a) for n = 1296, the enlarged codeword length = 3 * 1296 = 3888, and (b) for n = 1944, the enlarged codeword length = 3 * 1944 = 5832. In some implementations, in encoding, process 1300 may further involve processor 1212 applying a lifting matrix such that each element in the lifting matrix acting on a Z x Z cyclic permutation matrix in an LDPC parity check matrix creates a submatrix of size 3Z x 3Z such that: (1) for n = 1296, 3Z x 3Z = 3 * 54 x 3 * 54, and (2) for n = 1944, 3Z x 3Z = 3 * 81 x 3 * 81. In some implementations, in applying the lifting matrix, process 1300 may involve processor 1212 applying the lifting matrix in a one-step lifting such that: (i) a non-blank element "0" in the lifting matrix acting on the Z x Z cyclic permutation matrix creates the 3Z x 3Z submatrix with a value of an original element of the Z x Z cyclic permutation matrix disposed along a diagonal line from an upper-left corner to a lower-right corner of the 3Z x 3Z submatrix, (ii) a non-blank element "1" in the lifting matrix acting on the Z x Z cyclic permutation matrix creates the 3Z x 3Z submatrix with the value of the original element of the Z x Z cyclic permutation matrix disposed along another diagonal line from an upper-right corner to a lower-left corner of the 3Z x 3Z submatrix, and (iii) a blank element in the lifting matrix acting on the Z x Z cyclic permutation matrix creates a 3Z x 3Z zero-matrix.

**[0054]** In some implementations, in encoding, process 1300 may involve processor 1212 increasing a codeword length n by four times (4x) such that: (a) for n = 1296, the enlarged codeword length = 4 * 1296 = 5184, and (b) for n = 1944, the enlarged codeword length = 4 * 1944 = 7776. In some implementations, in encoding, process 1300 may further involve processor 1212 applying a lifting matrix such that each element in the lifting matrix acting on a Z x Z cyclic permutation matrix in an LDPC parity check matrix creates a submatrix of size 4Z x 4Z such that: (1) for n = 1296, 4Z x 4Z = 4 * 54 x 4 * 54, and (2) for n = 1944, 4Z x 4Z = 4 * 81 x 4 * 81. In some implementations, in applying the lifting matrix, process 1300 may involve processor 1212 applying the lifting matrix in a one-step lifting such that: (i) a non-blank element "0" in the lifting matrix acting on the Z x Z cyclic permutation matrix creates the 4Z x 4Z submatrix with a value of an original element of the Z x Z cyclic permutation matrix disposed along a diagonal line from an upper-left corner to a lower-right corner of the 4Z x 4Z submatrix, (ii) a non-blank element "1" in the lifting matrix acting on the Z x Z cyclic permutation matrix creates the 4Z x 4Z submatrix with the value of the original element of the Z x Z cyclic permutation matrix disposed along another diagonal line from an upper-right corner to a lower-left corner of the 4Z x 4Z submatrix, and (iii) a blank element in the lifting matrix acting on the Z x Z cyclic permutation matrix creates a 4Z x 4Z zero-matrix.

**[0055]** In some implementations, in encoding, process 1300 may involve processor 1212 increasing a codeword length by four times (4x) with a first-step lifting or a two-step lifting. In some implementations, in increasing the codeword length, process 1300 may involve processor 1212 increasing the codeword length with the two-step lifting by first applying a first-step lifting matrix (M1) and then applying a second-step lifting matrix (M2). In some implementations, the first-step lifting matrix and the second-step lifting matrix may be same. Alternatively, the first-step lifting matrix and the second-step lifting matrix may be different.

***Additional Notes***

**[0056]** The herein-described subject matter sometimes illustrates different components contained within, or connected with, different other components. It is to be understood that such depicted architectures are merely examples, and that in fact many other architectures can be implemented which achieve the same functionality. In a conceptual sense, any arrangement of components to achieve the same functionality is effectively "associated" such that the desired functionality is achieved. Hence, any two components herein combined to achieve a particular functionality can be seen as "associated with" each other such that the desired functionality is achieved, irrespective of architectures or intermedial components. Likewise, any two components so associated can also be viewed as being "operably connected", or "operably coupled", to each other to achieve the desired functionality, and any two components capable of being so associated can also be viewed as being "operably couplable", to each other to achieve the desired functionality. Specific examples of operably couplable include but are not limited to physically mateable and/or physically interacting components and/or wirelessly interactable and/or wirelessly interacting components and/or logically interacting and/or logically interactable components.

**[0057]** Further, with respect to the use of substantially any plural and/or singular terms herein, those having skill in the art can translate from the plural to the singular and/or from the singular to the plural as is appropriate to the context and/or application. The various singular/plural permutations may be expressly set forth herein for sake of clarity.

**[0058]** Moreover, it will be understood by those skilled in the art that, in general, terms used herein, and especially in the appended claims, e.g., bodies of the appended claims, are generally intended as “open” terms, e.g., the term “including” should be interpreted as “including but not limited to,” the term “having” should be interpreted as “having at least,” the term “includes” should be interpreted as “includes but is not limited to,” etc. It will be further understood by those within the art that if a specific number of an introduced claim recitation is intended, such an intent will be explicitly recited in the claim, and in the absence of such recitation no such intent is present. For example, as an aid to understanding, the following appended claims may contain usage of the introductory phrases "at least one" and "one or more" to introduce claim recitations. However, the use of such phrases should not be construed to imply that the introduction of a claim recitation by the indefinite articles "a" or "an" limits any particular claim containing such introduced claim recitation to implementations containing only one such recitation, even when the same claim includes the introductory phrases "one or more" or "at least one" and indefinite articles such as "a" or "an," e.g., “a” and/or “an” should be interpreted to mean “at least one” or “one or more;” the same holds true for the use of definite articles used to introduce claim recitations. In addition, even if a specific number of an introduced claim recitation is explicitly recited, those skilled in the art will recognize that such recitation should be interpreted to mean at least the recited number, e.g., the bare recitation of "two recitations," without other modifiers, means at least two recitations, or two or more recitations. Furthermore, in those instances where a convention analogous to “at least one of A, B, and C, etc.” is used, in general such a construction is intended in the sense one having skill in the art would understand the convention, e.g., “a system having at least one of A, B, and C” would include but not be limited to systems that have A alone, B alone, C alone, A and B together, A and C together, B and C together, and/or A, B, and C together, etc. In those instances where a convention analogous to “at least one of A, B, or C, etc.” is used, in general such a construction is intended in the sense one having skill in the art would understand the convention, e.g., “a system having at least one of A, B, or C” would include but not be limited to systems that have A alone, B alone, C alone, A and B together, A and C together, B and C together, and/or A, B, and C together, etc. It will be further understood by those within the art that virtually any disjunctive word and/or phrase presenting two or more alternative terms, whether in the description, claims, or drawings, should be understood to contemplate the possibilities of including one of the terms, either of the terms, or both terms. For example, the phrase “A or B” will be understood to include the possibilities of “A” or “B” or “A and B.”

**[0059]** From the foregoing, it will be appreciated that various implementations of the present disclosure have been described herein for purposes of illustration, and that various modifications may be made without departing from the scope and spirit of the present disclosure. Accordingly, the various implementations disclosed herein are not intended to be limiting, with the true scope and spirit being indicated by the following claims.

## CLAIMS

***What is claimed is:***

**1.** A method, comprising:

encoding, by a processor of an apparatus, a plurality of bits with an enlarged codeword length; and

communicating, by the processor, with the encoded plurality of bits in a wireless communication system.

**2.** The method of Claim 1, wherein the encoding comprises increasing a codeword length n by two times (2x) such that:

for n = 1296, the enlarged codeword length = 2 * 1296 = 2595, and

for n = 1944, the enlarged codeword length = 2 * 1944 = 3888.

**3.** The method of Claim 2, wherein the encoding further comprises applying a lifting matrix such that each element in the lifting matrix acting on a Z x Z cyclic permutation matrix in a low-density parity-check (LDPC) parity check matrix creates a submatrix of size 2Z x 2Z such that:

for n = 1296, 2Z x 2Z = 2 * 54 x 2 * 54, and

for n = 1944, 2Z x 2Z = 2 * 81 x 2 * 81.

**4.** The method of Claim 3, wherein the applying of the lifting matrix comprises applying the lifting matrix in a one-step lifting such that:

a non-blank element “0” in the lifting matrix acting on the Z x Z cyclic permutation matrix creates the 2Z x 2Z submatrix with a value of an original element of the Z x Z cyclic permutation matrix disposed along a diagonal line from an upper-left corner to a lower-right corner of the 2Z x 2Z submatrix,

a non-blank element “1” in the lifting matrix acting on the Z x Z cyclic permutation matrix creates the 2Z x 2Z submatrix with the value of the original element of the Z x Z cyclic permutation matrix disposed along another diagonal line from an upper-right corner to a lower-left corner of the 2Z x 2Z submatrix, and

a blank element in the lifting matrix acting on the Z x Z cyclic permutation matrix creates a 2Z x 2Z zero-matrix.

**5.** The method of Claim 1, wherein the encoding comprises increasing a codeword length n by three times (3x) such that:

for n = 1296, the enlarged codeword length = 3 * 1296 = 3888, and

for n = 1944, the enlarged codeword length = 3 * 1944 = 5832.

**6.** The method of Claim 5, wherein the encoding further comprises applying a lifting matrix such that each element in the lifting matrix acting on a Z x Z cyclic permutation matrix in a low-density parity-check (LDPC) parity check matrix creates a submatrix of size 3Z x 3Z such that:

for n = 1296, 3Z x 3Z = 3 * 54 x 3 * 54, and

for n = 1944, 3Z x 3Z = 3 * 81 x 3 * 81.

**7.** The method of Claim 6, wherein the applying of the lifting matrix comprises applying the lifting matrix in a one-step lifting such that:

a non-blank element “0” in the lifting matrix acting on the Z x Z cyclic permutation matrix creates the 3Z x 3Z submatrix with a value of an original element of the Z x Z cyclic permutation matrix disposed along a diagonal line from an upper-left corner to a lower-right corner of the 3Z x 3Z submatrix,

a non-blank element “1” in the lifting matrix acting on the Z x Z cyclic permutation matrix creates the 3Z x 3Z submatrix with the value of the original element of the Z x Z cyclic permutation matrix disposed along another diagonal line from an upper-right corner to a lower-left corner of the 3Z x 3Z submatrix, and

a blank element in the lifting matrix acting on the Z x Z cyclic permutation matrix creates a 3Z x 3Z zero-matrix.

**8.** The method of Claim 1, wherein the encoding comprises increasing a codeword length n by four times (4x) such that:

for n = 1296, the enlarged codeword length = 4 * 1296 = 5184, and

for n = 1944, the enlarged codeword length = 4 * 1944 = 7776.

**9.** The method of Claim 8, wherein the encoding further comprises applying a lifting matrix such that each element in the lifting matrix acting on a Z x Z cyclic permutation matrix in a low-density parity-check (LDPC) parity check matrix creates a submatrix of size 4Z x 4Z such that:

for n = 1296, 4Z x 4Z = 4 * 54 x 4 * 54, and

for n = 1944, 4Z x 4Z = 4 * 81 x 4 * 81.

**10.** The method of Claim 9, wherein the applying of the lifting matrix comprises applying the lifting matrix in a one-step lifting such that:

a non-blank element “0” in the lifting matrix acting on the Z x Z cyclic permutation matrix creates the 4Z x 4Z submatrix with a value of an original element of the Z x Z cyclic permutation matrix disposed along a diagonal line from an upper-left corner to a lower-right corner of the 4Z x 4Z submatrix,

a non-blank element “1” in the lifting matrix acting on the Z x Z cyclic permutation matrix creates the 4Z x 4Z submatrix with the value of the original element of the Z x Z cyclic permutation matrix disposed along another diagonal line from an upper-right corner to a lower-left corner of the 4Z x 4Z submatrix, and

a blank element in the lifting matrix acting on the Z x Z cyclic permutation matrix creates a 4Z x 4Z zero-matrix.

**11.** The method of Claim 1, the encoding comprises increasing a codeword length by four times (4x) with a first-step lifting or a two-step lifting.

**12.** The method of Claim 11, the increasing of the codeword length comprises increasing the codeword length with the two-step lifting by first applying a first-step lifting matrix (M1) and then applying a second-step lifting matrix (M2).

**13.** The method of Claim 12, the first-step lifting matrix and the second-step lifting matrix are same.

**14.** The method of Claim 12, the first-step lifting matrix and the second-step lifting matrix are different.

**15.** An apparatus, comprising:

a transceiver configured to communicate wirelessly; and

a processor coupled to the transceiver and configured to perform operations comprising:

encoding a plurality of bits with an enlarged codeword length; and

communicating, via the transceiver, with the encoded plurality of bits in a wireless communication system.

**16.** The apparatus of Claim 15, wherein the encoding comprises increasing a codeword length n by two times (2x) such that:

for n = 1296, the enlarged codeword length = 2 * 1296 = 2595, and

for n = 1944, the enlarged codeword length = 2 * 1944 = 3888.

**17.** The apparatus of Claim 15, wherein the encoding comprises increasing a codeword length n by three times (3x) such that:

for n = 1296, the enlarged codeword length = 3 * 1296 = 3888, and

for n = 1944, the enlarged codeword length = 3 * 1944 = 5832.

**18.** The apparatus of Claim 15, wherein the encoding comprises increasing a codeword length n by four times (4x) such that:

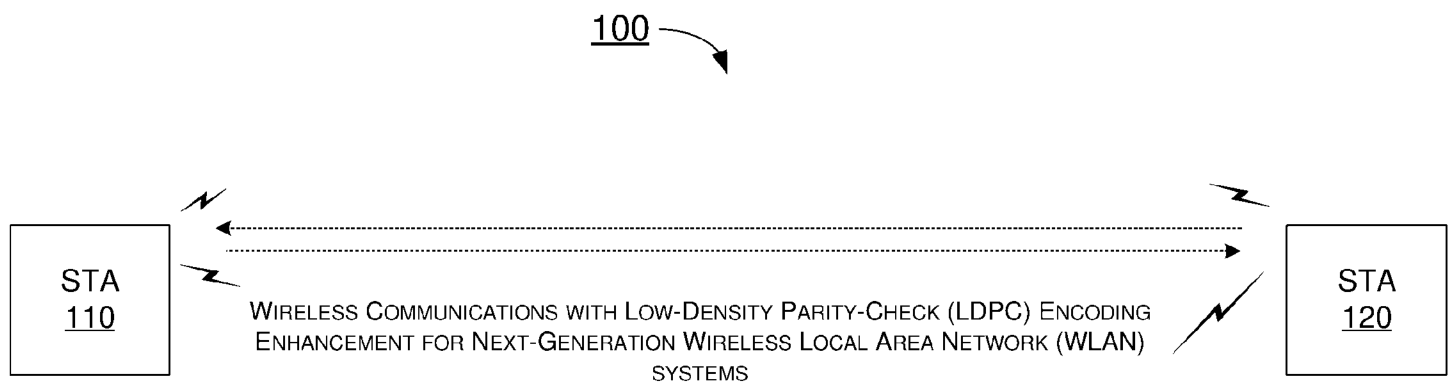
for n = 1296, the enlarged codeword length = 4 * 1296 = 5184, and

for n = 1944, the enlarged codeword length = 4 * 1944 = 7776.

**19.** The apparatus of Claim 15, the encoding comprises increasing a codeword length with a first-step lifting.

**20.** The apparatus of Claim 15, the encoding comprises increasing a codeword length with a two-step lifting by first applying a first-step lifting matrix (M1) and then applying a second-step lifting matrix (M2).

(A)




(B)

- **Coding rate=k/n**

Codeword length: n

Information part: k

parity part: n-k

n-k

FIG. 1

200

(c) Coding rate R = 3/4.

| | | | | | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 48 | 29 | 28 | 39 | 9 | 61 | - | - | - | 63 | 45 | 80 | - | - | - | 37 | 32 | 22 | 1 | 0 | - | - | - | - |
| 4 | 49 | 42 | 48 | 11 | 30 | - | - | - | 49 | 17 | 41 | 37 | 15 | - | 54 | - | - | - | 0 | 0 | - | - | - |
| 35 | 76 | 78 | 51 | 37 | 35 | 21 | - | 17 | 64 | - | - | - | 59 | 7 | - | - | 32 | - | - | 0 | 0 | - | - |
| 9 | 65 | 44 | 9 | 54 | 56 | 73 | 34 | 42 | - | - | - | 35 | - | - | - | 46 | 39 | 0 | - | - | 0 | 0 | - |
| 3 | 62 | 7 | 80 | 68 | 26 | - | 80 | 55 | - | 36 | - | 26 | - | 9 | - | 72 | - | - | - | - | - | 0 | 0 |
| 26 | 75 | 33 | 21 | 69 | 59 | 3 | 38 | - | - | - | 35 | - | 62 | 36 | 26 | - | - | 1 | - | - | - | - | 0 |

FIG. 2

300

(d) Coding rate R = 5/6.

| | | | | | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 13 | 48 | 80 | 66 | 4 | 74 | 7 | 30 | 76 | 52 | 37 | 60 | - | 49 | 73 | 31 | 74 | 73 | 23 | - | 1 | 0 | - | - |
| 69 | 63 | 74 | 56 | 64 | 77 | 57 | 65 | 6 | 16 | 51 | - | 64 | - | 68 | 9 | 48 | 62 | 54 | 27 | - | 0 | 0 | - |
| 51 | 15 | 0 | 80 | 24 | 25 | 42 | 54 | 44 | 71 | 71 | 9 | 67 | 35 | - | 58 | - | 29 | - | 53 | 0 | - | 0 | 0 |
| 16 | 29 | 36 | 41 | 44 | 56 | 59 | 37 | 50 | 24 | - | 65 | 4 | 65 | 52 | - | 4 | - | 73 | 52 | 1 | - | - | 0 |

FIG. 3

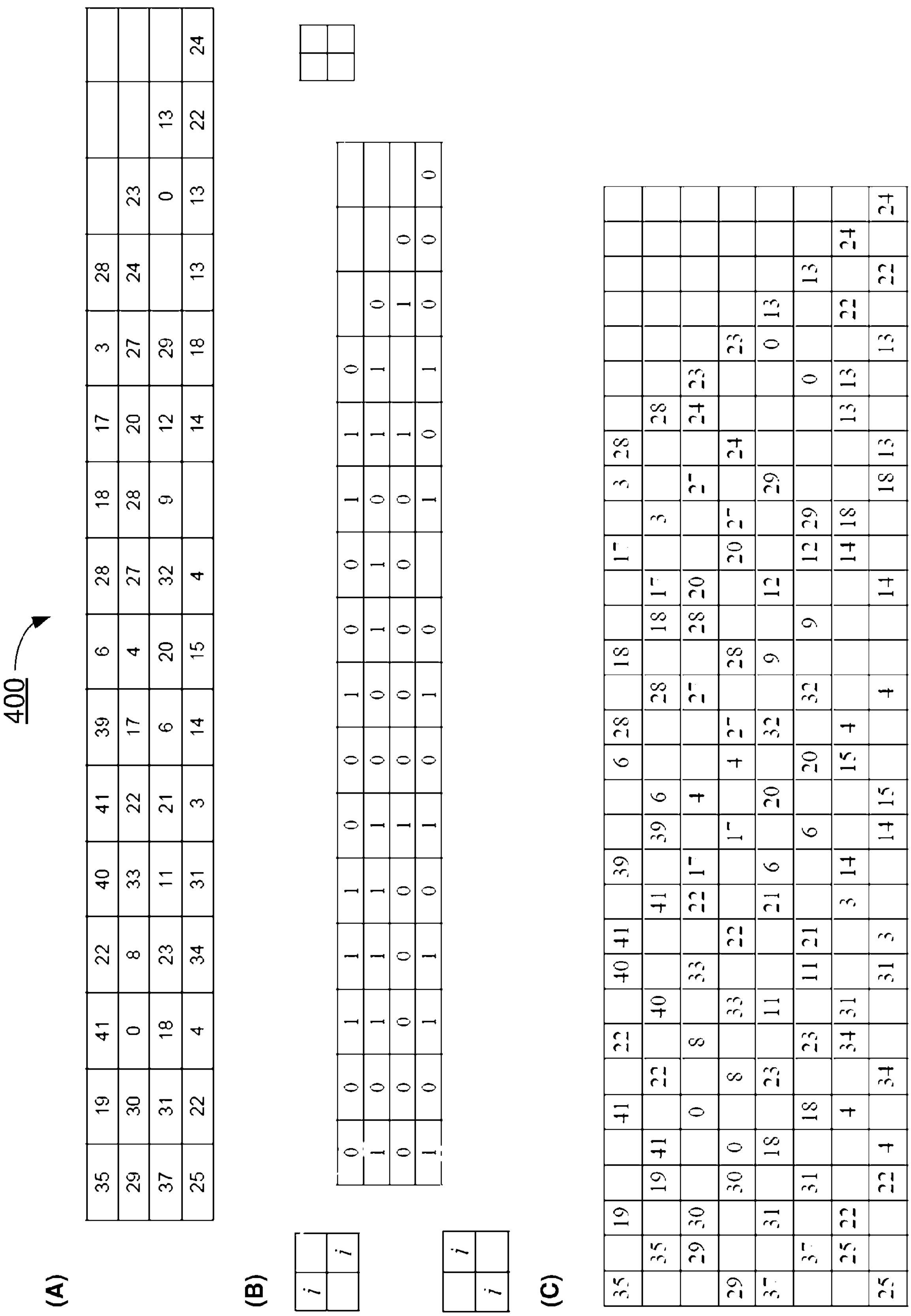
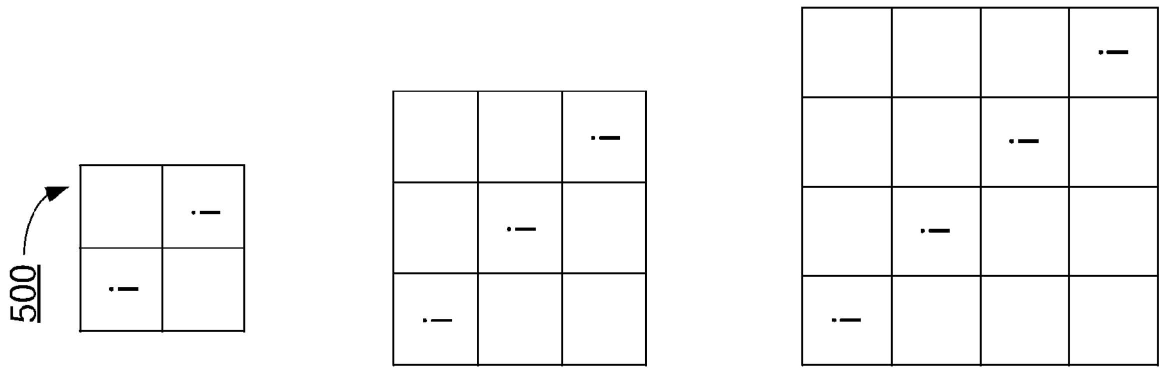
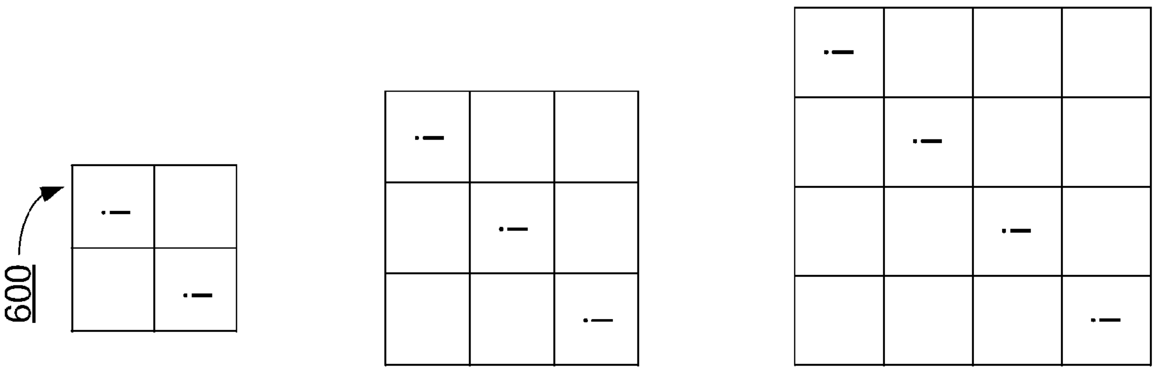



FIG. 4




(A) (B) (C)

FIG. 5




(A) (B) (C)

FIG. 6

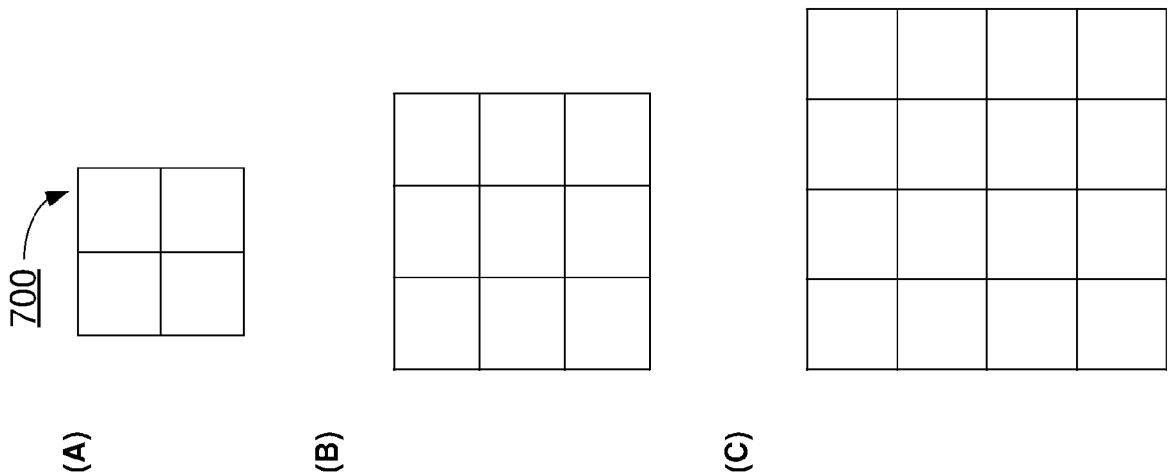



FIG. 7

800

(A)

(a) Coding rate R = 1/2.

| | | | | | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 40 | - | - | - | 22 | - | 49 | 23 | 43 | - | - | - | 1 | 0 | - | - | - | - | - | - | - | - | - | - |
| 50 | 1 | - | - | 48 | 35 | - | - | 13 | - | 30 | - | - | 0 | 0 | - | - | - | - | - | - | - | - | - |
| 39 | 50 | - | - | 4 | - | 2 | - | - | - | - | 49 | - | - | 0 | 0 | - | - | - | - | - | - | - | - |
| 33 | - | - | 38 | 37 | - | - | 4 | 1 | - | - | - | - | - | - | 0 | 0 | - | - | - | - | - | - | - |
| 45 | - | - | - | 0 | 22 | - | - | 20 | 42 | - | - | - | - | - | - | 0 | 0 | - | - | - | - | - | - |
| 51 | - | - | 48 | 35 | - | - | - | 44 | - | 18 | - | - | - | - | - | - | 0 | 0 | - | - | - | - | - |
| 47 | 11 | - | - | - | 17 | - | - | 51 | - | - | - | 0 | - | - | - | - | - | 0 | 0 | - | - | - | - |
| 5 | - | 25 | - | 6 | - | 45 | - | 13 | 40 | - | - | - | - | - | - | - | - | - | 0 | 0 | - | - | - |
| 33 | - | - | 34 | 24 | - | - | - | 23 | - | - | 46 | - | - | - | - | - | - | - | - | 0 | 0 | - | - |
| 1 | - | 27 | - | 1 | - | - | - | 38 | - | 44 | - | - | - | - | - | - | - | - | - | - | 0 | 0 | - |
| - | 18 | - | - | 23 | - | - | 8 | 0 | 35 | - | - | - | - | - | - | - | - | - | - | - | - | 0 | 0 |
| 49 | - | 17 | - | 30 | - | - | - | 34 | - | - | 19 | 1 | - | - | - | - | - | - | - | - | - | - | 0 |

(B)

| | | | | | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | | | | 0 | | 0 | 1 | 0 | | | | 0 | 0 | | | | | | | | | | |
| 1 | 0 | | | 0 | 1 | | | 1 | | 0 | | | 0 | 0 | | | | | | | | | |
| 0 | 1 | | | 1 | | 1 | | | | | 1 | | | 0 | 0 | | | | | | | | |
| 0 | | | 1 | 0 | | | 0 | 1 | | | | | | | 0 | 0 | | | | | | | |
| 0 | | | | 0 | 1 | | | 0 | 0 | | | | | | | 0 | 0 | | | | | | |
| 0 | | | 1 | 0 | | | | 1 | | 0 | | | | | | | 0 | 0 | | | | | |
| 1 | 0 | | | | 1 | | | 0 | | | | 0 | | | | | | 0 | 0 | | | | |
| 1 | | 1 | | 1 | | 1 | | 0 | 0 | | | | | | | | | | 0 | 0 | | | |
| 1 | | | 1 | 1 | | | | 0 | | | 0 | | | | | | | | | 0 | 0 | | |
| 0 | | 1 | | 1 | | | | 1 | | 1 | | | | | | | | | | | 0 | 0 | |
| | 0 | | | 0 | | | 1 | 1 | 1 | | | | | | | | | | | | | 0 | 0 |
| 1 | | 1 | | 0 | | | | 1 | | | 1 | 0 | | | | | | | | | | | 0 |

FIG. 8

900

(A)

(a) Coding rate R = 1 2.

| | | | | | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 57 | - | - | - | 50 | - | 11 | - | 50 | - | 79 | - | 1 | 0 | - | - | - | - | - | - | - | - | - | - |
| 3 | - | 28 | - | 0 | - | - | - | 55 | 7 | - | - | - | 0 | 0 | - | - | - | - | - | - | - | - | - |
| 30 | - | - | - | 24 | 37 | - | - | 56 | 14 | - | - | - | - | 0 | 0 | - | - | - | - | - | - | - | - |
| 62 | 53 | - | - | 53 | - | - | 3 | 35 | - | - | - | - | - | - | 0 | 0 | - | - | - | - | - | - | - |
| 40 | - | - | 20 | 66 | - | - | 22 | 28 | - | - | - | - | - | - | - | 0 | 0 | - | - | - | - | - | - |
| 0 | - | - | - | 8 | - | 42 | - | 50 | - | - | 8 | - | - | - | - | - | 0 | 0 | - | - | - | - | - |
| 69 | 79 | 79 | - | - | - | 56 | - | 52 | - | - | - | 0 | - | - | - | - | - | 0 | 0 | - | - | - | - |
| 65 | - | - | - | 38 | 57 | - | - | 72 | - | 27 | - | - | - | - | - | - | - | - | 0 | 0 | - | - | - |
| 64 | - | - | - | 14 | 52 | - | - | 30 | - | - | 32 | - | - | - | - | - | - | - | - | 0 | 0 | - | - |
| - | 45 | - | 70 | 0 | - | - | - | 77 | 9 | - | - | - | - | - | - | - | - | - | - | - | 0 | 0 | - |
| 2 | 56 | - | 57 | 35 | - | - | - | - | - | 12 | - | - | - | - | - | - | - | - | - | - | - | 0 | 0 |
| 24 | - | 61 | - | 60 | - | - | 27 | 51 | - | - | 16 | 1 | - | - | - | - | - | - | - | - | - | - | 0 |

(B)

| | | | | | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | | | | 0 | | 0 | | 1 | | 1 | | 0 | 0 | | | | | | | | | | |
| 1 | | 1 | | 1 | | | | 1 | 1 | | | | 0 | 0 | | | | | | | | | |
| 1 | | | | 1 | 1 | | | 0 | 1 | | | | | 0 | 0 | | | | | | | | |
| 1 | 1 | | | 0 | | | 0 | 0 | | | | | | | 0 | 0 | | | | | | | |
| 1 | | | 1 | 1 | | | 1 | 0 | | | | | | | | 0 | 0 | | | | | | |
| 1 | | | | 1 | | 0 | | 1 | | | 1 | | | | | | 0 | 0 | | | | | |
| 1 | 1 | 0 | | | | 0 | | 1 | | | | 0 | | | | | | 0 | 0 | | | | |
| 0 | | | | 1 | 0 | | | 0 | | 1 | | | | | | | | | 0 | 0 | | | |
| 1 | | | | 0 | 0 | | | 1 | | | 0 | | | | | | | | | 0 | 0 | | |
| | 0 | | 1 | 1 | | | | 1 | 1 | | | | | | | | | | | | 0 | 0 | |
| 0 | 0 | | 1 | 1 | | | | | | 1 | | | | | | | | | | | | 0 | 0 |
| 0 | | 1 | | 0 | | | 0 | 0 | | | 0 | 0 | | | | | | | | | | | 0 |

FIG. 9

1000

(A)

(c) Coding rate R = 3/4.

| | | | | | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 39 | 40 | 51 | 41 | 3 | 29 | 8 | 36 | - | 14 | - | 6 | - | 33 | - | 11 | - | 4 | 1 | 0 | - | - | - | - |
| 48 | 21 | 47 | 9 | 48 | 35 | 51 | - | 38 | - | 28 | - | 34 | - | 50 | - | 50 | - | - | 0 | 0 | - | - | - |
| 30 | 39 | 28 | 42 | 50 | 39 | 5 | 17 | - | 6 | - | 18 | - | 20 | - | 15 | - | 40 | - | - | 0 | 0 | - | - |
| 29 | 0 | 1 | 43 | 36 | 30 | 47 | - | 49 | - | 47 | - | 3 | - | 35 | - | 34 | - | 0 | - | - | 0 | 0 | - |
| 1 | 32 | 11 | 23 | 10 | 44 | 12 | 7 | - | 48 | - | 4 | - | 9 | - | 17 | - | 16 | - | - | - | - | 0 | 0 |
| 13 | 7 | 15 | 47 | 23 | 16 | 47 | - | 43 | - | 29 | - | 52 | - | 2 | - | 53 | - | 1 | - | - | - | - | 0 |

(B)

| | | | | | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | | 1 | | 1 | | 0 | | 1 | | 0 | 0 | 0 | | | | |
| 0 | 0 | 1 | 0 | 0 | 1 | 0 | | 0 | | 0 | | 1 | | 0 | | 0 | | | 0 | 0 | | | |
| 1 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | | 1 | | 0 | | 0 | | 1 | | 0 | | | 0 | 0 | | |
| 1 | 0 | 0 | 1 | 0 | 1 | 1 | | 0 | | 0 | | 1 | | 1 | | 1 | | 0 | | | 0 | 0 | |
| 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | | 0 | | 0 | | 1 | | 0 | | 1 | | | | | 0 | 0 |
| 1 | 0 | 1 | 1 | 0 | 1 | 0 | | 0 | | 1 | | 1 | | 0 | | 1 | | 0 | | | | | 0 |

FIG. 10

1100

(A)

(c) Coding rate R = 3/4.

| | | | | | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 48 | 29 | 28 | 39 | 9 | 61 | - | - | - | 63 | 45 | 80 | - | - | - | 37 | 32 | 22 | 1 | 0 | - | - | - | - |
| 4 | 49 | 42 | 48 | 11 | 30 | - | - | - | 49 | 17 | 41 | 37 | 15 | - | 54 | - | - | - | 0 | 0 | - | - | - |
| 35 | 76 | 78 | 51 | 37 | 35 | 21 | - | 17 | 64 | - | - | - | 59 | 7 | - | - | 32 | - | - | 0 | 0 | - | - |
| 9 | 65 | 44 | 9 | 54 | 56 | 73 | 34 | 42 | - | - | - | 35 | - | - | - | 46 | 39 | 0 | - | - | 0 | 0 | - |
| 3 | 62 | 7 | 80 | 68 | 26 | - | 80 | 55 | - | 36 | - | 26 | - | 9 | - | 72 | - | - | - | - | - | 0 | 0 |
| 26 | 75 | 33 | 21 | 69 | 59 | 3 | 38 | - | - | - | 35 | - | 62 | 36 | 26 | - | - | 1 | - | - | - | - | 0 |

(B)

| | | | | | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 1 | 0 | 1 | 0 | | | | 1 | 0 | 1 | | | | 0 | 0 | 1 | 0 | 0 | | | | |
| 1 | 0 | 1 | 1 | 0 | 0 | | | | 1 | 0 | 0 | 0 | 1 | | 1 | | | | 0 | 0 | | | |
| 1 | 0 | 0 | 0 | 1 | 1 | 0 | | 1 | 0 | | | | 1 | 0 | | | 0 | | | 0 | 0 | | |
| 0 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | | | | 0 | | | | 1 | 1 | 0 | | | 0 | 0 | |
| 1 | 0 | 1 | 0 | 1 | 1 | | 0 | 1 | | 1 | | 1 | | 0 | | 1 | | | | | | 0 | 0 |
| 1 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | | | | 0 | | 0 | 1 | 1 | | | 0 | | | | | 0 |

FIG. 11

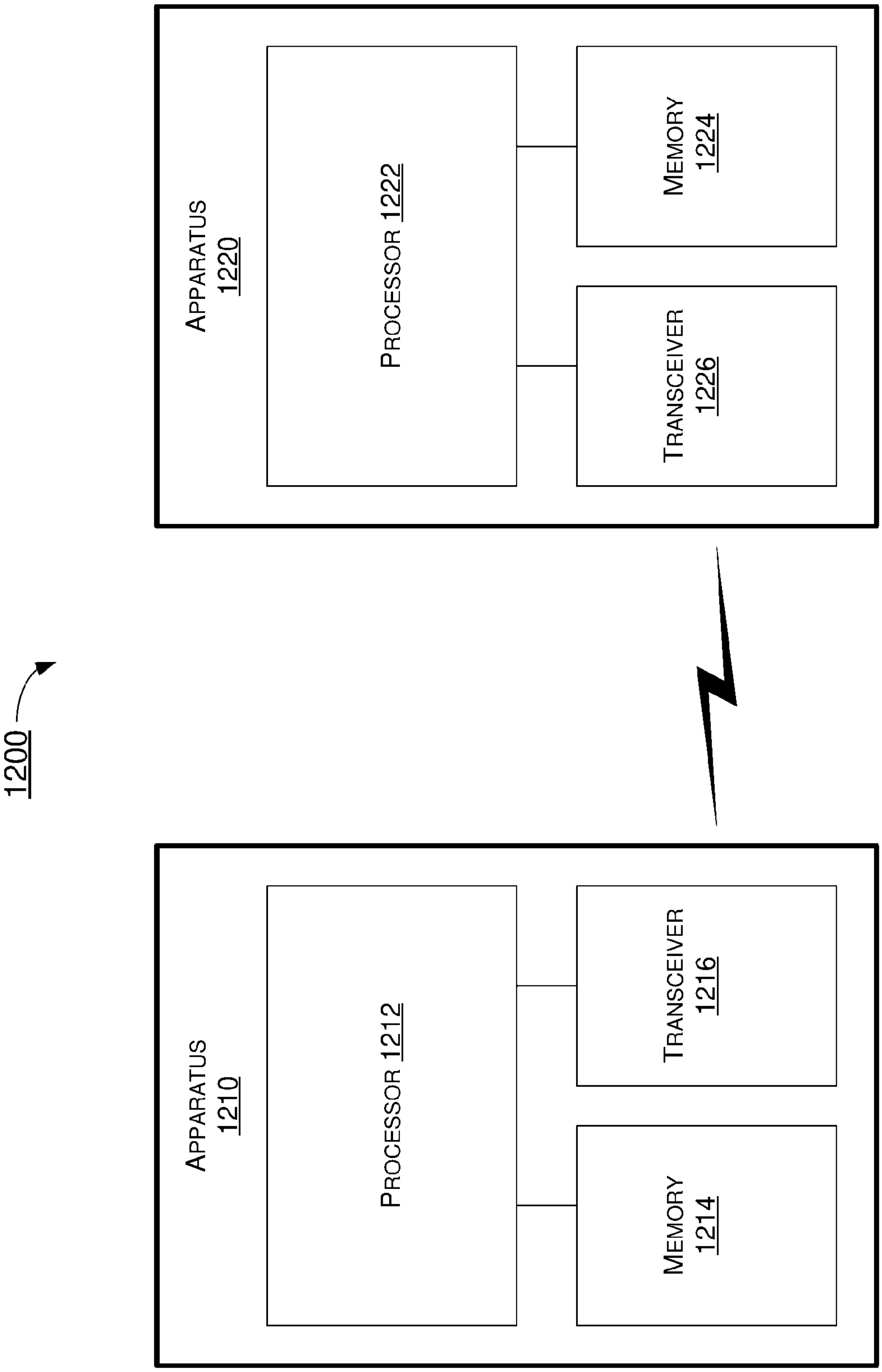

1200
APPARATUS
1220
PROCESSOR 1222
MEMORY
1224
TRANSCEIVER
1226
APPARATUS
1210
PROCESSOR 1212
TRANSCEIVER
1216
MEMORY
1214

FIG. 12

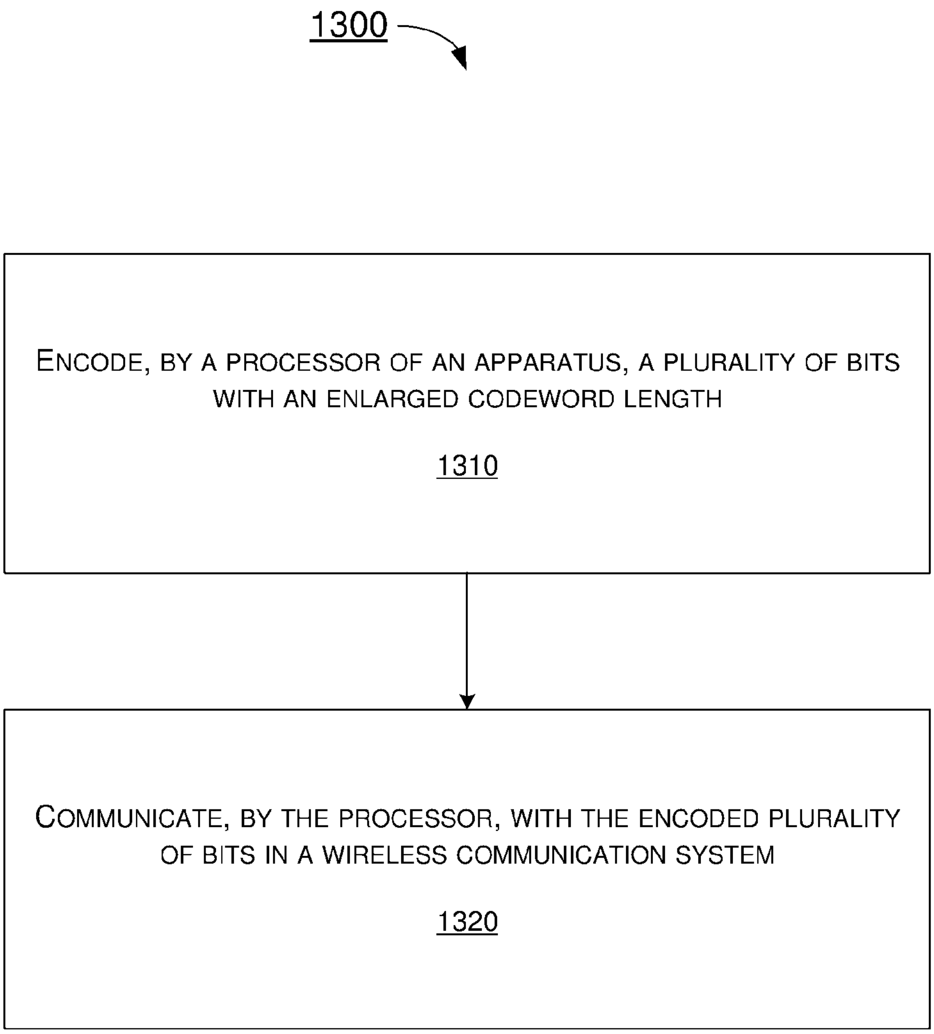

1300
ENCODE, BY A PROCESSOR OF AN APPARATUS, A PLURALITY OF BITS WITH AN ENLARGED CODEWORD LENGTH
1310
COMMUNICATE, BY THE PROCESSOR, WITH THE ENCODED PLURALITY OF BITS IN A WIRELESS COMMUNICATION SYSTEM
1320

FIG. 13

# INTERNATIONAL SEARCH REPORT

International application No.

**PCT/CN2024/098239**

## A. CLASSIFICATION OF SUBJECT MATTER

H04L1/00(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

## B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC:H04L, H03M

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

CNTXT,ENTXT,DWPI,ENTXTC,CNKI,IEEE:LDPC, lifting matrix, puncturing, encode, expansion,enlarge

## C. DOCUMENTS CONSIDERED TO BE RELEVANT

| Category* | Citation of document, with indication, where appropriate, of the relevant passages | Relevant to claim No. |
|---|---|---|
| X | US 2017134050 A1 (SAMSUNG ELECTRONICS CO., LTD) 11 May 2017 (2017-05-11)<br>description, paragraphs 0048-0150, and figures 1-29 | 1-20 |
| X | US 2006242534 A1 (LIVSHITZ, Michael ) 26 October 2006 (2006-10-26)<br>description, paragraphs 0012-0085, and figures 1-6 | 1-3,5,6,8,9,11-20 |
| X | CN 114902569 A (QUALCOMM INCORPORATED) 12 August 2022 (2022-08-12)<br>description, paragraphs 0034-0150 , and figures 1-17 | 1,15 |
| X | CN 1949694 A (SHANGHAI JIAOTONG UNIVERSITY) 18 April 2007 (2007-04-18)<br>description, pages 2-5, and figures 1-8 | 1,15 |

☐ Further documents are listed in the continuation of Box C. ☑ See patent family annex.

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- "P" document published prior to the international filing date but later than the priority date claimed
- "T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
- "X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
- "Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
- "&" document member of the same patent family

| Date of the actual completion of the international search | Date of mailing of the international search report |
|---|---|
| **22 August 2024** | **04 September 2024** |


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**CHINA NATIONAL INTELLECTUAL PROPERTY ADMINISTRATION**
**6, Xitucheng Rd., Jimen Bridge, Haidian District, Beijing 100088, China**

Authorized officer

**CHEN,ShiYuan**

Telephone No. **(+86) 010-53961762**

# INTERNATIONAL SEARCH REPORT
**Information on patent family members**

International application No.
**PCT/CN2024/098239**

| Patent document cited in search report | | | Publication date (day/month/year) | Patent family member(s) | | | Publication date (day/month/year) |
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| | | | | IN | 202247032594 | A | 24 June 2022 |
| | | | | TW | 202133564 | A | 01 September 2021 |
| CN | 1949694 | A | 18 April 2007 | None | | | |