



- (51) International Patent Classification:
G11C 7/06 (2006.01) *G11C 7/14* (2006.01)
G11C 7/10 (2006.01) *G11C 11/16* (2006.01)
G11C 7/12 (2006.01)
- (21) International Application Number:
PCT/US2009/055617
- (22) International Filing Date:
1 September 2009 (01.09.2009)
- (25) Filing Language: English
- (26) Publication Language: English
- (30) Priority Data:
12/206,933 9 September 2008 (09.09.2008) US
- (71) Applicant (for all designated States except US): **QUALCOMM INCORPORATED** [US/US]; Attn: International IP Administration, 5775 Morehouse Drive, San Diego, California 92121 (US).

- (72) Inventors; and
- (75) Inventors/Applicants (for US only): **DAVIERWALLA, Anosh B.** [US/US]; 5775 Morehouse Drive, San Diego, California 92121 (US). **ZHONG, Cheng** [CN/US]; 5775 Morehouse Drive, San Diego, California 92121 (US). **PARK, Dongkyu** [KR/US]; 5775 Morehouse Drive, San Diego, California 92121 (US). **ABU-RAHMA, Mo-hamed Hassan** [EG/US]; 5775 Morehouse Drive, San Diego, California 92121 (US). **SANI, Mehdi Hamidi** [US/US]; 5775 Morehouse Drive, San Diego, California 92121 (US). **YOON, Sei Seung** [KR/US]; 5775 Morehouse Drive, San Diego, California 92121 (US).
- (74) Agent: **TALPALATSKY, Sam**; 5775 Morehouse Drive, San Diego, California 92121 (US).
- (81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD,

[Continued on next page]

(54) Title: MEMORY DEVICE FOR RESISTANCE-BASED MEMORY APPLICATIONS

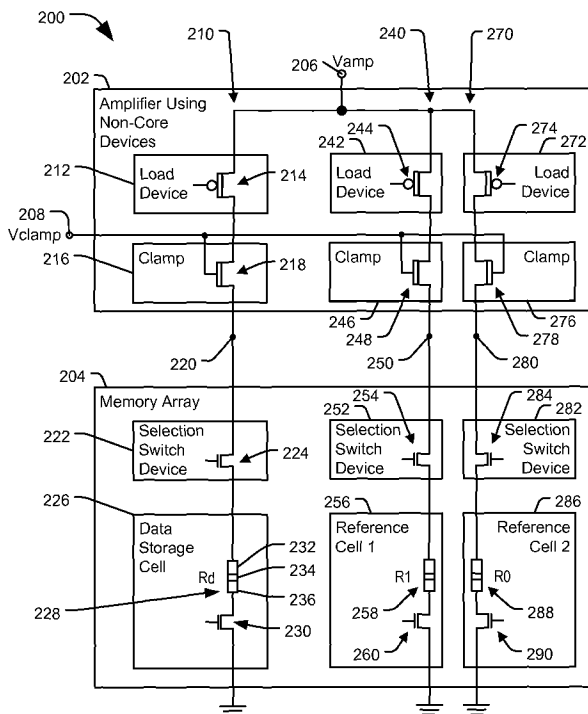


FIG. 2

(57) Abstract: In a particular embodiment, a memory device (100) is disclosed that includes a memory cell (226) including a resistance based memory element (228) coupled to an access transistor (230). The access transistor has a first oxide thickness to enable operation of the memory cell at an operating voltage. The memory device also includes a first amplifier (202) configured to couple the memory cell to a supply voltage (Vamp) that is greater than a voltage limit to generate a data signal based on a current through the memory cell. The first amplifier includes a clamp transistor (216) that has a second oxide thickness that is greater than the first oxide thickness. The clamp transistor is configured to prevent the operating voltage at the memory cell from exceeding the voltage limit.

WO 2010/030531 A1

ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PE, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

(84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, SE, SI, SK, SM,

Declarations under Rule 4.17:

- as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))
- as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))

Published:

- with international search report (Art. 21(3))

MEMORY DEVICE FOR RESISTANCE-BASED MEMORY APPLICATIONS

I. Field of the Disclosure

[0001] The present disclosure is generally directed to a memory device including an amplifier and a memory cell including a resistance-based memory element.

II. Background

[0002] Advances in non-volatile memory technology include resistance-based memory technologies, such as Magnetic Random Access Memory (MRAM). MRAM technology is an emerging non-volatile memory technology that employs ferromagnetic-based Magnetic Tunnel Junctions (MTJs) as the basic memory elements. A commonly used array architecture for MRAMs is the one-transistor, one-MTJ (1T1MTJ) architecture. As the name suggests, each bit cell in this architecture consists of an MTJ connected in series with an NMOS access transistor. In order to leverage the increased density and area reduction advantages associated with scaling down MOS technologies, it is desirable to use core transistors within the MRAM bit cell. However, while scaling down MOS technology into the deep submicron regime yields area and density benefits to the MRAM bit cells, using these deep submicron devices in the MRAM sense amplifier degrades the read performance (the output swing) of the MRAM sense amplifier due to operating voltage limitations of these deep submicron devices.

[0003] Conventional MRAM sense amplifier designs for the 1T1MTJ architecture use core transistors. However, due to breakdown and reliability considerations, the supply voltage for the core transistors is typically limited to about 1 volt (V) for leading-edge deep submicron technologies. The following devices are stacked between the supply rails in conventional MRAM sense amplifier designs for the 1T1MTJ architecture: the bit cell comprising an access transistor and an MTJ device, a mux transistor, a clamp transistor, and a PMOS load transistor. The access and mux transistors should be operated as switches (in the linear region), while the clamp and PMOS load transistors should remain in saturation for the sense amplifier to exhibit reasonable gain. However, the low supply voltage requirement that comes from using core devices in the sense

amplifier coupled with the transistor threshold voltage being a significant fraction of this supply voltage can make it difficult to keep the clamp and PMOS load transistors in saturation, which in turn, degrades the gain and results in a sub-optimal signal swing at the sense amplifier output.

III. Summary

[0004] In a particular embodiment, a memory device is disclosed that includes a memory cell including a resistance-based memory element coupled to an access transistor. The access transistor has a first oxide thickness to enable operation of the memory cell at an operating voltage. The memory device also includes a first amplifier configured to couple the memory cell to a supply voltage that is greater than a voltage limit to generate a data signal based on a current through the memory cell. The first amplifier includes a clamp transistor that has a second oxide thickness that is greater than the first oxide thickness. The clamp transistor is configured to prevent the operating voltage at the memory cell from exceeding the voltage limit.

[0005] In another embodiment, a memory device is disclosed that includes a data read path including a first load device coupled to a data storage cell via a first clamp transistor. The first load device has a first device configuration to operate at a first supply voltage. The data storage cell includes an access transistor having a second device configuration to operate at a voltage not to exceed a voltage limit that is less than the first supply voltage. A control terminal of the clamp transistor is biased to prevent the voltage at the data storage cell from exceeding the voltage limit.

[0006] In another embodiment, a method is disclosed that includes coupling a first amplifier stage to a memory array. The first amplifier stage includes transistors having an input-output (IO) supply voltage tolerance. The memory array including transistors having a core supply voltage tolerance that is less than the IO supply voltage tolerance. The method includes applying a control voltage at a clamp transistor coupled to the memory array to set a memory array voltage, such that the memory array voltage is less than the core supply voltage tolerance.

[0007] One particular advantage provided by the disclosed embodiments is an improvement in the read performance of the MRAM sense amplifier because the higher

supply voltage enables a greater output swing to distinguish logical values during read operations.

[0008] Other aspects, advantages, and features of the present disclosure will become apparent after review of the entire application, including the following sections: Brief Description of the Drawings, Detailed Description, and the Claims.

IV. Brief Description of the Drawings

[0009] FIG. 1 is a diagram of a particular illustrative embodiment of a memory device with an amplifier using a first type of device and a memory array using a second type of device;

[0010] FIG. 2 is a diagram of a second illustrative embodiment of a memory device with an amplifier using a first type of device and a memory array using a second type of device;

[0011] FIG. 3 is a diagram of a third illustrative embodiment of a memory device with an amplifier using a first type of device and a memory array using a second type of device; and

[0012] FIG. 4 is a flow diagram of a particular illustrative embodiment of a method of operating a memory device with an amplifier using a first type of device and a memory array using a second type of device.

V. Detailed Description

[0013] Referring to FIG. 1, a diagram of a particular illustrative embodiment of a memory device with an amplifier using a first type of device and a memory array using a second type of device is depicted and generally designated 100. The memory device 100 may include a memory array 102 using core devices. In a particular embodiment, the core devices may operate at core supply voltages V_{core} of up to about 1 volt (V). The memory array 102 may be coupled by bit lines 104 to a bit line logic circuit 106. The memory array 102 may be coupled by word lines 108 to a word line logic circuit 110. The bit line logic circuit 106 and the word line logic circuit 110 may be coupled to a core supply voltage V_{core} , as indicated at 114, and to ground, as indicated at 116. The memory array 102 may also be coupled to an amplifier 112 that

uses non-core devices. In a particular embodiment, the non-core devices may operate at input-output (IO) supply voltages V_{amp} of up to about 1.8V. The amplifier 112 may be coupled to an IO supply voltage V_{amp} , as indicated at 118. The amplifier 112 may include a clamp 120 coupled to the memory array 102 to keep an operating voltage V_{op} supplied to the memory array 102 by the amplifier 112 below a voltage limit V_{limit} .

[0014] By employing a higher supply voltage V_{amp} and high-voltage-tolerant input-output (IO) devices for transistors in the sense amplifier 112 while continuing to use area-efficient core devices in the memory array 102, for example, for MRAM bit cell transistors, such as access transistors and MUX transistors, read performance may be improved while maintaining a high array density. Since high-voltage-tolerant IO devices use a thicker gate oxide, their minimum feature size is also higher than that of core devices, which implies a higher area impact. As illustrated, the system 100 provides an improvement in the read performance (the output swing) of the MRAM sense amplifier 112 without much of an area penalty for the complete memory device 100 because (1) the higher supply voltage results in a greater output swing, thus, considerably improving the read performance, and (2) high-voltage-tolerant IO devices may be used only in the sense amplifier 112, while the MRAM bit cells that constitute a much larger portion of the memory device 100 area use high-density core devices. Since the number of sense amplifiers 112 on a memory chip is far less than the number of bit cells, the area penalty that comes from using high-voltage-tolerant IO devices for the clamp and PMOS load transistors in the sense amplifier 112 may be minor compared to the significantly improved read performance that is associated with the use of the higher supply voltage.

[0015] Referring to FIG. 2, a diagram of a second illustrative embodiment of a memory device with an amplifier using a first type of device and a memory array using a second type of device is depicted and generally designated 200. In a particular embodiment, the memory device 200 operates substantially similarly to the memory device 100 illustrated in FIG. 1. The memory device 200 may include a memory (or data storage) cell 226 that may include a resistance-based memory element 228 coupled to an access transistor 230. The access transistor 230 may have a first oxide thickness to enable operation of the memory cell 226 at an operating voltage V_{op} . In a particular embodiment, the memory cell 226 may be a spin-transfer torque magnetoresistive

random access memory (STT-MRAM) cell. The memory cell 226 may be included in a memory array 204. The memory device 200 may also include a first amplifier 202 configured to couple the memory cell 226 to a supply voltage V_{amp} at a supply terminal 206, where the supply voltage V_{amp} is greater than a voltage limit V_{limit} , to generate a data signal based on a current through the memory cell 226. The first amplifier 202 may include a first clamp transistor 218 that has a second oxide thickness that is greater than the first oxide thickness of the access transistor 230. The clamp transistor 218 may be configured to prevent the operating voltage V_{op} at the memory cell 226 from exceeding the voltage limit V_{limit} . By providing an appropriate clamp control voltage V_{clamp} at a control terminal 208 to protect the memory array 204 from voltages exceeding V_{limit} , the memory array 204 may use smaller devices for higher density and smaller sizes. In addition, the first amplifier 202 may use more robust devices to enhance operation using a larger supply voltage V_{amp} .

[0016] In a particular embodiment, the access transistor 230 may have a core device configuration and the first clamp transistor 218 may have an input-output (IO) device configuration. In these particular embodiments, the first clamp transistor 218 may be configured to operate at an input-output (IO) supply voltage, V_{amp} , and the access transistor 230 may be configured to operate at a core supply voltage, V_{core} . In these particular embodiments, the core supply voltage V_{core} may be approximately 1V, and the IO supply voltage V_{amp} may be approximately 1.8V. In a particular embodiment, the access transistor 230 may have the core device configuration with the first oxide thickness in a range from about 1nm to about 3nm. In these particular embodiments, the first clamp transistor 218 may have the input-output (IO) device configuration with the second oxide thickness in a range from about 3.5nm to about 10nm.

[0017] A data read path 210 may include a first load device 212 that may include a first load transistor 214. In a particular embodiment, the first load transistor 214 may be a PMOS load transistor. The first load device 212 may be coupled to a first clamp device 216 that may include the first clamp transistor 218, where the first load transistor 214 may be coupled to the first clamp transistor 218. The first clamp transistor 218 may be coupled to the control terminal 208 that may be biased with the clamp voltage V_{clamp} . The first clamp device 216 may be coupled through a first node 220 to a first selection switch device 222 that may include a first MUX

transistor 224, where the first clamp transistor 218 may be coupled to the first MUX transistor 224. The first selection switch device 222 may be included in the memory array 204. The first selection switch device 222 may be coupled to the memory cell 226, where the first MUX transistor 224 may be coupled to the access transistor 230 via the resistance-based memory element 228 having a resistance R_d . In a particular embodiment, the resistance-based memory element 228 may include a magnetic tunnel junction (MTJ) that may include a reference layer 232, a tunneling layer 234, and a free layer 236. The access transistor 230 may be coupled to ground.

[0018] A first reference path 240 may include a second load device 242 that may include a second load transistor 244. In a particular embodiment, the second load transistor 244 may be a PMOS load transistor. The second load device 242 may be coupled to a second clamp device 246 that may include a second clamp transistor 248, where the second load transistor 244 may be coupled to the second clamp transistor 248. The second clamp transistor 248 may be coupled to the control terminal 208 that may be biased with the clamp voltage V_{clamp} . The second clamp device 246 may be coupled through a second node 250 to a second selection switch device 252 that may include a second MUX transistor 254, where the second clamp transistor 248 may be coupled to the second MUX transistor 254. The second selection switch device 252 may be included in the memory array 204. The second selection switch device 252 may be coupled to a first reference cell 256, where the second MUX transistor 254 may be coupled to a first reference access transistor 260 via a first resistance-based reference element 258 having a resistance R_1 . In a particular embodiment, the resistance-based memory element 258 may include a magnetic tunnel junction (MTJ). The first reference access transistor 260 may be coupled to ground.

[0019] A second reference path 270 may include a third load device 272 that may include a third load transistor 274. In a particular embodiment, the third load transistor 274 may be a PMOS load transistor. The third load device 272 may be coupled to a third clamp device 276 that may include a third clamp transistor 278, where the third load transistor 274 may be coupled to the third clamp transistor 278. The third clamp transistor 278 may be coupled to the control terminal 208 that may be biased with the clamp voltage V_{clamp} . The third clamp device 276 may be coupled through a second node 280 to a third selection switch device 282 that may include a third MUX

transistor 284, where the third clamp transistor 278 may be coupled to the third MUX transistor 284. The third selection switch device 282 may be included in the memory array 204. The third selection switch device 282 may be coupled to a second reference cell 286, where the third MUX transistor 284 may be coupled to a second reference access transistor 290 via a second resistance-based reference element 288 having a resistance R_0 . In a particular embodiment, the resistance-based memory element 288 may include a magnetic tunnel junction (MTJ). The second reference access transistor 290 may be coupled to ground.

[0020] The first amplifier 202 may include the first load transistor 214 coupled to the first clamp transistor 218 to generate the data signal. The first amplifier 202 may include the second load transistor 244 coupled to the second clamp transistor 248 and the third load transistor 274 coupled to the third clamp transistor 278. The second clamp transistor 248 and the third clamp transistor 278 may be configured to couple to the first reference cell 256 and to the second reference cell 286, respectively, to generate a reference signal. The first clamp transistor 218, the second clamp transistor 248, the third clamp transistor 278, the first load transistor 214, the second load transistor 244, and the third load transistor 274 may have an input-output (IO) device configuration. At least one transistor 230, 260, 290 of the memory cell 226, the first reference cell 256, and the second reference cell 286 may have a core device configuration. In a particular embodiment, the first MUX transistor 224, the second MUX transistor 254, and the third MUX transistor 284 may have the core device configuration.

[0021] As described above, the data read path 210 may include the first load device 212 coupled to the data storage cell 226 via the first clamp transistor 218. The first load device 212 may have a first device configuration to operate at a first supply voltage V_{amp} supplied at the supply terminal 206. In a particular embodiment, the first device configuration may be a non-core device configuration. In these particular embodiments, the first device configuration may be an input-output (IO) device configuration. The data storage cell 226 may include the access transistor 230 that may have a second device configuration to operate at an operating voltage V_{op} , at the node 220, that is not to exceed a voltage limit V_{limit} that is less than the first supply voltage V_{amp} . In a particular embodiment, the second device configuration may be a core device configuration. In these particular embodiments, the core device configuration may have

a smaller physical dimension than the non-core configuration. The control terminal 208 of the first clamp transistor 218 may be biased to prevent the voltage V_{op} at the data storage cell 226 from exceeding the voltage limit V_{limit} . In a particular embodiment, the voltage limit V_{limit} may be approximately 1V.

[0022] As described above, the first reference path 240 may include the second load device 242 coupled to the first reference cell 256 and the second reference path 270 may include the third load device 272 coupled to the second reference cell 286. The second load device 242 and the third load device 272 may have the first device configuration. The first reference cell 256 and the second reference cell 286 each may include at least one transistor 260, 290 that may have the second device configuration. The second clamp transistor 248 may prevent a second voltage at the first reference cell 256 from exceeding the voltage limit V_{limit} . The third clamp transistor 278 may prevent a third voltage at the second reference cell 286 from exceeding the voltage limit V_{limit} . The first selection switch device 222 in the data read path 210 may selectively couple the data storage cell 226 to the first clamp transistor 218. The second selection switch device 252 in the first reference path 240 may selectively couple the first reference cell 256 to the second clamp transistor 248. The third selection switch device 282 in the second reference path 270 may selectively couple the second reference cell 286 to the third clamp transistor 278. Each of the first selection switch device 222, the second selection switch device 252, and the third selection switch device 282 may have the second device configuration.

[0023] Referring to FIG. 3, a diagram of a third illustrative embodiment of a memory device with an amplifier using a first type of device and a memory array using a second type of device is depicted and generally designated 300. In a particular embodiment, the memory device 300 operates substantially similarly to the memory device 100 illustrated in FIG. 1 and to the memory device 200 illustrated in FIG. 2. The memory device 300 may include a plurality of memory (or data storage) cells 326 that may each include a resistance-based memory element 328 coupled to an access transistor 330. The access transistor 330 may have a first oxide thickness to enable operation of the memory cells 326 at an operating voltage V_{op} . In a particular embodiment, the memory cells 326 may be spin-transfer torque magnetoresistive random access memory (STT-MRAM) cells. The memory cells 326 may be included in a memory array 304.

The memory device 300 may also include a first amplifier stage 302 configured to couple the memory cells 326 to a high supply voltage V_{amp} , where the supply voltage V_{amp} is greater than a voltage limit V_{limit} , to generate a data signal based on a current through one of the memory cells 326. The first amplifier stage 302 may include a first clamp transistor 318 that has a second oxide thickness that is greater than the first oxide thickness of the access transistor 330. The first clamp transistor 318 may be configured to prevent the operating voltage V_{op} at the memory cells 326 from exceeding the voltage limit V_{limit} . In a particular embodiment, the first clamp transistor 318 may be an NMOS transistor having a non-core device configuration.

[0024] In a particular embodiment, the access transistor 330 may have a core device configuration and the first clamp transistor 318 may have an input-output (IO) device configuration. In these particular embodiments, the first clamp transistor 318 may be configured to operate at an input-output (IO) supply voltage, V_{amp} , and the access transistor 330 may be configured to operate at a core supply voltage, V_{core} . In these particular embodiments, the core supply voltage V_{core} may be within a range from about 0.9V to about 1.2V, such as approximately 1V, and the IO supply voltage V_{amp} may be within a range from about 1.5V to about 2.0V, such as approximately 1.8V.

[0025] The first amplifier stage 302 may be further configured to couple at least one reference cell 356, 386 to the supply voltage V_{amp} to generate a reference signal. The memory device 300 may include a second amplifier stage 312 coupled to the first amplifier stage 302. The second amplifier stage 312 may be configured to provide an output signal V_{out} at terminal 316 based on a difference between the data signal and the reference signal. The second amplifier stage 312 may include at least one transistor that has the first oxide thickness of the access transistors 330 and that is coupled to a second supply voltage V_2 that does not exceed the voltage limit V_{limit} .

[0026] The memory array 304 may include a plurality of MUX transistors 324, M_0 , M_1 , ..., M_i , corresponding to the plurality of the memory cells 326 on the respective plurality of bit lines 104 (FIG. 1). In a particular embodiment, the MUX transistors 324 may be NMOS transistors having a core device configuration. Each of the plurality of MUX transistors 324, M_0 , M_1 , ..., M_i , may couple a corresponding one of the plurality of the memory cells 326 to the first clamp transistor 318, providing one of a plurality of data read paths 310.

[0027] Each of the data read paths 310 may include a first load transistor 314. In a particular embodiment, the first load transistor 314 may be a PMOS load transistor. The first load transistor 314 may be coupled to the first clamp transistor 318. The first clamp transistor 318 may be coupled to a control terminal 308 that may be biased with a clamp voltage V_{clamp} . The first clamp transistor 318 may be coupled to the MUX transistors 324. The MUX transistors 324 may be coupled to the access transistors 330 via the resistance-based memory elements 328 of the corresponding memory cells 326. The resistance-based memory elements 328 may each include a magnetic tunnel junction (MTJ) illustrated as a resistance R_{bit} , which may include a logic “0” or logic “1” resistance value. The access transistors 330 may be coupled to ground. The gates of the access transistors 330 may be coupled to one of the plurality of word lines 108 (FIG. 1). In a particular embodiment, the access transistors 330 may be NMOS transistors having a core device configuration.

[0028] A first reference path 340 may include a second load transistor 344. In a particular embodiment, the second load transistor 344 may be a diode-connected PMOS load transistor. The second load transistor 344 may be coupled to a second clamp transistor 348. The second clamp transistor 348 may be coupled to the control terminal 308 that may be biased with the clamp voltage V_{clamp} . In a particular embodiment, the second clamp transistor 348 may be an NMOS transistor having a non-core device configuration. The second clamp transistor 348 may be coupled to a MUX transistor 354. The MUX transistor 354 may be included in the memory array 304. In a particular embodiment, the MUX transistor 354 may be an NMOS transistor having a core device configuration. The gate of the MUX transistor 354 may be coupled to a voltage supply having a voltage V_{ddcx} that is less than a core device voltage limit. The MUX transistor 354 may be coupled to a first reference cell 356, where the MUX transistor 354 may be coupled to a first reference access transistor 360 via a first resistance-based reference element 358 having a resistance R_0 . In a particular embodiment, the resistance-based memory element 358 may include a magnetic tunnel junction (MTJ). The first reference access transistor 360 may be coupled to ground. The gate of the first reference access transistor 360 may be coupled to a word line 322, such as one of the plurality of word lines 108 depicted in FIG. 1. In a particular embodiment, the first reference access transistor 360 may be an NMOS transistor having a core device configuration.

[0029] A second reference path 370 may include a third load transistor 374. In a particular embodiment, the third load transistor 374 may be a PMOS load transistor. The third load transistor 274 may be coupled to a third clamp transistor 278. The third clamp transistor 278 may be coupled to the control terminal 208 that may be biased with the clamp voltage V_{clamp} . In a particular embodiment, the third clamp transistor 378 may be an NMOS transistor having a non-core device configuration. The third clamp transistor 278 may be coupled to a MUX transistor 384. The MUX transistor 384 may be included in the memory array 304. In a particular embodiment, the MUX transistor 384 may be an NMOS transistor having a core device configuration. The gate of the MUX transistor 384 may be coupled to the gate of the MUX transistor 354 and may also be coupled to a voltage supply having a voltage V_{ddcx} . The MUX transistor 384 may be coupled to a second reference cell 386, where the MUX transistor 384 may be coupled to a second reference access transistor 390 via a second resistance-based reference element 388 having a resistance R_1 . In a particular embodiment, the resistance-based memory element 358 may include a magnetic tunnel junction (MTJ). The second reference access transistor 390 may be coupled to ground. The gate of the second reference access transistor 390 may be coupled to one of the plurality of word lines 108 (FIG. 1). In a particular embodiment, the second reference access transistor 390 may be an NMOS transistor having a core device configuration.

[0030] The first amplifier stage 302 may include the first load transistor 314 coupled to the first clamp transistor 318 to generate the data signal. The first amplifier stage 302 may include the second load transistor 344 coupled to the second clamp transistor 348 and the third load transistor 374 coupled to the third clamp transistor 378. The second clamp transistor 348 and the third clamp transistor 378 may be configured to couple to the first reference cell 356 and to the second reference cell 386, respectively, to generate the reference signal. The second amplifier stage 312 may be coupled to each of the read data paths 310, the first reference path 340, and the second reference path 370. The second amplifier stage 312 may be configured to provide an output signal V_{out} at terminal 316 based on a difference between the data signal and the reference signal. The first clamp transistor 318, the second clamp transistor 348, the third clamp transistor 378, the first load transistor 314, the second load transistor 344, and the third load transistor 374 may have an input-output (IO) device configuration. At least one of the transistors 330, 360, 390 of the memory cells 326, the first reference cell 356, and

the second reference cell 386 may have a core device configuration. In a particular embodiment, the MUX transistors 324, the MUX transistor 354, and the MUX transistor 384 may have the core device configuration. The second amplifier stage 312 may include at least one transistor that has the core device configuration and that is coupled to the second supply voltage V_2 that does not exceed the voltage limit V_{limit} .

[0031] As described above, each of the data read paths 310 may include the first load transistor 314 coupled to the memory cells 326 via the first clamp transistor 318. The first load transistor 314 may have a first device configuration to operate at a first supply voltage V_{amp} . In a particular embodiment, the first device configuration may be a non-core device configuration. In these particular embodiments, the first device configuration may be an input-output (IO) device configuration. The memory cells 326 may include the access transistors 330 that may have a second device configuration to operate at an operating voltage V_{op} that is not to exceed a voltage limit V_{limit} that is less than the first supply voltage V_{amp} . In a particular embodiment, the second device configuration may be a core device configuration. In these particular embodiments, the core device configuration may have a smaller physical dimension than the non-core configuration. The control terminal 308 of the first clamp transistor 318 may be biased to prevent the voltage V_{op} at the memory cells 326 from exceeding the voltage limit V_{limit} . In a particular embodiment, the voltage limit V_{limit} may be approximately 1V.

[0032] As described above, the first reference path 340 may include the second load transistor 344 coupled to the first reference cell 356 and the second reference path 370 may include the third load transistor 374 coupled to the second reference cell 386. The second load transistor 344 and the third load transistor 374 may have the first device configuration. The first reference cell 356 and the second reference cell 386 each may include at least one transistor 360, 390 that may have the second device configuration. The second clamp transistor 348 may prevent a second voltage at the first reference cell 356 from exceeding the voltage limit V_{limit} . The third clamp transistor 378 may prevent a third voltage at the second reference cell 386 from exceeding the voltage limit V_{limit} . The MUX transistors 324 in the data read paths 310 may selectively couple the memory cells 326 to the first clamp transistor 318. The MUX transistor 354 in the first reference path 340 may be biased to couple the first reference cell 356 to the second clamp transistor 348. The MUX transistor 384 in the second reference path 370 may be

biased to couple the second reference cell 386 to the third clamp transistor 378. Each of the MUX transistors 324, 354, 384 may have the second device configuration.

[0033] Referring to FIG. 4, a flow diagram of a particular illustrative embodiment of a method of operating a memory device with an amplifier using a first type of device and a memory array using a second type of device is depicted and generally designated 400. At 402, a first amplifier stage may be coupled to a memory array. The first amplifier stage may include transistors having an input-output (IO) supply voltage tolerance. The memory array may include transistors having a core supply voltage tolerance that is less than the IO supply voltage tolerance. In a particular embodiment, the first amplifier stage may be the amplifier 112 and the memory array may be the memory array 102 of FIG. 1. In another particular embodiment, the first amplifier stage may be the first amplifier 202 and the memory array may be the memory array 204 of FIG. 2. In another particular embodiment, the first amplifier stage may be the first amplifier stage 302 and the memory array may be the memory array 304 of FIG. 3.

[0034] Continuing to 404, a control voltage may be applied at a clamp transistor coupled to the memory array to set a memory array voltage, such that the memory array voltage is less than the core supply voltage tolerance. For example, the control voltage V_{clamp} may be applied at the clamp transistors 218, 248, and 278 coupled to the memory array 204 to set the voltage at the nodes 220, 250, and 280 such that the memory array voltage is less than the core supply voltage tolerance, such as illustrated in FIG. 2. In a particular embodiment, the control voltage V_{clamp} may be applied at a clamp transistor 318, 348, 378 coupled to the memory array 304 to set a memory array voltage V_{op} (FIG. 1) such that the memory array voltage V_{op} is less than the core supply voltage tolerance V_{limit} , such as illustrated in FIG. 3. One consequence of not controlling V_{clamp} is that the memory array voltage may exceed the core supply voltage tolerance causing the core devices in the memory array to fail.

[0035] Moving to 406, a data read operation may be performed at a data storage cell of the memory array to generate a data signal at the first amplifier. In a particular embodiment, the data read operation may be performed at a data storage cell 226 of the memory array 204 to generate a data signal at the first amplifier 202 using the read data path 210, such as illustrated in FIG. 2. In a particular embodiment, the data read operation may be performed at one of the memory cells 326 of the memory array 304 to

generate a data signal at the first amplifier stage 302 using one of the read data paths 310, such as illustrated in FIG. 3.

[0036] Advancing to 408, the data signal from the first amplifier stage may be compared to a reference signal to generate an output signal at a second amplifier stage. The second amplifier stage may include devices having the core supply voltage tolerance. In a particular embodiment, the data signal from the first amplifier stage 302 may be compared to a reference signal to generate an output signal V_{out} at the second amplifier stage 312, the reference signal being generated using the first reference path 340 and the second reference path 370, such as illustrated in FIG. 3. In a particular embodiment, the second amplifier stage 312 may include devices having the core supply voltage tolerance, such as illustrated in FIG. 3.

[0037] In a particular embodiment, the data storage cell may be coupled to the first clamp transistor via a selection transistor to enable a current flow from a voltage supply of the first amplifier through the data storage cell. For example, the data storage cell 226 may be coupled to the first clamp transistor 218 via a selection transistor such as the first MUX transistor 224 to enable a current flow from the voltage supply 206 of the first amplifier 202 through the data storage cell 226, such as illustrated in FIG. 2. As another example, one of the memory cells 326 may be coupled to the first clamp transistor 318 via a selection transistor such as a respective one of the MUX transistors 324 to enable a current flow from the voltage supply of the first amplifier stage 302 through the corresponding one of the memory cells 326, such as illustrated in FIG. 3. In these particular embodiments, the selection transistor such as the first MUX transistor 224 and/or the MUX transistors 324 may have the core supply voltage tolerance V_{limit} . In these particular embodiments, increasing the voltage supply V_{amp} of the first amplifier 202 and/or the first amplifier stage 302 increases a read margin of the data read operation.

[0038] Those of skill would further appreciate that the various illustrative logical blocks, configurations, modules, circuits, and algorithm steps described in connection with the embodiments disclosed herein may be implemented as electronic hardware, computer software, or combinations of both. Skilled artisans may implement the described functionality in varying ways for each particular application, but such

implementation decisions should not be interpreted as causing a departure from the scope of the present disclosure.

[0039] The steps of a method or algorithm described in connection with the embodiments disclosed herein may be embodied directly in hardware, in a software module executed by a processor, or in a combination of the two. A software module may reside in random access memory (RAM), flash memory, read-only memory (ROM), programmable read-only memory (PROM), erasable programmable read-only memory (EPROM), electrically erasable programmable read-only memory (EEPROM), registers, hard disk, a removable disk, a compact disk read-only memory (CD-ROM), or any other form of storage medium known in the art. An exemplary storage medium is coupled to the processor such that the processor can read information from, and write information to, the storage medium. In the alternative, the storage medium may be integral to the processor. The processor and the storage medium may reside in an application-specific integrated circuit (ASIC). The ASIC may reside in a computing device or a user terminal. In the alternative, the processor and the storage medium may reside as discrete components in a computing device or user terminal.

[0040] The previous description of the disclosed embodiments is provided to enable any person skilled in the art to make or use the disclosed embodiments. Various modifications to these embodiments will be readily apparent to those skilled in the art, and the generic principles defined herein may be applied to other embodiments without departing from the scope of the disclosure. Thus, the present disclosure is not intended to be limited to the embodiments shown herein but is to be accorded the widest scope possible consistent with the principles and novel features as defined by the following claims.

WHAT IS CLAIMED IS:

1. A memory device, comprising:
a memory cell including a resistance-based memory element coupled to an access transistor, the access transistor having a first oxide thickness to enable operation of the memory cell at an operating voltage; and
a first amplifier configured to couple the memory cell to a supply voltage that is greater than a voltage limit to generate a data signal based on a current through the memory cell,
wherein the first amplifier includes a clamp transistor that has a second oxide thickness that is greater than the first oxide thickness, and wherein the clamp transistor is configured to prevent the operating voltage at the memory cell from exceeding the voltage limit.
2. The memory device of claim 1, wherein the access transistor has a core device configuration and wherein the clamp transistor has an input-output (IO) device configuration.
3. The memory device of claim 2, wherein the clamp transistor is configured to operate at an input-output (IO) supply voltage, and wherein the access transistor is configured to operate at a core supply voltage.
4. The memory device of claim 3, wherein the core supply voltage is approximately 1 volt, and wherein the IO supply voltage is approximately 1.8 volts.
5. The memory device of claim 1, wherein the memory cell is a spin-transfer torque magnetoresistive random access memory (STT-MRAM) cell.

6. The memory device of claim 1, wherein the first amplifier is further configured to couple at least one reference cell to the supply voltage to generate a reference signal, and further comprising:

a second amplifier coupled to the first amplifier and configured to provide an output signal based on a difference between the data signal and the reference signal, the second amplifier including at least one transistor that has the first oxide thickness and that is coupled to a second supply voltage that does not exceed the voltage limit.

7. The memory device of claim 1, wherein the first amplifier further comprises: a first load transistor coupled to the clamp transistor to generate the data signal; a second load transistor coupled to a second clamp transistor; and a third load transistor coupled to a third clamp transistor, wherein the second clamp transistor and the third clamp transistor are configured to couple to a first reference cell and to a second reference cell to generate a reference signal,

wherein the first clamp transistor, the second clamp transistor, the third clamp transistor, the first load transistor, the second load transistor, and the third load transistor have an input-output (IO) device configuration and wherein at least one transistor of each of the memory cell, the first reference cell, and the second reference cell has a core device configuration.

8. A memory device, comprising:

a data read path including a first load device coupled to a data storage cell via a first clamp transistor, the first load device having a first device configuration to operate at a first supply voltage, the data storage cell including an access transistor having a second device configuration to operate at a voltage not to exceed a voltage limit that is less than the first supply voltage, and wherein a control terminal of the first clamp transistor is biased to prevent the voltage at the data storage cell from exceeding the voltage limit.

9. The memory device of claim 8, wherein the second device configuration is a core device configuration and the first device configuration is a non-core device configuration.

10. The memory device of claim 9, wherein the first device configuration is an input-output (IO) device configuration.

11. The memory device of claim 9, wherein the core device configuration has a smaller physical dimension than the non-core device configuration.

12. The memory device of claim 8, wherein the voltage limit is approximately one volt.

13. The memory device of claim 8, further comprising:
a first reference path including a second load device coupled to a first reference cell; and
a second reference path including a third load device coupled to a second reference cell,
wherein the second load device and the third load device have the first device configuration and wherein the first reference cell and the second reference cell each include at least one transistor having the second device configuration.

14. The memory device of claim 13, further comprising:
a second clamp transistor to prevent a second voltage at the first reference cell from exceeding the voltage limit; and
a third clamp transistor to prevent a third voltage at the first reference cell from exceeding the voltage limit.

15. The memory device of claim 14, further comprising:
a first selection switch device in the data read path to selectively couple the data storage cell to the first clamp transistor;
a second selection switch device coupled between the second clamp transistor and the first reference cell; and
a third selection switch device coupled between the third clamp transistor and the second reference cell,
wherein each of the first selection switch device, the second selection switch device, and the third selection switch device have the second device configuration.

16. A method comprising:
coupling a first amplifier stage to a memory array, the first amplifier stage including transistors having an input-output (IO) supply voltage tolerance, the memory array including transistors having a core supply voltage tolerance that is less than the IO supply voltage tolerance; and
applying a control voltage at a clamp transistor coupled to the memory array to set a memory array voltage, such that the memory array voltage is less than the core supply voltage tolerance.

17. The method of claim 16, further comprising:
performing a data read operation at a data storage cell of the memory array to generate a data signal at the first amplifier stage; and
comparing the data signal from the first amplifier stage to a reference signal to generate an output signal at a second amplifier stage, the second amplifier stage including devices having the core supply voltage tolerance.

18. The method of claim 17, further comprising coupling the data storage cell to the clamp transistor via a selection transistor to enable a current flow from a voltage supply of the first amplifier stage through the data storage cell.

19. The method of claim 18, wherein the selection transistor has the core supply voltage tolerance.

20. The method of claim 18, wherein increasing the voltage supply of the first amplifier stage increases a read margin of the data read operation.

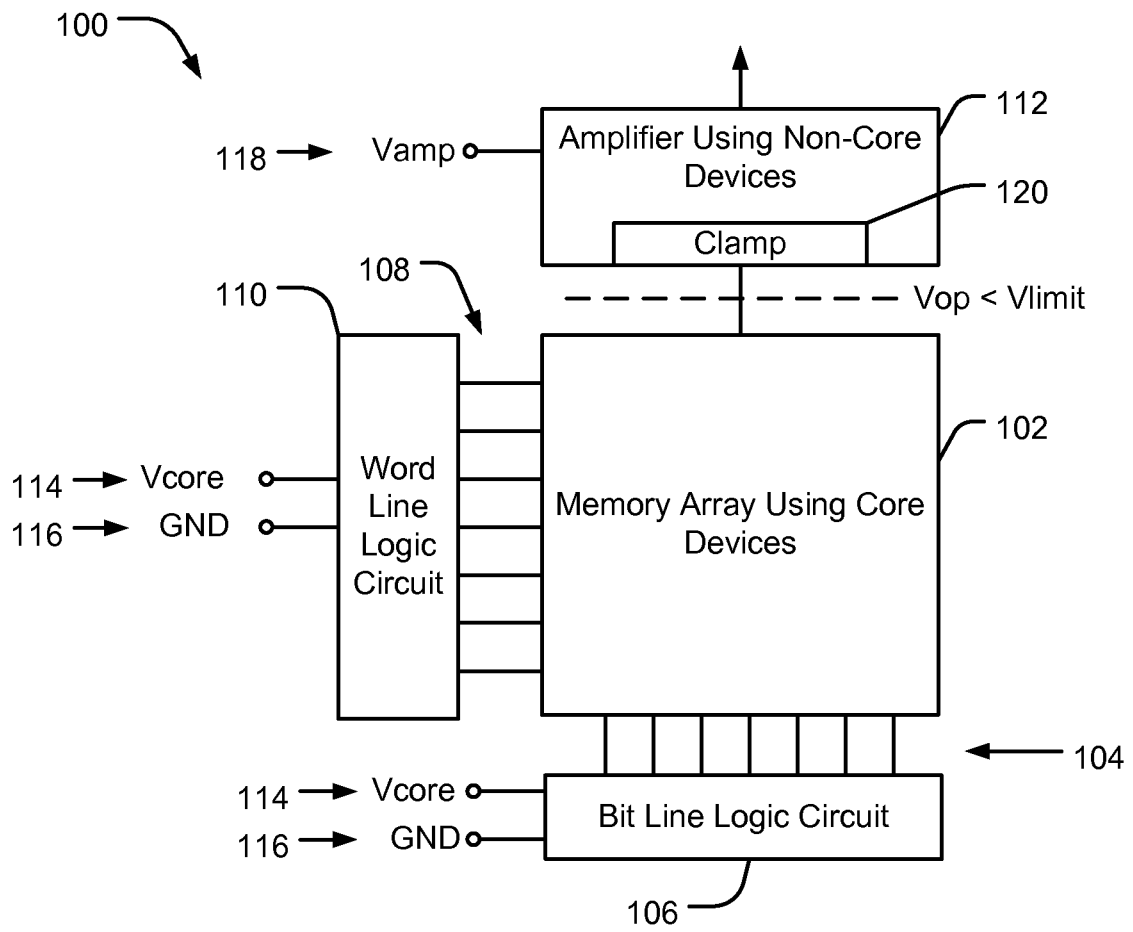


FIG. 1

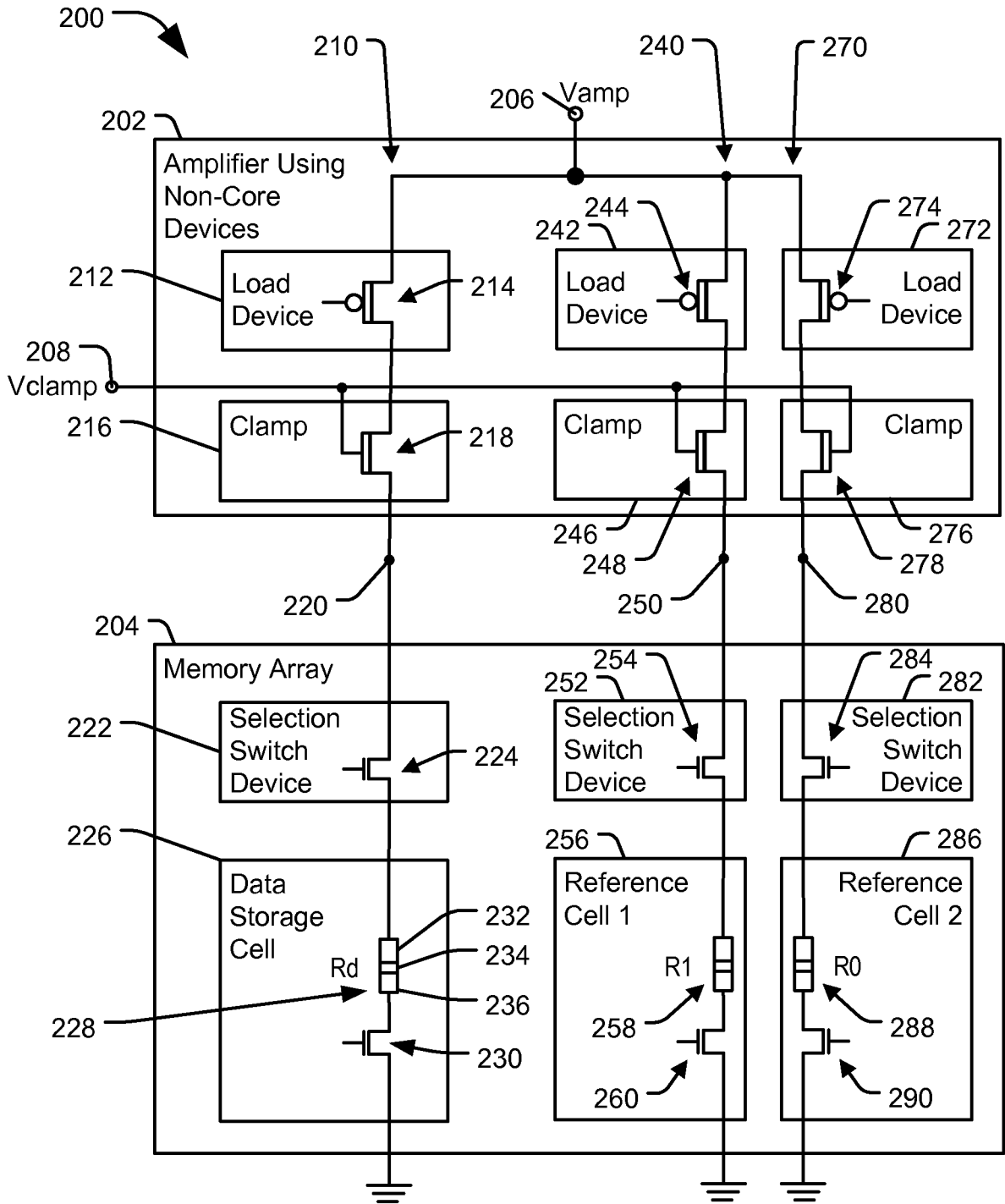
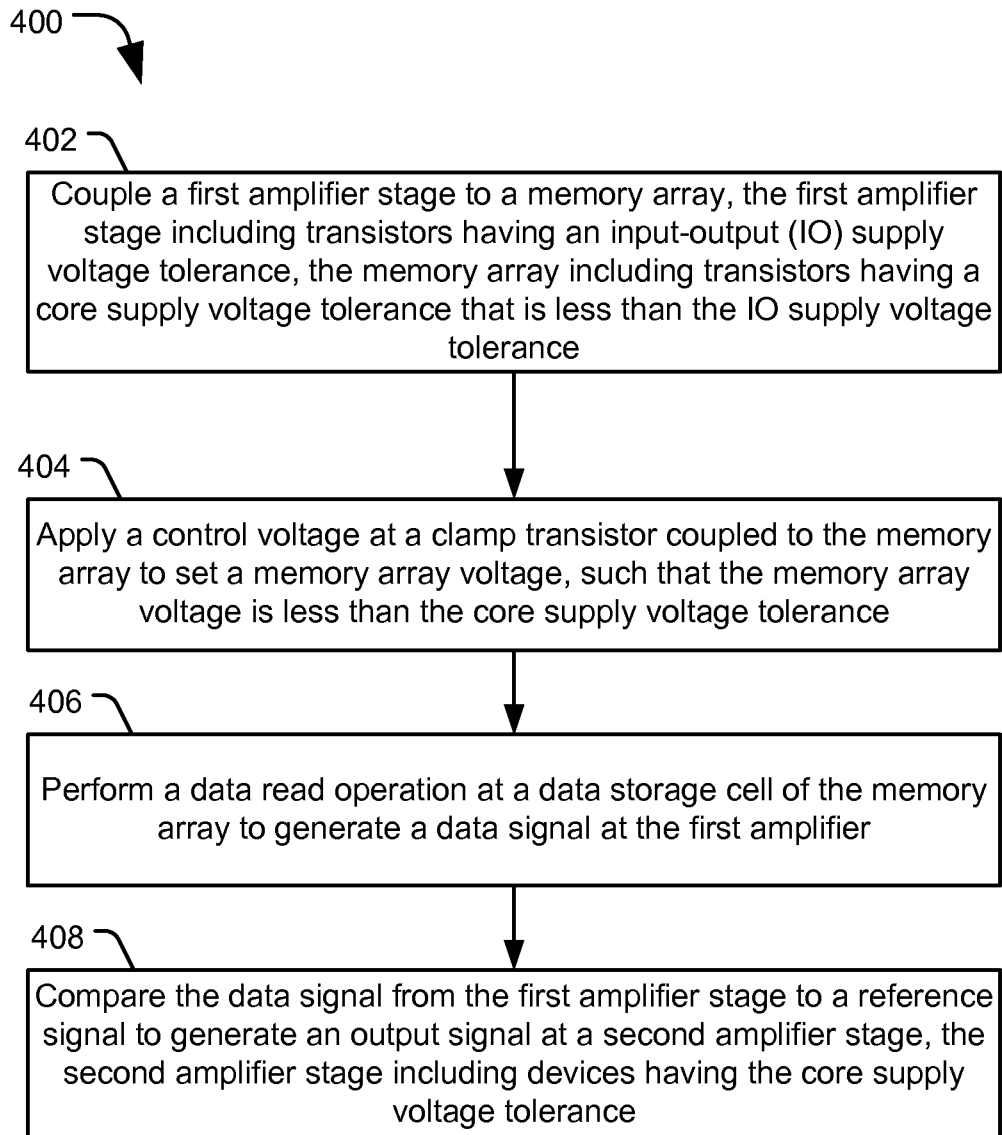


FIG. 2

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**FIG. 4**

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2009/055617A. CLASSIFICATION OF SUBJECT MATTER
INV. G11C7/06 G11C7/10 G11C7/12 G11C7/14 G11C11/16

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
G11C

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2008/137430 A1 (LASSEUGUETTE JEAN [FR]) 12 June 2008 (2008-06-12)	8, 13-14
A	paragraphs [0013] - [0030]; figures 3,4	1-7, 9-12, 15-20
A	----- US 7 272 035 B1 (CHEN EUGENE YOUJUN [US] ET AL) 18 September 2007 (2007-09-18) column 13, line 19 - column 14, line 40; figure 13	1-20
A	----- US 2004/125682 A1 (TAKASHIMA DAISABURO [JP]) 1 July 2004 (2004-07-01) the whole document	1-20

 Further documents are listed in the continuation of Box C. See patent family annex.

* Special categories of cited documents :

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X document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

Y document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

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Date of the actual completion of the international search

6 November 2009

Date of mailing of the international search report

16/11/2009

Name and mailing address of the ISA/

European Patent Office, P.B. 5818 Patentlaan 2
NL - 2280 HV Rijswijk
Tel. (+31-70) 340-2040,
Fax: (+31-70) 340-3016

Authorized officer

Trifonov, Antoniy

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/US2009/055617

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2008137430	A1	12-06-2008	NONE
US 7272035	B1	18-09-2007	NONE
US 2004125682	A1	01-07-2004	NONE