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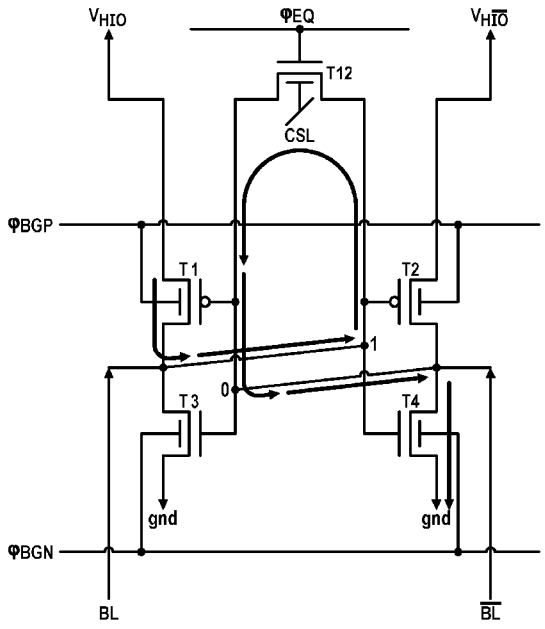
(54) Title: CIRCUIT AND METHOD FOR SENSING A DIFFERENCE IN VOLTAGE ON A PAIR OF DUAL SIGNAL LINES, IN PARTICULAR THROUGH EQUALIZE TRANSISTOR

FIG. 5



(57) Abstract: The invention relates to a circuit for sensing a difference in voltage on a pair of dual signal lines comprising a first signal line (BL) and a second signal line (/BL) complementary to the first signal line, comprising: - a pair of cross-coupled inverters arranged between the first and the second signal lines, each inverter having a pull-up transistor (T1, T2) and a pull-down transistor (T3, T4), the sources of the pull-up transistors or of the pull-down transistors being respectively connected to a first (V_{HIO}) and a second (V_{HIO}) pull voltage signals, - a decode transistor (T11, T12) having source and drain terminals respectively coupled to one of the first and second signal lines and a gate controlled by a decoding control signal (CSL), whereby when the decode transistor is turned on by the decoding control signal, a short circuit is established between the first and the second signal lines through which current flows from one of the first and second pull voltage signals, thereby generating a disturb in between the first and the second pull voltage signals.

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Circuit and method for sensing a difference in voltage on a pair of dual signal lines, in particular through equalize transistor

Field of the invention

The invention relates generally to a semiconductor circuit, such as semiconductor memory, for instance a Dynamic Random Access Memory (DRAM), and more particularly to a circuit for sensing a difference in voltage on a pair of dual signal lines, for instance a sense amplifier for sensing and amplifying data stored in a plurality of memory cells of a memory cell array.

Background of the invention

Basically, a DRAM is an integrated circuit that stores data in binary form (e.g., "1" or "0") in a large number of cells. The data is stored in a cell as a charge on a capacitor located within the cell. Typically, a high logic level is in general equal to the power supply voltage and a low logic level is in general equal to ground.

The cells of a conventional DRAM are arranged in an array so that individual cells can be addressed and accessed. The array can be thought of as rows and columns of cells. Each row includes a word line that interconnects cells on the row with a common control signal. Similarly, each column includes a bit line that is coupled to at most one cell in each row. Thus, the word and bit lines can be controlled so as to individually access each cell of the array.

To read data out of a cell, the capacitor of a cell is accessed by selecting the word line associated with the cell. A complementary bit line that is paired with the bit line for the selected cell is equilibrated to an equilibrium voltage. This equilibration voltage (Veq) is typically midway between the high Vdd and low Vss (typically ground) logic levels. Thus, conventionally, the bit lines are equilibrated to one-half of the power supply voltage, Vdd/2. When the word line is activated for the selected cell, the capacitor of the selected cell discharges the stored voltage onto the bit line, thus changing the voltage on the bit line. A differential amplifier, conventionally referred to as a sense amplifier, is then used to detect and amplify the difference in voltage on the pair of bit lines.

Figure 1 shows a conventional sense amplifier circuit which comprises ten transistors T1-T10 fabricated in bulk silicon CMOS technology. The sense amplifier comprises a pair of cross-coupled inverters arranged between the first bit line BL and the second bit line /BL complementary to the first bit line:

- a first CMOS inverter having an output connected to the bit line BL and an input connected to the complementary bit line /BL,

- a second CMOS inverter having an output connected to the complementary bit line /BL and an input connected to the bit line BL.

Each CMOS inverter comprises :

- a pull-up transistor T1, T2 having a drain and a source, and
- a pull-down transistor T3, T4 having a drain and a source,

the pull-up transistor T1, T2 and the pull-down transistor T3, T4 of each CMOS inverter having a common drain.

The sources of the pull-down transistors T3, T4 are connected to a foot switch transistor T5, which is itself connected to a pull-down voltage source providing a low supply voltage V_L usually at a low voltage level V_{BLL} referred to as ground GND, and controlled by a foot switch control signal “Sense”. The ground level of the low supply voltage $V_{Lsupply}$ is used as a reference for the other voltage levels in the sense amplifier. In the circuit illustrated by Fig. 1, the foot switch transistor T40 is an N-MOS transistor. When the foot switch control signal “Sense” is high, the foot switch transistor T5 is conducting, and the ground voltage is transmitted to the common source node of the pull-down transistors T3, T4. When the foot switch control signal “Sense” is low, the foot switch transistor T5 is blocked and the common source node of the pull-down transistors T3, T4 is not pulled down.

The sources of the pull-up transistors T21, T22 are connected to a pull-up voltage source providing a high supply voltage V_H usually at a high voltage level such as VDD.

The sense amplifier further comprises an equalization transistor T6 having its source/drain terminals respectively coupled to one of bit lines BL, /BL and having its gate controlled by an equalization control signal. The equalization transistor T50 of the circuit illustrated in Fig. 1 is an N-MOS type transistor.

The sense amplifier further comprises a pair of dedicated precharge transistors T7, T8 respectively coupled to the bit line BL and to the complementary bit line /BL and arranged to precharge the bit lines BL, /BL to a precharge voltage, usually at the mean value between the high supply voltage V_H and the low supply voltage V_L. This mean value is usually half the high supply voltage $V_{Hsupply}$ high value, i.e. $V_H/2$, since the low voltage level GND of the low supply voltage V_L is used as a reference for the other voltages and the high supply voltage V_H and low supply voltage V_{Ls} are usually then at their high and low voltage level, respectively. A precharge control signal ρ_{PCH} is applied to the gates of said precharge transistors T61, T62.

The sense amplifier further comprises two dedicated decode transistors T9, T10, the gates of which are controlled by a decoding control signal CSL. Each of the decode transistors T9, T10 connects one of the bit lines BL, /BL to a global bit line IO, /IO, also called

in-out line. The decode transistors T9, T10 are used to transfer data between the bit lines BL, /BL and the global bit lines IO, /IO.

Although sense amplifiers are technically necessary, from an economical point of view the sense amplifiers can be considered as service circuits of the memory array and therefore as overhead that increases the area of the entire circuit and thus also its cost of fabrication.

Therefore, continuous efforts are made to minimize the area consumption of such sense amplifiers.

Summary of the invention

The invention aims at proposing a simplified circuit for sensing a difference in voltage on a pair of dual signal lines. In this respect, the invention proposes according to its first aspect a circuit for sensing a difference in voltage on a pair of dual signal lines comprising a first signal line (BL) and a second signal line (/BL) complementary to the first signal line, comprising:

- a pair of cross-coupled inverters arranged between the first and the second signal lines, each inverter having a pull-up transistor (T1, T2) and a pull-down transistor (T3, T4), the sources of the pull-up transistors or of the pull-down transistors being respectively connected to a first (V_{HIO}) and a second ($V_{H/IO}$) pull voltage signals,
- a decode transistor (T11, T12) having source and drain terminals respectively coupled to one of the first and second signal lines and a gate controlled by a decoding control signal (CSL), whereby when the decode transistor is turned on by the decoding control signal, a short circuit is established between the first and the second signal lines through which current flows from one of the first and second pull voltage signals, thereby generating a disturb in between the first and the second pull voltage signals.

Other preferred, although non limitative, aspects of this circuit are as follows:

- the sources of the pull-up transistors are connected to the first and second pull up voltage signals;
- it further comprises a foot switch transistor intercalated between the sources of the pull-down transistors and a pull-down voltage source, the foot switch transistor being controlled by a sense signal;
- the decode transistor, the pull-up and the pull-down transistors are dual gate transistors;
- it is made on a semiconductor-on-insulator substrate comprising a thin layer of semiconducting material separated from a substrate by an insulating layer, and the

dual gate transistors each comprises a first and a second gate, one of which is a back gate formed in the substrate below the insulating layer;

- the decode transistor has a first gate controlled by the decoding control signal and a second gate controlled by an equalization control signal;
- the first gate of the decode transistor is a back gate;
- the first and second signal lines are bit lines of a memory cell array.

According to another aspect, the invention relates to a semiconductor memory comprising at least one array of memory cells and at least one circuit according to the first aspect of the invention.

According to yet another aspect, the invention relates to a method of operating a method for sensing a difference in voltage on a pair of dual signal lines comprising a first signal line and a second signal line complementary to the first signal line, comprising the steps of turning on the decode transistor of a circuit according to the first aspect of the invention, and of sensing the difference of current or of voltage between the pull voltage signals with a current sense amplifier or a voltage sense amplifier.

Brief description of the drawings

Other aspects, goals and advantages of the invention will become more apparent upon reading the following detailed description of preferred embodiments thereof, given by way of examples and with reference to the accompanying drawings upon which:

- figure 1, already described above, shows on conventional sense amplifier circuit;
- figure 2 shows a circuit according to a possible embodiment of the invention;
- figure 3 shows a sense amplifier circuit with dual gate transistors as previously proposed by the Applicant with no dedicated precharge transistors;
- figure 4 shows a circuit according to another embodiment of the invention, based on the design of figure 3;
- figure 5 shows a circuit according to yet another embodiment of the invention.

On these figures, functionally similar transistors have identical numerical references.

Detailed description of preferred embodiments of the invention

In its broader aspect, the invention relates to a new manner of sensing a difference in voltage on a pair of dual signal lines. Although it will be described here below in relation to a sense amplifier circuit and dual signal lines in the form of a bit line and a complementary bit

line, it is to be understood that the invention can be implemented on other circuits having dual signal lines, such as in bus drivers which have dual high speed busses (*signal* and */signal*).

In relation to figure 2, the invention proposes according to a first aspect a circuit for sensing a difference in voltage on a pair of dual signal lines comprising a first signal line and a second signal line complementary to the first signal line. In the exemplary embodiment of figure 2, the dual signal lines are bit lines of a memory cell array: a first bit line BL and a second bit line /BL complementary to the first bit line.

The sense circuit SC differs from the conventional sense amplifier of figure 1 in that it comprises a pair of cross-coupled inverters T1, T3; T2, T4 arranged between the first BL and the second /BL signal lines, each inverter having a pull-up transistor T1, T2 and a pull-down transistor T3, T4, the sources of the pull-up transistors or of the pull-down transistors being respectively connected to a first and a second pull voltage signals.

In the following description, the sources of the pull-up transistors T1, T2 are respectively connected to a first pull up voltage signal V_{HIO} and to a second pull up voltage signal $V_{H/IO}$. It will be understood that the invention also works with the symmetrical counterpart circuit in which the sources of the pull-down transistors T3, T4 are respectively connected to a first pull down voltage signal V_{LIO} and to a second pull voltage signal $V_{L/IO}$.

The sense circuit SC of figure 2 further differs from the conventional sense amplifier of figure 1 in that the conventional decode transistors T9, T10 of figure 1 are suppressed. Instead the sense circuit SC comprises a decode transistor T11 having source and drain terminals respectively coupled to one of the first BL and second /BL signal lines and a gate controlled by a decoding control signal CSL.

Hence when the decode transistor 11 is turned on by the decoding control signal CSL, a short circuit is established between the first BL and the second /BL signal lines through which current flows from one of the first V_{HIO} and second $V_{H/IO}$ pull voltage signals, thereby generating a disturb in between the first V_{HIO} and the second $V_{H/IO}$ pull voltage signals.

Considering the first bit line at “1”, then a current path is established as shown by the arrows on figure 2. Current flows through the first pull voltage signal V_{HIO} (T1 is in the ON state) while nothing happens on the second pull voltage signal $V_{H/IO}$ (T2 is in the OFF state). Of course situation is opposite if the first bit line at “0.

The two pull voltage signals two signals act as power supply but also as current sources (IO (Input/Output) lines) during decoding (when decode circuit is ON). A secondary current sense amplifier can thereby sense the difference of current between these two IO lines.

The difference of current generates a voltage drop on the corresponding pull voltage signal (V_{HIO} in the example of figure 2). Hence, provided the output impedances of the voltage sources V_{HIO}, $V_{H/IO}$ is high enough, the difference of voltage can be sensed by a secondary voltage sense amplifier.

Compared to the circuit of figure 1, it will be appreciated that the circuit of figure 2 has a lesser number of transistors (1 transistor on bulk technology) which proves advantageous in that less interconnections are needed, thereby minimizing the area consumption.

Further advantageously, the decode transistor T11 can be either a N or a P transistor, at the convenience of the circuit designer (the phase of the decoding signal CSL being arranged appropriately).

Turning now to figure 3, an exemplary embodiment of a sense amplifier circuit with dual gate transistors, as described in the French patent application n° 1153574 filed by the Applicant on April 26, 2011 and not yet published, is represented.

The sense amplifier of figure 3 is preferentially made on a semiconductor-on-insulator substrate comprising a thin layer of semiconducting material separated from a substrate by an insulating layer, and the second gates of the transistors are back gates formed in the substrate below the insulating layer.

According to another embodiment, each dual gate transistor is a Fin-type independent double gate transistor. According to yet another embodiment, each dual gate transistors is made of two single gate transistors arranged in parallel.

The circuit of figure 3 differs from the one of figure 1 in that the dedicated precharge transistors T7, T8 are suppressed, in that the pull-up transistors T1, T2 are each connected to a respective pull-up control signal V_{HIO} and $V_{H/IO}$, in that the pull-down transistors T3, T5 are directly grounded. In addition, while the first gates of the pull up and pull down transistors are connected to either the first signal line BL or the second signal line /BL, the second gates of the pull-up transistors T1, T2 are both controlled by a pull-up second gate control signal ρ_{BGP} and the second gates of the pull-down transistors are both controlled by a pull-down second gate control signal ρ_{BGN}.

Figure 4 shows a sense circuit according to another embodiment of the invention, based on the design of figure 3. It will be appreciated that a sense circuit according to the invention with dual gates transistors can be derived from any one of the proposed sense amplifiers described in French patent applications n°1153573, n° 1153574, n°1153575 filed by the Applicant on April 26, 2011 and not yet published.

As shown on figure 4, the decode transistors T9, T10 of figure 3 are suppressed. Instead the sense circuit comprises a decode transistor T11 having source and drain terminals respectively coupled to one of the first BL and second /BL signal lines and a gate controlled by a decoding control signal CSL.

Hence when the decode transistor 11 is turned on by the decoding control signal CSL, a short circuit is established between the first BL and the second /BL signal lines through which current flows (as shown by the arrows on figure 4 in the case the first bit line BL is at "1") from one of the first V_{HIO} and second $V_{H/IO}$ pull voltage signals, thereby generating a disturb in between the first V_{HIO} and the second $V_{H/IO}$ pull voltage signals.

The two pull-up voltage signals act as power supply but also as current sources (IO (Input/Output) lines) during decoding (when decode circuit is ON). A secondary current sense amplifier can thereby sense the difference of current between these two IO lines. The difference of current generates a voltage drop on the corresponding pull voltage signal (V_{HIO} in the example of figure 2). Hence, provided the output impedances of the voltage sources V_{HIO}, $V_{H/IO}$ is high enough, the difference of voltage can be sensed by a secondary voltage sense amplifier.

In the sense circuit of figure 4, both equalization transistor T6 and decode transistor T11 are used as single gated transistor (their second gate being merely grounded). In an advantageous variant of figure 4 represented on figure 5, a single dual gate transistor T12 is used for both equalization and decode functions. This transistor T12 has therefore a first gate controlled by the equalization control signal ρ_{EQ} and a second gate controlled by the decoding control signal CSL. It is to be noted that this advantageous variant is rendered possible if the circuit designer orientates one gate in a first direction (such as the x direction for the equalisation control signal) and the second gate perpendicularly to the first direction (such as the y direction for the decoding control signal. When working with SOI dual gate transistors, due to asymmetric gate oxide thickness, the second gate controlled by the decoding control signal CSL.is preferably the back gate.

It will be appreciated that the invention can be implemented on all technologies: bulk, PDSOI (Partially Depleted Silicon On Insulator), FDSOI (Fully Depleted Silicon On Insulator), as well as with FinFETs and other types of independent double gate transistors. FDSOI proves advantageous it that it enhances the advantages as it allows smaller area per functionality than bulk.

It will further be appreciated that the decode method proposed by the invention (making a temporary short circuit between dual signal lines and detecting the disturb) is not limited to sense amplifier circuits but can be used on many other circuits as long as they exhibit dual signal lines, such as for instance bus driver circuits or analog-to-digital converters.

It will further be appreciated that the invention is not limited to the sense circuit according to its first aspect, but also encompasses a semiconductor memory, in particular a DRAM memory, comprising at least one array of memory cells arranged in rows and columns and at least one sense circuit according to its first aspect arranged as a sense amplifier.

The invention also relates to the method of operating the sense circuit according to its first aspect for sensing a difference in voltage on a pair of dual signal lines comprising a first signal line and a second signal line complementary to the first signal line, the method comprising the steps of turning on the decode transistor of the sense, and of sensing the difference of current or of voltage between the pull voltage signals with a current sense amplifier or a voltage sense amplifier.

CLAIMS

1. A circuit for sensing a difference in voltage on a pair of dual signal lines comprising a first signal line (BL) and a second signal line (/BL) complementary to the first signal line, comprising:

- a pair of cross-coupled inverters arranged between the first and the second signal lines, each inverter having a pull-up transistor (T1, T2) and a pull-down transistor (T3, T4), the sources of the pull-up transistors or of the pull-down transistors being respectively connected to a first (V_{HIO}) and a second ($V_{H/IO}$) pull voltage signals,
- a decode transistor (T11, T12) having source and drain terminals respectively coupled to one of the first and second signal lines and a gate controlled by a decoding control signal (CSL), whereby when the decode transistor is turned on by the decoding control signal, a short circuit is established between the first and the second signal lines through which current flows from one of the first and second pull voltage signals, thereby generating a disturb in between the first and the second pull voltage signals.

2. Circuit according to claim 1, wherein the sources of the pull-up transistors are connected to the first and second pull up voltage signals.

3. Circuit according to claim 2, further comprising a foot switch transistor intercalated between the sources of the pull-down transistors and a pull-down voltage source, the foot switch transistor being controlled by a sense signal.

4. Circuit according to any one of the preceding claims, wherein the decode transistor, the pull-up and the pull-down transistors are dual gate transistors.

5. Circuit according to the preceding claim, made on a semiconductor-on-insulator substrate comprising a thin layer of semiconducting material separated from a substrate by an insulating layer, wherein the dual gate transistors each comprise a first and a second gate, one of which is a back gate formed in the substrate below the insulating layer.

6. Circuit according to one of claims 4 or 5, wherein the decode transistor has a first gate controlled by the decoding control signal and a second gate controlled by an equalization control signal.

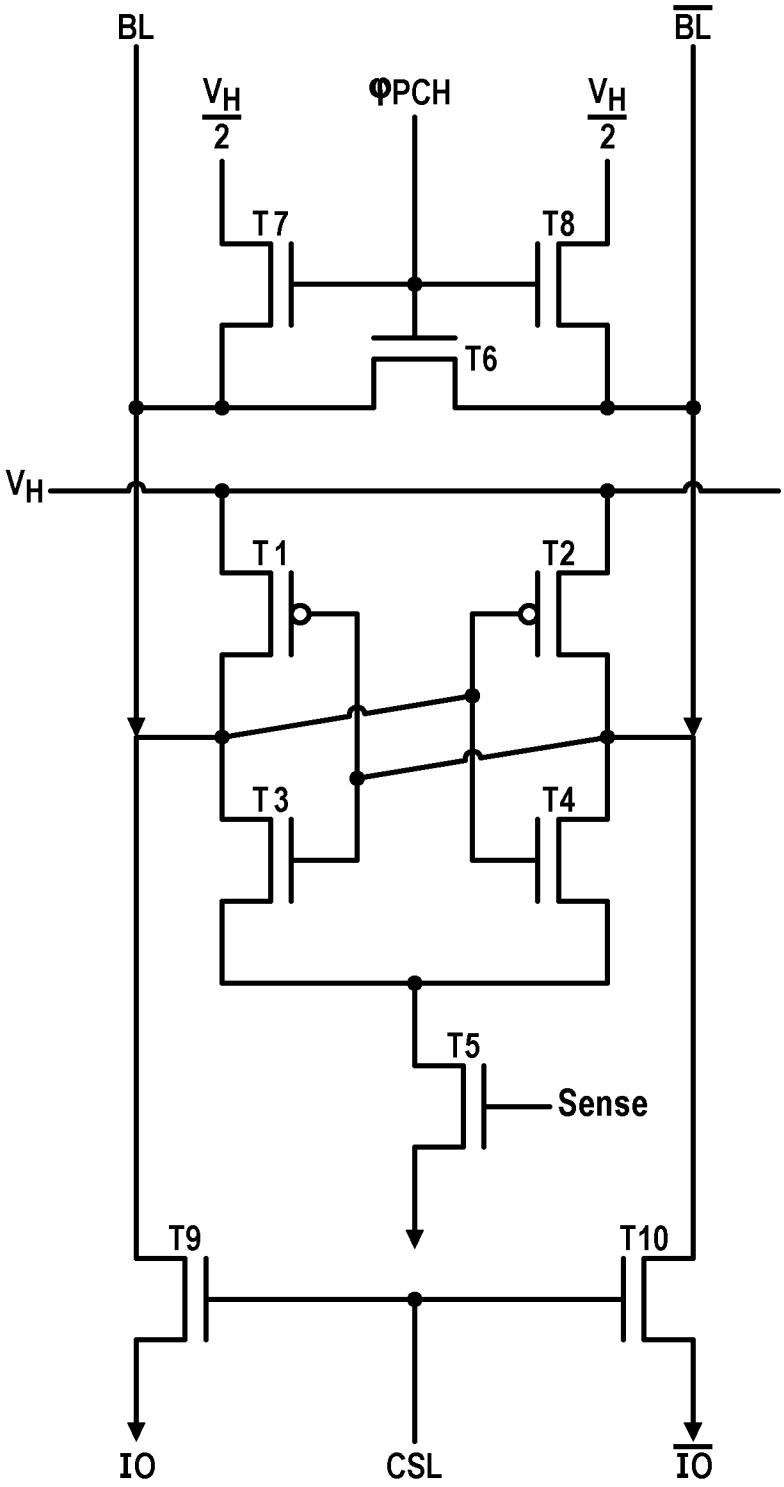
7. Circuit according to claim 6 when dependent upon claim 5, wherein the first gate of the decode transistor is a back gate.

8. Circuit according to any one of the preceding claims, wherein the first and second signal lines are bit lines of a memory cell array.

9. A semiconductor memory, comprising at least one array of memory cells and at least one circuit according to claim 8.

10. A method for sensing a difference in voltage on a pair of dual signal lines comprising a first signal line and a second signal line complementary to the first signal line, comprising the steps of turning on the decode transistor of a circuit according to any one of claims 1-7, and of sensing the difference of current or of voltage between the pull voltage signals with a current sense amplifier or a voltage sense amplifier.

FIG. 1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T7
T8
T6
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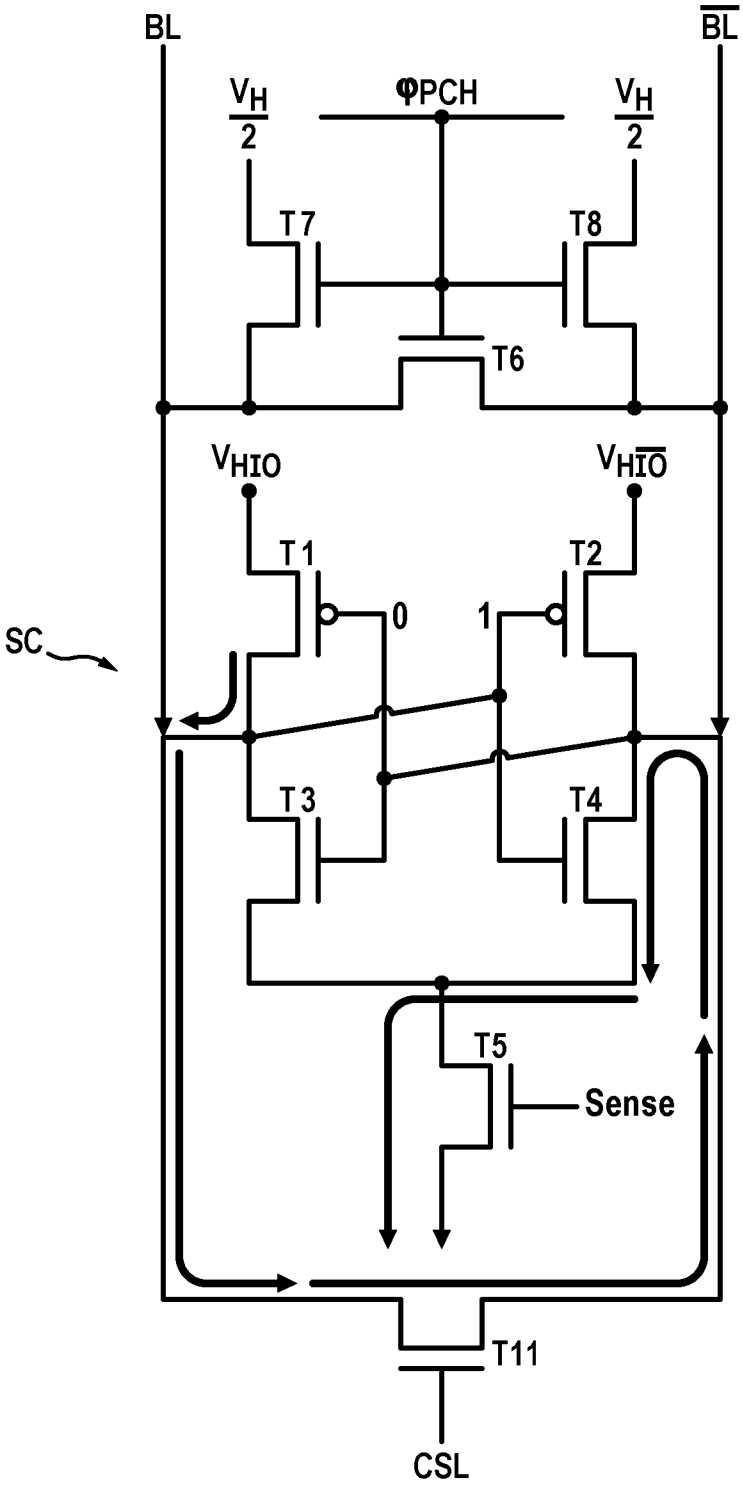
T4
T5
Sense
T9
T10
IO
CSL
$\overline{IO}$

FIG. 2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T11
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FIG. 3

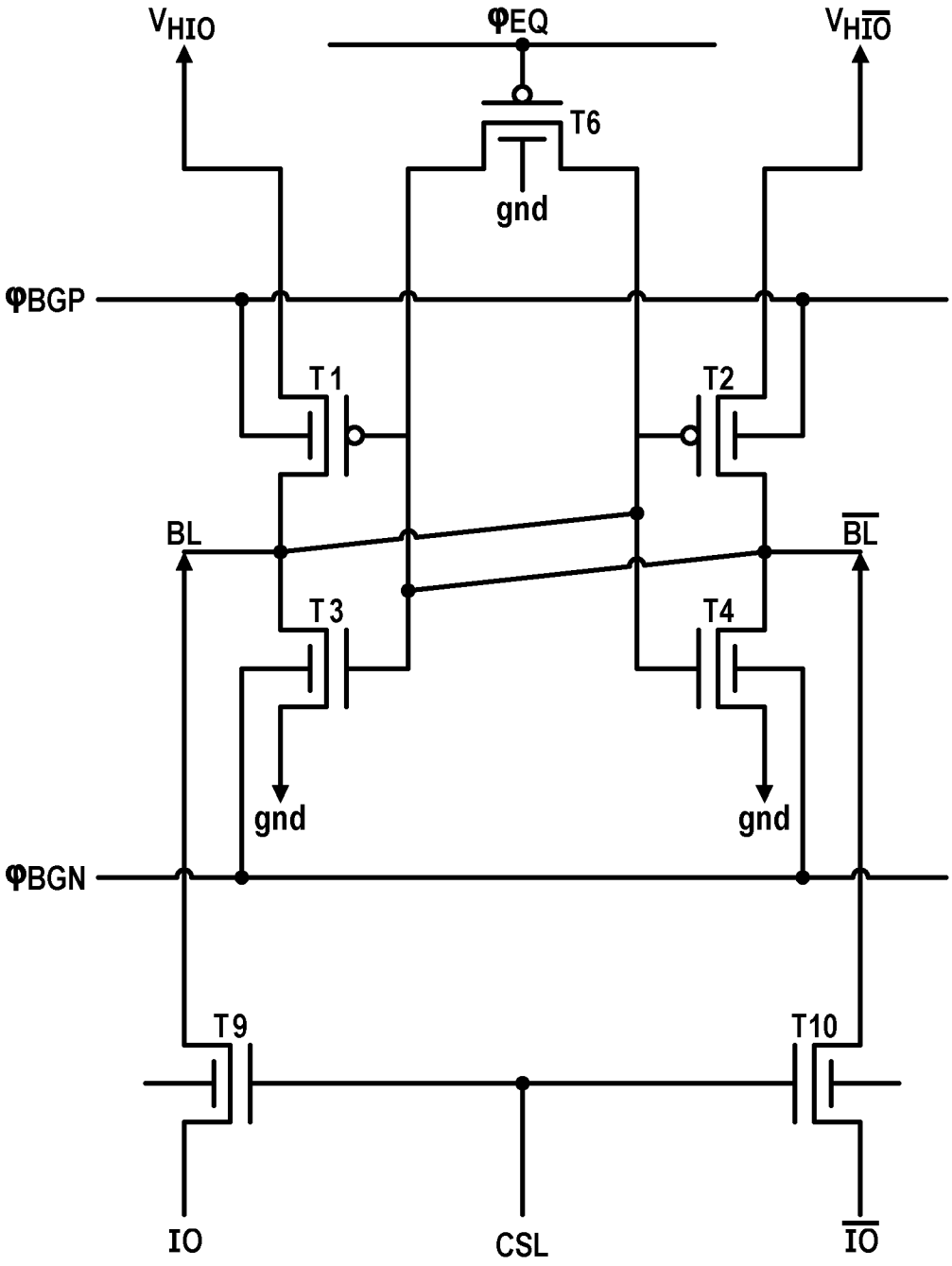
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FIG. 4

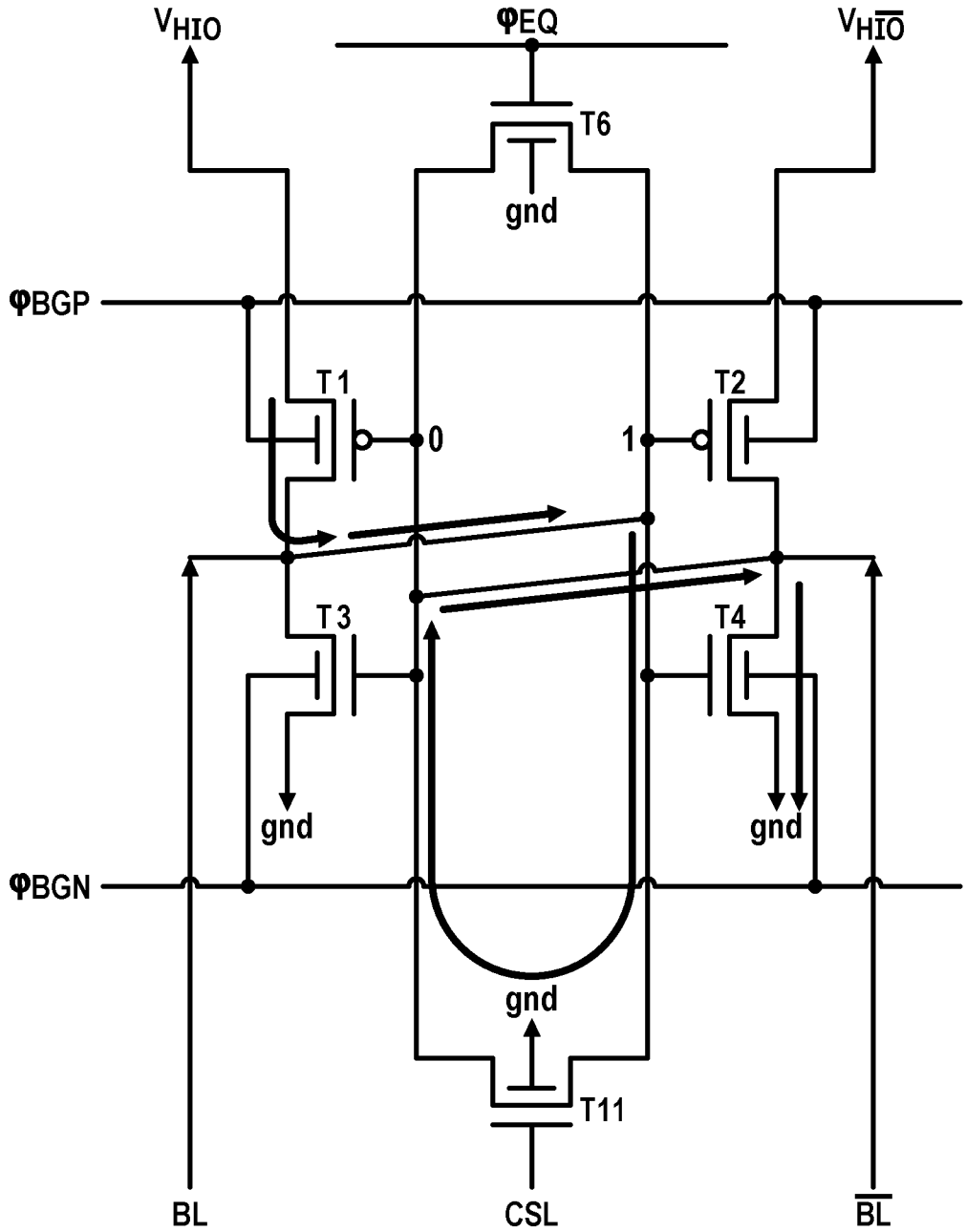
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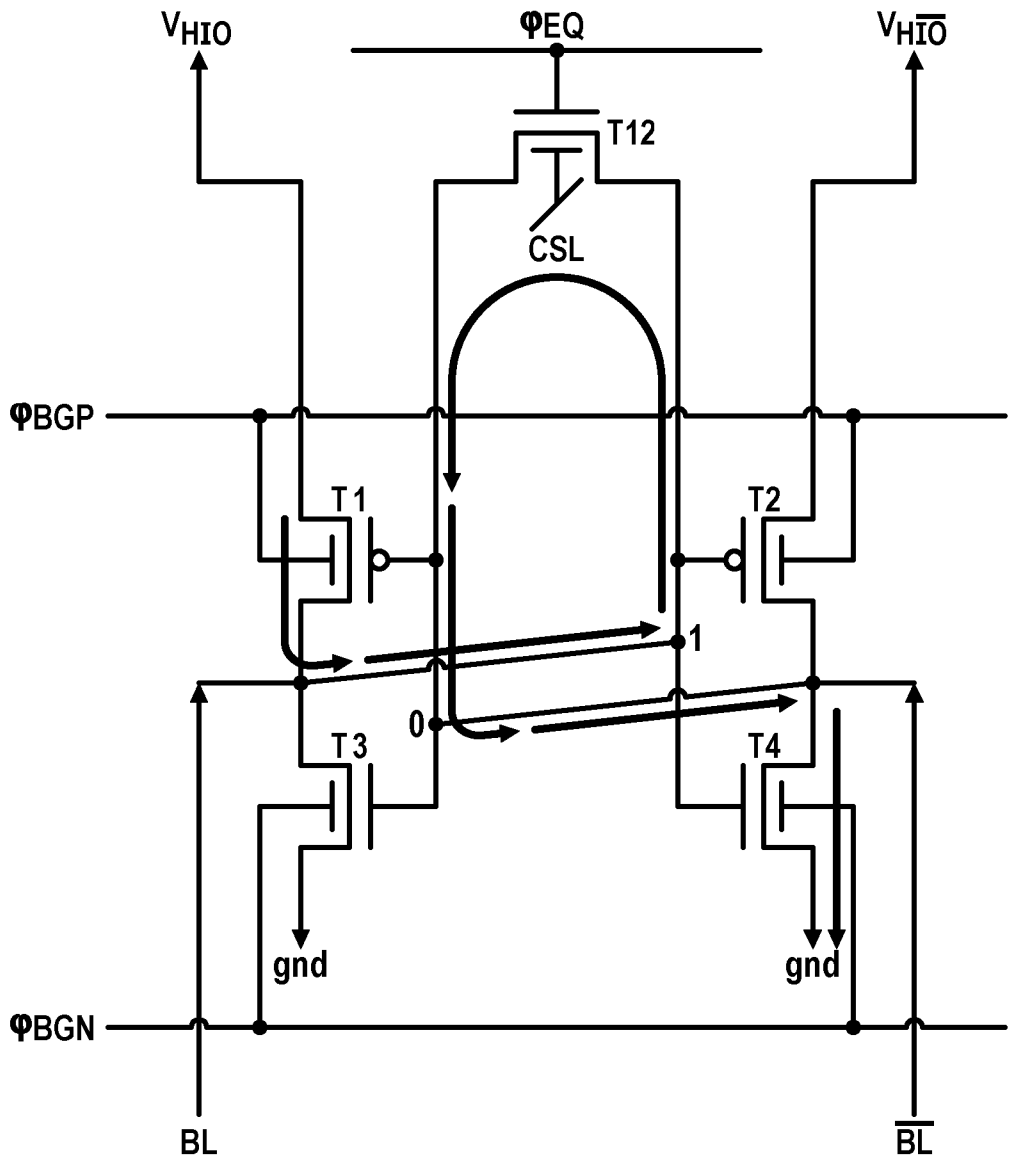
FIG. 5



INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2013/050760

A. CLASSIFICATION OF SUBJECT MATTER
INV. G11C7/06 G11C11/4091 G11C7/12
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
G11C

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2004/213064 A1 (GYOHTEN TAKAYUKI [JP] ET AL) 28 October 2004 (2004-10-28) paragraph [0071] - paragraph [0079]; figure 7	1-10
A	EP 0 411 818 A2 (INMOS LTD [GB]) 6 February 1991 (1991-02-06) column 4, line 36 - column 7, line 27; figure 6	1-10

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents :

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
20 February 2013	28/02/2013

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Colling, Pierre

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
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Patent document cited in search report	Publication date	Patent family member(s)	Publication date
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