

[54] **METHOD AND APPARATUS FOR GENERATING A TRAVELING DISPLAY**

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[51] Int. Cl.² **G06F 3/14**

[58] Field of Search..... **340/324 AD, 334, 337, 339, 340/336**

[56] **References Cited**

UNITED STATES PATENTS			
3,611,348	10/1971	Rogers	340/324 AD
3,643,252	2/1972	Roberts, Jr.....	340/324 AD
3,716,842	2/1973	Belady et al.	340/324 A
3,742,482	6/1973	Albrecht et al.	340/324 AD

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[57] **ABSTRACT**

This invention relates to a method and apparatus for causing the display on a display device such as a cathode ray tube (CRT) to travel or advance in fractional stroke increments. The circuit includes a first counter, each unit increment of which corresponds to a predetermined fractional stroke increment of the display, and a second counter, each unit increment of which corresponds to a full stroke increment of the display, the second counter being connected to be incremented in response to an overflow from the first counter. The circuit also includes elements for determining and indicating the number of predetermined fractional stroke increments which the display is to be incremented and for incrementing the first counter by the indicated number. The counts in the first and second counters are utilized for controlling both the stroke and bit of the stroke of the display at which display of the first of successive characters applied for display begins.

16 Claims, 5 Drawing Figures

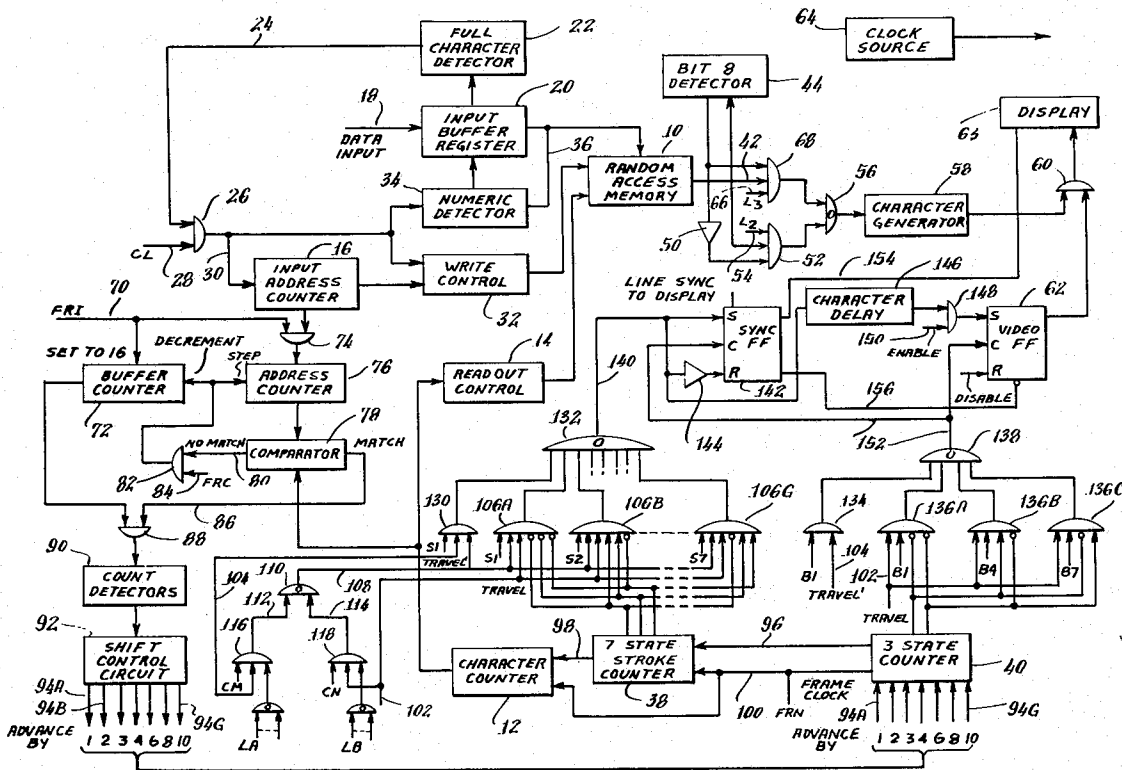


Fig. 1

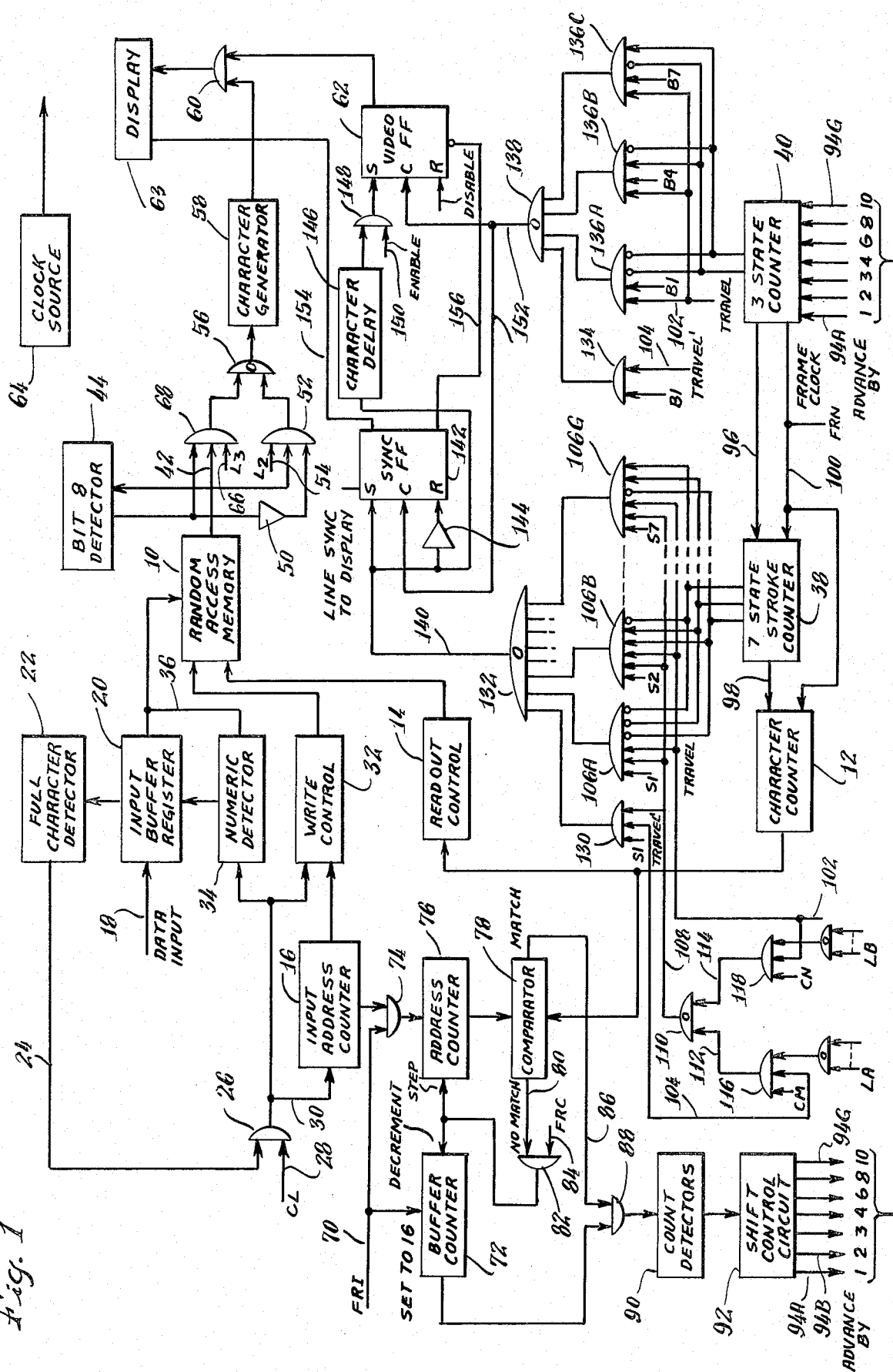


Fig. 2.

CHAR. #	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	54	55	56	57	58	59	60	61	62	63	64
	S	7	5							B	R	I	I	T		I	B	M	3	4	2	I	8	G	M	2
BIT	1	1	1																							

Fig. 3A.

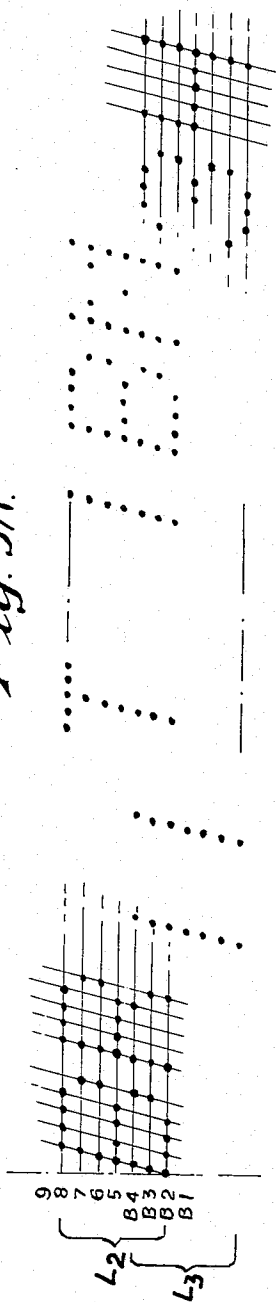


Fig. 3B.

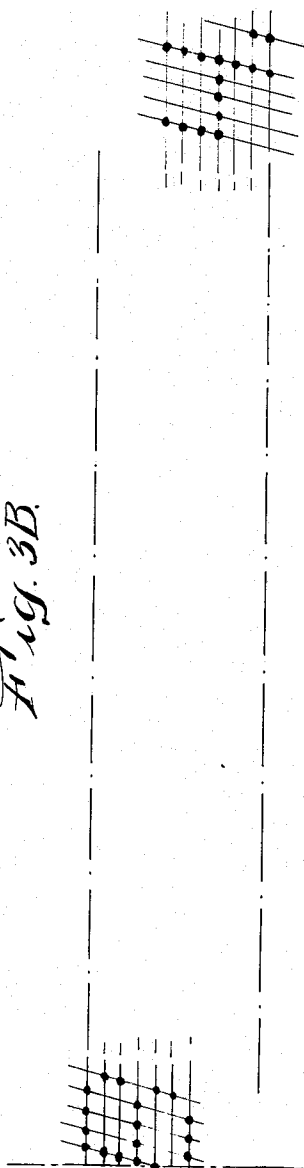
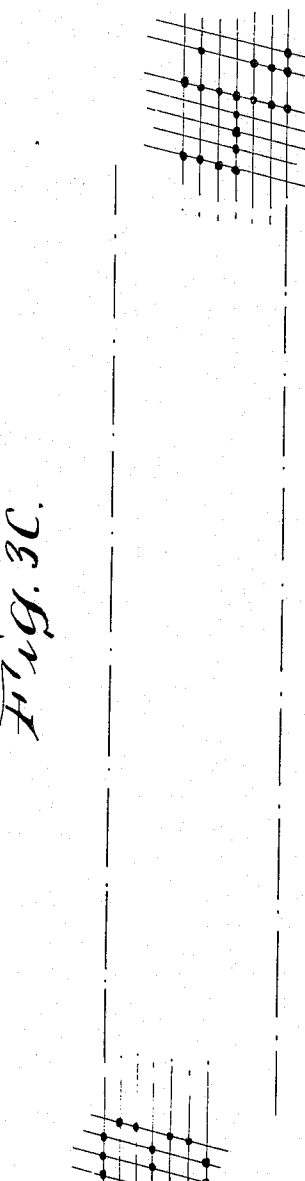


Fig. 3C.



METHOD AND APPARATUS FOR GENERATING A TRAVELING DISPLAY

This invention relates to traveling displays, and more particularly to a method and apparatus for causing the display on a display device such as a cathode ray tube (CRT) to travel or advance in fractional stroke increments.

BACKGROUND OF THE INVENTION

U.S. Pat. No. 3,742,482, entitled "METHOD AND APPARATUS FOR GENERATING A TRAVELING DISPLAY" issued to Francis E. Albrecht, et al., on June 26, 1973 discloses a technique for moving characters across the screen of a display device such as a CRT in increments of one or more character strokes, a stroke for purposes of the patent being one column of a character forming matrix. This capability of advancing the display by a fraction of a character for each frame retrace of the CRT, the fraction of a character by which the display is advanced being a function of the number of buffered characters awaiting display, theoretically provided a display which appeared to an observer to be moving at a fairly steady rate rather than in incremental jumps. However, in practice, it was found that even when advancing the display in increments of a single stroke, there was still a certain jerkiness to the display which was esthetically unacceptable. It is therefore apparent that a need exists for a technique adapted to control the display on a display device such as a CRT so as to permit the display to be advanced in increments of less than one stroke.

Another feature of the beforementioned Albrecht, et al. patent is the capability of displaying information of different types (for example stock IDs and related prices) one-half line spaced from each other, the information being received in succession on a single line. To accomplish this, the circuit of the Albrecht, et al. patent stored the information of different types in different sections of a memory, reading out the information from one section to refresh one line and reading out information from the other section to refresh the line spaced one-half line below. This technique is wasteful of memory in that two sections of memory are required in order to store information which could be stored in a single section of memory. A need therefore exists for a technique which permits the display advantages of the Albrecht, et al. patent to be achieved with the information being stored in a single section of memory.

SUMMARY OF THE INVENTION

In accordance with the above, this invention provides a circuit for use in a cyclically refreshed display device, such as a cathode ray tube (CRT), of the type which generates a plurality of writing strokes for each display line, information characters being displayed by selectively changing the visible state of M bits on each of N strokes for each character. The circuit causes the display to travel in fractional stroke increments. The circuit includes a first counter, each unit increment of which corresponds to a predetermined fractional stroke increment of the display and a second counter each unit increment of which corresponds to a full stroke increment of the display, the second counter being connected to be incremented in response to an overflow from the first counter. The circuit also includes means for determining and indicating the num-

ber of predetermined fractional stroke increments which the display is to be incremented; a means responsive to the number indicated by the determining and indicating means for incrementing the first counter by the number; a means for applying successive characters for display on the display device; and a means responsive to the outputs from the first and second counters for controlling both the stroke and bit of the stroke at which display of the first of the successive characters begins. Where the display is a CRT, the circuit includes a means operative at the end of each display line for initiating a retrace of the CRT writing beam, and a means for inhibiting the intensifying of the writing beam for a predetermined time period after the initiating of a retrace. The controlling means is then operative to control both the stroke and bit of the stroke of the last of the successive characters applied to the display at which the means for initiating a retrace is operated.

A line of characters to be displayed may contain characters of two different types, characters of one type being displayed a fraction of a line below the characters of the other type. A memory is provided for storing the characters of a line to be displayed in successive address positions, the characters of one type having a predetermined identifier stored with them in the memory. There is a means operative when the memory is being read out for detecting the character type from the stored identifier and for utilizing the character type identification to control the character position on the display.

The foregoing and other objects, features and advantages of the invention will be apparent from the following more particular description of a preferred embodiment of the invention as illustrated in the accompanying drawings.

BRIEF DESCRIPTION OF DRAWINGS

FIG. 1 is a schematic block diagram of a circuit of a preferred embodiment of the invention.

FIG. 2 is a diagram illustrating the contents of a character storing memory for the embodiment of the invention shown in FIG. 1.

FIG. 3A is a diagram illustrating a line of the display for a preferred embodiment of the invention.

FIG. 3B is a diagram illustrating the line of the display shown in FIG. 3A one frame time later under a first assumed set of conditions.

FIG. 3C is a diagram illustrating the line of the display shown in FIG. 3A one or more frame times later under a second assumed set of conditions.

DETAILED DESCRIPTION

While this invention is adapted for use with any traveling display in which characters are formed by selectively changing the visible state of M bits on each of N columns or strokes for each character, for the preferred embodiment of the invention the display will be considered to be a cathode ray tube (CRT) display. In particular, the display will be considered to be of the type described generally in the beforementioned Albrecht, et al. patent and in greater detail in U.S. Pat. No. 3,428,851 entitled "DATA DISPLAY SYSTEM" issued Feb. 18, 1967 to C. Greenblum, and in U.S. Pat. No. 3,500,327, entitled "DATA HANDLING APPARATUS" issued Mar. 10, 1970 to R. D. Belcher, et al. Generally, the display described in these patents is formed by generating a plurality of writing strokes for

each line of the display, a character being formed by selectively intensifying seven out of the 9 bit positions on each of five strokes. Two additional strokes are provided for each character for intercharacter spacing. A display of this type is shown in FIG. 3A for a single exemplary line of the display where the display is being utilized to display the New York Stock Exchange Ticker.

For esthetic reasons discussed in the beforementioned Albrecht, et al. patent, there is a half-line spacing between the alphabetic or stock ID portion of the ticker display and the price-volume information. The manner in which this half line spacing is obtained is described in greater detail in copending application Ser. No. 178,691 filed Sept. 8, 1970 on behalf of Frank Albrecht, et al. and entitled "RASTER CONTROL DEVICE".

Referring now to FIG. 1, it is seen that the circuit for the preferred embodiment of the invention includes a random access memory 10 in which is stored characters for display on the display device as well as a selected number of buffered characters awaiting display. Referring now to FIG. 2, the contents of a memory 10 for an illustrative embodiment of the invention are shown. For this embodiment of the invention, it is assumed that 48 characters are displayed on a traveling line and 16 buffered character positions are provided. As indicated in the beforementioned Albrecht, et al patent, a character counter 12 is provided which indicates the character position in memory 10 at which read out under control of a read out control circuit 14 is to commence for the line of characters being displayed. For purposes of illustration in the discussion to follow, it will be assumed that character position 11 is the character address contained in counter 12. The circuit also contains an input address counter 16 which indicates the address position in memory 10 at which the next received character is stored. For purposes of illustration, it will be assumed that this counter is pointing to character address 4. Arrows have been provided in FIG. 2 to illustrate these two assumed addresses.

As best seen in FIG. 3A, the stock market ticker information being displayed is seen to contain two types of information, alphabetic stock identification codes and numeric prices (and also sometimes volumes). It is also seen that the price and volume information is displayed a half-line below the stock ID information. In order to permit the two different types of information to be recognized and distinguished between, an extra bit, bit 8, is provided for each character in memory 10 which bit is marked for the numeric price and volume data. It should also at this point be noted that while memory 10 has been indicated above as containing only the traveling message for display on a given line, as a practical matter, this information would be contained in only a portion of a larger memory which contains information to be displayed for an entire frame on a given display device as well as alternative information to be displayed on the given display device and possibly on other display devices as well.

Referring now particularly to FIG. 1, it is seen that data bits received on input line 18 are stored in an input buffer register 20 until a full character is detected by full character detector 22. When this occurs, detector 22 generates an output on line 24 which is applied as one input to AND gate 26. At the next memory clock time, a signal appears on line 28, fully conditioning

AND gate 26 to generate an output on line 30 which is applied to enable write control circuit 32 and to condition numeric detector 34 to determine whether the character in buffer 20 is a stock ID or a numeric price-volume character. The enabling of write control circuit 32 causes the character stored in buffer register 20 to be written into memory 10 at the address indicated in counter 16. If detector 34 determines that the character in buffer 20 is a price or volume character, it generates an output on line 36, causing bit 8 of the stored character to be marked. The signal on line 30 is also applied to increment input address counter 16 to the address at which the next received character is to be stored.

As indicated previously, a character counter 12 is provided for indicating the character position in memory 10 from which the first character is to be read out to display a traveling line. In addition to character counter 12, there is also a seven state stroke counter 38 and a three state bit counter 40. The functions of these counters will be described shortly.

For purposes of the discussion to follow, it will be assumed that counter 12 is initially pointing to character position 11 and that counters 38 and 40 are both set to zero. Thus, when the line on which the traveling display is to appear is reached during the display of a frame, read out control 14 causes the characters to be displayed on the line to be successively read out onto line 42, starting with character position 11. Bit 8 of each character read out on line 42 is applied to bit 8 detector 44 which determines whether a bit 8 is present. Since the character in character position 11 is part of a stock ID, bit 8 is not marked for this character, resulting in inverter 50 applying one input to AND gate 52. Assuming that the display is to appear on line 2 of a frame, a signal also appears on line 2 clock line 54 at this time, conditioning AND gate 52 to pass the characters outputted on line 42 through OR gate 56 and video character generator 58, to AND gate 60. Assuming that video flip flop 62 is in its set state at this time, AND gate 60 is conditioned to pass the video information from generator 58 to display 63.

At this point clock source 64 should be mentioned. This is a device of conventional design which may include various counters and which generates outputs to indicate the line, character, stroke, and bit position at which writing is presently occurring during each frame retrace cycle of display 63. This device also generates clock pulses during frame retrace which are utilized in a manner to be described later. The outputs from source 64 are shown at various points in the circuit and properly labeled, the line 54 being one such output.

From the above it is apparent that only characters that do not have the bit 8 position marked (i.e. stock ID characters) are passed to character generator 58 when line 2 is being retraced on display 63. Thus, line 2 shown in FIG. 3A is retraced on the display.

When the retracing of line 2 has been completed, memory 10 is again read out, this time with a clock signal appearing on line 3 clock line 66. The signal on line 66 is applied as one conditioning input to AND gate 68, the other conditioning input to this AND gate being the output from bit 8 to detector 48. Thus, during line 3 time, the characters having a marked 8 bit, the price and volume characters, are passed through AND gate 68 and OR gate 56 to character generator 58, the video outputs from the character generator being applied

through AND gate 60 to display 63. Line 3, shown in FIG. 3A, is thus written during the second reading out of memory 10. The manner in which the half line spacing between lines is achieved is, as previously indicated, disclosed in the beforementioned Albrecht, et al. application, and forming no part of the present invention, will not be discussed further herein.

At the end of a frame, certain frame retrace clocks are generated. The first of these clocks to be utilized is a frame retrace one (FR 1 clock) on line 70 which is applied to set a buffer counter 72 to 16 and to condition gate 74 to pass the contents of input address counter 16 to be stored in address counter 76. The address stored in counter 76 is compared with the address stored in character counter 12 in a comparator 78. If these two addresses are not the same, which would be the case if there are any buffered characters awaiting display in memory 10, comparator 78 generates an output on no-match line 80 which conditions gate 82 to pass each succeeding FR clock on line 84 to decrement buffer counter 72 and to increment or step address counter 76. When counter 76 has been stepped to an address which is the same as the address in counter 12, the count stored in buffer counter 72 is equal to the number of characters being buffered in memory 10. At this time, there is a match output from comparator 78 which is applied to condition gate 88 to pass the count in counter 72 to count detectors 90. Detectors 90 are essentially decoders which generate an output on a given line depending on the count in buffer counter 72. Thus, there would be one output from detectors 90 if the count in buffer counter 72 was zero, another output if the count was 1, a third output if the count was between 3 and 5, another if the count was between 4 and 6 and the like. There would be some overlap between the counts since shift points would vary depending on whether the number of bits by which the shift was being incremented for each frame was being increased or decreased.

The outputs from detectors 90 are applied to a shift control circuit 92 which consists of a number of flip flops, one for each possible shift increment, and gating circuitry for controlling the setting of the proper flop depending on the output from detectors 90 and the existing state of the flops. Circuit 92 generates an output on one of seven lines 94. While circuits 90 and 92 have not been shown or described in detail herein, circuits for performing the functions indicated are shown in the beforementioned Albrecht, et al. patent and similar circuitry would be employed herein.

Referring again to FIG. 3A, it is seen that there are nine bits for each stroke of a character with seven of the 9 bits being utilized for display. For the preferred embodiment of the invention, the display is to be stepped in one-third stroke increments. Thus, display of a character stroke might begin at bit position one, bit position 4, or bit position 7 on the stroke. The outputs on lines 94 indicate the number of one-third stroke increments which the display is to be stepped between successive frames, an output on line 94A indicating that the display is to be incremented by three bits, an output on line 94B indicating that the display is to be incremented by six bits, and an output on line 94C indicating that the display is to be incremented by nine bits or one stroke. An output on line 94E indicates that the display is to be incremented by two strokes while an output on line 94G indicates that the display is to be in-

cremented by three and one-third strokes (i.e. 30 bits). As indicated previously, the smaller increments occur when there are a relatively small number of characters in the buffer portion of the memory while the larger increments occur when the buffer is full or nearly full.

Lines 94 are connected as stepping inputs to three-state bit counter 40. Each of the lines 94 causes counter 40 to be incremented by the number written adjacent thereto. Thus, a signal on line 94A causes the counter to be incremented by one, a signal on line 94D causes the counter to be incremented by four while a signal on line 94G causes the counter to be incremented by 10. An overflow from bit counter 40 on line 96 causes seven state stroke counter 38 to be incremented. Similarly, an overflow on line 98 from stroke counter 38 causes character counter 12 to be incremented. The incrementing of the counters 12, 38 and 40 occurs at a selected clock time during frame retrace (FR N time) when a clock signal appears on line 100.

Two signals which are utilized with the circuit of FIG. 1 are a "travel" signal on line 102 and a "not-travel" (travel') signal on line 104. A signal appears on travel line 102 when a line which is caused to travel across the display is being refreshed. A signal appears on not travel line 104 at all other times. The lines 102 and 104 may, for example, be outputs from a flip flop which is set by a suitable external device or in response to selected clocks, may be derived directly from an external device, or may be outputs from gates controlled by suitable clocks.

The three output lines from stroke counter 38 are applied either in direct or inverted form as inputs to each of seven AND gates 106A-106G, (only three of which are shown in FIG. 1) the other inputs to each of these AND gates being a selected stroke clock, travel line 102, and a sync enable line 108. Sync enable line 108 is the output line from OR gate 110, the inputs to which are output lines 112 and 114 from AND gates 116 and 118 respectively. The inputs to AND gate 116 are a character clock line CM, not travel line 104, and output line 120 from OR gate 122. The inputs to OR gate 122 are various selected line clocks (LA etc.). The inputs to AND gate 118 are a character clock line for the character CN travel line 102, and output line 124 from OR gate 126. The inputs to OR gate 126 are various other selected line clocks (for example lines 2 and 3 for the preferred embodiment of this invention). Sync enable line 108 and not travel line 104 are also connected as inputs to AND gate 130, the final input to this AND gate being the stroke 1 clock line. The outputs from AND gates 106 and 130 are connected as inputs to OR gate 132. Thus, for a line of display which is not to travel, an input is applied to OR gate 132 at stroke 1 time of a selected character (a CM character) time for the line. As will be seen shortly, the CM character is the character after the last character of the line to be displayed. For a line which is to travel, an input is applied to OR gate 132 at a selected stroke time, depending on which of the gates 106 is conditioned by the outputs from counter 38, at CN time of the line. For a preferred embodiment of the invention, character N is character 49. While this 49th character is, as will be described later, is either partially displayed or not displayed at all, it may be considered as the last character to be displayed.

Similarly, not travel line 104 is connected as one input to an AND gate 134, the other input to which is

a B1 clock line, while travel line 102 is connected as one input to each of three AND gates 136A-136C, the other inputs to these AND gates being the B1, B4, and B7 clock lines respectively and a selected combination of direct and inverted outputs on the two output lines from three state bit counter 40. The output lines from AND gates 134 and 136 are connected as inputs to OR gate 138. Thus, an input is applied to OR gate 138 at bit 1 time of each stroke if the display line is not a traveling line or at either B1, B4 or B7 time of a line, depending on the count in counter 40, if the line is a traveling line.

Output line 140 from OR gate 132 is connected as the set input to sync flip flop 142 and through inverter 144 as the reset input to this flip flop. The signal on line 140 is also applied through a six character delay 146 as one input to AND gate 148. Assuming the presence of an enable signal on line 150, this signal normally being present, AND gate 148 is conditioned to pass the output from delay 146 to the set input of video flip flop 62. Output line 152 from OR gate 138 is connected as the clock input to both video flip flop 62 and sync flip flop 142. Output line 154 from the set side of flip flop 142 is connected to the line sync or line retrace input of display 63. Output line 156 from the reset side of flip flop 142 is connected to the invert reset input of video flip flop 62. Thus, video flip flop 62 is reset when sync flip flop 142 is set. A disable input to the reset side of video flip flop 62 is also provided although this input is not utilized for the present invention.

From the above it is seen that, for a line of the display which is not to travel, an output on line 140 is generated by OR gate 132 at stroke one time of the character following the last character to appear on the line to enable the setting of sync flip flop 142, and at bit 1 time of this stroke, before any display can be generated for the character, a clocking signal appears on output line 152 from OR gate 138 setting flip flop 142 to generate a line return sync signal which is applied through line 154 to display 63. The setting of sync flip flop 142 terminates the signal on line 156 causing video flip flop 62 to be reset. This deconditions gate 60 to prevent video display during the line retrace operation.

At the end of stroke one (S1) time, AND gate 130 is deconditioned terminating the signal on line 140. This causes inverter 144 to generate an output which resets flip flop 142. It is assumed that line retrace takes exactly six character times. Thus, when line retrace is completed, delay 146 generates an output which is applied to again set flip flop 62, permitting video display to resume.

For a traveling line, the generating of a line retrace signal is more complicated. At, for example, character 49 time of the line preceding a traveling line, gate 118 is fully conditioned to cause a sync enable signal to appear on line 108. Depending on the count of stroke counter 38, one of the AND gates 106 will be fully conditioned. For the condition of the counters previously assumed (for the display shown in FIG. 3A), the gate which is fully conditioned is gate 106A. Thus, in this instance, a set input is being applied to flip flop 142 at stroke one time. Similarly, the AND gate 136 which is conditioned depends on the count in counter 40. For the FIG. 3A display, AND gate 136A is conditioned, resulting in OR gate 138 generating an output to clock flip flops 62 and 142 at B1 time. Thus, under these conditions, the circuit operates to perform a line return op-

eration in the same manner as was described above for a line which is not traveling.

Assume now that a relatively small number of characters are being buffered in memory 10 so that, at the end of the frame, shift control circuit 92 generates an output on line 94A, causing counter 40 to be incremented by one to a count of one. The next time that character N of line 1 is reached, gate 118 will again be conditioned to generate a sync enable signal on line 108, and the count in stroke counter 38 remaining unchanged, AND gate 106A will be conditioned at S1 time of this character to cause a set enable input to be applied to sync flip flop 142. However, since AND gate 136B rather than AND gate 136A is now conditioned by the outputs from counter 40, OR gate 138 does not generate a clocking signal to flip flops 62 and 142 until bit four time of the stroke. During S1 time six character times later, when the beam is starting to trace the first character of the next line, line 2, delay 146 generates a set enable signal to video flip flop 62. However, a clocking input on line 152 to flip flop 62 is not generated until three bit times later. Thus, since video is not enabled for the first two bits of the first character stroke, these bits are not visible. The result of this is shown in FIG. 3B. At the end of line 2, a signal again appears on line 140 at S1 time of character 49. However, since neither the sync flip flop nor the video flip flop is clocked until bit four time of this stroke, video remains enabled for an extra three bit times resulting in the possible display of the first two bits of the 49th character. While this condition does not occur for line 2 in FIG. 3B, it does occur for line 3.

Assume now that either (1) at the end of the first frame, the number of buffered characters in memory 10 was sufficient to cause an output on line 94D; or (2) that at the end of the second frame, the number of buffered characters had increased to the point where shift control circuit 92 generated an output on line 94C. In either event, counter 40 would be stepped through a complete cycle causing an overflow output to appear on line 96 and would be again stepped to a count of one. The overflow output on line 96 is effective to increment stroke counter 38 to a count of two, resulting in AND gate 106B being conditioned during the next L1 time that a signal appears on line 108. AND gate 106B being conditioned means that one full stroke of character 49 is completed before the signal appears on line 140 to condition flip flop 142. Further, since bit counter 40 is also set to one, AND gate 136B is not enabled until bit four time to generate a clocking output on line 152. Thus, line retrace does not begin until stroke two bit four of character 49. Since delay 146 lasts for six full character times, it is not until stroke two of the first character of line two that the write beam is ready to begin tracing characters on a new line and that a set enabling input is applied to video flip flop 62. However, character generator 58 is still operating in synchronism with clock source 64. Thus, it has completed generating the outputs for the first stroke of the first character by this time and is in the process of generating bits for the second stroke of the character. At B4 time of the second stroke of the first character, a clocking signal finally appears on line 152, setting video flip flop 62 and thus enabling the display. FIG. 3C illustrates the appearance of this first character as a result of the operations indicated above.

The same sequence of events described above occurs at the end of line two and at the beginning of line three. At the end of line three the first stroke of character 49 and the first 3 bits of the second stroke of this character are generated before a line retrace sync occurs and video flip flop 62 is reset. Thus, as shown in FIG. 3C, the 49th character is partially displayed.

As indicated in the beforementioned Albrecht, et al. patent, a line is required between the last traveling line and the first nontraveling line in order to restore proper synchronization between the character generator and the display.

From the above, it is apparent that a relatively simple technique has been provided for creating a traveling display on the screen of a display device such as a cathode ray tube which display is adapted to move in increments of a selected fraction of a stroke and to move at a rate which is a function of some predetermined criteria such as the number of characters in a buffer awaiting display. While for the preferred embodiment of the invention, the display has been moved in one-third stroke increments, it is apparent that the display could be moved in increments as small as 1 bit. Further, while specific circuitry has been provided for the illustrative embodiment of the invention, other equivalent elements could be utilized. Thus, while the invention has been particularly shown and described above with reference to a preferred embodiment thereof, the foregoing and other changes in form and detail may be made therein while still remaining within the spirit and scope of the invention.

What is claimed is:

1. In a cyclically refreshed display device of the type which generates a plurality of writing strokes for each display line, information characters being displayed by selectively changing the visible state of M bits on each of N strokes for each character, a circuit for causing the display to travel in fractional stroke increments, comprising:

a first counter, each unit increment of which corresponds to a predetermined fractional stroke increment of the display;

a second counter, each unit increment of which corresponds to a full stroke increment of the display, said second counter being connected to be incremented in response to an overflow from said first counter;

control means for determining the number of predetermined fractional stroke increments which the display is to be incremented and for producing a control signal manifesting such number;

means responsive to said control signal for incrementing said first counter by said number;

means for applying successive characters for display on said display device; and

means responsive to the outputs from said first and second counters for controlling both the stroke and bit of said stroke at which display of the first of said successive characters begins.

2. A circuit as claimed in claim 1 wherein there are a plurality of lines of information displayed on said display device;

wherein only a selected one or more of the lines of said display are traveling, the remaining lines being stationary; and

wherein said means for controlling includes means for utilizing the outputs of said counters to control

the stroke and bit at which display of said first character begins only for traveling lines of the display.

3. A circuit as claimed in claim 1 wherein said means for applying characters to the display is operative during each refresh cycle of the display device; and wherein the incrementing of the display by said number of predetermined fractional stroke increments occurs for each refresh cycle.

4. A circuit as claimed in claim 1 including a memory for storing said characters which are successively applied to the display, said memory also functioning as a buffer memory for characters awaiting display; and wherein said control means includes means for determining the number of characters awaiting display which are stored in said buffer memory, and means responsive to the number of characters determined for determining said number of predetermined fractional stroke increments.

5. A circuit as claimed in claim 1 wherein a line of characters to be displayed may contain characters of two different types, characters of one type being displayed a fraction of a line below characters of the other type; and

including a memory for storing the characters of a line to be displayed in successive address positions, the characters of one type having a predetermined identifier stored with them in said memory; means operative when said memory is being read out for detecting the character type from the stored identifier; and

means for utilizing said character type identification to control the character position on the display.

6. A circuit as claimed in claim 5 wherein said memory is read out twice for each line containing characters of different types; and

wherein said means for controlling character position includes means for applying to the display only characters of one type during a first read out for display on a given line and for applying to the display only characters of the other type during the second read out for display a fraction of a line below the characters of the one type.

7. A circuit as claimed in claim 1 wherein said display is a CRT having a writing beam; and

including means operative at the end of each display line for initiating a retrace of the CRT writing beam;

means for inhibiting the intensifying of said writing beam for a predetermined time period after the initiating of said retrace in response to said means for initiating a retrace; and

wherein said means for controlling is operative to control both the stroke and bit of the stroke of the last of said successive characters at which said means for initiating a retrace is operated.

8. A circuit as claimed in claim 1 wherein said display travels in one-third stroke increments; and

wherein said first counter is a three state counter.

9. In a cyclically refreshed cathode ray tube (CRT) display device of the type in which the CRT writing beam traverses a plurality of writing strokes for each display line, information characters being displayed by selectively intensifying the writing beam for M bits on each of N strokes for each character, a circuit for causing the display to travel in fractional stroke increments comprising:

a first counter, each unit increment of which corresponds to a predetermined fractional stroke increment of the display;

a second counter, each unit increment of which corresponds to a full stroke increment of the display, said second counter being connected to be incremented in response to an overflow from said first counter;

control means for determining the number of predetermined fractional stroke increments which the display is to be incremented and for producing a control signal manifesting such number;

means responsive to said control signal for incrementing said first counter by said number;

means for applying successive characters for display on said display device;

means operative at the end of each display line for initiating a retrace of the CRT writing beam;

means for inhibiting the intensifying of said writing beam for a predetermined time period after the initiating of said retrace in response to said means for initiating a retrace; and

means responsive at least in part to said first and second counters for controlling both the stroke and bit of the stroke of the last of said successive characters at which said means for initiating a retrace is operated.

10. A circuit as claimed in claim 9 wherein said display travels in one-third stroke increments; and wherein said first counter is a three state counter.

11. In a cyclically refreshed display device adapted for displaying at least one line of characters which line may contain characters of two different types, a circuit for controlling the display so that characters of one type are displayed a fraction of a line below characters of the other type comprising:

a memory for storing the characters of the line to be displayed in successive address positions, the characters of one type having a predetermined identifier stored with them in the memory; means for successively reading out the contents of said memory;

means for detecting said predetermined identifier in the characters read out from said memory;

means responsive to the detection of said identifier for permitting only characters of a first type to be applied to said display during a first read out of said memory to refresh the display along a given line; and

means responsive to said identifier detection means for applying only characters of said second type during a second read out of said memory to refresh the display along a line a fraction of a line below said given line.

12. In a cyclically refreshed display device of the type which generates a plurality of writing strokes for each display line, information characters being displayed by selectively changing the visible state of M bits on each of N strokes for each character, a method for causing the display to travel in fractional stroke increments, comprising the steps of:

determining the number of fractional stroke increments by which the display is to be incremented and producing a control signal manifesting such number;

incrementing a first counter in response to said control signal, each unit increment of said first counter

corresponding to a predetermined fractional stroke increment of the display;

incrementing a second counter in response to an overflow from said first counter, each unit increment of said second counter corresponding to a full stroke increment of the display;

applying successive characters for display on said display device; and

utilizing outputs from said first and second counters for controlling both the stroke and bit of the stroke at which display of the first of said successive characters begins.

13. A method as claimed in claim 12 wherein said display is a CRT having a writing beam; and including the steps of initiating a retrace of the CRT writing beam at the end of each display line; inhibiting the intensifying of said beam for a predetermined time period after the initiating of each said retrace;

and wherein said controlling step includes the step of controlling both the stroke and bit of said stroke at which each retrace is initiated.

14. In a cyclically refreshed display device of the type which generates a plurality of slanting writing strokes for each horizontal display line, information characters being displayed by selectively changing the visible state of M bits on each of N strokes for each character, a circuit for causing the display to travel horizontally in fractional stroke increments, comprising:

a first counter, each unit increment of which corresponds to a predetermined fractional stroke increment of the display;

a second counter, each unit increment of which corresponds to a full stroke increment of the display, said second counter being connected to be incremented in response to an overflow from said first counter;

control means for determining the number of predetermined fractional stroke increments which the display is to be incremented and for producing a control signal manifesting such number;

means responsive to said control signal for incrementing said first counter by said number;

means for applying successive characters for display on said display device; and

means responsive to the outputs from said first and second counters for controlling both the stroke and bit of said stroke at which display of the first of said successive characters begins.

15. In a cyclically refreshed display device of the type which generates a plurality of writing strokes for each display line, information characters being displayed by selectively changing the visible state of M bits on each of N strokes for each character, a circuit for causing the display to travel in fractional stroke increments, comprising:

a random access memory for storing representations of characters to be displayed in fixed locations therein;

readout control means for periodically reading from said memory representations of characters to be displayed;

a first counter, each unit increment of which corresponds to a predetermined fractional stroke increment of the display;

a second counter, each unit increment of which corresponds to a full stroke increment of the display,

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said second counter being connected to be incremented in response to an overflow from said first counter;
control means for determining the number of predetermined fractional stroke increments which the display is to be incremented and for producing a control signal manifesting such number;
means responsive to said control signal for incrementing said first counter by said number;
means for applying successive characters for display on said display device; and
means responsive to the outputs from said first and second counters and connected to said readout control means for controlling both the stroke and

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bit of said stroke at which display of the first of said successive characters begins.
16. A circuit as claimed in claim 15 including input means for receiving input data to be displayed, a buffer register for temporarily storing said input data, said random access memory being connected to receive data from said buffer register, signal producing means connected to said buffer register and operative to produce a signal manifesting the quantity of data stored therein, and means connecting said signal producing means with said control means, whereby said control means is responsive to the quantity of data stored in said buffer register.

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