

(19) World Intellectual Property Organization
International Bureau



(43) International Publication Date
11 May 2006 (11.05.2006)

PCT

(10) International Publication Number
WO 2006/049419 A1

(51) International Patent Classification⁷: **H04J 11/00**

(21) International Application Number:
PCT/KR2005/003657

(22) International Filing Date:
2 November 2005 (02.11.2005)

(25) Filing Language: Korean

(26) Publication Language: English

(30) Priority Data:
10-2004-0088765
3 November 2004 (03.11.2004) KR

(71) Applicant (for all designated States except US): **ELECTRONICS AND TELECOMMUNICATIONS RESEARCH INSTITUTE** [KR/KR]; 161 Gajeong-Dong, Yuseong-gu, Daejeon 305-350 (KR).

(72) Inventors; and

(75) Inventors/Applicants (for US only): **CHO, Sang In** [KR/KR]; 162-5 Shinsung-Dong, Yuseong-gu, Daejeon 305-345 (KR). **CHOI, Sang Sung** [KR/KR]; 397-51 Doryong-Dong, Yuseong-gu, Daejeon 305-340 (KR). **PARK, Kwang Roh** [KR/KR]; 103-401 Mugunghwa Apt., Wolpyeong-dong, Seo-gu, Daejeon 302-280 (KR).

(74) Agent: **LEE, Hwa Ik**; Young International Patent & Law Firm, 4th Fl. Yosam Bldg. 648-23, Yoksam-dong, Kangnam-gu, Seoul 135-748 (KR).

(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KZ, LC, LK, LR, LS, LT, LU, LV, LY, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SM, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

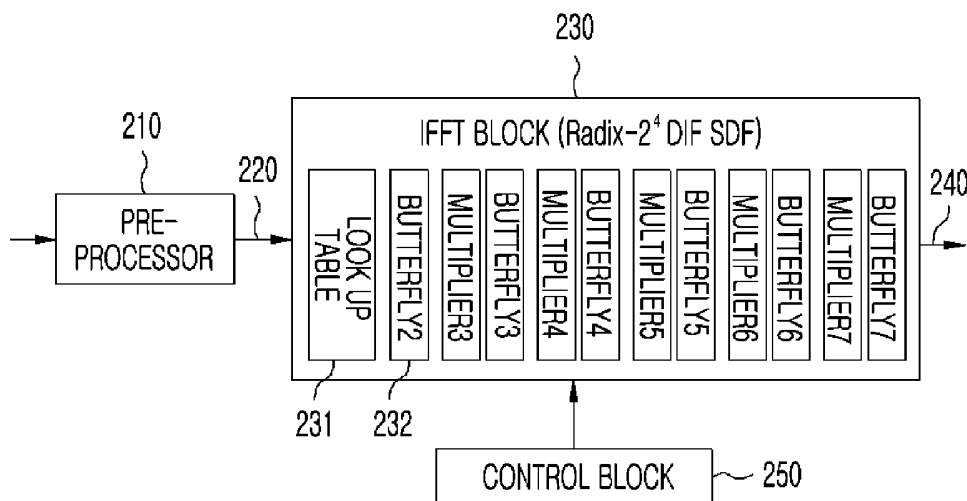
(84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IS, IT, LT, LU, LV, MC, NL, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:

— with international search report

[Continued on next page]

(54) Title: METHOD FOR TRANSFORMING DATA BY LOOK-UP TABLE



(57) Abstract: Provided is a method for transforming data using a look-up table. The method includes the steps of: (a) mapping pre-processed input binary data to a constellation diagram divided into four quadrants to output a first complex number; (b) performing addition/subtraction operations between real numbers and between imaginary numbers with respect to the first complex number and a second complex number; and (c) reading a fourth complex from a look-up table in response to the first complex number, the second complex number and a third complex number, the look-up table outputting the fourth complex by performing a subtraction operation on multiplication results between real numbers and between imaginary numbers and an addition operation on multiplication results between the real numbers and the imaginary numbers with respect to the result value of the step (b) and the third complex number. Accordingly, it is possible to reduce the hardware size at the time of IFFT/FFT design and to provide a high-speed, low-power operation.

WO 2006/049419 A1



For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

Description

METHOD FOR TRANSFORMING DATA BY LOOK-UP TABLE

Technical Field

- [1] The present invention relates to a method for transforming data by a look-up table, and more particularly, to a data transforming method that uses a look-up table for design of an inverse fast Fourier transform/fast Fourier transform (IFFT/FFT) for an orthogonal frequency division multiplexing (OFDM) system and thus can provide a high-speed operation, a low-power consumption and miniturization.

[2]

Background Art

- [3] Conventional OFDM systems have not strongly required a high-speed operation in an IFFT/FFT block. However, recent wireless communication systems requires a ultrahigh data rate of several tens to hundreds Mbps and thus must use a parallel structure or other VLSI techniques. In general, an OFDM scheme requiring an IFFT/FFT block is widely used for high-rate data transmission. The IFFT/FFT block requires a large amount of multiplication and addition and thus these arithmetic operations must be processed very rapidly.

- [4] In the OFDM scheme, high-rate data are divided into a large number of data sequences and the data sequences are simultaneously transmitted using a plurality of subcarriers. The IFFT/FFT operation is an arithmetic operation of generating subcarriers and combining data into the subcarriers. In the OFDM system, a transmitter performs an IFFT operation for combining data into subcarriers and a receiver performs an FFT operation for obtaining the data from the subcarriers. An FFT arithmetic expression is obtained from a discrete Fourier transform (DFT) expression that can be given by Equation 1 below.

[5]

$$X(k) = \sum_{n=0}^{N-1} x(n) e^{-j \frac{2\pi}{N} kn}$$

..... (1)

[6]

$$\begin{aligned}
X(0) &= x(0) + x(1) + x(2) + x(3) \\
X(1) &= x(0) + x(1)e^{-j\frac{2\pi}{4}1} + x(2)e^{-j\frac{2\pi}{4}2} + x(3)e^{-j\frac{2\pi}{4}3} \\
X(2) &= x(0) + x(1)e^{-j\frac{2\pi}{4}2} + x(2)e^{-j\frac{2\pi}{4}4} + x(3)e^{-j\frac{2\pi}{4}6} \\
X(3) &= x(0) + x(1)e^{-j\frac{2\pi}{4}3} + x(2)e^{-j\frac{2\pi}{4}6} + x(3)e^{-j\frac{2\pi}{4}9} \\
&\dots (2)
\end{aligned}$$

[7]

[8] In Equation 1, $X(k)$ is the frequency-domain result from the FFT and $x(n)$ is a time-domain input data value. In Equation 2,

$$e^{-j\frac{2\pi}{N}kx}$$

is a coefficient multiplied by the input. Equation 2 expresses a 4-point DFT arithmetic operation and includes multiplications and additions. As can be seen from Equations 1 and 2, the amount of the arithmetic calculation increases as N increases.

[9] The structure of the conventional IFFT/FFT block will now be described in detail.

[10] Fig. 1 is a block diagram of an OFDM IFFT block including a QPSK modulator and an radix-2⁴ DIF SDF 256-point IFFT block.

[11] Referring to Fig. 1, the OFDM IFFT block includes a pre-processor 110, a QPSK modulator 130, an IFFT block 150, and a control block 170. The pre-processor performs convolution coding and interleaving. Binary data 120 of '1' and '0' are inputted into the QPSK modulator 130. The QPSK modulator 130 divides the inputted binary data 120 on a 2-bit basis, maps the divided data to a QPSK constellation diagram, and generates a complex output 140.

[12] The IFFT block 150 uses an radix-2⁴ DIF (decimation in frequency) SDF(single-path delay feedback) structure and is an 256-point IFFT block receiving 128-point complex data and 128-point '0'. The 256-point IFFT operation requires a 8-stage butterfly. However, since 128 points are constituted by '0', a butterfly of one stage can be omitted. The radix-2⁴ structure needs a multiplier only at three stages but does not need a multiplier at the remaining stages that requires multiplication by j . A multiplier1 151 performs an arithmetic operation of j and does not actually perform multiplication. A butterfly1 152 as well as the other butterflies performs addition and subtraction on two inputted complex numbers. A multiplier2 153 actually performs multiplication by three coefficients, that is, (

$$e^{-j\frac{2\pi}{256}32}$$

,

$$e^{-j \frac{2\pi}{256} 128}$$

,

$$e^{-j \frac{2\pi}{256} 160}$$

). These multiplication coefficients are controlled by the control block 170. By the above process, the IFFT block 150 outputs a complex result 160.

[13] As above, the QPSK modulator obtains pre-processed binary data from complex data, and the IFFT block 150 performs addition and multiplication on the complex data to output time-domain complex data.

[14] However, since the complex data from the QPSK modulator are transformed into time-domain complex data by the IFFT block including seven butterflies and seven multipliers, the arithmetic operation speed of the IFFT/FFT is proportional to the speed of the addition and multiplication. That is, the arithmetic operation speed of the IFFT/FFT is proportional to the number of the butterflies and the multipliers.

[15]

Disclosure of Invention

Technical Problem

[16] Accordingly, the present invention is directed to a data transforming method that substantially obviates one or more of the problems due to limitations and disadvantages of the related art.

[17] An object of the present invention is to provide a data transforming method that uses inputted binary data as an address and uses a look-up table for performing addition and subtraction on two inputted complex numbers and multiplication by a coefficient selected by a control block, thereby making it possible to provide the high-speed operation, low-power consumption and miniturization of an IFFT/FFT block.

[18]

Technical Solution

[19] To achieve these and other advantages and in accordance with the purpose of the present invention, as embodied and broadly described, there is provided a method for transformign data using a look-up table, the method including the steps of: (a) mapping pre-processed input binary data to a constellation diagram divided into four quadrants to output a first complex number; (b) performing addition/subtraction operations between real numbers and between imaginary numbers with respect to the first complex number and a second complex number; and (c) reading a fourth complex number from a look-up table in response to the first complex number, the second complex number and a third complex number($A_o, A_I, B_o, B_I, C_o, C_I$) the look-up table

outputting the fourth complex(d_o, d_i) by performing a subtraction operation on multiplication results between real numbers and between imaginary numbers and an addition operation on multiplication results between the real numbers and the imaginary numbers with respect to the result value of the step (b) and the third complex number.

[20]

Advantageous Effects

[21] According to the present invention, the look-up table using the input binary data of the modulator as an address instead performs the addition/multiplication operations, thereby making it possible to reduce the hardware size at the time of the IFFT/FFT design and to provide the high-speed, low-power operation. When the look-up table is used, the QPSK modulator, an arithmetic device for $-j$, one butterfly, one complex multiplier a scaling block for each stage become unnecessary. This is very advantageous

[22] in view of hardware, power consumption, and operation speed. Also, a round-off error and a quantization error can be prevented from occurring at each stage, thereby enhancing the performance. The data transforming method according to the present invention can be applied to any system requiring the IFFT/FFT block, as well as the OFDM system.

[23]

Brief Description of the Drawings

[24] Fig. 1 is a block diagram illustrating a QPSK modulator and an Radix-2⁴ DIF SDF 256-point IFFT block.

[25] Fig. 2 is a block diagram of an IFFT block using a look-up table according to an embodiment of the present invention.

[26] Fig. 3 is an operational block diagram of a butterfly and a multiplier in the IFFT block.

[27] Fig. 4A is a constellation diagram of QPSK modulation.

[28] Fig. 4B is a diagram illustrating the arithmetic operation results of an adder in the butterfly.

[29] Fig. 4C is a diagram illustrating the arithmetic operation results of the multiplier.

[30] Fig. 5 is a diagram illustrating the input and output of the look-up table.

[31]

Best Mode for Carrying Out the Invention

[32] Hereinafter, preferred embodiments of the present invention will be described in detail with reference to accompanying drawings.

[33] Fig. 2 is a block diagram of an OFDM IFFT block according to an embodiment of

the present invention.

[34] In the embodiment, a QPSK modulation scheme is used and a 256-point IFFT block with a radix-2⁴ DIF SDF structure, which can be used in a multiband-OFDM (MB-OFDM) system performing a 128-point arithmetic operation, is used. The OFDM IFFT block is designed such that it performs a 256-point arithmetic operation by inserting 128 0's so as to widen a gap between repeated spectrums.

[35] Referring to Fig. 2, the OFDM IFFT block includes a pre-processor 210, an IFFT block 230, and a control block 250. Unlike the IFFT/FFT block in Fig. 1, the OFDM IFFT block uses a look-up table 231 instead of the QPSK modulator, the multiplier1, the butterfly1 and the multiplier2, and thus performs the functions of the non-used elements by using the look-up table 231. Like reference numerals in Figs. 1 and 2 denote like elements, and thus their description will be omitted for conciseness.

[36] The look-up table 231 uses the input binary data of the QPSK modulator as an address, and performs the functions of the non-used butterfly and multipliers. That is, the look-up table 231 divides inputted binary data 220 on a 2-bit basis, maps the divided data to a QPSK constellation, and outputs a complex number 240. Also performed are a j arithmetic operation on the outputted complex number 240, and addition/subtraction/multiplication operations on the two inputted complex numbers. At this time, three coefficients for the above multiplication operation are (

$$e^{-j\frac{2\pi}{256}32},$$

$$e^{-j\frac{2\pi}{256}128},$$

$$e^{-j\frac{2\pi}{256}160}$$

). These multiplication coefficients are controlled by the control block 250. By the above process, complex IFFT results 240 are outputted.

[37] Fig. 3 is an operational block diagram of the butterfly and the multiplier in the OFDM IFFT block.

[38] Referring to Fig. 3, complex numbers $a_0 + ja_1$ 330 and $b_0 + jb_i$ 340 are inputted into a butterfly 310, $c_0 + jc_1$ 350, which is the above multiplication coefficient, is inputted into a multiplier 320. $d_0 + jd_1$ 360 is an output of a butterfly 340. Addition/subtraction operations between real numbers Re and between imaginary numbers Im are performed with respect to the complex numbers $a_0 + ja_1$ 330 and $b_0 + jb_i$ 340, and the resulting values are re-inputted into the butterfly 310 through a delay or outputted from the butterfly 310 to the multiplier 350. The multiplier 320 performs multi-

plication operations between real numbers, between imaginary numbers, and between real numbers and imaginary numbers with respect to the outputted resulting values and the complex number $c_0 + jc_1$ 350, and outputs the real difference value between the multiplication results between the real numbers and between the imaginary numbers and the imaginary sum value of the multiplication results between the real numbers and the imaginary numbers.

[39] Fig. 4A is a constellation diagram of the QPSK modulation according to the present invention.

[40] Referring to Fig. 4A, when an input bit is '11' the output value of the QPSK modulation is $1 + j1$ 410. On the contrary, when the input bit is '01' the output value of the QPSK modulation is $-1 + j1$ 420.

[41] Fig. 4B is a diagram illustrating the arithmetic operation results of an adder in the butterfly.

[42] Referring to Fig. 4B, when the input complex numbers of the butterfly are $1 + j1$ and $1 + j1$, the output complex number is $2 + j2$ 420. In this case, the input bits 220 of the QPSK are '11' and '11' 420, respectively. On the contrary, when the input complex numbers of the butterfly are $-1 + j1$ and $1 + j1$, the output complex number is $0 + j2$ 421. In this case, the input bits 120 of the QPSK are '01' and '11' 421, respectively.

[43] Fig. 4C is a diagram illustrating the arithmetic operation results of the multiplier. Specifically, Fig. 4C illustrates multiplication results of the arithmetic results of the butterfly and a multiplication coefficient (twiddle factor). A multiplier2 (not illustrated) in the look-up table can have three multiplication coefficients and thus can be expressed by two bits. When a control signal of the control block 250 is '00', no value is multiplied. When the control signal of the control block 250 is '01',

$$e^{-j\frac{2\pi}{256}32}$$

is multiplied. When the control signal of the control block 250 is '10

$$e^{-j\frac{2\pi}{256}128}$$

is multiplied. When the control signal of the control block 250 is '1',

$$e^{-j\frac{2\pi}{256}160}$$

is multiplied. When the output value of the butterfly is $2 + j2$ 420 and the multiplication coefficient is '1', $2 + j2$ 430 is outputted. When the multiplication coefficient is

$$e^{-j\frac{2\pi}{256}32}$$

, 2

$$\sqrt{2}$$

+ j0 431 is outputted. When the multiplication coefficient is

$$e^{-j\frac{2\pi}{256}128}$$

, 2 - j2 432 is outputted. That is, depending on the multiplication coefficients, - j2

$$\sqrt{2}$$

433, j2 434, 2 + j

$$\sqrt{2}$$

435, '2' 436, or j - j

$$\sqrt{2}$$

437 is outputted.

- [44] Fig. 5 is a diagram illustrating the input and output of the look-up table. Specifically, Fig. 5 illustrates a relationship the output complex number and the input bits used as an address of the look-up table.

- [45] Referring to Fig. 5, $C_0, C_1, A_0, A_1, B_0, B_1$ are the input bits. C_0 541 and C_1 542 are control signals outputted from the control block 250 and are used to determine the multiplication coefficient. A_0 521, A_1 522, B_0 531 and B_1 532 are the input bits of the QPSK modulation corresponding to the input complex numbers calculated at the same time. When ' $C_0 C_1 A_0 A_1 B_0 B_1$ ' is '100111' 436, the result value of the look-up table is $2 + j0$, d_0 541 is 2, and d_1 542 is 0. That is, since $A_0 A_1, B_0 B_1$ and $C_0 C_1$, are '01', '11' and '10', respectively, the butterfly arithmetic result (input: $-1 + j1$ and $1 + j1$) multiplied by

$$e^{-j\frac{2\pi}{256}128}$$

is outputted. At this time, since the output values d_0 541 and d_1 542 of the look-up table must be scaled for the remaining calculation, it may be beforehand scaled to a proper size at the time of the storage of it in the look-up table. The stored value in the look-up table may be any value illustrated in Fig. 4C. It may be possible to store only values of one quadrant (e.g., the first quadrant) and use a combination of a real number, an imaginary number, and a code.

- [46] While the present invention has been described and illustrated herein with reference to the preferred embodiments thereof, it will be apparent to those skilled in the art that various modifications and variations can be made therein without departing from the spirit and scope of the invention. Thus, it is intended that the present invention covers the modifications and variations of this invention that come within the scope of the appended claims and their equivalents.

- [47]

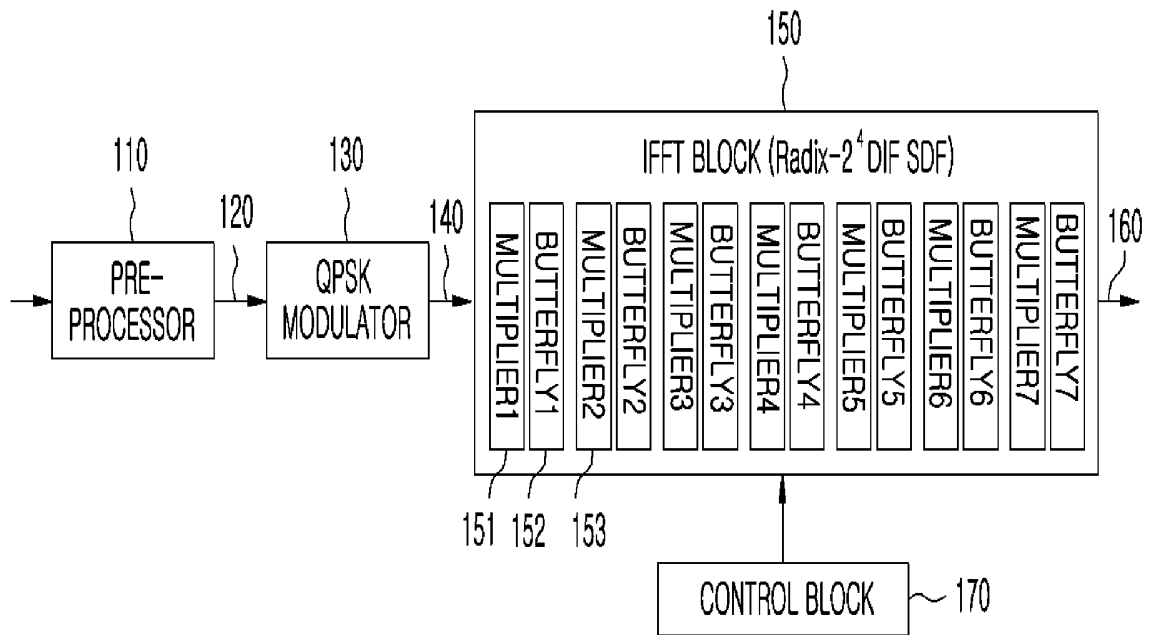
[48]

Claims

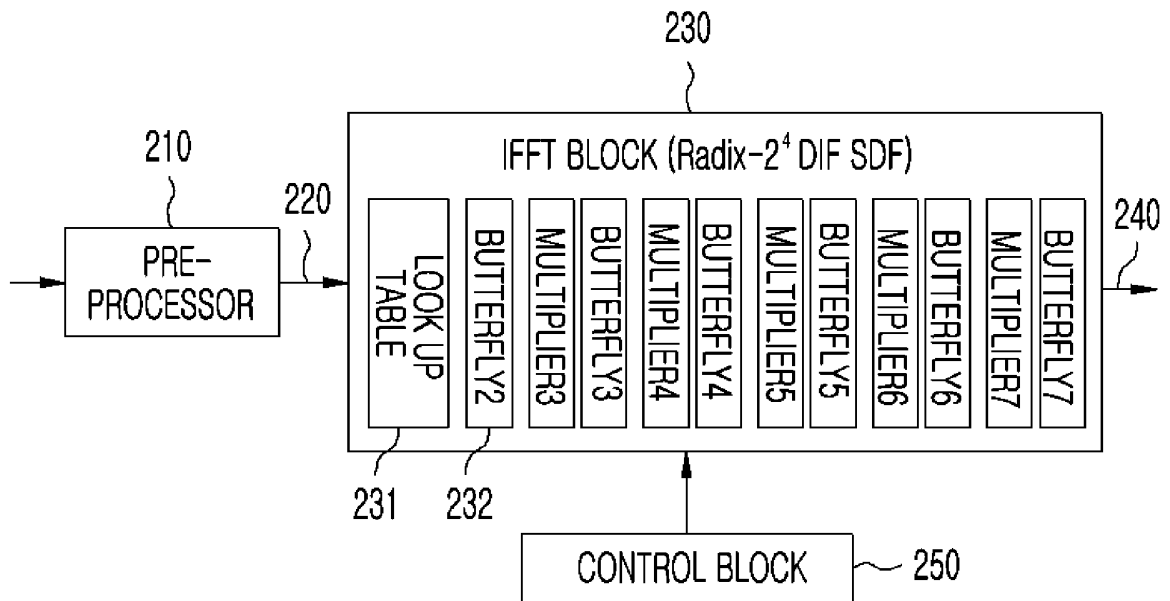
- [1] A method for transforming data using a look-up table, the method comprising the steps of:
- (a) mapping pre-processed input binary data to a constellation diagram divided into four quadrants to output a first complex number;
 - (b) performing addition/subtraction operations between real numbers and between imaginary numbers with respect to the first complex number and a second complex number; and
 - (c) reading a fourth complex from a look-up table in response to the first complex number, the second complex number and a third complex number, the look-up table outputting the fourth complex by performing a subtraction operation on multiplication results between real numbers and between imaginary numbers and an addition operation on multiplication results between the real numbers and the imaginary numbers with respect to the result value of the step (b) and the third complex number.
- [2] The method of claim 1, further comprising, after the step (c), the step of outputting time-domain complex data by multiplying the result values from the look-up table at a multi-stage multiplier and alternately and sequentially performing addition/subtraction operations on input complex numbers at a multi-stage butterfly.
- [3] The method of claim 1, wherein a multiplication coefficient multiplied during the step (c) is one selected from the group 1,
- $$e^{-j\frac{2\pi}{256}32}$$
- ,
- $$e^{-j\frac{2\pi}{256}128}$$
- , and
- $$e^{-j\frac{2\pi}{256}160}$$
- according to the third complex number.
- [4] The method of claim 3, wherein the multiplication coefficient is controlled by a control block.
- [5] The method of claim 1, wherein the arithmetic results of the step (b) is feedback as a parameter of the first complex number through a delay.
- [6] The method of claim 1, wherein the look-up table stores only a value of one quadrant among four quadrants of the output values.

- [7] The method of claim 1, wherein an output value of the look-up table is beforehand scaled to a predetermined size at the storage time thereof.
- [8] The method of claim 1, wherein the method is applied to an OFDM (orthogonal frequency division multiplexing) system.
- [9] The method of claim 1 or 6, wherein the method is applied to a 256-point FFT/IFFT (fast Fourier transform/inverse fast Fourier transform) operation with a radix-2⁴ DIF (decimation in frequency) SDF (single path delay feedback) structure, which is able to be used in a multiband-OFDM system performing a 128-point arithmetic operation.

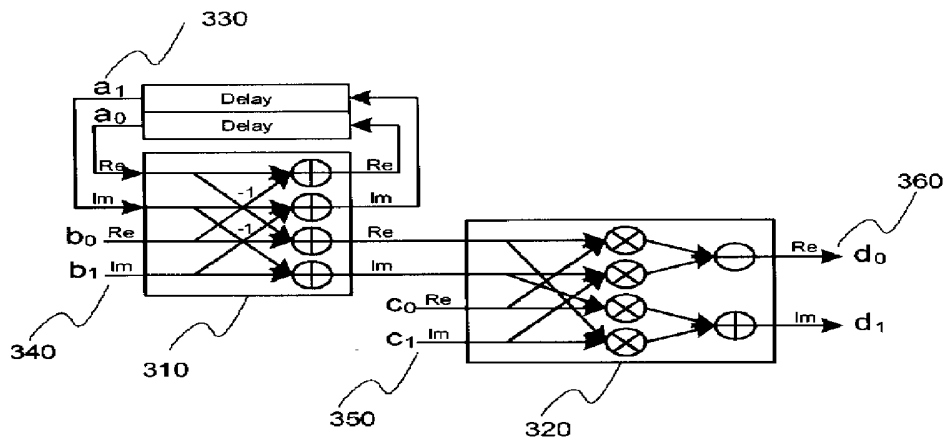
[Fig. 1]



[Fig. 2]

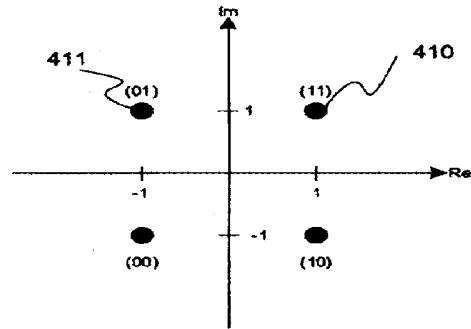


[Fig. 3]

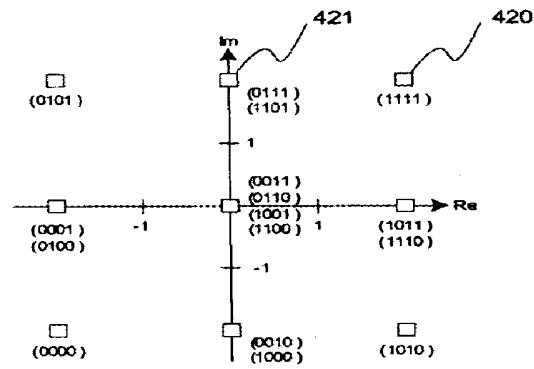


[Fig. 4]

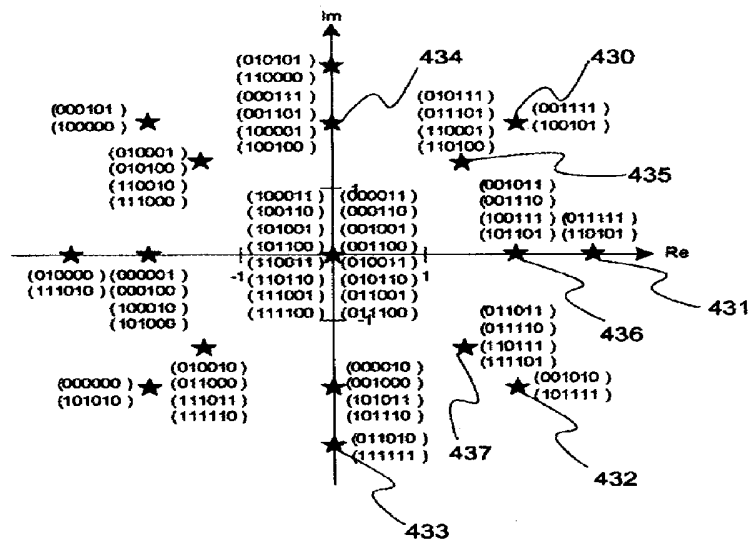
(a)



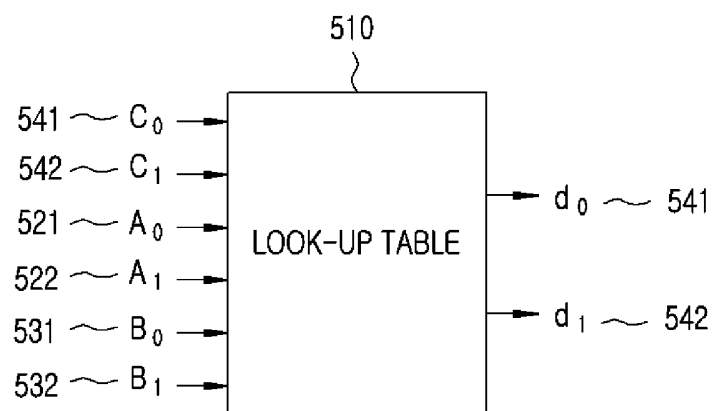
(b)



(c)



[Fig. 5]



INTERNATIONAL SEARCH REPORT

International application No.
PCT/KR2005/003657

A. CLASSIFICATION OF SUBJECT MATTER**IPC7 H04J 11/00**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC 7: H04J H04B H04L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
KOREAN PATENTS AND APPLICATIONS FOR INVENTIONS SINCE 1975

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
PAJ, FPD, USPAT, eKIPASS, IEEE "LOOK-UP TABLE""FFT/IFFT""COMPLEXITY""OFDM"

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	KR 1999-0081320 A1 (DAEWOO ELECTRONICS CO, Ltd.) 15 NOVEMBER 1999 see the whole document	1-9
A	KR 2001-0064866 A1 (INSTITUTE INFORMATION TECHNOLOGY ASSESSMENT, KOREA TELECOM) 11 JULY 2001 see the whole document	1-9



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

27 DECEMBER 2005 (27.12.2005)

Date of mailing of the international search report

28 DECEMBER 2005 (28.12.2005)

Name and mailing address of the ISA/KR



Korean Intellectual Property Office
920 Dunsan-dong, Seo-gu, Daejeon 302-701,
Republic of Korea

Facsimile No. 82-42-472-7140

Authorized officer

CHEKAL Hyun

Telephone No. 82-42-481-5667



INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/KR2005/003657

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
KR 1999-0081320 A1	15. 11. 1999	EP 1070400 A1 JP 14513242 US 6470030 BA	24.01.2001 08.05.2002 22.10.2002
=====			