

END OF LINE PARASITIC CAPACITANCE IMPROVEMENT USING IMPLANTS

BACKGROUND

Field

5 Integrated circuit devices.

Description of Related Art

Circuit transistors, such as complementary metal oxide semiconductor (CMOS) transistors can be dominated by parasitic capacitance that is equal to or in some cases larger than an intrinsic channel capacitance.

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BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 shows a cross-sectional side view of an embodiment of a non-planar field effect transistor (MOSFET) device.

15 **Figure 2** shows a cross-sectional side view of the structure of **Figure 1** through line 2-2'.

Figure 3 shows a perspective side view of a substrate having a fin formed therein according to an embodiment of forming a transistor device.

Figure 4 shows the structure of **Figure 3** having a trench dielectric layer on the substrate surrounding the fin.

20 **Figure 5** shows the structure of **Figure 4** following the removal of the fin to form a trench of a controlled size and shape.

Figure 6 shows the structure of **Figure 5** following the introduction of a buffer material in the trench.

25 **Figure 7** shows the structure of **Figure 6** following a removal of a portion of the buffer material in the trench and the introduction of an intrinsic material into the trench.

Figure 8 shows the structure of **Figure 7** following a recession of the dielectric layer to define a fin.

30 **Figure 9** shows the structure of **Figure 8** following the formation of a sacrificial or dummy gate stack on the fin and sidewall spacers on opposing sides of the sacrificial gate stack.

Figure 10 shows the structure of **Figure 9** through line 10-10' after forming a source and a drain and replacement of the sacrificial gate stack with a gate electrode, the forming of a passivation layer (ILD0) and contacts to the source, drain and gate electrode.

Figure 11 shows the structure of **Figure 10** and the implantation of halogen atoms into the structure.

Figure 12 shows the structure of **Figure 11** following the implantation of halogen atoms into dielectric materials of the structure.

5 **Figure 13** shows the structure of **Figure 12** following the patterning of a metal line, including traces connected to contacts of the transistor device, and a dielectric layer on the metal line and shows the implantation of halogen atoms.

Figure 14 shows the structure of **Figure 13** following the implantation of halogen atoms into the dielectric layer on the metal line.

10 **Figure 15** presents a flow chart of a process of forming the transistor device illustrated in **Figures 3-14**.

Figure 16 is an interposer implementing one or more embodiments.

Figure 17 illustrates an embodiment of a computing device.

15 DETAILED DESCRIPTION

Figure 1 shows a cross-sectional side view of an embodiment of a field effect transistor (FET) device such as a metal oxide semiconductor field effect transistor (MOSFET) device, a tunneling field effect transistor (TFET) device or other FET device.

20 **Figure 2** shows the structure of **Figure 1** through line 2-2'. In this embodiment, a non-planar transistor is described that includes a conducting channel above a level of a dielectric layer as part of a transistor body or fin. A gate electrode is disposed on adjacent sides of the transistor body or fin. Although a three-dimensional transistor is illustrated, it is appreciated that the techniques described are applicable to other transistors including planar transistors and gate all-around devices.

25 Referring to **Figure 1** and **Figure 2**, device 100 includes substrate 110 that is, for example, a single crystal silicon substrate such as a bulk substrate or a silicon on insulator substrate. Disposed on substrate 110, in this embodiment, is buffer or sub-fin layer 120. Buffer layer 120 contains, for example, a material that has a different lattice than a material of the substrate (e.g., silicon substrate 110). A suitable material for buffer layer 120 includes
30 but is not limited to indium phosphate (InP), germanium (Ge), silicon germanium (SiGe), gallium arsenide (GaAs), gallium phosphide (GaP), gallium arsenide antimony (GaAsSb), indium aluminum arsenide (InAlAs), indium aluminum antimony (InAlSb), gallium antimony (GaSb), or other group III-V compound semiconductor. To reduce a threading dislocation density, a material in buffer layer 120 may be graded with, for example, a

material of the underlying substrate (e.g., silicon) to gradually increase a material composition of buffer layer in an epitaxially grown film such that closer to substrate 110, a material concentration of buffer layer is less and increases away from the substrate. In another embodiment, two or more different materials may be present in buffer layer 120 such as a first material at the base of the buffer layer and a second material on the first material.

In the embodiment in **Figures 1-2**, disposed on buffer layer 120 is intrinsic layer 140. In one embodiment, intrinsic layer 140 is a channel material for the particular transistor device. In one embodiment, intrinsic layer 140 includes silicon, germanium, silicon germanium or a group III-V compound material. In one embodiment, the group III-V compound material includes indium (In) (i.e., has a concentration of indium). An example of a group III-V compound material including indium, particularly for an n-type transistor device is InGaAs. Germanium and silicon germanium are examples of material for intrinsic layer 140 for a p-type transistor device.

In one embodiment, buffer layer 120 and intrinsic layer project from a surface of substrate 110 as a pillar having a length greater than a width with buffer layer 120 surrounded by dielectric layer 125 and intrinsic layer 140 above or a primarily above dielectric layer 125. In another embodiment, rather than being formed of multiple materials or material layers, such a pillar may be formed of a single material such as only of a material for intrinsic layer 140. In still another embodiment, such a pillar may be formed of a material of substrate 110 such as silicon.

As illustrated in **Figure 1**, disposed in intrinsic layer 140 is diffusion or junction region 150 and diffusion or junction region 155. In one embodiment, diffusion region 150 is a source of a MOSFET and diffusion region 155 is a drain of the MOSFET. Disposed between diffusion regions 150 and 155 is channel 1400 of a material of intrinsic layer 140 having a length dimension, L of, for example, 10 nanometers (nm) to 30 nm.

Figure 2 is a cross-section through a channel region of the transistor of **Figure 1** and shows that the body of intrinsic layer 140 in this region has a generally rectangular profile that, in one embodiment, has a superior surface that appears substantially parallel to a surface of substrate 110. It is appreciated that a profile of the body of intrinsic layer will depend in part on the processing techniques (e.g., polish, etching, etc.) used to form the body. Accordingly, a body targeted to have a rectangular profile may have a profile approximating a rectangular profile (e.g., a profile with rounded edges, a trapezoidal profile, etc.). The rectangular profile is illustrated for explanation purposes and is intended as but one example of a profile employed in a transistor device. Alternative profiles are also contemplated.

Overlying channel region 1400 is gate dielectric layer 170 of, for example, a silicon dioxide or a dielectric material having a dielectric constant greater than silicon dioxide (a high-k material) or a combination of silicon dioxide and a high-k or a combination of dielectric material, including but not limited to high-k materials and low-k materials (e.g., hafnium oxide (HfO_2), yttrium oxide (Y_2O_3), strontium oxide (Sr_2O_3), magnesium oxide (MgO), tantalum nitride (TaN), germanium oxide (GeO_2), indium phosphide (InP), gallium oxide (GaO), scandium oxide (Sc_2O_3)). A representative thickness of gate dielectric layer 170 is on the order of a few nanometers. As illustrated in **Figure 2**, gate dielectric layer 170 is disposed on sidewalls of a length dimension, L, of the body or fin including channel 1400 exposed above dielectric layer 125 and on a superior surface of the body or fin as viewed. Disposed on gate dielectric 170 is gate electrode 175 of, for example, an electrically conductive material such as a metal material (e.g., tantalum (Ta), titanium (Ti), aluminum (Al), copper (Cu), gold (Au), silver (Ag), platinum (Pt), iron (Fe), nickel (Ni)), a metal nitride (e.g., titanium nitride (TiN), tantalum nitride (TaN), aluminum nitride (AlN), alloys of metals or metal nitrides, or a silicide. In one embodiment, as shown in **Figure 2**, gate electrode 175 is disposed on the top and two opposing sides of channel 1400. In this manner, gate electrode 175 is disposed on adjacent sides of channel 1400. For representative purposes, in one embodiment, gate electrode 175 has a total thickness on the order of 5 nm to 50 nm and dielectric layer 170 has a thickness of 1 nm to 15 nm. Referring to **Figure 1**, on opposite sides of gate electrode 175 defined by a length dimension, l, of channel 1400 are sidewall spacers 185 of a dielectric material such as silicon dioxide, a low-k dielectric material, a nitride material (e.g., Si_xN_y , $\text{Si}_x\text{O}_y\text{N}_z$) or a carbide material (e.g., $\text{Si}_x\text{O}_y\text{C}_z$, $\text{Si}_w\text{O}_x\text{C}_y\text{N}_z$).

Figure 1 shows a dielectric layer overlying the transistor device. Representatively, dielectric layer 145 is, for example, an interlayer dielectric layer (ILD0). Dielectric layer 145 is, for example, a silicon dioxide or a low-k dielectric material. Disposed through dielectric layer 145 are contacts to the junction or diffusion regions and the gate electrode. **Figure 1** shows contact 192A through dielectric layer 145 to contact source 150; contact 192B through dielectric layer 145 to contact drain 155; and contact 195 through dielectric layer 145 to contact gate electrode 175. Each contact 192A, 192B and 195 is an electrically conductive material such as tungsten.

In the embodiment shown in **Figures 1** and **2**, dielectric material on the transistor device includes a concentration of a halogen atom. Representative halogens include fluorine, chlorine or iodine. **Figure 1** shows halogen atoms 197 disposed in sidewall spacers 185 and dielectric layer 145. In one embodiment, the presence of halogen atoms is limited to the

sidewall spacers. In another embodiment, the halogen atoms are present only in dielectric layer 145. The presence of halogen atoms such as fluorine can reduce a parasitic capacitance of the dielectric material associated with transistor devices. In one embodiment, the halogen atoms are implanted or doped into spacer 185 and other passivation (e.g., dielectric layer 145) after forming of the material on the structure and after the transistor is formed. By performing the doping post processing before, for example, a subsequent dielectric layer is deposited, an etch property and selectivity of the doped material become less important.

Halogen doping or halogen silicate doping of dielectric materials post processing can be applied to dielectric spacers, liners and other isolation materials used in an integrated device circuit fabrication subsequent to the formation of transistors where there is a desire to lower a parasitic capacitance associated with such isolation material. Examples of dielectric materials that may be doped or implanted include silicon dioxide (SiO_2), silicon nitride (Si_xN_y), silicon oxynitride ($\text{Si}_x\text{O}_y\text{N}_z$), silicon oxycarbon nitride ($\text{Si}_w\text{O}_x\text{C}_y\text{N}_z$), silicon oxyboron nitride ($\text{Si}_w\text{O}_x\text{B}_y\text{N}_z$), silicon oxycarbon boron nitride ($\text{Si}_v\text{O}_w\text{C}_x\text{B}_y\text{N}_z$), hafnium oxide (HfO_2), aluminum oxide (Al_2O_3), zinc oxide (ZnO), indium gallium zinc oxide ($\text{In}_w\text{Ga}_x\text{Zn}_y\text{O}_z$), scandium oxide (Sc_2O_3), magnesium oxide (MgO).

Figures 3-14 describe one process for forming an integrated circuit device similar to that illustrated in **Figure 1** and **Figure 2**. **Figures 3-14** thus describe one embodiment of forming an integrated circuit device including a three-dimensional non-planar FET with dielectric spacers and other passivation materials doped with a halogen or halogen-doped silicate post formation of devices (e.g., after the fabrication of a transistor device) and/or post passivation. **Figure 15** presents a flow chart of forming the integrated circuit device described with reference to **Figures 3-14**.

Referring to **Figure 3** and with reference to the flow chart of **Figure 15**, the process begins by defining fin structures in a substrate material (block 410, **Figure 15**). **Figure 3** shows a perspective side view of structure 300 of substrate 310 that may be any material that may serve as a foundation of which an FET may be constructed. Representatively, substrate 310 is a portion of a larger substrate such as wafer. In one embodiment, substrate 310 is a semiconductor material such as single crystal silicon. Substrate 310 may be a bulk substrate or, in another embodiment, a semiconductor on insulator (SOI) structure. **Figure 3** shows substrate 310 following a patterning of the substrate to define fin 3100. Fin 3100 may be one of many fins formed in the substrate. Fin 3100 may be formed by a mask and etch process wherein a mask (e.g., a hard mask) is introduced on a surface (superior surface) of substrate 310 to protect areas of the substrate where the fins will be defined and to provide openings in

non-fin areas. Once the mask is patterned, substrate 310 may be etched to remove material in unprotected areas. A substrate of silicon may be etched with a wet or dry etch.

Representatively, a suitable etchant is chlorine or fluorine plasma based etch chemistry. In one embodiment, fin 3100 is formed to have a height, H, on the order of 100 nanometers (nm) to 400 nm. After fin 3100 is formed, the mask is removed to provide structure 300 shown in **Figure 3**.

Figure 4 shows structure 300 of **Figure 3** following a deposition of a trench dielectric layer on the substrate (block 415, **Figure 15**). In one embodiment, dielectric layer 325 is silicon dioxide or a low-k dielectric material. Following deposition of dielectric layer 325, a surface of the structure (a superior surface as viewed) is polished to the level of the top of fin 3100 so that the fin is exposed as shown in **Figure 4**.

In one embodiment, fin 3100 may serve as a device body (e.g., a channel) for a transistor device. In another embodiment, fin 3100 is removed and replaced with another material or materials. **Figures 5-8** describe the optional embodiment where fin 3100 is removed and replaced with other materials. **Figure 5** shows structure 300 of **Figure 4** following the removal of fin 3100 to form a trench of a controlled size and shape (block 420, **Figure 15**). The fin may be removed by a mask and etch process wherein a mask is patterned on a surface of dielectric layer 325 leaving fin 3100 exposed followed by an etch process to remove the fin. Sacrificial fins of a silicon material may be etched by a dry or wet etch or a combination of the two. Suitable etchants for etching sacrificial fins of a silicon material include potassium hydroxide (KOH) and tetramethylammonium hydroxide (TMAH). The removal of the sacrificial fin forms trench 318. In one embodiment, the etching of the sacrificial fin may be performed to provide a {111} faceting at the bottom of trench 318 to facilitate a growth of a material in the trench which is done using TMAH-like or any equivalent chemistry. Alternative geometries are also contemplated.

Figure 6 shows structure 300 of **Figure 5** following the introduction of a buffer material in trench 318 (block 422, **Figure 15**). In one embodiment, buffer material 320 is a material that has a different lattice than a material of the substrate (e.g., silicon substrate 110). A suitable material for buffer layer 120 includes but is not limited to indium phosphide (InP), germanium (Ge), silicon germanium (SiGe), gallium arsenide (GaAs), gallium phosphide (GaP), gallium arsenide antimony (GaAsSb), indium aluminum arsenide (InAlAs), indium aluminum antimony (InAlSb), gallium antimony (GaSb), or other group III-V compound semiconductor. To reduce a threading dislocation density, a material in buffer layer 320 may be graded with, for example, a material of the underlying substrate (e.g., silicon) to gradually

increase a material composition of buffer layer in an epitaxially grown film such that closer to substrate 310, a material concentration of buffer layer is less and increases away from the substrate. In another embodiment, two or more different materials may be present in buffer layer 320 such as a first material at the base of the buffer layer and a second material on the first material. Buffer material 320 may be introduced by an epitaxial growth process. In another embodiment, the trenches may be filled with a first buffer material of one of the noted materials as, for example, a nucleation layer at a base of trench 318 followed by a second buffer material of another of the noted materials. The trench confined growth of a retrograde material or materials offer an advantage of aspect ratio trapping (ART) whereby crystalline quality of the epitaxial layer(s) is enhanced through trapping of threading dislocations, stacking faults, twins, etc., at sidewalls of a trench where defects terminate such that overlying layers may be increasingly defect-free. **Figure 6** shows buffer material 320 in trench 318. The buffer material has a dimension measured in a z-direction on the order of 100 nm to 400 nm. **Figure 6** representatively shows buffer material 320 including {111} faceted overgrowth protruding off the superior plane defined by dielectric layer 325.

Figure 7 shows structure 300 of **Figure 6** following a removal of a portion of buffer material 320 in trench 318 and the introduction of an intrinsic material into the trench. In one embodiment, the removal of buffer material 320 is performed by an etch to recess the buffer material in the trench (block 424, **Figure 15**). **Figure 7** shows intrinsic layer 340 formed on buffer material 320 (block 426, **Figure 15**). The intrinsic layer may be epitaxially grown in trench 318. In one embodiment, intrinsic layer 340 is a material that is desired for a channel of a transistor device. Suitable materials include but are not limited to silicon, germanium, silicon germanium, a group III-IV compound semiconductor material (e.g., indium gallium arsenide (InGaAs), gallium arsenide (GaAs), indium arsenide (InAs), indium phosphide (InP)). Intrinsic layer 340 has a representative height on the order of 40 nm to 100 nm. **Figure 7** shows the structure following a polish of intrinsic layer 340 to a plane defined by dielectric layer 325.

Figure 8 shows the structure of **Figure 7** after a recession of dielectric layer 325 such that intrinsic layer 340 is protruding above a plane defined by dielectric layer 325 as a fin structure (block 430, **Figure 15**). Dielectric layer 325 may be recessed by an etch process. It is appreciated that in an embodiment where fin 3100 is retained rather than removed and replaced, the operations described with reference to **Figures 5-7** would be performed (blocks 420-426, **Figure 15**). In such case, a method can proceed directly from the structure shown in **Figure 4** (block 415, **Figure 15**) to that in **Figure 8** (block 430, **Figure 15**).

Figure 9 shows the structure of **Figure 8** following the formation of a sacrificial or dummy gate stack on the fin portion of intrinsic layer 340 extending above dielectric layer 325 (block 440, **Figure 15**). In one embodiment, a gate stack includes gate dielectric layer 360 of, for example, silicon dioxide or a high-k dielectric material. Disposed on gate dielectric layer 360, in one embodiment, is sacrificial or dummy gate 365 of, for example, polysilicon deposited by, for example, a chemical vapor deposition method. In one embodiment, following the forming of the gate stack, spacers 385 of a dielectric material of, for example, silicon dioxide, silicon nitride, silicon oxynitride, silicon oxycarbon nitride, silicon oxyboron nitride, silicon oxycarbon boron nitride or a low-k material are introduced on opposite sides of the gate stack spacers 385 maybe formed by a deposition process (e.g., chemical vapor deposition) and then patterned to be disposed on opposite sidewall of the gate stack (block 450, **Figure 15**). Spacers 385 may be formed by a deposition process (e.g., chemical vapor deposition (CVD)) and then patterned to be disposed on opposite sidewalls of the gate stack.

Figure 10 shows structure 300 of **Figure 9** through line 10-10' after forming diffusion or junctions and replacement of the sacrificial gate stack on the fin defined by intrinsic layer 340 with a gate stack (block 455, **Figure 15**). In one embodiment, source 350 and drain 355 are formed by initially removing portions of intrinsic layer 340 corresponding to diffusion regions (source and drain regions) in the fin. Representatively, an etch under cut (EUC) is performed to remove portions of intrinsic layer 340 in areas corresponding to a source region and a drain region with dummy gate 365 and sidewall spacers 385 protecting intrinsic layer 340 in a channel region. Following a removal of portions of intrinsic layer 340 in source and drain regions to leave voids, source 350 and drain 355 are formed in respective voids. In one embodiment where intrinsic layer 340 is germanium, source 350 and drain 355 are, for example, a highly doped germanium (p^{++}) such as a boron-doped germanium that is epitaxially grown. Where intrinsic layer 340 is InGaAs, source 350 and drain 355 are, for example, a highly doped InGaAs (n^{++}) such as arsenic-doped InGaAs.

Figure 10 also shows structure 300 of **Figure 9** following the replacement of the sacrificial gate stack. Following formation of source 350 and drain 355, a dielectric material is introduced on the structure (on a surface including source 350, drain 355 and dummy gate 365) as for example, an initial interlayer dielectric (ILD0). In one embodiment, dielectric material 345A is, for example, silicon dioxide or a low k material or a combination of materials (e.g., multiple low k materials or silicon dioxide and one or more low k materials). Sacrificial gate 365 and gate dielectric 360 are then removed by, for example, masking

dielectric material 390 with an opening to expose the sacrificial gate stack and then an etch process to remove dummy gate 365 and gate dielectric 360. The gate stack is replaced initially with gate dielectric 370 of, for example, silicon dioxide, a high-k material or a combination of silicon dioxide and a high-k material or a combination of high-k and low-k dielectric materials. This is followed by the formation of gate electrode 375 such as a metal gate electrode in a gate-last process flow (block 470, **Figure 15**). Representative materials for gate electrode 375 include, but are not limited to, tungsten, tantalum, titanium or a nitride, a metal alloy, a silicide or another material. Following formation of gate electrode 375, contacts may be made to source 350, drain 355 and gate electrode 375 (block 480, **Figure 15**). **Figure 10** shows contact 392A to source 350; contact 392B to drain 355; and contact 395 to gate electrode 375. A representative material for each contact is tungsten that may be deposited by a CVD process following formation of openings through dielectric material 345A to source 350, drain 355 and gate electrode 375, respectively.

The formation of transistor devices and an ILD0 (dielectric layer 345A) of structure 300 is now complete. **Figure 11** shows the structure of **Figure 10** showing the implantation of halogen atoms into the structure (block 485, **Figure 15**). More specifically, halogen atoms 397 of, for example, bromine, chlorine, iodine, fluorine are introduced into dielectric materials such as dielectric material 345 (ILD0) and spacers 385. In one embodiment, halogen atoms 397 are fluorine atoms. Halogen atoms 397 may be implanted or doped into the dielectric material by a plasma implantation process. In another embodiment, halogen atoms 397 may be introduced into one or all of the noted dielectric materials during a growth process of the dielectric material. For example, in one embodiment, dielectric material 345 and/or spacers 385 may be introduced by an atomic layer deposition (ALD) process involving sequential pulsing of a dielectric precursor. Halogen atoms 397 may also be sequentially pulsed as part of such a process. **Figure 12** shows the structure of **Figure 11** following the implantation of halogen atoms 397 such as fluorine into dielectric layer 345 and spacers 385. A representative concentration of halogen atoms 397 is on the order of $1E20$ to $2E22$. The presence of halogen atoms 397 in the dielectric material will tend to lower an overall parasitic capacitance associated with a transistor device.

Figure 13 shows the structure of **Figure 12** following the patterning of a metal line on the surface of the structure defined by dielectric layer 345A and the patterning of a second passivation layer (e.g., ILD1) and the implanting of halogen atoms into such passivation layer. Referring to **Figure 13**, the figure shows metal line 398 of an electrically conductive material such as a metal defined by the individual traces to contact 392A, contact 392B and

contact 395 (block 490, **Figure 15**). Metal line 398 is, for example, copper that may be introduced by an electroplating process. Following the formation of metal line 398, dielectric material 345B of, for example, silicon dioxide or low-k dielectric material may be introduced by a chemical vapor deposition process to form ILD1 (block 492, **Figure 15**). Subsequent to forming dielectric layer 345B, halogen atoms 397 may be implanted into the dielectric material (block 495, **Figure 15**). **Figure 14** shows the structure of **Figure 13** following the implantation of halogen atoms 397 into the dielectric material. The process of implanting halogen atoms may be repeated after the formation of each subsequent passivation layer (e.g., ILD2, ILD3, etc.). The process described allows the implantation of a halogen atom into passivation materials (dielectric materials) after device formation. Halogen atoms in passivation material will tend to lower a dielectric constant of these materials and improve overall parasitic capacitance of the integrated circuit device (e.g., a microprocessor). By performing the halogen atoms doping or implanting after device formation, potential issues such as poor etch selectivity and etch resistance in spacers or other passivation material is avoided.

Figure 16 illustrates interposer 500 that includes one or more embodiments. Interposer 500 is an intervening substrate used to bridge first substrate 502 to second substrate 504. First substrate 502 may be, for instance, an integrated circuit die including multigate transistor devices of the type described above. Second substrate 504 may be, for instance, a memory module, a computer motherboard, or another integrated circuit die. Generally, the purpose of interposer 500 is to spread a connection to a wider pitch or to reroute a connection to a different connection. For example, interposer 500 may connect an integrated circuit die to ball grid array (BGA) 506 that can subsequently be coupled to second substrate 504. In some embodiments, first and second substrates 502/504 are attached to opposing sides of interposer 500. In other embodiments, first and second substrates 502/504 are attached to the same side of interposer 500. In further embodiments, three or more substrates are interconnected by way of interposer 500.

Interposer 500 may be formed of an epoxy resin, a fiberglass-reinforced epoxy resin, a ceramic material, or a polymer material such as polyimide. In further implementations, the interposer may be formed of alternate rigid or flexible materials that may include the same materials described above for use in a semiconductor substrate, such as silicon, germanium, and other group III-V and group IV materials.

The interposer may include metal interconnects 508 and vias 510, including but not limited to through-silicon vias (TSVs) 512. Interposer 500 may further include embedded

devices 514, including both passive and active devices. Such devices include, but are not limited to, capacitors, decoupling capacitors, resistors, inductors, fuses, diodes, transformers, sensors, and electrostatic discharge (ESD) devices. More complex devices such as radio-frequency (RF) devices, power amplifiers, power management devices, antennas, arrays, sensors, and MEMS devices may also be formed on interposer 500.

Figure 17 illustrates computing device 600 in accordance with one embodiment. Computing device 600 may include a number of components. In one embodiment, these components are attached to one or more motherboards. In an alternate embodiment, these components are fabricated onto a single system-on-a-chip (SoC) die rather than a motherboard. The components in computing device 600 include, but are not limited to, integrated circuit die 602 and at least one communication chip 608. In some implementations communication chip 608 is fabricated as part of integrated circuit die 602. Integrated circuit die 602 may include CPU 604 as well as on-die memory 606, often used as cache memory, that can be provided by technologies such as embedded DRAM (eDRAM) or spin-transfer torque memory (STTM or STTM-RAM).

Computing device 600 may include other components that may or may not be physically and electrically coupled to the motherboard or fabricated within an SoC die. These other components include, but are not limited to, volatile memory 610 (e.g., DRAM), non-volatile memory 612 (e.g., ROM or flash memory), graphics processing unit 614 (GPU), digital signal processor 616, crypto processor 642 (a specialized processor that executes cryptographic algorithms within hardware), chipset 620, antenna 622, display or touchscreen display 624, touchscreen controller 626, battery 628 or other power source, a power amplifier (not shown), global positioning system (GPS) device 644, compass 630, motion coprocessor or sensors 632 (that may include an accelerometer, a gyroscope, and a compass), speaker 634, camera 636, user input devices 638 (such as a keyboard, mouse, stylus, and touchpad), and mass storage device 640 (such as hard disk drive, compact disk (CD), digital versatile disk (DVD), and so forth).

Communications chip 608 enables wireless communications for the transfer of data to and from computing device 600. The term “wireless” and its derivatives may be used to describe circuits, devices, systems, methods, techniques, communications channels, etc., that may communicate data through the use of modulated electromagnetic radiation through a non-solid medium. The term does not imply that the associated devices do not contain any wires, although in some embodiments they might not. Communication chip 608 may implement any of a number of wireless standards or protocols, including but not limited to

Wi-Fi (IEEE 802.11 family), WiMAX (IEEE 802.16 family), IEEE 802.20, long term evolution (LTE), Ev-DO, HSPA+, HSDPA+, HSUPA+, EDGE, GSM, GPRS, CDMA, TDMA, DECT, Bluetooth, derivatives thereof, as well as any other wireless protocols that are designated as 3G, 4G, 5G, and beyond. Computing device 600 may include a plurality of communication chips 608. For instance, a first communication chip may be dedicated to shorter range wireless communications such as Wi-Fi and Bluetooth and a second communication chip may be dedicated to longer range wireless communications such as GPS, EDGE, GPRS, CDMA, WiMAX, LTE, Ev-DO, and others.

Processor 604 of computing device 600 includes one or more devices, such as multigate transistors, that are formed in accordance with embodiments described above. The term “processor” may refer to any device or portion of a device that processes electronic data from registers and/or memory to transform that electronic data into other electronic data that may be stored in registers and/or memory.

Communication chip 608 may also include one or more devices, such as transistors, that are formed in accordance with embodiments.

In further embodiments, another component housed within computing device 600 may contain one or more devices, such as multigate transistors, that are formed in accordance with implementations.

In various embodiments, computing device 600 may be a laptop computer, a netbook computer, a notebook computer, an ultrabook computer, a smartphone, a tablet, a personal digital assistant (PDA), an ultra mobile PC, a mobile phone, a desktop computer, a server, a printer, a scanner, a monitor, a set-top box, an entertainment control unit, a digital camera, a portable music player, or a digital video recorder. In further implementations, computing device 600 may be any other electronic device that processes data.

EXAMPLES

The following examples pertain to embodiments:

Example 1 is a transistor including a channel; a source formed on one side of the channel and a drain formed on an opposite side of the channel; a gate electrode on the channel; and a spacer between the gate electrode and each of the source and the drain, wherein the sidewall spacer includes a concentration of a halogen atom.

In Example 2, the spacer of the transistor of Example 1 includes a dielectric material including nitrogen.

In Example 3, the spacer of the transistor of Example 2 includes one of silicon nitride,

silicon oxynitride, silicon oxycarbon nitride, silicon oxyboron nitride and silicon oxycarbon boron nitride.

In Example 4, the spacer of the transistor of Example 1 includes an oxide.

In Example 5, the spacer of the transistor of Example 4 includes silicon dioxide.

5 In Example 6, the spacer of the transistor of Example 1 or 2 includes a material having a dielectric constant greater than a dielectric constant of silicon dioxide.

In Example 7, the halogen of the transistor of any of Examples 1-6 includes fluorine.

Example 8 is a method of forming an integrated circuit device including forming a plurality of transistor devices on a substrate; insulating the plurality of transistor devices with
10 a dielectric material; and implanting the dielectric material with a concentration of a halogen atom.

In Example 9, prior to implanting the dielectric material with a halogen atom, the method of Example 8 includes forming contacts to ones of the plurality of transistors.

15 In Example 10, insulating the plurality of transistors with a dielectric material in the method of Example 8 or 9 includes forming spacers adjacent opposite sides of a gate electrode of each of the plurality of transistors.

In Example 11, forming spacers adjacent opposite sides of a gate electrode in the method of Example 10 includes a first insulating with a first dielectric material, the method including second insulating of the plurality of transistor devices with a second dielectric
20 material after the first insulating.

In Example 12, the method of Example 11 further includes implanting the second dielectric material with a concentration of a halogen atom after implanting the first dielectric material.

25 In Example 13, the halogen atom in the method of any of Examples 8-12 includes fluorine.

In Example 14, the dielectric material in the method of any of Examples 8-12 includes nitrogen.

In Example 15, the first dielectric material and the second dielectric material in the method of Example 11 are different.

30 Example 16 is a method of forming an integrated circuit device including forming a transistor device including a gate electrode on a channel on a substrate, a source on one side of the gate electrode, a drain on an opposite side of the gate electrode and the gate electrode separated from each of the source and the drain by a dielectric material; forming contacts to the gate electrode and each of the source and the drain; and after forming contacts,

implanting the dielectric material with a halogen atom.

In Example 17, the dielectric material in the method of Example 16 includes nitrogen.

In Example 18, the dielectric material in the method of Example 17 includes one of silicon nitride, silicon oxynitride, silicon oxycarbon nitride, silicon oxyboron nitride and

5 silicon oxycarbon boron nitride.

In Example 19, the dielectric material in the method of Example 16 includes an oxide.

In Example 20, the dielectric material in the method of Example 19 includes silicon dioxide.

In Example 21, the dielectric material in the method of Example 16 includes a
10 material having a dielectric constant greater than a dielectric constant of silicon dioxide.

In Example 22, the halogen in the method of Example 16 includes fluorine.

In Example 23, after implanting the dielectric material, the method of Example 16 includes forming a dielectric layer on the transistor device and, after forming the dielectric layer, the method includes implanting the dielectric material with a halogen atom.

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The above description of illustrated implementations, including what is described in the Abstract, is not intended to be exhaustive or to limit the invention to the precise forms disclosed. While specific implementations of, and examples for, the invention are described herein for illustrative purposes, various equivalent modifications are possible within the
20 scope, as those skilled in the relevant art will recognize.

These modifications may be made in light of the above detailed description. The terms used in the following claims should not be construed to limit the invention to the specific implementations disclosed in the specification and the claims. Rather, the scope of the invention is to be determined entirely by the following claims, which are to be construed
25 in accordance with established doctrines of claim interpretation.

CLAIMS

1. A transistor comprising:
a channel;
5 a source formed on one side of the channel and a drain formed on an opposite side of the channel;
a gate electrode on the channel; and
a spacer between the gate electrode and each of the source and the drain, wherein the sidewall spacer comprises a concentration of a halogen atom.
10
2. The transistor of claim 1, wherein the spacer comprises a dielectric material comprising nitrogen.
3. The transistor of claim 2, wherein the spacer comprises one of silicon nitride, silicon
15 oxynitride, silicon oxycarbon nitride, silicon oxyboron nitride and silicon oxycarbon boron nitride.
4. The transistor of claim 1, wherein the spacer comprises an oxide.
- 20 5. The transistor of claim 4, wherein the spacer comprises silicon dioxide.
6. The transistor of claim 1, wherein the spacer comprises a material having a dielectric constant greater than a dielectric constant of silicon dioxide.
- 25 7. The transistor of claim 1, wherein the halogen comprises fluorine.
8. A method of forming an integrated circuit device comprising:
forming a plurality of transistor devices on a substrate;
insulating the plurality of transistor devices with a dielectric material; and
30 implanting the dielectric material with a concentration of a halogen atom.
9. The method of claim 8, wherein prior to implanting the dielectric material with a halogen atom, the method comprises forming contacts to ones of the plurality of transistors.

10. The method of claim 8, wherein insulating the plurality of transistors with a dielectric material comprises forming spacers adjacent opposite sides of a gate electrode of each of the plurality of transistors.

11. The method of claim 10, wherein forming spacers adjacent opposite sides of a gate electrode comprises a first insulating with a first dielectric material, the method comprising second insulating of the plurality of transistor devices with a second dielectric material after the first insulating.

12. The method of claim 11, wherein the method further comprises implanting the second dielectric material with a concentration of a halogen atom after implanting the first dielectric material.

13. The method of claim 8, wherein the halogen atom comprises fluorine.

14. A method of forming an integrated circuit device comprising:
forming a transistor device comprising a gate electrode on a channel on a substrate, a source on one side of the gate electrode, a drain on an opposite side of the gate electrode and the gate electrode separated from each of the source and the drain by a dielectric material;
forming contacts to the gate electrode and each of the source and the drain; and
after forming contacts, implanting the dielectric material with a halogen atom.

15. The method of claim 14, wherein the dielectric material comprises nitrogen.

16. The method of claim 15, wherein the dielectric material comprises one of silicon nitride, silicon oxynitride, silicon oxycarbon nitride, silicon oxyboron nitride and silicon oxycarbon boron nitride.

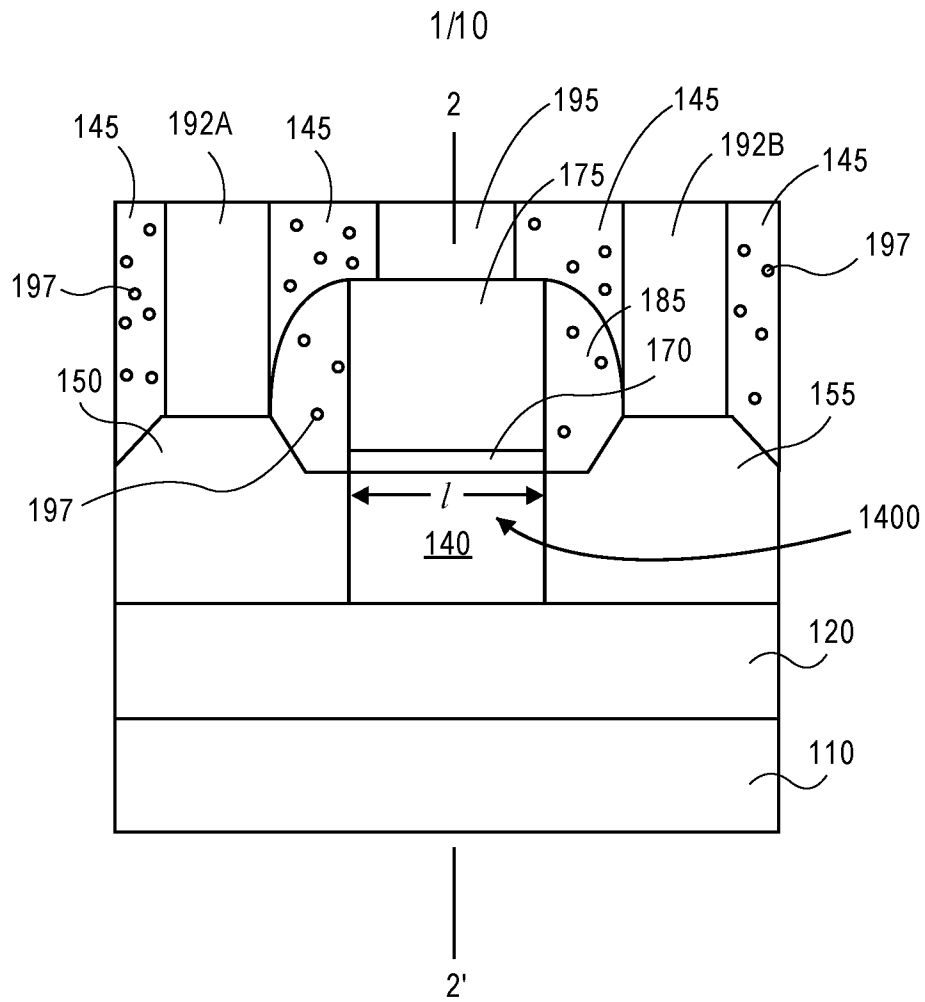
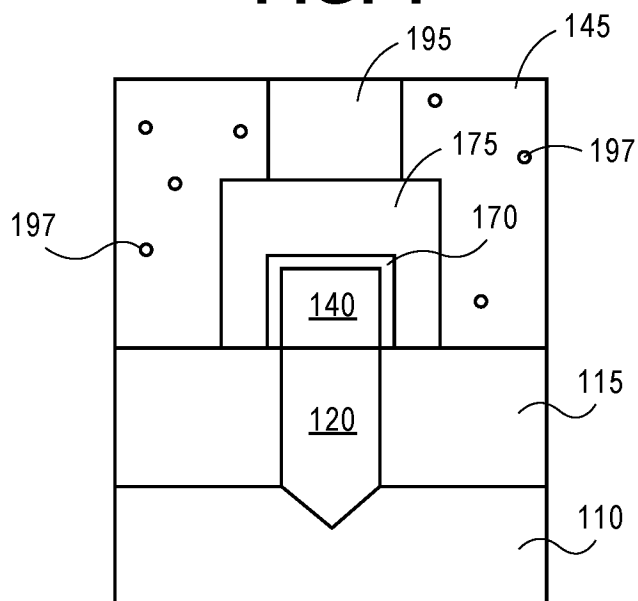
17. The method of claim 14, wherein the dielectric material comprises an oxide.

18. The method of claim 17, wherein the dielectric material comprises silicon dioxide.

19. The method of claim 14, wherein the dielectric material comprises a material having a dielectric constant greater than a dielectric constant of silicon dioxide.

20. The method of claim 14, wherein the halogen comprises fluorine.

21. The method of claim 14, wherein after implanting the dielectric material, the method
5 comprises forming a dielectric layer on the transistor device and, after forming the dielectric layer, the method comprises implanting the dielectric material with a halogen atom.

**FIG. 1****FIG. 2**

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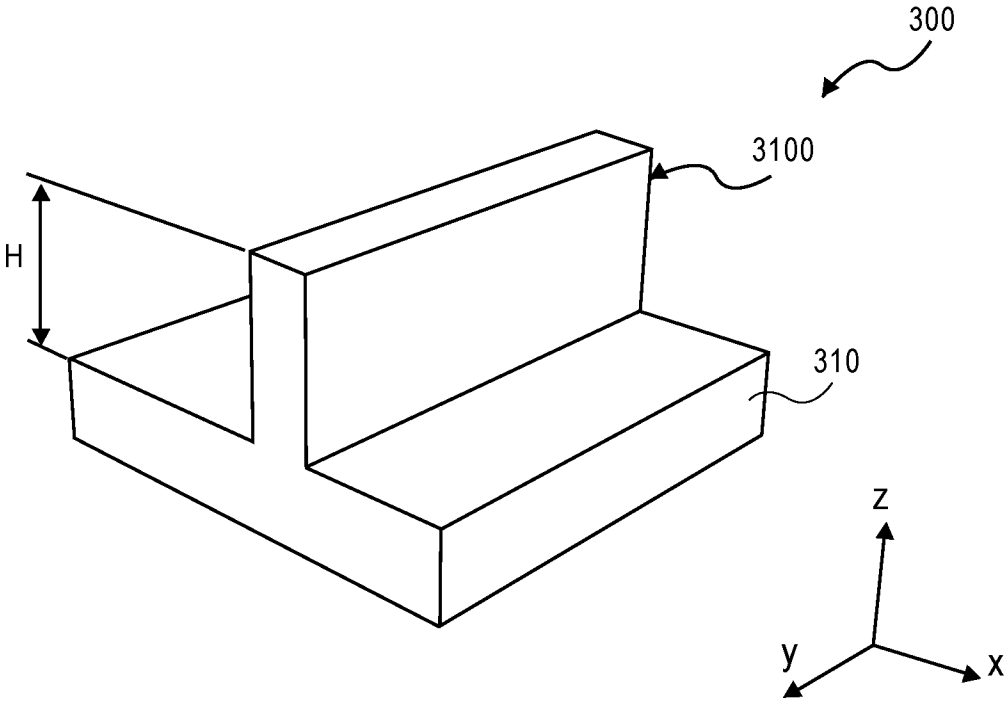


FIG. 3

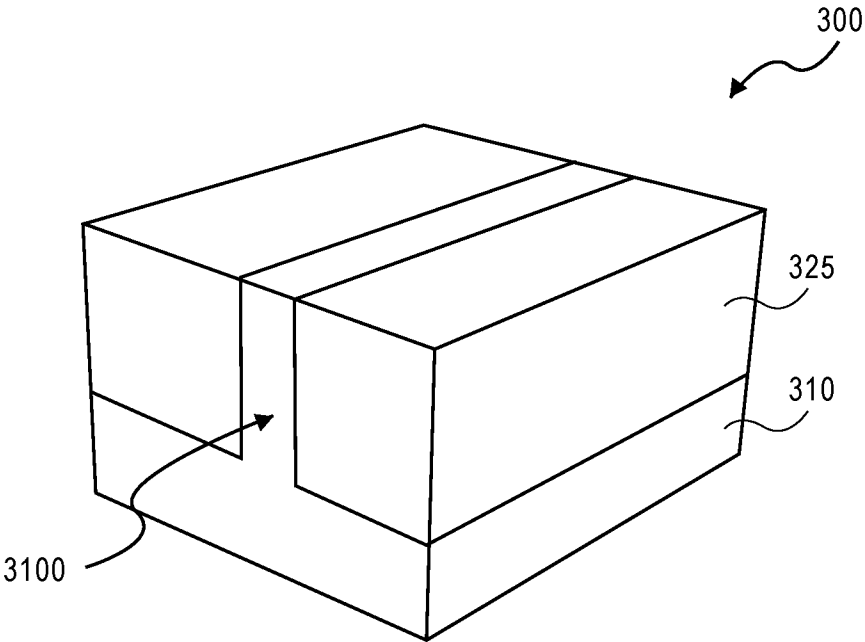


FIG. 4

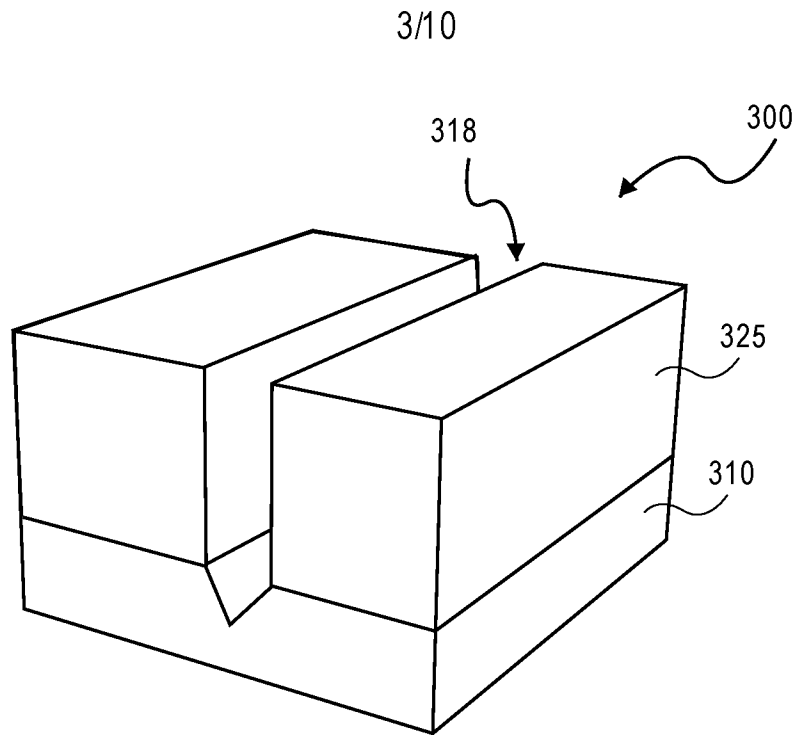


FIG. 5

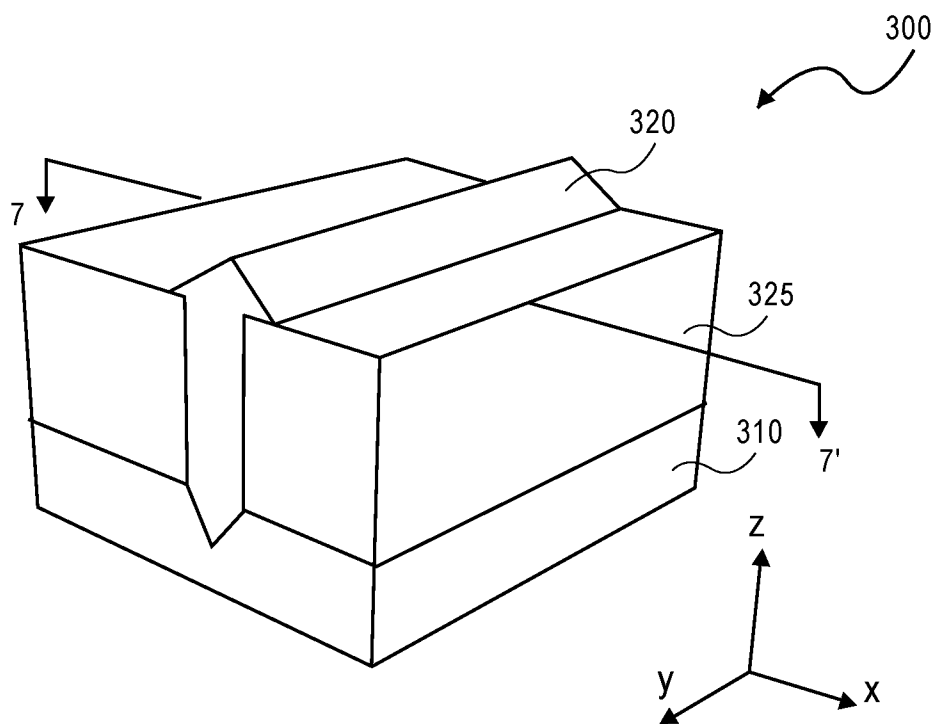


FIG. 6

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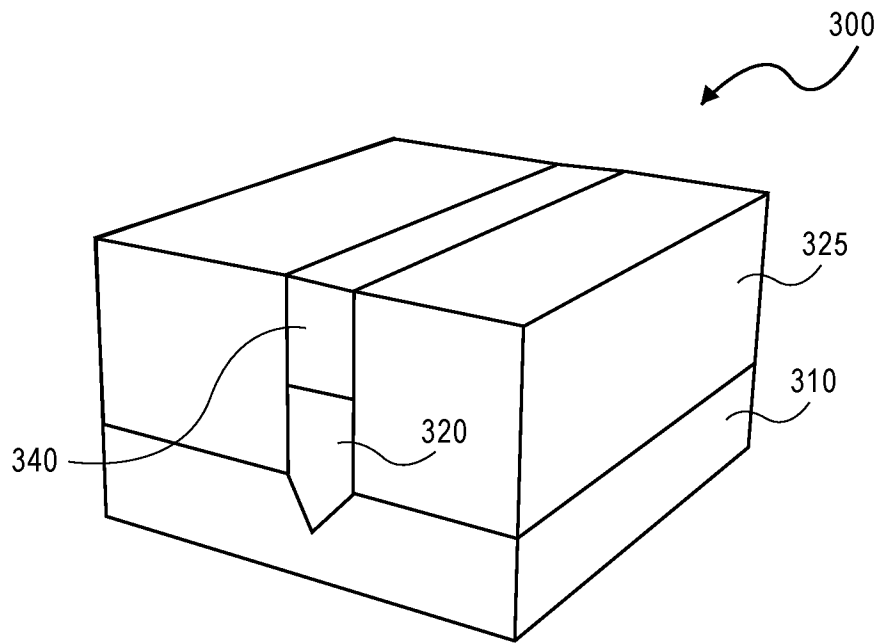


FIG. 7

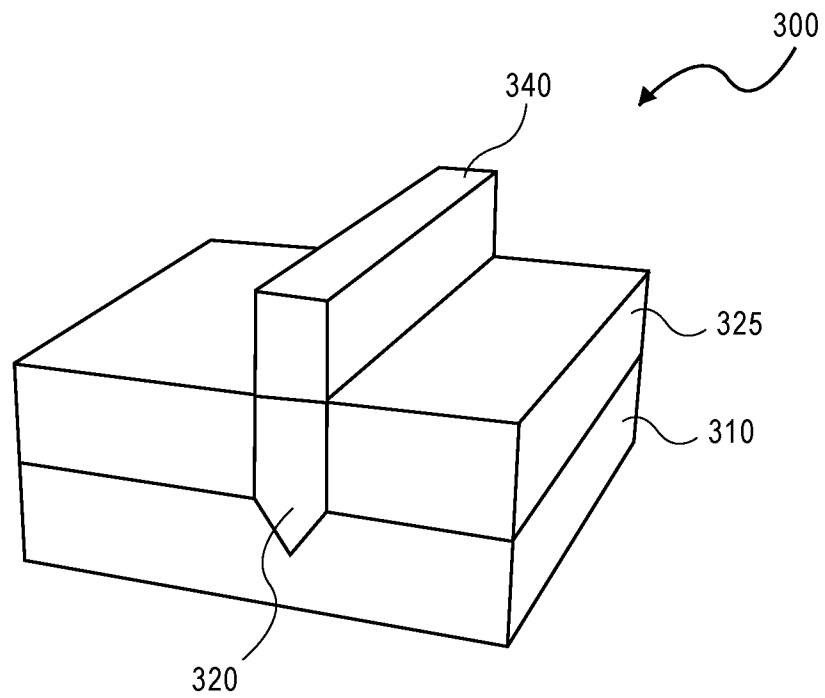
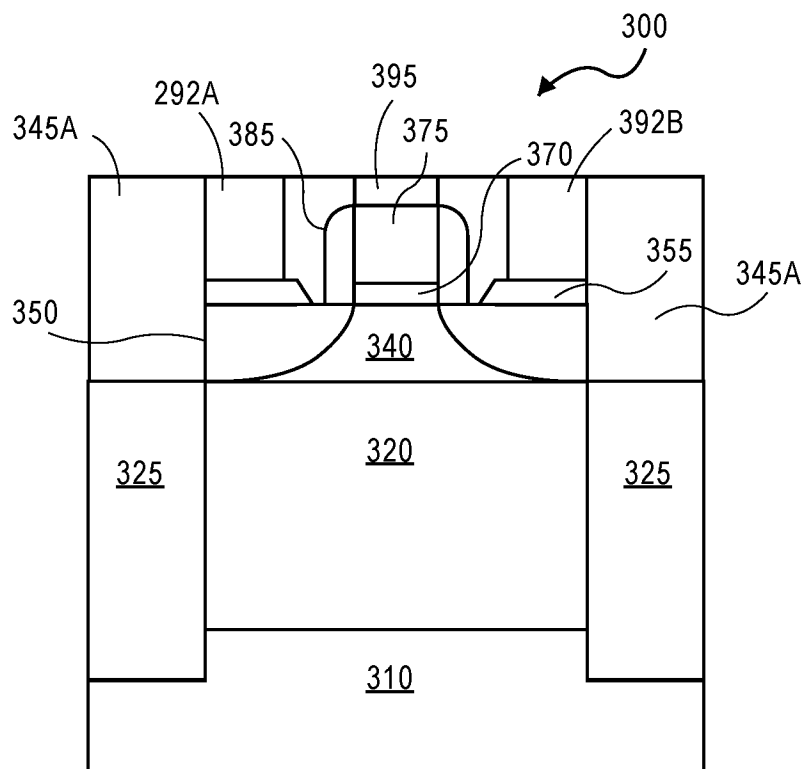
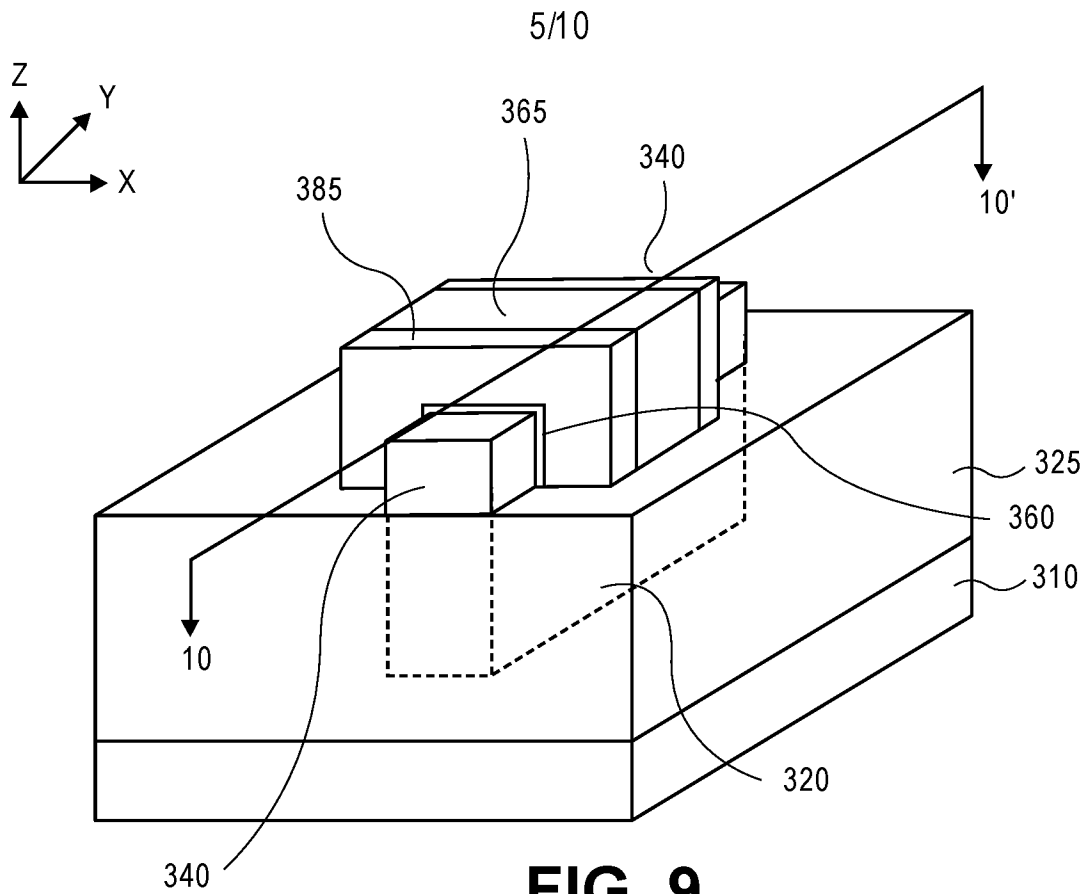


FIG. 8



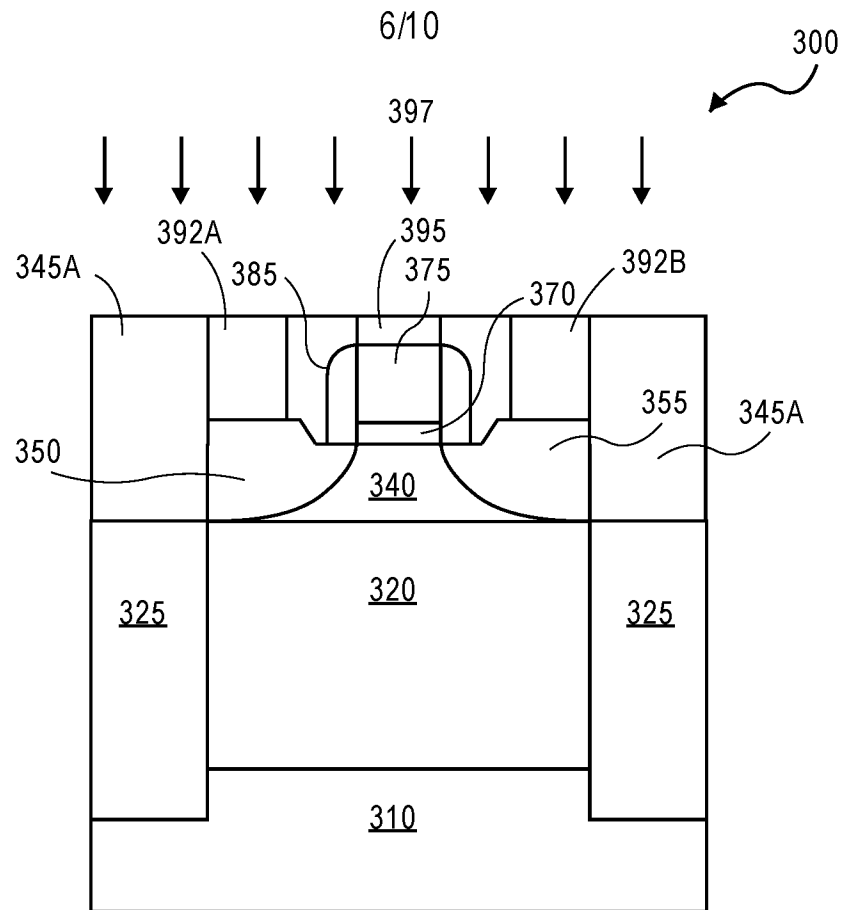


FIG. 11

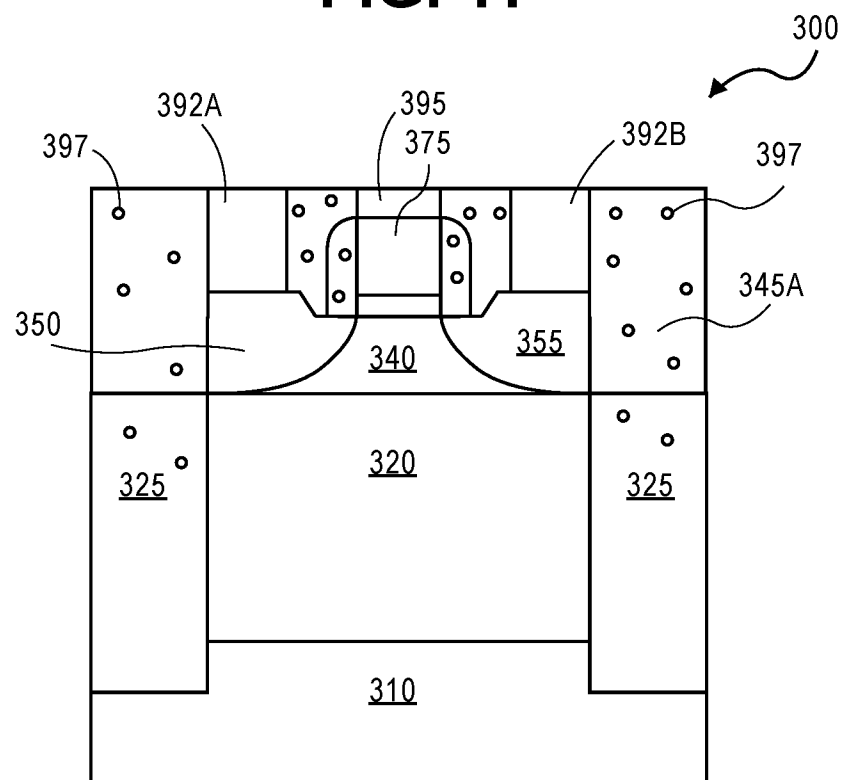


FIG. 12

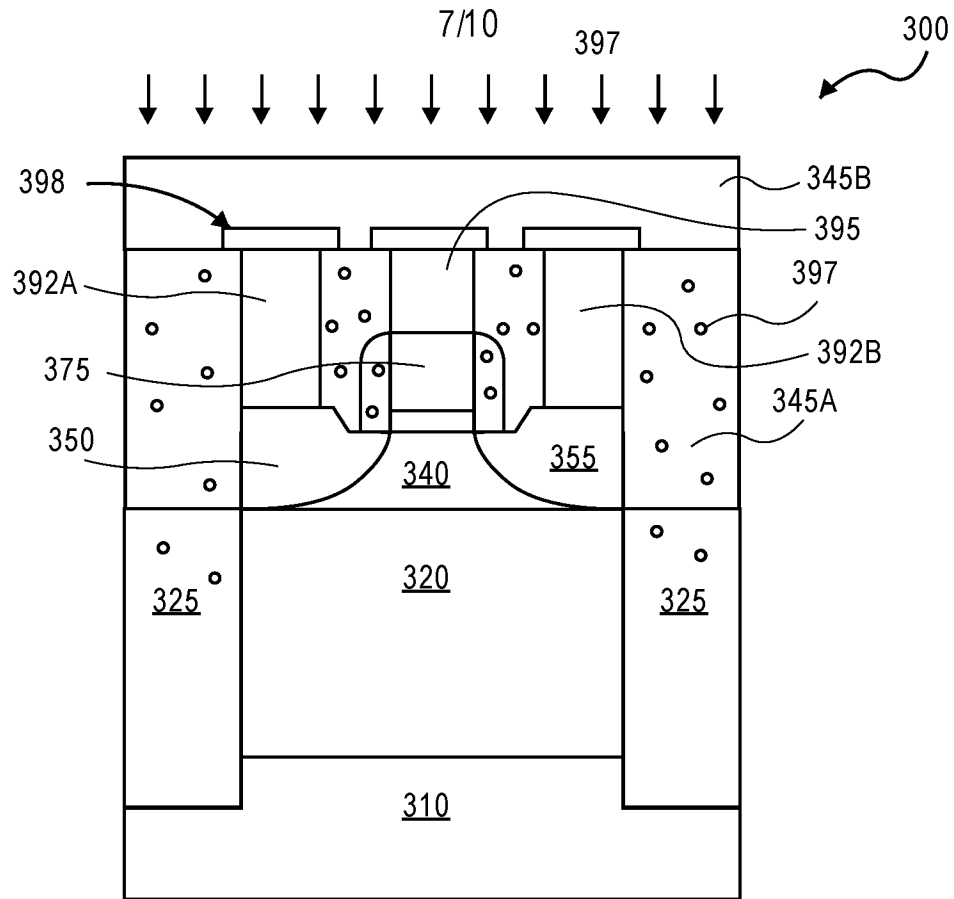


FIG. 13

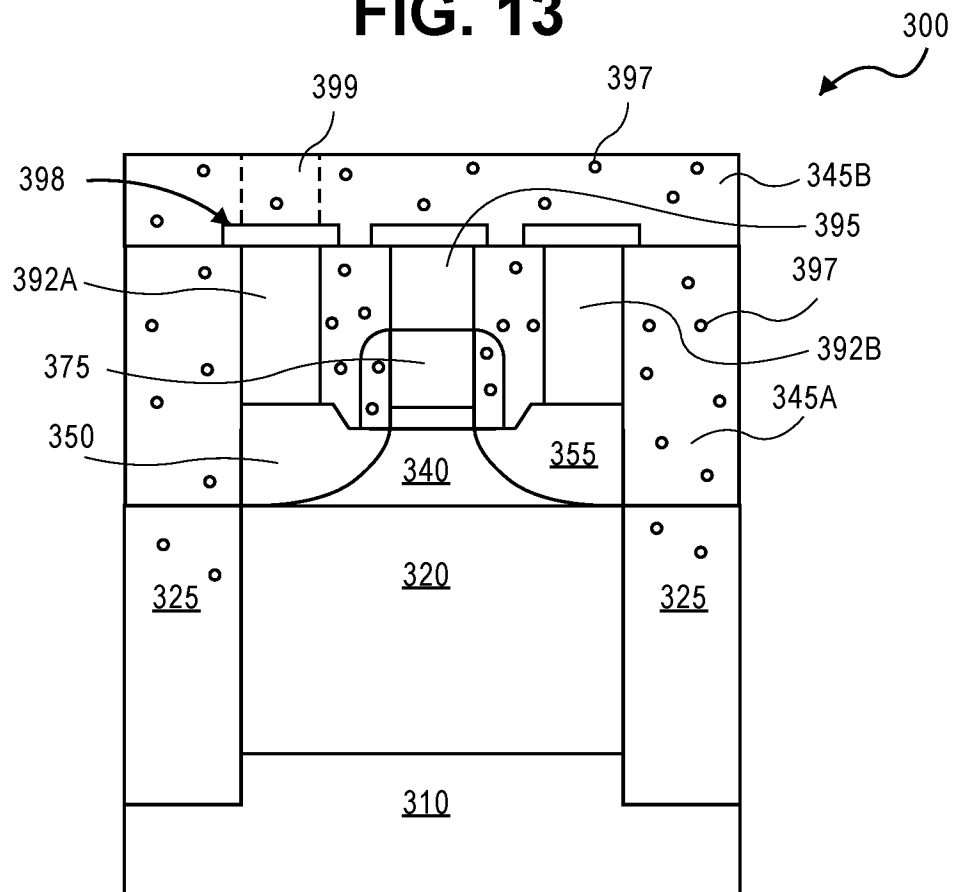
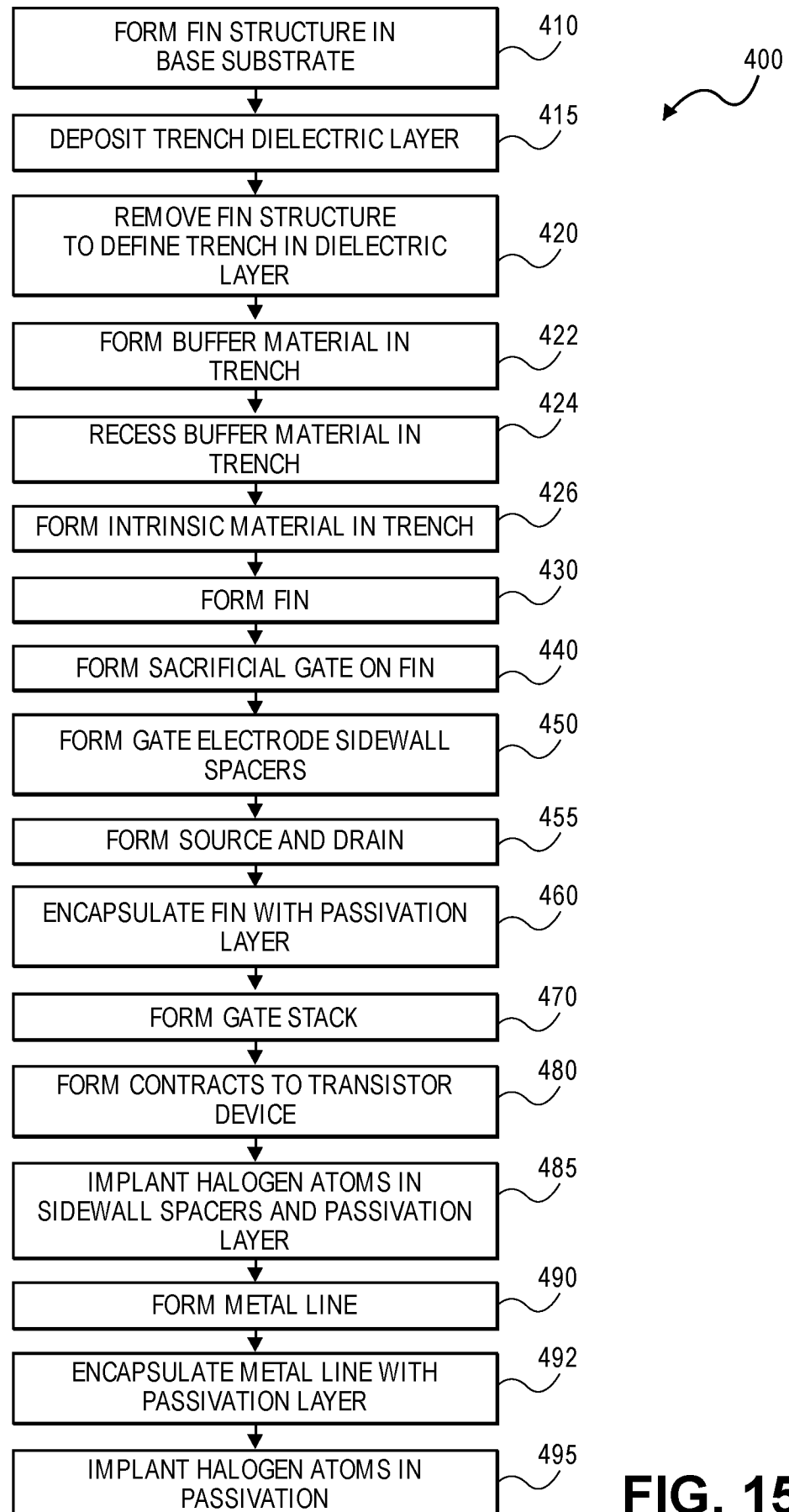


FIG. 14

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**FIG. 15**

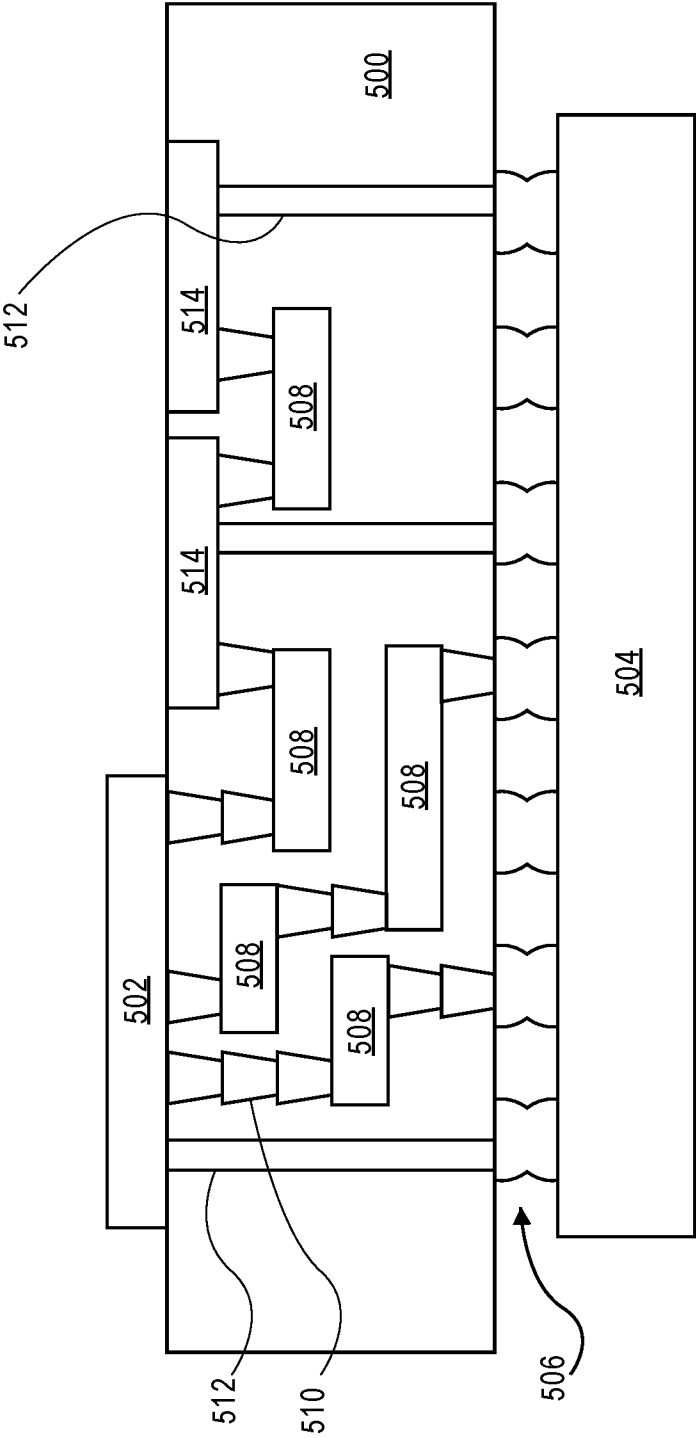


FIG. 16

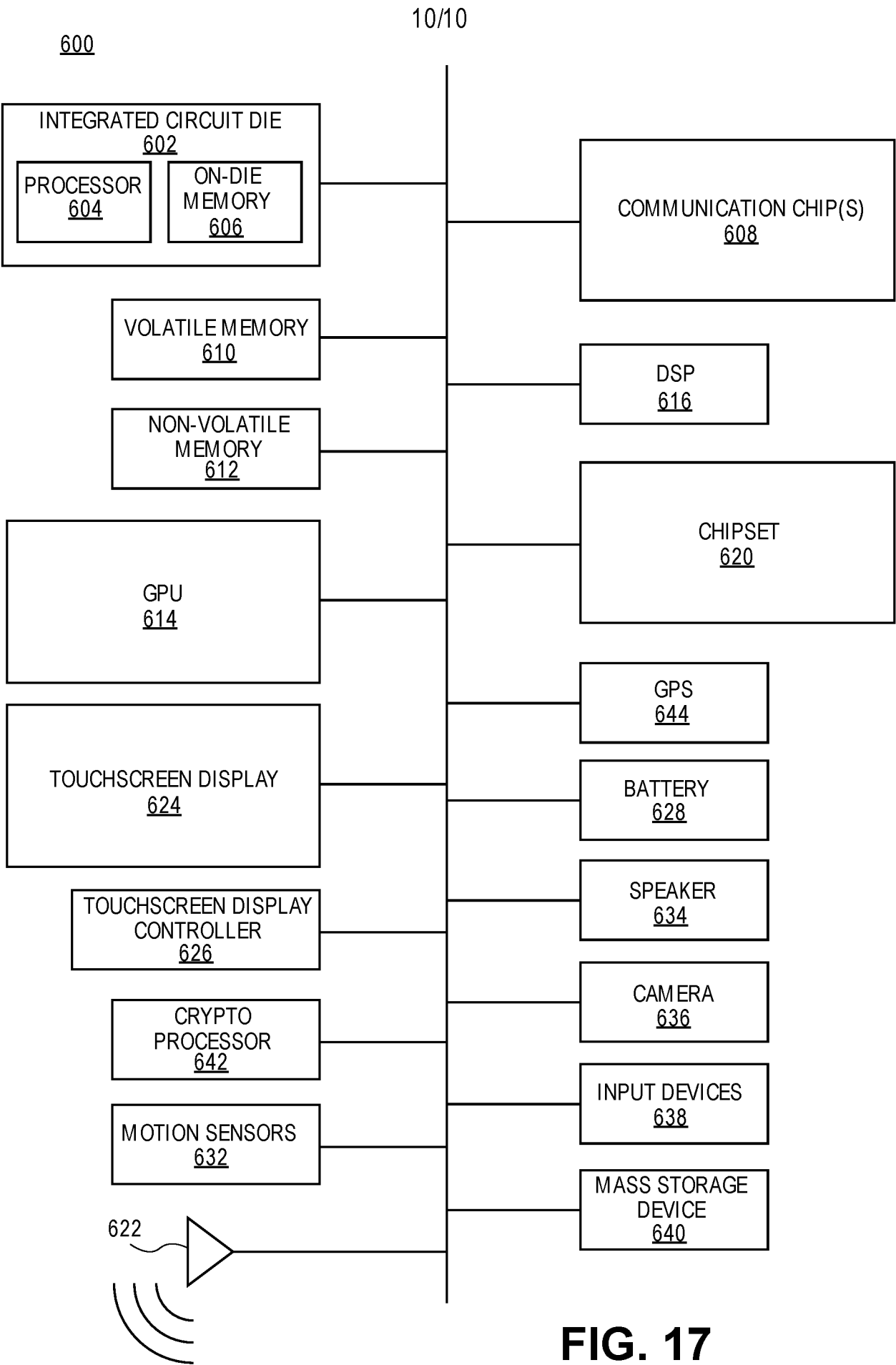


FIG. 17

A. CLASSIFICATION OF SUBJECT MATTER**H01L 29/78(2006.01)i, H01L 29/66(2006.01)i, H01L 49/02(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 29/78; H01L 29/49; H01L 21/4763; H01L 21/336; H01L 21/8238; H01L 29/76; H01L 29/66; H01L 49/02

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: spacer, implant, halogen, capacitance, CMOS

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2011-0031538 A1 (HSIEH et al.) 10 February 2011 See paragraphs [0006],[0011],[0018], claims 1,5,7,9,16 and figure 7.	1-21
A	US 2005-0275034 A1 (DESHPANDE et al.) 15 December 2005 See claim 11 and figure 9.	1-21
A	US 2010-0006956 A1 (CHANG et al.) 14 January 2010 See claims 8-10 and figure 1G.	1-21
A	US 2003-0017689 A1 (AKRAM et al.) 23 January 2003 See paragraphs [0034]-[0036] and figures 8-10.	1-21
A	US 7033897 B2 (CHEN et al.) 25 April 2006 See claims 1,15 and figures 19-21.	1-21



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents:

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"E" earlier application or patent but published on or after the international filing date

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

31 August 2017 (31.08.2017)

Date of mailing of the international search report

31 August 2017 (31.08.2017)

Name and mailing address of the ISA/KR

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2016/069260

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2011-0031538 A1	10/02/2011	CN 102214693 A CN 102214693 B US 8299508 B2	12/10/2011 29/05/2013 30/10/2012
US 2005-0275034 A1	15/12/2005	None	
US 2010-0006956 A1	14/01/2010	CN 101388340 A CN 101388340 B US 2009-0065876 A1 US 2009-0298275 A1 US 2010-0327376 A1 US 2012-0187506 A1 US 7776732 B2 US 7843007 B2 US 7855135 B2 US 8216907 B2 US 8502325 B2	18/03/2009 24/11/2010 12/03/2009 03/12/2009 30/12/2010 26/07/2012 17/08/2010 30/11/2010 21/12/2010 10/07/2012 06/08/2013
US 2003-0017689 A1	23/01/2003	AU 1933199 A JP 2002-509361 A KR 10-0389899 B1 US 2006-0001054 A1 US 2007-0020868 A1 US 6288433 B1 US 6593196 B2 US 7105411 B1 US 7189623 B2 WO 99-31732 A2 WO 99-31732 A3	05/07/1999 26/03/2002 04/07/2003 05/01/2006 25/01/2007 11/09/2001 15/07/2003 12/09/2006 13/03/2007 24/06/1999 29/07/1999
US 7033897 B2	25/04/2006	US 2005-0087775 A1 US 2005-0263834 A1	28/04/2005 01/12/2005