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(54) IMPROVEMENTS IN OR RELATING TO SEMICONDUCTOR STORES

(71) We, SIEMENS AKTIENGESELLSCHAFT, a German Company of Berlin and Munich, German Federal Republic, do hereby declare the invention, for which we

pray that a patent may be granted to us, and the method by which it is to be performed to be particularly described in and by the following statement:—

The present invention relates to semiconductor stores and more particularly to such stores in which the individual storage cells comprise a V-MOS transistor and a storage capacitor.

Semiconductor storage cells comprising one transistor (single-transistor storage cells) are usually made up of a MOS-transistor (which is also referred to as selector transistor) connected to a storage capacitor, in which the item of information to be stored is contained as a charge. The storage cell so composed is arranged between a word line and a bit line, the word line being connected to the control input (i.e. the gate) of the selector transistor, whilst the one of the controlled electrodes of the selector transistor (i.e. the source or drain electrode) is connected to or forms part of the bit line. The other controlled electrode of the transistor is connected to the storage capacitor. Single-transistor storage cells of this kind have the advantage that they can be constructed in a semiconductor substrate in a very small space.

It is known to produce MOS transistors by means of the so-called V-MOS technique, in which a V-section trench is etched into an epitaxial semiconductor layer arranged on a semiconductor substrate. In this trench there is arranged an insulating layer up which a terminal for the control electrode of the MOS transistor is then provided. The channel of the MOS transistor runs along the flanks of the trench. The two controlled electrodes of the MOS transistor can, for example, be arranged alongside the V-section trench.

In one prior art method of constructing a semiconductor storage cell which consists of a MOS selector transistor controlled by a drive line and of a storage capacitor connected to the selector transistor, and in which the selector transistor is produced used the V-MOS technique, in a highly doped semiconductor substrate of one conductivity type, there is arranged a highly doped buried layer of the other conductivity type. A weakly doped epitaxial layer of the one conductivity type is then arranged on the semiconductor substrate above the buried layer, and a trench of V-shaped cross-section is cut into the surface of the epitaxial layer so that its apex extends into the buried layer. The V-MOS transistor serving as the selector transistor is formed in the epitaxial layer extending across the trench.

The single-transistor storage cell so formed has a very high bit density and can be produced by means of conventional photolithographic processes with structure resolutions of 5μm. However, an epitaxial layer is required for its formation, which slows down mass production.

It is an object of the present invention to provide a semiconductor store of the type referred to above, which does not require the use of an epitaxial layer in its production.

According to the invention, there is provided a semiconductor store comprising a plurality of storage cells each comprising an MOS-selector transistor produced using the V-MOS technique, and a storage capacitor, each said storage cell being formed in a semiconductor body of one conductivity type and comprising a buried layer of the other conductivity type formed in said body, two further layers extending between said buried layer and a surface of said body, said buried layer and said further layers being of alternating conductivity type, and a trench of V-shaped cross-section formed in said surface and extending at least to said buried layer, said buried layer and said further layers being produced in said body by diffusion and/or implantation, and said storage capacitor being formed by the p-n junction between said buried layer and the adjacent one of said further layers, or between said two further layers.

The V-section trench preferably also divides the buried layer into two parts. It is advantageous if one of the layers serves as a bit line. Preferably this layer is one which adjoins the surfaces of the semiconductor body. Alternatively, the bit line may be formed by the buried layer.

The semiconductor store of the invention is characterised by a simple construction and does not include an epitaxial layer. Consequently, it can be produced in a particularly simple way and is thus suitable for mass production.

The invention will now be further described with reference to the drawing, in which:—

Figures 1 and 2 are similar schematic side-sectional views of part of a semiconductor body to illustrate the production of a first embodiment of the invention;

Figure 3 is a schematic side-sectional view of part of a semiconductor body to illustrate a second embodiment of the invention;

Figures 4 and 5 are similar schematic side-sectional views of part of a semiconductor body to illustrate the production of a third embodiment of the invention; and

Figure 6 is a schematic side-sectional view of part of a semiconductor body to illustrate a fourth embodiment of the invention.

Referring to Figure 1, an n^+-doped zone 2 having a doping concentration of about 10^{16} dopant atoms/cm^3 is introduced by diffusion or implantation into a p-doped semiconductor body 1. This n^+-doped zone will eventually form a part of a buried p-n storage capacitor. Then, using diffusion of implantation, a p^+-conducting zone 3 is formed in the entire surface of the body 1, which serves as a "channel-stop" and also serves to form the buried storage capacitor. Finally an n^+-conducting zone 4 is formed by diffusion or implantation in the surface of the zone 3; this zone serves for subsequent formation of the source and drain zones. The zone 3 has a doping concentration of 10^{18} dopant atoms/cm^3. The zone 4 has a doping concentration of 5×10^{19} dopant atoms/cm^3.

In this way, the arrangement illustrated in Figure 1 is formed.

As shown in Figure 2, a trench having a V-shaped cross-section is then cut into the surface of the arrangement illustrated in Figure 1, for example, by means of photolithography using a photo-lacquer and etching. The trench 5 divides the zones 3 and 4 into two parts and its apex extends into the buried zone 2. A thick oxide layer 7 is produced on the original remaining surface of the body 1, whilst a thin oxide layer 6 is formed on the surface of the flanks of the trench 5. Both oxide layers consist of silicon dioxide.

The arrangement shown in Figure 2 thus possesses n-conducting zones 2 and 4 and p-conducting zones 1 and 3. The storage capacitor is formed by the zones 2 and 3. The zone 4 serves as a bit line. The zone 3 lying between the zone 4 and the zone 2 of the storage capacitor represents the channel of the selector transistor.

Figure 3 illustrates an arrangement which is basically similar to that shown in Figure 2, differing from it in that the trench 5 extends through the zone 2 into the semiconductor material 1.

In the exemplary embodiments shown in Figures 1 to 3, the p-n storage capacitor is in each case arranged beneath the bit line 4 and the channel zone. If, however, a doping as described above is assumed, the p-n storage capacitance relative to the surface will be smaller than the bit line capacitance relative to the surface.

In order to improve this unfavourable ratio between the p-n storage capacitance and the bit line capacitance, the portions of the bit line and the p-n storage capacitor can be interchanged. Embodiments in which this is effected are shown in Figures 4 to 6.

Referring to Figure 4, an n-conducting zone 12 having a doping concentration of 10^{16} doping atoms/cm^3 is first introduced into a p-conducting semiconductor material 11. This zone 12 has smaller lateral dimensions than the zone 2 of Figure 1. Then, as in the embodiment of Figure 1, a p^+-conducting zone 13 having a doping atom concentration of 5×10^{17}/cm^3 is produced at the surface of the body. Finally, an n^+-conducting zone 14 having a doping concentration of 5×10^{19} doping atoms/cm^3 is formed in the surface of the zone 13 above the zone 12. The zones 12, 13 and 14 can each be formed by diffusion or by implantation.

In the surface of the arrangement shown in Figure 4 there is formed a trench 15 of V-shaped cross-section which can either extend into the zone 12 (Figure 5) or through the zone 12 into the original part of the semiconductor body 11 (Figure 6). A thin oxide layer 16 consisting of silicon dioxide is formed on the flanks of the trench, while a thicker oxide layer 17 also consisting of silicon dioxide is produced on the surface of the body outside the trench.

In the embodiment illustrated in Figure 5, the zones 12 and 14 are n-conducting, whilst the zone 11 is p-conducting.

The zones 13 and 14 form the storage capacitor. The channel of the selector transistor lies between the zones 14 and 12. The zone 12 forms the bit line.

WHAT WE CLAIM IS:—

1. A semiconductor store comprising a

plurality of storage cells each comprising an MOS-selector transistor produced using the V-MOS technique, and a storage capacitor, each said storage cell being formed in a semiconductor body of one conductivity type and comprising a buried layer of the other conductivity type formed in said body, two further layers extending between said buried layer and a surface of said body, said buried layer and said further layers being of alternating conductivity type, and a trench of V-shaped cross-section formed in said surface and extending at least to said buried layer, said buried layer and said further layers being produced in said body by diffusion and/or implantation, and said storage capacitor being formed by the p-n junction between said buried layer and the adjacent one of said further layers, or between said two further layers.

2. A semiconductor store as claimed in Claim 1, wherein said trench divides said buried layer into two parts.

3. A semiconductor store as claimed in Claim 1 or Claim 2, wherein one of said layers forms a bit line.

4. A semiconductor store as claimed in Claim 3, wherein said bit line is formed by the further layer which adjoins the surface of said semiconductor body.

5. A semiconductor store as claimed in Claim 3, wherein said bit line is formed by said buried layer.

6. A semiconductor store substantially as hereinbefore described with reference to and as illustrated in Figures 1 and 2, or Figure 3, or Figures 4 and 5, or Figure 6, of the drawing.

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1 SHEET *This drawing is a reproduction of the Original on a reduced scale*

Fig. 1

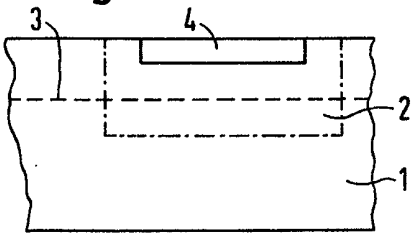

Fig. 2

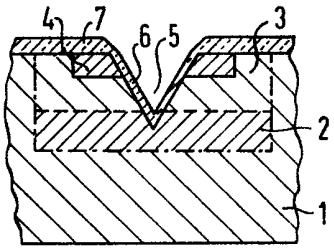

Fig. 3

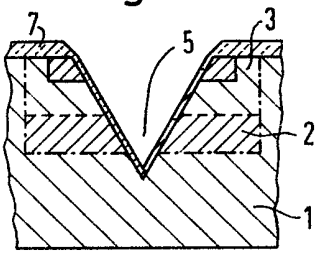

Fig. 4

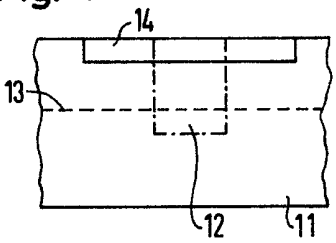

Fig. 5

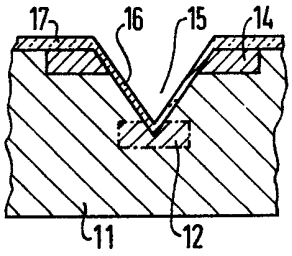

Fig. 6