

(43) International Publication Date
24 November 2016 (24.11.2016)

- (51) International Patent Classification:
G05F 1/70 (2006.01) *H02M 1/42* (2007.01)
- (21) International Application Number:
PCT/US2016/033138
- (22) International Filing Date:
18 May 2016 (18.05.2016)
- (25) Filing Language: English
- (26) Publication Language: English
- (30) Priority Data:
14/715,051 18 May 2015 (18.05.2015) US
- (63) Related by continuation (CON) or continuation-in-part (CIP) to earlier application:
US 14/715,051 (CON)
Filed on 18 May 2015 (18.05.2015)
- (71) Applicant: TEXAS INSTRUMENTS INCORPORATED [US/US]; P.O. Box 655474, Mail Station 3999, Dallas, TX 75265-5474 (US).
- (71) Applicant (for JP only): TEXAS INSTRUMENTS JAPAN LIMITED [JP/JP]; 24-1, Nishi-Shinjuku 6-Chome, Shinjuku-ku Tokyo, 160-8366 (JP).
- (72) Inventor: CHOUDHURY, Shamim, A.; 20507 Cajon Canyon Court, Katy, TX 77450 (US).
- (74) Agents: DAVIS, Michael A., Jr. et al.; Texas Instruments Incorporated, P.O. Box 655474, Mail Station 3999, Dallas, TX 75265-5474 (US).

(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JP, KE, KG, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Declarations under Rule 4.17:

- as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))
- as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))

Published:

- with international search report (Art. 21(3))

(54) Title: POWER FACTOR CORRECTION

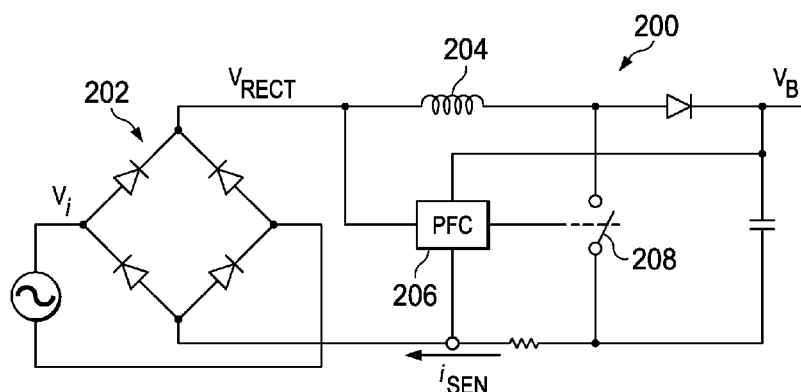


FIG. 2A

(57) Abstract: In described examples, a power supply (200) includes a power factor correction module (206) that is real-time adaptive based on the operating conditions.

POWER FACTOR CORRECTION

BACKGROUND

[0001] Electrical power supplies commonly use diode rectifier circuits to convert from alternating current (AC) to direct current (DC). A diode rectifier conducts current only when the input voltage of the rectifier exceeds the output voltage of the rectifier, so a sinusoidal input voltage results in intermittent non-sinusoidal current flow. The intermittent current flow has a primary frequency component equal to the AC input frequency and substantial energy at integer multiples of the AC input frequency (harmonics). Input current harmonics can cause transient current flow in the AC mains, which can increase the power required from the AC mains and can cause heating of the distribution system. Also, input current harmonics create electrical noise that can interfere with other systems connected to the AC mains. Increased power, heating, and electrical noise are especially important considerations for uninterruptable power supply (UPS) systems used to provide AC power in large computer server systems.

[0002] The power factor of a power supply is the ratio of the real power delivered to a load divided by the apparent input power, where the apparent input power is the root-mean-square (RMS) input voltage times RMS input current. Generally, input current harmonics cause the RMS value of the input current to be substantially higher than the current delivered to the load. Many power supplies include power factor correction to reduce input current harmonics. Some jurisdictions legally require power factor correction for supplies with output power over a specified limit, which includes most power supplies for computer systems.

[0003] FIG. 1A illustrates an example of part of a power supply 100 (simplified to facilitate illustration and discussion) with conventional power factor correction. An AC input voltage V_i is rectified by a full-wave rectifier 102. An inductor 104 provides energy storage to enable a continuous input current. A power factor correction (PFC) module 106 controls an electronic switch 108 using pulse-width-modulation (PWM) to control the DC output voltage V_B and to generate a continuous sinusoidal input current in phase with the input voltage V_i . The circuit of FIG. 1A may be a front end to a DC-DC converter. Alternatively, there may be multiple

inductors and switches driving multiple DC outputs, which in turn may connect to multiple DC-DC converters.

[0004] FIG. 1B illustrates an example of additional detail for the PFC module 106 of FIG. 1A. The output bus voltage V_B is subtracted from a reference voltage V_{REF} at a summing node 110. The resulting voltage error signal is input to a voltage loop controller 112, which regulates the bus voltage V_B to be equal to V_{REF} . An RMS calculator 114 computes the inverse of the square of the RMS value of the input voltage V_i . The output of controller 112 is multiplied by $1/V_{i_{RMS}}^2$ by a multiplier 116. That result is multiplied by the input voltage V_i by a multiplier 118 with a gain of K , the value of which depends on system parameters. That result is used as a sinusoidal reference signal i_{REF} for a current control loop. Sensed current I_{SEN} is subtracted from the reference current signal i_{REF} at a summing node 120, and resulting current error signal is processed by a current loop controller 122, and the result is used to generate the PWM output that controls the electronic switch 108.

[0005] For some power supplies, such as power supplies used for computer servers, the operating conditions may vary widely, with input voltages ranging from 90V to 264V, and output loads varying from zero to full load. Under such varying operating conditions, the PFC power stage characteristics can change significantly, which results in a corresponding significant change in gain, bandwidth, and stability margins (phase margin and gain margin) of the current control loop, making it difficult to achieve a good power factor and low input current total harmonic distortion (THD) under all operating conditions, especially for light loads and high input voltages.

SUMMARY

[0006] In described examples, a power supply includes a power factor correction module that is real-time adaptive based on the operating conditions.

BRIEF DESCRIPTION OF THE DRAWINGS

[0007] FIG. 1A is a block diagram schematic of an example embodiment of part of a conventional power supply with power factor correction.

[0008] FIG. 1B is a block diagram schematic illustrating additional detail for a power factor correction module of FIG. 1A.

[0009] FIG. 2A is a block diagram schematic illustrating an example embodiment of part of a power supply with improved power factor correction.

[0010] FIG. 2B is a block diagram schematic illustrating additional detail for a power correction module of FIG. 2A.

DETAILED DESCRIPTION OF EXAMPLE EMBODIMENTS

[0011] As discussed above, a high power factor and low THD are difficult to achieve under all operating conditions, especially for light loads and high input voltages.

[0012] In the improved design discussed below, instead of using a fixed current loop controller for all operating conditions, a power factor controller uses an adaptive current loop controller that changes depending on the operating conditions. In a firmware implementation, a system controller switches among sets of control coefficients for the current loop controller, maintaining a high current loop gain for a wide range of operating conditions.

[0013] FIG. 2A illustrates an example of part of a power supply 200 (simplified to facilitate illustration and discussion) with improved power factor correction. An AC input voltage V_i is rectified by a full-wave rectifier 202. An inductor 204 provides energy storage to enable a continuous input current. A PFC module 206 controls an electronic switch 208 using PWM to control the DC output voltage V_B and to generate a continuous input current matching the shape of the rectified input voltage V_{RECT} and in phase with V_{RECT} . The PFC module 206 of FIG. 2A uses the rectified input voltage V_{RECT} instead of the AC input voltage V_i as in FIG. 1A.

[0014] FIG. 2B illustrates example additional detail for the PFC module 206 of FIG. 2A. The output bus voltage V_B is subtracted from a reference voltage V_{REF} at a summing node 210. The resulting voltage error signal is input to a voltage loop controller 212, which regulates the bus voltage V_B to be equal to V_{REF} . The output U_V of the voltage loop controller 212 is then multiplied by three parameters (K , $1/V_{RECT(rms)}^2$, and V_{RECT}) to form a reference current i_{REF} . A RMS calculator 214 computes the RMS value of the rectified input voltage V_{RECT} . A calculator 216 computes the inverse of the square of the RMS value of the rectified input voltage V_{RECT} . The output U_V of the voltage loop controller 212 is multiplied by $1/V_{RECT(rms)}^2$ by a multiplier 218. That result is multiplied by the rectifier output voltage V_{RECT} by a multiplier 220 with a system dependent gain of K . That result is used as a reference current signal i_{REF} for a current control loop. The variable gain K is used to adjust the range of the reference current signal i_{REF} to the full range of the input voltage V_i . Sensed current i_{SEN} is oversampled and averaged by a sampling and averaging module 222 and the averaged result is subtracted from the reference current signal i_{REF} at a summing node 224. An automatic gain control (AGC) module 226

controls the selection of one of multiple current loop controllers 228, each of which has gain and control coefficients appropriate for a particular input voltage range and load range. The current error signal from the output of summing node 224 is input to a selected current loop controller 228, and the result is used to control the PWM duty-cycle of the electronic switch 208 so that the output voltage V_B is equal to V_{REF} and the current i_{SEN} tracks the shape and phase of the reference current signal i_{REF} . Notably, i_{SEN} is both the input current and the output current, so that controlling i_{SEN} also controls the power factor.

[0015] In the example of FIG. 2B, the selector of a current controller 228 is depicted as a switch 230 and the coupling of the output of the selected current controller 228 is depicted as a switch 232, but these can also be implemented as a multiplexer and a demultiplexer, or by firmware in a system controller. In one embodiment, essentially everything in the PFC module 206 is implemented by firmware in a system controller.

[0016] The AGC module 226 receives at least one calculated operating parameter. In the example of FIG. 2B, the AGC module 226 receives the output U_V of the voltage controller 212, and the calculated RMS value of the rectified input voltage $V_{RECT(rms)}$. Each of these operating parameters is compared to a range of values. For example, the range of U_V may be 0-1, and the range of $V_{RECT(rms)}$ may be 90V to 260V. At lower values of U_V , current controllers 228 with higher gains are selected, and at higher values of U_V , current controllers 228 with lower gains are selected. At lower values of $V_{RECT(rms)}$, current controllers 228 with lower gains are selected, and at higher values of $V_{RECT(rms)}$, current controllers 228 with higher gains are selected. For example, these selections may be done using IF/THEN statements. For example: IF ($V_{RECT(rms)}$ is between 220V-260V AND U_V is between 0.8 and 1.0) THEN select the current controller 228 having the lowest gain.

[0017] Under no-load or relatively light load conditions, relatively little current flows and relatively little energy is stored in the inductor 104. Under these conditions, the inductor may fail to provide current for the entire cycle so that current becomes discontinuous. In the PFC module 206 of figure 2B, the sampling and averaging module 222 samples the current i_{SEN} multiple times during each switching cycle and averages the current samples to improve accuracy under discontinuous inductor current mode.

[0018] The voltage loop controller 212 and the current loop controllers 228 may be any conventional loop control algorithms such as proportional-integrative-derivative (PID) or various

compensation filters. In one embodiment, each of the current loop controllers 228 is a two-pole two-zero compensation filter, implemented as firmware in a system controller, having the following general z-transform form:

$$G(z) = \frac{C_1 - C_2 z^{-1} + C_3 z^{-2}}{1 - C_4 z^{-1} + C_5 z^{-2}}$$

where the coefficients $C_1 - C_5$ vary for each current loop controller 228 and they are selected to provide an appropriate gain and filter characteristic for selected combinations of U_V and $V_{RECT(rms)}$.

[0019] Accordingly, in example embodiments, a method for power factor correction may include adapting, by a system controller, characteristics of a current loop controller, in a power factor correction module, to control power factor.

[0020] Modifications are possible in the described embodiments, and other embodiments are possible, within the scope of the claims.

CLAIMS

What is claimed is:

1. A power supply, comprising:
a power factor correction module having a current loop controller that is real-time adaptive based on the operating conditions.
2. The power supply of claim 1, wherein the power factor correction module selects among a plurality of current loop controllers.
3. The power supply of claim 2, wherein selection of a current loop controller depends on at least one measured operating parameter of the power supply.
4. The power supply of claim 3, wherein the measured operating parameter includes at least one of: a voltage controller output signal and a root-mean-square input voltage signal.
5. The power supply of claim 4, further comprising an automatic-gain-control module, capable of receiving the voltage controller output signal and the root-mean-square input voltage signal, and capable of selecting a current loop controller in response to the voltage controller output signal and the root-mean-square input voltage signal.
6. The power supply of claim 2, wherein each current loop controller is implemented as firmware in a system controller.
7. The power supply of claim 6, wherein the firmware in the system controller selects among sets of current loop controller coefficients.
8. The power supply of claim 7, wherein each set of controller coefficients is a set of coefficients of a two-pole two-zero compensation filter.
9. The power supply of claim 1, further comprising a sampling and averaging module to sample power factor correction module output current multiple times and average the samples for current feedback.
10. A method for power factor correction, comprising:
adapting, by a system controller, characteristics of a current loop controller, in a power factor correction module, to control power factor.
11. A method of claim 10, further comprising:
measuring, by the system controller, at least one operating parameter of a power supply.

12. A method of claim 11, wherein the adapting includes:
adapting, by the system controller, the current loop controller, based on the measured operating parameter.
13. The method of claim 12, wherein the adapting includes:
selecting, by the system controller, one current loop controller from a plurality of current loop controllers, based on the measured operating parameter.
14. The method of claim 10, further comprising:
sampling, current being controlled by the current loop controller, multiple times; and
averaging the sampled currents for use as a feedback signal.

1/2

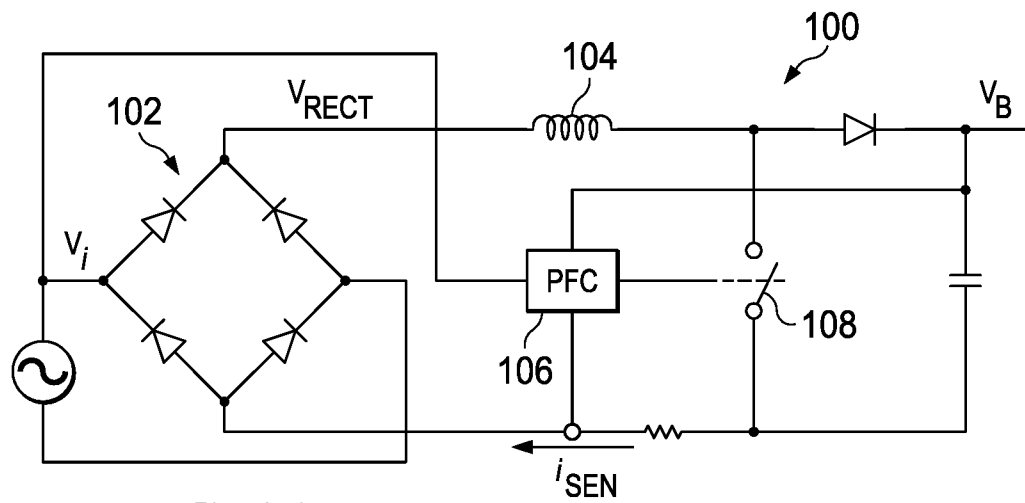


FIG. 1A

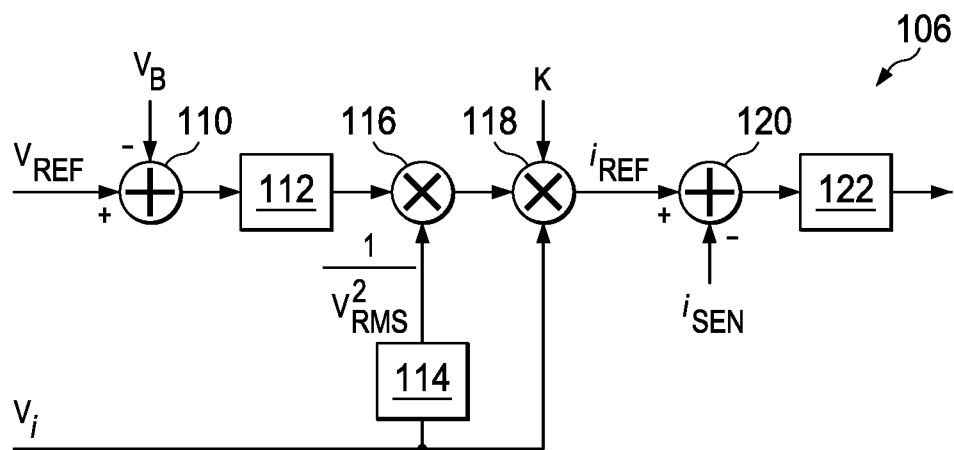


FIG. 1B

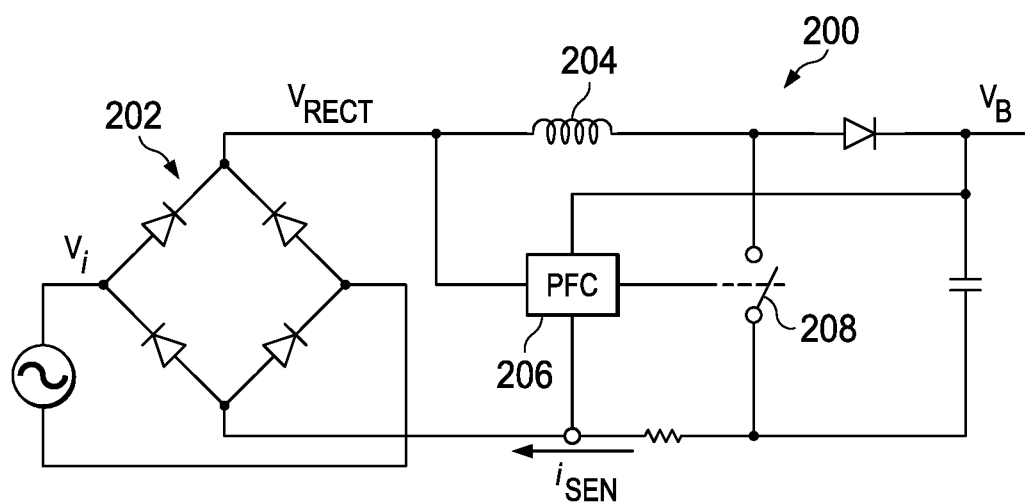


FIG. 2A

2/2

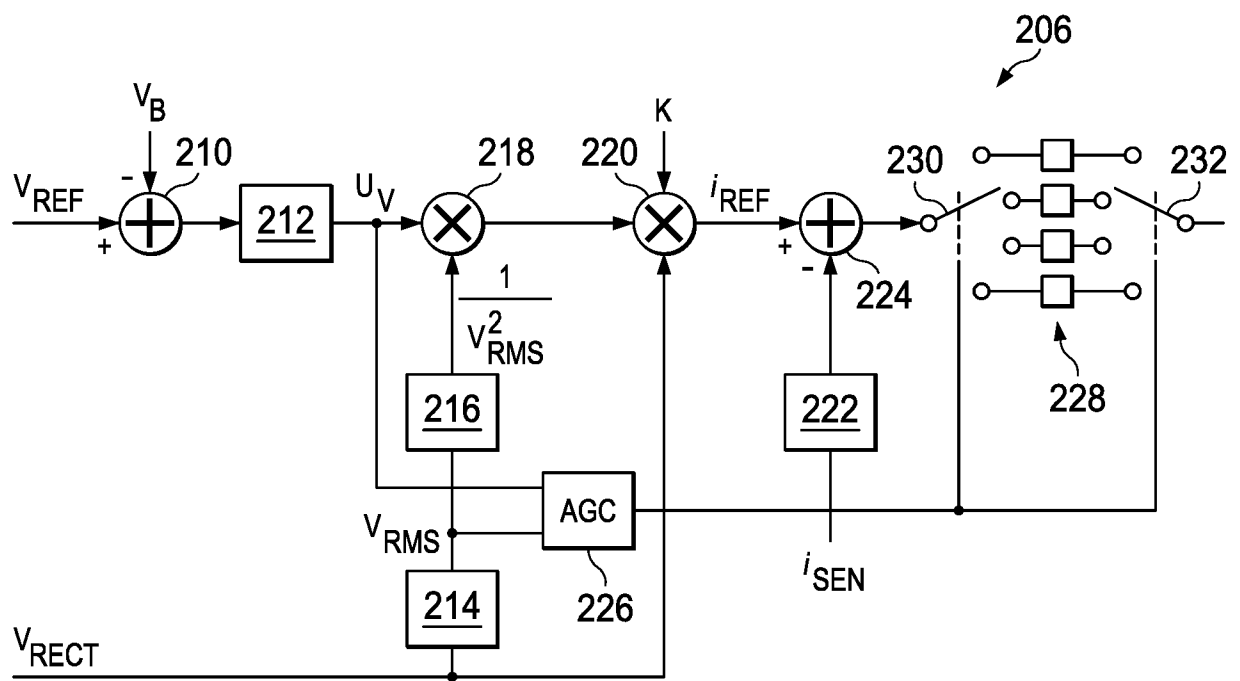


FIG. 2B

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US 2016/033138

A. CLASSIFICATION OF SUBJECT MATTER G05F 1/70 (2006.01) H02M 1/42 (2007.01) According to International Patent Classification (IPC) or to both national classification and IPC																
B. FIELDS SEARCHED Minimum documentation searched (classification system followed by classification symbols) G05F 1/70, H02M 1/00, 1/42, 7/00 Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched Electronic data base consulted during the international search (name of data base and, where practicable, search terms used) PatSearch (RUPTO internal), USPTO, PAJ, Esp@cenet, DWPI, EAPATIS, PATENTSCOPE, Information Retrieval System of FIPS																
C. DOCUMENTS CONSIDERED TO BE RELEVANT <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 10%;">Category*</th> <th style="width: 70%;">Citation of document, with indication, where appropriate, of the relevant passages</th> <th style="width: 20%;">Relevant to claim No.</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">X</td> <td rowspan="2">US 2015/0117074 A1 (ANALOG DEVICES, INC.) 30.04.2015, fig.1, 2</td> <td style="text-align: center;">10-12, 14</td> </tr> <tr> <td style="text-align: center;">Y</td> <td style="text-align: center;">1-9, 13</td> </tr> <tr> <td style="text-align: center;">Y</td> <td>US 2007/0067069 A1 (ARTESYN TECHNOLOGY, INC.) 22.03.2007, fig.1, 2</td> <td style="text-align: center;">1-9</td> </tr> <tr> <td style="text-align: center;">Y</td> <td>CN 103840652 A (SHANGHAI RUJING ELECTRONIC SCI & TECNOLOGY) 04.06.2014, claims, abstract</td> <td style="text-align: center;">1-8, 13</td> </tr> </tbody> </table>			Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.	X	US 2015/0117074 A1 (ANALOG DEVICES, INC.) 30.04.2015, fig.1, 2	10-12, 14	Y	1-9, 13	Y	US 2007/0067069 A1 (ARTESYN TECHNOLOGY, INC.) 22.03.2007, fig.1, 2	1-9	Y	CN 103840652 A (SHANGHAI RUJING ELECTRONIC SCI & TECNOLOGY) 04.06.2014, claims, abstract	1-8, 13
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.														
X	US 2015/0117074 A1 (ANALOG DEVICES, INC.) 30.04.2015, fig.1, 2	10-12, 14														
Y		1-9, 13														
Y	US 2007/0067069 A1 (ARTESYN TECHNOLOGY, INC.) 22.03.2007, fig.1, 2	1-9														
Y	CN 103840652 A (SHANGHAI RUJING ELECTRONIC SCI & TECNOLOGY) 04.06.2014, claims, abstract	1-8, 13														
☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.																
<table border="0" style="width: 100%;"> <tr> <td style="vertical-align: top; width: 50%;"> * Special categories of cited documents: "A" document defining the general state of the art which is not considered to be of particular relevance "E" earlier document but published on or after the international filing date "L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified) "O" document referring to an oral disclosure, use, exhibition or other means "P" document published prior to the international filing date but later than the priority date claimed </td> <td style="vertical-align: top; width: 50%;"> "T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention "X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone "Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art "&" document member of the same patent family </td> </tr> </table>			* Special categories of cited documents: "A" document defining the general state of the art which is not considered to be of particular relevance "E" earlier document but published on or after the international filing date "L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified) "O" document referring to an oral disclosure, use, exhibition or other means "P" document published prior to the international filing date but later than the priority date claimed	"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention "X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone "Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art "&" document member of the same patent family												
* Special categories of cited documents: "A" document defining the general state of the art which is not considered to be of particular relevance "E" earlier document but published on or after the international filing date "L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified) "O" document referring to an oral disclosure, use, exhibition or other means "P" document published prior to the international filing date but later than the priority date claimed	"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention "X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone "Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art "&" document member of the same patent family															
Date of the actual completion of the international search 29 August 2016 (29.08.2016)		Date of mailing of the international search report 08 September 2016 (08.09.2016)														
Name and mailing address of the ISA/RU: Federal Institute of Industrial Property, Berezhevskaya nab., 30-1, Moscow, G-59, GSP-3, Russia, 125993 Facsimile No: (8-495) 531-63-18, (8-499) 243-33-37		Authorized officer S. Pudov Telephone No. (499) 240-25-91														