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(54) **Detector Array with a Through-via Interposer.**

(57) A method for forming a sensor stack is presented. The method includes providing a substrate having a first side and a second side. The method includes disposing an integrated circuit having a first side and a second side on the first side of the substrate, where the integrated circuit comprises a first plurality of contact pads disposed on the first side of the integrated circuit. The method includes providing a sensor array having a plurality of sensor elements, each of the sensor elements having a first side and a second side; the sensor array comprising a second plurality of contact pads disposed on the second side of the sensor array. The method includes disposing an interposer having one or more interposer elements and one or more through vias disposed therethrough between the one or more sensor elements of the sensor array and the integrated circuit to raise the sensor array away from the first side of the integrated circuit such that a plane of the one or more sensor elements is locally normal to a sensor stack normal, wherein the interposer is configured to operationally couple the second side of the sensor elements in the sensor array to the first side of the integrated circuit. The method also includes operationally coupling the first plurality of contact pads on the first side of the integrated circuit to a second plurality of contact pads on the second side of the sensor array to form a tileable sensor stack.

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Detector Array with a Through-via Interposer

BACKGROUND

[0001] Embodiments of the present disclosure relate to sensor arrays, and more particularly to construction of modular sensor arrays.

[0002] Sensors or transducers are devices that transform input signals of one form into output signals of a different form. Commonly used transducers include light sensors, heat sensors, and acoustic sensors. A wide variety of various applications, such as biomedical non-invasive diagnostics and non-destructive testing (NDT) of materials entail the use of sensor arrays, where the sensors are often configured in two-dimensions (that is, the X-Y plane). Moreover, applications such as medical and industrial imaging, non-destructive testing (NDT) and inspection, security, baggage scanning, astrophysics and medicine may entail the use of sensors that encompass large areas. In the field of medical diagnostics, such as, but not limited to, X-ray, computed tomography (CT), ultrasound and mammography, it may be desirable to employ sensors that encompass large areas. For instance, in an X-ray imaging system, large area transducers may be useful to encompass the area of the X-ray detector. Moreover, in non-medical applications even larger arrays may be desired.

[0003] As noted hereinabove, large area detector arrays have desirable characteristics for certain applications. Sensor modules may be arranged to form the large area detector array. Furthermore, it is desirable that the edges of the sensor modules in the array are aligned with the edges of neighboring modules without any significant gaps or offsets. However, it is becoming increasingly difficult to achieve this tileable structure. Particularly, since the sensor detection element must be electrically connected to readout application specific integrated circuits (ASICs), the high density of interconnect requires a close correspondence between the ASIC contact pads and the sensor contact pads. Typically, the ASIC has contacts disposed on only one side. Furthermore, the ASIC in addition to using these contact pads to couple the ASIC to the sensor, also needs to use these contact pads to make power and digital communication connections to other system electronics. Therefore, it is desirable to implement some means of connecting both the sensor and system

interconnects to this ASIC surface, while also supporting the four-sided tiling structure and a high pixel pitch in the sensor.

[0004] A currently available technique typically uses a staircase array of modules where a top surface of the ASIC is directly bonded to a bottom surface of the sensor element. This requires a match between the bump bond array on the ASIC and the bump bond array on the sensor. In addition the ASIC chip extends laterally beyond the sensor element and this extension is used to place wire bonds to couple the top surface of the ASIC to a backplane layer. Unfortunately, this extension of the ASIC creates a need to raise subsequent modules vertically to create a clearance space for the wire bonds. Additionally, all the modules in this detector array are not aligned in the same plane. These offsets disadvantageously create a non-ideal imaging geometry as the different modules are at different distances from an X-ray source. In particular, when the X-ray incident direction is not normal, there can be shadowing effects when one module occludes other modules.

[0005] Presently, certain other techniques entail forming the detector array by shingling sensor modules like roofing tiles or fish scales. In this embodiment, the extension of the sensor module and wire bonds is accommodated by the space created by the angle of the sensor modules. However, the module plane normal is not locally aligned to the detector plane normal since the edges of the sensor modules do not line up. This technique presents a non-ideal imaging geometry.

[0006] It would therefore be desirable to have a sensor module that allows assembly of large area detector arrays. Specifically, there exists a need for a detector array created by arranging a plurality of sensor modules as detailed herein. Furthermore, it is desirable to tile the sensor modules efficiently to form a high-density large area detector array in order to minimize system size, complexity, interconnect lengths and enhance the performance of the detector arrays.

BRIEF DESCRIPTION

[0007] In accordance with aspects of the present technique, a method for forming a sensor stack is presented. The method includes providing a substrate having a first side and a second side. Furthermore, the method includes disposing an integrated circuit having a first side and a second side on the first side of the substrate, where the

integrated circuit comprises a first plurality of contact pads disposed on the first side of the integrated circuit. The method also includes providing a sensor array having a plurality of sensor elements, wherein each of the sensor elements has a first side and a second side, and wherein the sensor array includes a second plurality of contact pads disposed on a second side of the sensor array. Furthermore, the method includes disposing an interposer having one or more interposer elements and one or more through vias disposed therethrough between the one or more sensor elements of the sensor array and the integrated circuit to raise the sensor array away from the first side of the integrated circuit such that a plane of the one or more sensor elements is locally normal to a sensor stack normal, wherein the interposer is configured to operationally couple the second side of the sensor elements in the sensor array to the first side of the integrated circuit. In addition, the method includes operationally coupling the first plurality of contact pads on the first side of the integrated circuit to the second plurality of contact pads on the second side of the sensor array to form a tileable sensor stack.

[0008] In accordance with other aspects of the present technique, a method for forming a tileable detector array is presented. The method includes forming a tileable sensor stack, where forming the tileable sensor stack includes providing a sensor element having a first side and a second side, wherein the sensor element comprises a first plurality of contact pads disposed on the second side of the sensor element, disposing the sensor element on a portion of an area of an integrated circuit having a first side and a second side, disposing a wedge shaped interposer element between the sensor element and the integrated circuit, wherein the wedge shaped interposer element is configured to raise the sensor element away from the first side of the integrated circuit such that a plane of the sensor element is locally normal to a sensor stack normal, wherein the wedge shaped interposer element comprises through vias disposed therethrough, and wherein the interposer is configured to operationally couple the second side of the sensor element to the first side of the integrated circuit, operationally coupling the first plurality of contact pads on the second side of the sensor element to a second plurality of contact pads on the first side of the integrated circuit to form the tileable sensor stack. Additionally, the method includes tiling a

plurality of tileable sensor stacks on a first side of a substrate to form the tileable detector array.

[0009] In accordance with further aspects of the present technique, a method for forming a tileable detector array is presented. The method includes forming a first plurality of tileable stepped sensor stacks, where forming the first plurality of stepped sensor stacks includes providing a sensor element having a first side and a second side, wherein the sensor element comprises a first plurality of contact pads disposed on the second side of the sensor element, disposing the sensor element on a portion of an area of an integrated circuit having a first side and a second side, disposing an stepped interposer element between the sensor element and the integrated circuit, wherein the stepped interposer element is configured to raise the sensor element away from the first side of the integrated circuit such that a plane of the sensor element is locally normal to a sensor stack normal, wherein the stepped interposer element comprises through vias disposed therethrough, and wherein the stepped interposer element is configured to operationally couple the second side of the sensor element to the first side of the integrated circuit, operationally coupling the first plurality of contact pads on the second side of the sensor element to a second plurality of contact pads on the first side of the integrated circuit to form the first plurality of tileable stepped sensor stacks. Furthermore, the method includes forming a second plurality of sensor stacks, where forming the second plurality of sensor stacks includes providing a sensor element having a first side and a second side, wherein the sensor element comprises a first plurality of contact pads disposed on the second side of the sensor element, disposing the sensor element on a portion of an area of an integrated circuit having a first side and a second side, operationally coupling the first plurality of contact pads on the second side of the sensor element to a second plurality of contact pads on the first side of the integrated circuit to form the second plurality of tileable stepped sensor stacks. In addition, the method includes tiling the first plurality of tileable stepped sensor stacks and the second plurality of tileable stepped sensor stacks on a first side of a substrate to form the tileable detector array.

[0010] In accordance with yet another aspect of the present technique, a detector array is presented. The detector array includes a substrate having a first side and a second side. Furthermore, the detector array includes a plurality of tileable sensor

stacks arranged on the first side of the substrate to form a planar detector array, wherein each of the plurality of tileable sensor stacks includes a sensor element having a first side and a second side, wherein the sensor element comprises a first plurality of contact pads disposed on the second side of the sensor element, an integrated circuit having a first side and a second side, an interposer element having one or more through vias disposed therethrough, wherein the interposer element is disposed between the sensor element and the integrated circuit and configured to raise the sensor array away from the first side of the integrated circuit such that a plane of the sensor element is locally normal to detector array normal, and wherein the interposer element is configured to operationally couple the second side of the sensor element to the first side of the integrated circuit, wherein the first plurality of contact pads on the second side of the sensor element is operationally coupled to a second plurality of contact pads on the first side of the integrated circuit to form the tileable sensor stack.

DRAWINGS

[0011] These and other features, aspects, and advantages of the present invention will become better understood when the following detailed description is read with reference to the accompanying drawings in which like characters represent like parts throughout the drawings, wherein:

[0012] FIG. 1 is a diagrammatic illustration of a method for forming a detector array, in accordance with aspects of the present technique;

[0013] FIG. 2 is a diagrammatic illustration of an embodiment of a planar detector array formed using sensor modules that include a stepped interposer or a wedge shaped interposer, in accordance with aspects of the present technique;

[0014] FIG. 3 is a diagrammatic illustration of an embodiment of an arc detector array formed using sensor modules that include a stepped interposer or a wedge shaped interposer, in accordance with aspects of the present technique;

[0015] FIG. 4 is a diagrammatic illustration of a method of forming a sensor stack having a wedge shaped interposer element, in accordance with aspects of the present technique;

[0016] FIG. 5 is a diagrammatic illustration of a method of forming a flat detector array using a plurality of the sensor stacks of FIG. 4, in accordance with aspects of the present technique;

[0017] FIG. 6 is a diagrammatic representation of one embodiment of wedge shaped interposer having through vias disposed therethrough and configured for use in the detector modules of FIGs. 2 and 3, in accordance with aspects of the present technique;

[0018] FIG. 7 is a diagrammatic illustration of computation of a wedge angle for the wedge shaped interposer of FIG. 6, in accordance with aspects of the present technique;

[0019] FIG. 8 is a diagrammatic illustration of a method of forming a planar detector array employing a plurality of stepped sensor stacks having a stepped interposer element, in accordance with aspects of the present technique;

[0020] FIGs. 9-11 are diagrammatic illustrations of different embodiments of stepped sensor stacks for use in forming the planar detector array of FIG. 8, in accordance with aspects of the present technique;

[0021] FIG. 12 is a block diagram of an exemplary imaging system in the form of a CT imaging system; and

[0022] FIG. 13 is a block diagram of a physical implementation of the CT system of FIG. 12.

DETAILED DESCRIPTION

[0023] As will be described in detail hereinafter, systems and methods for forming detector arrays and various embodiments of large area detector arrays are presented. By employing the methods and detector arrays described hereinafter, a large area planar or arc detector array with a locally smooth surface is formed.

[0024] Although, the exemplary embodiments illustrated hereinafter are described in the context of a detector array configured for use in a computed tomography (CT) imaging system, it will be appreciated that use of the detector array in other imaging systems, such as, but not limited to an X-ray imaging system, an ultrasound imaging system, a magnetic resonance (MR) imaging system, a positron emission tomography (PET) imaging system, a single photon emission computed tomography (SPECT)

imaging system and the like are also contemplated in conjunction with the present technique. Furthermore, use of the detector array in other applications such as equipment diagnostics and inspections, baggage inspections, and security applications is also envisaged.

[0025] Turning now to the drawings, and referring to FIG. 1, a flow chart 10 illustrating exemplary logic of a method of forming a tileable planar detector array for use in a system, such as, but not limited to an X-ray imaging system or a CT imaging system, is depicted. The detector array so formed may be used to sense a plurality of input signals. As used herein, the term "detector array" is used to refer to a determined arrangement of sensor stacks. Furthermore, it may be noted that in one embodiment, the term "planar detector array" is used to refer to a detector array that is formed by arranging a plurality of sensor stacks such that the plane of the sensor stacks is locally normal to the detector normal and the detector array has a locally smooth surface. It may further be noted that the planar detector array may include a flat panel detector array or an arc detector array. Also, as used herein, the term "sensor array" is used to refer to an arrangement of one or more sensors or sensor elements. In addition, the term "sensor stack" is used to refer to a stacked arrangement of at least one sensor element, an integrated circuit, such as an ASIC, and an interposer element disposed therebetween.

[0026] As illustrated in FIG. 1, the method starts at step 12, wherein a substrate is provided. The substrate has a first side and a second side. Also, the substrate may be a rigid substrate or a flexible substrate. In one embodiment, the rigid substrate may be formed using high-density organic materials such as a multi-layered substrate made of expanded Teflon, such as Rogers 2800, FR4 or BT laminate materials. Alternatively, an inorganic material such as ceramic (96% Alumina) or a Si interposer may be employed to form the rigid substrate. Furthermore, the flexible substrate may be formed using polyimide thin films. Moreover, the substrate may be representative of a backplane layer that includes other system electronics, in certain embodiments.

[0027] Subsequently, as depicted by step 14, one or more integrated circuits having a respective first side and a second side are disposed on the first side of the substrate. Particularly, the second sides of the one or more integrated circuits are coupled to the first side of the substrate. In one embodiment, the one or more

integrated circuits may be coupled to the substrate using conventional assembly methods such as wire bonding or flip chip attach. It may be noted that in certain embodiments, the one or more integrated circuits may include an application specific integrated circuit (ASIC). Furthermore, a plurality of contact pads is disposed on the first side of each of the one or more integrated circuits. These contact pads aid in coupling the integrated circuits to one or more sensor elements. Additionally, these contact pads also facilitate power and/or digital communication connections from the integrated circuits to other system electronics, such as the system electronics in the substrate.

[0028] Furthermore, at step 16, a sensor array is provided. As previously noted, the term "sensor array" is used to refer to a patterned arrangement of one or more sensor elements, where the one or more sensor elements are configured to detect input signals, such as radiation signals, acoustic signals, light signals, and the like. Each of the one or more sensor elements has a respective first side and a second side. In certain embodiments, the first side of the one or more sensor elements is configured to receive the input signals. Also, a plurality of contact pads is disposed on the second side of each sensor element. It may be noted that in some embodiments, each sensor element may have only one contact pad disposed on the second side. These contact pads are employed to operationally couple the sensor elements in the sensor array to the integrated circuit.

[0029] As described hereinabove, it is desirable to form a substantially planar detector array in which the sensor elements are assembled on one side of the substrate and the one or more integrated circuits (IC) are assembled on the other side of the substrate to form a tileable module. An array of these modules may then be assembled to the next level of carrier to produce a larger sensor array. In accordance with aspects of the present technique, the shortcomings of the presently available techniques may be circumvented via use of an interposer to form a substantially planar detector array. As will be appreciated, an interposer is an electrical interface routing between one connection to another. Particularly, the purpose of the interposer in one example is to spread a connection to a different pitch or to reroute a connection to a different connection. It may be noted that in certain embodiments the interposer may be a rigid interposer, while in certain other embodiments, the interposer may be a

flexible interposer. By way of example, the rigid interposer may include a FR4 material, while the flexible interposer may include a polyimide. Additionally, the interposer may include a ceramic material or an organic material.

[0030] Particularly, in accordance with aspects of the present technique, an interposer is used to facilitate creation of a substantially planar detector array. More specifically, an interposer having one or more interposer elements is disposed between the one or more sensor elements in the sensor array and the one or more integrated circuits, as depicted by step 18. The interposer elements are configured to operationally couple the sensor elements to respective integrated circuits. Furthermore, a plurality of top contact pads are disposed on the first side of the interposer, where these contact pads are configured to operationally couple the interposer to the contact pads disposed on the second side to the sensor elements in the sensor array. Moreover, a plurality of bottom contact pads are disposed on the second side of the interposer, where the bottom contact pads are configured to couple the interposer to the contact pads disposed on the first side of the integrated circuits.

[0031] Additionally, in accordance with further aspects of the present technique, the interposer so disposed between the sensor elements and the integrated circuits aids is raising the sensor array away from the first side of the integrated circuits, thereby creating a clearance space between the sensor array and the integrated circuit. Wire bonds and/or other flexible interconnect that are used to operationally couple the integrated circuits to other electronics may be disposed in the clearance space between the sensor array and the integrated circuits created by the use of the interposer.

[0032] Furthermore, in accordance with further aspects of the present technique, the interposer elements include one or more through vias disposed therethrough. Also, in one embodiment, the through vias may include through silicon vias (TSVs). As will be appreciated, a through silicon via is a vertical connection that passes completely through a silicon wafer or die and is configured to aid in coupling devices in a package while reducing the footprint of the package. In the present embodiment, the TSVs in the interposer elements allow for power signals, ground signals, analog signals and/or digital signals to be routed directly from the sensor array through the TSVs to the integrated circuits. Specifically, these vias are used to route any

connections between the sensor elements in the sensor array and the integrated circuits.

[0033] Moreover, in one embodiment, the interposer may be formed using a multilayer ceramic material. The interposer may include one or more lateral routing layers, where the lateral routing layers are configured to aid in pitch adaptation in which the substrate can interconnect the input/output (I/O) pads of the IC die with the corresponding elements on the sensor. Also, the interposer may include one or more lateral routing traces, where the lateral routing traces are configured to aid in coupling the top contact pads to the bottom contact pads on the interposer. These lateral routing traces may include metalized traces, in certain embodiments.

[0034] Moreover, in accordance with exemplary aspects of the present technique, the interposer includes interposer elements having a varying thickness. By way of example, the thickness of the interposer elements may be varied based on a thickness required to form a substantially planar detector array. Particularly, the thickness of the interposer element corresponding to a sensor element may be varied to ensure that the sensor element is disposed in the same plane as the other sensor elements in the detector array. It may be noted that based on a level of a sensor element in the planar detector array, some sensor elements in the sensor array may not entail use of an interposer element to elevate the sensor element.

[0035] In accordance with further aspects of the present technique, the interposer may include interposer elements having a square shape or a rectangular shape. In certain other embodiments, the interposer elements may have a wedge shape. It may be noted that although the interposer elements are described as having square, rectangular or wedge shapes, other shapes of the interposer elements are also envisaged. These embodiments will be described in greater detail with reference to FIGs. 4-11.

[0036] The sensor elements in the sensor array are then operationally coupled to the one or more integrated circuits employing the one or more interposer elements, as indicated by step 20. Particularly, the contact pads on the second side of the sensor elements are coupled to the top contact pads on the first side of the interposer. In some embodiments, the contact pads on the second side of the sensor elements are coupled to the top contact pads on the first side of the interposer using either flip chip

attach (FCA) or wire bonding of the ASIC die. In the case of FCA, a full area array of I/O pads may be used for coupling the sensor elements to the interposer. However, in the case of wire bonding, a perimeter array of I/O pads may be used to couple the sensor elements to the interposer. Additionally, at step 20, the integrated circuits are coupled to the interposer elements by attaching the bottom contact pads on the second side of the interposer to the contact pads on the first side of the integrated circuits. In certain embodiments, the contact pads on the second side of the sensor elements are coupled to the top contact pads on the first side of the interposer using an area array assembly process. In the case of a Si device, a FCA process is typically used. However, variations of this process entail use of a gold-stud bump on the die surface along with silver-fill conductive epoxy, which can be carried out at substantially lower temperatures than conventional solder FCA methods. Also, if a sensor element is not associated with an interposer element, that sensor element may be directly coupled to the corresponding integrated circuit.

[0037] Consequent to the processing of steps 12-20, a plurality of sensor stacks 22 is formed. Accordingly, in certain embodiments, the method of forming the detector array includes forming a plurality of sensor stacks 22. Specifically, an interposer element of a desired thickness is disposed between a sensor element and an integrated circuit to form a sensor stack 22. This stacking of the sensor element, the interposer element and the integrated circuit allows creation of the sensor stack 22 with four-sided tileability. Particularly, the sensor stack 22 allows the first side of the integrated circuit to be coupled to the second side of the sensor element. Additionally, the sensor stack 22 also allows the same first side of the integrated circuit to be coupled to other system electronics.

[0038] The sensor stacks 22 with four-sided tileability so formed may then be arranged in determined pattern on a first side of a substrate, as indicated in step 24. Specifically, the sensor stacks 22 may be tiled on the first side of the substrate to form a substantially planar detector array. Once the sensor stacks 22 are arranged in a determined pattern to form a substantially planar detector array, the integrated circuits are coupled to the other system electronics. In one embodiment, wire bonds may be used to operationally couple the integrated circuits to the other system electronics.

[0039] Subsequent to steps 12-24, a substantially planar detector array 26 is formed. The four-sided tileability of the sensor stacks 22 allows the sensor stacks 22 to be tiled on the substrate to form the substantially planar detector array 26 that is constructed with sensor stacks 22 that are all disposed in the same plane. In addition, these sensor stacks 22 allow creation of detector arrays of different geometries while maintaining a small pitch sensor.

[0040] FIG. 2 depicts a diagrammatic illustration of one embodiment 30 of a substantially planar detector array formed employing the method of FIG. 1. Particularly, FIG. 2 depicts a flat panel detector array 30 that is configured for use with a parallel ray source 34. The flat panel detector array 30 is constructed by tiling an array of sensor stacks 32, such as the sensor stacks 22 (see FIG. 1). More specifically, the sensor stacks 32 are tiled such that the sensor elements in the sensor array are all in the same plane. The substantially planar detector array 30 depicted in FIG. 2 may be configured for use in an X-ray imaging system, for example.

[0041] Referring now to FIG. 3, an embodiment 40 of an arc detector array is depicted. In particular, the arc detector array 40 is representative of a locally flat array of sensor stacks 42 configured for use such as a CT arc detector. Reference numeral 44 is generally representative of a CT arc source. Here again, the detector array 40 is formed by arraying a plurality of sensor stacks 42, such as the sensor stacks 22 of FIG. 1. It may be noted that although the sensor stacks 42 are not disposed in the same plane globally, the edges of the sensor stacks 42 are lined up without offsets or with minimal offsets to form a smooth curve of the arc detector array 40.

[0042] As noted hereinabove, the substantially planar detector array is formed by tiling a plurality of sensor stacks. Furthermore, the sensor stacks may include an interposer element. In one example, the interposer element is configured to aid is raising the sensor element away from the integrated circuit, thereby creating a clearance space. The interposer element also facilitates coupling the sensor element to the integrated circuit.

[0043] Turning now to FIG. 4, one embodiment 50 of an exemplary sensor stack for use in forming a substantially planar detector array is illustrated. In a presently contemplated configuration, the sensor stack 50 includes a sensor element 52 disposed

on an integrated circuit 54. Specifically, the sensor element 52 is disposed on the integrated circuit 54 such that an area of the sensor element 52 covers only a portion of an area of the integrated circuit 54.

[0044] In accordance with aspects of the present technique, an interposer element 56 configured to couple the sensor element 52 to the integrated circuit 54 is disposed between the sensor element 52 and the integrated circuit 54. The interposer element 56 in the embodiment of FIG. 4 includes a wedge shaped interposer element. As used herein, the term "wedge shaped interposer element" is used to refer to an interposer element that has an angled profile. In one example, the wedge shaped interposer element has at least one trapezoidal cross-section. Particularly, the interposer element 56 has a first thickness at a first end and a second thickness at a second end, where the first thickness is different from the second thickness. By way of example, the first thickness may be less than the second thickness. Also, in one embodiment, the wedge shaped interposer element 56 is formed using a ceramic material. In certain other embodiments, the wedge shaped interposer element 56 may be formed using semiconductor materials and/or polymetric materials. Particularly, in each case the material used to form the wedge shaped interposer element 56 has a mechanical function to support the sensor element in a detector array with the intended impact to overall geometry of the detector array. Also, the material is selected such that the material allows adaption of electrical interconnects between the sensor contact and the readout electronics.

[0045] As previously noted, the sensor element 52 has one or more contact pads disposed on a second side. Also, a first side of the integrated circuit 54 has one or more contact pads disposed thereon. Furthermore, the interposer element 56 aids in coupling the sensor element 52 to the integrated circuit 54 using contact pads disposed on a first side and a second side of the interposer element 56. Additionally, in accordance with aspects of the present technique, the interposer element 56 includes one or more through vias (not shown in FIG. 4) disposed therethrough. The interposer element 56 also may include one or more lateral routing traces and/or one or more lateral routing layers (not shown in FIG. 4). The interposer element 56 will be described in greater detail with reference to FIGs. 6-7.

[0046] Disposing the wedge shaped interposer element 56 between the sensor element 52 and the integrated circuit 54 aids in raising the sensor element 52 away from the integrated circuit 54, thereby creating a clearance space 58 between the sensor element 52 and the integrated circuit 56. Any interconnect configured to couple the integrated circuit 54 to other system electronics (not shown in FIG. 4) may be disposed in this clearance space 58. In one embodiment, the interconnect may include a wire bond 62 that couples the integrated circuit 54 to other electronics that may be disposed in a substrate 60. It may also be noted that use of the wedge shaped interposer element 56 in the sensor stack 50 advantageously allows the first side of the integrated circuit 54 to be operationally coupled to the second side of the sensor element 52 while also permitting coupling of the same first side of the integrated circuit 54 to other system electronics.

[0047] Additionally, the sensor stack 50 may also include a spacer element 64. Specifically, in the illustrated embodiment of FIG. 5, the spacer element 64 is disposed between the second side of the integrated circuit 54 and a first side of the substrate 60 that the sensor stack 50 is disposed on. Also, in one embodiment, the spacer element 64 includes a wedge shaped spacer element. The spacer element 64 is configured to compensate geometrically for the wedge shaped interposer element 56 so that the substrate 72 is also in a single plane. A simplifying feature of the spacer element 64 is that it does not provide any electrical interconnects and provides only a mechanical function. Moreover, the spacer element 64 is formed using polymetric materials, metals or ceramic materials.

[0048] The sensor stack 50 so formed advantageously creates the clearance space 58 where interconnects, such as flexible interconnects and/or wire bonds may be disposed, thereby reducing the footprint of the sensor stack 50. Also, the sensor stack 50 creates a sensor stack with four-sided tileability that allows implementation of various geometries of detector arrays while maintaining a small pitch.

[0049] As previously noted, it is desirable to form substantially planar large area detector arrays, such as the detector arrays 30 (see FIG. 2) and 40 (see FIG. 3), for use in applications such as but not limited to imaging systems and security screening applications. In accordance with aspects of the present technique, a plurality of sensor

stacks, such as the sensor stacks 50 of FIG. 4 are tiled to form a large area substantially planar detector array.

[0050] FIG. 5 depicts one embodiment 70 of a substantially planar large area detector array. Particularly, a plurality of sensor stacks 50 (see FIG. 4) is tiled on a first side of a substrate 72. The substrate 72 may be a flexible substrate or a rigid substrate. Also, the substrate 72 may be formed employing circuit boards materials such as FR4, BT-Epoxy, CEM-1,5, Teflon, polytetrafluoroethylene (PTFE) or polyimide. The plurality of sensor stacks 50 is arranged on the substrate 72 in a determined pattern based on an application. The four-sided tileability of the sensor stacks 50 permits tiling of the plurality of sensor stacks 50 on the substrate 72 to form the substantially planar detector array 70. As previously noted, use of the wedge shaped interposer element 56 raises the sensor element 52 away from the integrated circuit 54 thereby creating the clearance space 58. Wire bonds 74 and other flexible interconnects (not shown in FIG. 5) are disposed in this clearance space 58. The wire bonds 74 and/or other interconnect are employed to couple the integrated circuit 54 to other system electronics that may be disposed in the substrate 72.

[0051] Tiling the plurality of sensor stacks 50 having the wedge shaped interposer elements 56 on the substrate 72 aids in creating a substantially planar detector array 70. Furthermore, use of the interposer element 56 having through vias disposed therethrough in the sensor stack 50 facilitates coupling the first side of the integrated circuit 54 to the second side of the sensor element 52. It may be noted that a high pitch may be maintained using the wedge shaped interposer element 56. Additionally, use of the interposer element 56 circumvents the need for an exact match between the array of contact pads on the first side of the integrated circuit 54 and the array of contact pads of the second side of the sensor element 52. In addition, the interposer element 56 covers only a portion of the integrated circuit area and also raises the sensor element 52 away from the first side of the integrated circuit 54. These partial-coverage and spacing-away features create a clearance space 58 in the tiled detector array structure where wire bonds 74 or some other flexible interconnect can attach the surface of the integrated circuit 54 to the system electronics. In this way the interconnect needs are met while still providing four-sided tileablity with a fine pitch sensor.

[0052] Referring now to FIG. 6, a cross-sectional view 80 of a wedge shaped interposer element, such as the wedge shaped interposer element 56 of FIG. 4 configured for use in the detector arrays of FIGs. 2 and 3 is depicted. As previously noted, the wedge shaped interposer element 80 is formed using a multilayer ceramic material, a semiconductor material or other polymetric materials. Also, as described hereinabove, the interposer element 80 is configured to operationally couple a sensor element, such as the sensor element 52 (see FIG. 4) to an integrated circuit, such as the integrated circuit 54 (see FIG. 4). To that end, the interposer element 80 includes a first plurality contact pads 82 disposed on a first side 84 of the interposer element 80. The first plurality of contact pads 82 is configured to couple the first side 84 of the interposer element 80 to the contact pads disposed on the second side of the sensor element. Additionally, a second plurality contact pads 86 is disposed on a second side 88 of the interposer element 80, where the second plurality of contact pads 86 is configured to operationally couple the second side 88 of the interposer element 80 to the contact pads disposed on the first side of the integrated circuit. It may be noted that the first and second pluralities of contact pads 82 and 86 may be attached to the first side 84 and the second side 88 of the interposer element 80 respectively using a solder, compressive displacement or conductive adhesive attach process.

[0053] Furthermore, the arrangement of the contact pads 82 and 86 on the first and second sides 84, 88 of the interposer element 80 is configured to adapt the layout of contact pads on the first side of the integrated circuit to the layout of the contact pads on the second side of the sensor element using one or more through vias 90 and/or one or more lateral routing layers 92 in the interposer element 80. In one embodiment, the through vias 90 may include through silicon vias (TSVs), as previously noted. In the present embodiment, the TSVs 90 in the interposer element 80 allow for power signals, ground signals, analog signals and/or digital signals to be routed directly from the sensor element through the TSVs 90 directly under the die. Additionally, the lateral routing layers 92 are configured to provide greater flexibility in routing design such that the contacts 82 and 86 are laterally positioned to match the desired configuration of the contacts on the to contact pads on the ASIC die. Moreover, reference numeral 94 is generally representative of lateral routing traces configured to

aid in coupling the first plurality of contact pads 82 to the second plurality of contact pads 86. These traces may include metalized traces, in one embodiment.

[0054] It may further be noted, that if the interposer element 80 includes only through vias 90 disposed therethrough, then it is desirable that the layout of the contact pads on the second side of the sensor element be substantially similar to the layout of contact pads disposed on the first side of the integrated circuit. However, if the interposer element 80 includes the lateral routing layers 92 in addition to the through vias 90, then the interposer element 80 may be configured to couple a disparate arrangement of contact pads of the sensor element to the contact pads of the integrated circuit.

[0055] As previously noted, the wedge shaped interposer element 80 is configured to raise the sensor element away from the integrated circuit thereby creating a clearance space between the sensor element and the integrated circuit that can be utilized to position any interconnect, such as wire bonds. To that end, in accordance with other aspects of the present technique, a wedge angle of the wedge shaped interposer element 80 is determined. As used herein, the term "wedge angle" is used to refer to an inclination formed by two sides of the wedge shaped interposer element 80. Particularly, the wedge angle is determined based on an angle that is required on the wedge shaped interposer element to create a desired clearance space for the wire bonds corresponding to a desired clearance height and width of the sensor stack.

[0056] FIG. 7 depicts a diagrammatic illustration 100 of the computation of a wedge angle for the interposer element 80 (see FIG. 6). In accordance with aspects of the present technique, the wedge angle a 106 may be computed using the following equation:

$$c = w * \tan(a) \qquad (1)$$

where c is a clearance height 102 and w is the width 104 of the sensor stack.

[0057] By way of example, if a desired clearance height 102 of a sensor stack is 0.5 mm and a desired width 104 of the sensor stack is 8 mm, the desired wedge angle a 106 is computed using equation (1) to have a value of 3.6 degrees.

[0058] In the embodiment of the substantially planar detector array 70 depicted in FIG. 5, each sensor stack 50 is substantially similar to the other sensor stacks in the detector array 70. Particularly, each sensor stack 50 includes a sensor element, a

wedge shaped interposer element and an integrated circuit stacked to form the sensor stack 50. Furthermore, since this embodiment of the detector array 70 entails use of substantially similar stacks 50, the efficiency of the detector array 70 is enhanced. Additionally, the cost of forming this detector array 70 is reduced since the creation of the detector array 70 entails use of substantially similar sensor stacks 50.

[0059] According to further aspects of the present technique, a substantially planar detector array may also be formed using a plurality of stepped sensor stacks. As used herein, the term "stepped sensor stacks" is used to refer to sensor stacks that include interposer elements and/or spacer elements of different thicknesses. Also, in some embodiments, the stepped sensor stack may include a sensor element, an interposer, an integrated circuit and a spacer element, while in certain other embodiments, the stepped sensor stack may include only a sensor element, an interposer element and an integrated circuit.

[0060] Turning now to FIG. 8, another embodiment of a substantially planar detector array 110 is depicted. Particularly, the detector array 110 of FIG. 8 is formed by tiling a first plurality of stepped sensor stacks and a second plurality of stepped sensor stacks on a first side of a substrate 112. As used herein, the term "first plurality of stepped sensor stacks" is used to refer to a sensor stack that includes a sensor element that is indirectly coupled to an integrated circuit using an interposer element disposed therebetween. In this sensor stack, the element has a substantially square or rectangular shape. Further, the term "second plurality of stepped sensor stacks" is used to refer to a sensor stack that includes a sensor element that is directly coupled to an integrated circuit and does not include an interposer element disposed therebetween. In addition, the first and second pluralities of sensor stacks may also optionally include a spacer element , in certain embodiments. However, in certain other embodiment, the spacer element may be omitted.

[0061] With continuing reference to FIG. 8, reference numerals 114 and 116 are examples of the first plurality of stepped sensor stacks that include a sensor element, an integrated circuit and an interposer element disposed therebetween. Also, one example of the second plurality of stepped sensor stacks that includes a sensor element directly coupled to an integrated circuit but does not include an interposer element disposed therebetween is generally referenced by reference numeral 118.

[0062] In accordance with aspects of the present technique, the stepped sensor stacks 114 and 116 include interposer elements of varying thickness. Specifically, the sensor stack 114 includes an interposer element of a smaller thickness, while the sensor stack 116 includes an interposer element of a relatively greater thickness. According to aspects of the present technique, the thickness of the interposer elements is varied to facilitate formation of sensor stacks that aid in creating substantially planar detector arrays. Accordingly, the thickness of the interposer element is varied based on the thicknesses of the other elements in the sensor stack.

[0063] Furthermore, the stepped sensor stack 118 includes a sensor element that is directly coupled to the integrated circuit without the use of an interposer element. Moreover, the sensor stacks 114, 116 and 118 may optionally include a spacer element 120. The thickness of the spacer element 120 may be varied to aid in the creation of a substantially planar detector array. Also, use of the interposer element aids in raising the sensor element away from a surface of the integrated circuit, thereby creating a clearance space 122. Wire bonds 124 and/or other flexible interconnect used to couple the first side of the integrated circuit to other system electronics may be disposed in this clearance space 122.

[0064] FIGs. 9-11 depict various embodiments of the stepped sensor stacks that are employed to create the substantially planar detector array 110 (see FIG. 8). Referring now to FIG. 9, one embodiment of the sensor stack 114 is depicted. The sensor stack 114 includes a sensor element 132 disposed on a portion of an area of an integrated circuit 134. The sensor element 132 is operationally coupled to the integrated circuit 134 using an interposer element 136. In one example, the interposer element 136 is not wedge shaped, but may have a polygonal shape such as a square or a rectangle. Use of the interposer element 136 aids in raising the sensor element 132 away from a surface of the integrated circuit 134. The partial coverage of the area of the integrated circuit 134 by the sensor element 132 and the spacing away of the sensor element 132 from the integrated circuit 134 creates a clearance space 138 in the sensor stack 114. Wire bonds 140, such as wire bonds 124 of FIG. 8, and/or other flexible interconnect used to couple a first side of the integrated circuit 134 to other system electronics may be disposed in this clearance space 138. The sensor stack 114 is also shown as including a spacer element 142.

[0065] FIG. 10 depicts one embodiment of the sensor stack 116 of FIG. 8. The sensor stack 116 includes a sensor element 152 disposed on a portion of an area of an integrated circuit 154. In this embodiment, the sensor element 152 is operationally coupled to the integrated circuit 154 using an interposer element 156 that is relatively thicker than the interposer element 136 of FIG. 9. A clearance space 158 in the sensor stack 116 created by the partial coverage of an area of the integrated circuit 154 by the sensor element 152 and the spacing away of the sensor element 152 from a surface of the integrated circuit 154 is used to dispose wire bonds 160 to couple a first side of the integrated circuit 154 to other system electronics. It may be noted that this sensor stack 116 does not entail use of a spacer element.

[0066] Referring now to FIG. 11, one embodiment of the sensor stack 118 of FIG. 8, is depicted. The sensor stack 118 includes a sensor element 172 disposed on a portion of an area of an integrated circuit 174. In this embodiment, the sensor element 172 is directly coupled to the integrated circuit 174 without the use of an interposer element. A clearance space 178 in the sensor stack 118 created by the partial coverage of an area of the integrated circuit 174 by the sensor element 172 is used to dispose wire bonds 180 to couple the first side of the integrated circuit 174 to other system electronics. It may be noted that this sensor stack 118 entails use of a spacer element 176.

[0067] With returning reference to FIG. 8, the various embodiments of the sensor stacks 114 (see FIG. 9), 116 (see FIG. 10) and 118 (see FIG. 11) are representative of sensor stacks that allow four-sided tileability. Subsequently, these sensor stacks 114, 116, 118 are tiled in a determined pattern on the first side of the substrate 112 to form the substantially planar detector array 110. Tiling the plurality of sensor stacks 114, 116, 118 as described hereinabove ensures that the interconnect needs are met while still providing four-sided tileablity with fine pitch sensor.

[0068] The flat panel detector array 30 of FIG. 2 and the arc detector array 40 of FIG. 3 may find application in a medical imaging system, such as a CT imaging system. FIG. 12 is a block diagram showing an imaging system 190 for acquiring and processing image data in accordance with the present technique. In the illustrated embodiment, the system 190 is a computed tomography system designed to acquire X-ray projection data, to reconstruct the projection data into an image, and to process

the image data for display and analysis in accordance with the present technique. In the embodiment illustrated in FIG. 12, the imaging system 190 includes a source of X-ray radiation 192. In one exemplary embodiment, the source of X-ray radiation 192 may include an X-ray tube. The source of X-ray radiation 192 may include thermionic or solid-state electron emitters directed at an anode to generate X-rays or, indeed, any other emitter capable of generating X-rays having a spectrum and energy useful for imaging a desired object. Examples of suitable electron emitters include tungsten filament, tungsten plate, field emitter, thermal field emitter, dispenser cathode, thermionic cathode, photo-emitter, and ferroelectric cathode.

[0069] The source of radiation 192 may be positioned near a collimator 194, which may be configured to shape a stream of radiation 196 that is emitted by the source of radiation 192. The stream of radiation 196 passes into the imaging volume containing the subject to be imaged, such as a patient 198. The stream of radiation 196 may be generally fan-shaped or cone-shaped, depending on the configuration of the detector array, discussed below, as well as the desired method of data acquisition. A portion 200 of radiation passes through or around the subject and impacts a detector array, represented generally at reference numeral 202. Detector elements of the detector 202 produce electrical signals that represent the intensity of the incident X-ray beam. These signals are acquired and processed to reconstruct an image of the features within the subject.

[0070] The radiation source 192 is controlled by a system controller 204, which furnishes both power, and control signals for CT examination sequences. Moreover, the detector 202 is coupled to the system controller 204, which commands acquisition of the signals generated in the detector 202. The system controller 204 may also execute various signal processing and filtration functions, such as for initial adjustment of dynamic ranges, interleaving of digital image data, and so forth. In general, the system controller 204 commands operation of the imaging system 190 to execute examination protocols and to process acquired data. In the present context, the system controller 204 also includes signal processing circuitry, typically based upon a general purpose or application-specific digital computer, associated memory circuitry for storing programs and routines executed by the computer, as well as configuration parameters and image data, interface circuits, and so forth.

[0071] In the embodiment illustrated in FIG. 12, the system controller 204 is coupled via a motor controller 212 to a rotational subsystem 206 and a linear positioning subsystem 208. In one embodiment, the rotational subsystem 206 enables the X-ray source 192, the collimator 194 and the detector 202 to be rotated one or multiple turns around the patient 198. In other embodiments, the rotational subsystem 206 may rotate only one of the source 192 or the detector 202 or may differentially activate various stationary electron emitters to generate X-ray radiation and/or detector elements arranged in a ring about the imaging volume. In embodiments in which the source 192 and/or detector 202 are rotated, the rotational subsystem 206 may include a gantry (not shown in FIG. 12). Thus, the system controller 204 may be utilized to operate the gantry. The linear positioning subsystem 208 enables the patient 198, or more specifically a patient table (not shown in FIG. 12), to be displaced linearly. Thus, the patient table may be linearly moved within the gantry to generate images of particular areas of the patient 198.

[0072] Additionally, as will be appreciated by one skilled in the art, the source of radiation 192 may be controlled by an X-ray controller 210 disposed within the system controller 204. Particularly, the X-ray controller 210 is configured to provide power and timing signals to the X-ray source 192.

[0073] Further, the system controller 204 is also illustrated as including a data acquisition system 214. In this exemplary embodiment, the detector 202 is coupled to the system controller 204, and more particularly to the data acquisition system 214. The data acquisition system 214 receives data collected by readout electronics of the detector 202. The data acquisition system 214 typically receives sampled analog signals from the detector 202 and converts the data to digital signals for subsequent processing by a computer 216.

[0074] The computer 216 typically is coupled to or incorporates the system controller 204. The data collected by the data acquisition system 214 may be transmitted to the computer 216 for subsequent processing and reconstruction. The computer 216 may include or communicate with a memory 218 that may store data processed by the computer 216 or data to be processed by the computer 216. It may be noted that any type of memory configured to store a large amount of data might be utilized by the system 190. Moreover, the memory 218 may be located at the

acquisition system or may include remote components, such as network accessible memory media, for storing data, processing parameters, and/or routines for implementing the techniques described below.

[0075] Additionally, the computer 216 may also be adapted to control features such as scanning operations and data acquisition that may be enabled by the system controller 204. Furthermore, the computer 216 may be configured to receive commands and scanning parameters from an operator via an operator workstation 220, which is typically equipped with a keyboard and other input devices (not shown). It may be noted that the operator workstation 220 may include a user interface, in certain embodiments. An operator, such as a clinician, may thereby control the system 190 via the input devices. Thus, the clinician may observe the reconstructed image and other data relevant to the system from computer 216, initiate imaging, and so forth.

[0076] A display 222 coupled to the operator workstation 220 may be utilized to observe the reconstructed images. Additionally, the scanned image may also be printed by a printer 224, which may be coupled to the operator workstation 220. The display 222 and the printer 224 may also be connected to the computer 216, either directly or via the operator workstation 220. The operator workstation 220 may also be coupled to a picture archiving and communications system (PACS) 226. It should be noted that PACS 226 might be coupled to a remote system 228, such as radiology department information system (RIS), hospital information system (HIS) or to an internal or external network, so that other clinicians at different locations may gain access to the image data.

[0077] It should be further noted that the computer 216 and operator workstation 220 may be coupled to other output devices, which may include standard or special purpose computer monitors and associated processing circuitry. One or more operator workstations 220 may be further linked in the system for outputting system parameters, requesting examinations, viewing images, and so forth. In general, displays, printers, workstations, and similar devices supplied within the system may be local to the data acquisition components, or may be remote from these components, such as elsewhere within an institution or hospital, or in an entirely different location,

linked to the image acquisition system via one or more configurable networks, such as the Internet, a virtual private network or the like.

[0078] As noted above, an exemplary imaging system utilized in a present embodiment may be a CT scanning system 230, as depicted in greater detail in FIG. 13. The CT scanning system 230 may be a multi-slice CT (MSCT) system that offers a wide array of axial coverage, high rotational speed of the gantry, and high spatial resolution. Alternately, the CT scanning system 230 may be a volumetric CT (VCT) system utilizing a cone-beam geometry and an area detector to allow the imaging of a volume, such as an entire internal organ of a subject, at high or low gantry rotational speeds. The CT scanning system 230 is illustrated with a frame 232 and a gantry 234 that has an aperture 236 through which the patient 198 (see FIG. 12) may be moved. A patient table 238 may be positioned in the aperture 236 of the frame 232 and the gantry 234 to facilitate movement of the patient 198, typically via linear displacement of the table 238 by the linear positioning subsystem 208 (see FIG. 12). The gantry 234 is illustrated with the source of radiation 192, such as an X-ray tube that emits X-ray radiation from a focal point 240. For cardiac imaging, the stream of radiation is directed towards a cross section of the patient 198 including the heart.

[0079] In typical operation, the X-ray source 192 (see FIG. 12) projects an X-ray beam from the focal point 240 and toward the detector 202. The collimator 194 (see FIG. 12), such as lead or tungsten shutters, typically defines the size and shape of the X-ray beam that emerges from the X-ray source 192. The detector 202 is generally formed by a plurality of detector elements, which detect the X-rays that pass through and around a subject of interest, such as the heart or chest. Each detector element produces an electrical signal that represents the intensity of the X-ray beam at the position of the element during the time the beam strikes the detector. The gantry 234 is rotated around the subject of interest so that a plurality of radiographic views may be collected by the computer 216 (see FIG. 12).

[0080] Thus, as the X-ray source 192 and the detector 202 rotate, the detector 202 collects data related to the attenuated X-ray beams. Data collected from the detector 202 then undergoes pre-processing and calibration to condition the data to represent the line integrals of the attenuation coefficients of the scanned objects. The processed data, commonly called projections, may then be filtered and backprojected to

formulate an image of the scanned area. A formulated image may incorporate, in certain modes, projection data for less or more than 360 degrees of rotation of the gantry 234.

[0081] Once reconstructed, the image produced by the system of FIGs. 12-13 reveals internal features 244 of the patient 198. In traditional approaches for the diagnosis of disease states, and more generally of medical conditions or events, a radiologist or physician typically consider the reconstructed image 242 to discern characteristic features of interest. In cardiac imaging, such features 244 include coronary arteries or stenotic lesions of interest, and other features, which would be discernable in the image, based upon the skill and knowledge of the individual practitioner. Other analyses may be based upon capabilities of various algorithms, including algorithms generally referred to as computer-aided detection or computer-aided diagnosis (CAD) algorithms.

[0082] Furthermore, the foregoing examples, demonstrations, and process steps such as those that may be performed by the imaging system 190, 230 may be implemented by suitable code on a processor-based system, such as a general-purpose or special-purpose computer. It should also be noted that different implementations of the present technique may perform some or all of the steps described herein in different orders or substantially concurrently, that is, in parallel. Furthermore, the functions may be implemented in a variety of programming languages, including but not limited to C++ or Java. Such code may be stored or adapted for storage on one or more tangible, machine readable media, such as on data repository chips, local or remote hard disks, optical disks (that is, CDs or DVDs), memory or other media, which may be accessed by a processor-based system to execute the stored code. Note that the tangible media may comprise paper or another suitable medium upon which the instructions are printed. For instance, the instructions may be electronically captured via optical scanning of the paper or other medium, then compiled, interpreted or otherwise processed in a suitable manner if necessary, and then stored in the data repository 248 or memory.

[0083] The methods for forming the substantially planar detector arrays and the various embodiments of the detector arrays described hereinabove dramatically enhance the ability to form two-dimensional high-density large area tileable detector

arrays with a locally smooth surface. Additionally, the four-sided tileable sensor stacks allow the sensor stacks to be arranged such that there are no offsets at the boundaries of these tiled sensor stacks, thereby circumventing occurrence of imaging artifacts. Also, the four-sided tileable sensor stacks provide the ability to tile fine pitch sensor stacks into a large area detector without significant offsets between sensor stack edges.

[0084] Moreover, use of the interposer circumvents the need for an exact match between the ASIC pad array and the sensor pad array, thereby maintaining a high pitch of the interconnect. In addition, the interposer covers only part of the ASIC area and raises the sensor away from the ASIC surface. These partial coverage and spacing away features create a gap in the tiled detector array structure where wire bonds or other flexible interconnect can be disposed to attach the ASIC bond surface to system electronics. Consequently, the interconnect needs are met while still providing four-sided tileablity with fine pitch sensor.

[0085] Also, a flat panel detector may be constructed from an array of sensor stacks with sensor elements all in the same plane. Furthermore, a CT arc detector array may also be constructed by tiling these sensor stacks, where although the modules are not in the same plane globally, the edges of the modules lined up without offsets. The sensor stacks allow creation of different geometries of detector arrays while maintaining a small pitch sensor. Additionally, the sensor stacks provide a means to electrically connect one side of the ASIC to the sensor and also facilitate coupling the same side of the ASIC to the system electronics.

[0086] While only certain features of the invention have been illustrated and described herein, many modifications and changes will occur to those skilled in the art. It is, therefore, to be understood that the appended claims are intended to cover all such modifications and changes as fall within the true spirit of the invention.

Detector Array with a Through-via Interposer

ELEMENT LIST

10	Flow chart depicting method for forming a planar tileable detector array
12-26	Steps for forming a planar tileable detector array
30	Planar tileable detector array
32	Sensor stacks
34	Parallel ray source
40	Arc detector array
42	Sensor stacks
44	CT arc source
50	Sensor stack
52	Sensor element
54	Integrated circuit
56	Interposer element
58	Clearance space
60	Substrate
62	Wire bond
64	Spacer element
70	Planar tileable detector array formed by tiling sensor stacks having wedge shaped interposer elements
72	Substrate
74	Wire bond
80	Wedge shaped interposer element
82	Contact pads
84	First side of wedge shaped interposer element
86	Contact pads
88	Second side of wedge shaped interposer element
90	Through vias
92	Lateral routing layers
94	Lateral routing traces
100	Diagrammatical illustration of method for computing wedge angle

102	Clearance height
104	Width of sensor stack
106	Wedge angle
110	Planar tileable detector array formed by tiling stepped sensor stacks
112	Substrate
114	First plurality of stepped sensor stacks
116	First plurality of stepped sensor stacks
118	Second plurality of stepped sensor stacks
120	Spacer element
122	Clearance space
124	Wire bond
132	Sensor element
134	Integrated circuit
136	Interposer element
138	Clearance space
140	Wire bond
142	Spacer element
152	Sensor element
154	Integrated circuit
156	Interposer element
158	Clearance space
160	Wire bond
172	Sensor element
174	Integrated circuit
176	Spacer element
178	Clearance space
180	Wire bond
190	Imaging system
192	Source
194	Collimator
196	Stream of radiation
198	Patient

200	Portion of radiation
202	Detector
204	System controller
206	Rotational subsystem
208	Linear positioning subsystem
210	X-ray controller
212	Motor controller
214	Data acquisition system
216	Computer
218	Memory
220	Operator workstation
222	Display
224	Printer
226	Picture archiving and communication system
228	Remote system
230	CT scanning system
232	Frame
234	Gantry
236	Aperture
238	Patient table
240	Focal point
242	Image slice
244	Features

C O N C L U S I E S

1. Een werkwijze voor het vormen van een sensorstapel, omvattende:
het verstrekken van een substraat met een eerste zijde en een tweede zijde;
het aanbrengen van een geïntegreerde schakeling met een eerste zijde en een tweede zijde op de eerste zijde van het substraat, waarbij de geïntegreerde schakeling een eerste veelheid aan contactvlakken heeft die zijn aangebracht op de eerste zijde van de geïntegreerde schakeling;
het verstrekken van een sensorrij met een veelheid aan sensorelementen, waarbij elk van de sensorelementen een eerste zijde en een tweede zijde heeft, en waarbij de sensorrij een veelheid aan tweede contactvlakken heeft die zijn aangebracht op een tweede zijde van de sensorrij;
het aanbrengen van een tussenlaag met een of meer tussenlaagelementen en een of meer doorgangen daardoor aangebracht tussen de een of meer sensorelementen van de sensorrij en de geïntegreerde schakeling om de sensorrij te verheffen, weg van de eerste zijde van de geïntegreerde schakeling zodanig dat een vlak van de een of meer sensorelementen lokaal loodrecht is met een sensorstapelnormaal, waarbij de tussenlaag is ingericht om de tweede zijde van de sensorelementen in de sensorrij operationeel te verbinden met de eerste zijde van de geïntegreerde schakeling, en
het operationeel verbinden van de eerste veelheid aan contactvlakken op de eerste zijde van de geïntegreerde schakeling met de tweede veelheid aan contactvlakken op de tweede zijde van de sensorrij om een tegelbare sensorstapel te vormen.

2. De werkwijze van conclusie 1, waarbij de een of meer tussenlaagelementen in de tussenlaag een schuine profiel hebben, en waarbij de een of meer tussenlaagelementen in de tussenlaag een rechthoekige vorm, een wigvormige vorm, een vierkante vorm, een ronde vorm, of combinaties daarvan hebben.

3. De werkwijze van conclusie 1, verder omvattende:
het aanbrengen van een of meer sensorelementen in de sensorrij over een gedeelte van een gebied van de geïntegreerde schakeling, en
het aanbrengen van een afstandhouderelement tussen de tweede zijde van de geïntegreerde schakeling en het substraat.

4. Een werkwijze voor het vormen van een tegelbare detectorrij, omvattende:
het vormen van een tegelbare sensorstapel, omvattende:
het verstrekken van een sensorelement met een eerste zijde en een tweede zijde, waarbij het sensorelement een eerste veelheid aan contactvlakken omvat die zijn aangebracht op de

tweede zijde van het sensorelement;
het aanbrengen van het sensorelement op een gedeelte van een gebied van een geïntegreerde schakeling met een eerste zijde en een tweede zijde;
het aanbrengen van een wigvormig tussenlaagelement tussen het sensorelement en de geïntegreerde schakeling, waarbij het wigvormige tussenlaagelement is ingericht om het sensorelement te verheffen, weg van de eerste zijde van de geïntegreerde schakeling, zodanig dat een vlak van het sensorelement lokaal loodrecht is op een sensorstapelnormaal, waarbij het wigvormige tussenlaagelement een doorgang omvat daardoor aangebracht, en waarbij de tussenlaag is ingericht om de tweede zijde van het sensorelement aan de eerste zijde van de geïntegreerde schakeling operationeel te verbinden;
het operationeel verbinden van de eerste veelheid aan contactvlakken op de tweede zijde van het sensorelement met een tweede veelheid aan contactvlakken op de eerste zijde van de geïntegreerde schakeling om de tegelbare sensorstapel vormen, en
het betegelen van een veelheid van tegelbare sensorstapels op een eerste zijde van een substraat om de tegelbare detectorrij te vormen.

5. De werkwijze volgens conclusie 4, verder omvattende:
het aanbrengen van een afstandhouderelement tussen de tweede zijde van de geïntegreerde schakeling en de eerste zijde van het substraat, waarbij het afstandhouderelement is ingericht om te compenseren voor de wigvormige vorm van het tussenlaagelement, en
het operationeel verbinden van de geïntegreerde schakeling naar andere elektronica met behulp van draadverbindingen of flexibele tussenverbinding, waarbij het operationeel verbinden van de geïntegreerde schakeling aan de andere elektronica het aanbrengen van de draadverbindingen of de flexibele tussenverbindingen in een vrije ruimte ontstaan tussen het sensorelement en de geïntegreerde schakeling omvat.

6. Een werkwijze voor het vormen van een tegelbare detectorrij, omvattende:
het vormen van een eerste veelheid aan getrapte sensorstapels, omvattende:
het verstrekken van een sensorelement met een eerste zijde en een tweede zijde, waarbij het sensorelement een eerste veelheid aan contactvlakken omvat die zijn aangebracht op de tweede zijde van het sensorelement;
het aanbrengen van het sensorelement op een gedeelte van een gebied van een geïntegreerde schakeling met een eerste zijde en een tweede zijde;
het aanbrengen van een getrapt tussenlaagelement tussen het sensorelement en de geïntegreerde schakeling, waarbij het getrapte tussenlaagelement is ingericht om het sensorelement te verheffen, weg van de eerste zijde van de geïntegreerde schakeling, zodanig dat een vlak van het sensorelement lokaal loodrecht is op een sensorstapelnormaal, waarbij het getrapte tussenlaagelement een doorgang omvat daardoor aangebracht, en

waarbij de getrapte tussenlaag is ingericht om de tweede zijde van het sensorelement aan de eerste zijde van de geïntegreerde schakeling operationeel te verbinden;
het operationeel verbinden van de eerste veelheid aan contactvlakken op de tweede zijde van het sensorelement met een tweede veelheid aan contactvlakken op de eerste zijde van de geïntegreerde schakeling om de eerste veelheid aan tegelbare getrapte sensorstapels vormen,
het vormen van een tweede veelheid aan sensorstapels, omvattende:
het aanbrengen van een sensorelement met een eerste zijde en een tweede zijde, waarbij het sensorelement een eerste veelheid aan contactvlakken omvat die zijn aangebracht op de tweede zijde van het sensorelement;
het aanbrengen van het sensorelement op een gedeelte van een gebied van een geïntegreerde schakeling met een eerste zijde en een tweede zijde;
het operationeel verbinden van de eerste veelheid aan contactvlakken op de tweede zijde van het sensorelement met een tweede veelheid aan contactvlakken op de eerste zijde van de geïntegreerde schakeling om de tweede veelheid aan tegelbare getrapte sensorstapels te vormen, en
het betegelen van de eerste veelheid aan tegelbare getrapte sensorstapels en de tweede veelheid aan tegelbare getrapte sensorstapels op een eerste zijde van een substraat om tegelbare detectorrij te vormen.

7. Een detectorrij (30), (40), (70), (110), omvattende:
een substraat (72) met een eerste zijde en een tweede zijde;
een veelheid aan tegelbare sensorstapels (32), (42), (50) gerangschikt op de eerste zijde van het substraat (72) om een vlakke detectorrij vormen, waarbij elk van de veelheid aan tegelbare sensorstapels (32), (42), (50) omvat:
een sensorelement (52) met een eerste zijde en een tweede zijde, waarbij het sensorelement (52) een eerste veelheid aan contactvlakken (82) omvat die zijn aangebracht op de tweede zijde van het sensorelement (52);
een geïntegreerde schakeling (54) met een eerste zijde en een tweede zijde;
een tussenlaagelement (56) met een of meer doorgangen (90) daardoor aangebracht, waarbij het tussenlaagelement (56) is aangebracht tussen het sensorelement (52) en de geïntegreerde schakeling (54) en is ingericht om het sensorelement te verheffen (52), weg van de eerste zijde van de geïntegreerde schakeling (54) zodanig dat een vlak van het sensorelement (52) lokaal loodrecht is met een detectorrijnormaal, en waarbij het tussenlaagelement (56) is ingericht om de tweede zijde van het sensorelement (52) aan de eerste zijde van de geïntegreerde schakeling (54) operationeel te verbinden,
waarbij de eerste veelheid aan contactvlakken (82) op de tweede zijde van het sensorelement (52) operationeel verbonden is met een tweede veelheid aan contactvlakken

(86) op de eerste zijde van de geïntegreerde schakeling (54) om een tegelbare sensorstapel (50) te vormen.

8. De detectorrij (30), (40), (70), (110) volgens conclusie 7, waarbij het tussenlaagelement (56) een getrapt tussenlaagelement of een wigvormig tussenlaagelement omvat.

9. De detectorrij (30), (40), (70), (110) volgens conclusie 7, waarbij het tussenlaagelement (56) verder omvat:
een of meer routinglagen (92), een of meer routingsporen, of zowel de een of meer routinglagen en de een of meer routingsporen, en
bovenzijdecontactvlakken aangebracht op een eerste zijde van het tussenlaagelement en onderzijdecontactvlakken aangebracht op een tweede zijde van het tussenlaagelement.

10. De detectorrij (30), (40), (70), (110) volgens conclusie 7, verder omvattende een asfstandhouderelement aangebracht tussen de tweede zijde van de geïntegreerde schakeling en de eerste zijde van het substraat.

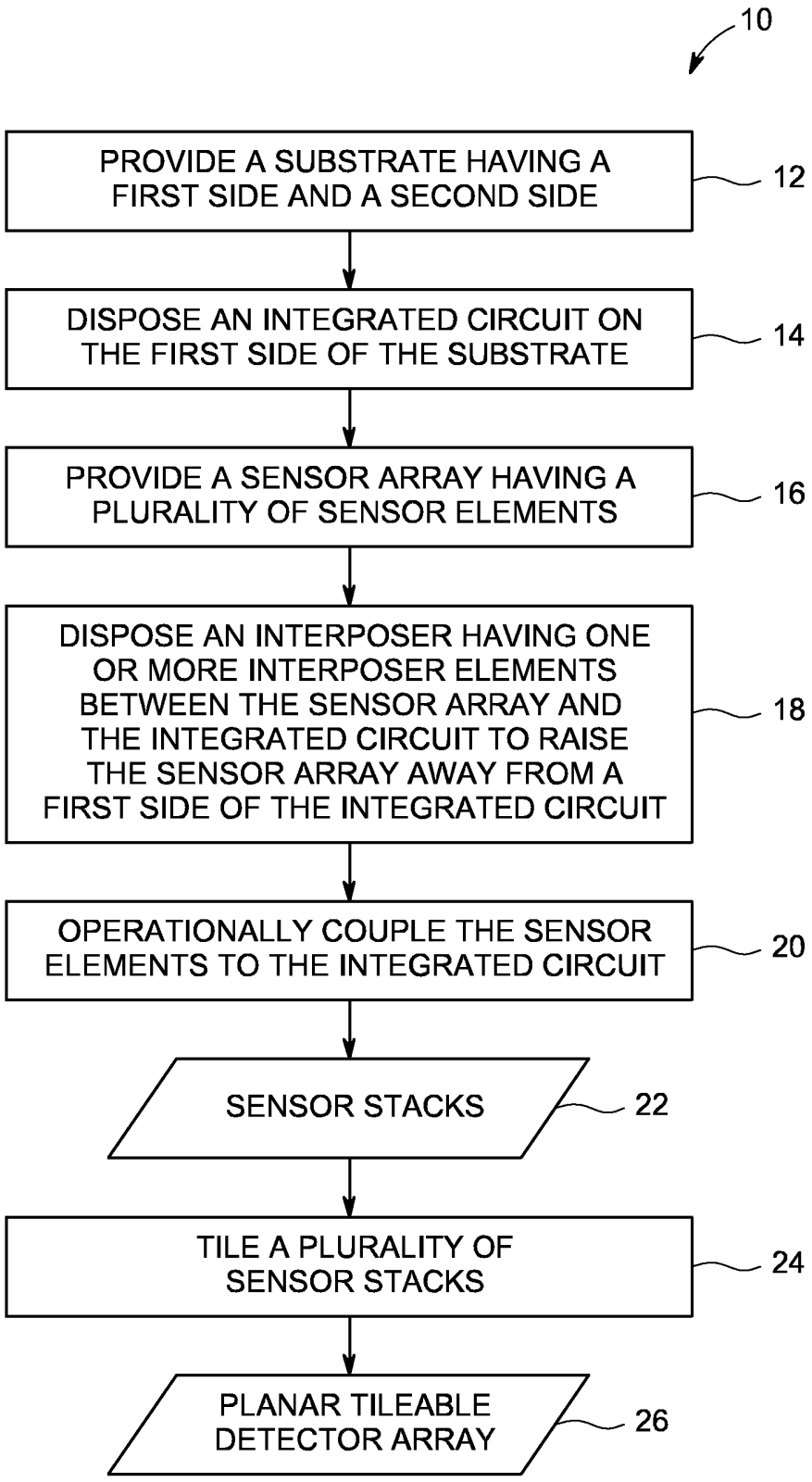
10
PROVIDE A SUBSTRATE HAVING A FIRST SIDE AND A SECOND SIDE
12
DISPOSE AN INTEGRATED CIRCUIT ON THE FIRST SIDE OF THE SUBSTRATE
14
PROVIDE A SENSOR ARRAY HAVING A PLURALITY OF SENSOR ELEMENTS
16
DISPOSE AN INTERPOSER HAVING ONE OR MORE INTERPOSER ELEMENTS BETWEEN THE SENSOR ARRAY AND THE INTEGRATED CIRCUIT TO RAISE THE SENSOR ARRAY AWAY FROM A FIRST SIDE OF THE INTEGRATED CIRCUIT
18
OPERATIONALLY COUPLE THE SENSOR ELEMENTS TO THE INTEGRATED CIRCUIT
20
SENSOR STACKS
22
TILE A PLURALITY OF SENSOR STACKS
24
PLANAR TILEABLE DETECTOR ARRAY
26

FIG. 1

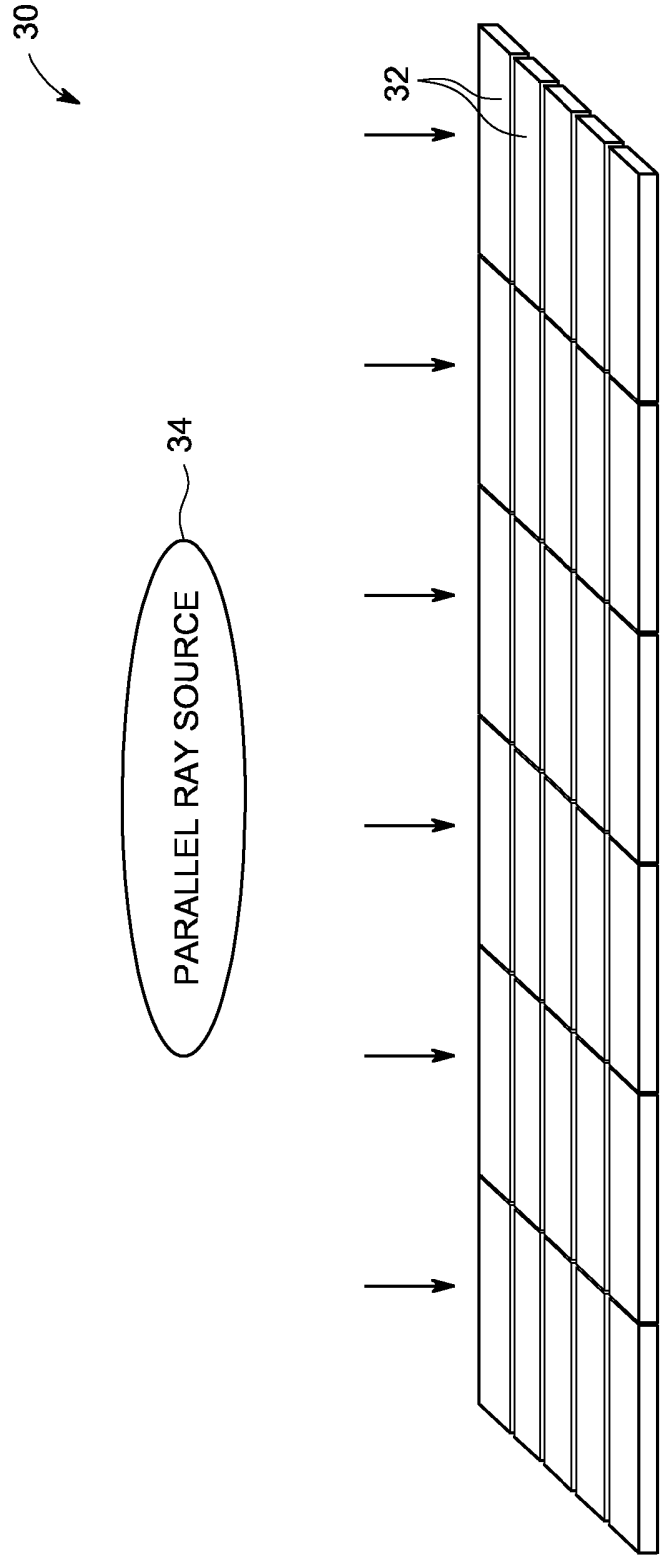

FIG. 2

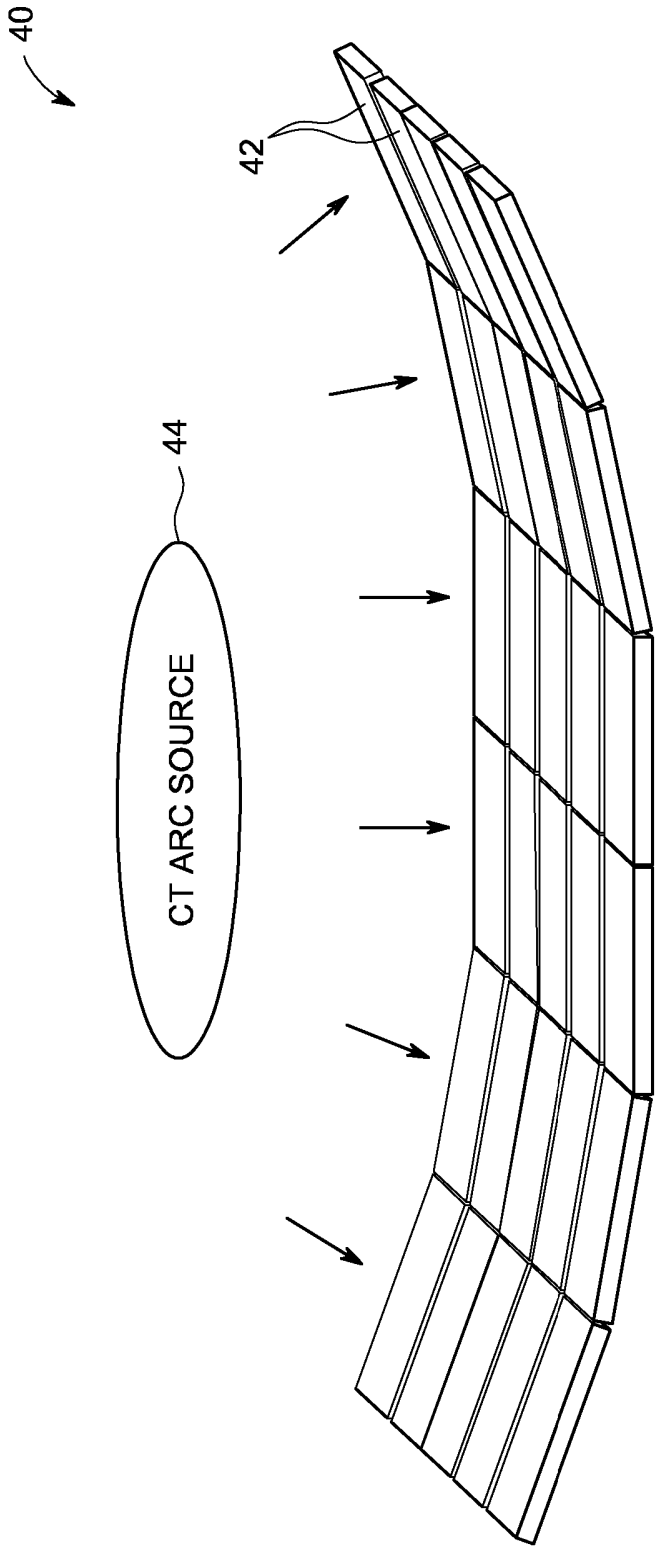

FIG. 3

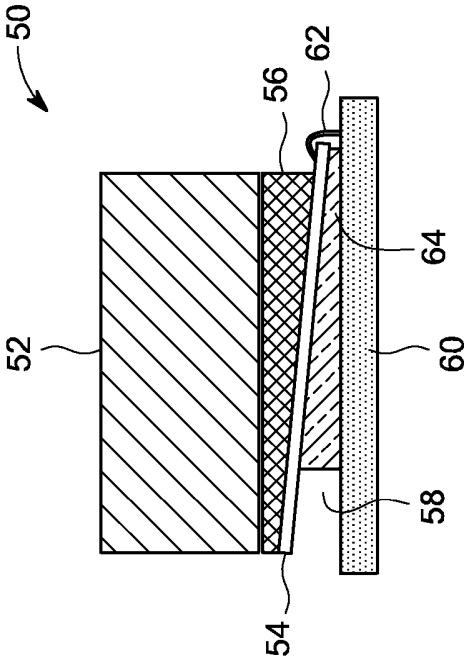

FIG. 4

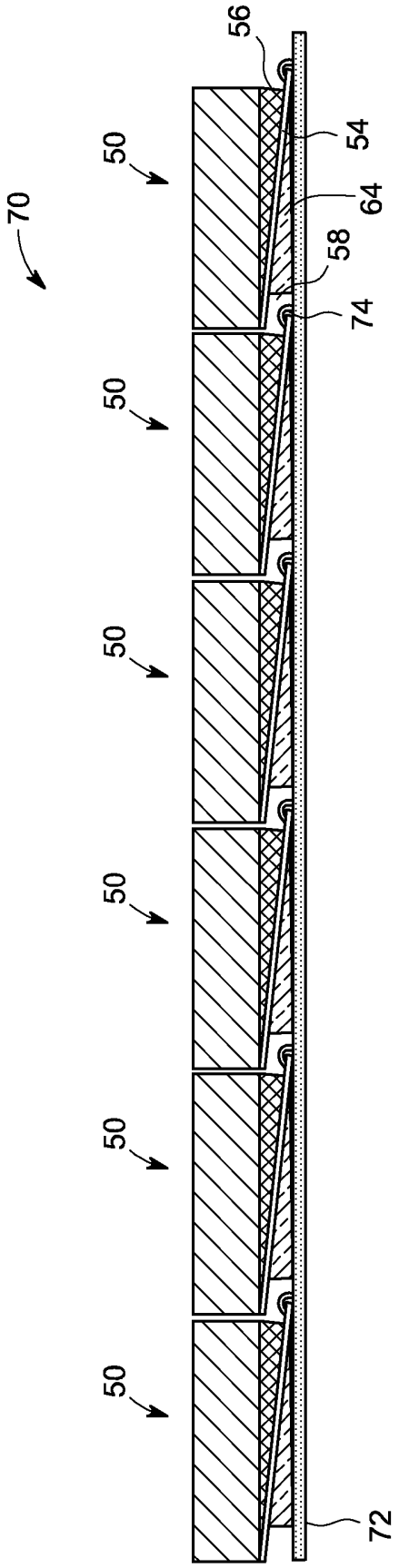

FIG. 5

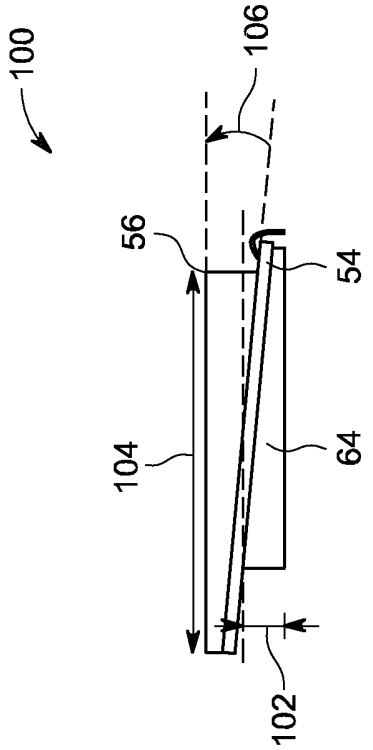

FIG. 7

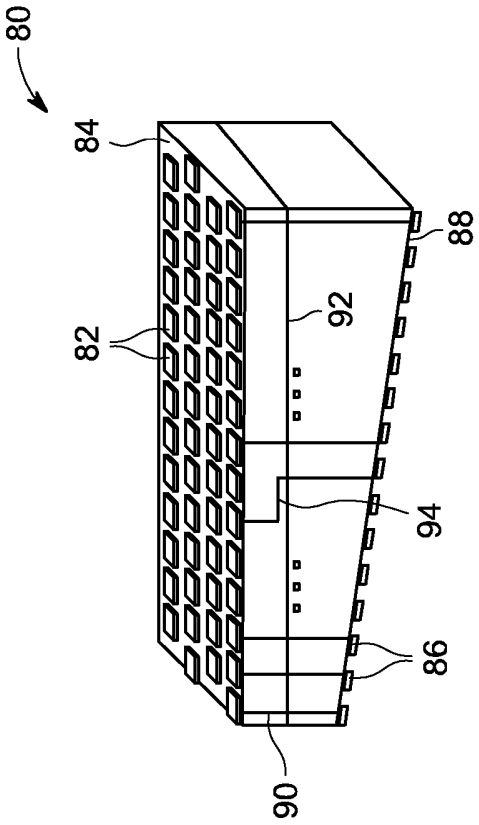

FIG. 6

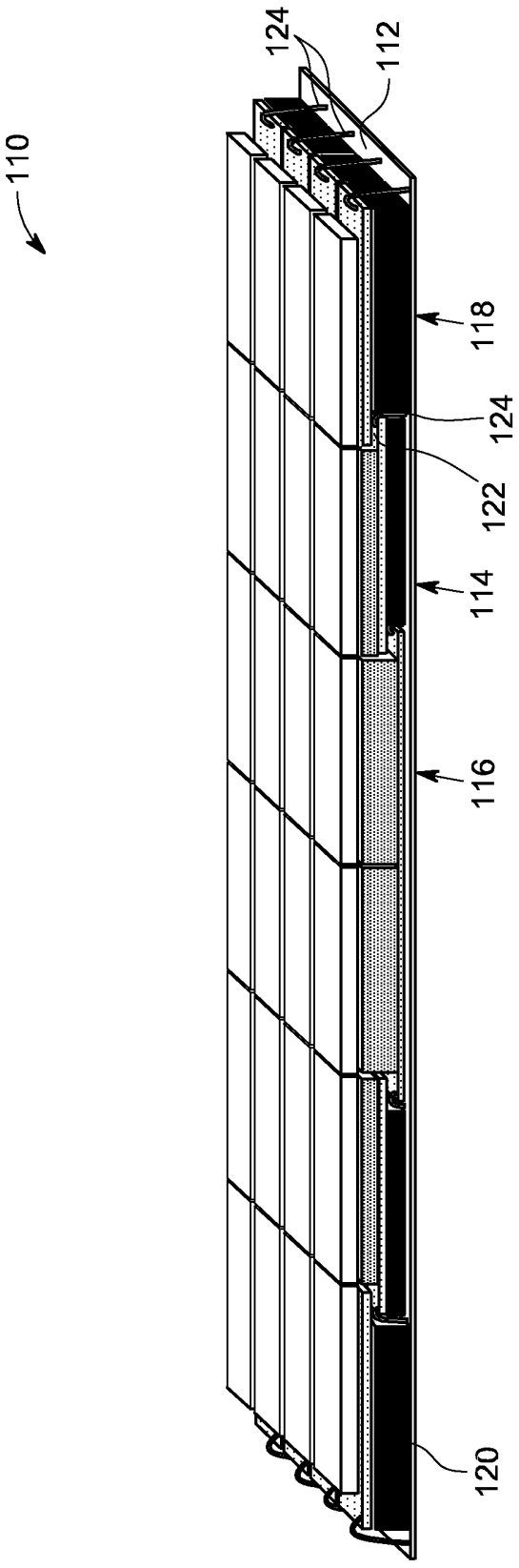

FIG. 8

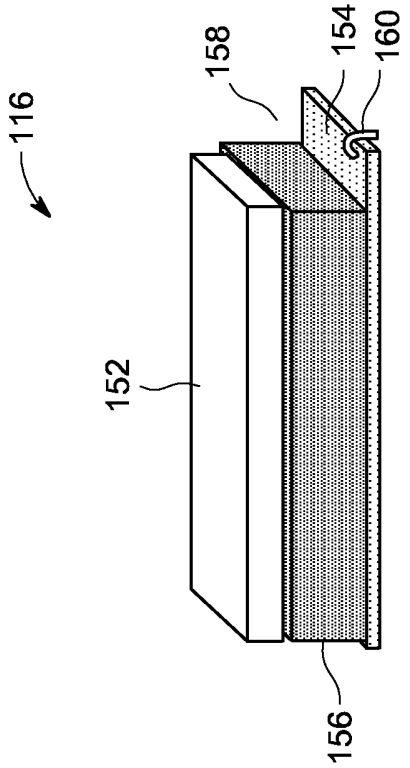

FIG. 10

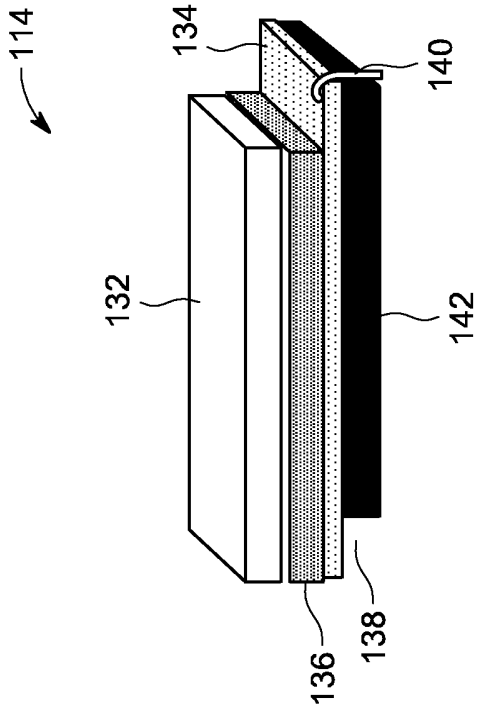

FIG. 9

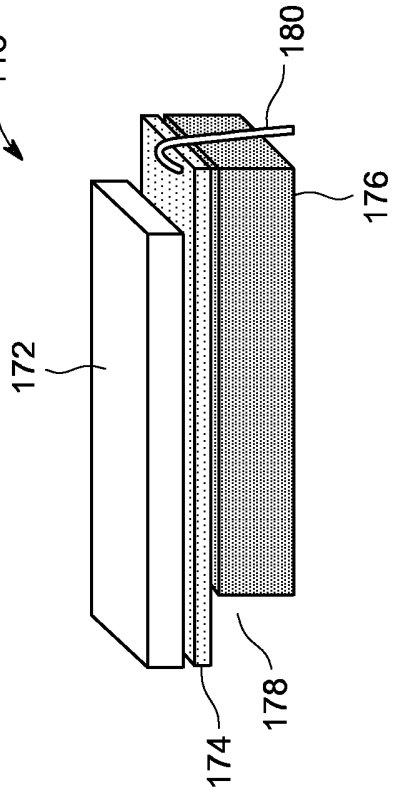

FIG. 11

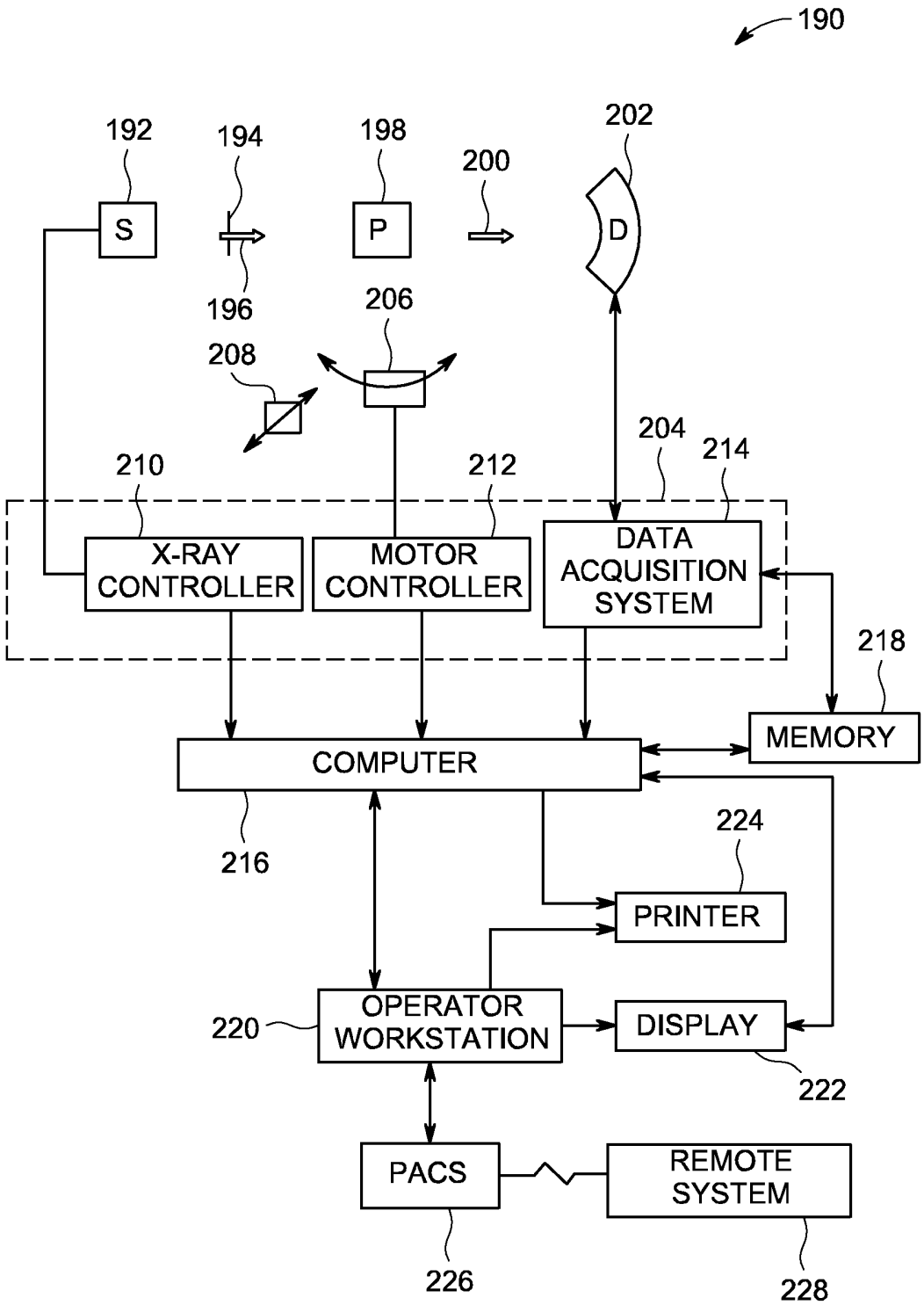
190
192
194
198
200
202
S
P
D
196
206
208
204
214
210
212
X-RAY CONTROLLER
MOTOR CONTROLLER
DATA ACQUISITION SYSTEM
218
MEMORY
COMPUTER
216
224
PRINTER
220
OPERATOR WORKSTATION
DISPLAY
222
PACS
REMOTE SYSTEM
226
228

FIG. 12

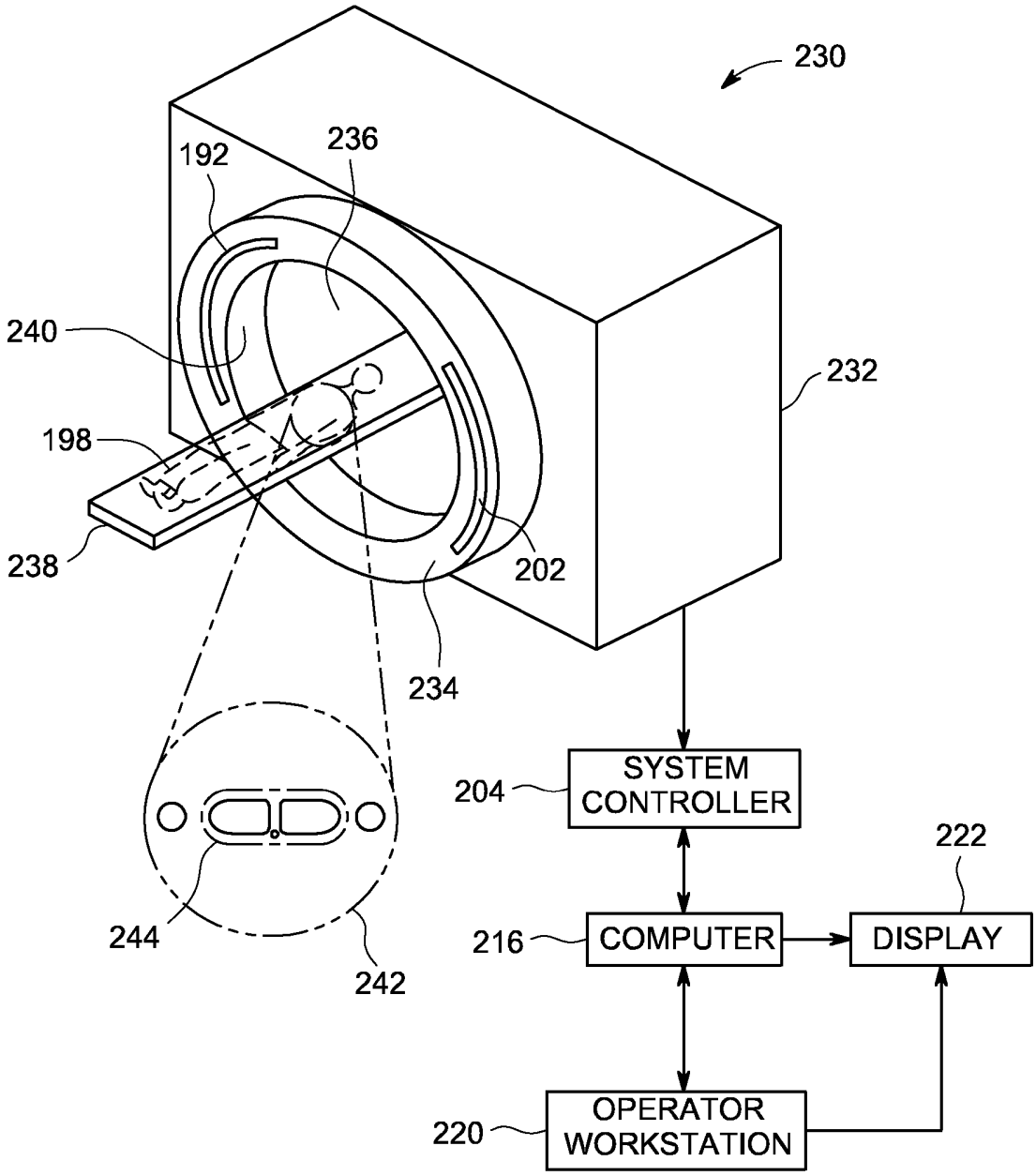
230
192
236
240
232
198
238
202
234
244
242
204
SYSTEM CONTROLLER
222
216
COMPUTER
DISPLAY
220
OPERATOR WORKSTATION

FIG. 13

Agentschap NL
Ministerie van Economische Zaken

OCTROOIAANVRAAG NR.:
NO 138100
NL 2007885

ONDERZOEKSRAPPORT

BETREFFENDE HET RESULTAAT VAN HET ONDERZOEK NAAR DE STAND VAN DE TECHNIEK

RELEVANTE LITERATUUR

Categorie[1]	Literatuur met, voor zover nodig, aanduiding van speciaal van belang zijnde tekstgedeelten of figuren.	Van belang voor conclusie(s) nr:	Classificatie (IPC)
	EENHEID VAN UITVINDING ONTBREEKT zie aanvullingsblad B		INV. H01L27/146 G01T1/24
X	US 2003/155516 A1 (SPARTIOTIS KONSTANTINOS [FI] ET AL) 21 augustus 2003 (2003-08-21) * alineas [0050], [0053], [0056] - [0059]; figuren 5A,5B,6A,6B,11 *	1-3,7-10	A61B6/00 H01L31/08
X	WO 2008/012748 A2 (KONINKL PHILIPS ELECTRONICS NV [NL]; WEEKAMP JOHANNUS W [NL]; PETERS S) 31 januari 2008 (2008-01-31) * alineas [0027] - [0033]; figuur 1 *	1,2,7	
X	EP 1 598 863 A1 (HAMAMATSU PHOTONICS KK [JP]) 23 november 2005 (2005-11-23) * alineas [0034] - [0042], [0048], [0051] - [0053], [0063], [0073] - [0075], [0079], [0099] - [0111]; figuren 1-6,9-10 *	1-3,7,9, 10	
			Onderzochte gebieden van de techniek
A	WO 2004/038810 A2 (GOLDPOWER LTD; PUHAKKA KIMMO; BENSON IAIN) 6 mei 2004 (2004-05-06) * figuren 1-6,13-14 *	1-3,7-9	H01L
A	WO 00/65376 A1 (SIMAGE OY [FI]; SPARTIOTIS KONSTANTINOS EVANGE [FI]; JURTHE STEFAN [FI] 2 november 2000 (2000-11-02) * figuren 4-6 *	1-3,7-9	

Indien gewijzigde conclusies zijn ingediend, heeft dit rapport betrekking op de conclusies ingediend op:

Plaats van onderzoek:	Datum waarop het onderzoek werd voltooid:	Bevoegd ambtenaar:
's-Gravenhage	13 juni 2013	Cabrita, Ana

[1] CATEGORIE VAN DE VERMELDE LITERATUUR

X: de conclusie wordt als niet nieuw of niet inventief beschouwd ten opzichte van deze literatuur
Y: de conclusie wordt als niet inventief beschouwd ten opzichte van de combinatie van deze literatuur met andere geciteerde literatuur van dezelfde categorie, waarbij de combinatie voor de vakman voor de hand liggend wordt geacht
A: niet tot de categorie X of Y behorende literatuur die de stand van de techniek beschrijft
O: niet-schriftelijke stand van de techniek
P: tussen de voorrangsdatum en de indieningsdatum gepubliceerde literatuur
T: na de indieningsdatum of de voorrangsdatum gepubliceerde literatuur die niet bezwarend is voor de octrooiaanvrage, maar wordt vermeld ter verheldering van de theorie of het principe dat ten grondslag ligt aan de uitvinding
E: eerdere octrooi(aanvrage), gepubliceerd op of na de indieningsdatum, waarin dezelfde uitvinding wordt beschreven
D: in de octrooiaanvrage vermeld
L: om andere redenen vermelde literatuur
&: lid van dezelfde octrooifamilie of overeenkomstige octrooipublicatie

EOB FORM 02.83 (P0414B)

GEBREK AAN EENHEID VAN UITVINDING

Octrooiaanvrage Nr.:
NO 138100
NL 2007885

AANVULLINGSBLAD B

De Instantie belast met het uitvoeren van het onderzoek naar de stand van de techniek heeft vastgesteld dat deze aanvrage meerdere uitvindingen bevat, te weten:

1. conclusies: 1-3, 7-9

   A method of forming a sensor stack and a detector array comprising a plurality of sensor stacks, wherein the method comprises a.o. the steps of providing an interposer having one or more elements, having through vias, between an integrated circuit and one or more sensor elements of a sensor array.

   ---

2. conclusies: 4, 5

   A method of forming a tileable detector array comprising forming a tileable sensor stack comprising: disposing a sensor element on a portion of an area of an integrated circuit; disposing a wedge shape interposer element, having through vias, between a sensor element and the integrated circuit, tiling a plurality of tileable sensor stacks on a substrate to form a tileable detector array.

   ---

3. conclusie: 6

   method of forming a tileable detector array comprising forming a first tileable stepped sensor stacks comprising: disposing a sensor element on a portion of an area of an integrated circuit; disposing a stepped interposer element, having through vias, between a sensor element and the integrated circuit; forming a second plurality of sensor stacks comprising: disposing a sensor element on a portion of an area of an integrated circuit; tiling the first plurality of tileable stepped sensor stacks and the second plurality of tileable sensor stacks on a substrate to form a tileable detector array.

Het vooronderzoek werd tot het eerste onderwerp beperkt.

AANHANGSEL BEHORENDE BIJ HET RAPPORT BETREFFENDE HET ONDERZOEK NAAR DE STAND VAN DE TECHNIEK, UITGEVOERD IN DE OCTROOIAANVRAGE NR.

NO 138100
NL 2007885

Het aanhangsel bevat een opgave van elders gepubliceerde octrooiaanvragen of octrooien (zogenaamde leden van dezelfde octrooifamilie), die overeenkomen met octrooischriften genoemd in het rapport.
De opgave is samengesteld aan de hand van gegevens uit het computerbestand van het Europees Octrooibureau per
De juistheid en volledigheid van deze opgave wordt noch door het Europees Octrooibureau, noch door het Bureau voor de Industriële eigendom gegarandeerd; de gegevens worden verstrekt voor informatiedoeleinden.

13-06-2013

In het rapport genoemd octrooigeschrift	Datum van publicatie	Overeenkomend(e) geschrift(en)	Datum van publicatie
US 2003155516 A1	21-08-2003	AU 2003223024 A1	22-09-2003
		EP 1516367 A2	23-03-2005
		US 2003155516 A1	21-08-2003
		WO 03077538 A2	18-09-2003
WO 2008012748 A2	31-01-2008	CN 101495247 A	29-07-2009
		EP 2046507 A2	15-04-2009
		US 2010156243 A1	24-06-2010
		WO 2008012748 A2	31-01-2008
EP 1598863 A1	23-11-2005	CN 1748300 A	15-03-2006
		EP 1598863 A1	23-11-2005
		IL 170458 A	28-02-2011
		JP 3935091 B2	20-06-2007
		JP 2004265959 A	24-09-2004
		KR 20060022636 A	10-03-2006
		US 2007075408 A1	05-04-2007
		WO 2004077549 A1	10-09-2004
WO 2004038810 A2	06-05-2004	AT 440383 T	15-09-2009
		AU 2003276401 A1	13-05-2004
		EP 1554760 A2	20-07-2005
		JP 2006504258 A	02-02-2006
		US 2008093560 A1	24-04-2008
		US 2011156273 A1	30-06-2011
		WO 2004038810 A2	06-05-2004
WO 0065376 A1	02-11-2000	AU 4603200 A	10-11-2000
		US 6703617 B1	09-03-2004
		WO 0065376 A1	02-11-2000

SCHRIFTELIJKE OPINIE

DOSSIER NUMMER	INDIENINGSDATUM	VOORRANGSDATUM	AANVRAAGNUMMER
NO138100	29.11.2011	30.11.2010	NL2007885

CLASSIFICATIE
INV. H01L27/146 G01T1/24 A61B6/00 H01L31/08

AANVRAGER
General Electric Company

Deze schriftelijke opinie bevat een toelichting op de volgende onderdelen:

- ☒ Onderdeel I Basis van de schriftelijke opinie
- ☐ Onderdeel II Voorrang
- ☒ Onderdeel III Vaststelling nieuwheid, inventiviteit en industriële toepasbaarheid niet mogelijk
- ☒ Onderdeel IV De aanvraag heeft betrekking op meer dan één uitvinding
- ☒ Onderdeel V Gemotiveerde verklaring ten aanzien van nieuwheid, inventiviteit en industriële toepasbaarheid
- ☐ Onderdeel VI Andere geciteerde documenten
- ☐ Onderdeel VII Overige gebreken
- ☐ Onderdeel VIII Overige opmerkingen

DE BEVOEGDE AMBTENAAR
Cabrita, Ana

Aanvraag nr.:

SCHRIFTELIJKE OPINIE

NL2007885

Onderdeel I Basis van de Schriftelijke Opinie

1. Deze schriftelijke opinie is opgesteld op basis van de meest recente conclusies ingediend voor aanvang van het onderzoek.

2. Met betrekking tot **nucleotide en/of aminozuur sequenties** die genoemd worden in de aanvraag en relevant zijn voor de uitvinding zoals beschreven in de conclusies, is dit onderzoek gedaan op basis van:

   a. type materiaal:

   ☐ sequentie opsomming

   ☐ tabel met betrekking tot de sequentie lijst

   b. vorm van het materiaal:

   ☐ op papier

   ☐ in elektronische vorm

   c. moment van indiening/aanlevering:

   ☐ opgenomen in de aanvraag zoals ingediend

   ☐ samen met de aanvraag elektronisch ingediend

   ☐ later aangeleverd voor het onderzoek

3. ☐ In geval er meer dan één versie of kopie van een sequentie opsomming of tabel met betrekking op een sequentie is ingediend of aangeleverd, zijn de benodigde verklaringen ingediend dat de informatie in de latere of additionele kopieën identiek is aan de aanvraag zoals ingediend of niet meer informatie bevatten dan de aanvraag zoals oorspronkelijk werd ingediend.

4. Overige opmerkingen:

Aanvraag nr.:

SCHRIFTELIJKE OPINIE

NL2007885

Onderdeel III Vaststelling nieuwheid, inventiviteit en industriële toepasbaarheid niet mogelijk

De vraag of de uitvinding in de aanvraag nieuw, inventief en industrieel toepasbaar is, wordt niet behandeld in deze schriftelijke opinie met betrekking tot:

☐ de gehele aanvraag

☒ conclusies 4-6

omdat:

☐ deze aanvraag of deze conclusies , betrekking hebben op materie waarvoor het niet zinvol is een schriftelijke opinie op te stellen.

☐ de beschrijving, figuren of deze conclusies , , zo onduidelijk zijn dat het niet zinvol is een schriftelijke opinie op te stellen.

☐ deze conclusies , onvoldoende steun vinden in de beschrijving waardoor het niet zinvol is een schriftelijke opinie op te stellen.

☒ geen onderzoek naar de stand van de techniek is uitgevoerd voor deze conclusies 4-6.

☐ een zinvolle schriftelijke opinie niet opgesteld kon worden omdat de sequentie opsomming niet beschikbaar was in het juiste formaat, of in het geheel niet beschikbaar was (WIPO ST25).

☐ een zinvolle schriftelijke opinie niet opgesteld kon worden zonder de tabellen met betrekking tot de sequentie opsommingen; of deze tabellen waren niet beschikbaar in elektronische vorm.

☐ Zie aparte bladzijde

Onderdeel IV De aanvraag heeft betrekking op meer dan één uitvinding

1. Vastgesteld is dat de octrooiaanvraag betrekking heeft op meer dan één uitvinding.

   Zie aparte bladzijde

2. Het onderzoek naar de stand van de techniek is beperkt tot de eerstgenoemde uitvinding in de conclusies en betreft:

   ☐ alle conclusies

   ☒ conclusies: (zie nieuwheidsrapport)

Aanvraag nr.:

SCHRIFTELIJKE OPINIE

NL2007885

Onderdeel V Gemotiveerde verklaring ten aanzien van nieuwheid, inventiviteit en industriële toepasbaarheid

1. Verklaring

Nieuwheid	Ja:	Conclusies	3, 8-10
	Nee:	Conclusies	1, 2, 7
Inventiviteit	Ja:	Conclusies	
	Nee:	Conclusies	1-3, 7-10
Industriële toepasbaarheid	Ja:	Conclusies	1-3, 7-10
	Nee:	Conclusies	

2. Citaties en toelichting:

Zie aparte bladzijde

Re Item IV

Lack of unity of invention

1 It is considered that there are three inventions covered by the claims indicated as follows:

i. claims: 1-3, 7-10

A method of forming a sensor stack and a detector array comprising a plurality of sensor stacks, wherein the method comprises a.o.: providing an integrated circuit on a substrate; providing an interposer having one or more elements, having through vias, between the integrated circuit and one or more sensor elements of a sensor array.

problem solved/technical effect: provision of a planar tiled detector array wherein the interposer facilitates the electrical connections between the sensor elements and the circuitry while maintaining a fine pitch.

ii. claims: 4, 5

A method of forming a tileable detector array comprising forming a tileable sensor stack comprising: disposing a sensor element on a portion of an area of an integrated circuit; disposing a wedge shape interposer element, having through vias, between a sensor element and the integrated circuit, tiling a plurality of tileable sensor stacks on a substrate to form a tileable detector array.

problem solved/technical effect: provision of a planar tiled detector array wherein the wedge shape interposer creates free space to other electronics and/or connections and the wedge shape increases the geometrical freedom of the tiled array.

iii. claim: 6

method of forming a tileable detector array comprising forming a first tileable stepped sensor stacks comprising: disposing a sensor element on a portion of an area of an integrated circuit; disposing a stepped interposer element, having through vias, between a sensor element and the integrated circuit; forming a second plurality of sensor stacks comprising: disposing a sensor element on a portion of an area of an

integrated circuit; tiling the first plurality of tileable stepped sensor stacks and the second plurality of tileable sensor stacks on a substrate to form a tileable detector array.

problem solved/technical effect: provision of a tiled detector array using stepped sensor stacks having a stepped interposer combined with sensor stacks without interposer. Due to the difference in thickness of the interposer and/or due to its absence a tiled detector array having more freedom of elements choices is obtained.

1.1 The reasons for which the inventions are not so linked as to form a single general inventive concept, are as follows:

The prior art has been identified as D1 and discloses a method of forming a tileable sensor stack comprising (figures 5A,. 5B, 6A, 10, 11, [0050], [0053]): providing a substrate having a first side and a second side (130); providing an integrated circuit (132) having a first side and a second side on a first side of the substrate, wherein the integrated circuit comprises a first plurality of contact pads disposed on the first side of the integrated circuit (136, 140); providing a sensor array having a plurality of sensor elements (90, 100), wherein each of the sensor elements has a first side and a second side, and wherein the sensor array comprises a second plurality of contact pads (102) disposed on a second side of the sensor array; disposing an interposer (170) having one or more interposer elements and one or more through vias (178) disposed therethrough between the one or more sensor elements of the sensor array and the integrated circuit to raise the sensor array away from the first side of the integrated circuit such that a plane of the one or more sensor elements is locally normal to a sensor stack normal, wherein the interposer is configured to operationally couple the second side of the sensor elements in the sensor array to the first side of the integrated circuit; and operationally electrically coupling the first plurality of contact pads on the first side of the integrated circuit to the second plurality of contact pads on the second side of the sensor array to form a tileable sensor stack.

1.2 It follows that the following technical features of claim 4 make a contribution over the prior art and can be considered as a special technical feature: disposing a sensor element on a portion of an area of an integrated circuit;

disposing a wedge shape interposer element, having through vias, between a sensor element and the integrated circuit, tiling a plurality of tileable sensor stacks on a substrate to form a tileable detector array.

1.2.1 The problem solved by this special technical feature can therefore be construed as the provision of a planar tiled detector array wherein the wedge shape interposer creates free space to other electronics and/or connections and the wedge shape increases the geometrical freedom of the tiled array.

1.3 Similarly, the following technical features of claim 6 make a contribution over the prior art and can be considered as a special technical feature: forming a tileable detector array comprising forming a first tileable stepped sensor stacks comprising: disposing a sensor element on a portion of an area of an integrated circuit; disposing a stepped interposer element, having through vias, between a sensor element and the integrated circuit; forming a second plurality of sensor stacks comprising: disposing a sensor element on a portion of an area of an integrated circuit; tiling the first plurality of tileable stepped sensor stacks and the second plurality of tileable sensor stacks on a substrate to form a tileable detector array.

1.3.1 The problem solved by this special technical feature can therefore be construed as the provision of a tiled detector array combining sensor stacks using a stepped interposer and sensor stacks without interposer.

1.4 Also, examining the possible correspondence by technical effect, one finds that the technical effect of the first invention is facilitating the electrical connections between the sensor elements and the circuitry and that the technical effect of the second and third inventions is respectively increase free space for electronics and increase the freedom of choice of elements.

1.5 This appears to show lack of corresponding technical effect as well. Consequently, neither the objective problem underlying the subjects of the claimed inventions, nor their solutions defined by the special technical features allow for a relationship to be established between the said inventions, which involves a single general inventive concept.

In conclusion, the groups of claims are not linked by common or corresponding special technical features and define three different inventions not linked by a single general inventive concept.

The application, hence does not meet the requirements of unity of invention.

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Re Item V

Reasoned statement with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

Reference is made to the following documents:

D1 US 2003/155516 A1 (SPARTIOTIS KONSTANTINOS [FI] ET AL) 21 augustus 2003 (2003-08-21)

D2 WO 2008/012748 A2 (KONINKL PHILIPS ELECTRONICS NV [NL]; WEEKAMP JOHANNUS W [NL]; PETERS S) 31 januari 2008 (2008-01-31)

1 The present application does not meet the criteria of patentability, because the subject-matter of claims 1, 2 and 7 is not new.

1.1 D1 discloses a sensor stack and a method for forming the sensor stack comprising (figures 5A,. 5B, 6A, 10, 11, [0050], [0053]): providing a substrate having a first side and a second side (130); providing an integrated circuit (132) having a first side and a second side on a first side of the substrate, wherein the integrated circuit comprises a first plurality of contact pads disposed on the first side of the integrated circuit (136, 140); providing a sensor array having a plurality of sensor elements (90, 100), wherein each of the sensor elements has a first side and a second side, and wherein the sensor array comprises a second plurality of contact pads (102) disposed on a second side of the sensor array; disposing an interposer (170) having one or more interposer elements and one or more through vias (178) disposed therethrough between the one or more sensor elements of the sensor array and the integrated circuit to raise the sensor array away from the first side of the integrated circuit such that a plane of the one or more sensor elements is locally normal to a sensor stack normal, wherein the interposer is configured to operationally couple the second side of the sensor elements in the sensor array to the first side of the integrated circuit; and operationally electrically coupling the first plurality of contact pads on the first side of the integrated circuit to the second plurality of contact pads on the second side of the sensor array to form a tileable sensor stack.

1.2 D2 discloses discloses a sensor stack and a method for forming the sensor stack comprising (figure 1, [0028], [0029]): providing an integrated circuit (14) having a first side and a second side on a first side of a substrate, wherein the integrated circuit comprises a first plurality of contact pads (16) disposed on the first side of the integrated circuit; providing a sensor array having a plurality of sensor elements (22), wherein each of the sensor elements has a first side and a second side, and wherein the sensor array comprises a second plurality of contact pads disposed on a second side of the sensor array; disposing an interposer (12) having one or more interposer elements and one or more through vias (26) disposed therethrough between the one or more sensor elements of the sensor array and the integrated circuit to raise the sensor array away from the first side of the integrated circuit such that a plane of the one or more sensor elements is locally normal to a sensor stack normal, wherein the interposer is configured to operationally couple the second side of the sensor elements in the sensor array to the first side of the integrated circuit; and operationally electrically coupling the first plurality of contact pads on the first side of the integrated circuit to the second plurality of contact pads on the second side of the sensor array to form a tileable sensor stack.

The subject-matter of claims 1 and 7 is thus not novel.

1.3 D2 further discloses ([0031]) that the interposer (or interposer elements) has an angled profile and that the interposer (or/and interposer elements) has a rectangular shape.

Hence the subject-matter of claim 2 is not new.

2 Dependent claims 3, 8-10 do not contain any features which, in combination with the features of any claim to which they refer, meet the requirements of novelty and/or inventive step. These claims relate to common features (adding a spacer, changing geometry of the interposer, adding routing layers and routing traces to the interposer) which are considered to be obvious or freely available for the skilled person in the field of imaging arrays. These features can not be the basis of an inventive step. The subject-matter of these claims is thus not inventive.