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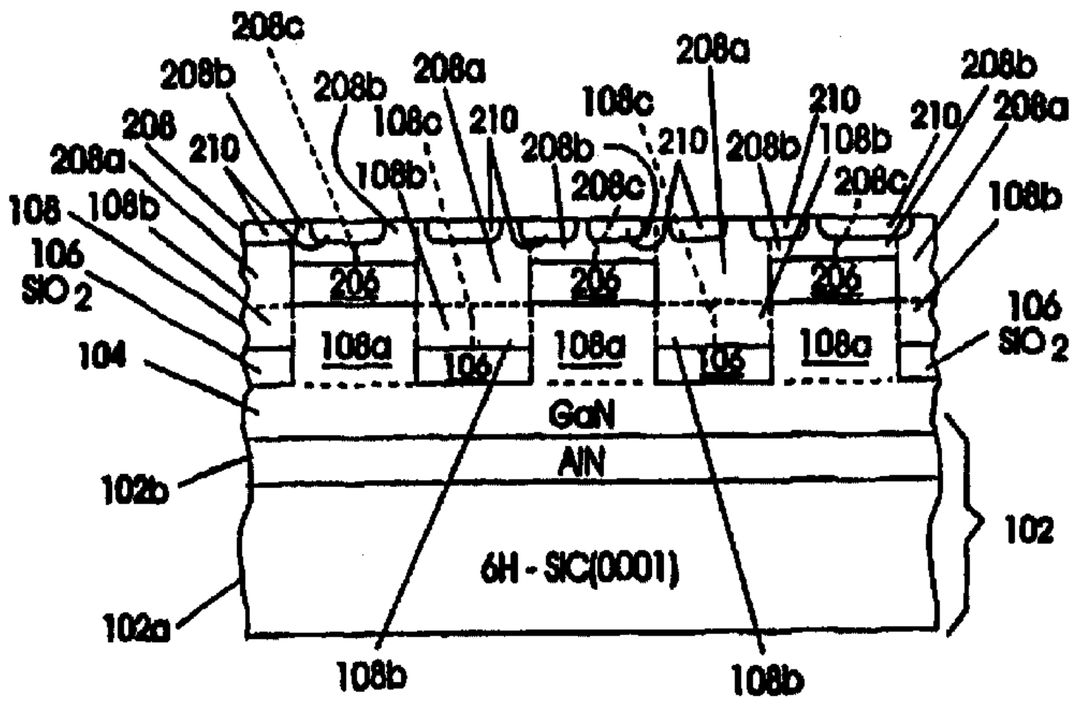
(54) **PROCEDE PERMETTANT DE PRODUIRE DES COUCHES SEMI-CONDUCTRICES DE NITRURE DE GALLIUM PAR CROISSANCE DE RECOUVREMENT LATERALE A TRAVERS DES MASQUES, ET STRUCTURES SEMI-CONDUCTRICES DE NITRURE DE GALLIUM AINSI PRODUITES**

(54) **METHODS OF FABRICATING GALLIUM NITRIDE SEMICONDUCTOR LAYERS BY LATERAL OVERGROWTH THROUGH MASKS, AND GALLIUM NITRIDE SEMICONDUCTOR STRUCTURES FABRICATED THEREBY**



(57) L'invention concerne un procédé permettant de produire une couche semi-conductrice de nitrure de gallium. Ce procédé consiste à masquer une couche (104) de nitrure de gallium sous-jacente avec un premier masque (106) comprenant une première série d'ouvertures et à faire croître la couche (104) de nitrure de gallium à travers cette première série d'ouvertures et sur le premier masque, et à former ainsi la couche (108 a,b) de nitrure de gallium de recouvrement. On masque ensuite cette couche de recouvrement avec un second masque (206) comprenant une seconde série d'ouvertures. La seconde série d'ouvertures est décalée

(57) A gallium nitride semiconductor layer is fabricated by masking an underlying gallium nitride layer (104) with a first mask (106) that includes a first array of openings therein and growing the underlying gallium nitride layer (104) through the first array of openings and onto the first mask, to thereby form a first overgrown gallium nitride semiconductor layer (108a, b). The first overgrown layer is then masked with the second mask (206) that includes a second array of openings therein. The second array of openings is laterally offset from the first array of openings. The first overgrown gallium nitride layer (108a, b) is then grown through the second

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latéralement par rapport à la première série d'ouvertures. On fait ensuite croître la première couche (108 a,b) de nitrure de gallium de recouvrement à travers la seconde série d'ouvertures et sur le second masque (206) de manière à former une seconde couche (208 a,b) de recouvrement semi-conductrice de nitrure de gallium. Des dispositifs (210) micro-électronique peuvent être formés dans cette seconde couche

array of openings and onto the second mask (206), to thereby form a second overgrown gallium nitride semiconductor layer (208a, b). Microelectronic devices (210) may then be formed in the second overgrown gallium nitride semiconductor layer (208a, b).

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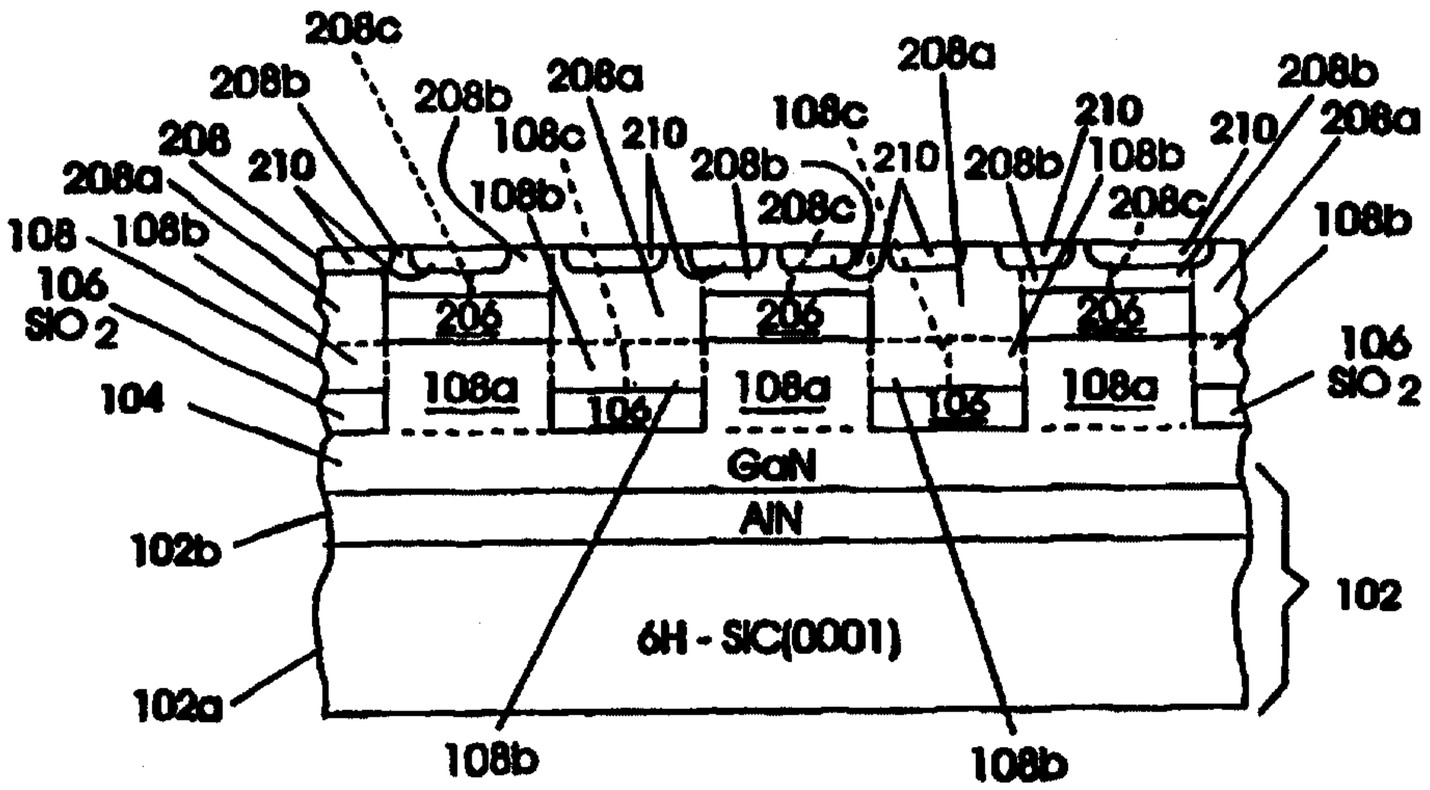

(57) Abstract

A gallium nitride semiconductor layer is fabricated by masking an underlying gallium nitride layer (104) with a first mask (106) that includes a first array of openings therein and growing the underlying gallium nitride layer (104) through the first array of openings and onto the first mask, to thereby form a first overgrown gallium nitride semiconductor layer (108a, b). The first overgrown layer is then masked with the second mask (206) that includes a second array of openings therein. The second array of openings is laterally offset from the first array of openings. The first overgrown gallium nitride layer (108a, b) is then grown through the second array of openings and onto the second mask (206), to thereby form a second overgrown gallium nitride semiconductor layer (208a, b). Microelectronic devices (210) may then be formed in the second overgrown gallium nitride semiconductor layer (208a, b).

METHODS OF FABRICATING GALLIUM NITRIDE SEMICONDUCTOR LAYERS BY LATERAL OVERGROWTH THROUGH MASKS, AND GALLIUM NITRIDE SEMICONDUCTOR STRUCTURES FABRICATED THEREBY

Field of the Invention

This invention relates to microelectronic devices and fabrication methods, and more particularly to gallium nitride semiconductor devices and fabrication methods therefor.

Background of the Invention

Gallium nitride is being widely investigated for microelectronic devices including but not limited to transistors, field emitters and optoelectronic devices. It will be understood that, as used herein, gallium nitride also includes alloys of gallium nitride such as aluminum gallium nitride, indium gallium nitride and aluminum indium gallium nitride.

A major problem in fabricating gallium nitride-based microelectronic devices is the fabrication of gallium nitride semiconductor layers having low defect densities. It is known that one contributor to defect density is the substrate on which the gallium nitride layer is grown. Accordingly, although gallium nitride layers have been grown on sapphire substrates, it is known to reduce defect density by growing gallium nitride layers on aluminum nitride buffer layers which are themselves formed on silicon carbide substrates. Notwithstanding these advances, continued reduction in defect density is desirable.

It is also known to fabricate gallium nitride structures through openings in a mask. For example, in fabricating field emitter arrays, it is known to selectively grow gallium nitride on stripe or circular patterned substrates. See, for example, the publications by coinventor Nam et al. entitled *"Selective Growth of GaN and $Al_{0.2}Ga_{0.8}N$ on GaN/AlN/6H-SiC(0001) Multilayer Substrates Via Organometallic Vapor Phase Epitaxy"*, Proceedings of the Materials Research Society, December 1996, and *"Growth of GaN and $Al_{0.2}Ga_{0.8}N$ on Patterened Substrates via*

Organometallic Vapor Phase Epitaxy", Japanese Journal of Applied Physics., Vol. 36, Part 2, No. 5A, May 1997, pp. L-532-L535. As disclosed in these publications, undesired ridge growth or lateral overgrowth may occur under certain conditions.

In a publication entitled *"Lateral Epitaxy of Low Defect Density GaN Layers Via Organometallic Vapor Phase Epitaxy"*, to Nam et al., Applied Physics Letters, Vol. 71, No. 18, November 3, 1997, pp. 2638-2640, organometallic vapor phase lateral epitaxy and coalescence of GaN layers originating from GaN stripes deposited within 3-μm-wide windows spaced 3 μm apart and contained in SiO_2 masks on GaN/AlN/6H-SiC(0001) substrates are reported. The extent and microstructural characteristics of the lateral overgrowth were a strong function of strip orientation. A high density of threading dislocations, originating form the interface of the underlying GaN with the AlN buffer layer, were contained in the GaN grown in the window regions. The overgrowth regions, by contrast, contained a very low density of dislocations. The coalesced layers had a rms surface roughness of 0.25 nm.

In European Patent Application EP 0 852 416 A1, an insulating member of an amorphous structure is partially opened to expose a substrate is formed on the substrate. At least a compound semiconductor containing at least nitrogen as a constituent element is deposited on the insulating member and the substrate exposed by the opening thereby to form a semiconductor material. A semiconductor material configured of the first semiconductor material or configured of the first semiconductor material and another semiconductor material grown on the first semiconductor material is processed thereby to form a semiconductor device.

Summary of the Invention

It is therefore an object of the present invention to provide improved methods of fabricating gallium nitride semiconductor layers, and improved gallium nitride layers so fabricated.

It is another object of the invention to provide methods of fabricating gallium nitride semiconductor layers that can have low defect densities, and gallium nitride semiconductor layers so fabricated.

These and other objects are provided, according to the present invention, by fabricating a gallium nitride semiconductor layer by laterally growing an underlying gallium nitride layer to thereby form a laterally grown gallium nitride semiconductor layer, and forming microelectronic devices in the laterally grown gallium nitride

semiconductor layer. In a preferred embodiment, a gallium nitride semiconductor layer is fabricated by masking an underlying gallium nitride layer with a mask that includes an array of openings therein and growing the underlying gallium nitride layer through the array of openings and onto the mask, to thereby form an overgrown gallium nitride semiconductor layer. Microelectronic devices may then be formed in the overgrown gallium nitride semiconductor layer.

It has been found, according to this aspect of the present invention, that although dislocation defects may propagate vertically from the underlying gallium nitride layer to the grown gallium nitride layer above the mask openings, the overgrown gallium nitride layer is relatively defect-free. Accordingly, high performance microelectronic devices may be formed in the overgrown gallium nitride semiconductor layer.

According to another aspect of the present invention, the overgrown gallium nitride semiconductor layer is overgrown until the overgrown gallium nitride layer coalesces on the mask, to form a continuous overgrown monocrystalline gallium nitride semiconductor layer. The overgrown layer can thus have overgrown regions of relatively low defect in the area of coalescence and regions of relatively high defects over the mask openings.

According to another aspect of the present invention, a gallium nitride semiconductor layer is fabricated by laterally growing an underlying gallium nitride layer to thereby form a first laterally grown gallium nitride semiconductor layer, and laterally growing the first laterally grown gallium nitride layer to thereby form a second laterally grown gallium nitride semiconductor layer. Microelectronic devices may then be formed in the second laterally grown gallium nitride semiconductor layer.

More specifically, in a preferred embodiment, a gallium nitride semiconductor layer is fabricated by masking an underlying gallium nitride layer with a first mask that includes a first array of openings therein and growing the underlying gallium nitride layer through the first array of openings and onto the first mask, to thereby form a first overgrown gallium nitride semiconductor layer. The first overgrown layer is then masked with the second mask that includes a second array of openings therein. The second array of openings is laterally offset from the first array of openings. The first overgrown gallium nitride layer is then grown through the second array of openings and onto the second mask, to thereby form a second overgrown gallium nitride semiconductor layer. Microelectronic devices may then be formed in the second overgrown gallium nitride semiconductor layer.

It has been found, according to this aspect of the present invention, that although dislocation defects may propagate vertically from the underlying gallium nitride layer to the grown gallium nitride layer above the first mask openings, the first overgrown gallium nitride layer is relatively defect-free. Moreover, since the second array of mask openings is laterally offset from the first array of mask openings, the relatively defect-free overgrown first gallium nitride layer propagates through the second array of openings and onto the second mask. Accordingly, high performance microelectronic devices may be formed in the second overgrown gallium nitride semiconductor layer.

According to another aspect of the present invention, the second overgrown gallium nitride semiconductor layer is overgrown until the second overgrown gallium nitride layer coalesces on the second mask, to form a continuous overgrown monocrystalline gallium nitride semiconductor layer. The entire continuous overgrown layer can thus be relatively defect-free compared to the underlying gallium nitride layer.

The first and second gallium nitride semiconductor layers may be grown using metalorganic vapor phase epitaxy (MOVPE). Preferably, the openings in the masks are stripes that are oriented along the $<1\bar{1}00>$ direction of the underlying gallium nitride layer. The overgrown gallium nitride layers may be grown using triethylgallium (TEG) and ammonia (NH_3) precursors at 1000-1100°C and 45 Torr. Preferably, TEG at 13-39μmol/min and NH_3 at 1500 sccm are used in combination with 3000 sccm H_2 diluent. Most preferably, TEG at 26μmol/min, NH_3 at 1500 sccm and H_2 at 3000 sccm at a temperature of 1100°C and 45 Torr are used. The underlying gallium nitride layer preferably is formed on a substrate, which itself includes a buffer layer such as aluminum nitride, on a substrate such as 6H-SiC(0001).

Gallium nitride semiconductor structures according to the present invention include an underlying gallium nitride layer, a lateral gallium nitride layer that extends from the underlying gallium nitride layer, and a plurality of microelectronic devices in the lateral gallium nitride layer. In a preferred embodiment, gallium nitride semiconductor structures according to the present invention include an underlying gallium nitride layer and a patterned layer (such as a mask) that includes an array of openings therein, on the underlying gallium nitride layer. A vertical gallium nitride layer extends from the underlying gallium nitride layer through the array of openings. A lateral gallium nitride layer extends from the vertical gallium nitride layer onto the patterned layer, opposite the underlying gallium nitride layer. A plurality of microelectronic devices including but not limited to optoelectronic devices and field emitters, are formed in the lateral gallium nitride layer.

Preferably, the lateral gallium nitride layer is a continuous monocrystalline gallium nitride semiconductor layer. The underlying gallium nitride layer and the vertical gallium nitride layer both include a predetermined defect density, and the lateral gallium nitride semiconductor layer is of lower defect density than the predetermined defect density. Accordingly, low defect density gallium nitride semiconductor layers may be produced, to thereby allow the production of high-performance microelectronic devices.

Other gallium nitride semiconductor structures according to the present invention include an underlying gallium nitride layer, a first lateral gallium nitride layer that extends from the underlying gallium nitride layer and a second lateral

gallium nitride layer that extends from the first lateral gallium nitride layer. A plurality of microelectronic devices are provided in the second lateral gallium nitride layer.

In a preferred embodiment, gallium nitride semiconductor structures according to the present invention include an underlying gallium nitride layer and a first mask that includes a first array of openings therein, on the underlying gallium nitride layer. A first vertical gallium nitride layer extends from the underlying gallium nitride layer through the first array of openings. A first lateral gallium nitride layer extends from the vertical gallium nitride layer onto the mask, opposite the underlying gallium nitride layer. A second mask on the first lateral gallium nitride layer includes a second array of openings therein that are laterally offset from the first array of openings. A second vertical gallium nitride layer extends from the first lateral gallium nitride layer and through the second array of openings. A second lateral gallium nitride layer extends from the second vertical gallium nitride layer onto the second mask, opposite the first lateral gallium nitride layer. A plurality of microelectronic devices including but not limited to optoelectronic devices and field emitters, are formed in the second vertical gallium nitride layer and in the second lateral gallium nitride layer.

Preferably, the second lateral gallium nitride layer is a continuous monocrystalline gallium nitride semiconductor layer. The underlying gallium nitride layer includes a predetermined defect density, and the second vertical and lateral gallium nitride semiconductor layers are of lower defect density than the predetermined defect density. Accordingly, continuous low defect density gallium nitride semiconductor layers may be produced, to thereby allow the production of high-performance microelectronic devices, using laterally offset masks.

Brief Description of the Drawings

Figure 1 is a cross-sectional view of first embodiments of gallium nitride semiconductor structures according to the present invention.

Figures 2-5 are cross-sectional views of structures of Figure 1 during intermediate fabrication steps, according to the present invention.

Figure 6 is a cross-sectional view of second embodiments of gallium nitride semiconductor structures according to the present invention.

Figure 7-14 are cross-sectional views of structures of Figure 6 during intermediate fabrication steps, according to the present invention.

Detailed Description of Preferred Embodiments

The present invention now will be described more fully hereinafter with reference to the accompanying drawings, in which preferred embodiments of the invention are shown. This invention may, however, be embodied in many different forms and should not be construed as limited to the embodiments set forth herein; rather, these embodiments are provided so that this disclosure will be thorough and complete, and will fully convey the scope of the invention to those skilled in the art. In the drawings, the thickness of layers and regions are exaggerated for clarity. Like numbers refer to like elements throughout. It will be understood that when an element such as a layer, region or substrate is referred to as being "on" another element, it can be directly on the other element or intervening elements may also be present. In contrast, when an element is referred to as being "directly on" another element, there are no intervening elements present. Moreover, each embodiment described and illustrated herein includes its complementary conductivity type embodiment as well.

Referring now to Figure 1, gallium nitride semiconductor structures according to the present invention are illustrated. The gallium nitride structures **100** include a substrate **102**. The substrate may be sapphire or gallium nitride. However, preferably, the substrate includes a 6H-SiC(0001) substrate **102a** and an aluminum nitride buffer layer **102b** on the silicon carbide substrate **102a** The aluminum nitride buffer layer **102b** may 0.01μm thick.

The fabrication of substrate **102** is well known to those having skill in the art and need not be described further. Fabrication of silicon carbide substrates are described, for example, in U.S. Patents 4,865,685 to Palmour; Re 34,861 to Davis et al.; 4,912,064 to Kong et al. and 4,946,547 to Palmour et al., the disclosures of which are hereby incorporated herein by reference. Also, the crystallographic designation conventions used herein are well known to those having skill in the art, and need not be described further.

An underlying gallium nitride layer **104** is also included on buffer layer **102b** opposite substrate **102a**. The underlying gallium nitride layer **104** may be between

about 1.0 and 2.0μm thick, and may be formed using heated metalorganic vapor phase epitaxy (MOVPE). The underlying gallium nitride layer generally has an undesired relatively high defect density, for example dislocation densities of between about 10^8 and $10^{10}cm^{-2}$. These high defect densities may result from mismatches in lattice parameters between the buffer layer **102b** and the underlying gallium nitride layer **104**. These high defect densities may impact performance of microelectronic devices formed in the underlying gallium nitride layer **104**.

Still continuing with the description of Figure 1, a mask such as a silicon dioxide mask **106** is included on the underlying gallium nitride layer **104**. The mask **106** includes an array of openings therein. Preferably, the openings are stripes that extend along the $<1\bar{1}00>$ direction of the underlying gallium nitride layer **104**. The mask **106** may have a thickness of about 1000Å and may be formed on the underlying gallium nitride layer **104** using low pressure chemical vapor deposition (CVD) at 410°C. The mask **106** may be patterned using standard photolithography techniques and etched in a buffered hydrofluoric acid (HF) solution.

Continuing with the description of Figure 1, a vertical gallium nitride layer **108a** extends from the underlying gallium nitride layer **104** and through the array of openings in the mask **106**. As used herein, the term "vertical" means a direction that is orthogonal to the faces of the substrate **102**. The vertical gallium nitride layer **108a** may be formed using metalorganic vapor phase epitaxy at about 1000-1100°C and 45 Torr. Precursors of triethygallium (TEG) at 13-39μmol/min and ammonia (NH_3) at 1500 sccm may be used in combination with a 3000 sccm H_2 diluent, to form the vertical gallium nitride layer **108a**.

Still continuing with the description of Figure 1, the gallium nitride semiconductor structure **100** also includes a lateral gallium nitride layer **108b** that extends laterally from the vertical gallium nitride layer **108a** onto the mask **106** opposite the underlying gallium nitride layer **104**. The lateral gallium nitride layer **108b** may be formed using metalorganic vapor phase epitaxy as described above. As used herein, the term "lateral" denotes a direction parallel to the faces of substrate **102**.

As shown in Figure 1, lateral gallium nitride layer **108b** coalesces at interfaces **108c** to form a continuous monocrystalline gallium nitride semiconductor layer **108**. It has been found that the dislocation densities in the underlying gallium nitride layer

104 generally do not propagate laterally with the same intensity as vertically. Thus, lateral gallium nitride layer **108b** can have a relatively low defect density, for example less that $10^4 cm^{-2}$. Accordingly, lateral gallium nitride layer **108b** may form device quality gallium nitride semiconductor material. Thus, as shown in Figure 1, microelectronic devices **110** may be formed in the lateral gallium nitride layer **108b**.

Referring now to Figures 2-5, methods of fabricating gallium nitride semiconductor structures according to the present invention will now be described. As shown in Figure 2, an underlying gallium nitride layer **104** is grown on a substrate **102**. The substrate **102** may include a 6H-SiC(0001) substrate **102a** and an aluminum nitride buffer layer **102b**. The gallium nitride layer **104** may be between 1.0 and 2.0μm thick, and may be grown at 1000°C on a high temperature (1100°C) aluminum nitride buffer layer **102b** that was deposited on 6H-SiC substrate **102a** in a cold wall vertical and inductively heated metalorganic vapor phase epitaxy system using triethylgallium at 26μmol/min, ammonia at 1500 sccm and 3000 sccm hydrogen diluent. Additional details of this growth technique may be found in a publication by T.W. Weeks et al. entitled *"GaN Thin Films Deposited Via Organometallic Vapor Phase Epitaxy on α(6H)-SiC(0001) Using High-Temperature Monocrystalline AlN Buffer Layers"*, Applied Physics Letters, Vol. 67, No. 3, July 17, 1995, pp. 401-403, the disclosure of which is hereby incorporated herein by reference. Other substrates, with or without buffer layers, may be used.

Still referring to Figure 2, the underlying gallium nitride layer **104** is masked with a mask **106** that includes an array of openings **107** therein. The mask may comprise silicon dioxide at thickness of 1000Å and may be deposited using low pressure chemical vapor deposition at 410°C. Other masking materials may be used. The mask may be patterned using standard photolithography techniques and etching in a buffered HF solution. In one embodiment, the openings **107** are 3μm-wide openings that extend in parallel at distances of between 3 and 40μm and that are oriented along the $<1\bar{1}00>$ direction on the underlying gallium nitride layer **104**. Prior to further processing, the structure may be dipped in a 50% buffered hydrochloric acid (HCl) solution to remove surface oxides from the underlying gallium nitride layer **104**.

Referring now to Figure 3, the underlying gallium nitride layer **104** is grown through the array of openings **107** to form vertical gallium nitride layer **108a** in the

openings. Growth of gallium nitride may be obtained at 1000-1100°C and 45 Torr. The precursors TEG at 13-39μmol/min and NH_3 at 1500 sccm may be used in combination with a 3000 sccm H_2 diluent. If gallium nitride alloys are formed, additional conventional precursors of aluminum or indium, for example, may also be used. As shown in Figure 3, the gallium nitride layer **108a** grows vertically to the top of the mask **106**.

It will be understood that underlying gallium nitride layer **104** may also be grown laterally without using a mask **106**, by appropriately controlling growth parameters and/or by appropriately patterning the underlying gallium nitride layer **104**. A patterned layer may be formed on the underlying gallium nitride layer after vertical growth or lateral growth, and need not function as a mask.

It will also be understood that lateral growth in two dimensions may be used to form an overgrown gallium nitride semiconductor layer. Specifically, mask **106** may be patterned to include an array of openings **107** that extend along two orthogonal directions such as $<1\bar{1}00>$ and $<11\bar{2}0>$. Thus, the openings can form a rectangle of orthogonal striped patterns. In this case, the ratio of the edges of the rectangle is preferably proportional to the ratio of the growth rates of the $\{11\bar{2}0\}$ and $\{1\bar{1}01\}$ facets, for example, in a ratio of 1.4:1.

Referring now to Figure 4, continued growth of the gallium nitride layer **108a** causes lateral overgrowth onto the mask **106**, to form lateral gallium nitride layer **108b**. Growth conditions for overgrowth may be maintained as was described in connection with Figure 3.

Referring now to Figure 5, lateral overgrowth is allowed to continue until the lateral growth fronts coalesce at interfaces **108c**, to form a continuous gallium nitride layer **108**. The total growth time may be approximately 60 minutes. As shown in Figure 1, microelectronic devices may then be formed in regions **108b**. Devices may also be formed in regions **108a** if desired.

Referring now to Figure 6, gallium nitride semiconductor structures according to second embodiments of the present invention are illustrated. The gallium nitride structures **200** include a substrate **102** as described above. An underlying gallium nitride layer **104** is also included on buffer layer **102b** opposite substrate **102a** as described above. A first mask such as a first silicon dioxide mask **106** is included on

the underlying gallium nitride layer **104**. The first mask **106** includes a first array of openings therein. Preferably, the first openings are first stripes that extend along the $<1\bar{1}00>$ direction of the underlying gallium nitride layer **104** as described above. A first vertical gallium nitride layer **108a** extends from the underlying gallium nitride layer **104** and through the first array of openings in the first mask **106** as described above. The gallium nitride semiconductor structure **200** also includes a first lateral gallium nitride layer **108b** that extends laterally from the first vertical gallium nitride layer **108a** onto the first mask **106** opposite the underlying gallium nitride layer **104** as described above.

Continuing with the description of Figure 6, a second mask such as a second silicon dioxide mask **206** is included on the first vertical gallium nitride layer **108a**. As shown, second mask **206** is laterally offset from first mask **106**. It will also be understood that second mask **206** may also extend onto first vertical gallium nitride layer **108b**. Preferably, second mask **206** covers all of first vertical gallium nitride layer **108b** such that defects in this layer do not propagate further. It will also be understood that the second mask **206** need not be symmetrically offset with respect to first mask **106**. The second mask **206** includes a second array of openings therein. The second openings are preferably oriented as described in connection with the first mask **106**. The second mask **206** also may be fabricated similar to first mask **106**.

Still continuing with the description of Figure 6, a second vertical gallium nitride layer **208a** extends from the first lateral gallium nitride layer **108a** and through the second array of openings in the second mask **206**. The second vertical gallium nitride layer **208a** may be formed similar to first vertical gallium nitride layer **108a**. The gallium nitride semiconductor structure **200** also includes a second lateral gallium nitride layer **208b** that extends laterally from the second vertical gallium nitride layer **208a** onto the second mask **206** opposite the first gallium nitride layer **108**. The second lateral gallium nitride layer **208b** may be formed using metalorganic vapor phase epitaxy as was described above.

As shown in Figure 6, the second lateral gallium nitride layer **208b** coalesces at second interfaces **208c**, to form a second continuous monocrystalline gallium nitride semiconductor layer **208**. It has been found that since the first lateral gallium nitride layer **108b** is used to grow second gallium nitride layer **208**, the second gallium nitride layer **208** including second vertical gallium nitride layer **208a** and

second lateral gallium nitride layer **208b**, can have a relatively low defect density, for example less than $10^4 cm^{-2}$. Accordingly, the entire gallium nitride layer **208** can form device quality gallium nitride semiconductor material. Thus, as shown in Figure 1, microelectronic devices **210** may be formed in both the second vertical gallium nitride layer **208a** and the second lateral gallium nitride layer **208b**, and may bridge these layers as well. By offsetting masks **106** and **206**, a continuous device quality gallium nitride layer may be obtained.

Referring now to Figures 7-14, methods of fabricating second embodiments of gallium nitride semiconductor structures according to the present invention will now be described. As shown in Figure 7, an underlying gallium nitride layer **104** is grown on a substrate **102** as was described in detail in connection with Figure 2. Still referring to Figure 7, the underlying gallium nitride layer **104** is masked with a first mask **106** that includes a first array of openings **107** therein as was described in connection with Figure 2.

Referring to Figure 8, the underlying gallium nitride layer **104** is grown through the first array of openings **107** to form first vertical gallium nitride layer **108a** in the first openings as was described in connection with Figure 3. Referring to Figure 9, continued growth of the first gallium nitride layer **108a** causes lateral overgrowth onto the first mask **106**, to form first lateral gallium nitride layer **108b**, as was described in connection with Figure 4. Referring now to Figure 10, lateral overgrowth is optionally allowed to continue until the lateral growth fronts coalesce at first interfaces **108c**, to form a first continuous gallium nitride layer **108**, as was described in connection with Figure 5.

Referring now to Figure 11, the first vertical gallium nitride layer **108a** is masked with a second mask **206** that includes a second array of openings **207** therein. The second mask may be fabricated as was described in connection with the first mask. The second mask may also be eliminated, as was described in connection with the first mask of Figure 3. The second mask may also be eliminated, as was described in connection with Figure 3. As already noted, the second mask **206** preferably covers the entire first vertical gallium nitride layer **108a**, so as to prevent defects therein from propagating vertically or laterally. In order to provide defect-free propagation, mask **206** may extend onto first lateral gallium nitride layer **108b** as well.

Referring now to Figure 12, the first lateral gallium nitride layer **108c** is grown vertically through the second array of openings **207**, to form second vertical gallium nitride layer **208a** in the second openings. Growth may be obtained as was described in connection with Figure 3.

Referring now to Figure 13, continued growth of the second gallium nitride layer **208a** causes lateral overgrowth onto the second mask **206**, to form second lateral gallium nitride layer **208b**. Lateral growth may be obtained as was described in connection with Figure 3.

Referring now to Figure 14, lateral overgrowth preferably continues until the lateral growth fronts coalesce at second interfaces **208c** to form a second continuous gallium nitride layer **208**. Total growth time may be approximately 60 minutes. Microelectronic devices may then be formed in regions **208a** and in regions **208b** as shown in Figure 6, because both of these regions are of relatively low defect density. Devices may bridge these regions as well, as shown. Accordingly, a continuous device quality gallium nitride layer **208** may be formed.

Additional discussion of the methods and structures of the present invention will now be provided. As described above, the openings **107** and **207** in the masks are preferably rectangular stripes that preferably extend along the $<11\bar{2}0>$ and/or $<1\bar{1}00>$ directions relative to the underlying gallium nitride layer **104**. Truncated triangular stripes having $(1\bar{1}01)$ slant facets and a narrow (0001) top facet may be obtained for mask openings **107** and **207** along the $<11\bar{2}0>$ direction. Rectangular stripes having a (0001) top facet, $(11\bar{2}0)$ vertical side faces and $(1\bar{1}01)$ slant facets may be grown along the $<1\bar{1}00>$ direction. For growth times up to 3 minutes, similar morphologies may be obtained regardless of orientation. The stripes develop into different shapes if the growth is continued.

The amount of lateral growth generally exhibits a strong dependence on stripe orientation. The lateral growth rate of the $<1\bar{1}00>$ oriented stripes is generally much faster than those along $<11\bar{2}0>$. Accordingly, it is most preferred to orient the openings **107** and **207** so that they extend along the $<1\bar{1}00>$ direction of the underlying gallium nitride layer **104**.

The different morphological development as a function of opening orientation appears to be related to the stability of the crystallographic planes in the gallium

nitride structure. Stripes oriented along $<11\bar{2}0>$ may have wide $(1\bar{1}00)$ slant facets and either a very narrow or no (0001) top facet depending on the growth conditions. This may be because $(1\bar{1}01)$ is the most stable plane in the gallium nitride wurtzite crystal structure, and the growth rate of this plane is lower than that of others. The $\{1\bar{1}01\}$ planes of the $<1\bar{1}00>$ oriented stripes may be wavy, which implies the existence of more than one Miller index. It appears that competitive growth of selected $\{1\bar{1}01\}$ planes occurs during the deposition which causes these planes to become unstable and which causes their growth rate to increase relative to that of the $(1\bar{1}01)$ of stripes oriented along $<11\bar{2}0>$.

The morphologies of the gallium nitride layers selectively grown on openings oriented along $<1\bar{1}00>$ are also generally a strong function of the growth temperatures. Layers grown at 1000°C may possess a truncated triangular shape. This morphology may gradually change to a rectangular cross-section as the growth temperature is increased. This shape change may occur as a result of the increase in the diffusion coefficient and therefore the flux of the gallium species along the (0001) top plane onto the $\{1\bar{1}01\}$ planes with an increase in growth temperature. This may result in a decrease in the growth rate of the (0001) plane and an increase in that of the $\{1\bar{1}01\}$. This phenomenon has also been observed in the selective growth of gallium arsenide on silicon dioxide. Accordingly, temperatures of 1100°C appear to be most preferred.

The morphological development of the gallium nitride regions also appears to depend on the flow rate of the TEG. An increase in the supply of TEG generally increases the growth rate of the stripes in both the lateral and the vertical directions. However, the lateral/vertical growth rate ratio decrease from 1.7 at the TEG flow rate of 13μmol/min to 0.86 at 39μmol.min. This increased influence on growth rate along <0001> relative to that of $<11\bar{2}0>$ with TEG flow rate may be related to the type of reactor employed, wherein the reactant gases flow vertically and perpendicular to the substrate. The considerable increase in the concentration of the gallium species on the surface may sufficiently impede their diffusion to the $\{1\bar{1}01\}$ planes such that chemisorption and gallium nitride growth occur more readily on the (0001) plane.

Continuous 2μm thick gallium nitride layers **108** and **208** may be obtained using 3μm wide stripe openings **107** and **207** spaced 7μm apart and oriented along $<1\bar{1}00>$, at 1100°C and a TEG flow rate of 26μmol/min. The overgrown gallium nitride layers **108b** and **208b** may include subsurface voids that form when two growth fronts coalesce. These voids may occur most often using lateral growth conditions wherein rectangular stripes having vertical $\{11\bar{2}0\}$ side facets developed.

The coalesced gallium nitride layers **108** and **208** may have a microscopically flat and pit-free surface. The surfaces of the laterally grown gallium nitride layers may include a terrace structure having an average step height of 0.32nm. This terrace structure may be related to the laterally grown gallium nitride, because it is generally not included in much larger area films grown only on aluminum nitride buffer layers. The average RMS roughness values may be similar to the values obtained for the underlying gallium nitride layers **104**.

Threading dislocations, originating from the interface between the gallium nitride underlayer **104** and the buffer layer **102b**, appear to propagate to the top surface of the first vertical gallium nitride layer **108a** within the first openings **107** of the first mask **106**. The dislocation density within these regions is approximately $10^9 cm^{-2}$. By contrast, threading dislocations do not appear to readily propagate into the first overgrown regions **108b**. Rather, the first overgrown gallium nitride regions **108b** contain only a few dislocations. These few dislocations may be formed parallel to the (0001) plane via the extension of the vertical threading dislocations after a 90° bend in the regrown region. These dislocations do not appear to propagate to the top surface of the first overgrown GaN layer. Since both the second vertical gallium nitride layer **208a** and the second lateral gallium nitride layer **208b** propagate from the low defect first overgrown gallium nitride layer **108b**, the entire layer **208** can have low defect density.

As described, the formation mechanism of the selectively grown gallium nitride layer is lateral epitaxy. The two main stages of this mechanism are vertical growth and lateral growth. During vertical growth, the deposited gallium nitride grows selectively within the mask openings **107** and **207** more rapidly than it grows on the masks **106** and **206**, apparently due to the much higher sticking coefficient, s, of the gallium atoms on the gallium nitride surface (s=1) compared to on the mask (s~1). Since the SiO_2 bond strength is 799.6 kJ/mole and much higher than that of Si-

N (439 kJ/mole), Ga-N (103 kJ/mole), and Ga-O (353.6 kJ/mole), Ga or N atoms should not readily bond to the mask surface in numbers and for a time sufficient to cause gallium nitride nuclei to form. They would either evaporate or diffuse along the mask surface to the openings **107** or **207** in the masks or to the vertical gallium nitride surfaces **108a** or **208a** which have emerged. During lateral growth, the gallium nitride grows simultaneously both vertically and laterally over the mask from the material which emerges over the openings.

Surface diffusion of gallium and nitrogen on the masks may play a minor role in gallium nitride selective growth. The major source of material appears to be derived from the gas phase. This may be demonstrated by the fact that an increase in the TEG flow rate causes the growth rate of the (0001) top facets to develop faster than the $(1\bar{1}01)$ side facets and thus controls the lateral growth.

The laterally grown gallium nitride layers **108b** and **208b** bond to the underlying masks **106** and **206** sufficiently strongly so that they generally do not break away on cooling. However, lateral cracking within the SiO_2 may take place due to thermal stresses generated on cooling. The viscosity (ρ) of the SiO_2 at 1050°C is about $10^{15.5}$ poise which is one order of magnitude greater than the strain point (about $10^{14.5}$ poise) where stress relief in a bulk amorphous material occurs within approximately six hours. Thus, the SiO_2 mask may provide limited compliance on cooling. As the atomic arrangement on the amorphous SiO_2 surface is quite different from that on the GaN surface, chemical bonding may occur only when appropriate pairs of atoms are in close proximity. Extremely small relaxations of the silicon and oxygen and gallium and nitrogen atoms on the respective surfaces and/or within the bulk of the SiO_2 may accommodate the gallium nitride and cause it to bond to the oxide.

Accordingly, regions of lateral epitaxial overgrowth through mask openings from an underlying gallium nitride layer may be achieved via MOVPE. The growth may depend strongly on the opening orientation, growth temperature and TEG flow rate. Coalescence of overgrown gallium nitride regions to form regions with both extremely low densities of dislocations and smooth and pit-free surfaces may be achieved through 3μm wide mask openings spaced 7μm apart and extending along the $<1\bar{1}00>$ direction, at 1100°C and a TEG flow rate of 26μmol/min. The lateral

overgrowth of gallium nitride via MOVPE may be used to obtain low defect density continuous gallium nitride layers for microelectronic devices.

In the drawings and specification, there have been disclosed typical preferred embodiments of the invention and, although specific terms are employed, they are used in a generic and descriptive sense only and not for purposes of limitation, the scope of the invention being set forth in the following claims.

That which is claimed

1. A method of fabricating a gallium nitride semiconductor layer that comprises the steps of masking an underlying gallium nitride layer (104) with a mask (106) that includes an array of openings therein and growing the underlying gallium nitride layer through the array of openings and onto the mask to thereby form a first overgrown gallium nitride semiconductor layer (108), characterized by the additional steps of:

masking the first overgrown gallium nitride layer (108) with a second mask (206) that includes a second array of openings therein, the second array of openings being laterally offset from the first array of openings; and

growing the first overgrown gallium nitride layer through the second array of openings and onto the second mask, to thereby form a second overgrown gallium nitride semiconductor layer (208).

2. A method according to Claim 1 wherein the growing step comprises the step of growing the underlying gallium nitride layer through the array of openings and onto the mask until the grown gallium nitride layer coalesces on the mask to form a first continuous overgrown monocrystalline gallium nitride semiconductor layer.

3. A method according to Claim 1 wherein the growing step comprises the step of growing the underlying gallium nitride layer using metalorganic vapor phase epitaxy.

4. A method according to Claim 1 wherein the masking step is preceded by the step of forming the underlying gallium nitride layer on a substrate (102).

5. A method according to Claim 4 wherein the forming step comprises the steps of:

forming a buffer layer (102b) on a substrate (102a); and

forming the underlying gallium nitride layer on the buffer layer opposite the substrate.

6. A method according to Claim 1 wherein the masking step comprises the step of:

masking the underlying gallium nitride layer with a mask that includes an array of stripe openings therein, the stripe openings extending along a $<1\bar{1}00>$ direction of the underlying gallium nitride layer.

7. A method according to Claim 1 wherein the underlying gallium nitride layer includes a defect density, and wherein the step of growing the underlying gallium nitride layer through the array of openings and onto the mask to thereby form an overgrown gallium nitride semiconductor layer comprises the steps of:

vertically growing the underlying gallium nitride layer through the array of openings while propagating the defect density; and

laterally growing the underlying gallium nitride layer from the array of openings onto the mask to thereby form an overgrown gallium nitride semiconductor layer of lower defect density than the defect density.

8. A method according to Claim 1 wherein the growing step comprises the step of growing the underlying gallium nitride layer using metalorganic vapor phase epitaxy of triethylgallium at 13-39μmol/min and ammonia at 1500 sccm at a temperature of 1000°C-1100°C.

9. A method according to Claim 6 wherein the growing step comprises the step of growing the underlying gallium nitride layer using metalorganic vapor phase epitaxy of triethylgallium at 26μmol/min and ammonia at 1500 sccm at a temperature of 1100°C.

10. A method according to Claim 1 wherein the step of growing the first overgrown gallium nitride layer is followed by the step of forming microelectronic devices (210) in the second overgrown gallium nitride semiconductor layer.

11. A method according to Claim 1 wherein the step of growing the first overgrown gallium nitride layer comprises the step of growing the first overgrown gallium nitride layer through the second array of openings and onto the second mask

until the second overgrown gallium nitride layer coalesces on the second mask to form a continuous overgrown monocrystalline gallium nitride semiconductor layer.

12. A method according to Claim 1 wherein the growing steps comprise the steps of growing the underlying gallium nitride layer and growing the first overgrown gallium nitride layer using metalorganic vapor phase epitaxy.

13. A method according to Claim 1 wherein the first and second masking steps comprise the steps of:

masking the underlying gallium nitride layer and the first overgrown gallium nitride layer with a first mask and a second mask respectively, that include respective first and second arrays of stripe openings therein, the stripe openings extending along a $<1\bar{1}00>$ direction of the underlying gallium nitride layer.

14. A method according to Claim 1 wherein the underlying gallium nitride layer includes a defect density, and wherein the step of growing the underlying gallium nitride layer through the first array of openings and onto the mask to thereby form a first overgrown gallium nitride semiconductor layer comprises the steps of:

vertically growing the underlying gallium nitride layer through the first array of openings while propagating the defect density; and

laterally growing the underlying gallium nitride layer from the first array of openings onto the first mask to thereby form a first overgrown gallium nitride semiconductor layer of lower defect density than the defect density.

15. A method according to Claim 14 wherein the step of growing the first overgrown gallium nitride layer comprises the steps of:

vertically growing the first overgrown gallium nitride semiconductor layer through the second array of openings; and

laterally growing the first overgrown gallium nitride semiconductor layer from the second array of openings onto the second mask, to thereby form a second overgrown gallium nitride semiconductor layer of lower defect density than the defect density.

16. A method according to Claim 1 wherein the underlying gallium nitride layer includes a defect density, and wherein the second overgrown gallium nitride semiconductor layer is of lower defect density than the defect density.

17. A method according to Claim 1 wherein the growing steps comprise the steps of growing the underlying gallium nitride layer and growing the first overgrown gallium nitride layer using metalorganic vapor phase epitaxy of triethylgallium at 13-39μmol/min and ammonia at 1500 sccm at a temperature of 1000°C-1100°C.

18. A method according to Claim 13 wherein the steps of growing the underlying gallium nitride layer and growing the first overgrown gallium nitride layer comprise the steps of growing the underlying gallium nitride layer and the first overgrown gallium nitride layer using metalorganic vapor phase epitaxy of triethylgallium at 26μmol/min and ammonia at 1500 sccm at a temperature of 1100°C.

19. A method of fabricating a gallium nitride semiconductor layer that comprises the step of laterally growing an underlying gallium nitride layer (104) relative to the underlying gallium nitride layer (104) to thereby form a first laterally grown gallium nitride semiconductor layer(108), characterized by the additional step of:

laterally growing the first laterally grown gallium nitride layer (108) relative to the underlying gallium nitride layer (104), to thereby form a second laterally grown gallium nitride semiconductor layer (208).

20. A method according to Claim 19 wherein the step of laterally growing the first laterally grown gallium nitride layer is followed by the step of forming microelectronic devices (210) in the second laterally grown gallium nitride semiconductor layer (208).

21. A method according to Claim 19 wherein the step of laterally growing the first laterally grown gallium nitride layer comprises the step of laterally growing the first laterally grown gallium nitride layer until the second laterally grown gallium

nitride layer coalesces to form a continuous laterally grown monocrystalline gallium nitride semiconductor layer.

22. A method according to Claim 19 wherein the laterally growing steps comprise the steps of laterally growing the underlying gallium nitride layer and laterally growing the first laterally grown gallium nitride layer using metalorganic vapor phase epitaxy.

23. A method according to Claim 19 wherein the step of laterally growing the first laterally grown gallium nitride layer comprises the step of laterally overgrowing the first laterally grown gallium nitride layer.

24. A method according to Claim 19 wherein the underlying gallium nitride layer includes a defect density, and wherein the step of laterally growing the first laterally grown gallium nitride layer comprises the step of:

laterally growing the first laterally grown gallium nitride semiconductor layer, to thereby form a second laterally grown gallium nitride semiconductor layer of lower defect density than the defect density.

25. A gallium nitride semiconductor structure comprising an underlying gallium nitride layer (104), a first patterned layer (106) that includes a first array of openings therein on the underlying gallium nitride layer, a first vertical gallium nitride layer (108a) that extends from the underlying gallium nitride layer and through the first array of openings, and a first lateral gallium nitride layer (108b) that extends from the first vertical gallium nitride layer onto the first patterned layer opposite the underlying gallium nitride layer, characterized by:

a second patterned layer (206) that includes a second array of openings therein, on the first lateral gallium nitride layer, the second array of openings being laterally offset from the first array of openings;

a second vertical gallium nitride layer (208a) that extends from the first lateral gallium nitride layer and through the second array of openings; and

a second lateral gallium nitride layer (208b) that extends from the second vertical gallium nitride layer onto the second patterned layer opposite the first lateral gallium nitride layer.

26. A structure according to Claim 25 wherein the first lateral gallium nitride layer is a first continuous monocrystalline gallium nitride semiconductor layer.

27. A structure according to Claim 25 further comprising a substrate (102a), and wherein the underlying gallium nitride layer is on the substrate.

28. A structure according to Claim 27 further comprising a buffer layer (102b) between the substrate and the underlying gallium nitride layer.

29. A structure according to Claim 25 wherein the first patterned layer includes an array of openings therein, the openings extending along a $<1\bar{1}00>$ direction of the underlying gallium nitride layer.

30. A structure according to Claim 25 wherein the underlying gallium nitride layer includes a defect density, wherein the first vertical gallium nitride layer includes the defect density, and wherein the first lateral gallium nitride semiconductor layer is of lower defect density than the defect density.

31. A structure according to Claim 25 further comprising:

a plurality of microelectronic devices (210) in the second lateral gallium nitride layer.

32. A structure according to Claim 25 wherein the second lateral gallium nitride layer is a continuous monocrystalline gallium nitride semiconductor layer.

33. A structure according to Claim 25 wherein the first and second arrays of openings extend along a $<1\bar{1}00>$ direction of the underlying gallium nitride layer.

34. A structure according to Claim 25 wherein the underlying gallium nitride layer includes a defect density and wherein the second vertical gallium nitride layer and the second lateral gallium nitride semiconductor layer are of lower defect density than the defect density.

35. A continuous monocrystalline gallium nitride layer (208) on an underlying gallium nitride layer (104) having a defect density, characterized by:

the continuous monocrystalline gallium nitride layer (208) having lower defect density throughout the continuous monocrystalline gallium nitride layer, than the defect density of the underlying gallium nitride layer (104).

36. A layer according to Claim 35 wherein the defect density is at least $10^8 cm^{-2}$ and wherein the lower defect density is less than $10^4 cm^{-2}$.

37. A gallium nitride semiconductor structure comprising an underlying gallium nitride layer (104) and a first lateral gallium nitride layer (108b) that extends from the underlying gallium nitride layer, characterized by:

a second lateral gallium nitride layer (208b) that extends from the first lateral gallium nitride layer; and

a plurality of microelectronic devices (210) in the second lateral gallium nitride layer.

38. A structure according to Claim 37 wherein the second lateral gallium nitride layer is a continuous monocrystalline gallium nitride semiconductor layer.

39. A structure according to Claim 37 further comprising a substrate (102), and wherein the underlying gallium nitride layer is on the substrate.

40. A structure according to Claim 37 wherein the underlying gallium nitride layer includes a defect density and wherein the second lateral gallium nitride semiconductor layer is of lower defect density than the defect density.

41. A structure according to Claim 37 further comprising:

a first vertical gallium nitride layer (108a) between the underlying gallium nitride layer and the first lateral gallium nitride layer; and

a second vertical gallium nitride layer (208a) between the first lateral gallium nitride layer and the second lateral gallium nitride layer.

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FIG. 1

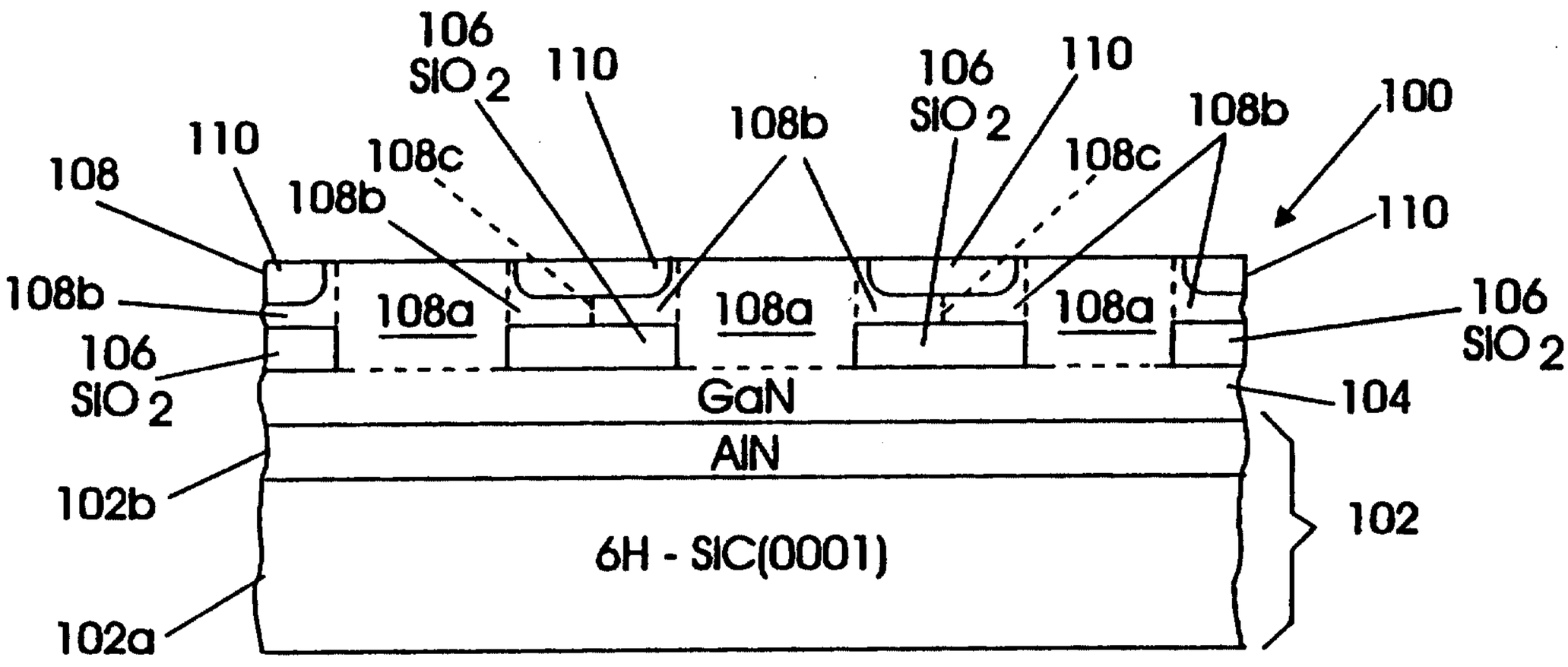
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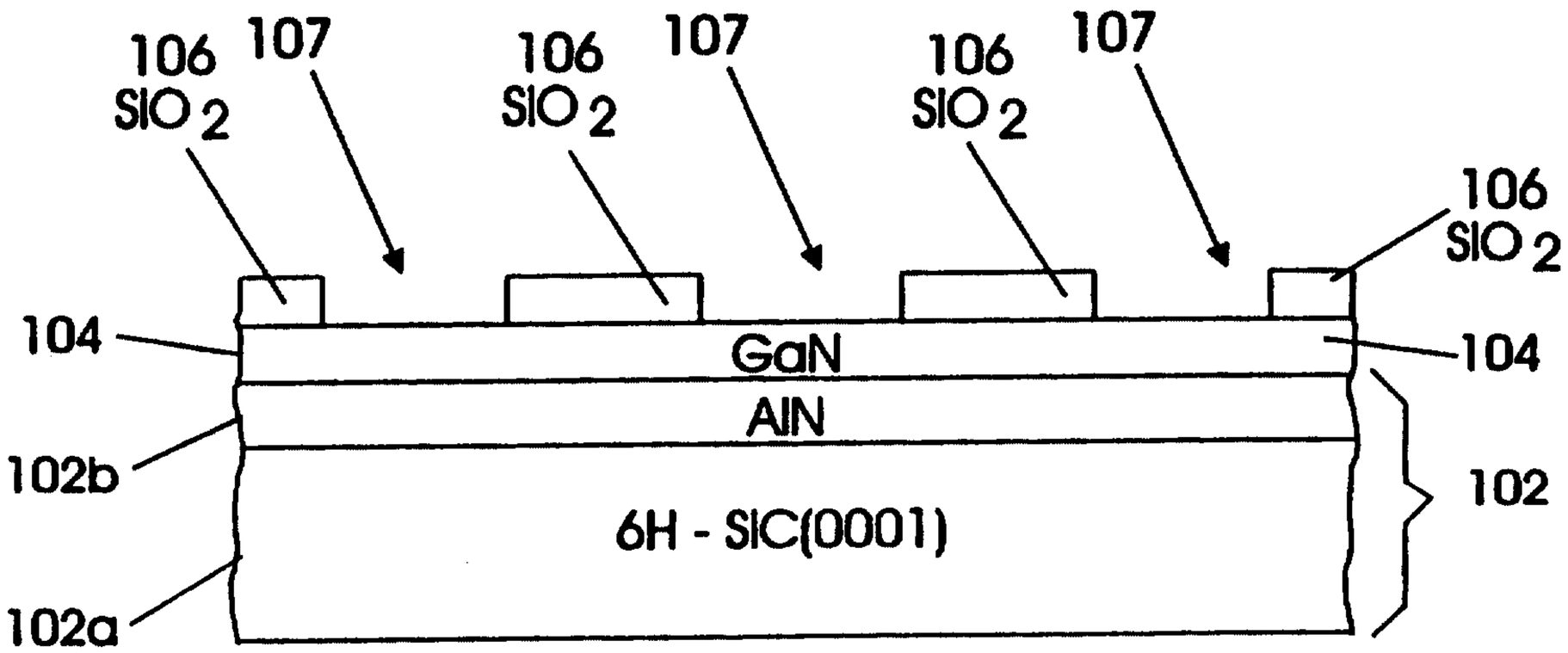
FIG. 2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102a

FIG. 3

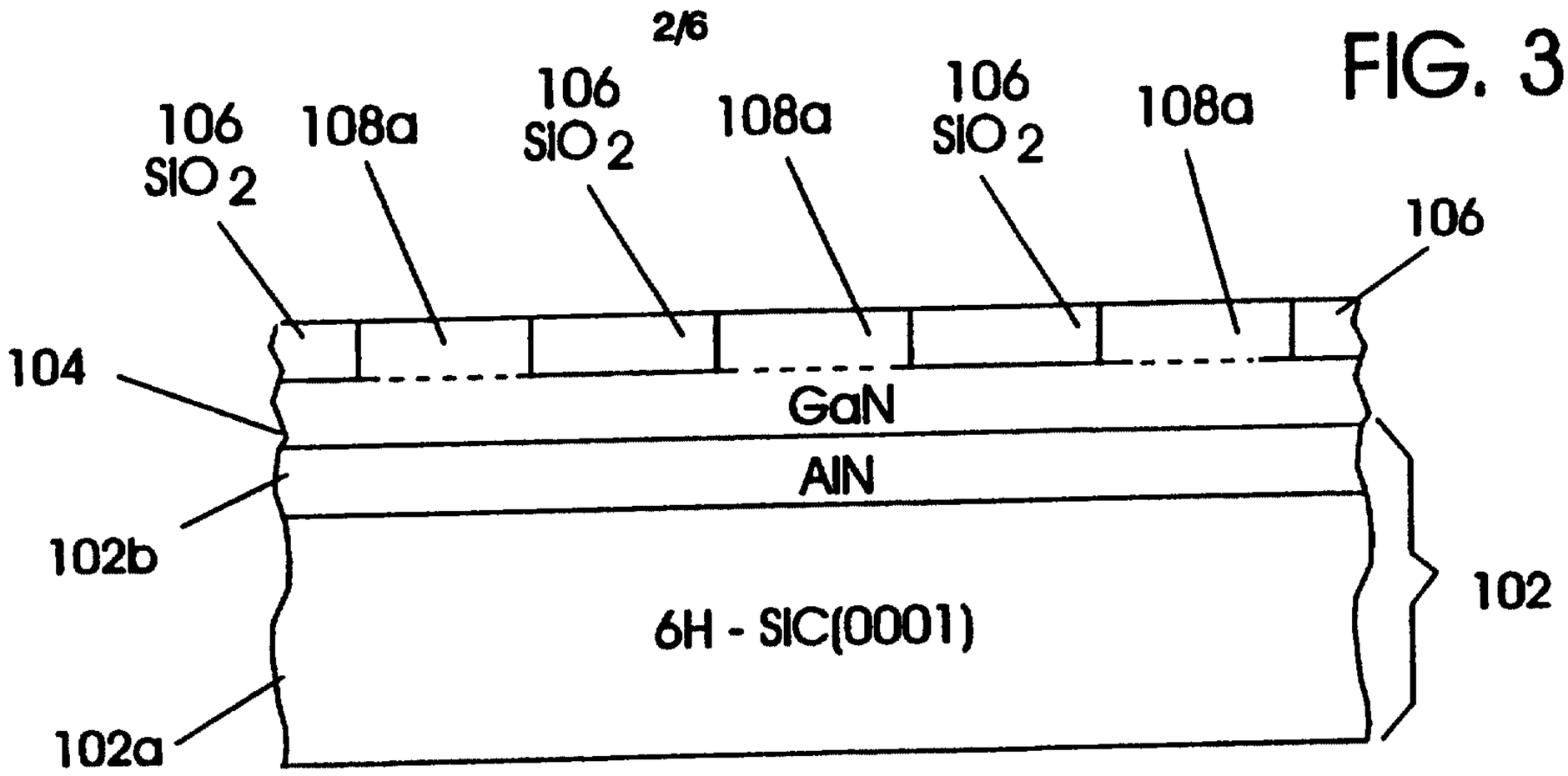


FIG. 4

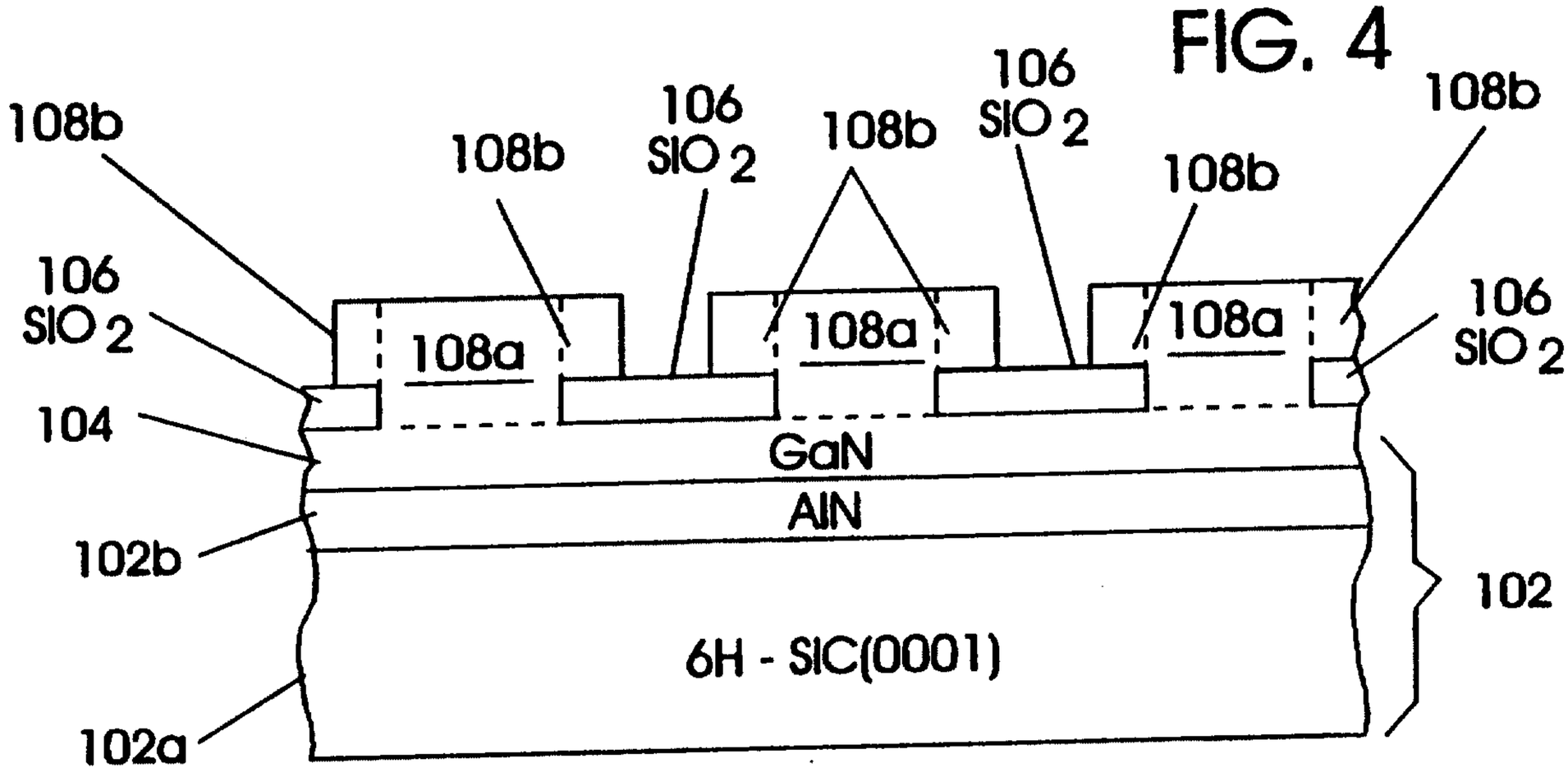


FIG. 5

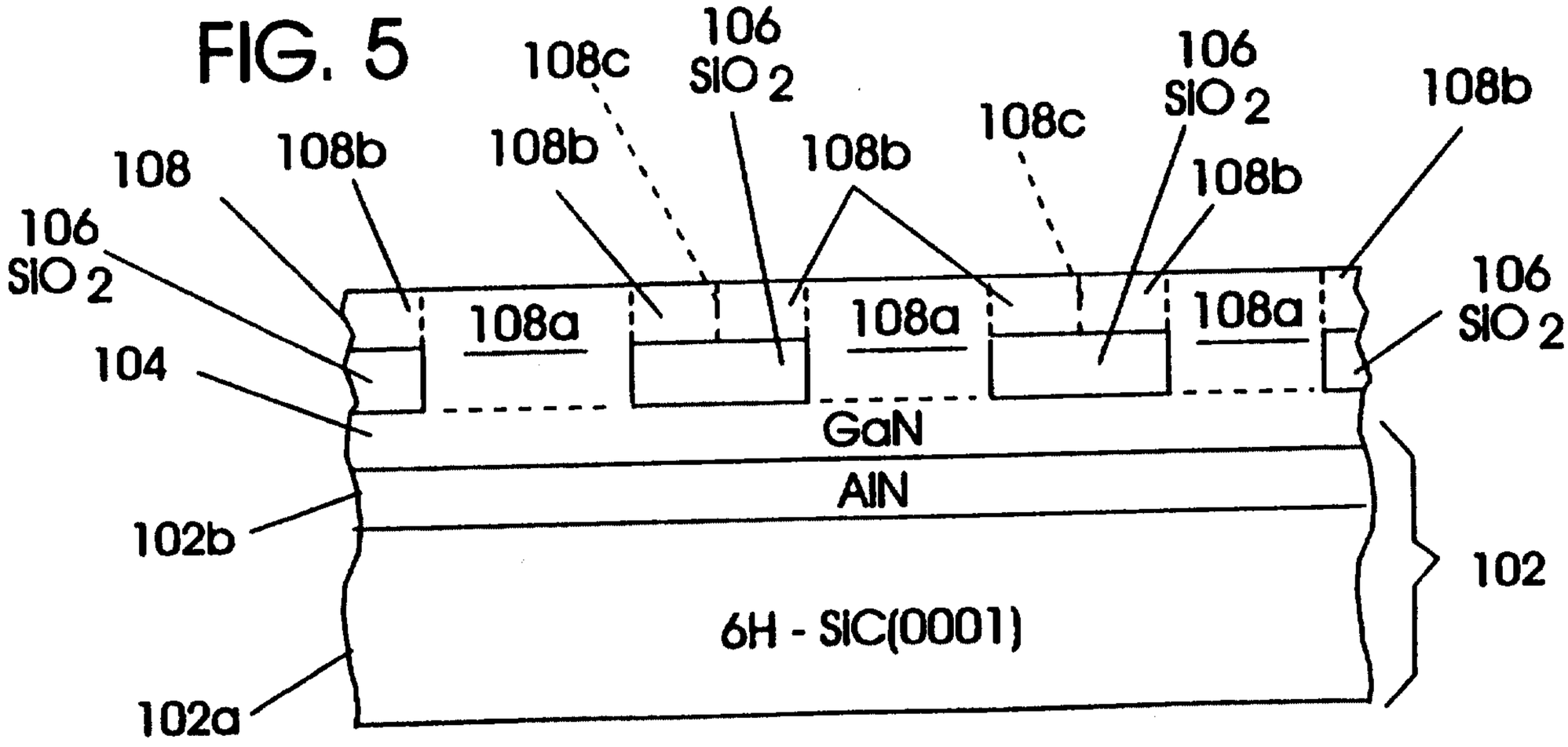
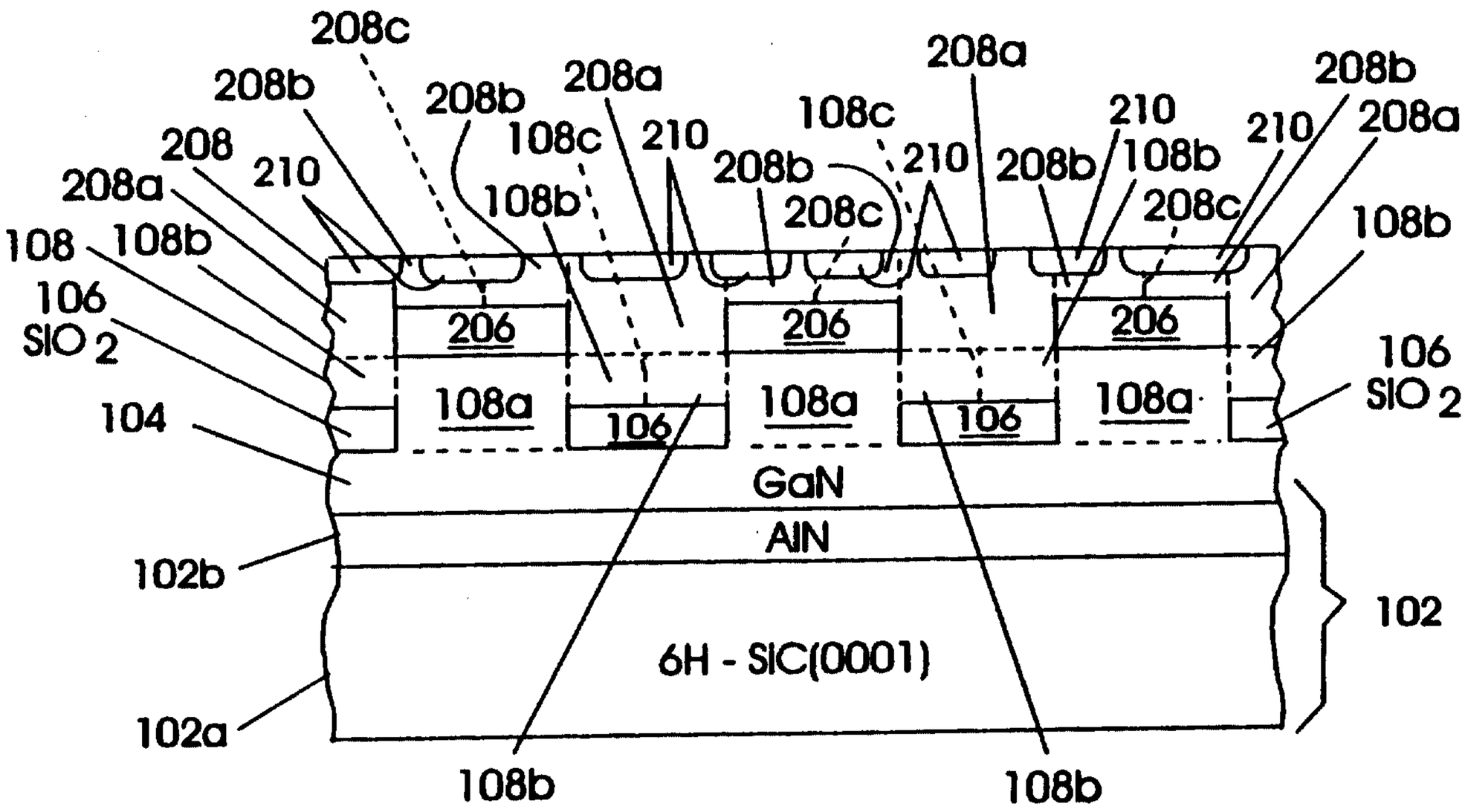


FIG. 6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SiO 2
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AlN
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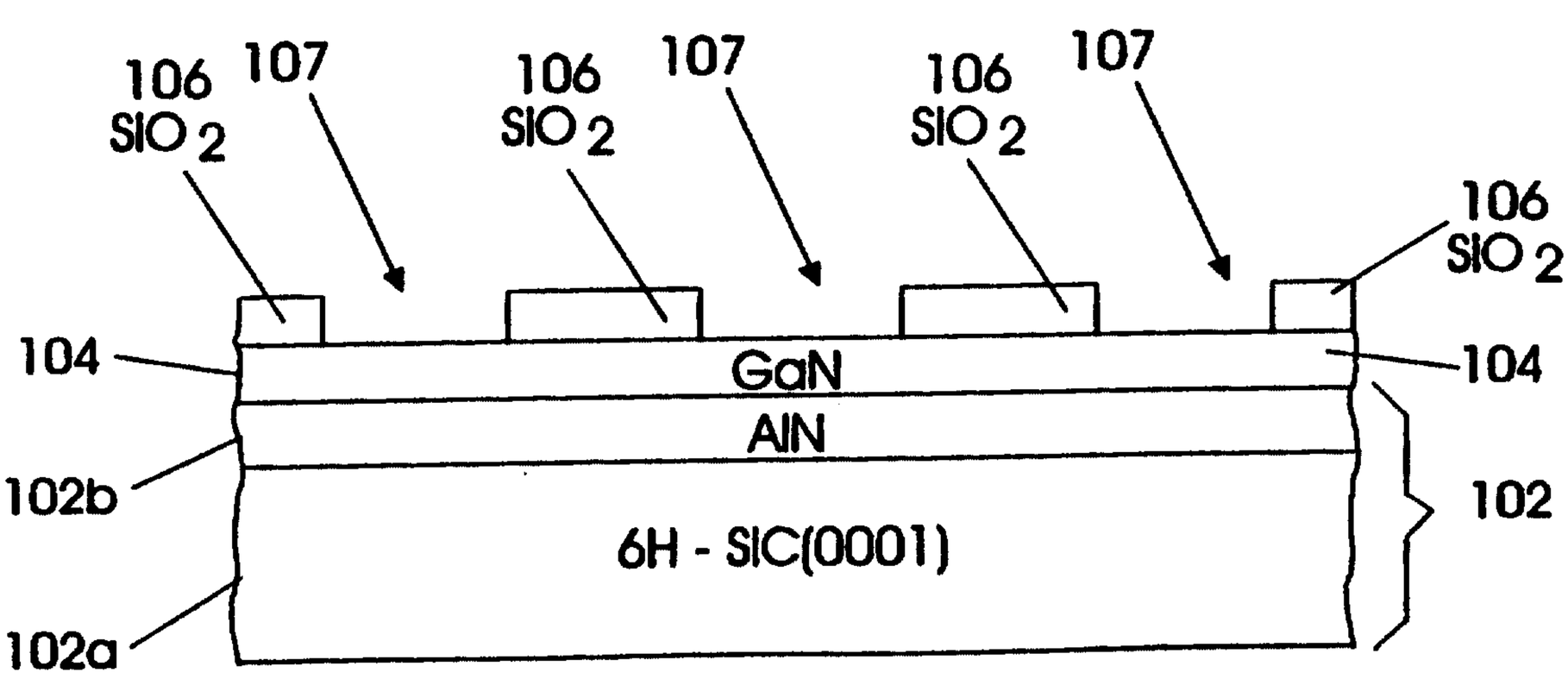
6H - SiC(0001)
102a
108b
108b

FIG. 7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6H - SiC(0001)
102a

FIG. 8

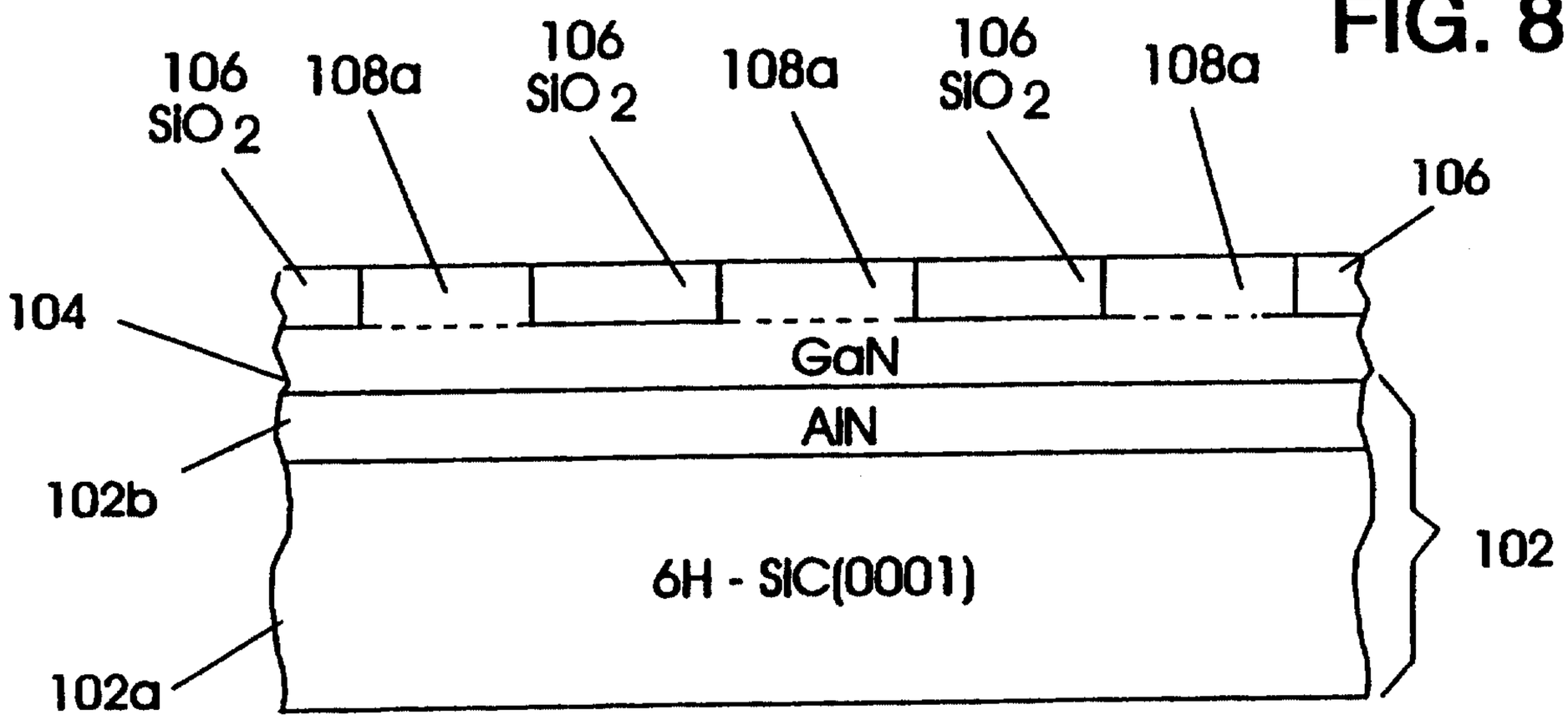


FIG. 9

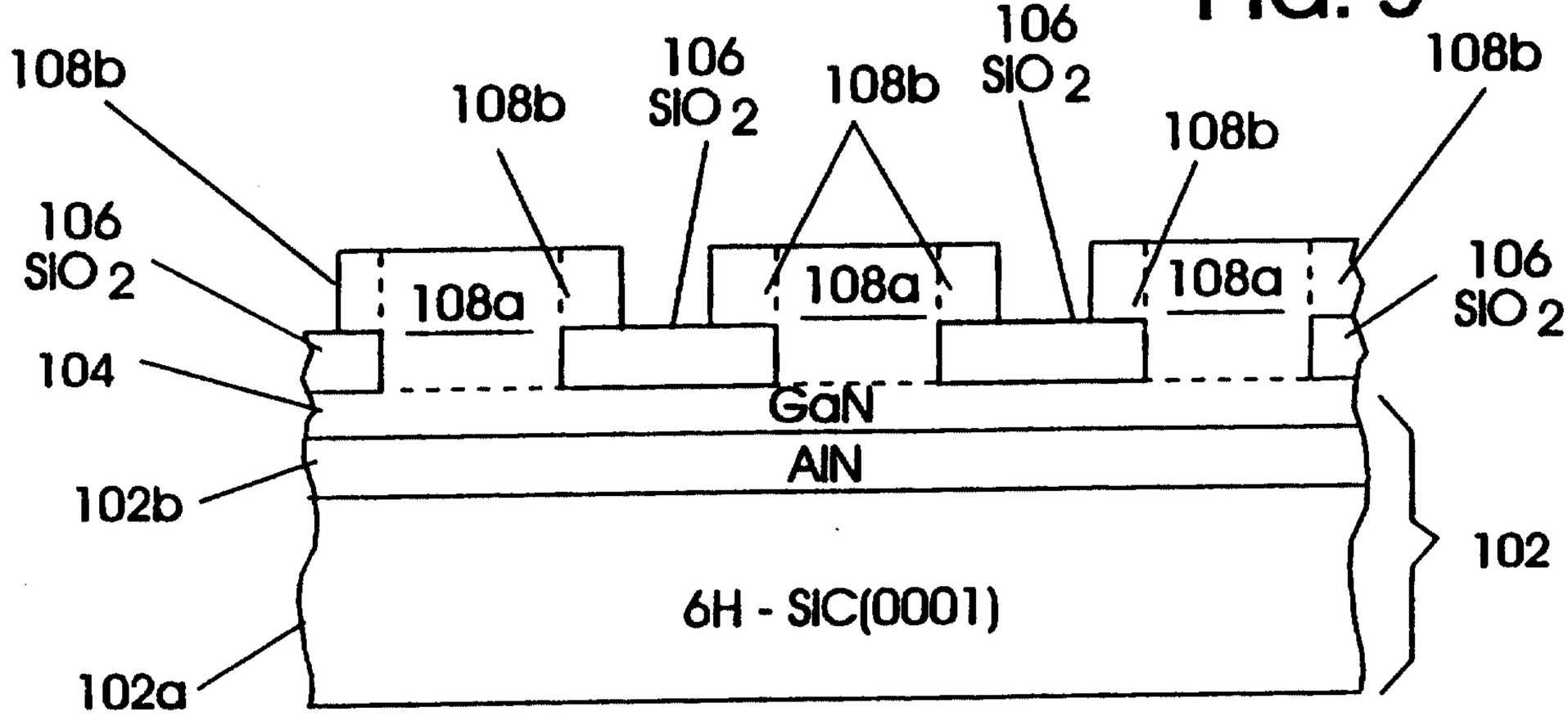


FIG. 10

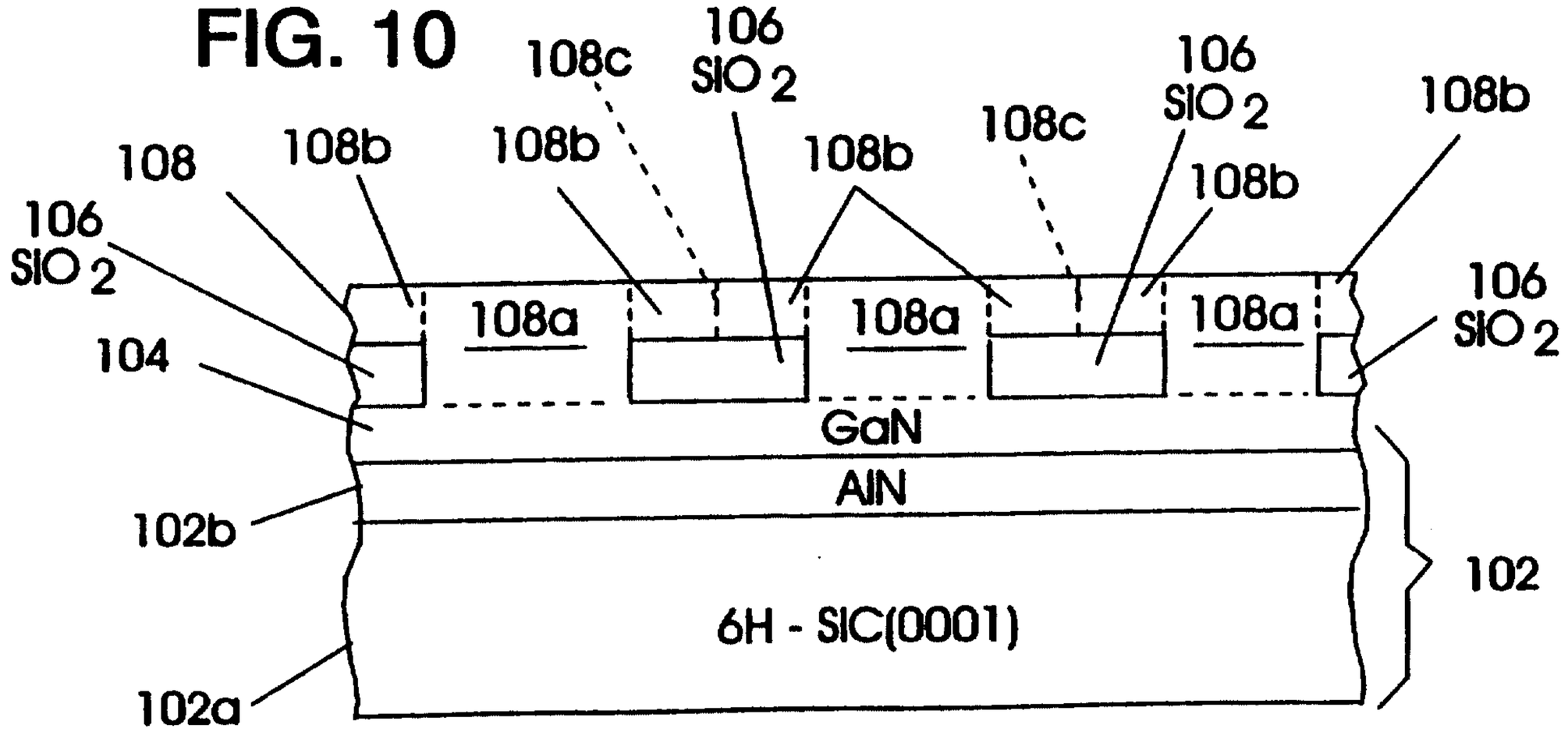
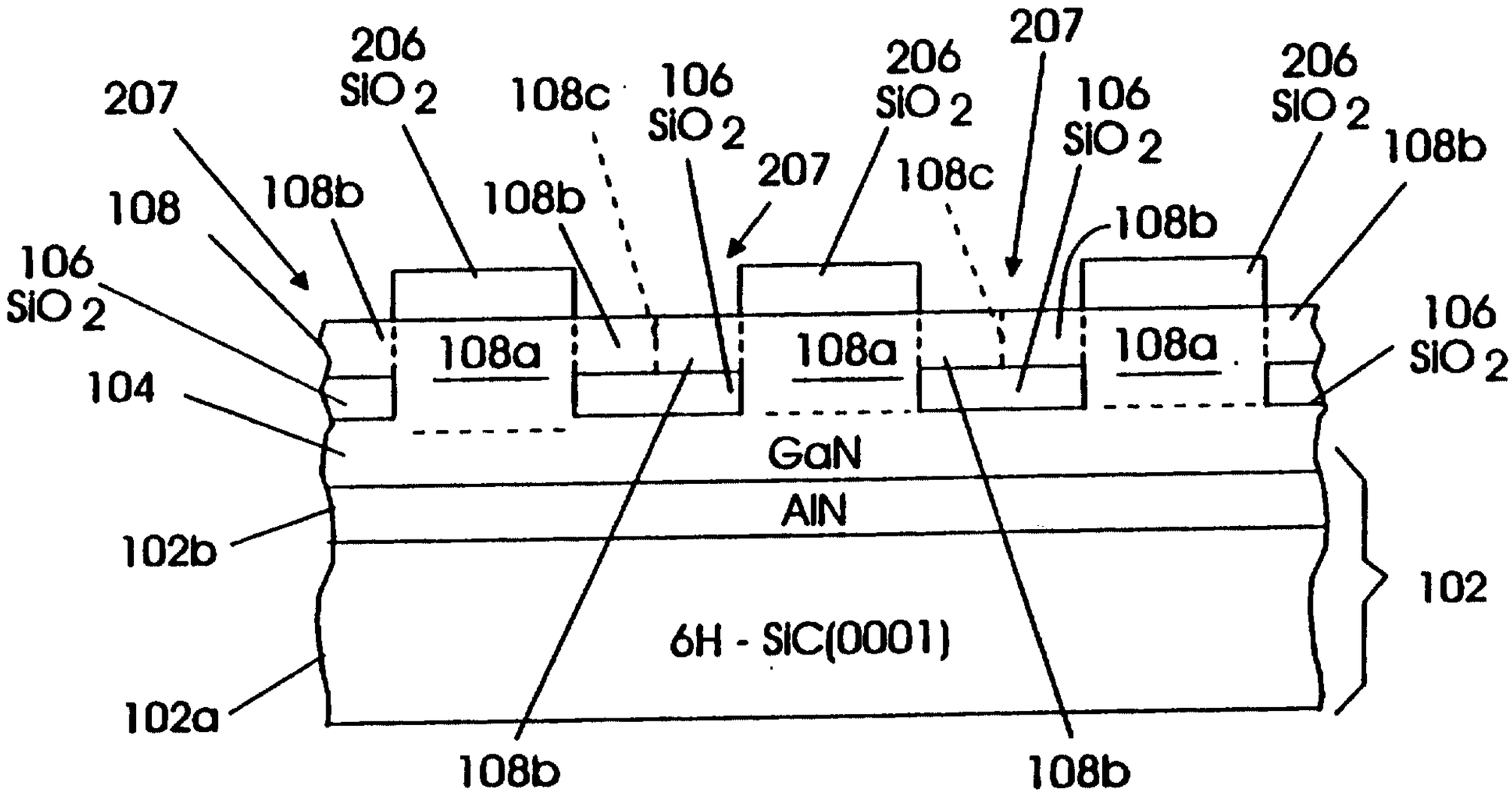


FIG. 11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108b
108b
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108c
106
SiO 2
108b
106
SiO 2
108a
108a
108a
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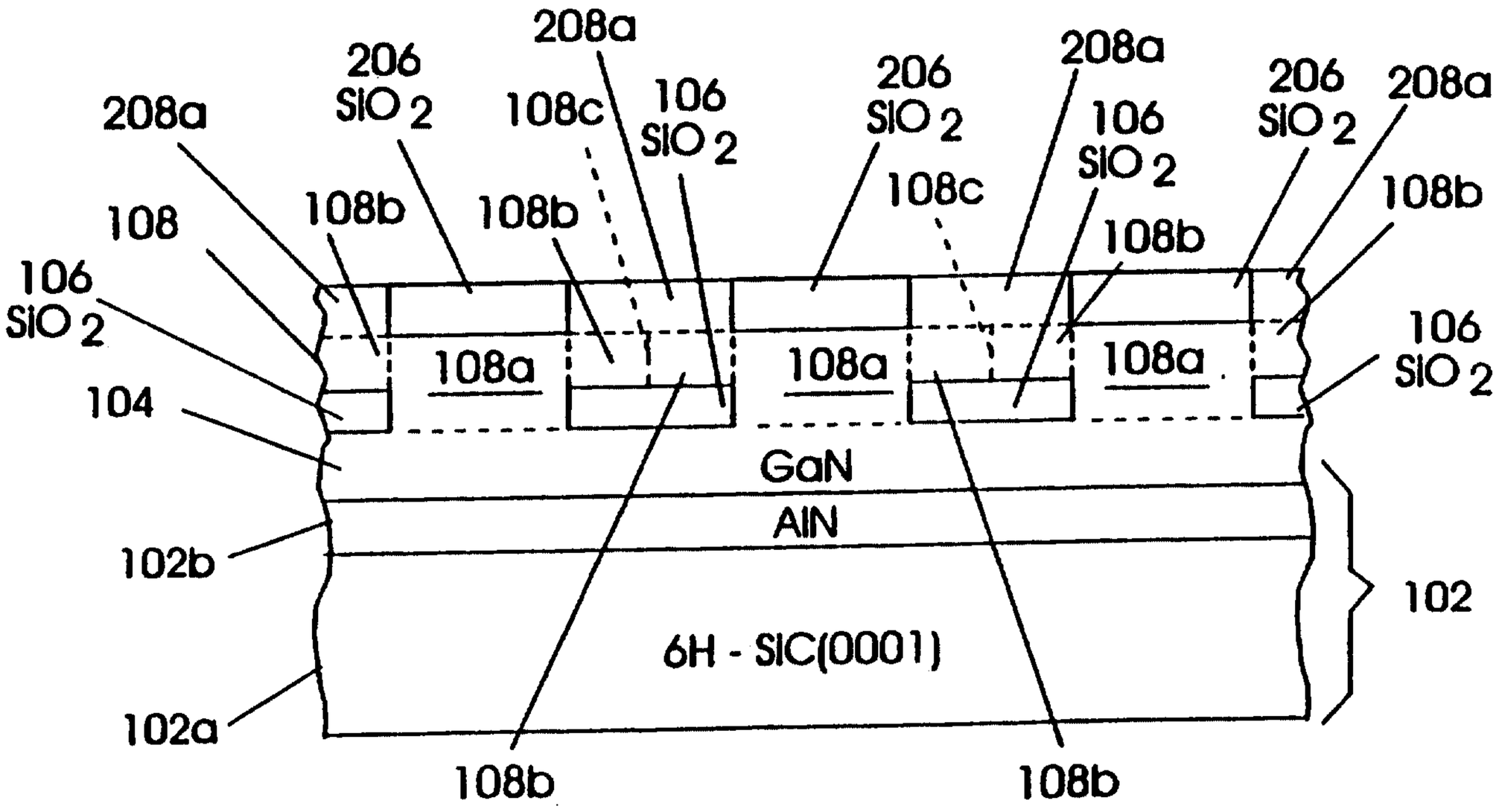
GaN
AlN
102b
102
6H - SiC(0001)
102a
108b
108b

FIG. 12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106
SiO 2
108b
108b
106
SiO 2
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AlN
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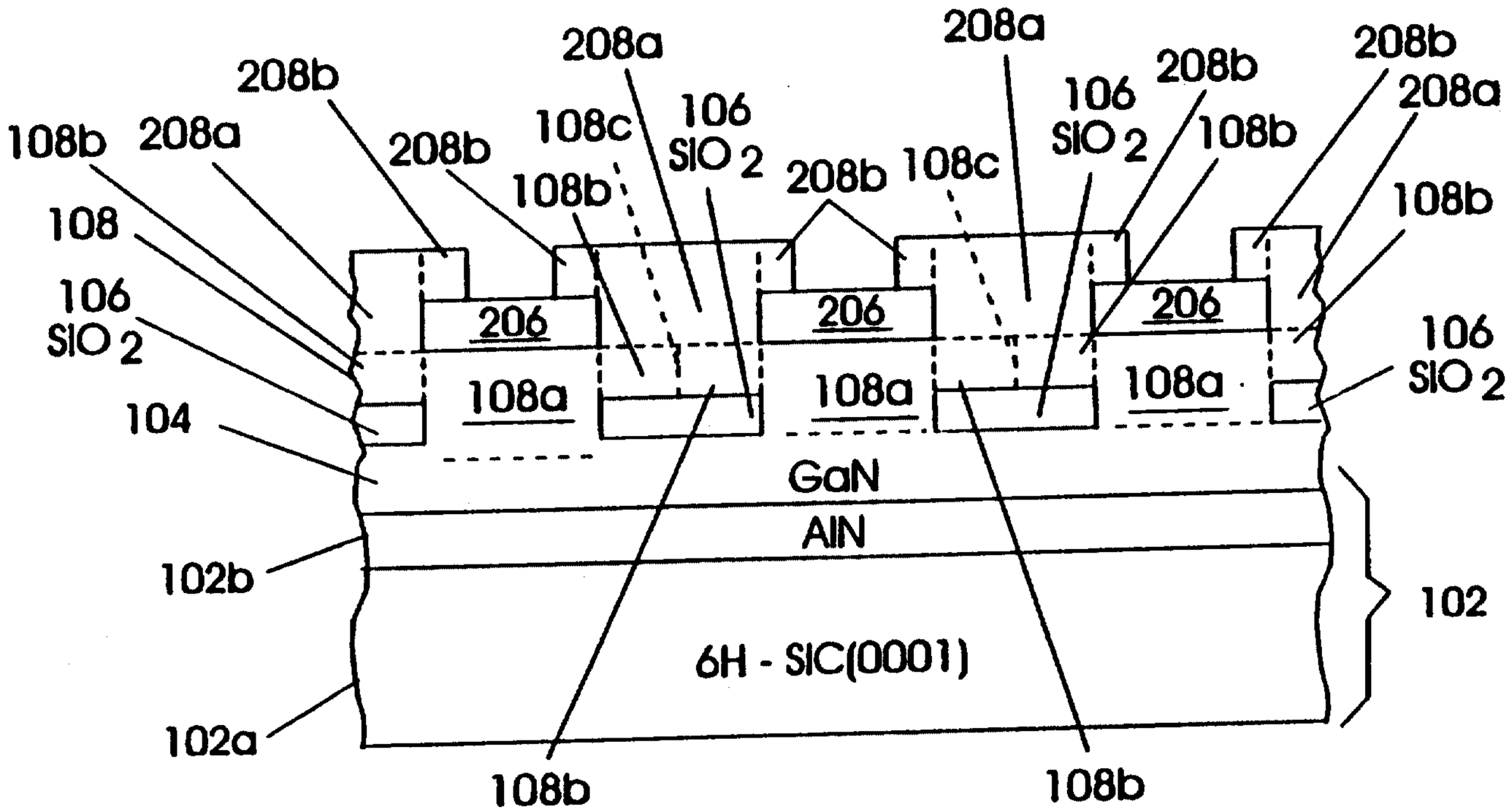
102
6H - SiC(0001)
102a
108b
108b

FIG. 13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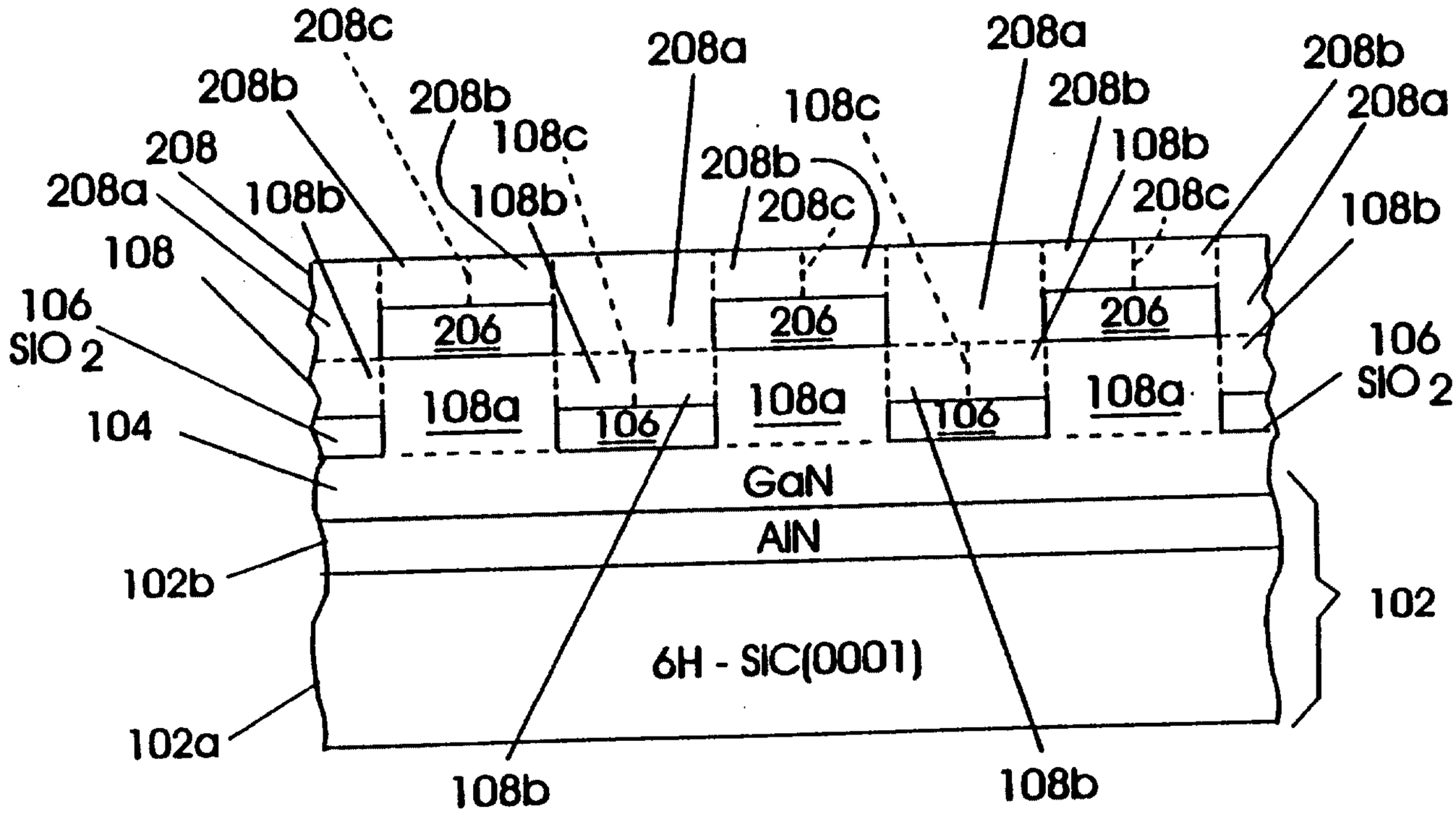
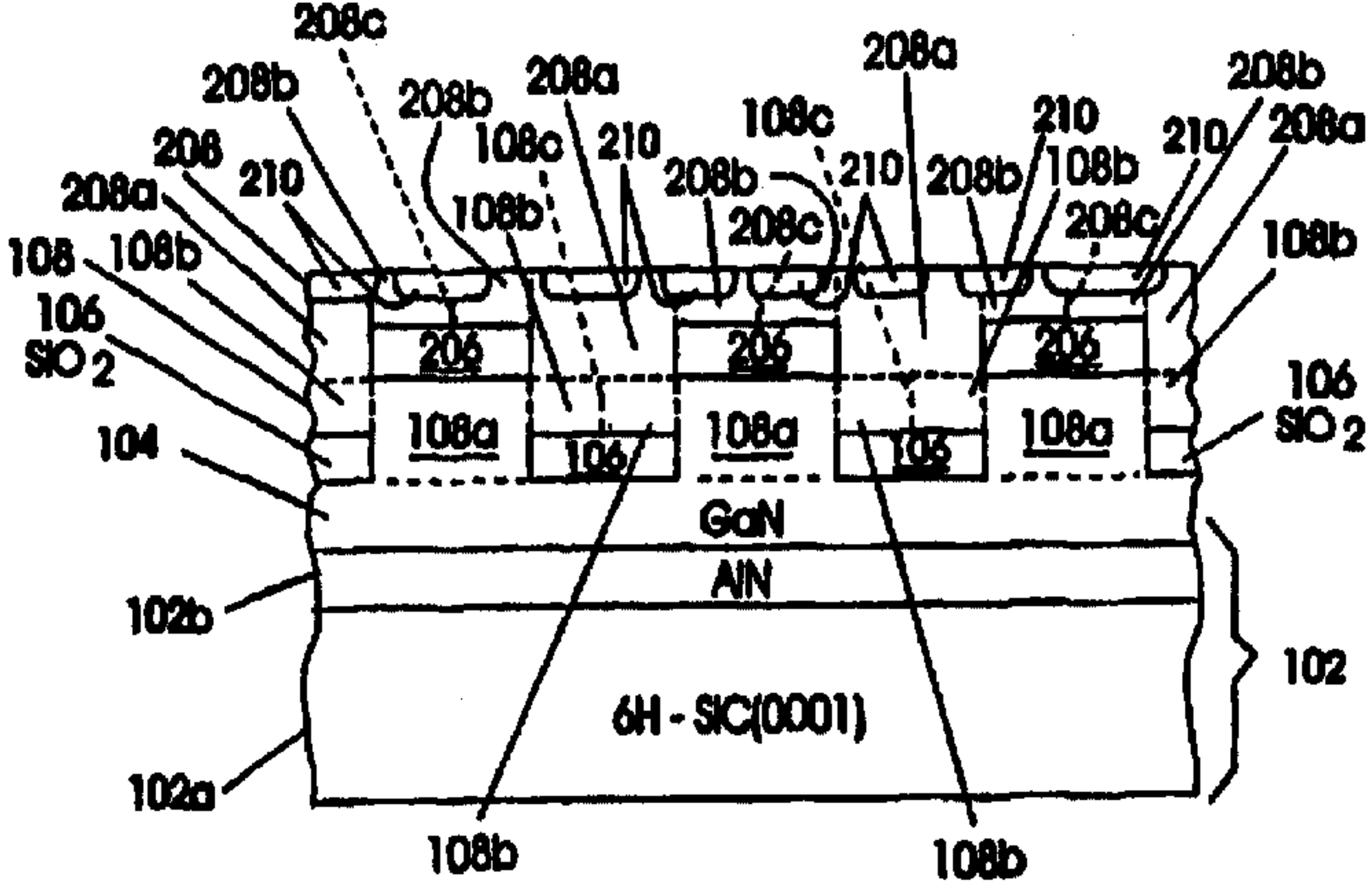
208b
108b
108
106
SiO 2
206
206
206
108a
108a
108a
104
GaN
AlN
102b
102
6H - SiC(0001)
102a
108b
108b

FIG. 14


208c
208a
208a
208b
208b
208b
208b
208a
108c
108c
208b
108b
208
208a
108b
108b
208c
208c
108b
108
106
SiO 2
206
206
206
106
SiO 2
108a
108a
108a
106
106
104
GaN
AlN
102b
102
6H - SiC(0001)
102a
108b
108b


208c
208b
208b
208a
208a
208b
208b
206
210
108c
210
108c
210
210
208a
208a
108
108b
108b
208c
208b
208b
208c
108b
106
SiO2
206
206
206
106
SiO2
104
108a
108a
108a
GaN
AlN
102b
102
6H - SiC(0001)
102a
108b
108b