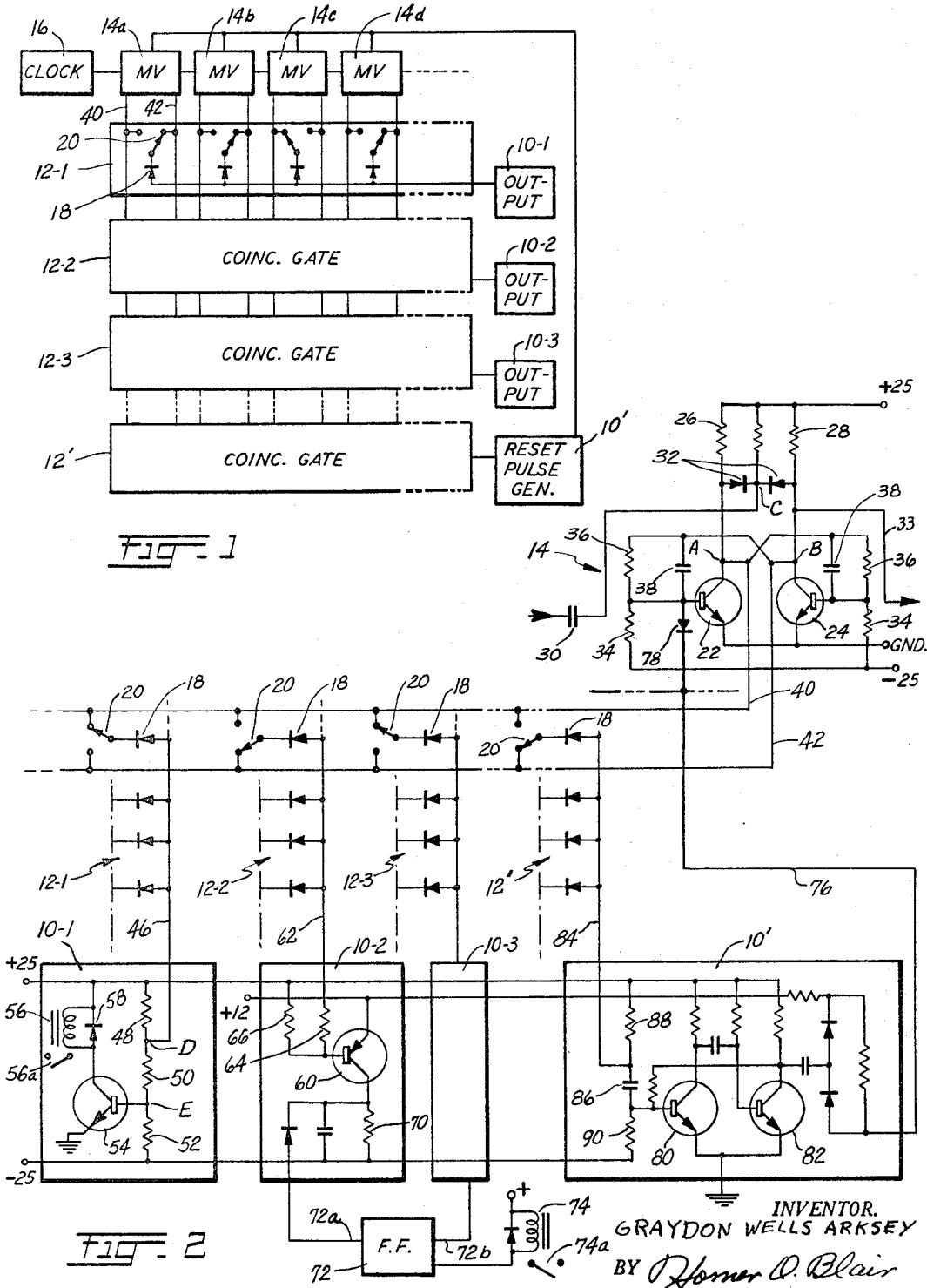


May 14, 1968

G. W. ARKSEY

3,383,525

SELECTABLE CYCLE TIMER WITH PLURAL OUTPUTS OF
DIFFERENT TIME INTERVALS AND AUTOMATIC RESET
Filed Jan. 21, 1966



1

3,383,525

SELECTABLE CYCLE TIMER WITH PLURAL OUTPUTS OF DIFFERENT TIME INTERVALS AND AUTOMATIC RESET

Graydon W. Arksey, Edmonton, Alberta, Canada, assignor to Chemcell Limited—Chemcell Limitee, a corporation of Canada

Filed Jan. 21, 1966, Ser. No. 522,131
15 Claims. (Cl. 307—269)

ABSTRACT OF THE DISCLOSURE

An electronic cycle timer is provided having a counter driven by clock pulses and having a series of relay circuits and a reset circuit, each operated when respective preset counts are reached. A relay stage may be on-and-off during one clock-pulse interval, or the relay stage may be turned "on" by one preset-count detector and "off" at another preset count. Successful use of many preset-count detectors is promoted by particular circuit features.

In its various aspects, the present invention relates to electronic gates and to electronic cycle timers.

A widely used form of timer uses a series of cams on a shaft to operate a number of switches at various times after the start of the cycle. The cam shaft is operated by a small synchronous motor and a reduction gear train. The total cycle duration is the time taken for a complete rotation of the cam shaft, and this is usually established by choice of an appropriate reduction gear train.

Cycle timers of this type have many disadvantages. Since the cams rotate relatively slowly, each cam operates its switch gradually in at least one direction to close or to open the contacts. This condition limits the life of the switches and leads to erratic switch operation. The problem is only partially met by resort to special snap-acting switches, or by using overly rugged contacts or by careful design of the control circuits to minimize contact erosion. Secondly, the times of operation of the switches are determined only with limited repeatable accuracy. Particularly in the case of long cycle times and where the cycle calls for certain switches to operate in close succession, the degree of inaccuracy and inconsistency of conventional cam cycle timers is a source of trouble. Further, the "on" time of cam-operated switches can be controlled only approximately, and this limitation becomes more serious as the "on" time becomes short in relation to the total cycle time. Finally, the total cycle time is limited by available gearing, so that (for example) 3-minute timers and 4-minute timers may be made by assembling appropriate gears in the driving train, but the gear drive is not flexible in the sense that the user may not be free to establish an intermediate cycle time that may be desired, such as a cycle time between 3 and 4 minutes. In any case, cycle timers that use cam contacts are subject to wear and all the other difficulties characteristic of mechanical devices.

An object of the present invention resides in the provision of an electronic analogue of such a cam cycle timer, for virtually eliminating all the foregoing difficulties. More specifically, an object of the present invention resides in providing a novel cycle timer wherein the total time of the cycle can be determined with far greater flexibility, wherein switch action is sudden in both "on" and "off" operations, wherein the "on" time of the sequence of switches can be accurately determined and maintained consistently even where short "on" times and long total cycle times are involved, and wherein mechanical wear and its consequences are avoided.

In achieving the foregoing objects, a novel cycle timer

2

is provided in which a clock-pulse source supplies pulses to an electronic pulse counter; a gate and set of selective switches connected to the counter enable presetting a precise count of clock-pulse intervals at which a relay is to operate; a large number of such gates and sets of selective switches enables a large number of times in the cycle when different relays are to operate; and one such gate and set of switches activates a reset circuit for the counter, to start a new cycle. A specific but important feature of such a cycle timer is the inclusion of a pair of gates and sets of count-presetting switches to turn "on" and then to turn "off" a relay and thereby to control the "on" time of such a relay. This form of cycle timer characteristically produces sudden operation of relay contacts, and the total cycle time that may be selected is limited only by the total capacity of the counter and the clock-pulse interval selected. Operating points of all the relays are consistently maintained and may be set at any time desired, limited only by the clock-pulse interval.

A further feature of this invention resides in the provision of a novel preset counter circuit wherein any possible interaction between the counter and the controlled circuit, particularly a large number of controlled circuits, is reduced to a minimum.

A further object of the invention relates to novel gate circuits of general application wherein solid-state diodes or other one-way conducting devices are used in such a manner that their leakage-current characteristic is virtually or entirely eliminated as a concern. In known gates using many solid-state diodes, the combined leakage currents can simulate the forward current to be expected in one diode, and in this way leakage currents can simulate erroneously a failure of agreement of the circuits compared by the gate.

In the illustrative embodiment of the invention detailed below, preset counter circuits and the gates in these circuits are related in a novel manner. The counter stages, as usual, include electronic devices which operate in either a high-conduction state or a block state. A gate connected to many selected electronic devices of the counter maintains an output device in one condition so long as any of the selected electronic devices is in its high-conduction state; and at this time one or more of the diodes (or substitute devices) are in their conducting state. When all the selected electronic devices of the counter change to their blocked state, each gate releases the output device to operate as if it were actually separate from the counter stages. In one instance, the voltage on the gate is reduced and reversed so that a low value of voltage is applied to the diodes, and the circuit in other respects is such as to make inconsequential the resulting combined leakage of the diodes in the gates. In another form, the voltage on the gate elements is largely or entirely removed so that there can be no leakage current and no leakage-current problems.

The nature of the invention in its various aspects, and further objects, novel features and advantages, will be more readily apparent from the following detailed description of an illustrative embodiment shown in the accompanying drawing. In the drawing:

FIGURE 1 is a block diagram of a novel cycle timer illustrating certain features of the present invention; and

FIGURE 2 is a diagram of portions of the cycle timer of FIG. 1 including the wiring diagrams of portions thereof, illustrating further features of the invention.

In FIG. 1, devices 10-1, 10-2, 10-3 . . . are a series of units for operating switches in sequence at preset times. The three units 10 shown in the drawing represent a much larger number of units normally included in practical cycle timers of this form. Clock-pulse source 16 provides impulses counted by stages 14.

Various values registered in the counter represent various elapsed times following the start of pulse-counting. Each gate 12 is adjustable to respond to a predetermined count. For this purpose each gate 12 includes a series of semiconductor diodes 18 connected to a selected one of two output points of a related counter stage 14 via two-position switch 20.

In the form of counter shown (and described in detail below) each stage 14 includes two electronic devices, one of which is in a high-conduction state while the companion device is blocked. When a particular device of each pair of devices in a counter stage is blocked, the stage is said to represent "0." All the stages are reset to "0" at the start of pulse-counting by means of gate 12' and reset pulse generator 10'. In response to successive pulses of a certain polarity input to each counter stage, its condition reverses repeatedly and represents "1" and then "0," alternately. In response to each pulse, a previously blocked device forming part of the counter stage becomes highly conductive and the companion device becomes blocked. In response to two input pulses, each stage delivers one triggering pulse to the next counter stage.

The count represented in the counter depends on the particular combination of states ("0" or "1") of all the stages 14. By connecting diodes 18 to the output points of the proper devices in stages 14, diodes 18 in any one gate 12 can provide an output signal only when the stages 14 are in a particular combination of "0" and "1" states. This represents a predetermined count. With each input pulse from clock-pulse source 16 representing a discrete time interval, each gate 12 provides a signal controlling a respective output device 10 at the end of a predetermined time interval following reset of all the counter stages to "0." The predetermined time intervals are selected by the adjustment of switches 20.

The described apparatus represents a cycle timer that is the analogue of mechanical cam-operated switches driven by a clock motor and reduction gearing. The novel cycle timer has many advantages. It is immune to wear. The operation of each switch-operating unit 10 is sudden regardless of how slow may be the advance of the timer. (This will be appreciated by considering a practical embodiment, where each switch operates abruptly despite an elapsed-time increment between clock pulses of six seconds.) This feature gives the dual advantages of avoiding gradual or "tease" operation of the switches and of determining with precisely repeating consistency the time of each switch operation. In contrast, tease-operation of cam switches is only partly avoided through the use of snap-acting switches; and operation of each cam switch at a given time is limited as to repeatable accuracy to some substantial percentage of the 360-degree cam rotation of the cams. Finally, the flexibility of cam timers driven by geared-down clock drive mechanisms is limited both as to accuracy of interval-selection and as to total cycle time, the latter being limited to available gearing. In contrast, any desired accuracy of time-interval selection is readily achieved with the foregoing cycle timer, using an appropriate clock-pulse interval and an appropriate number of stages 14; and the total cycle time is also capable of highly flexible selection merely by selective setting of the switches in gate 12'.

FIG. 2 shows certain details of a practical embodiment of the invention, illustrating further novel features.

In FIG. 2, a conventional form of binary counter stage 14 is illustrated. This includes transistors 22 and 24, their respective load resistors 26 and 28 providing output points A and B, and appropriate cross-coupled circuits between the collector of each transistor and the base of the other. In counter stage 14, one transistor is blocked while the other is saturated. Input is supplied via coupling capacitor 30 to a junction C of a pair of isolating diodes 32. Pulse output to the next stage appears on line 33 connected to output point B. The cross-coupling circuits mentioned

above include biasing resistors 34, cross-coupling resistors 36 and capacitors 38.

In a well-known manner, successive input pulses of a given polarity reverse the states of the transistors 22 and 24 successively; and upon every second reversal, a pulse of the given polarity appears on line 33 for the next-following stage. As a term of reference, each transistor and its associated load, bias and coupling means is here called an electronic device which is either blocked or in a high-conduction state. The high-conduction state is the result of a clamping arrangement in some forms of known binary counter stages, but in the circuit shown the high-conduction state is due to its operation at the saturation level. The load current of resistor 26 or 28 does not change due to other load currents in lines 40 and 42 when the associated transistor is operating in its high-conduction, saturated state. Typical circuit values with NPN transistors 22 and 24 type TI 495 are: resistors 28 and 30, 10,000 ohms; resistors 34, 680,000 ohms; resistors 36, 150,000 ohms. The transistor emitters are connected to ground, at the junction of a collector supply of plus 25 volts and a base bias supply of minus 25 volts.

Output points A and B of the counter stage 14 extend via lines 40 and 42 to the selective terminals of switches 20, whose selector contact is connected to a diode 18.

The common lead 46 of diodes 18 connected to switch-operating unit 10-1 extends to a point D in a voltage divider. This consists of resistors 48, 50 and 52 connected between the collector supply and the bias supply of transistor 54 whose emitter is grounded. Tap E of the voltage divider is connected to the transistor base. Relay 56 with its contacts 56a is the collector load. Diode 58 shunts relay 56 to accommodate the discharge of its magnetic field when transistor 54 is switched from its "on" condition to its blocked condition. In an example, resistor 48 is 150,000 ohms; resistor 50 is 150,000 ohms; resistor 52 is 470,000 ohms; the collector and bias supplies are plus 25 volts and minus 25 volts, respectively, and transistor 54 is NPN type TI 495.

In operation, it may be assumed that transistor 22 is in its high-conduction state, bringing terminal A close to ground potential. The connected diode 18 is forward-conducting in this circuit condition, shifting point E below ground and driving transistor 54 to cut-off. In this phase of operation, the small current in lead 46 is supplied by transistor 22, but this presents no problem. Due to its saturated operating condition, transistor 22 can readily supply this current and like currents in the leads 46 to additional output devices like 10-1. Moreover, some part of the current in lead 46 is derived from the transistors of other counter stages that may happen to be in their high-conduction states. Output device 10-1 remains in its inactive state, and accordingly relay 56 is deenergized, so long as any diode of the related gate 12 is connected to a high-conduction transistor in a counter stage 14.

It may now be assumed that the stage 14 in FIG. 2 has changed condition and transistor 22 is blocked; and it may also be assumed that a like condition prevails for every diode 18 in coincidence gate 12-1 connected to line 46. Points A shift almost to the potential of the collector supply, here a positive potential, as determined by the voltage divider consisting of load resistor 26 and resistors 34 and 36 associated with transistor 24. Points D also rise to a voltage level determined by voltage divider 48, 50, 52. The voltage at point D is below that of the counter-stage collector supply by an amount sufficient for diodes 18 to be reverse-biased and thus blocked. Diodes 18 may carry some small leakage current at this time; but any such current—even the combined leakage currents of all the diodes of gate 12—can have only a minimal effect on the voltage at point E that provides switching-on bias for transistor 54. Furthermore, such diode leakage current and that of the diodes in all the other gates 12 have virtually no effect on the counter-stage operation. A very stable condition exists when all

diodes 18 of a gate 10 are blocked due to their connection to the collector of a blocked counter-stage transistor; for then device 10-1 is released for operation under control of its own bias network.

Device 10-1 thus turns "on" in response to shift of all diodes 18 in the related gate 12 into their blocked state. This condition provides a high degree of mutual immunity between device 10-1 and the counter stages.

Device 10-1 remains "on" until the next clock pulse is registered in the counter. Accordingly, contacts 56a of relay 56 remain in their operated condition for the duration of one clock pulse before returning to their normal condition.

Output device 10-1 is one of plural output devices of this type that may be included in the complete apparatus. Output devices 10-2 and 10-3 represent another form of gate-controlled switch-operating circuit having operating characteristics in some respects similar to device 10-1 and used in a practical embodiment with one or more devices 10-1.

Output device 10-2 is connected by lead 62 to the common terminals of the several diodes 18 forming the gate 12-2 for device 10-2. As shown, the illustrated switch 20 connected to the related diode 18 is set for control by terminal B of the counter stage 14. Resistor 64 is interposed between the common gate lead 62 and the base of transistor 60. Base bias is supplied via resistor 66 which extends to the same voltage supply level as the collector supply in counter stage 14. In a practical example, transistor 60 is of the PNP type, with plus 25 volts at the bias supply terminal and plus 12 volts for emitter reference potential. The collector load resistor 70 extends to minus 25 volts.

With these connections, so long as terminal B in the counter stage shown (or terminal B in any other counter stage connected to the gate 12 of output device 10-2) is near ground potential due to the high-conduction state of the related transistor 24, diode 18 is forward conducting, and the base of transistor 60 is biased to turn this transistor "on."

When the selected points A and B of all stages 14 connected by switches 20 and diodes 18 to lead 62 shift close to the collector supply potential (due to blocking of transistor 22 or 24 selected by switches 20) the base of transistor 60 shifts virtually to the same potential as that of the collector supply in the counter stage. Transistor 60 is cut off.

There is then virtually no voltage difference across diodes 18 in gate 12-2 of unit 10-2. Any small voltage across the diode is in the back-biasing direction so there is little if any current flow. This represents an enormous effective impedance in the gate circuit when device 10-2 is allowed to change its state as the result of coincidence in gate 12-2. A very high degree of isolation results between the counter stages at one side of a particular gate 12 and the controlled output device 10-2 when the latter has been released by the gate and is turned "off" by its own bias supply. In an example, resistor 64 is 1.0 megohms and resistor 66 is 6.8 megohms.

Output device 10-2 and output device 10-3 are of identical form in this illustrative apparatus. The switches 20 of gates 12-2 and 12-3 are adjusted so that a sequence of clock pulses drives the pulse-counter to reach coincidence in gate 12-2 first and later in gate 12-3. The output of device 10-2 is coupled to one input point 72a of flip-flop 72 (a bistable stage having two input points) and the output of device 10-3 is coupled to input point 72b of flip-flop 72. A relay 74 having contacts 74a is connected as a load operated by flip-flop 72. Relay 74 is deenergized in the normal condition of the flip-flop, at the start of a timing cycle. When unit 10-2 responds to coincidence in gate 12-2, flip-flop 72 reverses and energizes relay 74. The "on" time for relay 74 continues in effect after control potential at point 72a disappears and until coincidence in gate 12-3 causes device 10-3 to apply

a reversing signal to input lead 72b of flip-flop 72. Relay 74 is then deenergized. The "on" time of relay 74 can thus be determined precisely at a very short time interval, even at a one-clock-pulse period, despite a vastly larger total time of the timing cycle.

The pair of output devices 10-2 and 10-3 and their gates 12-2 and 12-3 shown, together with the related flip-flops 72 and relays 74 are only one pair among many. A practical form of this apparatus includes eighteen pairs of such units controlling the "on" times of eighteen relays.

Gate 12' in FIGS. 1 and 2 triggers a reset pulse generator 10' for the counter stages 14. This occurs at a time established by the setting of the switches 20 in gate 12'. Naturally this time is later than the time settings of the other gates 12. The occurrence of coincidence in gate 12' causes unit 10' to deliver a reset pulse to all the counter stages 14 via common lead 76 and an isolating diode 78 individual to each counter stage.

Reset pulse generator 10' is a monostable multivibrator, including transistors 80 and 82. Input to the base of transistor 80 is applied by gate 12' via lead 84 and coupling condenser 86. Resistor 88 extends between lead 84 and the same positive voltage level as the collector supply of the counter stages. So long as any counter stage 14 has a saturated transistor connected via a diode 18 to lead 84, this lead remains at a level close to ground potential. Resistor 90 maintains cut-off bias on the base of transistor 80. When coincidence develops in gate 12' due to all the connected counter output points shifting to their collector-supply level, a positive-going pulse (in this example) is coupled by coupling condenser 86. This pulse is provided by resistor 88, the only function of the gate being to release lead 84 from ground potential. Leakage current in diodes 18 of gate 12' is of no concern here since there is no voltage across the diodes when coincidence is reached. Isolation between the output device 10' and the counter stages is complete during the time of coincidence in gate 12'.

In FIG. 2, lead 62 is one of many which are connected by diodes 18 and switches 20 of other gates to the various output points A or B of the several counter stages in the whole apparatus more fully shown in FIG. 1. Likewise, leads 46 and 84 are connected by diodes 18 and switches 20 to output points A and B of the counter stages. It may be assumed that many diodes 18 in corresponding gates 12 extend to an output point A or B of a counter stage that is at the voltage level of the collector supply in the counter, due to the blocked condition of the related transistor in the counter; and at the same time, many other diodes of those gates extend to output points A and B of other counter stages that may be assumed to be in their high-conduction state and thus very close to ground potential. At such a time the diode extending to the output point A or B of a blocked counter-stage transistor is itself blocked by virtue of its polarization. The common leads 46, 62, 84, etc. of the gates are all held near ground potential by the forward conduction of those diodes extending to output points of other counter stages assumed now to be in their high-conduction condition. The blocking action of those diodes 18 which extend to blocked transistors 22, 24, etc. provides isolation between the blocked transistors of the counter and those counter-stage transistors in their high-conduction state.

When any of the gates 12-1, 12-2, 12', etc. is in the condition of having all of its diodes 18 extending to blocked transistors in the counter stages, the lead 46, 62, 84, etc. of that gate is either at or at least near the +25-volt level of the output point A or B. Consequently, little or no reverse-current flow occurs in a gate in which none of the diodes is forward-conducting. Such limited-current condition has the important advantage of effectively imparting a high-impedance characteristic to each gate when none of the diodes thereof is forward-conducting. In turn, the input circuit of the output device can then be made of large-valued resistors. This high-impedance char-

acteristic makes practical the use of large numbers of gates connected in common to the counter-stage transistors. In a simulated cam timer, it is an advantage to be able to use many gates for operating large numbers of switching devices 56, 74, etc. Certain switching devices 74 are operated once by gate 12-2 to close and later by another gate 12-3 to open, thus requiring two gates per switching device. As already stated, the inclusion of many gates creates no special problem here. Switching devices controlled by two gates acting successively are not merely closed and then opened at accurate times in the total timing cycle, but they have accurately defined short or long "on" times, irrespective of how long may be the total time of the cycle timer.

The illustrative embodiment of the invention in its various aspects has proved highly successful and is presently preferred, but nonetheless it is readily modified by those skilled in the art, as by omitting or modifying some portions of the apparatus shown, and its various novel features may be utilized in other applications. Consequently the invention should be construed broadly in accordance with its full spirit and scope.

The embodiments of the invention in which an exclusive property or privilege is claimed are defined as follows:

1. A gating network, including a plurality of electronic devices each operable in either a blocked state or a high-conduction state, each said device having a load providing an output point, an output device having an input circuit providing a control point biased, in the absence of input current, to a level at least approaching that of the output point of a blocked electronic device, and a gate comprising plural one-way conductive solid-state devices connected in common to said control point and severally connected to the output points of said electronic devices for providing current to said control point when the related electronic device is in its high-conduction state, said output device being in one state in response to said bias level and being driven to a different state by input current to said control point from any of said one-way conductive solid-state devices in the forward conducting condition thereof, each of said solid-state devices being polarized to be forward-conducting when its respective electronic device is in its high-conduction state, whereby said control point is released to assume its bias level for causing response of the output device to the blocked state of all of said electronic devices and the tendency of said one-way conductive solid-state devices to contribute leakage current to said control point is minimal.

2. A gating network in accordance with claim 1, wherein each of said electronic devices is a transistor circuit in saturated condition when in its high-conduction state.

3. A gating network in accordance with claim 1, wherein said input circuit of said output device includes series resistors forming a voltage divider providing a first tap constituting said control point and providing a second tap more remote from the level of the output point of a said electronic device in its blocked state, said output device including a transistor having a base connected to said second tap, and said transistor having an emitter connected to a reference voltage level approximated by the output point of the electronic device in its high-conduction state.

4. A gating circuit in accordance with claim 1, wherein said electronic devices have transistors of a first semiconductor type and said output device has a transistor of a second semiconductor type opposite to said first type, the emitter of said second-type transistor being connected to a bias point between the levels of a said output point of a said electronic device when blocked and when in its high-conduction state, and the base of said second-type transistor having a bias resistor connected to a voltage level that approximates that of said output point in the blocked state of said electronic device.

5. A gating circuit in accordance with claim 1, where-

in the input circuit of said output device includes a resistor and a capacitor connected to form said control point, the resistor having another connection to a voltage supply point approximating that of said output point in the blocked state of said electronic device, and said capacitor having an opposite biasing connection, whereby the capacitor provides an output pulse as all of said electronic devices assume their blocked state.

6. A gating network, including a plurality of pairs of electronic devices each operable in either a blocked state or a high-conduction state, one such device of each pair being blocked while the companion device of that pair is in its high conduction state, an output device having an input circuit providing a control point biased, in the absence of input current, to a level at least approaching that of the output point of a blocked electronic device, and a gate comprising plural solid-state diodes connected in common to said control point and said gate including switching means for connecting each said diode to a selected electronic device of a respective one of said pairs for providing current to said control point when the electronic device connected thereto by said switching means is in its high-conduction state, said output device being in one state in response to said bias level and being driven to a different state by input current to said control point from any of said one-way conductive solid-state devices in the forward conducting condition thereof, each of said diodes being polarized to be forward-conducting when its respective electronic device is in its high-conduction state, whereby said control point is released to assume its bias level for causing response of the output device to the blocked state of all the selected electronic devices and the tendency of said one-way conductive solid-state devices to contribute leakage current to said control point is minimal.

7. A gating network in accordance with claim 6 wherein plural gates and plural output devices as aforesaid are included, the output devices having their control points connected to respective gates.

8. A gating network in accordance with claim 6 wherein plural gates and plural output devices as aforesaid are included, the output devices having their control points connected to respective gates, and wherein said pairs of electronic devices are interconnected as a pulse counter, further including clock pulse input means to the pulse counter whereby said output devices respond to the counter in timed succession as determined by the selective settings of the corresponding switching means.

9. A gating network in accordance with claim 6 wherein said pairs of electronic devices are interconnected as a pulse counter, further including clock-pulse input means to the pulse counter whereby said output device responds to the counter when a certain time is reached as determined by the selective setting of said switching means.

10. A gating network in accordance with claim 6 wherein a pair of gates and a pair of output devices as aforesaid are included, said pair of output devices having their control points connected, respectively, to the common connections of said pair of gates, further including a switching device and a bistable control device for said switching device, said bistable device having respective reversing connections to said output devices for control thereby.

11. A gating network in accordance with claim 6 wherein said pairs of electronic devices are interconnected as a pulse counter, further including clock-pulse input means to the pulse counter, and wherein plural gates and plural output devices as aforesaid are included, the output devices having their control points connected to respective gates, and wherein one of said output devices is a reset pulse generator having reset connections to said pairs of electronic devices, whereby said output devices respond to the counter in timed succession as determined by the selective settings of the corresponding switching

means and said counter is automatically reset at timed intervals in conditions to start another timing cycle.

12. A gating network in accordance with claim 6 wherein said pairs of electronic devices are interconnected as a pulse counter, and wherein said output device includes a relay comprising contacts in a normal condition in the normal state of the output device wherein all of said diodes are non-conducting, further including clock-pulse input means to the pulse counter, whereby said relay contacts when operated in response to the blocked state of all the selected electronic devices remains in its operated condition only during one clock-pulse period.

13. A simulated cam timer, including a pulse-counter comprising plural interconnected stages each including an electronic device that alternately assumes a high-conduction state and a blocked state, said device having an output point that assumes a first voltage level when said device is in its high-conduction state and a second voltage level when said device is in said blocked state, a clock-pulse source connected to an input point of said pulse-counter, a plurality of output devices each having an input biasing connection, and a plurality of gates each connected between a respective one of said output devices and selected points of said pulse-counter for representing different time intervals, each of said gates including a plurality of one-way conductive solid-state devices connected between said output point of a respective one of said electronic devices and the related input biasing point and being polarized for forward conduction when its said electronic device is in its high-conduction state, said output device being polarized to become operative when all of the one-way conductive devices connected to the input biasing point thereof become blocked,

and reset coupling means connected between the pulse-counter and that one of said output devices which represents the largest time intervals of said gates for starting successive timing cycles.

14. A cycle timer, including a clock-pulse generator, an electronic counter including interconnected counter units responsive to the clock-pulse generator, plural gating means each including switches connected to said counter units selectively for responding to different predetermined numbers of clock pulses registered in the counter, and plural output devices connected to said plural gating means, respectively, said output device which is connected to the gating means set for the largest predetermined number being a reset pulse generator and being connected to said counter unit for the start of a timing cycle, the others of said output devices having switching devices operated in succession at times predetermined by the settings of said gating-means switches.

15. A cycle timer in accordance with claim 14, wherein at least certain of said switching devices are connected to respective pairs of said pairs of output units for successive operation and return to normal so as to be in the operated condition during a precise preset time interval.

References Cited

UNITED STATES PATENTS

2,519,184	8/1950	Grosdoff	328—48
3,129,339	4/1964	Fritzsche et al.	307—88.5
3,172,042	3/1965	Dawirs	328—48
3,263,174	7/1966	Bjorkman et al.	328—48

JOHN S. HEYMAN, *Primary Examiner.*