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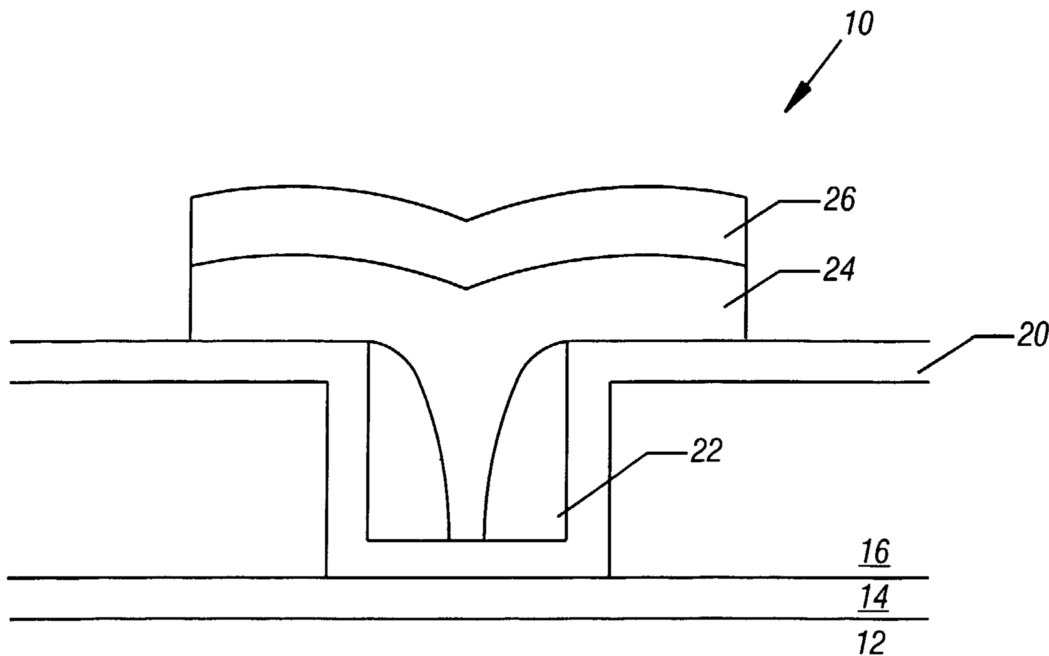
(54) Title: CARBON-CONTAINING INTERFACIAL LAYER FOR PHASE-CHANGE MEMORY



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(57) Abstract: A phase-change memory cell (10) may be formed with a carbon-containing interfacial layer (20) that heats a phase-change material (24). By forming the phase-change material (24) in contact, in one embodiment, with the carbon containing interfacial layer (20), the amount of heat that may be applied to the phase-change material (24), at a given current and temperature, may be increased. In some embodiments, the performance of the interfacial layer (20) at high temperatures may be improved by using a wide band gap semiconductor material such as silicon carbide.

Carbon-Containing Interfacial Layer For Phase-Change Memory

Background

This invention relates generally to memories that use phase-change materials.

Phase-change materials may exhibit at least two different states. The states may be
5 called the amorphous and crystalline states. Transitions between these states may be selectively initiated. The states may be distinguished because the amorphous state generally exhibits higher resistivity than the crystalline state. The amorphous state involves a more disordered atomic structure and the crystalline state involves a more ordered atomic structure. Generally, any phase-change material may be utilized; however, in some embodiments, thin-
10 film chalcogenide alloy materials may be particularly suitable.

The phase-change may be induced reversibly. Therefore, the memory may change from the amorphous to the crystalline state and may revert back to the amorphous state thereafter or vice versa. In effect, each memory cell may be thought of as a programmable resistor, which reversibly changes between higher and lower resistance states.

15 In some situations, the cell may have a large number of states. That is, because each state may be distinguished by its resistance, a number of resistance determined states may be possible allowing the storage of multiple bits of data in a single cell.

A variety of phase-change alloys are known. Generally, chalcogenide alloys contain one or more elements from column VI of the periodic table. One particularly suitable group
20 of alloys are GeSbTe alloys.

A phase-change material may be formed within a passage or pore defined through a dielectric material. The phase-change material may be coupled to contacts on either end of the passage.

The phase-change may be induced by heating the phase-change material. In some
25 embodiments of phase-change memories, a current is applied through a lower electrode that has sufficient resistivity or other characteristics to heat the phase-change material and to induce the appropriate phase change. In some embodiments, the lower electrode may produce temperatures on the order of 600° C.

One problem with existing electrode arrangements is that the higher the temperature,
30 the lower the resistivity of the material. Thus, as the lower electrode is heating up in order to

induce the phase change, it progressively becomes less resistive, thereby decreasing the amount of heat that is generated.

Thus, there is a need for a controllable way to provide sufficient resistance proximate to the phase-change material even at elevated temperatures.

5 Brief Description of the Drawings

Figure 1 is a greatly enlarged, cross-sectional view in accordance with one embodiment of the present invention;

Figure 2 is a greatly enlarged, cross-sectional view of an early stage of fabrication of the device shown in Figure 1 in accordance with one embodiment of the present invention;

10 Figure 3 is a greatly enlarged, cross-sectional view of the embodiment shown in Figure 2 at a subsequent stage of manufacturing in accordance with one embodiment of the present invention;

Figure 4 is a greatly enlarged, cross-sectional view of the embodiment shown in Figure 3 at the subsequent stage of manufacturing in accordance with one embodiment of the
15 present invention;

Figure 5 is a greatly enlarged, cross-sectional view of the embodiment of Figure 4 at a subsequent stage of manufacturing in accordance with one embodiment of the present invention;

Figure 6 is a greatly enlarged, cross-sectional view of a subsequent stage of
20 manufacturing in accordance with one embodiment of the present invention;

Figure 7 is an enlarged, cross-sectional view of still a subsequent stage of manufacturing in accordance with one embodiment of the present invention; and

Figure 8 is a schematic depiction of a system in accordance with one embodiment of the present invention.

25 Detailed Description

Referring to Figure 1, a memory cell 10 may include a phase-change material layer 24. The phase-change material layer 24 may be sandwiched between an upper electrode 26 and a lower electrode 14. In one embodiment, the lower electrode 14 may be cobalt silicide. However, the lower electrode 14 may be any conductive material. Similarly, the upper
30 electrode 26 may be any conductive material.

The lower electrode 14 may be defined over a semiconductor substrate 12. Over the lower electrode 14, outside the region including the phase-change material layer 24, may be an insulative material 16, such as silicon dioxide or silicon nitride, as two examples. A buried wordline (not shown) in the substrate 12 may apply signals and current to the phase-
5 change material 24 through the lower electrode 14.

A carbon-containing interfacial layer 20 may be positioned between the phase-change material layer 24 and the insulator 16. In one embodiment, a cylindrical sidewall spacer 22 may be defined within a tubular pore that is covered by the carbon-containing interfacial layer 20 and the phase-change material layer 24.

10 In one embodiment of the present invention, the carbon-containing interfacial layer 20 may be formed of silicon carbide. Silicon carbide, in its single crystal form, is a wide band gap semiconductor with alternating hexagonal planes of silicon and carbon atoms. Silicon carbide may be heated to 600° C in operation and may have a resistivity that does not significantly go down with increasing temperature. Therefore, silicon carbide is very
15 effective for heating the phase-change material layer 24. Again, it is desirable to heat the phase-change material layer 24 to induce changes of the phase-change material layer 24 between the amorphous and crystalline states.

The interfacial layer 20 does not increase its conductivity with increasing temperature to the same degree as other available materials such as cobalt silicide. The reduced resistivity
20 at increased temperature makes conventional materials less than ideal as heating electrodes for the phase-change material layer 24. At relatively high temperatures, such as 600° C, where the resistivity of other materials decreases, the effectiveness of the interfacial layer 20 as a heater to induce phase changes is not substantially diminished.

Silicon carbide, in particular, is less prone to losing its resistivity at higher
25 temperatures because it is a wide band gap material. Other wide band gap materials include galium nitride and aluminum nitride. Other carbon containing materials that may be utilized as the interfacial layer 20 in embodiments of the present invention may include sputtered carbon and diamond.

The interfacial layer 20 may be deposited, for example, by chemical vapor deposition
30 in the case of silicon carbide and by sputtering in the case of diamond or carbon. Other layer forming techniques may be utilized as well.

In some embodiments, it may be desirable to dope the interfacial layer 20 to increase its conductivity. In some embodiments, undoped silicon carbide, for example, may have too high a resistivity, resulting in either too high a temperature or too much voltage drop across the electrodes 14 and 26. Thus, ion implantation, for example, may be utilized to dope the
5 layer 20 with P-type or N-type impurities to improve its conductivity after annealing.

In some embodiments of the present invention, a layer (not shown) may be provided to improve the adhesion between the phase-change material layer 24 and the carbon-containing interfacial layer 20. Suitable adhesion promoting layers may include any conductive materials including titanium, titanium nitride and Tungsten, as a few examples.

10 Referring to Figure 2, a semiconductor substrate 12 may be covered with the lower electrode 14 in one embodiment. The electrode 14 may then be covered by an insulator 16 and a suitable pore 18 formed through the insulator 16.

The resulting structure may be blanket deposited, for example using chemical vapor deposition, with the carbon-containing interfacial layer 20 as shown in Figure 3. Thereafter,
15 in some embodiments, the carbon-containing interfacial layer 20 may be subjected to an ion implantation, as shown in Figure 4, to increase its conductivity and to decrease its resistivity after annealing.

As shown in Figure 5, a spacer material 22 may be deposited over the layer 20. The spacer material 22 may, in one embodiment, be a chemical vapor deposited oxide. The oxide
20 material 22 may then be subjected to an anisotropic etch to form the cylindrical sidewall spacer 22, shown in Figure 6, in the pore 18.

Turning to Figure 7, in one embodiment, the phase-change material layer 24 may be formed into the pore 18 and specifically into the region defined by the sidewall spacer 22 so as to contact the layer 20. An upper electrode 26 may be deposited over the phase-change
25 material 24. Then, the electrode 26 and the phase-change material 24 may be patterned and etched to form the structure shown in Figure 1.

Through the use of a carbon-containing interfacial layer 20, the resistivity of the phase-change material heater may be substantially increased while at the same time improving the heating performance of the heater at high temperatures. The heater effectively
30 includes the series combination of the lower electrode 14 and the carbon-containing interfacial layer 20. However, a series resistive combination is dominated by the element with the higher resistance, which may be the carbon-containing interfacial layer 20 in some

embodiments. As a result, the resistance of the series combination of layers 20 and 14 may be dominated by the resistance of the interfacial layer 20.

Referring to Figure 8, the memory cell shown in Figure 1 may be replicated to form a memory array including a large number of cells. That memory may be utilized as a memory of a wide variety of processor-based systems such as the system 40 shown in Figure 8. For example, the memory may be utilized as the system memory or other memory in a variety of personal computer products such as laptop products or desk top products or servers. Similarly, the memory may be utilized in a variety of processor-based appliances. Likewise, it may be used as memory in processor-based telephones including cellular telephones.

In general, the use of the phase-change memory may be advantageous in a number of embodiments in terms of lower cost and/or better performance. Referring to Figure 8, the memory 48, formed according to the principles described herein, may act as a system memory. The memory 48 may be coupled to a interface 44, for instance, which in turn is coupled between a processor 42, a display 46 and a bus 50. The bus 50 in such an embodiment is coupled to an interface 52 that in turn is coupled to another bus 54.

The bus 54 may be coupled to a basic input/output system (BIOS) memory 62 and to a serial input/output (SIO) device 56. The device 56 may be coupled to a mouse 58 and a keyboard 60, for example. Of course, the architecture shown in Figure 8 is only an example of a potential architecture that may include the memory 48 using the phase-change material.

While the present invention has been described with respect to a limited number of embodiments, those skilled in the art will appreciate numerous modifications and variations therefrom. It is intended that the appended claims cover all such modifications and variations as fall within the true spirit and scope of this present invention.

What is claimed is:

1 1. A method comprising:
2 forming a carbon-containing interfacial layer on a semiconductor; and
3 forming a phase-change material over said carbon-containing interfacial layer.

1 2. The method of claim 1 wherein forming a carbon-containing interfacial layer
2 on a semiconductor includes forming said interfacial layer over a conductive layer formed
3 over a semiconductor.

1 3. The method of claim 1 wherein forming a carbon-containing interfacial layer
2 includes forming a layer including a wide band gap semiconductor material.

1 4. The method of claim 3 wherein forming a carbon-containing interfacial layer
2 includes forming a silicon carbide layer.

1 5. The method of claim 4 further including doping said silicon carbide layer.

1 6. The method of claim 5 further including doping said silicon carbide layer
2 using ion implantation.

1 7. The method of claim 1 including forming a pore through an insulator,
2 depositing said carbon-containing interfacial layer over said semiconductor and in said pore.

1 8. The method of claim 7 including depositing the phase-change material over
2 the carbon-containing interfacial layer in said pore.

1 9. The method of claim 8 including forming a sidewall spacer between said
2 interfacial layer and said phase-change material.

1 10. The method of claim 1 wherein forming a phase-change material includes
2 depositing a chalcogenide layer over said interfacial layer.

1 11. A memory comprising:
2 a surface;
3 a carbon-containing interfacial layer over said surface; and
4 a phase-change material over said carbon-containing interfacial layer.

1 12. The memory of claim 11 wherein said surface includes a conductive layer over
2 a semiconductor substrate.

1 13. The memory of claim 11 wherein said carbon-containing interfacial layer
2 includes a wide band gap semiconductor material.

1 14. The memory of claim 13 wherein said carbon-containing interfacial layer
2 includes silicon carbide.

1 15. The memory of claim 14 wherein said silicon carbide layer is doped with
2 conductivity-type determining impurities.

1 16. The memory of claim 15 including an insulator positioned over said surface, a
2 pore formed through said insulator, said carbon-containing interfacial layer formed in said
3 pore over said surface.

1 17. The memory of claim 16 wherein said phase-change material is formed on
2 said carbon-containing interfacial layer and in said pore.

1 18. The memory of claim 17 including a sidewall spacer in said pore.

1 19. The memory of claim 18 wherein said sidewall spacer is positioned between
2 said interfacial layer and said insulator.

1 20. The memory of claim 11 wherein said phase-change material includes a
2 chalcogenide material.

1 21. An electronic device comprising:
2 a surface;
3 a carbon-containing interfacial layer over said surface; and
4 a phase-change material over said carbon-containing interfacial layer.

1 22. The device of claim 21 wherein said electronic device is a storage device.

1 23. The device of claim 22 wherein said storage device is part of a computer.

1 24. The device of claim 23 including a processor, an interface and a bus coupled
2 to said storage.

1 25. A memory comprising:
2 a semiconductor substrate;
3 a silicon carbide layer positioned over said substrate; and
4 a phase-change material over said silicon carbide layer.

1 26. The memory of claim 25 including a conductive layer between said
2 semiconductor substrate and said silicon carbide layer.

1 27. The memory of claim 26 including an insulator over said conductive layer,
2 said insulator having a pore defined therein, and said phase-change material and said silicon
3 carbide layer being formed in said pore.

1 28. The memory of claim 25 wherein said silicon carbide layer is doped.

1 29. The memory of claim 28 wherein said phase-change material includes
2 chalcogenide.

1 30. The memory of claim 29 including a sidewall spacer between said phase-
2 change material and said silicon carbide layer.

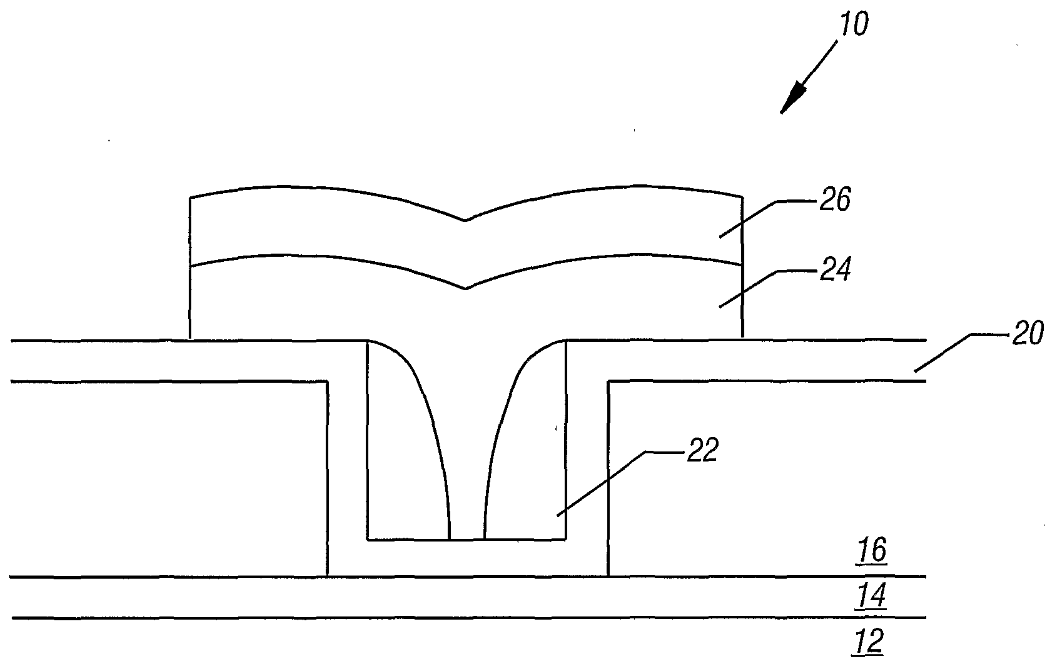

FIG. 1

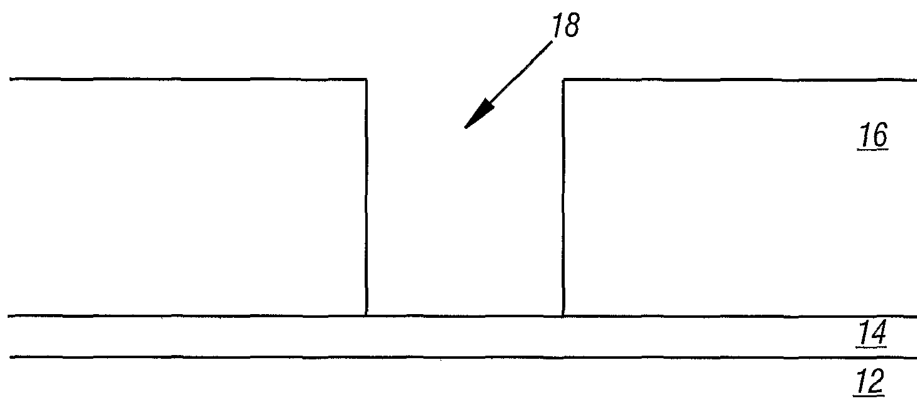

FIG. 2

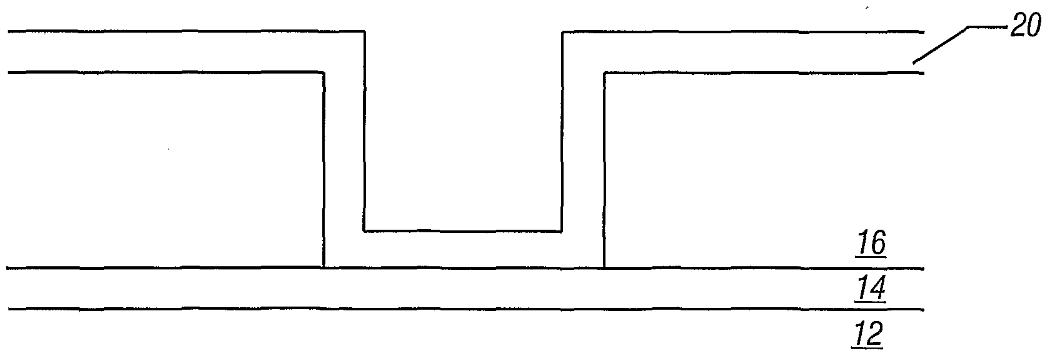

FIG. 3

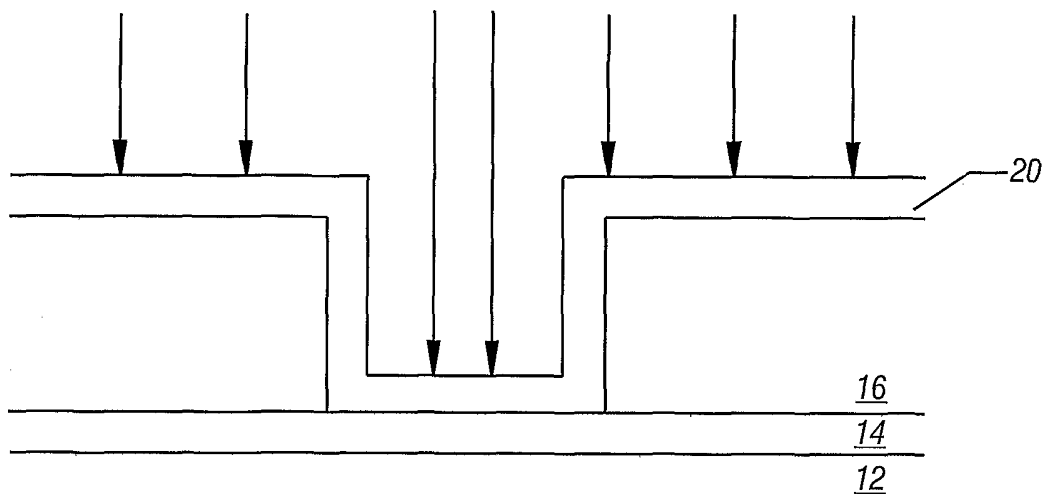

FIG. 4

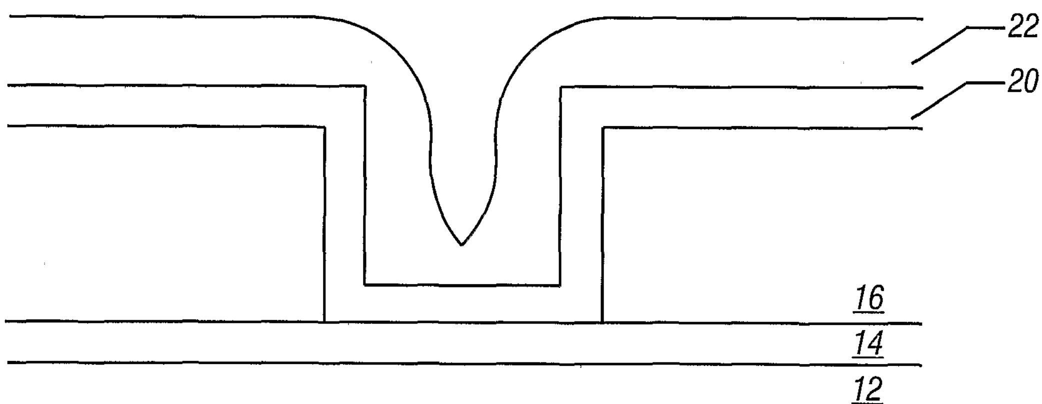

FIG. 5

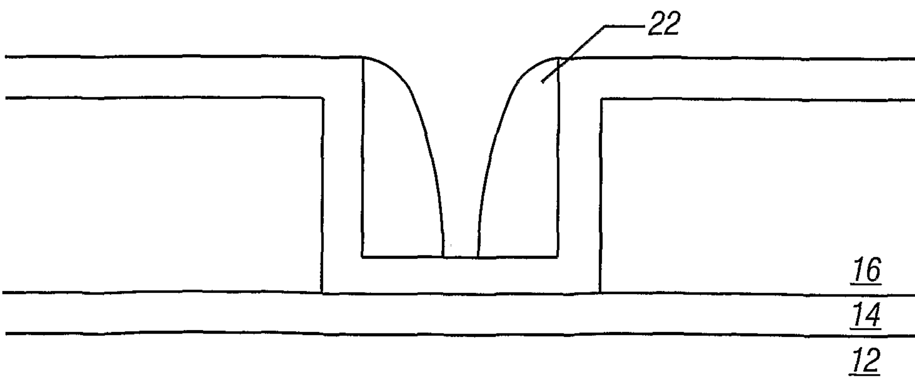

FIG. 6

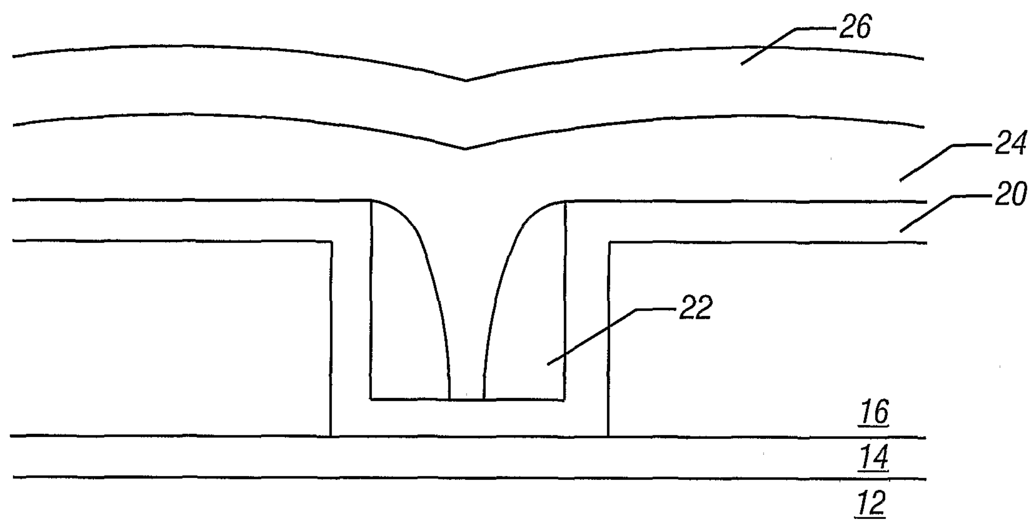

FIG. 7

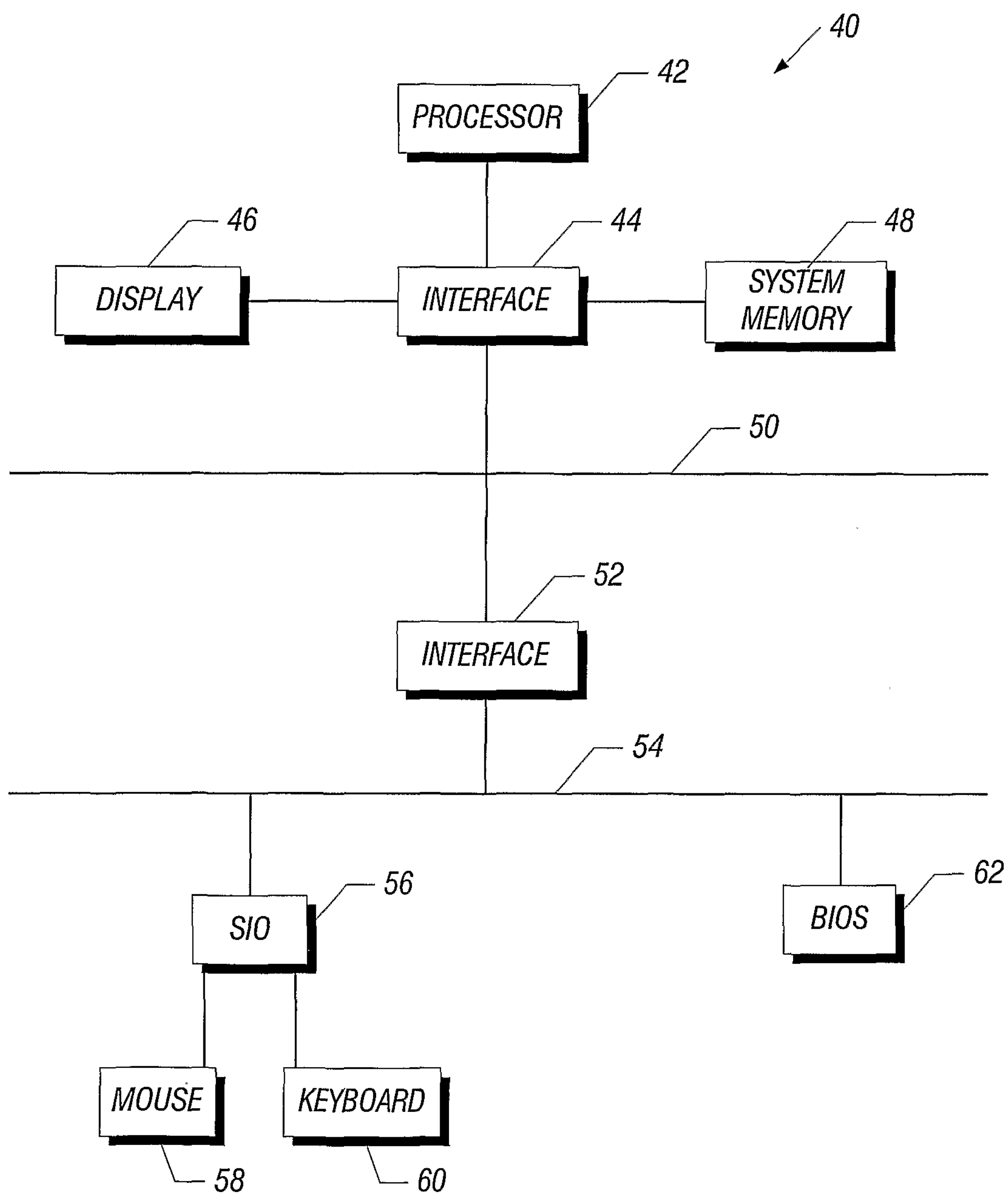

FIG. 8

INTERNATIONAL SEARCH REPORT

International Application No
PCT/US 02/29021

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 G11C11/34

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 G11C H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, WPI Data, PAJ, IBM-TDB

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5 825 046 A (KLERSY PATRICK ET AL) 20 October 1998 (1998-10-20)	1-3, 7-13, 16-24
A	column 5, line 18 - line 50 column 8, line 24 - line 62 column 9, line 10 - line 36 column 10, line 27 - line 43 column 11, line 8 - line 65; figure 1 ---	25-27, 29,30
X	US 5 933 365 A (KLERSY PATRICK ET AL) 3 August 1999 (1999-08-03)	1-3, 7-13, 16-24
A	column 10, line 30 -column 16, line 44; figure 1 --- -/--	25-27, 29,30

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
4 December 2002	17/12/2002

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31–70) 340–2040, Tx. 31 651 epo nl, Fax: (+31–70) 340–3016	Harms, J

Form PCT/ISA/210 (second sheet) (July 1992)

International Application No
PCT/US 02/29021

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 6 031 287 A (HARSHFIELD STEVEN T) 29 February 2000 (2000-02-29) entire document	1-30

Form PCT/ISA/210 (continuation of second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT
Information on patent family members

International Application No
PCT/US 02/29021

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