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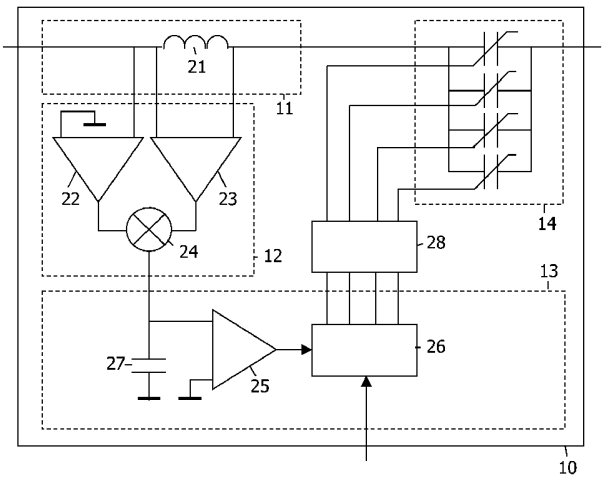
(54) **Title:** DEVICE COMPRISING A CONTROLLED MATCHING STAGE



(57) **Abstract:** Device (5) comprising controlled matching stages (10) for matching second stages such as antenna stages (2) to first stages such as power amplifier stages (1) get a simple construction by providing the controlled matching stages (10) with deriving means (11) for deriving first signals and second signals from output signals of the first stages, with detecting means (12) for detecting phases between the first signals and the second signals, and with controlling means (13) for controlling adjustable impedance networks (14) in response to said detecting for said matching. The deriving means (11) comprise elements (21) such as passive elements such as inductors and capacitors, with the first signals being the output signals and the second signals being derived via the elements (21). The detecting means (12) comprise phase detectors (22-24) made of first and second limiters (22,23) for limiting the first and second signals and mixers (24) for mixing the limited first and second signals. The controlling means (13) comprise analog-to-digital converters (25) such as limiters and digital circuits (26) such as up-down counters.

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Device comprising a controlled matching stage

The invention relates to a device comprising a controlled matching stage for matching a second stage to a first stage, and further relates to a controlled matching stage for matching a second stage to a first stage, to a method for matching a second stage to a first stage, and to a processor program product for matching a second stage to a first stage.

Examples of such a device are mobile phones, wireless interfaces, and further transmitters and/or receivers.

A prior art device is known from WO 02/063782 A2, which discloses in its Fig. 10 a controlled matching stage. This controlled matching stage uses a directional coupler for sampling a forward power signal and a reflected power signal and converts the power signals into control signals. These control signals are supplied to a processing unit, which controls a capacitor bank.

The known device is disadvantageous, inter alia, owing to the fact that it is relatively complex. The power signals need to be converted into control signals. These control signals need to be processed in the processing unit, before it can control the capacitor bank.

It is an object of the invention, inter alia, to provide a device which is relatively simple.

Furthers objects of the invention are, inter alia, to provide a controlled matching stage, a method and a processor program product which are relatively simple.

The device according to the invention comprises a controlled matching stage for matching a second stage to a first stage, the controlled matching stage comprising:

- deriving means for deriving a first signal and a second signal from an output signal of the first stage;
- detecting means for detecting a phase between the first signal and the second signal; and

- controlling means for controlling an adjustable impedance network in response to said detecting for said matching.

By introducing the detecting means for detecting a phase between the first signal and the second signal, it is no longer necessary to use a forward power signal and a reflected power signal. In response to said detecting, the controlling means directly control the adjustable impedance network. As a result, the device according to the invention is relatively simple.

The device according to the invention is further advantageous in that the controlled (and/or adaptive) matching stage will improve the linearity and the efficiency of the first stage and/or the second stage, will relax reliability requirements which can be traded off against further size and/or cost reductions, and will improve the user friendliness of the device when it gets less hot than before.

A controlled matching stage is a matching stage that is (automatically) controlled, for example via a loop such as an open loop (forward control) or a closed loop (backward control).

It should be noted that the article "Automatic Antenna Tuning for RF Transmitter IC Applying High Q Antenna" by Attila Zólomy, Ferenc Mernyei, János Erdélyi, Matthijs Pardoen+ and Gábor Tóth, Integration Hungary Ltd., Záhony u. 7. 1031 Budapest, Hungary, +Integration Associates Inc., 110 Pioneer Way, Unit L, Mountain View, California 94041 USA, 0-7803-8333-8/04/$20.00 (C) 2004 IEEE discloses in its Fig. 3 an antenna tuning circuitry comprising deriving means for deriving a first signal from an output signal of a power amplifier (the first stage being a power amplifier stage) and for deriving a second signal from a control signal of the power amplifier. So, the second signal is not derived from the output signal of the power amplifier stage but comes from somewhere inside the power amplifier stage. This is a disadvantageous solution. The article does not show the advantageous deriving means for deriving a first signal and a second signal from an output signal of the first stage.

An embodiment of the device according to the invention is defined by the second stage comprising an antenna stage and the first stage comprising a power amplifier stage or a switching stage. In this case, the controlled matching stage is located between a power amplifier stage or a switching stage on the one hand and an antenna stage on the other hand. The power amplifier stage for example comprises a power amplifier and the antenna stage for example comprises an antenna and/or an antenna connection.

An embodiment of the device according to the invention is defined by the first stage comprising a power amplifier stage and the second stage comprising a switching stage or an antenna stage. In this case, the controlled matching stage is located between a power amplifier stage on the one hand and an antenna stage or a switching stage on the other hand.

An embodiment of the device according to the invention is defined by the deriving means comprising an element, the first signal being the output signal and the second signal being derived via the element. Such an element might for example comprise (a resistance of) a diode or a switch, with the output signal being an output voltage and with the first signal being this output voltage and with the second signal being a voltage across the element. So, parts of the deriving means might coincide with other parts of the same controlled matching stage or with parts of a following stage.

An embodiment of the device according to the invention is defined by the element comprising a passive element and the adjustable impedance network comprising an adjustable capacitor. Such a passive element can be a resistor, in which case one of the signals will need to be phase shifted and a phase shifter is to be introduced into the controlled matching stage. Such a passive element can also be an inductor, in which case the inductor may be shifted from the adjustable impedance network into the deriving means. With the output signal being an output voltage and with the first signal being this output voltage and with the second signal being a voltage across the inductor, it is no longer necessary to introduce the phase shifter into the controlled matching stage. This is because the voltage across and the current through the inductor are already shifted in phase. The adjustable impedance network comprises an adjustable capacitor that for example corresponds with a capacitor bank, and may further comprise the inductor. Such a passive element can also be a capacitor etc.

An embodiment of the device according to the invention is defined by the detecting means comprising a phase detector. Such a phase detector is an advantageous (low cost and simple) embodiment.

An embodiment of the device according to the invention is defined by the phase detector comprising first and second limiters for limiting the first and second signals and comprising a mixer for mixing the limited first and second signals. Such first and second limiters and such a mixer are an advantageous (low cost and simple) embodiment.

An embodiment of the device according to the invention is defined by the controlling means comprising an analog-to-digital converter and a digital circuit. Such a digital circuit is an advantageous (low cost and simple) embodiment, and therefore the

analog-to-digital converter is to be located directly after the detecting means, to make an analog part as small as possible and to make a digital part as large as possible.

An embodiment of the device according to the invention is defined by the digital circuit comprising an up-down counter, the up-down counter comprising a counting input coupled to the analog-to-digital converter and an enabling input to be coupled to a base band controller. Such an up-down counter is an advantageous (low cost and simple) embodiment. An output of the up-down counter is for example via a dc-dc level shifter coupled to a control input of the adjustable impedance network. The base band controller for example supplies a pulse to the enabling input in dependence of for example a mode of the device (for example a TDMA frame), such as a transmitter mode. A rising edge of the pulse for example defines the loading of the up-down counter via the counting input (positive or negative value) and a falling edge of the pulse for example defines the up-counting (in case of a loaded positive value) or the down-counting (in case of a loaded negative value) dependently on the loading.

Embodiments of the controlled matching stage according to the invention and of the method according to the invention and of the processor program product according to the invention correspond with the embodiments of the device according to the invention.

The invention is based upon an insight, inter alia, that a use of forward power signals and reflected power signals make the device unnecessary complex (and large in order to create directivity in the bidirectional coupler), and is based upon a basic idea, inter alia, that a first signal and a second signal are to be derived from an output signal of a first stage, a phase between the first signal and the second signal is to be detected, and an adjustable impedance network is to be controlled in response to said detecting for said matching.

The invention solves the problem, inter alia, to provide a device which is relatively simple, and is advantageous, inter alia, in that the controlled matching stage will improve the linearity and the efficiency of the first stage and/or the second stage, will relax reliability requirements which can be traded off against further size and cost reductions, and will improve the user friendliness of the device when it gets less hot than before.

These and other aspects of the invention will be apparent from and elucidated with reference to the embodiments(s) described hereinafter.

In the drawings:

Fig. 1 shows diagrammatically a device according to the invention comprising a power amplifier stage, a controlled matching stage according to the invention and an antenna stage;

Fig. 2 shows diagrammatically a device according to the invention comprising a power amplifier stage, a receiver stage, a controlled matching stage according to the invention and an antenna stage, with a switching stage located between the power amplifier stage and the receiver stage on the one hand and the controlled matching stage on the other hand;

Fig. 3 shows diagrammatically a device according to the invention comprising a power amplifier stage, a receiver stage, a controlled matching stage according to the invention and an antenna stage, with a switching stage located between the power amplifier stage, the controlled matching stage and the receiver stage on the one hand and the antenna stage on the other hand;

Fig. 4 shows diagrammatically a controlled matching stage according to the invention in greater detail for use in a device according to the invention;

Fig. 5 shows a series LC network design and a corresponding Smith chart for use in a controlled matching stage according to the invention; and

Fig. 6 shows a maximum-to-minimum capacitor ratio Cmax/Cmin ratio and a maximum peak voltage Vpk across the capacitor as a function of an inductor value L of the series LC network design shown in Fig. 5.

The device 5 according to the invention shown in Fig. 1 comprises a power amplifier stage 1, a controlled matching stage 10 according to the invention and an antenna stage 2. An output of the power amplifier stage 1 is coupled to an input of the controlled matching stage 10, and an output of controlled matching stage 10 is coupled to an input of the antenna stage 2. The power amplifier stage 1 for example comprises a power transistor, and the antenna stage 2 for example comprises an antenna and/or an antenna connection.

The device 5 according to the invention shown in Fig. 2 comprises a power amplifier stage 1, a receiver stage 4, a switching stage 3, a controlled matching stage 10 according to the invention and an antenna stage 2. An output of the power amplifier stage 1 is coupled to an input of the switching stage 3, an input of the receiver stage 4 is coupled to an output of the switching stage 3, and an in/output of the switching stage 3 is coupled to an in/output of the controlled matching stage 10. A further in/output of the controlled matching

stage 10 is coupled to an in/output of the antenna stage 2. In a transmitter mode, the controlled matching stage 10 is active, in a receiver mode, the controlled matching stage 10 is inactive, for example by being short-circuited (not shown) or by disconnecting it (not shown). An option of having (further) stages in parallel is not to be excluded.

The device 5 according to the invention shown in Fig. 3 comprises a power amplifier stage 1, a receiver stage 4, a controlled matching stage 10 according to the invention, a switching stage 3, and an antenna stage 2. An output of the power amplifier stage 1 is coupled to an input of the controlled matching stage 10, an output of the controlled matching stage 10 is coupled to an input of the switching stage 3, an input of the receiver stage 4 is coupled to an output of the switching stage 3, and an in/output of the switching stage 3 is coupled to an in/output of the antenna stage 2.

The controlled matching stage 10 according to the invention shown in Fig. 4 comprises deriving means 11 for deriving a first signal and a second signal from an output signal of a first stage 1,3, detecting means 12 for detecting a phase between the first signal and the second signal, and controlling means 13 for controlling an adjustable impedance network 14 in response to said detecting for said matching. The deriving means 11 comprise an element 21 such as for example an inductor or, alternatively, a (variable) capacitor, with the first signal being the output signal (the voltage at the output of the first stage 1,3 with respect to ground) and the second signal being derived via the element 21 (the voltage across the inductor). The adjustable impedance network 14 comprises an adjustable capacitor, such as for example four adjustable capacitors in parallel (a binary weighted 4-bit switched capacitor array).

The detecting means 12 comprising a phase detector 22-24. This phase detector 22-24 comprises first and second limiters 22,23 for limiting the first and second signals and comprises a mixer 24 for mixing the limited first and second signals and a capacitor 27 coupled to ground to remove unwanted RF frequency components. The controlling means 13 comprise an analog-to-digital converter 25 such as for example a third limiter of which an input is coupled to an output of the mixer 24. The controlling means 13 further comprise a digital circuit 26 such as for example an up-down counter comprising a counting input coupled to an output of the analog-to-digital converter 25 and comprising an enabling input to be coupled to an output of a base band controller (not shown). Outputs of the digital circuit 26 are coupled via a dc-dc level shifter 28 to control inputs of the adjustable impedance network 14 for controlling its four adjustable (switchable) capacitors. The base band controller (not shown) for example supplies a pulse to the enabling input in dependence

of for example a mode of the device 5, such as a transmitter mode. A rising edge of the pulse for example defines the loading of the up-down counter via the counting input (positive or negative value) and a falling edge of the pulse for example defines the up-counting (in case of a loaded positive value) or the down-counting (in case of a loaded negative value) dependently on the loading.

Between the first stage 1 (or 3 or 1 respectively) and the second stage 2 (or 2 or 3 respectively), the controlled matching stage 10 introduces a so-called series LC network. Of this series LC network, the inductor L has a fixed value and the capacitor C has an adjustable value. The use of this series LC network is very advantageous, as explained hereafter.

Nowadays, a device 5 in the form of a cellular phone usually makes use of a build-in antenna that is constructed as a planar inverted-F antenna (PiFa). A dual-band planar inverted-F antenna is designed to be series resonant at both bands of operation. Body-effects detune the antenna resonance frequencies downwards causing an inductive behavior of the antenna at both bands. This fluctuation in the reactive part of the antenna impedance is typically much larger than the change in the resistive part of the antenna impedance that represents its radiation resistance. The limited antenna bandwidth results mainly in a capacitive behavior of the antenna feed impedance at the lower end of the band and in an inductive behavior at the higher end. The body-effects and limited antenna bandwidth cause mainly a change in the reactance of the antenna feed impedance. Therefore, a variable series LC network, located close to this feed point, can effectively be used to compensate for a major part of antenna impedance variations that occur in practice. This series LC network is embedded in a control loop comprising the deriving means 11, the detecting means 12 and the controlling means 13 to automatically correct the mismatches.

The control loop controls the detected phase of the matched impedance φ_{Zdet} to zero. This phase is given by the phase difference between the series LC network input voltage u and its input current i. It is detected by a (Gilbert cell) mixer 24 which input signals are hard limited by the limiters 22,23. The phase of the input current i is derived from the voltage across the series inductor L that acts as, an almost frequency independent, +90 degrees phase shifter. The phase detector output signal φ_{Zdet} is fed to the analog-to-digital converter 25 in the form of a limiter to determine the sign of the phase error. Depending on this sign of the phase error the up-down counter will either increase or decrease its output value in steps of one least significant bit under control of a base band enable signal. In a Time Division Multiple Access based system, reading of the phase error can occur at the

rising edge of the base band enable signal while a power burst is being transmitted, whereas an update of the capacitor value can be done outside the power burst at the falling edge of the base band enable signal. This avoids spurious emission and hot-switching during adaptation.

The controlled matching stage 10 is made variable with for example a 4-bit binary weighted switched capacitor array. Its capacitance can be changed in steps of 0.25 pF to a maximum of 8 pF. A possible implementation of the switched capacitor array might use RF-MEMS devices that need high actuation voltages. Therefore, a level shifter between the up-down counter output and the switched capacitor control lines might need to be used.

A series LC network design and a corresponding Smith chart for use in a controlled matching stage 10 according to the invention are shown in Fig. 5. The series LC network comprises, to get a Z-matched, a serial circuit of X-L-series, X-C-series, X-load and R-load. The X-L-series and the X-C-series together form X-cor.

A maximum-to-minimum capacitor ratio Cmax/Cmin ratio and a maximum peak voltage Vpk across the capacitor as a function of an inductor value L of the series LC network design shown in Fig. 5 are shown in Fig. 6.

These Figs. 5 and 6 are to be looked at as follows. A variable series LC network allows for correction of both capacitive and inductive mismatches. This correction of the load reactance X-cor is visualized in the Smith chart of Fig. 5 as a rotation over the bold circle segment of constant resistance R-load. X-cor is positive (inductive) when the load is capacitive and is negative (capacitive) when the load is inductive. The maximum-to-minimum capacitance ratio depends on the series inductor reactance X-L-series and on the amount of correction that is desired on both sides of the circle segment of constant resistance R-load. In Fig. 6 a curve of Cmax/Cmin versus L-series is shown as an example in which the magnitude of the reflection coefficient $|\Gamma|$ is reduced from approx. 0.6 to 0.3 for a capacitive mismatch and from approx. 0.7 to 0.3 for an inductive mismatch. Especially for small values of L-series the ratio becomes very large. In a series LC network relatively high voltages Vpk across the variable capacitor occur at high power and large mismatch conditions. Typical values of this peak voltage Vpk are given on the right-hand-side Y-axis in Fig. 6. These are valid for 2 Watt delivered into a 50 Ω load resistance at 900 MHz. At these high RF-voltages self-actuation of the electrostatic RF-MEMS devices shall be avoided and harmonic distortion shall be kept below -70 dBc in order to be able to meet typical GSM system specification.

It should be noted that the above-mentioned embodiments illustrate rather than limit the invention, and that those skilled in the art will be able to design many alternative

embodiments without departing from the scope of the appended claims. In the claims, any reference signs placed between parentheses shall not be construed as limiting the claim. Use of the verb "to comprise" and its conjugations does not exclude the presence of elements or steps other than those stated in a claim. The article "a" or "an" preceding an element does not exclude the presence of a plurality of such elements. The invention may be implemented by means of hardware comprising several distinct elements, and by means of a suitably programmed computer. In the device claim enumerating several means, several of these means may be embodied by one and the same item of hardware. The mere fact that certain measures are recited in mutually different dependent claims does not indicate that a combination of these measures cannot be used to advantage.

CLAIMS:

1. Device (5) comprising a controlled matching stage (10) for matching a second stage to a first stage, the controlled matching stage (10) comprising:
- deriving means (11) for deriving a first signal and a second signal from an output signal of the first stage;
- detecting means (12) for detecting a phase between the first signal and the second signal; and
- controlling means (13) for controlling an adjustable impedance network (14) in response to said detecting for said matching.

2. Device (5) according to claim 1, the second stage comprising an antenna stage (2) and the first stage comprising a power amplifier stage (1) or a switching stage (3).

3. Device (5) according to claim 1, the first stage comprising a power amplifier stage (1) and the second stage comprising a switching stage (3) or an antenna stage (2).

4. Device (5) according to claim 1, the deriving means (11) comprising an element (21), the first signal being the output signal and the second signal being derived via the element (21).

5. Device (5) according to claim 4, the element (21) comprising a passive element and the adjustable impedance network (14) comprising an adjustable capacitor.

6. Device (5) according to claim 1, the detecting means (12) comprising a phase detector (22-24).

7. Device (5) according to claim 6, the phase detector (22-24) comprising first and second limiters (22,23) for limiting the first and second signals and comprising a mixer (24) for mixing the limited first and second signals.

8. Device (5) according to claim 1, the controlling means (13) comprising an analog-to-digital converter (25) and a digital circuit (26).

9. Device (5) according to claim 8, the digital circuit (26) comprising an up-down counter, the up-down counter comprising a counting input coupled to the analog-to-digital converter (25) and an enabling input to be coupled to a base band controller.

10. Controlled matching stage (10) for matching a second stage to a first stage, the controlled matching stage (10) comprising:

- deriving means (11) for deriving a first signal and a second signal from an output signal of the first stage;
- detecting means (12) for detecting a phase between the first signal and the second signal; and
- controlling means (13) for controlling an adjustable impedance network (14) in response to said detecting for said matching.

11. Method for matching a second stage to a first stage, the method comprising the steps of:

- deriving a first signal and a second signal from an output signal of the first stage;
- detecting a phase between the first signal and the second signal; and
- controlling an adjustable impedance network (14) in response to said detecting for said matching.

12. Processor program product for matching a second stage to a first stage, the processor program product comprising the functions of:

- deriving a first signal and a second signal from an output signal of the first stage;
- detecting a phase between the first signal and the second signal; and
- controlling an adjustable impedance network (14) in response to said detecting for said matching.

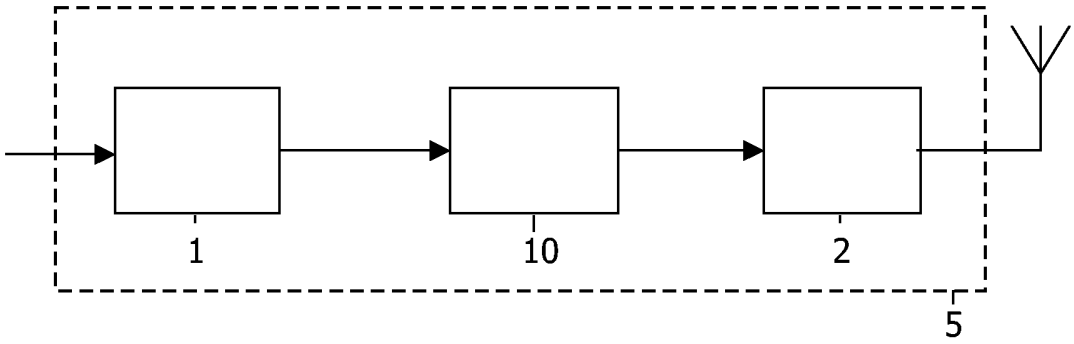

FIG.1

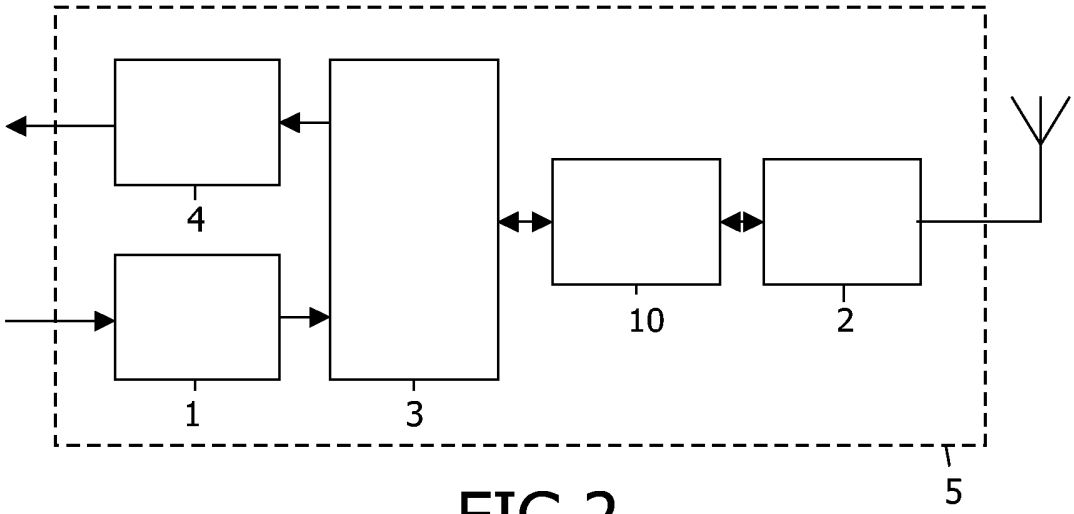

FIG.2

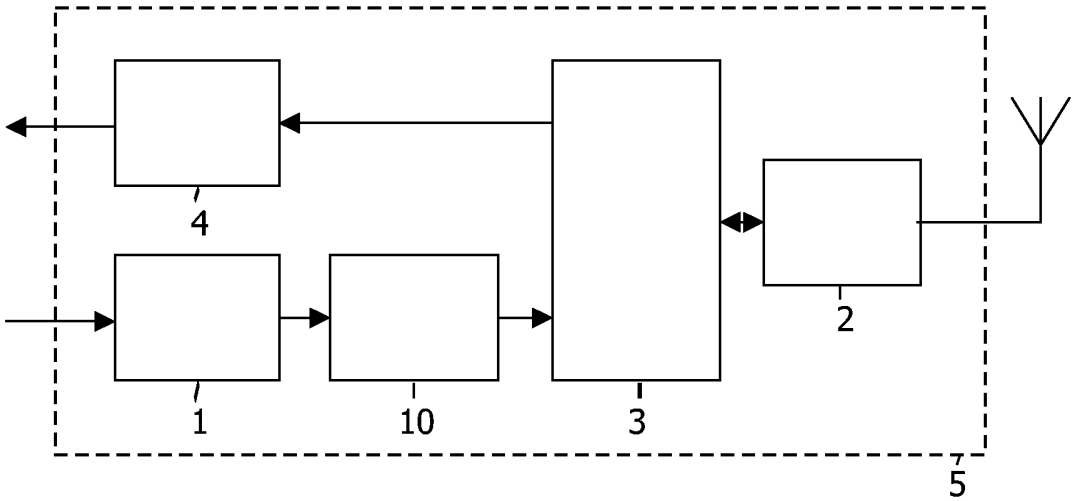

FIG.3

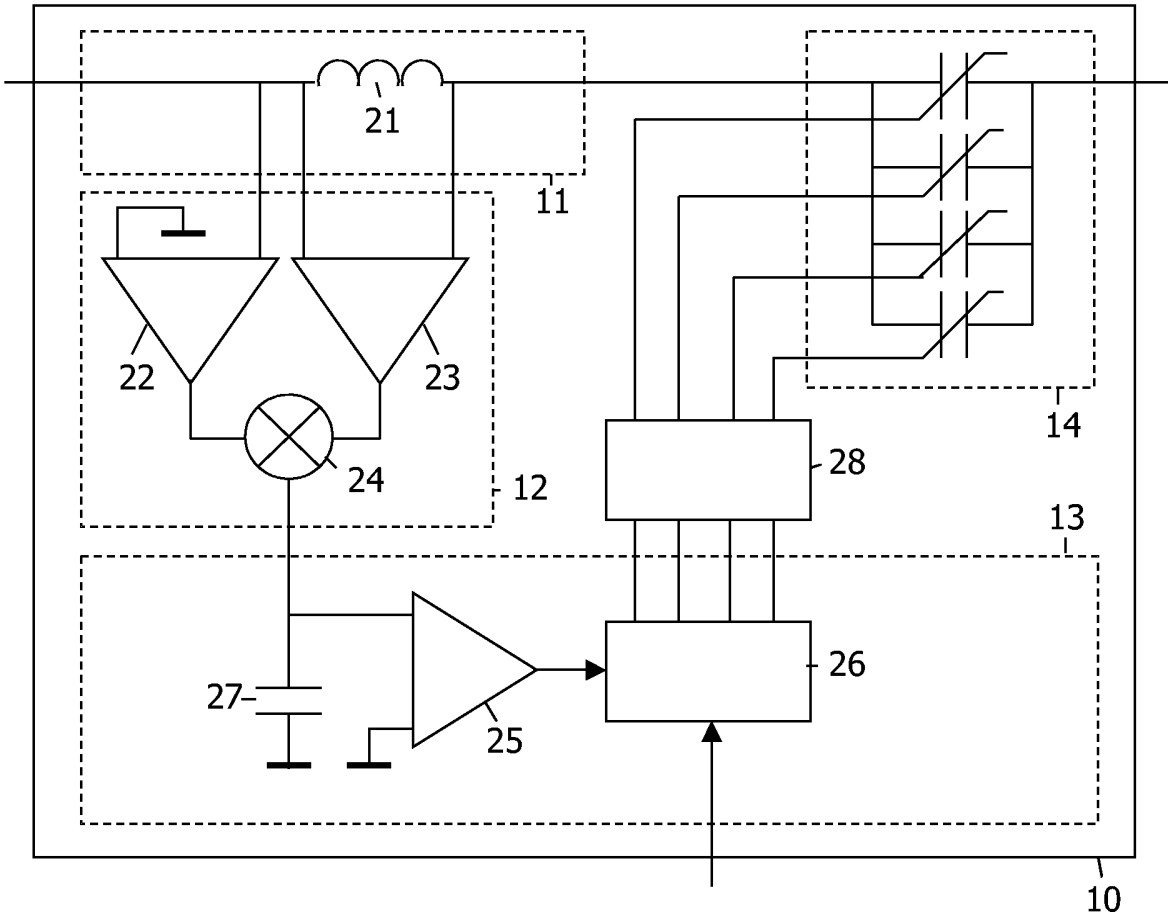

FIG.4

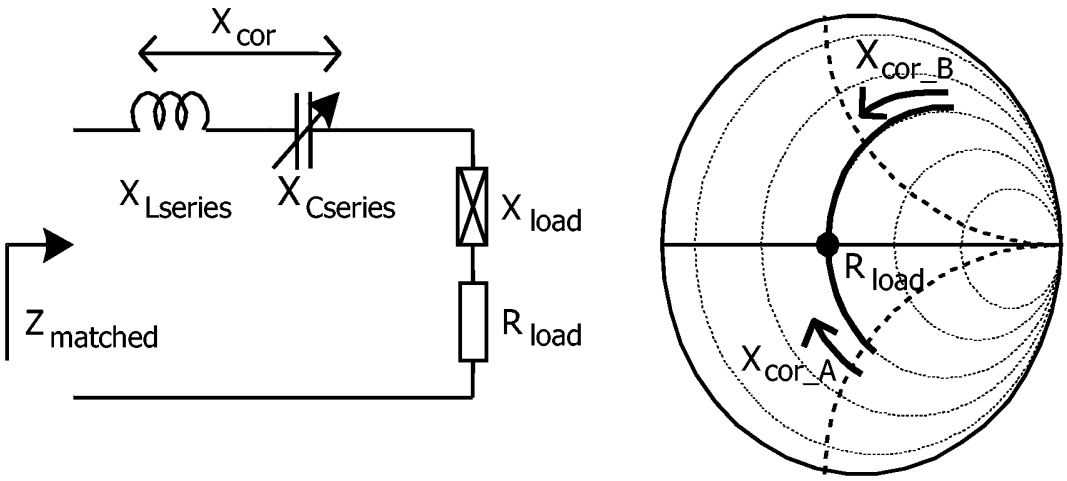
X cor
X Lseries
X Cseries
X load
R load
Z matched
X cor_B
R load
X cor_A

FIG.5

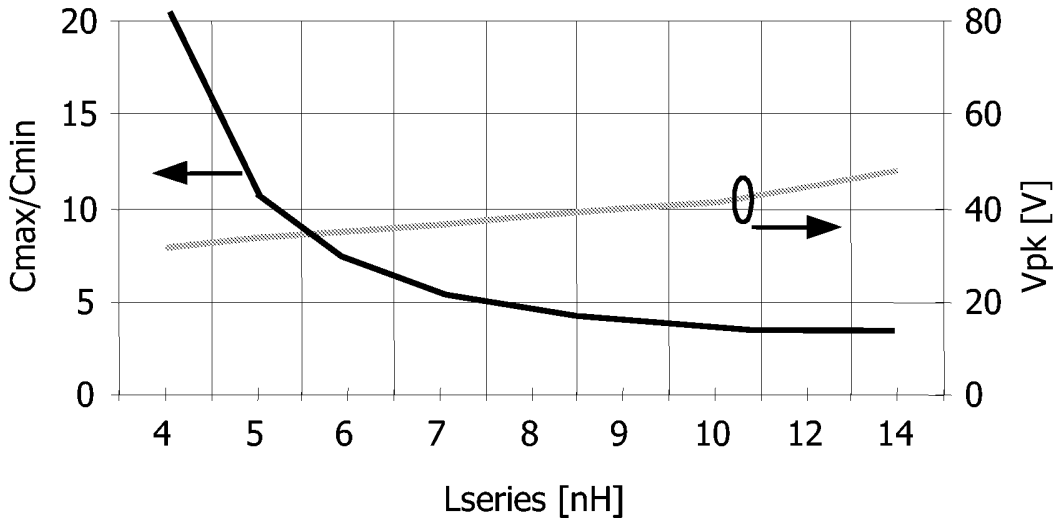
20
15
10
5
0
Cmax/Cmin
80
60
40
20
0
Vpk [V]
4
5
6
7
8
9
10
12
14
Lseries [nH]

FIG.6

INTERNATIONAL SEARCH REPORT

International application No
PCT/IB2005/053777

A. CLASSIFICATION OF SUBJECT MATTER
H04B1/04 H04B1/18

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H04B

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the International search (name of data base and, where practical, search terms used)
EPO-Internal, WPI Data, PAJ

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	WO 02/063782 A (ERICSSON INC; DENT, PAUL, W; HOLSHOUSER, HOWARD, EUGENE; PHILLIPS, JOH) 15 August 2002 (2002-08-15) cited in the application page 3, line 12 - page 7, line 5; figures 7-10 page 18, line 3 - page 25, column 5 -/--	1-12

[X] Further documents are listed in the continuation of Box C. [X] See patent family annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
23 February 2006	01/03/2006

Name and mailing address of the ISA/	Authorized officer
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Form PCT/ISA/210 (second sheet) (April 2005)

INTERNATIONAL SEARCH REPORT

International application No
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C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
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