(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
6 September 2013 (06.09.2013)

WIPO | PCT

(10) International Publication Number
WO 2013/131051 A1

(51) International Patent Classification:
H04B 1/00 (2006.01) *H04B 1/48* (2006.01)

(21) International Application Number:
PCT/US2013/028742

(22) International Filing Date:
1 March 2013 (01.03.2013)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
13/411,444 2 March 2012 (02.03.2012) US

(71) Applicant: **QUALCOMM INCORPORATED** [US/US]; Attn: International IP Administration, 5775 Morehouse Drive, San Diego, California 92121 (US).

(72) Inventors: **GUDEM, Prasad Srinivasa Siva**; 5775 Morehouse Drive, San Diego, California 92121 (US). **SAHOTA, Gurkanwal Singh**; 5775 Morehouse Drive, San Diego, California 92121 (US). **CHANG, Li-Chung**; 5775 Morehouse Drive, San Diego, California 92121 (US). **HOLENSTEIN, Christian**; 5775 Morehouse Drive, San Diego, California 92121 (US). **BOSSU, Frederic**; 5775 Morehouse Drive, San Diego, California 92121 (US).

(74) Agent: **HOOKS, William M.**; Attn: International IP Administration, 5775 Morehouse Drive, San Diego, Califonia 92121 (US).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Declarations under Rule 4.17:

— *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))*

— *as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))*

Published:

— *with international search report (Art. 21(3))*

[Continued on next page]

(54) Title: SINGLE-CHIP SIGNAL SPLITTING CARRIER AGGREGATION RECEIVER ARCHITECTURE

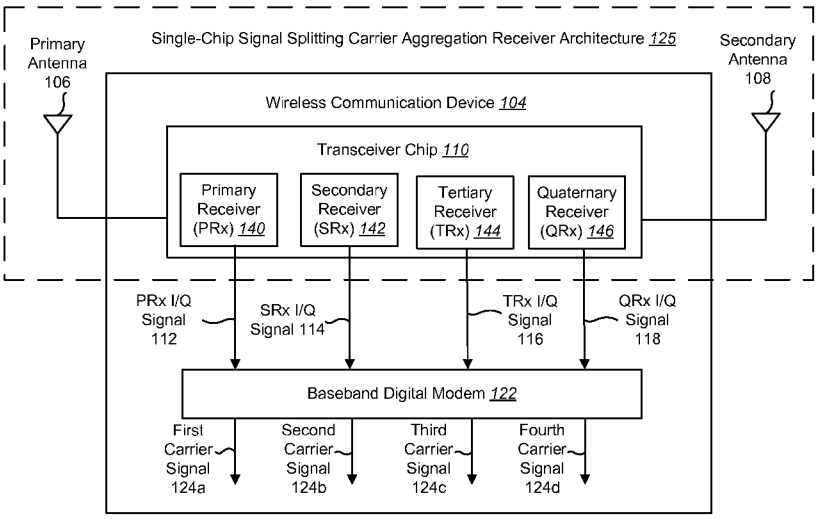

FIG. 1

(57) Abstract: A wireless communication device configured for receiving a multiple carrier signal is described. The wireless communication device includes a single-chip signal splitting carrier aggregation receiver architecture. The single-chip signal splitting carrier aggregation receiver architecture includes a primary antenna, a secondary antenna and a transceiver chip. The single-chip signal splitting carrier aggregation receiver architecture reuses a simultaneous hybrid dual receiver path.

WO 2013/131051 A1

— *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments (Rule 48.2(h))*

SINGLE-CHIP SIGNAL SPLITTING CARRIER AGGREGATION RECEIVER ARCHITECTURE

TECHNICAL FIELD

[0001] The present disclosure relates generally to wireless devices for communication systems. More specifically, the present disclosure relates to systems and methods for a single-chip signal splitting carrier aggregation receiver architecture.

BACKGROUND

[0002] Electronic devices (cellular telephones, wireless modems, computers, digital music players, Global Positioning System units, Personal Digital Assistants, gaming devices, etc.) have become a part of everyday life. Small computing devices are now placed in everything from automobiles to housing locks. The complexity of electronic devices has increased dramatically in the last few years. For example, many electronic devices have one or more processors that help control the device, as well as a number of digital circuits to support the processor and other parts of the device.

[0003] These electronic devices may communicate wirelessly with each other and with a network. As the demand for information by these electronic devices has increased, the downlink throughput has also increased. One such way to increase downlink throughput is the use of carrier aggregation. In carrier aggregation, multiple carriers may be aggregated on the physical layer to provide the required bandwidth (and thus the required throughput).

[0004] It may be desirable for an electronic device to maximize battery life. Because an electronic device often runs on a battery with a limited operation time, reductions in the power consumption of an electronic device may increase the desirability and functionality of the electronic device.

[0005] The electronic devices have also become smaller and cheaper. To facilitate both the decrease in size and the decrease in cost, additional circuitry and more complex circuitry are being used on integrated circuits. Thus, any reduction in the die area used by circuitry may reduce both the size and cost of an electronic device. Benefits may be

realized by improvements to electronic devices that allow an electronic device to participate in carrier aggregation while minimizing the cost and size of the electronic device while also minimizing the power consumption of the electronic device.

SUMMARY

[0006] A wireless communication device configured for receiving a multiple carrier signal is described. The wireless communication device includes a single-chip signal splitting carrier aggregation receiver architecture. The single-chip signal splitting carrier aggregation receiver architecture includes a primary antenna, a secondary antenna and a transceiver chip. The single-chip signal splitting carrier aggregation receiver architecture reuses a simultaneous hybrid dual receiver path.

[0007] The single-chip signal splitting carrier aggregation receiver architecture may not require four antennas, a power splitter, an external low noise amplifier or die-to-die signal routing. The transceiver chip may include a transmitter, a primary receiver, a secondary receiver, a tertiary receiver and a quaternary receiver. Each receiver may include multiple low noise amplifiers. Each low noise amplifier may include a first stage amplifier and a second stage amplifier. The first stage amplifier may be a transconductance stage and the second stage amplifier may be a cascode stage.

[0008] The multiple low noise amplifiers may include multiple low noise amplifiers for a first band and multiple low noise amplifiers for a second band. In one configuration, the first band may be a low band and the second band may be a mid band. In another configuration, the first band may be a low band and the second band may be a high band. In yet another configuration, the first band may be a mid band and the second band may be a high band.

[0009] A first routing may be used from the primary antenna through the primary receiver to obtain a primary inphase/quadrature signal. A second routing may be used from the primary antenna through the tertiary receiver to obtain a TRx inphase/quadrature signal. A third routing may be used from the secondary antenna through the secondary receiver to obtain a secondary inphase/quadrature signal. A fourth routing may be used from the secondary antenna through the quaternary receiver to obtain a QRx inphase/quadrature signal.

[0010] The single-chip signal splitting carrier aggregation receiver architecture may be in inter-band operation. The first routing may pass through a first primary receiver low noise amplifier. The second routing may pass through a second primary receiver low noise amplifier. The second routing may also pass through a first signal splitting stage. The third routing may pass through a first secondary receiver low noise amplifier. The fourth routing may pass through a second secondary receiver low noise amplifier. The fourth routing may also pass through a second signal splitting stage.

[0011] The first signal splitting stage may include a routing between a first stage amplifier in a low noise amplifier of the primary receiver and a second stage amplifier in a low noise amplifier of the tertiary receiver. The second signal splitting stage may include a routing between a first stage amplifier in a low noise amplifier of the secondary receiver and a second stage amplifier in a low noise amplifier of the quaternary receiver.

[0012] The first signal splitting stage may include a routing between a second stage amplifier in a low noise amplifier of the primary receiver and a mixer in the tertiary receiver. The second signal splitting stage may include a routing between a second stage amplifier in a low noise amplifier of the secondary receiver and a mixer in the quaternary receiver.

[0013] The single-chip signal splitting carrier aggregation receiver architecture may be in intra-band operation. The first routing and the second routing may pass through a primary receiver low noise amplifier. The second routing may also pass through a first signal splitting stage. The third routing and the fourth routing may pass through a secondary receiver low noise amplifier. The fourth routing may also pass through a second signal splitting stage.

[0014] The first signal splitting stage may include a routing between a first stage amplifier in a low noise amplifier of the primary receiver and a second stage amplifier in a low noise amplifier of the tertiary receiver. The second signal splitting stage may include a routing between a first stage amplifier in a low noise amplifier of the secondary receiver and a second stage amplifier in a low noise amplifier of the quaternary receiver.

[0015] The first signal splitting stage may include a routing between a second stage amplifier in a low noise amplifier of the primary receiver and a mixer in the tertiary

receiver. The second signal splitting stage may include a routing between a second stage amplifier in a low noise amplifier of the secondary receiver and a mixer in the quaternary receiver.

[0016] A method for receiving a multiple carrier signal using a single-chip signal splitting carrier aggregation receiver architecture is also described. A first signal is received using a primary antenna. The first signal is routed through a primary receiver on a transceiver chip in the single-chip signal splitting carrier aggregation receiver architecture to obtain a primary inphase/quadrature signal. The first signal is routed through a tertiary receiver on the transceiver chip to obtain a TRx inphase/quadrature signal. A second signal is received using a secondary antenna. The second signal is routed through a secondary receiver on the transceiver chip to obtain a secondary inphase/quadrature signal. The second signal is routed through a quaternary receiver on the transceiver chip to obtain a QRx inphase/quadrature signal.

[0017] An apparatus for receiving a multiple carrier signal using a single-chip signal splitting carrier aggregation receiver architecture is described. The apparatus includes means for receiving a first signal using a primary antenna. The apparatus also includes means for routing the first signal through a primary receiver on a transceiver chip in the single-chip signal splitting carrier aggregation receiver architecture to obtain a primary inphase/quadrature signal. The apparatus further includes means for routing the first signal through a tertiary receiver on the transceiver chip to obtain a TRx inphase/quadrature signal. The apparatus also includes means for receiving a second signal using a secondary antenna. The apparatus further includes means for routing the second signal through a secondary receiver on the transceiver chip to obtain a secondary inphase/quadrature signal. The apparatus also includes means for routing the second signal through a quaternary receiver on the transceiver chip to obtain a QRx inphase/quadrature signal.

BRIEF DESCRIPTION OF THE DRAWINGS

[0018] Figure 1 shows a wireless communication device for use in the present systems and methods;

[0019] Figure 2 is a flow diagram of a method for receiving signals using a single-chip signal splitting carrier aggregation receiver architecture;

[0020] Figure 3 is a block diagram illustrating a single-chip signal splitting carrier aggregation receiver architecture;

[0021] Figure 4 is a block diagram illustrating a single-chip signal splitting carrier aggregation receiver architecture operating in inter-band mode;

[0022] Figure 5 is another block diagram illustrating a single-chip signal splitting carrier aggregation receiver architecture operating in inter-band mode;

[0023] Figure 6 is a block diagram illustrating a single-chip signal splitting carrier aggregation receiver architecture operating in intra-band mode;

[0024] Figure 7 is another block diagram illustrating a single-chip signal splitting carrier aggregation receiver architecture operating in intra-band mode;

[0025] Figure 8 is a block diagram illustrating a signal splitting stage;

[0026] Figure 9 is a block diagram illustrating another signal splitting stage; and

[0027] Figure 10 illustrates certain components that may be included within a wireless communication device.

DETAILED DESCRIPTION

[0028] The 3rd Generation Partnership Project (3GPP) is a collaboration between groups of telecommunications associations that aims to define a globally applicable 3rd generation (3G) mobile phone specification. 3GPP Long Term Evolution (LTE) is a 3GPP project aimed at improving the Universal Mobile Telecommunications System (UMTS) mobile phone standard. The 3GPP may define specifications for the next generation of mobile networks, mobile systems and mobile devices. In 3GPP LTE, a mobile station or device may be referred to as a "user equipment" (UE).

[0029] 3GPP specifications are based on evolved Global System for Mobile Communications (GSM) specifications, which are generally known as the Universal Mobile Telecommunications System (UMTS). 3GPP standards are structured as releases. Discussion of 3GPP thus frequently refers to the functionality in one release or another. For example, Release 99 specifies the first UMTS third generation (3G) networks, incorporating a CDMA air interface. Release 6 integrates operation with wireless local area networks (LAN) networks and adds High Speed Uplink Packet Access (HSUPA). Release 8 introduces dual downlink carriers and Release 9 extends dual carrier operation to uplink for UMTS.

[0030] CDMA2000 is a family of 3rd generation (3G) technology standards that use code division multiple access (CDMA) to send voice, data and signaling between wireless devices. CDMA2000 may include CDMA2000 1X, CDMA2000 EV-DO Rev. 0, CDMA2000 EV-DO Rev. A and CDMA2000 EV-DO Rev. B. 1x or 1xRTT refers to the core CDMA2000 wireless air interface standard. 1x more specifically refers to 1 times Radio Transmission Technology and indicates the same radio frequency (RF) bandwidth as used in IS-95. 1xRTT adds 64 additional traffic channels to the forward link. EV-DO refers to Evolution-Data Optimized. EV-DO is a telecommunications standard for the wireless transmission of data through radio signals.

[0031] Figure 1 shows a wireless communication device 104 for use in the present systems and methods. A wireless communication device 104 may also be referred to as, and may include some or all of the functionality of, a terminal, an access terminal, a user equipment (UE), a subscriber unit, a station, etc. A wireless communication device 104 may be a cellular phone, a personal digital assistant (PDA), a wireless device, a wireless modem, a handheld device, a laptop computer, a PC card, compact flash, an external or internal modem, a wireline phone, etc. A wireless communication device 104 may be mobile or stationary. A wireless communication device 104 may communicate with zero, one or multiple base stations on a downlink and/or an uplink at any given moment. The downlink (or forward link) refers to the communication link from a base station to a wireless communication device 104, and the uplink (or reverse link) refers to the communication link from a wireless communication device 104 to a base station. Uplink and downlink may refer to the communication link or to the carriers used for the communication link.

[0032] A wireless communication device 104 may operate in a wireless communication system that includes other wireless devices, such as base stations. A base station is a station that communicates with one or more wireless communication devices 104. A base station may also be referred to as, and may include some or all of the functionality of, an access point, a broadcast transmitter, a Node B, an evolved Node B, etc. Each base station provides communication coverage for a particular geographic area. A base station may provide communication coverage for one or more wireless communication devices 104. The term "cell" can refer to a base station and/or its coverage area, depending on the context in which the term is used.

[0033] Communications in a wireless communication system (e.g., a multiple-access system) may be achieved through transmissions over a wireless link. Such a communication link may be established via a single-input and single-output (SISO) or a multiple-input and multiple-output (MIMO) system. A multiple-input and multiple-output (MIMO) system includes transmitter(s) and receiver(s) equipped, respectively, with multiple (NT) transmit antennas and multiple (NR) receive antennas for data transmission. SISO systems are particular instances of a multiple-input and multiple-output (MIMO) system. The multiple-input and multiple-output (MIMO) system can provide improved performance (e.g., higher throughput, greater capacity or improved reliability) if the additional dimensionalities created by the multiple transmit and receive antennas are utilized.

[0034] The wireless communication system may utilize both single-input and multiple-output (SIMO) and multiple-input and multiple-output (MIMO). The wireless communication system may be a multiple-access system capable of supporting communication with multiple wireless communication devices 104 by sharing the available system resources (e.g., bandwidth and transmit power). Examples of such multiple-access systems include code division multiple access (CDMA) systems, wideband code division multiple access (W-CDMA) systems, time division multiple access (TDMA) systems, frequency division multiple access (FDMA) systems, orthogonal frequency division multiple access (OFDMA) systems, single-carrier frequency division multiple access (SC-FDMA) systems, 3rd Generation Partnership Project (3GPP) Long Term Evolution (LTE) systems and spatial division multiple access (SDMA) systems.

[0035] The wireless communication device 104 may utilize signal splitting. In signal splitting, signals are directed to a specific path. One form of signal splitting is current steering. In one configuration of intra-band carrier aggregation, signal splitting refers to taking a signal from the output of a first stage amplifier (such as a transconductance stage (Gm)), splitting the signal and piping the signal into two separate second stage amplifiers (such as cascode stages (Cas)) and subsequent mixers for carrier aggregation. In another configuration of intra-band carrier aggregation, signal splitting refers to taking a signal from the output of a second stage amplifier (such as a

cascode stage (Cas)), splitting the signal and piping the signal into two separate mixers for carrier aggregation.

[0036] In one configuration of inter-band carrier aggregation, signal splitting refers to taking a signal output from a first stage amplifier (such as a transconductance stage (Gm)) and steering (or diverting or pumping) the signal into a second stage amplifier (such as a cascode stage (Cas)) and subsequent mixer in a diversity path, to be downconverted using the downconverting circuitry of the diversity receiver. In another configuration of inter-band carrier aggregation, signal splitting refers to taking a signal output from a second stage amplifier (such as a cascode stage (Cas)) and steering (or diverting or pumping) the signal into a subsequent mixer in a diversity path to be downconverted using the downconverting circuitry of the diversity receiver.

[0037] The signal steering herein is current steering. However, voltage steering may also be used. In one configuration of voltage steering for inter-band carrier aggregation, a signal output from a first stage amplifier (such as a transconductance stage (Gm)) may be diverted to a second stage amplifier (such as a cascode stage (Cas)) and subsequent mixer in a diversity path to be downconverted using downconverting circuitry of the diversity receiver. In another configuration of voltage steering for inter-band carrier aggregation, a signal output from a second stage amplifier (such as a cascode stage (Cas)) may be diverted to a subsequent mixer in a diversity path to be downconverted using the downconverting circuitry of the diversity receiver.

[0038] The wireless communication device 104 may include a primary antenna 106 and a secondary antenna 108. The secondary antenna 108 may be referred to as the diversity antenna. A transceiver chip 110 may be coupled to the primary antenna 106 and the secondary antenna 108. The transceiver chip 110 may include a transmitter, a primary receiver (PRx) 140, a secondary receiver (SRx) 142, a tertiary receiver (TRx) 144 and a quaternary receiver (QRx) 146. The primary receiver (PRx) 140 of the transceiver chip 110 may output a PRx inphase/quadrature (I/Q) signal 112 to a baseband digital modem 122 on the wireless communication device 104. The secondary receiver (SRx) 142 of the transceiver chip 110 may output a SRx inphase/quadrature (I/Q) signal 114 to the baseband digital modem 122. The tertiary receiver (TRx) 144 of the transceiver chip 110 may output a TRx inphase/quadrature (I/Q) signal 116 to the baseband digital modem 122. The quaternary receiver (QRx) 146 of the transceiver chip

110 may output a QRx inphase/quadrature (I/Q) signal 118 to the baseband digital modem 122. The configuration of the primary antenna 106, the secondary antenna 108 and the transceiver chip 110 may be referred to as a single-chip signal splitting carrier aggregation receiver architecture 125. The single-chip signal splitting carrier aggregation receiver architecture 125 may be implemented with only a single chip to achieve board area reduction without performance degradation for legacy modes (diversity and simultaneous dual hybrid receiver (SHDR)).

[0039] In general, the single-chip signal splitting carrier aggregation receiver architecture 125 may split the signal received by the primary antenna 106 into the PRx inphase/quadrature (I/Q) signal 112 and the TRx inphase/quadrature (I/Q) signal 116 using a routing between a source low noise amplifier (LNA) in the primary receiver (PRx) 140 and a target low noise amplifier (LNA) in the tertiary receiver (TRx) 144. The routing is discussed in additional detail below in relation to Figure 4, Figure 5, Figure 6 and Figure 7. The single-chip signal splitting carrier aggregation receiver architecture 125 may also split the signal received by the secondary antenna 108 into the SRx inphase/quadrature (I/Q) signal 114 and the QRx inphase/quadrature (I/Q) signal 118 using a routing between a source low noise amplifier (LNA) in the secondary receiver (SRx) 142 and a target low noise amplifier (LNA) in the quaternary receiver (QRx) 146. This routing is also discussed in additional detail below in relation to Figure 4, Figure 5, Figure 6 and Figure 7. As used herein, source low noise amplifier (LNA) refers to a low noise amplifier (LNA) from which a signal routing is taken and target low noise amplifier (LNA) refers to a low noise amplifier (LNA) to which the signal routing is directed.

[0040] There may be many different ways to split the signals (for either or both the signal received by the primary antenna 106 and the signal received by the secondary antenna 108). In one configuration, a signal output from a first stage in the source low noise amplifier (LNA) (e.g., a transconductance stage (Gm)) may be routed to a second stage in the target low noise amplifier (LNA) (e.g., a cascode stage (Cas)). In another configuration, a signal output from a first stage in the source low noise amplifier (LNA) (e.g., a transconductance stage (Gm)) may be routed to a second stage in the target low noise amplifier (LNA) (e.g., a transformer used to split the signal).

[0041] The wireless communication device 104 may use a single-chip signal splitting carrier aggregation receiver architecture 125 that reuses the simultaneous hybrid dual receiver (SHDR) path for carrier aggregation. One advantage of the single-chip signal splitting carrier aggregation receiver architecture 125 of the present systems and methods is the ability to operate using only two antennas. Because a wireless communication device 104 with fewer antennas is cheaper, less bulky and less complicated, a wireless communication device 104 with the minimum number of antennas may be advantageous.

[0042] The wireless communication device 104 of the present systems and methods does not require the use of a power splitter. By removing a power splitter from the wireless communication device 104, the wireless communication device 104 may consume less power. Furthermore, the lack of a power splitter may reduce the cost of the wireless communication device 104 and free up die area. The single-chip signal splitting carrier aggregation receiver architecture 125 of the present systems and methods may also not require the use of external low noise amplifiers (LNAs). External low noise amplifiers (LNAs) may consume large amounts of power and increase the cost of a wireless communication device 104. Another benefit of the single-chip signal splitting carrier aggregation receiver architecture 125 of the present systems and methods is the ability to operate without die-to-die signal routing. Removing die-to-die signal routing may reduce both the complexity and cost of the wireless communication device 104. Removing die-to-die signaling may also allow for optimal placement of antennas on the wireless communication device 104. The single-chip signal splitting carrier aggregation receiver architecture 125 may have only two synthesizers running.

[0043] The baseband digital modem 122 may perform processing on the PRx inphase/quadrature (I/Q) signal 112, the SRx inphase/quadrature (I/Q) signal 114, the TRx inphase/quadrature (I/Q) signal 116 and the QRx inphase/quadrature (I/Q) signal 118. For example, the baseband digital modem 122 may convert the signals to the digital domain using analog-to-digital converters (ADCs) and perform digital processing on the signals using digital signal processors (DSPs). The baseband digital modem 122 may then output a first carrier signal 124a, a second carrier signal 124b, a third carrier signal 124c and a fourth carrier signal 124d. A carrier signal 124 may refer to the carrier that the signal used.

[0044] In one configuration, the first carrier signal 124a and the second carrier signal 124b may be located in a low band while the third carrier signal 124c and the fourth carrier signal 124d are located within a midband. This may be referred to as inter-band operation or Dual-Band 4-Carrier according to Rel-10. Inter-band operation is discussed in additional detail below in relation to Figure 4 and Figure 5 below. In another configuration, the first carrier signal 124a, second carrier signal 124b, third carrier signal 124c and fourth carrier signal 124d may all be located within a single band, such as the low band. This may be referred to as intra-band operation or Single-Band 4-Carrier in Release-10. Intra-band operation is discussed in additional detail below in relation to Figure 6 and Figure 7 below.

[0045] Figure 2 is a flow diagram of a method 200 for receiving signals using a single-chip signal splitting carrier aggregation receiver architecture 125. The method 200 may be performed by a wireless communication device 104. The wireless communication device 104 may be operating in either inter-band mode or intra-band mode. In inter-band mode, the wireless communication device 104 may receive four carrier signals; two within a first band and two within a second band. In intra-band mode, the wireless communication device 104 may receive four carrier signals within a single band.

[0046] The wireless communication device 104 may receive 202 a first signal using a primary antenna 106. The wireless communication device 104 may route 204 the first signal through a primary receiver (PRx) 140 on a transceiver chip 110 to obtain a PRx inphase/quadrature (I/Q) signal 112. The wireless communication device 104 may also route 206 the first signal through a tertiary receiver (TRx) 144 on the transceiver chip 110 to obtain a TRx inphase/quadrature (I/Q) signal 116.

[0047] The wireless communication device 104 may also receive 208 a second signal using a secondary antenna 108. The wireless communication device 104 may route 210 the second signal through a secondary receiver (SRx) 142 on the transceiver chip 110 to obtain a SRx inphase/quadrature (I/Q) signal 114. The wireless communication device 104 may route 212 the second signal through a quaternary receiver (QRx) 146 on the transceiver chip 110 to obtain a QRx inphase/quadrature (I/Q) signal 118.

[0048] Figure 3 is a block diagram illustrating a single-chip signal splitting carrier aggregation receiver architecture 325. The single-chip signal splitting carrier aggregation receiver architecture 325 of Figure 3 may be one configuration of the single-chip signal splitting carrier aggregation receiver architecture 125 of Figure 1. The single-chip signal splitting carrier aggregation receiver architecture 325 may include a primary antenna 306, a first low-pass high-pass diplexer 326a, a first switch 328a, four duplexers 330a-d, a secondary antenna 308, a second low-pass high-pass diplexer 326b, a second switch 328b, four surface acoustic wave (SAW) filters 334a-d and a transceiver chip 310.

[0049] The primary antenna 306 may be coupled to the first low-pass high-pass diplexer 326a. A low-pass high-pass diplexer 326 may bundle low band frequencies into one signal and high band (or midband) frequencies into another signal, thus allowing the primary antenna 306 to pass both low band and midband signals to the transceiver chip 310. The first low-pass high-pass diplexer 326a may be coupled to the first switch 328a. The first switch 328a may have two inputs (the signal that includes the bundled low band frequencies and the signal that includes the bundled high band frequencies) and multiple outputs. In one configuration, the first switch 328a may have six possible outputs to the four duplexers 330 (representing the six possible configurations of duplexer 330 pairs). The four duplexers 330 may include a first duplexer 330a, a second duplexer 330b, a third duplexer 330c and a fourth duplexer 330d. In one configuration, the first duplexer 330a and the second duplexer 330b may be used for a low band while the third duplexer 330c and the fourth duplexer 330d are used for a midband.

[0050] The transceiver chip 310 may include a transmitter 332, a primary receiver (PRx) 340, a secondary receiver (SRx) 342, a tertiary receiver (TRx) 344 and a quaternary receiver (QRx) 346. The transmitter 332 may include four transmit outputs: a first transmit output, a second transmit output, a third transmit output and a fourth transmit output. In one configuration, the first transmit output and the second transmit output may be low band outputs while the third transmit output and the fourth transmit output are midband outputs.

[0051] The first transmit output may be coupled to the first duplexer 330a via a power amplifier (PA) 338a. The second transmit output may be coupled to the second

duplexer 330b via a power amplifier 338b. The third transmit output may be coupled to the third duplexer 330c via a power amplifier 338c. The fourth transmit output may be coupled to the fourth duplexer 330d via a power amplifier 338d.

[0052] The primary receiver (PRx) 340 may include a first PRx low noise amplifier (LNA) 348a coupled to the first duplexer 330a, a second PRx low noise amplifier (LNA) 348b coupled to the second duplexer 330b, a third PRx low noise amplifier (LNA) 348c coupled to the third duplexer 330c and a fourth PRx low noise amplifier (LNA) 348d coupled to the fourth duplexer 330d. In one configuration, the first PRx low noise amplifier (LNA) 348a and the second PRx low noise amplifier (LNA) 348b may be low band low noise amplifiers (LNAs) while the third PRx low noise amplifier (LNA) 348c and the fourth PRx low noise amplifier (LNA) 348d are midband low noise amplifiers (LNAs).

[0053] The primary receiver (PRx) 340 may also include a mixer 356a (e.g., a downconverter). The mixer 356a may be coupled to the output of the first PRx low noise amplifier (LNA) 348a, the output of the second PRx low noise amplifier (LNA) 348b, the output of the third PRx low noise amplifier (LNA) 348c and the output of the fourth PRx low noise amplifier (LNA) 348d.

[0054] The primary receiver (PRx) 340 may include a phase locked loop (PLL) 362a, a PRx voltage controlled oscillator (VCO) 360a and a Div stage 358a that are used to generate the downconverting frequency for the mixer 356a. The output of the mixer 356a may be coupled to a PRx baseband filter (BBF) 364a. The PRx baseband filter (BBF) 364a may then output the PRx inphase/quadrature (I/Q) signal 312. The transceiver chip 310 may include a switch 366 that allows the downconverting frequency generated by the PRx voltage controlled oscillator (VCO) 360 to be used by a mixer 356b in the secondary receiver (SRx) 342, a mixer 356c in the tertiary receiver (TRx) 344 and/or a mixer 356d in the quaternary receiver (QRx) 346.

[0055] The secondary antenna 308 may be coupled to the second low-pass high-pass diplexer 326b. The second low-pass high-pass diplexer 326b may be coupled to the second switch 328b. The second switch 328b may have two inputs (the signal that includes the bundled low band frequencies and the signal that includes the bundled high band frequencies) and multiple outputs. In one configuration, the second switch 328b may have six possible outputs to the four surface acoustic wave (SAW) filters 334

(representing the six possible configurations of surface acoustic wave (SAW) filter 334 pairs). The four surface acoustic wave (SAW) filters 334 may include a first surface acoustic wave (SAW) filter 334a, a second surface acoustic wave (SAW) filter 334b, a third surface acoustic wave (SAW) filter 334c and a fourth surface acoustic wave (SAW) filter 334d. In one configuration, the first surface acoustic wave (SAW) filter 334a and the second surface acoustic wave (SAW) filter 334b may be used for the low band while the third surface acoustic wave (SAW) filter 334c and the fourth surface acoustic wave (SAW) filter 334d are used for the midband.

[0056] The secondary receiver (SRx) 342 may include a first SRx low noise amplifier (LNA) 350a coupled to the first surface acoustic wave (SAW) filter 334a, a second SRx low noise amplifier (LNA) 350b coupled to the second surface acoustic wave (SAW) filter 334b, a third SRx low noise amplifier (LNA) 350c coupled to the third surface acoustic wave (SAW) filter 334c and a fourth SRx low noise amplifier (LNA) 350d coupled to the fourth surface acoustic wave (SAW) filter 334d. In one configuration, the first SRx low noise amplifier (LNA) 350a and the second SRx low noise amplifier (LNA) 350b may be low band low noise amplifiers (LNAs) while the third SRx low noise amplifier (LNA) 350c and the fourth SRx low noise amplifier (LNA) 350d are midband low noise amplifiers (LNAs).

[0057] The secondary receiver (SRx) 342 may include a mixer 356b coupled to the output of the first SRx low noise amplifier (LNA) 350a, the output of the second SRx low noise amplifier (LNA) 350b, the output of the third SRx low noise amplifier (LNA) 350c and the output of the fourth SRx low noise amplifier (LNA) 350d. The secondary receiver (SRx) 342 may also include a phase locked loop (PLL) 362b, a SRx voltage controlled oscillator (VCO) 361 and a Div stage 358b that are used to generate a downconverting frequency for the mixer 356b. In one configuration, the switch 366 on the transceiver chip 310 may be set so that the Div stage 358b receives the downconverting frequency generated by the PRx voltage controlled oscillator (VCO) 360 from the primary receiver (PRx) 340. The output of the mixer 356b may be coupled to an SRx baseband filter (BBF) 364b. The SRx baseband filter (BBF) 364b may then output the SRx inphase/quadrature (I/Q) signal 314.

[0058] The tertiary receiver (TRx) 344 may include a first TRx low noise amplifier (LNA) 352a, a second TRx low noise amplifier (LNA) 352b, a third TRx low noise

amplifier (LNA) 352c and a fourth TRx low noise amplifier (LNA) 352d. In one configuration, the first TRx low noise amplifier (LNA) 352a and the second TRx low noise amplifier (LNA) 352b may be low band low noise amplifiers (LNAs) while the third TRx low noise amplifier (LNA) 352c and the fourth TRx low noise amplifier (LNA) 352d are midband low noise amplifiers (LNAs). The inputs to the first TRx low noise amplifier (LNA) 352a, the second TRx low noise amplifier (LNA) 352b, the third TRx low noise amplifier (LNA) 352c and the fourth TRx low noise amplifier (LNA) 352d may be disabled.

[0059] The tertiary receiver (TRx) 344 may include a mixer 356c coupled to the outputs of the first TRx low noise amplifier (LNA) 352a, the second TRx low noise amplifier (LNA) 352b, the third TRx low noise amplifier (LNA) 352c and the fourth TRx low noise amplifier (LNA) 352d. The tertiary receiver (TRx) 344 may also include a Div stage 358c coupled to the mixer 356c. The Div stage 358c may be coupled to the switch 366 on the transceiver chip 310. In one configuration, the switch 366 may be set so that the Div stage 358c may receive the downconverting frequency generated by the PRx voltage controlled oscillator (VCO) 360 from the primary receiver (PRx) 340. In another configuration, the switch 366 may be set so that the Div stage 358c receives the downconverting frequency generated by the SRx voltage controlled oscillator (VCO) 361. The output of the mixer 356c may be coupled to a TRx baseband filter (BBF) 364c. The TRx baseband filter (BBF) 364c may then output the TRx inphase/quadrature (I/Q) signal 316.

[0060] The quaternary receiver (QRx) 346 may include a first QRx low noise amplifier (LNA) 354a, a second QRx low noise amplifier (LNA) 354b, a third QRx low noise amplifier (LNA) 354c and a fourth QRx low noise amplifier (LNA) 354d. In one configuration, the first QRx low noise amplifier (LNA) 354a and the second QRx low noise amplifier (LNA) 354b may be low band low noise amplifiers (LNAs) while the third QRx low noise amplifier (LNA) 354c and the fourth QRx low noise amplifier (LNA) 354d are midband low noise amplifiers (LNAs). The inputs to the first QRx low noise amplifier (LNA) 354a, the second QRx low noise amplifier (LNA) 354b, the third QRx low noise amplifier (LNA) 354c and the fourth QRx low noise amplifier (LNA) 354d may be disabled.

[0061] The quaternary receiver (QRx) 346 may include a mixer 356d coupled to the outputs of the first QRx low noise amplifier (LNA) 354a, the second QRx low noise amplifier (LNA) 354b, the third QRx low noise amplifier (LNA) 354c and the fourth QRx low noise amplifier (LNA) 354d. The quaternary receiver (QRx) 346 may also include a Div stage 358d coupled to the mixer 356d. The Div stage 358d may be coupled to the switch 366 on the transceiver chip 310. In one configuration, the switch 366 may be set so that the Div stage 358d may receive the downconverting frequency generated by the PRx voltage controlled oscillator (VCO) 360 from the primary receiver (PRx) 340. In another configuration, the switch 366 may be set so that the Div stage 358d receives the downconverting frequency generated by the SRx voltage controlled oscillator (VCO) 361 from the secondary receiver (SRx) 342. The output of the mixer 356d may be coupled to a QRx baseband filter (BBF) 364d. The QRx baseband filter (BBF) 364d may then output the QRx inphase/quadrature (I/Q) signal 318.

[0062] Figure 4 is a block diagram illustrating a single-chip signal splitting carrier aggregation receiver architecture 425 operating in inter-band mode. The single-chip signal splitting carrier aggregation receiver architecture 425 of Figure 4 may be one configuration of the single-chip signal splitting carrier aggregation receiver architecture 124 of Figure 1. The single-chip signal splitting carrier aggregation receiver architecture 425 may include a primary antenna 406, a secondary antenna 408 and a transceiver chip 410. The primary antenna 406 and the secondary antenna 408 may be used to receive a dual-band 4-carrier signal (i.e., four carriers 474a-d over a first band 470 and a second band 472 (the first band 470 and the second band 472 are separated from each other)).

[0063] The transceiver chip 410 may include a transmitter 432, a primary receiver (PRx) 440, a secondary receiver (SRx) 442, a tertiary receiver (TRx) 444 and a quaternary receiver (QRx) 446. The primary antenna 406 may be coupled to PRx circuitry 468a of the primary receiver (PRx) 440. The PRx circuitry 468a may include the PRx low noise amplifiers (LNAs) 348a-d, downconverting circuitry and the PRx baseband filter (BBF) 364a. The PRx circuitry 468a may output a PRx inphase/quadrature (I/Q) signal 412 that includes the first carrier 474a and the second carrier 474b in the first band 470.

[0064] The transceiver chip 410 may include a routing 435a from the PRx circuitry 468a to TRx circuitry 468c in the tertiary receiver (TRx) 444. In one configuration, the routing 435a may be from a first stage amplifier in a PRx low noise amplifier (LNA) 348 of the PRx circuitry 468a to the TRx circuitry 468c. In another configuration, the routing 435a may be output from a second stage amplifier in a PRx low noise amplifier (LNA) 348 of the PRx circuitry 438a. The TRx circuitry 468c may include the TRx low noise amplifiers (LNAs) 352a-d, the downconverting circuitry and the TRx baseband filter (BBF) 364c. In one configuration, the routing 435 from the PRx circuitry 468a may be input to a second stage amplifier in a TRx low noise amplifier (LNA) 352 of the TRx circuitry 468c. In another configuration, the routing 435a from the PRx circuitry 468a may be input to a mixer 356c of the tertiary receiver (TRx) 444. The TRx circuitry 468c may output a TRx inphase/quadrature (I/Q) signal 416 that includes the third carrier 474c and the fourth carrier 474d in the second band 472.

[0065] The secondary antenna 408 may be coupled to SRx circuitry 468b of the secondary receiver (SRx) 442. The SRx circuitry 468b may include the SRx low noise amplifiers (LNAs) 350a-d, the downconverting circuitry and the SRx baseband filter (BBF) 364b. The SRx circuitry 468b may output a SRx inphase/quadrature (I/Q) signal 414 that includes the first carrier 474a and the second carrier 474b in the first band 470.

[0066] The transceiver chip 410 may include a routing 435b from the SRx circuitry 468b to QRx circuitry 468d in the quaternary receiver (QRx) 446. In one configuration, the routing 435b may be output from a first stage amplifier in a SRx low noise amplifier (LNA) 350 of the SRx circuitry 468b. In another configuration, the routing 435b may be output from a second stage amplifier in a SRx low noise amplifier (LNA) 350 of the SRx circuitry 468b. The QRx circuitry 468d may include the QRx low noise amplifiers (LNAs) 354a-d, the downconverting circuitry and the QRx baseband filter (BBF) 364d. In one configuration, the routing 435b from the SRx circuitry 468b may be input to a second stage amplifier in a QRx low noise amplifier (LNA) 354 of the QRx circuitry 468d. In another configuration, the routing 435b from the SRx circuitry 468b may be input to a mixer 356d of the quaternary receiver (QRx) 446. The QRx circuitry 468d may output a QRx inphase/quadrature (I/Q) signal 418 that includes the third carrier 474c and the fourth carrier 474d in the second band 472.

[0067] The routing 435a from the PRx circuitry 468a to the TRx circuitry 468c may be part of a first signal splitting stage 433a. The routing from the SRx circuitry 468b to the QRx circuitry 468b may be part of a second signal splitting stage 433b. The signal splitting stages 433a-b are discussed in additional detail below in relation to Figure 8 and Figure 9.

[0068] Figure 5 is another block diagram illustrating a single-chip signal splitting carrier aggregation receiver architecture 325 operating in inter-band mode. The single-chip signal splitting carrier aggregation receiver architecture 325 of Figure 5 may be the single-chip signal splitting carrier aggregation receiver architecture 325 of Figure 3. The primary antenna 306 and the secondary antenna 308 may be used to receive a dual-band 4-carrier signal (i.e., four carriers 474a-d over two separate bands). A routing 537 from the primary antenna 306 through the primary receiver (PRx) 340 to obtain the PRx inphase/quadrature (I/Q) signal 314 is shown. The routing 537 may pass through the first PRx low noise amplifier (LNA) 348a. The PRx inphase/quadrature (I/Q) signal 314 may include a first carrier 474a and a second carrier 474b from a first band 470 for this configuration.

[0069] A routing 535a from the primary antenna 306 through the tertiary receiver (TRx) 344 to obtain the TRx inphase/quadrature (I/Q) signal 316 is also shown. The TRx inphase/quadrature (I/Q) signal 316 may include a third carrier 474c and a fourth carrier 474d from a second band 472. The routing 535a from the primary antenna 306 through the tertiary receiver (TRx) 344 to obtain the TRx inphase/quadrature (I/Q) signal 316 may pass through a first signal splitting stage 433a. The first signal splitting stage 433a may allow the single-chip signal splitting carrier aggregation receiver architecture 325 to reuse the simultaneous hybrid dual receiver (SHDR) receiver path.

[0070] The first signal splitting stage 433a may include the routing 535a from the third PRx low noise amplifier (LNA) 348c in the primary receiver (PRx) 340 to the third TRx low noise amplifier (LNA) 352c in the tertiary receiver (TRx) 344. In one configuration, the routing 535a may be output from a first amplifier stage (e.g., a transconductance stage (Gm)) of the third PRx low noise amplifier (LNA) 348c and input to a second amplifier stage (e.g., a cascode stage (Cas)) of the third TRx low noise amplifier (LNA) 352c. In another configuration, the routing 535a may be output from a

second amplifier stage (e.g., a cascode stage (Cas)) of the third PRx low noise amplifier (LNA) 348c and input to the mixer 356c in the tertiary receiver (TRx) 344.

[0071] A routing 539 from the secondary antenna 308 through the secondary receiver (SRx) 342 to obtain the SRx inphase/quadrature (I/Q) signal 316 is also shown. The routing 539 may pass through the first SRx low noise amplifier (LNA) 350a. The SRx inphase/quadrature (I/Q) signal 314 may include a first carrier 474a and a second carrier 474b from the first band 470 for this configuration. A routing 535b from the secondary antenna 308 through the quaternary receiver (QRx) 346 to obtain the QRx inphase/quadrature (I/Q) signal 318 is also shown. The QRx inphase/quadrature (I/Q) signal 318 may include a third carrier 474c and a fourth carrier 474d from the second band 472. The routing 535b from the secondary antenna 308 through the quaternary receiver (QRx) 346 to obtain the QRx inphase/quadrature (I/Q) signal 318 may pass through a second signal splitting stage 433b. The second signal splitting stage 433b may also allow the single-chip signal splitting carrier aggregation receiver architecture 325 to reuse the simultaneous hybrid dual receiver (SHDR) receiver path.

[0072] The second signal splitting stage 433b may route 535b a signal from the third SRx low noise amplifier (LNA) 350c in the secondary receiver (SRx) 342 to the third QRx low noise amplifier (LNA) 354c in the quaternary receiver (QRx) 346. In one configuration, the routing 535b may be the output of a first amplifier stage (e.g., a transconductance stage (Gm)) of the third SRx low noise amplifier (LNA) 350c to the input of a second amplifier stage (e.g., a cascode stage (Cas)) of the third QRx low noise amplifier (LNA) 354c. In another configuration, the routing 535b may be the output of a second amplifier stage (e.g., a cascode stage (Cas)) of the third SRx low noise amplifier (LNA) 350c to the input of the mixer 356d in the quaternary receiver (QRx) 346.

[0073] Figure 6 is a block diagram illustrating a single-chip signal splitting carrier aggregation receiver architecture 625 operating in intra-band mode. The single-chip signal splitting carrier aggregation receiver architecture 625 of Figure 6 may be one configuration of the single-chip signal splitting carrier aggregation receiver architecture 124 of Figure 1. The single-chip signal splitting carrier aggregation receiver architecture 625 may include a primary antenna 606, a secondary antenna 608 and a transceiver chip 610. The primary antenna 606 and the secondary antenna 608 may be

used to receive a single-band 4-carrier signal (i.e., four carriers 674a-d over a first band 670).

[0074] The transceiver chip 610 may include a transmitter 632, a primary receiver (PRx) 640, a secondary receiver (SRx) 642, a tertiary receiver (TRx) 644 and a quaternary receiver (QRx) 646. The primary antenna 606 may be coupled to PRx circuitry 668a of the primary receiver (PRx) 640. The PRx circuitry 668a may include the PRx low noise amplifiers (LNAs) 348a-d, downconverting circuitry and the PRx baseband filter (BBF) 364a. The PRx circuitry 668a may output a PRx inphase/quadrature (I/Q) signal 612 that includes the first carrier 674a and the second carrier 674b in the first band 670.

[0075] The transceiver chip 610 may include a routing 635a from the PRx circuitry 668a to TRx circuitry 668c in the tertiary receiver (TRx) 644. In one configuration, the routing 635a may be from a first stage amplifier in a PRx low noise amplifier (LNA) 348 of the PRx circuitry 668a to the TRx circuitry 668c. In another configuration, the routing 635a may be output from a second stage amplifier in a PRx low noise amplifier (LNA) 348 of the PRx circuitry 668a. The TRx circuitry 668c may include the TRx low noise amplifiers (LNAs) 352a-d, the downconverting circuitry and the TRx baseband filter (BBF) 364c. In one configuration, the routing 635 from the PRx circuitry 668a may be input to a second stage amplifier in a TRx low noise amplifier (LNA) 352 of the TRx circuitry 668c. In another configuration, the routing 635a from the PRx circuitry 668a may be input to a mixer 356c of the tertiary receiver (TRx) 644. The TRx circuitry 668c may output a TRx inphase/quadrature (I/Q) signal 616 that includes the third carrier 674c and the fourth carrier 674d in the first band 670.

[0076] The secondary antenna 608 may be coupled to SRx circuitry 668b of the secondary receiver (SRx) 642. The SRx circuitry 668b may include the SRx low noise amplifiers (LNAs) 350a-d, the downconverting circuitry and the SRx baseband filter (BBF) 364b. The SRx circuitry 668b may output a SRx inphase/quadrature (I/Q) signal 614 that includes the first carrier 674a and the second carrier 674b in the first band 670.

[0077] The transceiver chip 610 may include a routing 635b from the SRx circuitry 668b to QRx circuitry 668d in the quaternary receiver (QRx) 646. In one configuration, the routing 635b may be output from a first stage amplifier in a SRx low noise amplifier (LNA) 350 of the SRx circuitry 668b. In another configuration, the routing 635b may

be output from a second stage amplifier in a SRx low noise amplifier (LNA) 350 of the SRx circuitry 668b. The QRx circuitry 668d may include the QRx low noise amplifiers (LNAs) 354a-d, the downconverting circuitry and the QRx baseband filter (BBF) 364d. In one configuration, the routing 635b from the SRx circuitry 668b may be input to a second stage amplifier in a QRx low noise amplifier (LNA) 354 of the QRx circuitry 668d. In another configuration, the routing 635b from the SRx circuitry 668b may be input to a mixer 356d of the quaternary receiver (QRx) 646. The QRx circuitry 668d may output a QRx inphase/quadrature (I/Q) signal 618 that includes the third carrier 674c and the fourth carrier 674d in the first band 670.

[0078] The routing 635a from the PRx circuitry 668a to the TRx circuitry 668c may be part of a first signal splitting stage 633a. The routing from the SRx circuitry 668b to the QRx circuitry 668b may be part of a second signal splitting stage 633b. The signal splitting stages 633a-b are discussed in additional detail below in relation to Figure 8 and Figure 9.

[0079] Figure 7 is another block diagram illustrating a single-chip signal splitting carrier aggregation receiver architecture 325 operating in intra-band mode. The single-chip signal splitting carrier aggregation receiver architecture 325 of Figure 7 may be the single-chip signal splitting carrier aggregation receiver architecture 325 of Figure 3. Intra-band mode may require current splitting. A 6 decibel (dB) loss may lead to 0.2 – 0.5 db noise factor (NF) degradation. The low noise amplifiers (LNA) in the radio frequency integrated circuit (RFIC) may need to be designed as mixer Gm.

[0080] The primary antenna 306 and the secondary antenna 308 may be used to receive a single-band 4-carrier signal (i.e., four carriers 674a-d over a first band 670 and no carriers in a second band 672). A routing 737 from the primary antenna 306 through the primary receiver (PRx) 340 to obtain the PRx inphase/quadrature (I/Q) signal 314 is shown. The routing 737 may pass through the first PRx low noise amplifier (LNA) 348a. The PRx inphase/quadrature (I/Q) signal 314 may include a first carrier 674a and a second carrier 674b from a first band 670 for this configuration.

[0081] A routing 735a from the primary antenna 306 through the tertiary receiver (TRx) 344 to obtain the TRx inphase/quadrature (I/Q) signal 316 is also shown. The TRx inphase/quadrature (I/Q) signal 316 may include a third carrier 674c and a fourth carrier 674d from the first band 670. The routing 735a from the primary antenna 306

through the tertiary receiver (TRx) 344 to obtain the TRx inphase/quadrature (I/Q) signal 316 may pass through a first signal splitting stage 633a. The first signal splitting stage 633a may allow the single-chip signal splitting carrier aggregation receiver architecture 325 to reuse the simultaneous hybrid dual receiver (SHDR) receiver path.

[0082] The first signal splitting stage 633a may include a routing 735a from the first PRx low noise amplifier (LNA) 348a in the primary receiver (PRx) 340 to the third TRx low noise amplifier (LNA) 352c in the tertiary receiver (TRx) 344. In one configuration, the routing 735a may be output from a first amplifier stage (e.g., a transconductance stage (Gm)) of the first PRx low noise amplifier (LNA) 348a and input to a second amplifier stage (e.g., a cascode stage (Cas)) of the third TRx low noise amplifier (LNA) 352c. In another configuration, the routing 735a may be output from a second amplifier stage (e.g., a cascode stage (Cas)) of the first PRx low noise amplifier (LNA) 348c and input to the mixer 356c in the tertiary receiver (TRx) 344.

[0083] A routing 739 from the secondary antenna 308 through the secondary receiver (SRx) 342 to obtain the SRx inphase/quadrature (I/Q) signal 316 is also shown. The routing 739 may pass through the first SRx low noise amplifier (LNA) 350a. The SRx inphase/quadrature (I/Q) signal 314 may include a first carrier 674a and a second carrier 674b from the first band 670 for this configuration. A routing 735b from the secondary antenna 308 through the quaternary receiver (QRx) 346 to obtain the QRx inphase/quadrature (I/Q) signal 318 is also shown. The QRx inphase/quadrature (I/Q) signal 318 may include a third carrier 674c and a fourth carrier 674d from the first band 670. The routing 735b from the secondary antenna 308 through the quaternary receiver (QRx) 346 to obtain the QRx inphase/quadrature (I/Q) signal 318 may pass through a second signal splitting stage 633b. The second signal splitting stage 633b may also allow the single-chip signal splitting carrier aggregation receiver architecture 325 to reuse the simultaneous hybrid dual receiver (SHDR) receiver path.

[0084] The second signal splitting stage 633b may route 735b a signal from the first SRx low noise amplifier (LNA) 350a in the secondary receiver (SRx) 342 to the third QRx low noise amplifier (LNA) 354c in the quaternary receiver (QRx) 346. In one configuration, the routing 735b may be the output of a first amplifier stage (e.g., a transconductance stage (Gm)) of the first SRx low noise amplifier (LNA) 350a to the input of a second amplifier stage (e.g., a cascode stage (Cas)) of the third QRx low noise

amplifier (LNA) 354c. In another configuration, the routing 735b may be the output of a second amplifier stage (e.g., a cascode stage (Cas)) of the first SRx low noise amplifier (LNA) 350a to the input of the mixer 356d in the quaternary receiver (QRx) 346.

[0085] Figure 8 is a block diagram illustrating a signal splitting stage 833. The signal splitting stage 833 of Figure 8 may be one configuration of the signal splitting stages 433a-b in Figure 4 and the signal splitting stages 633a-b in Figure 6. The signal splitting stage 833 may include a source first stage amplifier 874a and a source second stage amplifier 876a as part of a source low noise amplifier (LNA) 878a, a target first stage amplifier 874b and a target second stage amplifier 876b of a target low noise amplifier (LNA) 878b and passive mixers 856a-d. In one configuration, the source low noise amplifier (LNA) 878a may be a PRx low noise amplifier (LNA) 348 and the target low noise amplifier (LNA) may be a TRx low noise amplifier 352. In another configuration, the source low noise amplifier (LNA) 878a may be an SRx low noise amplifier (LNA) 350 and the target low noise amplifier (LNA) 878b may be a QRx low noise amplifier (LNA) 354.

[0086] In one configuration, the source first stage amplifier 874a and the target first stage amplifier 874b may be transconductance stages (Gm) while the source second stage amplifier 876a and the target second stage amplifier 876b may be cascode stages (Cas). The outputs of the source first stage amplifier 874a may be input to the source second stage amplifier 876a. The outputs of the source second stage amplifier 876a may then be mixed via the passive mixers 856a-b to obtain the source inphase signals 880a-b and the source quadrature signals 880c-d. In the signal splitting stage 833, the signal splitting occurs after the source first stage amplifier 874a. Thus, the outputs of the source first stage amplifier 874a may be input to the inputs of the target second stage amplifier 876b. The outputs of the target second stage amplifier 876b may then be mixed via the passive mixers 856c-d to obtain the target inphase signals 880e-f and the target quadrature signals 880g-h.

[0087] Switches may be used between the source low noise amplifier (LNA) 878a and the target low noise amplifier (LNA) 878b to allow a clean standalone operation. The low noise amplifier (LNA) topology may drive the signal splitting sensing point.

[0088] Figure 9 is a block diagram illustrating another signal splitting stage 933. The signal splitting stage 933 of Figure 9 may be one configuration of the signal

splitting stages 433a-b in Figure 4 and the signal splitting stages 633a-b in Figure 6. The signal splitting stage 933 may include a source first stage amplifier 974a and a source second stage amplifier 976a as part of a source low noise amplifier (LNA) 978a, a target first stage amplifier 974b and a target second stage amplifier 976b of a target low noise amplifier (LNA) 978b and passive mixers 956a-d. In one configuration, the source low noise amplifier (LNA) 978a may be a PRx low noise amplifier (LNA) 348 and the target low noise amplifier (LNA) may be a TRx low noise amplifier 352. In another configuration, the source low noise amplifier (LNA) 978a may be an SRx low noise amplifier (LNA) 350 and the target low noise amplifier (LNA) 978b may be a QRx low noise amplifier (LNA) 354.

[0089] In one configuration, the source first stage amplifier 974a and the target first stage amplifier 974b may be transconductance stages (Gm) while the source second stage amplifier 976a and the target second stage amplifier 976b may be cascode stages (Cas). The outputs of the source first stage amplifier 974a may be input to the source second stage amplifier 976a. The outputs of the source second stage amplifier 976a may then be mixed via the passive mixers 956a-b to obtain the source inphase signals 980a-b and the source quadrature signals 980c-d. In the signal splitting stage 933, the signal splitting occurs after the source second stage amplifier 976a. Thus, the outputs of the source second stage amplifier 976a may be input to the passive mixers 856c-d to obtain the target inphase signals 980e-f and the target quadrature signals 980g-h.

[0090] Switches may be used between the source low noise amplifier (LNA) 978a and the target low noise amplifier (LNA) 978b to allow a clean standalone operation. The low noise amplifier (LNA) topology may drive the signal splitting sensing point.

[0091] Figure 10 illustrates certain components that may be included within a wireless communication device 1004. The wireless communication device 1004 may be an access terminal, a mobile station, a user equipment (UE), etc. The wireless communication device 1004 includes a processor 1003. The processor 1003 may be a general purpose single- or multi-chip microprocessor (e.g., an ARM), a special purpose microprocessor (e.g., a digital signal processor (DSP)), a microcontroller, a programmable gate array, etc. The processor 1003 may be referred to as a central processing unit (CPU). Although just a single processor 1003 is shown in the wireless

communication device 1004 of Figure 10, in an alternative configuration, a combination of processors (e.g., an ARM and DSP) could be used.

[0092] The wireless communication device 1004 also includes memory 1005. The memory 1005 may be any electronic component capable of storing electronic information. The memory 1005 may be embodied as random access memory (RAM), read-only memory (ROM), magnetic disk storage media, optical storage media, flash memory devices in RAM, on-board memory included with the processor, EPROM memory, EEPROM memory, registers and so forth, including combinations thereof.

[0093] Data 1007a and instructions 1009a may be stored in the memory 1005. The instructions 1009a may be executable by the processor 1003 to implement the methods disclosed herein. Executing the instructions 1009a may involve the use of the data 1007a that is stored in the memory 1005. When the processor 1003 executes the instructions 1009, various portions of the instructions 1009b may be loaded onto the processor 1003, and various pieces of data 1007b may be loaded onto the processor 1003.

[0094] The wireless communication device 1004 may also include a transmitter 1011 and a receiver 1013 to allow transmission and reception of signals to and from the wireless communication device 1004 via a first antenna 1017a and a second antenna 1017b. The transmitter 1011 and receiver 1013 may be collectively referred to as a transceiver 1015. The wireless communication device 1004 may also include (not shown) multiple transmitters, additional antennas, multiple receivers and/or multiple transceivers.

[0095] The wireless communication device 1004 may include a digital signal processor (DSP) 1021. The wireless communication device 1004 may also include a communications interface 1023. The communications interface 1023 may allow a user to interact with the wireless communication device 1004.

[0096] The various components of the wireless communication device 1004 may be coupled together by one or more buses, which may include a power bus, a control signal bus, a status signal bus, a data bus, etc. For the sake of clarity, the various buses are illustrated in Figure 15 as a bus system 1019.

[0097] The term "determining" encompasses a wide variety of actions and, therefore, "determining" can include calculating, computing, processing, deriving,

investigating, looking up (e.g., looking up in a table, a database or another data structure), ascertaining and the like. Also, "determining" can include receiving (e.g., receiving information), accessing (e.g., accessing data in a memory) and the like. Also, "determining" can include resolving, selecting, choosing, establishing and the like.

[0098] The phrase "based on" does not mean "based only on," unless expressly specified otherwise. In other words, the phrase "based on" describes both "based only on" and "based at least on."

[0099] The term "processor" should be interpreted broadly to encompass a general purpose processor, a central processing unit (CPU), a microprocessor, a digital signal processor (DSP), a controller, a microcontroller, a state machine and so forth. Under some circumstances, a "processor" may refer to an application specific integrated circuit (ASIC), a programmable logic device (PLD), a field programmable gate array (FPGA), etc. The term "processor" may refer to a combination of processing devices, e.g., a combination of a DSP and a microprocessor, a plurality of microprocessors, one or more microprocessors in conjunction with a DSP core, or any other such configuration.

[00100] The term "memory" should be interpreted broadly to encompass any electronic component capable of storing electronic information. The term memory may refer to various types of processor-readable media such as random access memory (RAM), read-only memory (ROM), non-volatile random access memory (NVRAM), programmable read-only memory (PROM), erasable programmable read-only memory (EPROM), electrically erasable PROM (EEPROM), flash memory, magnetic or optical data storage, registers, etc. Memory is said to be in electronic communication with a processor if the processor can read information from and/or write information to the memory. Memory that is integral to a processor is in electronic communication with the processor.

[00101] The terms "instructions" and "code" should be interpreted broadly to include any type of computer-readable statement(s). For example, the terms "instructions" and "code" may refer to one or more programs, routines, sub-routines, functions, procedures, etc. "Instructions" and "code" may comprise a single computer-readable statement or many computer-readable statements.

[00102] The functions described herein may be implemented in hardware, software, firmware, or any combination thereof. If implemented in software, the functions may be

stored as one or more instructions on a computer-readable medium. The terms "computer-readable medium" or "computer-program product" refers to any available medium that can be accessed by a computer. By way of example, and not limitation, a computer-readable medium may comprise RAM, ROM, EEPROM, CD-ROM or other optical disk storage, magnetic disk storage or other magnetic storage devices, or any other medium that can be used to carry or store desired program code in the form of instructions or data structures and that can be accessed by a computer. Disk and disc, as used herein, includes compact disc (CD), laser disc, optical disc, digital versatile disc (DVD), floppy disk and Blu-ray® disc where disks usually reproduce data magnetically, while discs reproduce data optically with lasers.

[00103] Software or instructions may also be transmitted over a transmission medium. For example, if the software is transmitted from a website, server, or other remote source using a coaxial cable, fiber optic cable, twisted pair, digital subscriber line (DSL), or wireless technologies such as infrared, radio and microwave, then the coaxial cable, fiber optic cable, twisted pair, DSL, or wireless technologies such as infrared, radio and microwave are included in the definition of transmission medium.

[00104] The methods disclosed herein comprise one or more steps or actions for achieving the described method. The method steps and/or actions may be interchanged with one another without departing from the scope of the claims. In other words, unless a specific order of steps or actions is required for proper operation of the method that is being described, the order and/or use of specific steps and/or actions may be modified without departing from the scope of the claims.

[00105] Further, it should be appreciated that modules and/or other appropriate means for performing the methods and techniques described herein, such as those illustrated by Figure 2, can be downloaded and/or otherwise obtained by a device. For example, a device may be coupled to a server to facilitate the transfer of means for performing the methods described herein. Alternatively, various methods described herein can be provided via a storage means (e.g., random access memory (RAM), read-only memory (ROM), a physical storage medium such as a compact disc (CD) or floppy disk, etc.), such that a device may obtain the various methods upon coupling or providing the storage means to the device. Moreover, any other suitable technique for providing the methods and techniques described herein to a device can be utilized.

[00106] It is to be understood that the claims are not limited to the precise configuration and components illustrated above. Various modifications, changes and variations may be made in the arrangement, operation and details of the systems, methods and apparatus described herein without departing from the scope of the claims.

[00107] What is claimed is:

CLAIMS

1. A wireless communication device configured for receiving a multiple carrier signal, comprising:

a single-chip signal splitting carrier aggregation receiver architecture that comprises:

a primary antenna;

a secondary antenna; and

a transceiver chip, wherein the single-chip signal splitting carrier aggregation receiver architecture reuses a simultaneous hybrid dual receiver path.

2. The wireless communication device of claim 1, wherein the single-chip signal splitting carrier aggregation receiver architecture does not require four antennas, a power splitter, an external low noise amplifier or die-to-die signal routing.

3. The wireless communication device of claim 1, wherein the transceiver chip comprises:

a transmitter;

a primary receiver;

a secondary receiver;

a tertiary receiver; and

a quaternary receiver, wherein each receiver comprises multiple low noise amplifiers, and wherein each low noise amplifier comprises a first stage amplifier and a second stage amplifier.

4. The wireless communication device of claim 3, wherein the first stage amplifier is a transconductance stage, and wherein the second stage amplifier is a cascode stage.

5. The wireless communication device of claim 3, wherein the multiple low noise amplifiers comprise multiple low noise amplifiers for a first band and multiple low noise amplifiers for a second band.

6. The wireless communication device of claim 5, wherein the first band is a low band and the second band is a mid band.

7. The wireless communication device of claim 5, wherein the first band is a low band and the second band is a high band.

8. The wireless communication device of claim 5, wherein the first band is a mid band and the second band is a high band.

9. The wireless communication device of claim 3, wherein a first routing is used from the primary antenna through the primary receiver to obtain a primary inphase/quadrature signal, wherein a second routing is used from the primary antenna through the tertiary receiver to obtain a TRx inphase/quadrature signal, wherein a third routing is used from the secondary antenna through the secondary receiver to obtain a secondary inphase/quadrature signal, and wherein a fourth routing is used from the secondary antenna through the quaternary receiver to obtain a QRx inphase/quadrature signal.

10. The wireless communication device of claim 9, wherein the single-chip signal splitting carrier aggregation receiver architecture is in inter-band operation, wherein the first routing passes through a first primary receiver low noise amplifier, wherein the second routing passes through a second primary receiver low noise amplifier, wherein the second routing passes through a first signal splitting stage, wherein the third routing passes through a first secondary receiver low noise amplifier, wherein the fourth routing passes through a second secondary receiver low noise amplifier, and wherein the fourth routing passes through a second signal splitting stage.

11. The wireless communication device of claim 10, wherein the first signal splitting stage comprises a routing between a first stage amplifier in a low noise amplifier of the primary receiver and a second stage amplifier in a low noise amplifier of the tertiary receiver.

12. The wireless communication device of claim 10, wherein the second signal splitting stage comprises a routing between a first stage amplifier in a low noise amplifier of the secondary receiver and a second stage amplifier in a low noise amplifier of the quaternary receiver.

13. The wireless communication device of claim 10, wherein the first signal splitting stage comprises a routing between a second stage amplifier in a low noise amplifier of the primary receiver and a mixer in the tertiary receiver.

14. The wireless communication device of claim 10, wherein the second signal splitting stage comprises a routing between a second stage amplifier in a low noise amplifier of the secondary receiver and a mixer in the quaternary receiver.

15. The wireless communication device of claim 9, wherein the single-chip signal splitting carrier aggregation receiver architecture is in intra-band operation, wherein the first routing and the second routing pass through a primary receiver low noise amplifier, wherein the second routing passes through a first signal splitting stage, wherein the third routing and the fourth routing pass through a secondary receiver low noise amplifier, and wherein the fourth routing passes through a second signal splitting stage.

16. The wireless communication device of claim 15, wherein the first signal splitting stage comprises a routing between a first stage amplifier in a low noise amplifier of the primary receiver and a second stage amplifier in a low noise amplifier of the tertiary receiver.

17. The wireless communication device of claim 15, wherein the second signal splitting stage comprises a routing between a first stage amplifier in a low noise amplifier of the secondary receiver and a second stage amplifier in a low noise amplifier of the quaternary receiver.

18. The wireless communication device of claim 15, wherein the first signal splitting stage comprises a routing between a second stage amplifier in a low noise amplifier of the primary receiver and a mixer in the tertiary receiver.

19. The wireless communication device of claim 15, wherein the second signal splitting stage comprises a routing between a second stage amplifier in a low noise amplifier of the secondary receiver and a mixer in the quaternary receiver.

20. A method for receiving a multiple carrier signal using a single-chip signal splitting carrier aggregation receiver architecture, comprising:

receiving a first signal using a primary antenna;

routing the first signal through a primary receiver on a transceiver chip in the single-chip signal splitting carrier aggregation receiver architecture to obtain a primary inphase/quadrature signal;

routing the first signal through a tertiary receiver on the transceiver chip to obtain a TRx inphase/quadrature signal;

receiving a second signal using a secondary antenna;

routing the second signal through a secondary receiver on the transceiver chip to obtain a secondary inphase/quadrature signal; and

routing the second signal through a quaternary receiver on the transceiver chip to obtain a QRx inphase/quadrature signal.

21. The method of claim 20 wherein the single-chip signal splitting carrier aggregation receiver architecture does not require four antennas, a power splitter, an external low noise amplifier or die-to-die signal routing.

22. The method of claim 20, wherein the transceiver chip comprises:

a transmitter;

a primary receiver;

a secondary receiver;

a tertiary receiver; and

a quaternary receiver, wherein each receiver comprises multiple low noise amplifiers, and wherein each low noise amplifier comprises a first stage amplifier and a second stage amplifier.

23. The method of claim 22, wherein the first stage amplifier is a transconductance stage, and wherein the second stage amplifier is a cascode stage.

24. The method of claim 22, wherein the multiple low noise amplifiers comprise multiple low noise amplifiers for a first band and multiple low noise amplifiers for a second band.

25. The method of claim 24, wherein the first band is a low band and the second band is a mid band.

26. The method of claim 24, wherein the first band is a low band and the second band is a high band.

27. The method of claim 24, wherein the first band is a mid band and the second band is a high band.

28. The method of claim 22, wherein a first routing is used from the primary antenna through the primary receiver to obtain a primary inphase/quadrature signal, wherein a second routing is used from the primary antenna through the tertiary receiver to obtain a TRx inphase/quadrature signal, wherein a third routing is used from the secondary antenna through the secondary receiver to obtain a secondary inphase/quadrature signal, and wherein a fourth routing is used from the secondary antenna through the quaternary receiver to obtain a QRx inphase/quadrature signal.

29. The method of claim 28, wherein the single-chip signal splitting carrier aggregation receiver architecture is in inter-band operation, wherein the first routing passes through a first primary receiver low noise amplifier, wherein the second routing passes through a second primary receiver low noise amplifier, wherein the second routing passes through a first signal splitting stage, wherein the third routing passes through a first secondary receiver low noise amplifier, wherein the fourth routing passes through a second secondary receiver low noise amplifier, and wherein the fourth routing passes through a second signal splitting stage.

30. The method of claim 29, wherein the first signal splitting stage comprises a routing between a first stage amplifier in a low noise amplifier of the primary receiver and a second stage amplifier in a low noise amplifier of the tertiary receiver.

31. The method of claim 29, wherein the second signal splitting stage comprises a routing between a first stage amplifier in a low noise amplifier of the secondary receiver and a second stage amplifier in a low noise amplifier of the quaternary receiver.

32. The method of claim 29, wherein the first signal splitting stage comprises a routing between a second stage amplifier in a low noise amplifier of the primary receiver and a mixer in the tertiary receiver.

33. The method of claim 29, wherein the second signal splitting stage comprises a routing between a second stage amplifier in a low noise amplifier of the secondary receiver and a mixer in the quaternary receiver.

34. The method of claim 28, wherein the single-chip signal splitting carrier aggregation receiver architecture is in intra-band operation, wherein the first routing and the second routing pass through a primary receiver low noise amplifier, wherein the second routing passes through a first signal splitting stage, wherein the third routing and the fourth routing pass through a secondary receiver low noise amplifier, and wherein the fourth routing passes through a second signal splitting stage.

35. The method of claim 34, wherein the first signal splitting stage comprises a routing between a first stage amplifier in a low noise amplifier of the primary receiver and a second stage amplifier in a low noise amplifier of the tertiary receiver.

36. The method of claim 34, wherein the second signal splitting stage comprises a routing between a first stage amplifier in a low noise amplifier of the secondary receiver and a second stage amplifier in a low noise amplifier of the quaternary receiver.

37. The method of claim 34, wherein the first signal splitting stage comprises a routing between a second stage amplifier in a low noise amplifier of the primary receiver and a mixer in the tertiary receiver.

38. The method of claim 34, wherein the second signal splitting stage comprises a routing between a second stage amplifier in a low noise amplifier of the secondary receiver and a mixer in the quaternary receiver.

39. An apparatus for receiving a multiple carrier signal using a single-chip signal splitting carrier aggregation receiver architecture, comprising:

means for receiving a first signal;

means for routing the first signal through a primary receiver on a transceiver chip in the single-chip signal splitting carrier aggregation receiver architecture to obtain a primary inphase/quadrature signal;

means for routing the first signal through a tertiary receiver on the transceiver chip to obtain a TRx inphase/quadrature signal;

means for receiving a second signal;

means for routing the second signal through a secondary receiver on the transceiver chip to obtain a secondary inphase/quadrature signal; and

means for routing the second signal through a quaternary receiver on the transceiver chip to obtain a QRx inphase/quadrature signal.

40. The apparatus of claim 39 wherein the single-chip signal splitting carrier aggregation receiver architecture does not require four antennas, a power splitter, an external low noise amplifier or die-to-die signal routing.

41. The apparatus of claim 39, wherein the transceiver chip comprises:

a transmitter;

a primary receiver;

a secondary receiver;

a tertiary receiver; and

a quaternary receiver, wherein each receiver comprises multiple low noise amplifiers, and wherein each low noise amplifier comprises a first stage amplifier and a second stage amplifier.

42. The apparatus of claim 41, wherein the first stage amplifier is a transconductance stage, and wherein the second stage amplifier is a cascode stage.

43. The apparatus of claim 41, wherein the multiple low noise amplifiers comprise multiple low noise amplifiers for a first band and multiple low noise amplifiers for a second band.

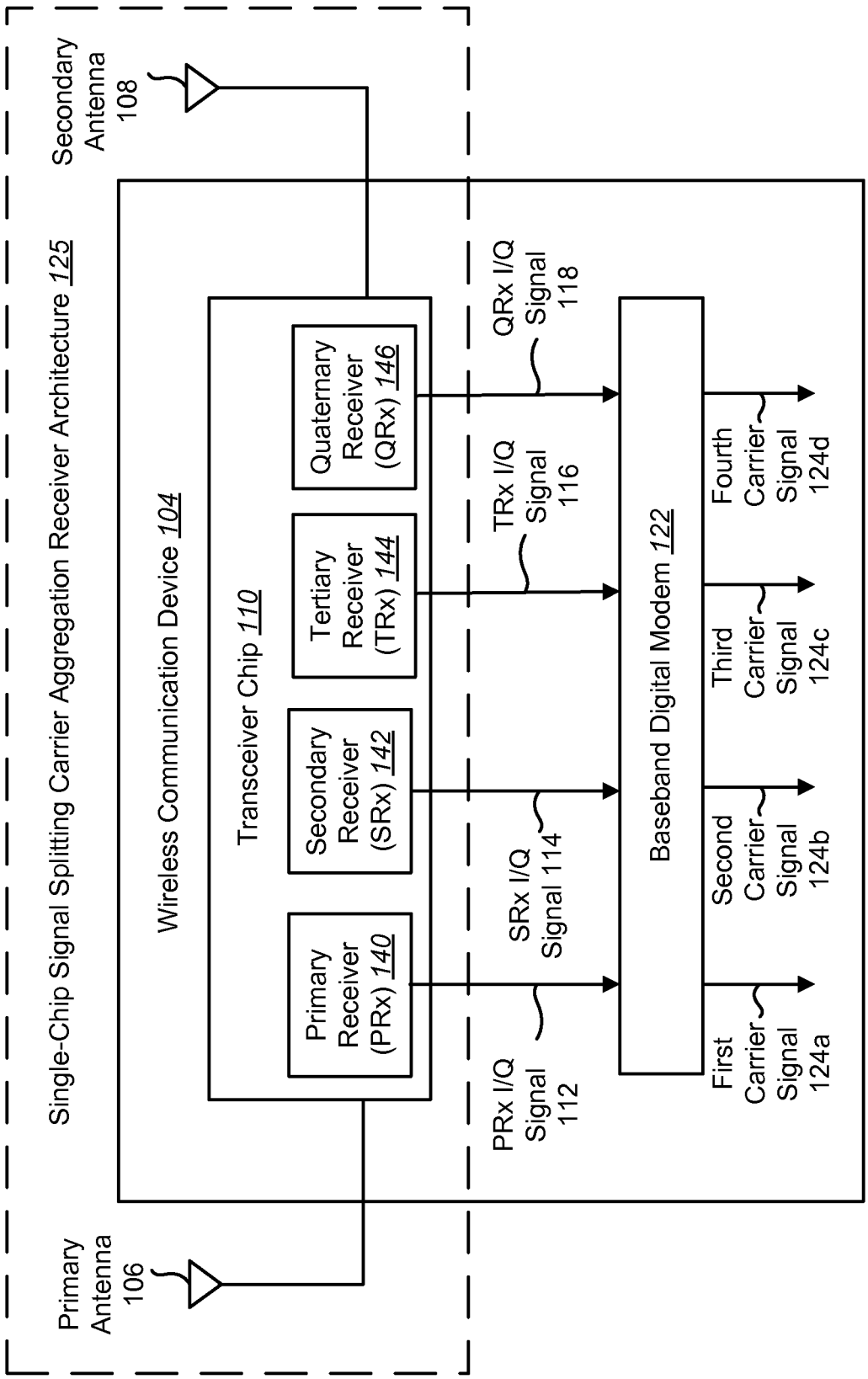
Single-Chip Signal Splitting Carrier Aggregation Receiver Architecture 125
Primary Antenna 106
Secondary Antenna 108
Wireless Communication Device 104
Transceiver Chip 110
Primary Receiver (PRx) 140
Secondary Receiver (SRx) 142
Tertiary Receiver (TRx) 144
Quaternary Receiver (QRx) 146
PRx I/Q Signal 112
SRx I/Q Signal 114
TRx I/Q Signal 116
QRx I/Q Signal 118
Baseband Digital Modem 122
First Carrier Signal 124a
Second Carrier Signal 124b
Third Carrier Signal 124c
Fourth Carrier Signal 124d

FIG. 1

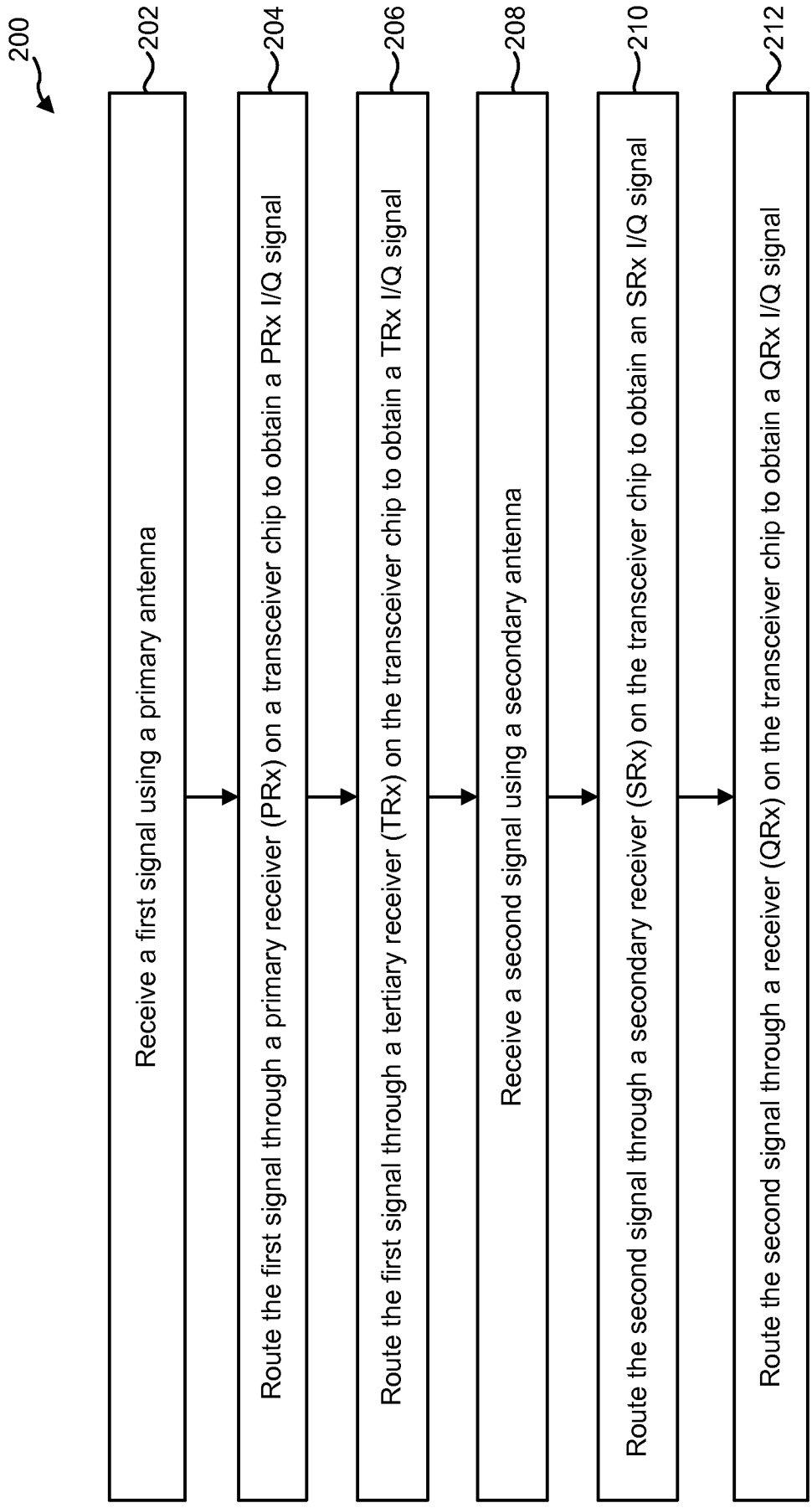
200
202
Receive a first signal using a primary antenna
204
Route the first signal through a primary receiver (PRx) on a transceiver chip to obtain a PRx I/Q signal
206
Route the first signal through a tertiary receiver (TRx) on the transceiver chip to obtain a TRx I/Q signal
208
Receive a second signal using a secondary antenna
210
Route the second signal through a secondary receiver (SRx) on the transceiver chip to obtain an SRx I/Q signal
212
Route the second signal through a receiver (QRx) on the transceiver chip to obtain a QRx I/Q signal

FIG. 2

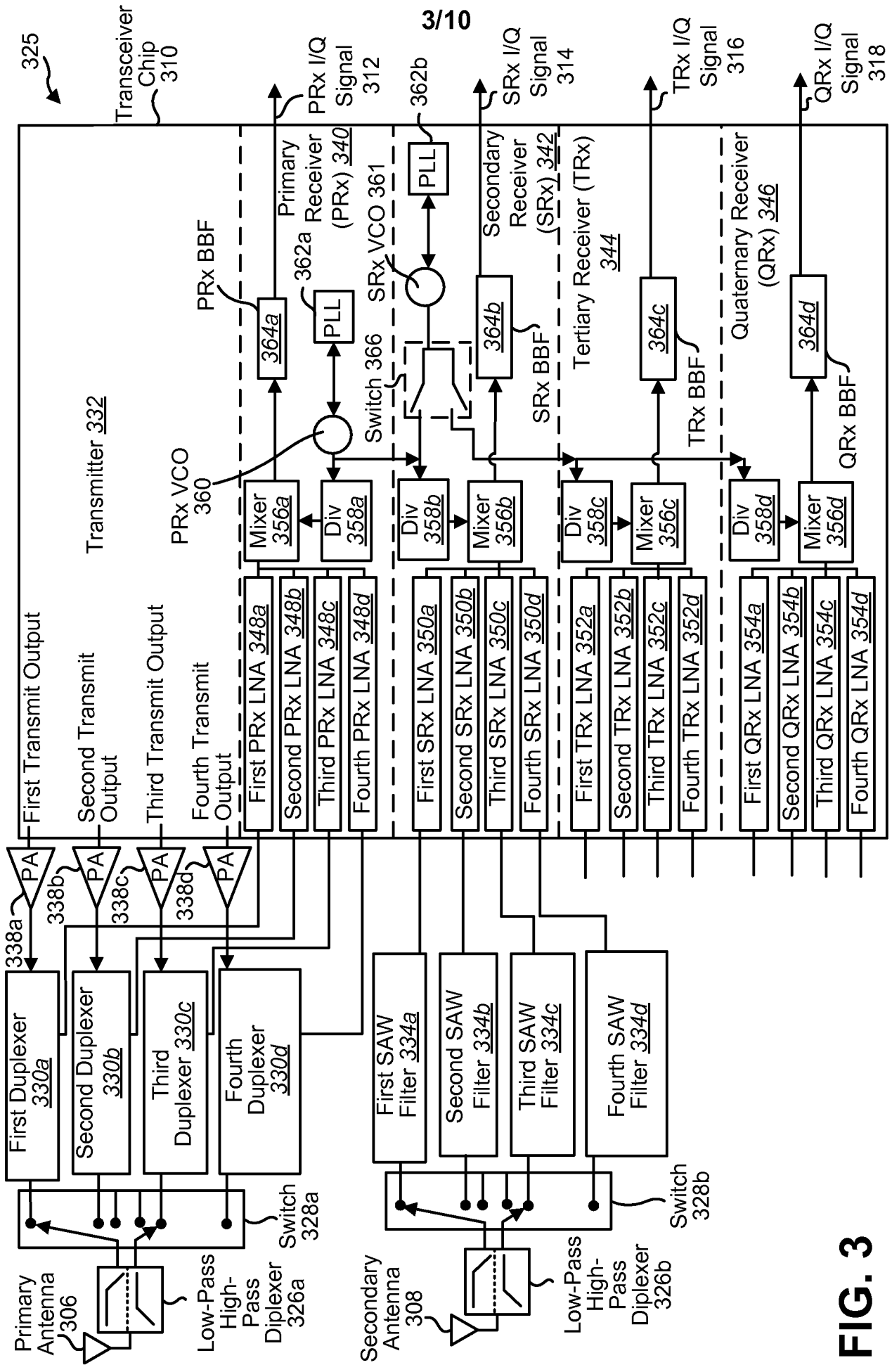
325
Transceiver Chip 310
PRx I/Q Signal 312
SRx I/Q Signal 314
TRx I/Q Signal 316
QRx I/Q Signal 318
Transmitter 332
First Transmit Output
Second Transmit Output
Third Transmit Output
Fourth Transmit Output
PA
338a
338b
338c
338d
PRx VCO 360
PRx BBF
Primary Receiver (PRx) 340
362a
PLL
SRx VCO 361
362b
Switch 366
Secondary Receiver (SRx) 342
SRx BBF
Tertiary Receiver (TRx) 344
TRx BBF
Quaternary Receiver (QRx) 346
QRx BBF
364a
364b
364c
364d
Mixer 356a
Mixer 356b
Mixer 356c
Mixer 356d
Div 358a
Div 358b
Div 358c
Div 358d
First PRx LNA 348a
Second PRx LNA 348b
Third PRx LNA 348c
Fourth PRx LNA 348d
First SRx LNA 350a
Second SRx LNA 350b
Third SRx LNA 350c
Fourth SRx LNA 350d
First TRx LNA 352a
Second TRx LNA 352b
Third TRx LNA 352c
Fourth TRx LNA 352d
First QRx LNA 354a
Second QRx LNA 354b
Third QRx LNA 354c
Fourth QRx LNA 354d
First Duplexer 330a
Second Duplexer 330b
Third Duplexer 330c
Fourth Duplexer 330d
First SAW Filter 334a
Second SAW Filter 334b
Third SAW Filter 334c
Fourth SAW Filter 334d
Switch 328a
Switch 328b
Primary Antenna 306
Secondary Antenna 308
Low-Pass High-Pass Diplexer 326a
Low-Pass High-Pass Diplexer 326b

FIG. 3

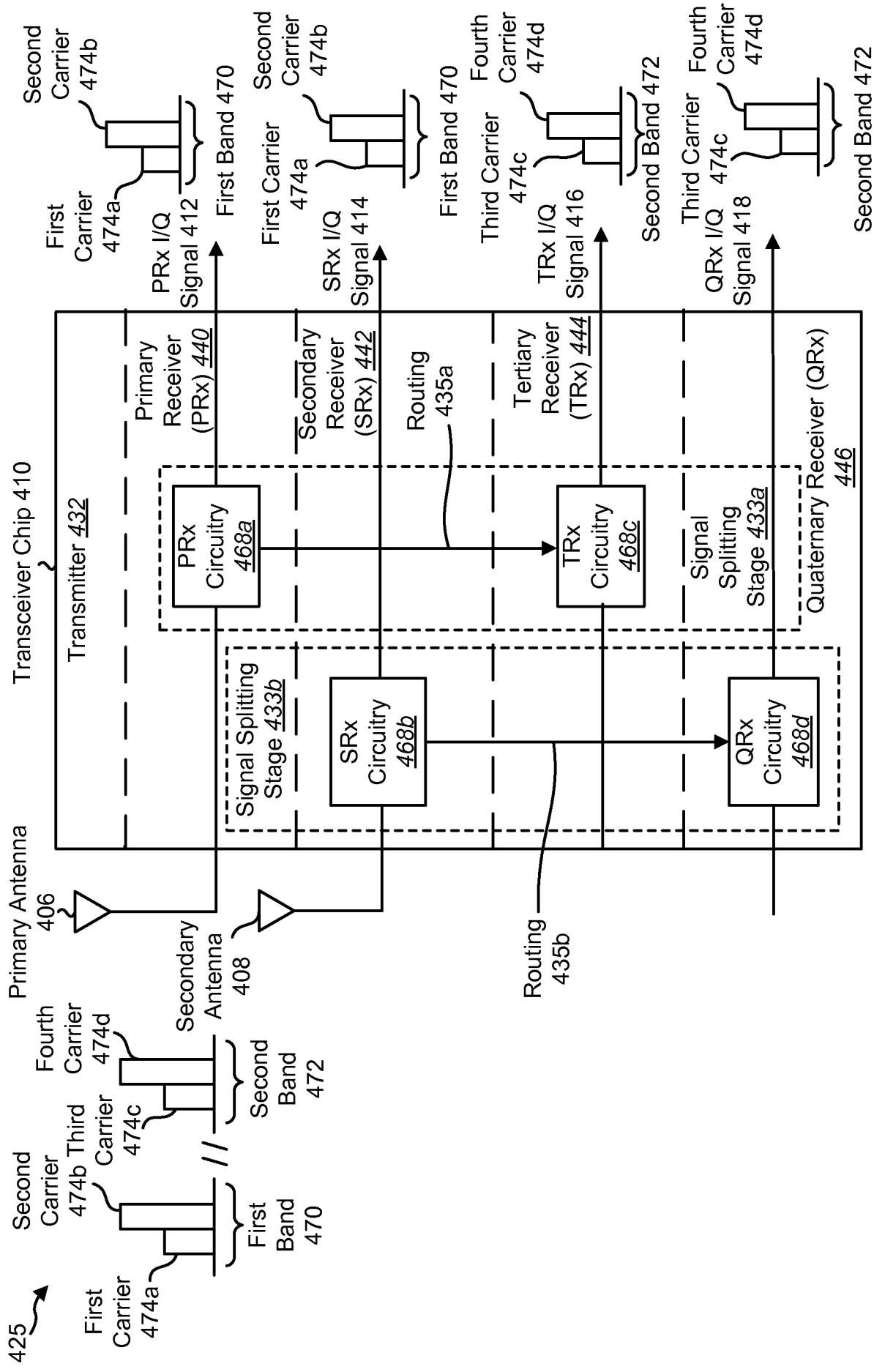
425
First Carrier 474a
Second Carrier 474b
Third Carrier 474c
Fourth Carrier 474d
First Band 470
Second Band 472
Primary Antenna 406
Secondary Antenna 408
Transceiver Chip 410
Transmitter 432
Primary Receiver (PRx) 440
Secondary Receiver (SRx) 442
Tertiary Receiver (TRx) 444
Quaternary Receiver (QRx) 446
PRx Circuitry 468a
SRx Circuitry 468b
TRx Circuitry 468c
QRx Circuitry 468d
Signal Splitting Stage 433b
Signal Splitting Stage 433a
Routing 435a
Routing 435b
PRx I/Q Signal 412
SRx I/Q Signal 414
TRx I/Q Signal 416
QRx I/Q Signal 418

FIG. 4

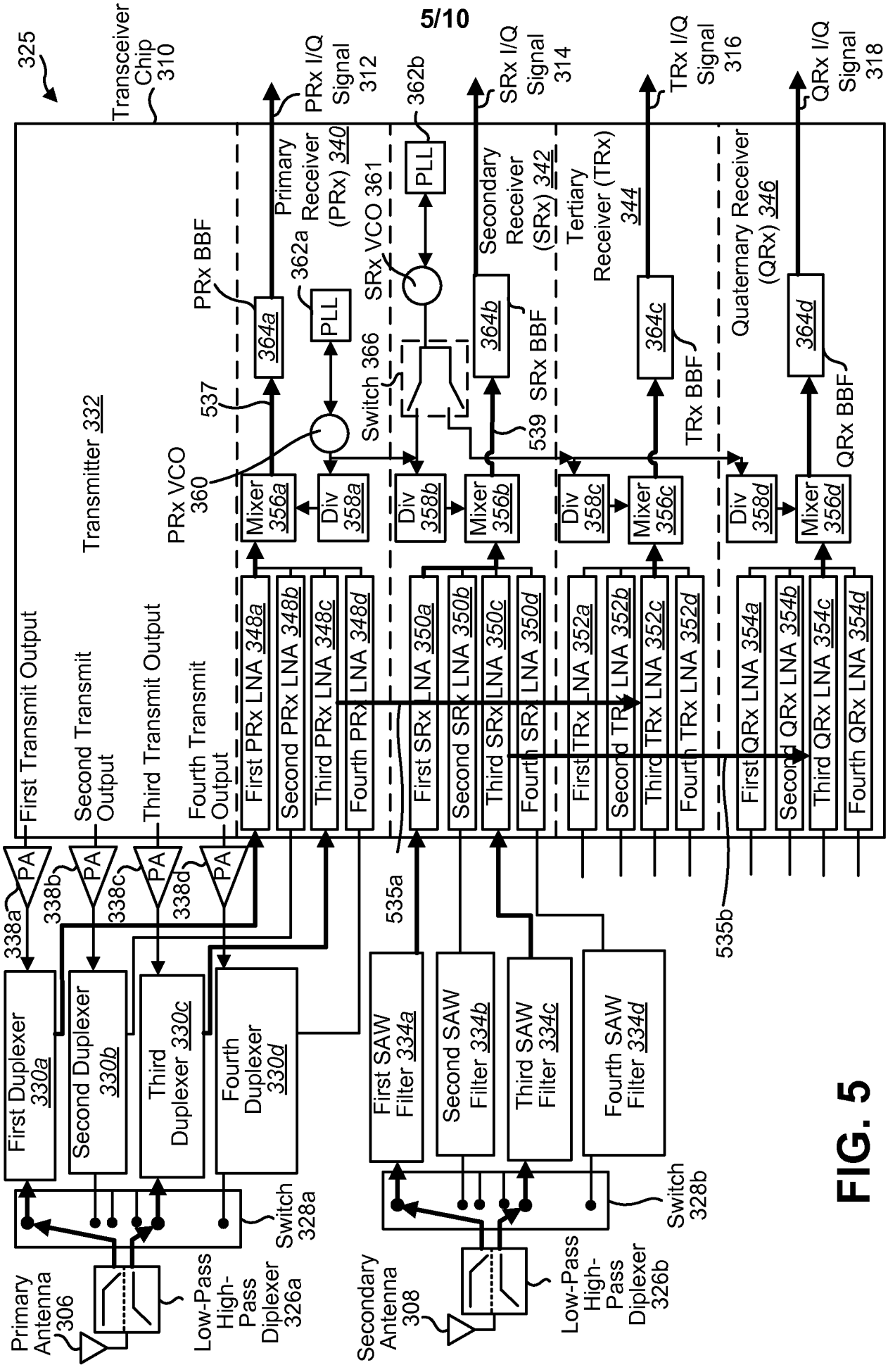
325
Transceiver Chip 310
PRx I/Q Signal 312
SRx I/Q Signal 314
TRx I/Q Signal 316
QRx I/Q Signal 318
Transmitter 332
First Transmit Output
Second Transmit Output
Third Transmit Output
Fourth Transmit Output
PRx VCO 360
PRx BBF
Primary Receiver (PRx) 340
SRx VCO 361
SRx BBF
Secondary Receiver (SRx) 342
Tertiary Receiver (TRx) 344
TRx BBF
Quaternary Receiver (QRx) 346
QRx BBF
362a
362b
537
539
Switch 366
PLL
Mixer 356a
Mixer 356b
Mixer 356c
Mixer 356d
Div 358a
Div 358b
Div 358c
Div 358d
364a
364b
364c
364d
First PRx LNA 348a
Second PRx LNA 348b
Third PRx LNA 348c
Fourth PRx LNA 348d
First SRx LNA 350a
Second SRx LNA 350b
Third SRx LNA 350c
Fourth SRx LNA 350d
First TRx LNA 352a
Second TRx LNA 352b
Third TRx LNA 352c
Fourth TRx LNA 352d
First QRx LNA 354a
Second QRx LNA 354b
Third QRx LNA 354c
Fourth QRx LNA 354d
PA 338a
PA 338b
PA 338c
PA 338d
535a
535b
First Duplexer 330a
Second Duplexer 330b
Third Duplexer 330c
Fourth Duplexer 330d
First SAW Filter 334a
Second SAW Filter 334b
Third SAW Filter 334c
Fourth SAW Filter 334d
Switch 328a
Switch 328b
Primary Antenna 306
Secondary Antenna 308
Low-Pass High-Pass Diplexer 326a
Low-Pass High-Pass Diplexer 326b

FIG. 5

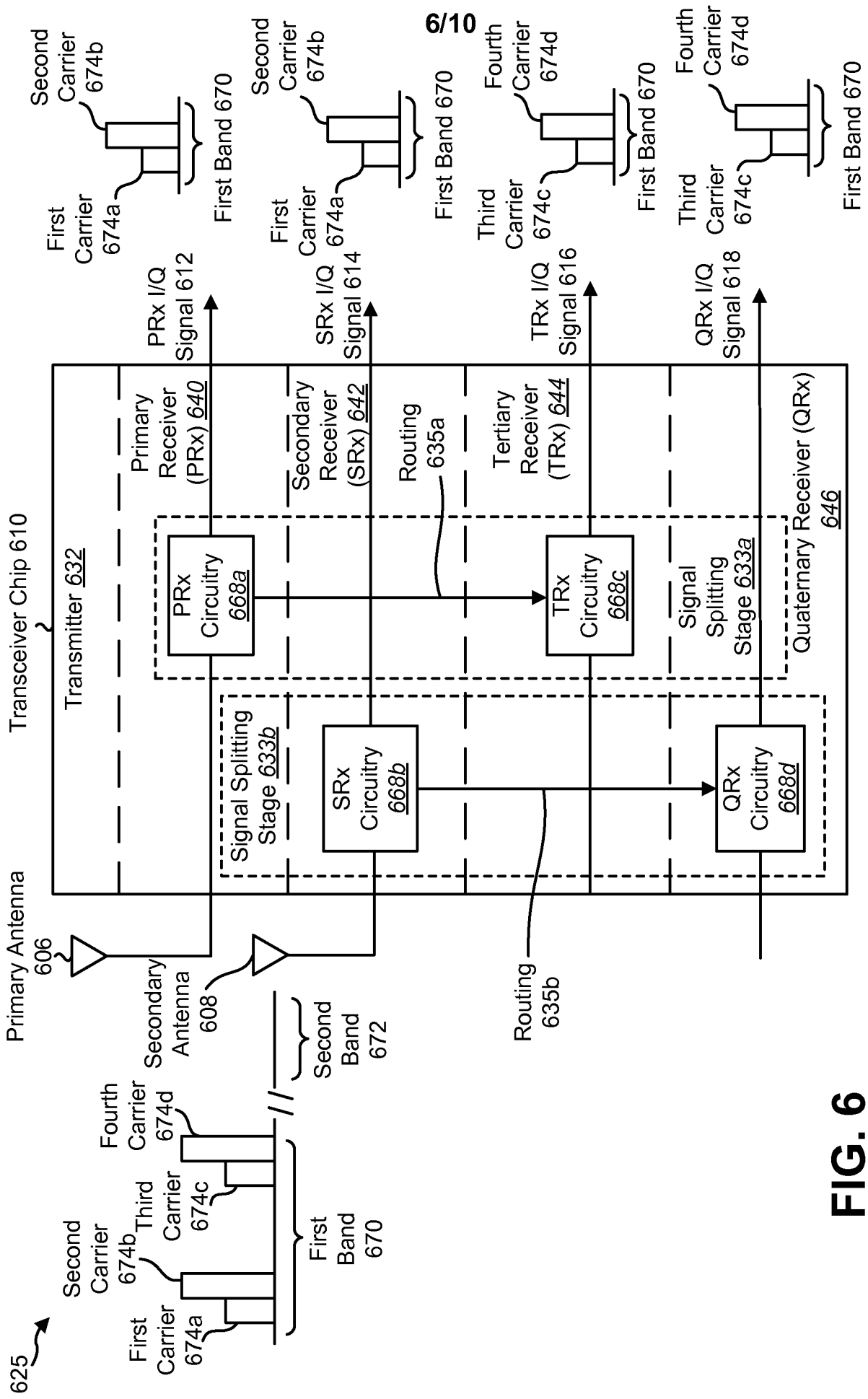
625
First Carrier 674a
Second Carrier 674b
Third Carrier 674c
Fourth Carrier 674d
First Band 670
Second Band 672
Primary Antenna 606
Secondary Antenna 608
Transceiver Chip 610
Transmitter 632
Primary Receiver (PRx) 640
Secondary Receiver (SRx) 642
Tertiary Receiver (TRx) 644
Quaternary Receiver (QRx) 646
PRx Circuitry 668a
SRx Circuitry 668b
TRx Circuitry 668c
QRx Circuitry 668d
Signal Splitting Stage 633b
Signal Splitting Stage 633a
Routing 635a
Routing 635b
PRx I/Q Signal 612
SRx I/Q Signal 614
TRx I/Q Signal 616
QRx I/Q Signal 618

FIG. 6

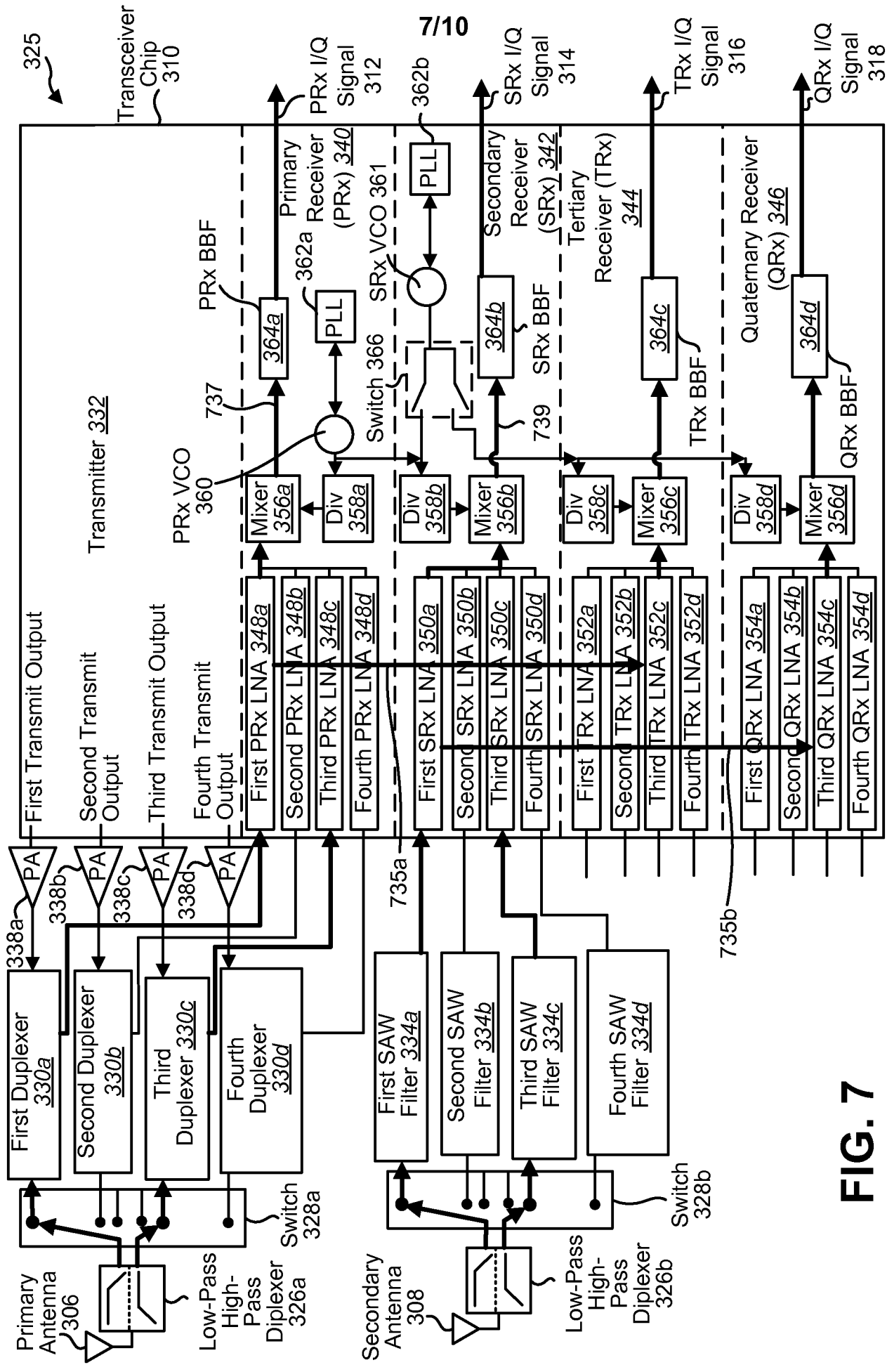
325
Transceiver Chip 310
PRx I/Q Signal 312
SRx I/Q Signal 314
TRx I/Q Signal 316
QRx I/Q Signal 318
Primary Receiver (PRx) 340
Secondary Receiver (SRx) 342
Tertiary Receiver (TRx) 344
Quaternary Receiver (QRx) 346
Transmitter 332
PRx BBF
SRx BBF
TRx BBF
QRx BBF
PRx VCO 360
SRx VCO 361
362a
362b
PLL
Switch 366
737
739
735a
735b
Mixer 356a
Mixer 356b
Mixer 356c
Mixer 356d
Div 358a
Div 358b
Div 358c
Div 358d
364a
364b
364c
364d
First Transmit Output
Second Transmit Output
Third Transmit Output
Fourth Transmit Output
First PRx LNA 348a
Second PRx LNA 348b
Third PRx LNA 348c
Fourth PRx LNA 348d
First SRx LNA 350a
Second SRx LNA 350b
Third SRx LNA 350c
Fourth SRx LNA 350d
First TRx LNA 352a
Second TRx LNA 352b
Third TRx LNA 352c
Fourth TRx LNA 352d
First QRx LNA 354a
Second QRx LNA 354b
Third QRx LNA 354c
Fourth QRx LNA 354d
PA
338a
338b
338c
338d
First Duplexer 330a
Second Duplexer 330b
Third Duplexer 330c
Fourth Duplexer 330d
First SAW Filter 334a
Second SAW Filter 334b
Third SAW Filter 334c
Fourth SAW Filter 334d
Switch 328a
Switch 328b
Primary Antenna 306
Secondary Antenna 308
Low-Pass High-Pass Diplexer 326a
Low-Pass High-Pass Diplexer 326b

FIG. 7

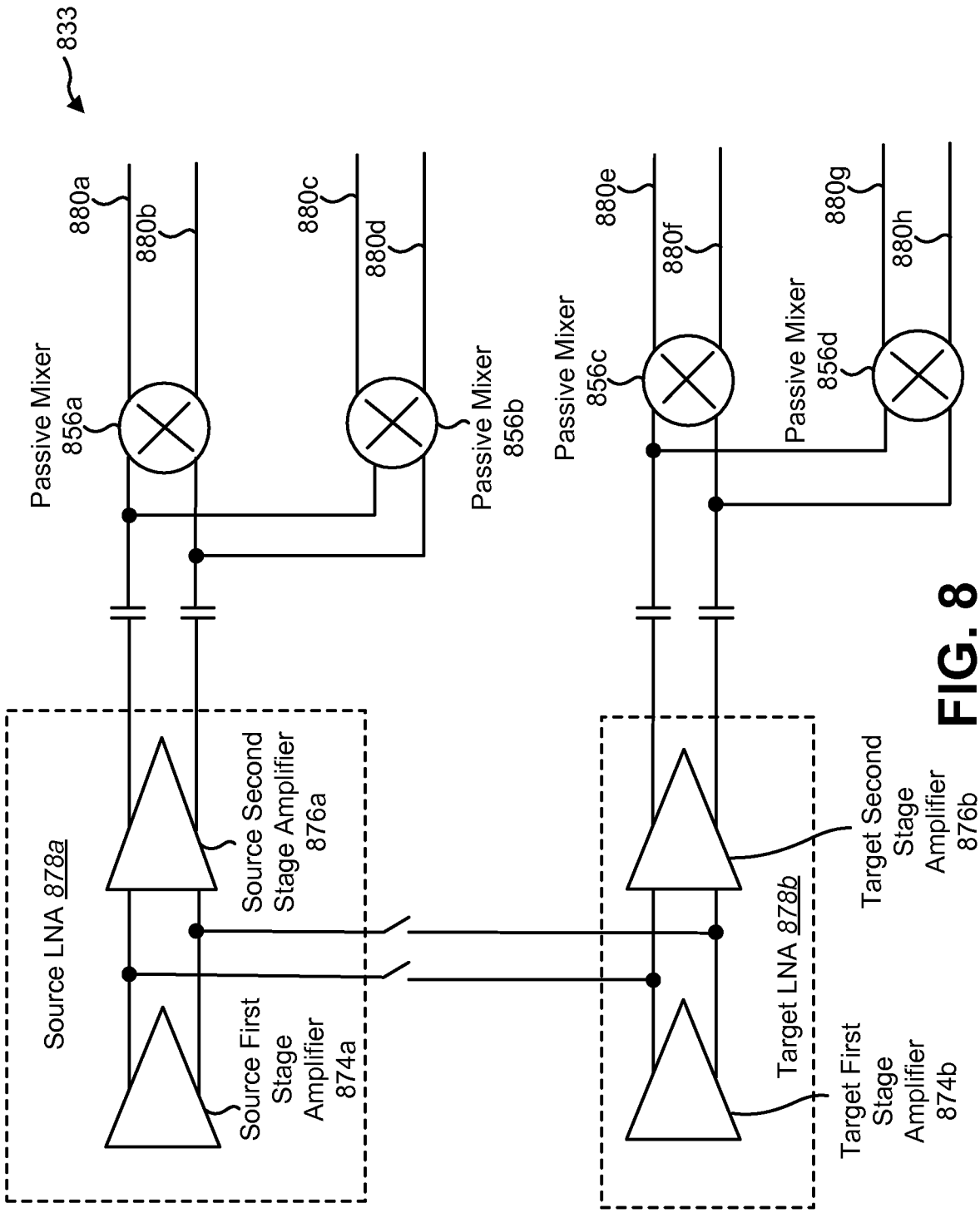
833
880a
880b
880c
880d
880e
880f
880g
880h
Passive Mixer
856a
Passive Mixer
856b
Passive Mixer
856c
Passive Mixer
856d
Source LNA 878a
Source First Stage Amplifier 874a
Source Second Stage Amplifier 876a
Target LNA 878b
Target First Stage Amplifier 874b
Target Second Stage Amplifier 876b

FIG. 8

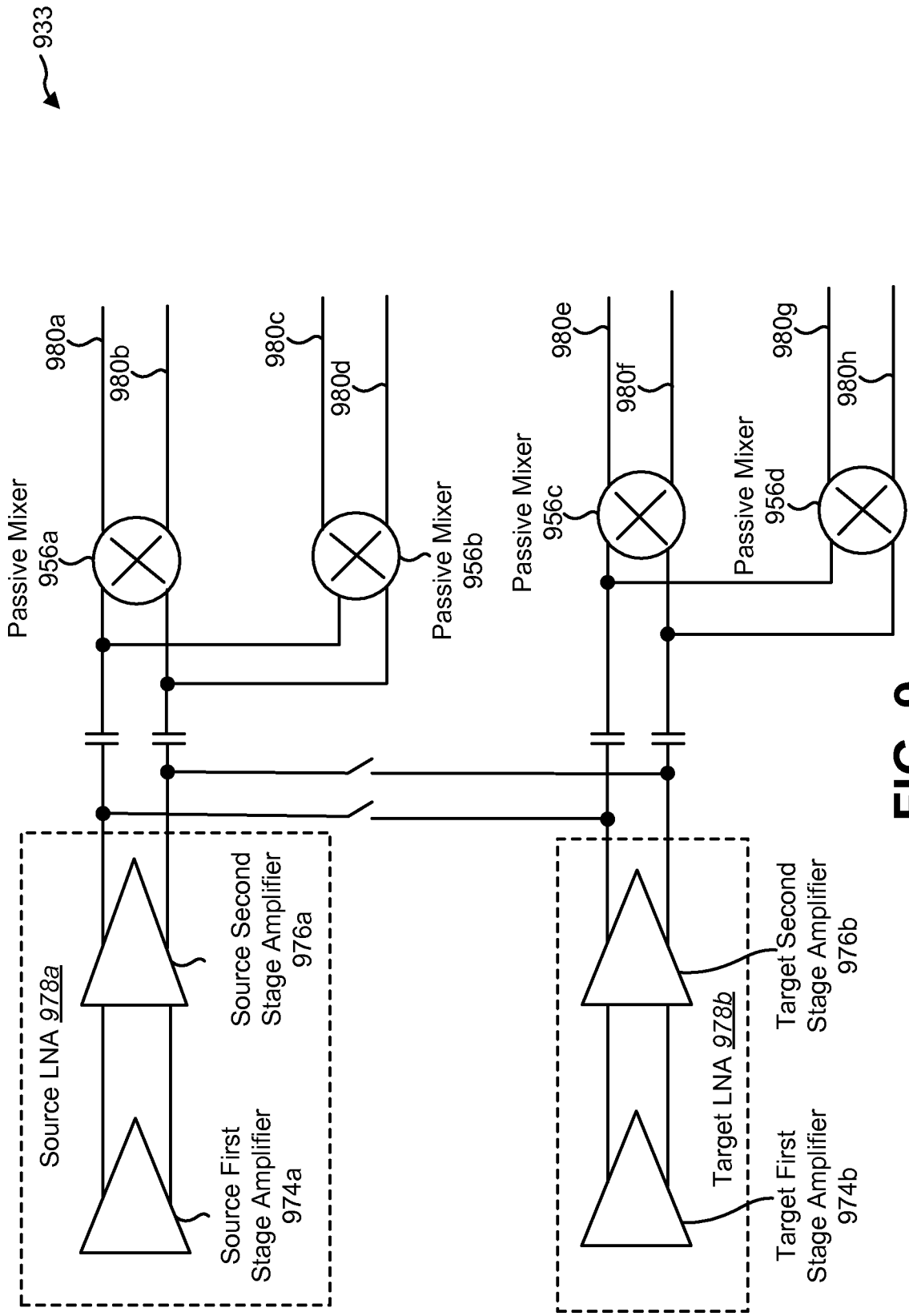
933
980a
980b
980c
980d
980e
980f
980g
980h
Passive Mixer 956a
Passive Mixer 956b
Passive Mixer 956c
Passive Mixer 956d
Source LNA 978a
Source First Stage Amplifier 974a
Source Second Stage Amplifier 976a
Target LNA 978b
Target First Stage Amplifier 974b
Target Second Stage Amplifier 976b

FIG. 9

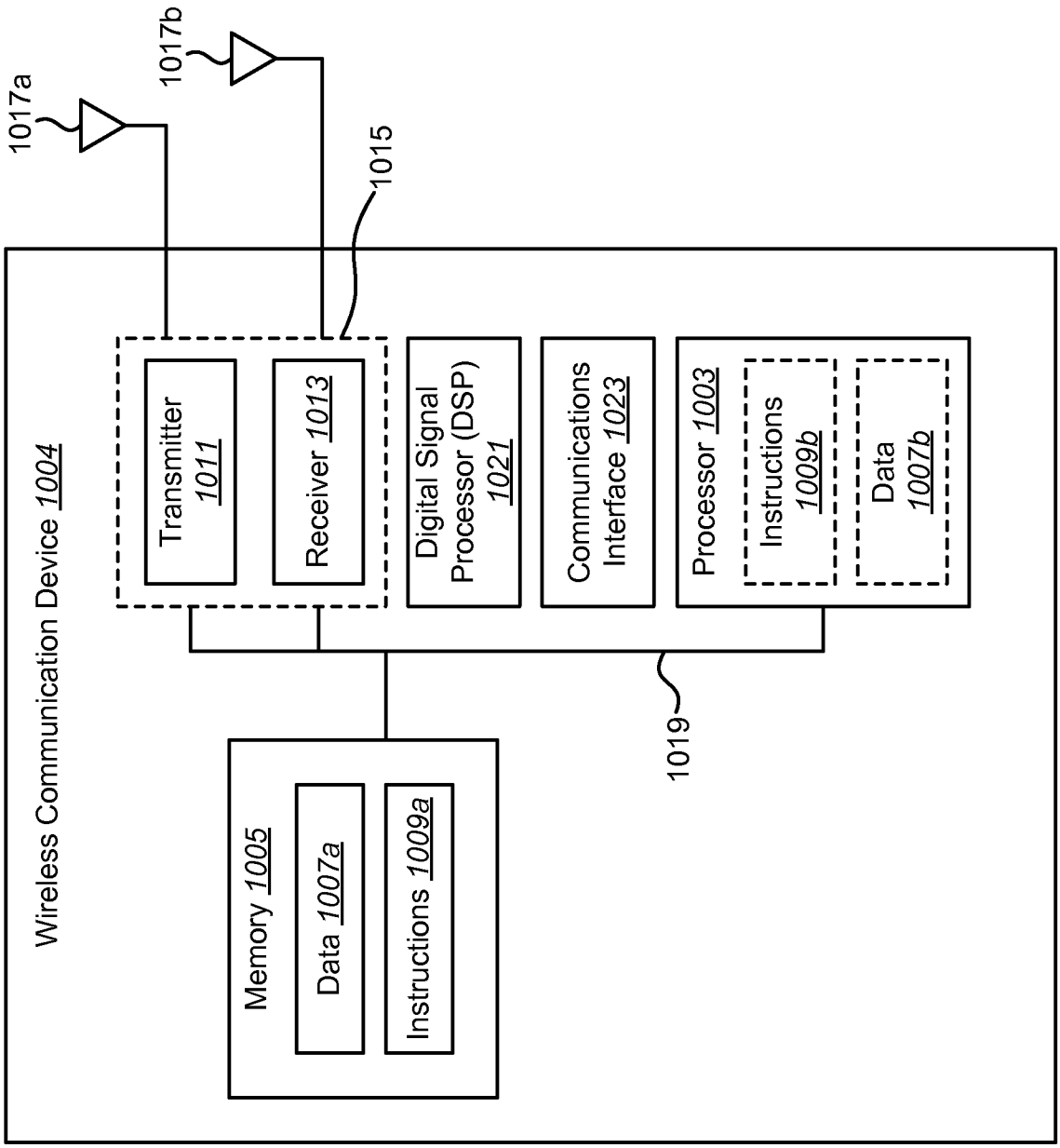
1017a
1017b
1015
Wireless Communication Device 1004
Transmitter 1011
Receiver 1013
Digital Signal Processor (DSP) 1021
Communications Interface 1023
Processor 1003
Instructions 1009b
Data 1007b
Memory 1005
Data 1007a
Instructions 1009a
1019

FIG. 10

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2013/028742

A. CLASSIFICATION OF SUBJECT MATTER
INV. H04B1/00 H04B1/48
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H04B

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal, WPI Data, COMPENDEX, INSPEC

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2010/225414 A1 (GORBACHOV OLEKSANDR [US]) 9 September 2010 (2010-09-09)	1,2
Y	paragraph [0009] - paragraph [0013] paragraph [0087] - paragraph [0093]; figure 13 paragraph [0117] - paragraph [0120]; figure 15	2-10,15, 20-29, 34,39-43

Y	CHANG-MING LAI ET AL: "Compact router transceiver architecture for carrier aggregation systems", MICROWAVE CONFERENCE (EUMC), 2011 41ST EUROPEAN, IEEE, 10 October 2011 (2011-10-10), pages 693-696, XP032072825, ISBN: 978-1-61284-235-6 the whole document	1,20,39

	-/--	

[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
4 July 2013	11/07/2013

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Giglietto, Massimo

2

Form PCT/ISA/210 (second sheet) (April 2005)

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2013/028742

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	EP 2 068 583 A1 (KYOCERA CORP [JP]) 10 June 2009 (2009-06-10) paragraph [0006] - paragraph [0017]; figure 1	1
Y	US 2009/237161 A1 (FAGG RUSSELL [US]) 24 September 2009 (2009-09-24) paragraph [0019] - paragraph [0041]; figure 1	2-10,15, 20-29, 34,39-43
X,P	WO 2012/158976 A1 (QUALCOMM INC [US]; FERNANDO UDARA C [US]) 22 November 2012 (2012-11-22) the whole document	1-43

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/US2013/028742

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2010225414 A1	09-09-2010	US 2010225414 A1	09-09-2010
		US 2010226291 A1	09-09-2010
		US 2010226292 A1	09-09-2010
		WO 2010101584 A1	10-09-2010
EP 2068583 A1	10-06-2009	CN 101523967 A	02-09-2009
		EP 2068583 A1	10-06-2009
		JP 4864625 B2	01-02-2012
		JP 2008085793 A	10-04-2008
		US 2010142440 A1	10-06-2010
		WO 2008047554 A1	24-04-2008
US 2009237161 A1	24-09-2009	AT 523957 T	15-09-2011
		CN 101978598 A	16-02-2011
		EP 2263310 A1	22-12-2010
		JP 2011515969 A	19-05-2011
		JP 2013066184 A	11-04-2013
		KR 20100127840 A	06-12-2010
		TW 200945772 A	01-11-2009
		US 2009237161 A1	24-09-2009
		WO 2009117713 A1	24-09-2009
WO 2012158976 A1	22-11-2012	US 2012294299 A1	22-11-2012
		WO 2012158976 A1	22-11-2012